Master Graduation Thesis

Micro-Fluidic MEMS

for

Micro-Particle Filtration

Delft University of Technology

Delft Institute of Microsystems and Nanoelectronics

MicroNed

Student: Li, Sheng Jie
Student no.: 1520105
Supervisor: Shen, Chenggang
Professor: Sarro, Pasqualina Maria

Date: 1 Sept 2011

Abstract

Recently there has been an onset of fluidic filters fabricated using micro electro-mechanical systems (MEMS) technology. These filters, compared to conventional ones, are more accurate and precise due to the highly sophisticated techniques that are used to define and implement the separation mechanism. In order to contribute to this new field of research, a project on micro- and nanoparticle filtration was started in the MEMS group of Delft Institute of Microsystems and Nanoelectronics. This project had grown to produce two MEMS filter designs prior to the beginning of this graduation thesis.

This thesis study seeks to identify and analyze reoccurring issues in the two MEMS filter designs and from those results, realize a new design that is superior in the aspects of performance, robustness and durability.

The first MEMS filter design proves that it is possible to create vertical membrane filtration devices using MEMS technology and seal these with dry film photo-resist. However, the first design suffers from a high flow resistance that cannot be dealt with effectively, without relying on a more area efficient design.

The second MEMS filter design is meant to outperform the first design in the aspect of flow resistance. The second design is a promising concept, but does not reach its full potential. Critical issues from a number of sources degrade and limit its performance to such a degree that it is close to dysfunctional. A redesign is necessary to fully exploit the advantageous aspects of the second design.

A third MEMS filter design was developed based on the knowledge and experience gained from the preceding designs. This third design aims to incorporate the advantages of both the first and second designs while avoiding their disadvantages. Although the third design does address and solve the problems encountered in preceding designs, the development of this design resulted in new issues that are yet to be addressed. However, despite the addition of new issues, fully functional devices for fluidic experiments could still be fabricated.

A series of fluidic experiments were performed to verify the functionality and performance of the fabricated designs. The basic filter function was hereby confirmed for all devices. Moreover, pressure and flow rate experiments were carried out to quantify the performance parameters of the filter devices. From these results, devices from the third design were found to have the best pressure and flow rate performance.

A qualitative comparison was made between the three different filter designs. This comparison considers both the structural aspects of the designs and the data gained from the fluidic experiments. Based on the comparison, the conclusion is made that the problem initially defined for this thesis has been properly addresses by the third design. Although further optimization is still possible, the third design has proven to be the best amongst the three MEMS filter designs.

Table of contents

1 Introduction

This Master graduation thesis contains research on fluidic filters designed for micro-particle filtration.

Fluidic filters can separate and sort particles based on certain distinct properties. These devices play an important role in our lives as they work behind the scenes to provide us with our day to day needs, such as clean tap water, fresh coffee and the efficient modern combustion engine.

Recently there has been an onset of fluidic filters fabricated using micro electro-mechanical systems (MEMS) technology. These filters, compared to conventional ones, are generally more accurate and precise due to the highly sophisticated techniques that are used to define and implement the separation mechanism [1-5].

In order to contribute to this relatively new field of research, a project on micro- and nanoparticle filtration was started in the MEMS group of Delft Institute of Microsystems and Nanoelectronics (DIMES). The project and group was headed by prof. dr. Pasqualina M. Sarro, while the research on micro- and nanoparticle filtration was conducted by PhD candidate Chenggang Shen. In 2010, the author of this thesis joined the research project which by that time had already grown to produce two MEMS filter designs able to perform microfiltration.

This thesis study seeks to identify and analyze reoccurring issues in the two MEMS filter designs and from those results, realize a new design that is superior in the aspects of performance, robustness and durability. Due to time constraints, the focus will be mainly on design, fabrication and preliminary testing of particle filtration. Modeling and particle sorting are therefore only briefly discussed in this thesis.

To further introduce the field of research and to position our work, the following sections define some basic terms and give a brief overview of a few separation processes that are considered to be the state of the art.

1.1 Micro-fluidics

A fluid is defined as a substance that deforms continuously under application of any non-zero amount of shear stress. Unlike a solid, a fluid retains its new shape after deformation, even when there are no more forces applied to it [6-7].

While the aforementioned definition of a fluid is shared amongst different groups of scientists, the term micro-fluidics has many different interpretations. In this thesis, the preferred definition for micro-fluidics is: The study of devices with sub-millimeter scale dimensions to which a fluid, with or without suspended particles, is geometrically constrained and manipulated in.

1.1.1 Suspended particles

For the contents of this thesis, the presence of suspended particles in a fluid is important because we are considering micro-fluidic devices meant to separate or sort particles. Therefore, unless stated otherwise, when the term fluid is used, it should be interpreted as a fluid with the addition of suspended particles of unknown but distinguishable sizes.

1.1.2 Fluid dynamics

The research in this thesis includes micro-fluidic devices with fluids in motion. The theories behind fluid dynamics were for that reason studied in order to make proper predictions and conclusions. Fluid dynamics can be fully described by the equations for the conservation of mass, momentum and energy [8]. These equations, in their general forms, are difficult to solve and can be greatly simplified when assuming that a fluid:

- Is a continuum and have properties that are constant over space and time.
- Is incompressible.
- When moving, exhibits a laminar flow which has a parabolic velocity profile.

Whether these assumptions are applicable or not, depends on the dimensions and velocities being considered. For the devices in this thesis which can hold volumes in the order of nanoliters and has volumetric flow rates in the order of microliters per minute, the assumptions above can be assumed applicable [6-8]. Fluid dynamics is discussed in more detail in Chapter 5.

1.2 Liquid chromatography

Liquid chromatography (LC) is a well-known and commonly used separation principle. It is globally applied in many different forms for high volume purification and sample analysis.

Most LC processes function based on subtle variations in the affinities of mobile particles when subjected to a certain stationary medium [9]. While traversing the medium, different suspended particles in a fluid undergo different rates of transitions between immobile and mobile phases which resolve in distinguishable propagation times for each unique particle. The separation principle of LC is illustrated in Figure 1.1.

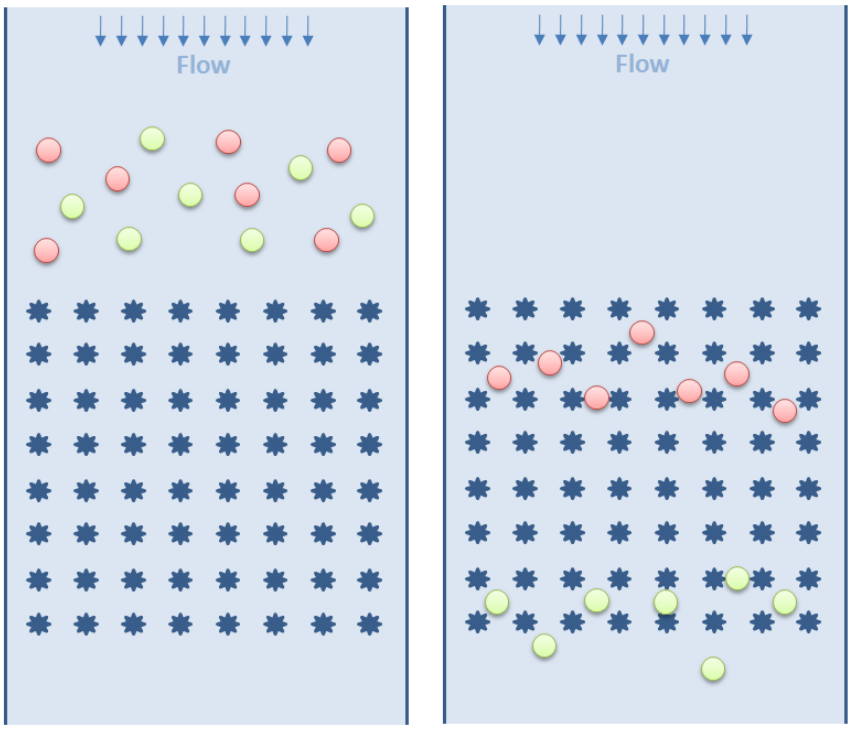


Figure 1.1: Illustration of liquid chromatography.
Initial state (left) and after a period of time (right).

1.2.1 Field flow fractionation

Field flow fractionation (FFF) is a more disassociated class of LC, because its separation processes are based on a slightly different principle as it conveniently lacks the immobile phase [10-12].

In FFF, a force field is applied perpendicularly to a fluid flow. The force field directionally displaces the suspended particles in the fluid while natural diffusion counters this displacement. The magnitude of the counteraction is a function of particle dimensions, hence size based spatial separation of particles occurs when the forces reaches an equilibrium. To further the separation, FFF exploits the parabolic velocity profile present in laminar flows to convert the spatial separation into a dominant temporal separation. This is favorable for the detection as components will continue to separate over time.

Different types of force fields can be applied to a fluid in order to agitate a displacement response in the suspended particles. Two common FFF field types are discussed in the following subsections.

1.2.2 Electrical field flow fractionation

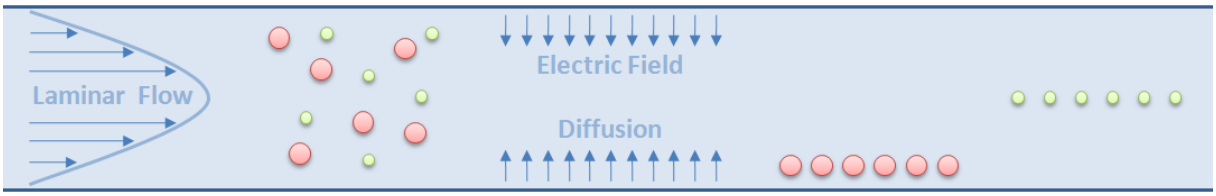


Figure 1.2: Illustration of electrical field flow fractionation.
Initial state (left) and after a period of time (right).

The separation mechanism of electrical field flow fractionation (EFFF) is depicted in Figure 1.2. An electric field is perpendicularly applied to a channel in which a fluid flows. As a result of the electric field, the suspended particles in the fluid will migrate towards the channel boundary according to a specific electrophoretic mobility. This is the phenomenon of electrophoresis (Equation 1.1).

$$x = \frac{\varepsilon_r \varepsilon_0 \zeta}{\eta} \cdot E \cdot t = \mu_e \cdot E \cdot t$$

Equation 1.1: Electrophoresis with x the displacement, ε_r the dielectric constant, ε_0 the permittivity of free space, ζ the zeta potential, η the dynamic viscosity, μ_e the electrophoretic mobility, E the electric field strength and t the time.

The displacement due to electrophoresis is counteracted by a natural diffusive force. This force can be modeled by the Einstein-Stokes equation (Equation 1.2) which states that smaller particles have a longer diffusion path than larger particles. Particles of small radii can therefore stray further from the channel boundary per unit time and reach equilibrium nearer to the center of the channel.

$$D = \frac{k_B \cdot T}{6 \cdot \pi \cdot \eta \cdot r}$$

Equation 1.2: Einstein-Stokes with D the diffusion constant, k_B the Boltzmann's constant, T the absolute temperature, η the fluid dynamic viscosity and r the particle radius.

Laminar flow is characterized by a parabolic velocity distribution present in the fluid channel. Fluid velocities at the channel boundaries are zero while maximum in the center. With the addition of laminar flow, the particles present at different distances from the channel boundary will travel at different velocities and exit the channel at distinct times, resulting in temporal separation.

1.2.3 Asymmetric flow field flow fractionation

Asymmetric flow field flow fractionation (AF4) can separate particles without an electrophoretic mobility (Figure 1.3). A semi-permeable membrane, impervious for suspended particles, but transparent for the carrier fluid, causes a cross flow inside the separation channel. Together with natural diffusion and a laminar flow, separation is achieved over time.

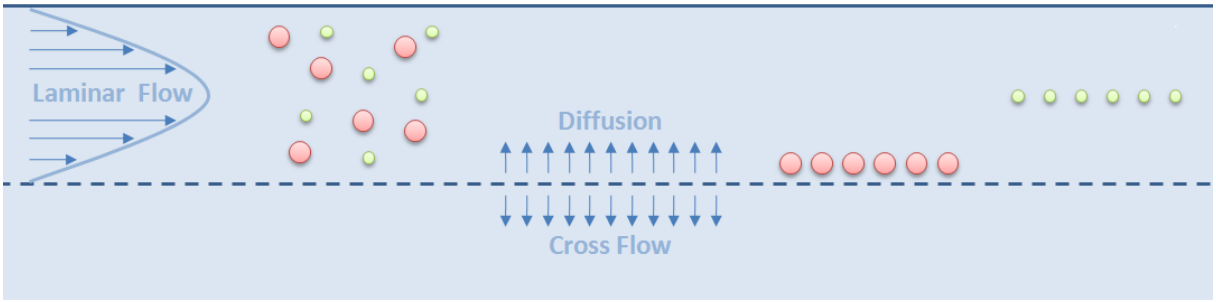


Figure 1.3: Illustration of asymmetric flow field flow fractionation.
Initial state (left) and after a period of time (right).

1.3 Membrane filtration

Membrane filtration (MF) is a very straightforward separation principle based on size exclusion. A common configuration to perform MF is dead-end filtration (Figure 1.4) where a membrane with well-defined openings, called pores, is used to selectively obstruct all particles in a flowing fluid that are larger than the pore dimensions.

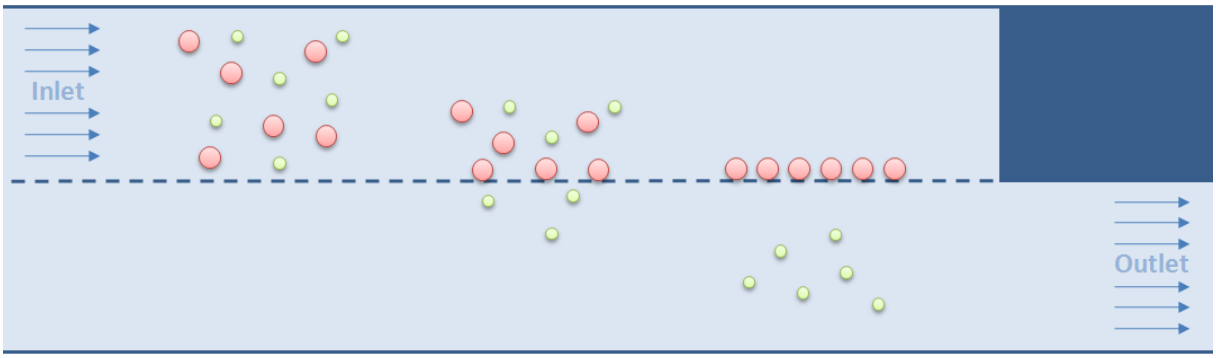


Figure 1.4: Illustration of dead-end membrane filtration.

MF can be divided, according to pore sizes, into the following categories: conventional filtration, microfiltration, ultrafiltration, nanofiltration and reverse osmosis. Figure 1.5 illustrates these categories together with some common microscopic particles to refer them with. Note that in this thesis, we focus on microfiltration.

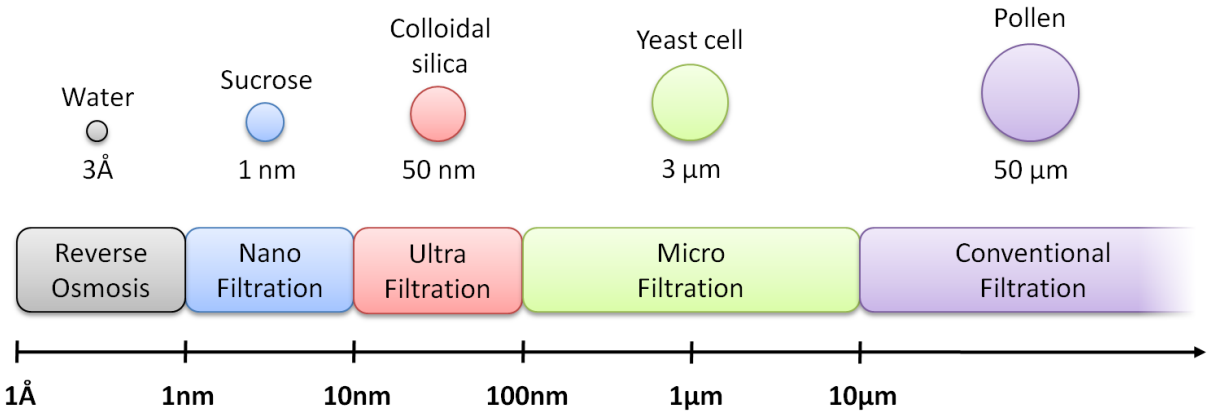


Figure 1.5: Categories of membrane filtration.

1.3.1 Flow resistance

Within a set of geometric boundaries, a fluid will displace over time with the presence of a pressure gradient. We can speak of a flow resistance when the displacement is finite. This is true for most, if not all, practical cases. The flow resistance, in its most ideal form, has a linear relationship with the fluid displacement and applied pressure (Equation 1.3). In general, a low flow resistance is highly desired for MF devices, because then less energy (pressure) is lost over the membrane, while more is put to use in the flow rate.

$$R_f = \frac{P}{VFR}$$

Equation 1.3: Linear relation between R_f the flow resistance, P the absolute pressure and VFR the volumetric flow rate.

1.3.2 Membrane fouling

An important disadvantage of MF is membrane fouling. As time progresses in a MF process, separated particles will accumulate at the membrane and start to clog the pores. Eventually, this will become noticeable in the performance as the flow resistance continuously increases until the membrane becomes completely blocked.

There are many ways to prevent or delay membrane fouling. A simple method to increase the operation time is by using an alternative MF configuration called cross flow filtration (Figure 1.6). With an additional outlet compared to dead-end filtration, cross flow filtration presents an exit path for clogging particles.

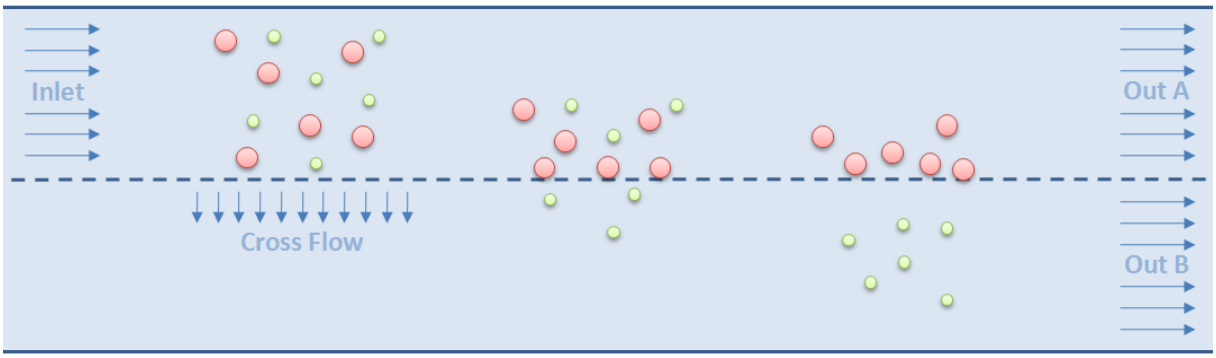


Figure 1.6: Illustration of cross flow membrane filtration.

1.3.3 Particle sorting

Unlike LC, MF separates particles based on one size criteria. Hence, a configuration with multiple membranes is necessary in order to sort particles. A possible configuration is shown in Figure 1.7, where the pore size is reduced in each consecutive membrane. Using this configuration, particles can be sorted from large to small.

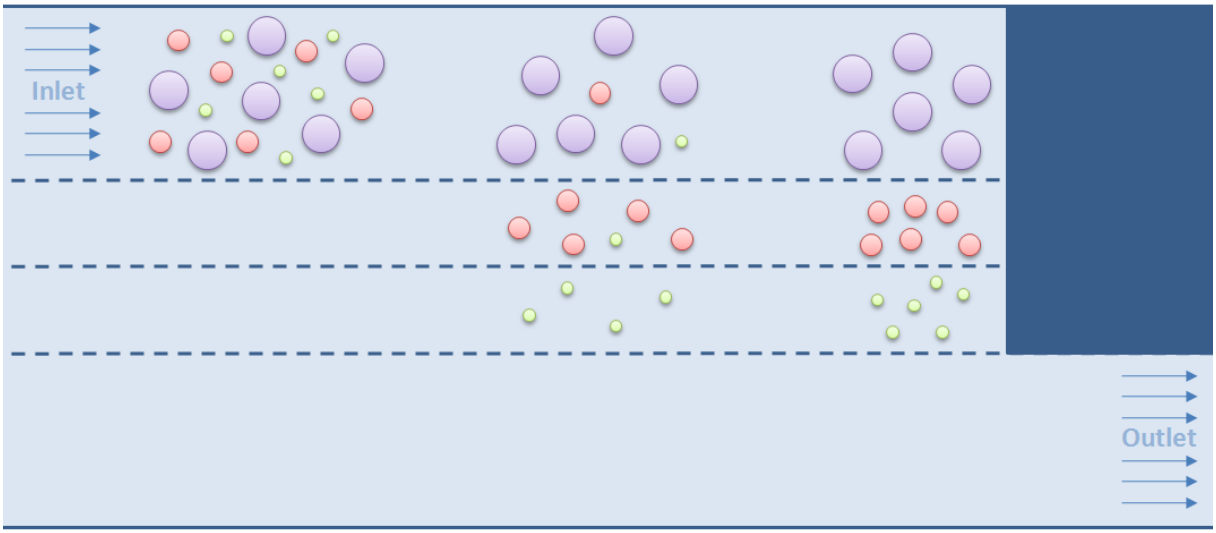


Figure 1.7: Configuration for particle sorting. Each consecutive membrane has smaller pore size.

1.4 The possibilities with MEMS technology

Conventional MEMS technology includes mainly planar processes, e.g. photolithography, chemical vapor deposition, epitaxy, plasma etching. These processes produce devices by sequencely and selectively manipulating the surface of a flat substrate. The developments over the past years has driven MEMS technology to such an extent that we can now accurately create devices on sub-micrometer scales. By exploiting this, a new generation of fluidic filters can be created that:

- Are small (millimeter size).
- Are geometrically well-defined.
- Can filter small volumes of fluids (femtoliters).
- Can be integrated with addition elements in for example, lab-on-a-chip applications.

When implementing a fluid filter with MEMS technology, a number of considerations have to be made. One of these considerations is how the filter is orientated on the substrate. This is important, because the orientation has strong influences on:

- The surface area of the substrate required to fabricate the filter.
- The positioning of the fluid channels.
- The method of sealing.
- The integration capacity with additional elements.

For the LC family, the channel is an integral part of the separation mechanism. Its length is related to the desired separation resolution and is often required to be much longer than the thickness of a substrate. Consequently, the orientation is fixed for these types of filters and the separation mechanism has to be parallel (horizontal) to the surface of the substrate.

For MF, the separation occurs over a porous membrane which is generally thin (several micrometers) for micro-particle applications. A porous membrane could therefore be implemented at any angle of orientation. However, since we are considering planar processes to fabricate the devices. The viable orientations are limited to either horizontal or vertical.

The aforementioned settings are depicted in Figure 1.8.

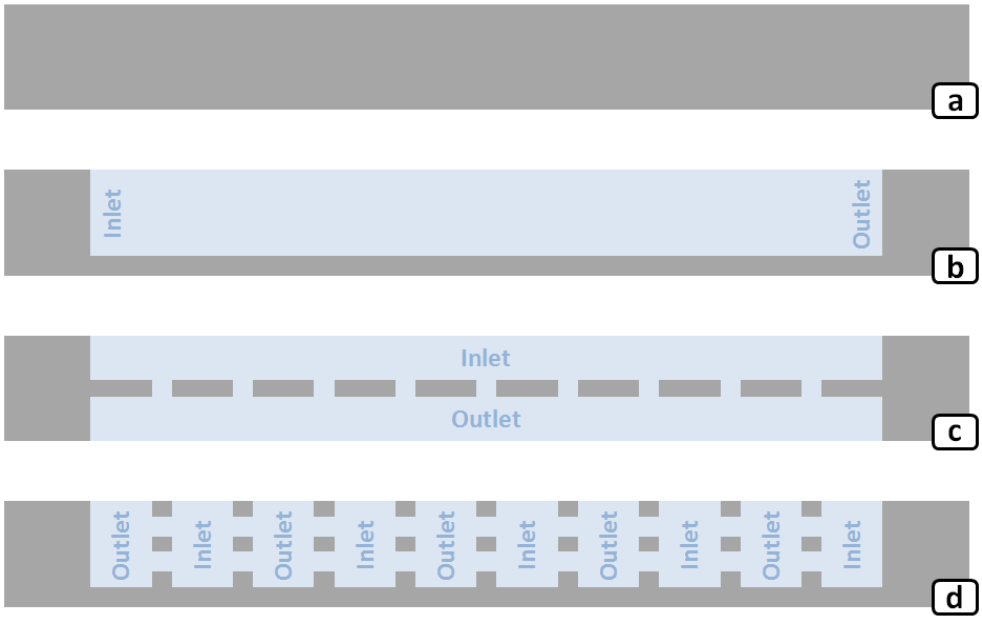


Figure 1.8: Orientation possibilities illustrated with cross-sectional views.
Flat substrate (a). Horizontal LC (b). Horizontal MF (c). Vertical MF (d).

1.5 Discussion

The main advantages and disadvantages of LC are:

+ Continuous operation is possible.
+ Can separate particles based on various criteria and properties.
− Large separation mechanism.
− Long separation times (minutes) [13-14].

The main advantages and disadvantages of MF are:

+ Well defined pores allow near-ideal separation.
+ Small separation mechanism.
+ Low separation times (seconds).
− Membrane fouling.
− Each membrane with predefined pores can only separate particles based on one size criteria.

When we consider combining one of the above separation principles with MEMS technology then MF presents itself as the most interesting case. In fact, MF has a simple and small separation mechanism that behaves more ideally when more accurately defined. MEMS technology has a less enhancing effect on the separation mechanism of LC, because the separation occurs mainly over time and not over any specific geometric boundary.

MF membranes can be orientated at different angles on a flat substrate. The main advantages and disadvantages of vertically orientated MF membranes are:

+ Efficient use of surface area.
+ Configurations containing differently sized membranes can be made on a single substrate.
+ Additional surface elements can be integrated if the separation mechanism is buried.
− Pores cannot be defined by conventional photolithography.

Vertical MF membranes have many advantages over its horizontal alternative. However, in order to realize these membranes with the planar processes of MEMS technology, the challenge of accurately defining sub-micrometer pores vertically has to be faced. This has been addressed in the research project and two new MEMS filter designs able to perform microfiltration have been developed. They are analyzed in the next chapters, to acquire sufficient insights to design a third module with an improved performance.

2 The first design: a porous membrane fabricated from a jagged thin film layer stack

The first MEMS filter for microfiltration [15], henceforth referred to as V1, is discussed in this chapter. Its advantages, disadvantages, issues and optimizations are the main points of discussion.

2.1 Concept

The V1 design features a vertical porous membrane fabricated using conventional MEMS technology (Figure 2.1). The V1 membrane is surface micromachined and can be, in theory, fabricated on a variety of substrates. For this thesis, V1 devices were fabricated out of stacked layers of silicon oxide (SiO) and silicon nitride (SiN) on a silicon (Si) substrate. A dry film photo-resist (DFR) is used to seal the fluidic devices [16].

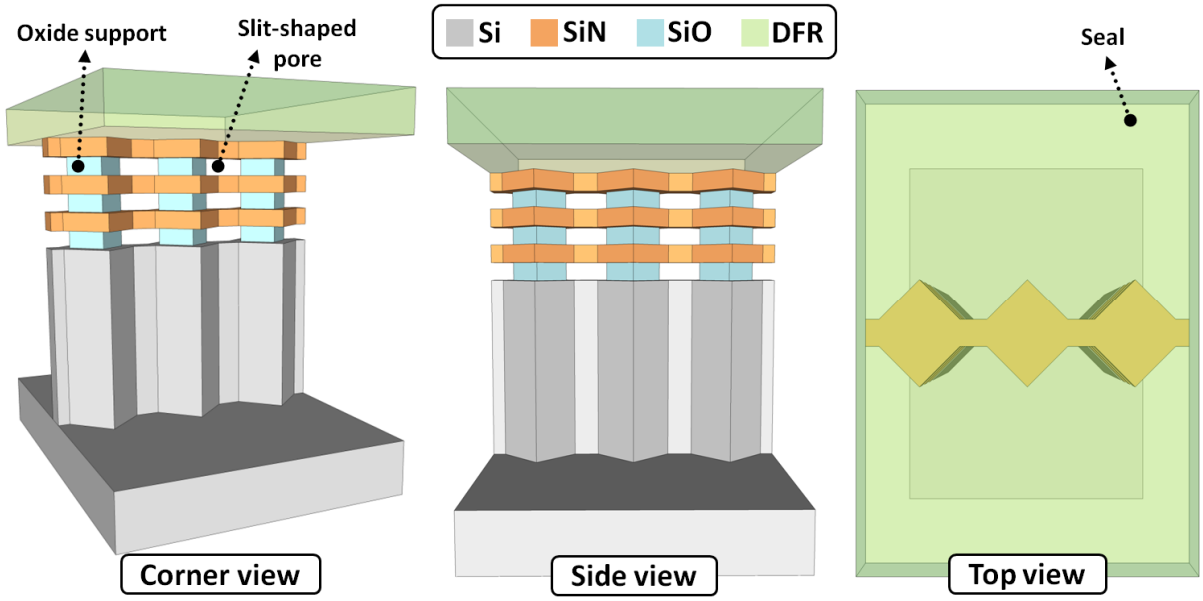


Figure 2.1: Conceptual drawings of the first micro-fluidic filter from different perspective points of view.

The V1 filter design requires, unlike most MEMS processes, just a single photolithography mask for its structural components. This fundamentally reduces the fabrication complexity and cost which allows for a relatively effortless integration of the V1 design with other MEMS devices.

The V1 membrane contains numerous slit-shaped pores which are present in the oxide layers, between the oxide supports. The pore size is defined along with the thickness of the oxide layers by plasma enhanced chemical vapor deposition (PECVD), and can be varied during fabrication independently from other process steps. Fully functional V1 devices have been fabricated with 100nm, 500nm and 1µm sized pores without requiring additional photolithography or additional process steps.

One of the main disadvantages of the V1 design is its high flow resistance. The flow resistance is inversely proportional to the size and porosity of the membrane. Therefore, by either increasing the number of oxide layers or the density of the pores, a lower flow resistance can be achieved. However, stresses in the layer stack put restraints on these options, making it inefficient to implement the V1 design in any high throughput (liters/minute) application.

2.1.1 Dimensions

Devices with 100nm, 500nm and 1µm pore sizes have been fabricated based on the V1 design. Scaled drawings of a 500nm device are provided in Figure 2.2. Note that 100nm and 1µm devices differ from 500nm devices by only the thicknesses of the oxide layers.

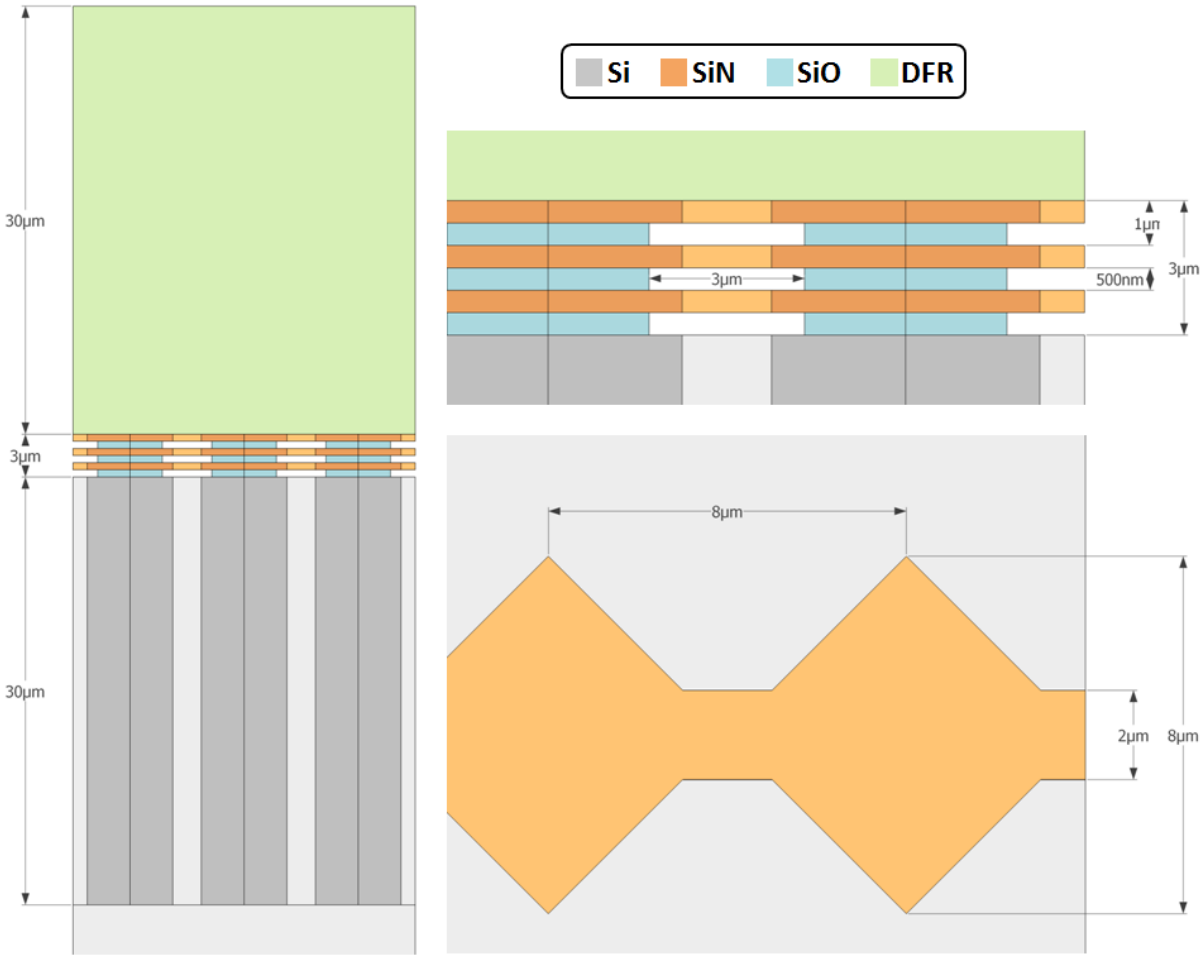


Figure 2.2: Scaled drawings of the first MEMS filter, dimensions included.
Side view (left). Enlarged side view (top right). Top view (bottom right).

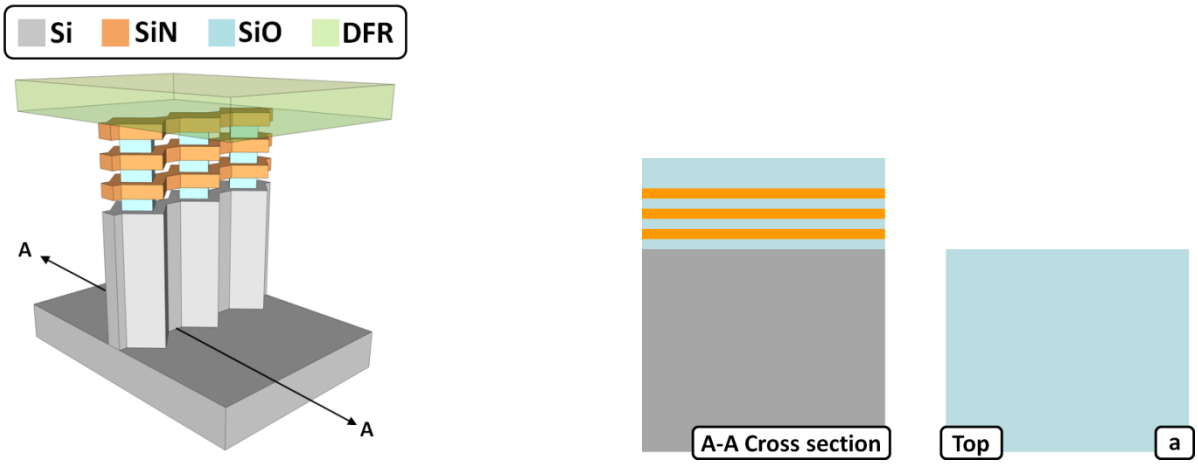
The microchannels of the V1 device are not indicated in the figure above. However, these channels are present to supply and retrieve the necessary fluids to and from the porous membrane. There are two rectangular, 50µm wide and 30µm high, microchannels located parallel along the membrane. Each microchannel can be addressed individually making it either the in- or outlet channel.

The V1 membrane, seen from above, is jagged shaped and contains wide and narrow parts which are respectively 8µm and 2µm in width. The shape of the membrane is such that an isotropic etchant will laterally penetrate the narrow parts of oxide before it does the wide parts, thereby respectively creating the slit-shaped pores and oxide support structures. The membrane is periodic every 8µm and is approximately 10mm in length.

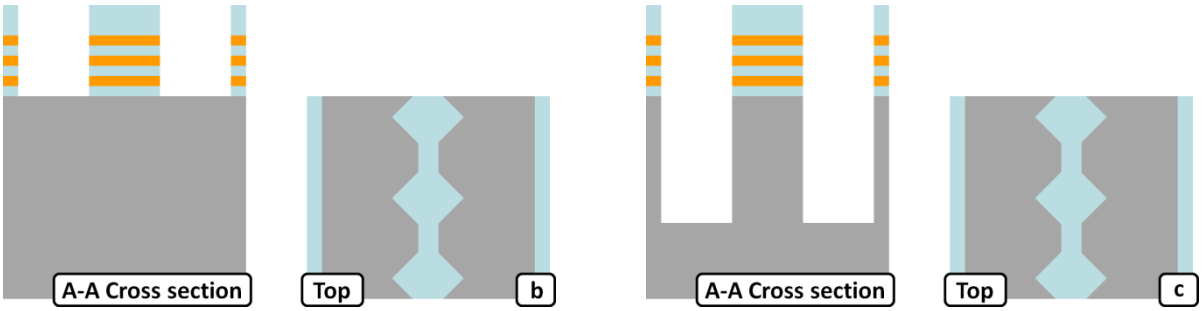
The V1 membrane is quite small when compared to the height of the microchannels (1:10) and even smaller when related to the height of the silicon substrate (1:160). We may therefore note that only a portion of the substrate is occupied to form the porous membrane and that the majority of available space is unused.

2.2 Fabrication process

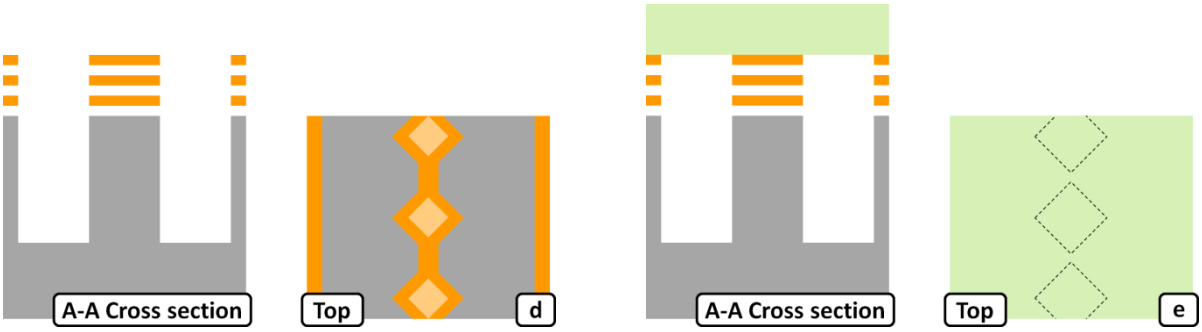
The following section contains the key fabrication steps for a V1 device with 500nm pores. The steps are presented with schematic views and outlined textually. A more detailed and complete process flow is included in Appendix A. The following uncaptioned pictures are referred to as Figure 2.3.



(a) A stack consisting out of 3 alternating layers of 500nm PECVD SiO and SiN is deposited on a 500µm thick Si substrate. The stack is topped with a 2µm SiO layer which functions as mask during the deep reactive ion etch (DRIE) in step *c*.



(b) The layer stack is patterned by photolithography and etched by directional plasma. These steps define the membrane and the microchannels.
(c) With the uppermost SiO layer as mask, DRIE etches 30µm deep into the substrate, creating the microchannels alongside the membrane.



(d) The SiO layers are partially etched with a buffered hydrofluoric acid (BHF). After this etch, the remaining SiO and SiN layers form the V1 membrane structure.
(e) A 30µm negative DFR [17] is laminated over the entire device and uniformly exposed. After properly curing, the DFR functions as seal for the fluidic device.

Scanning electron microscope (SEM) and optical images of a V1 device during and after fabrication are shown in Figure 2.4 through Figure 2.7.

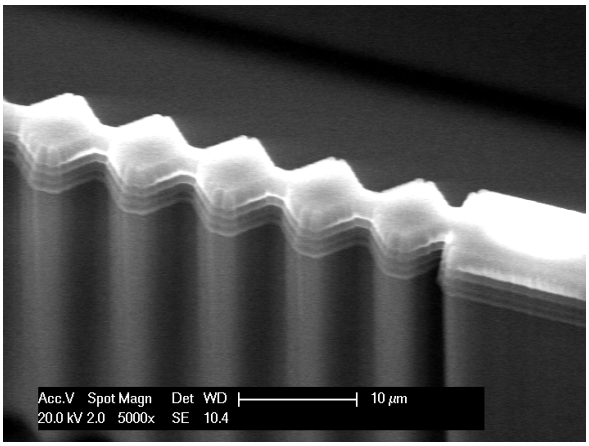


Figure 2.4: V1 device processed through step *c*.
Corner view.

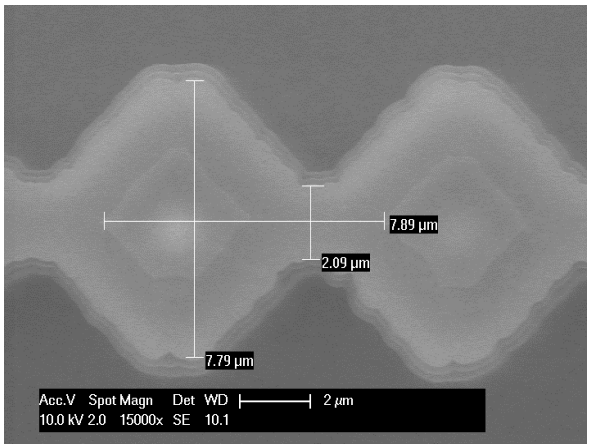


Figure 2.5: V1 device processed through step *c*.
Top view.

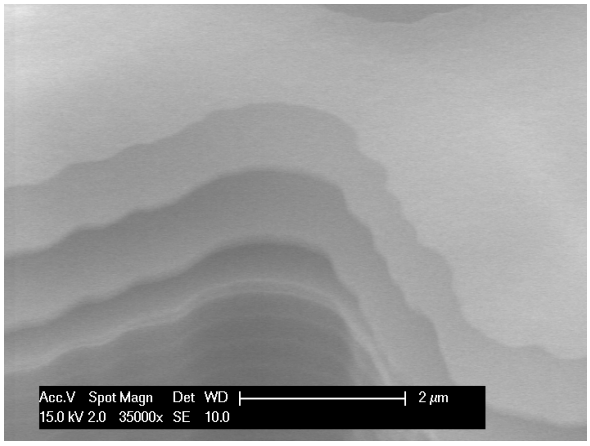


Figure 2.6: V1 device processed through step *d*.
Corner view.

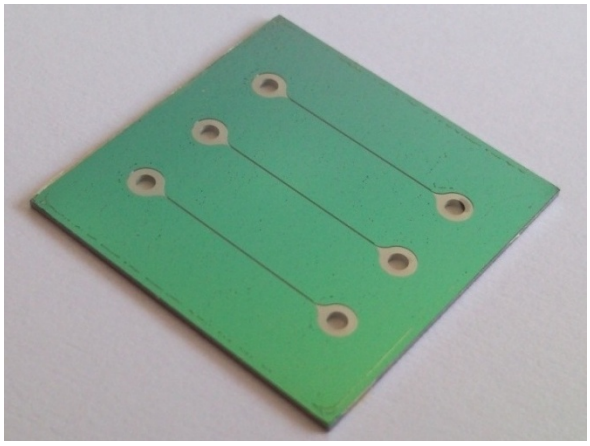


Figure 2.7: A completed and diced V1 device.

2.3 Design analysis

To understand the potential and limitations of the V1 design, a thorough analysis was conducted. We found a number of issues related to the fabrication yield and performance. These issues were addressed to optimize the V1 design and are discussed in this section.

2.3.1 Fabrication variations

The V1 design is fabricated using mostly standard recipes. These are managed by the DIMES clean room staff to ensure a correct and stable result. There are two process steps however, were there is freedom to vary process parameters at the costs that users have to account for equipment variations themselves. These processes are photolithography (Figure 2.3b) and BHF etch (Figure 2.3d).

In the first batch of devices we found signs of overexposure (Figure 2.8) and over-etch (Figure 2.9). Overexposed devices have a degraded robustness. This is due to the unwelcome deviation in the jagged shape of the membrane. The deviation is eventually troublesome for the BHF etch, because the etching parameters have to be re-adjusted to ensure a good trade-off between the pore dimensions and oxide supports. A poor trade-off would lead to either a relatively high flow resistance or a mechanically weak membrane. Figure 2.10 shows a V1 membrane that is completely dislocated due to the insufficient size of the oxide supports. The dark jagged shadow in the middle of the figure is the unfocused Si frame on which the membrane should have been attached.

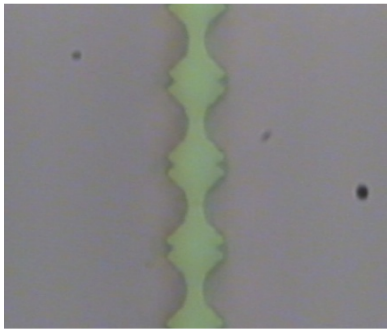


Figure 2.8: Overexposed membrane.

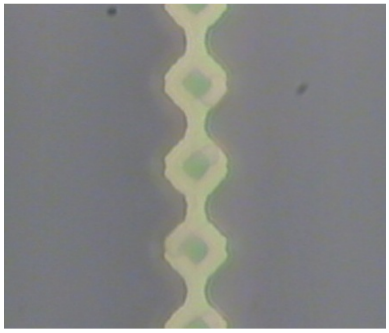


Figure 2.9: Over-etched membrane.

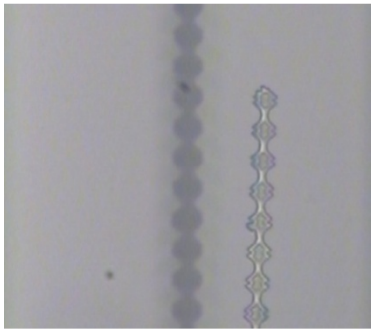


Figure 2.10: Broken membrane.

We optimized the process parameters of both the photolithography (Figure 2.11) and the BHF etch process (Figure 2.12). It can be seen that through optimization alone, the size of the oxide supports can be significantly increased which greatly contributes to the robustness of the membrane.

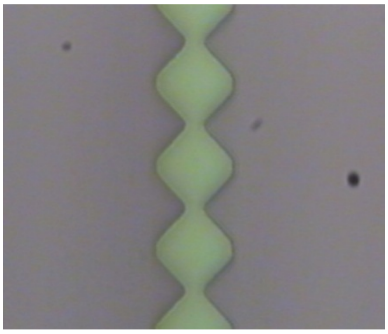


Figure 2.11: Well exposed membrane.

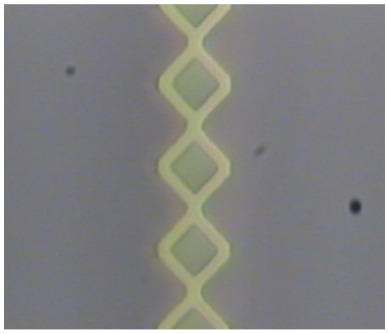


Figure 2.12: Well etched membrane.

Note that different contours can be identified in Figure 2.9 and Figure 2.12. The outer contour is shaped by the (transparent) nitride layers and the inner contours by the oxide supports.

2.3.2 Sealing method

DFR is a photosensitive resin centered in a multilayer configuration with a carrier- and cover film [17]. The conventional use for DFR is patterning which is no different from any other photo-resist (PR). However, DFR can also be completely cured into a uniform thin film and adapted to seal fluidic devices. DFR sealing has many advantages compared to conventional sealing techniques like glass or poly dimethyl siloxane (PDMS) bonding. This is because DFR:

- Can be applied on rough and uneven surfaces.
- Is simple to apply.
- Does not require any pre-treatment to improve substrate-to-seal adhesion.
- Is resistant against strong corrosives [18].

For these reasons, all the MEMS filters considered in this thesis are sealed using a 30µm negative epoxy DFR by means of lamination. However, unlike conventional applications involving DFR, here it has to meet the requirement to span across and not obstruct the 50µm wide microchannels that are present on the surface of our devices.

Extensive development took place to find the lamination process that produces the most robust and fault-free DFR seal. This was necessary because the manufacturer-specified lamination process was deemed unfit for our devices due to the high temperature (85°C) baking steps required according to the manufacturer [18]. These baking steps cause DFR to deform and collapse into our microchannels which permanently blocks the fluid path (Figure 2.13).

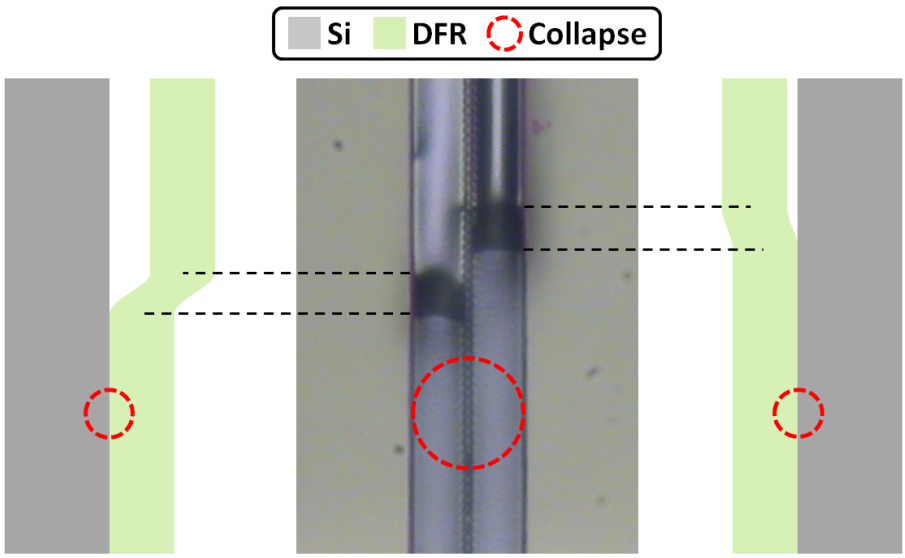


Figure 2.13: Optical image of collapsed DFR in a V1 device (middle).
Corresponding schematic cross sections of the blocked microchannels (left and right).

As proof of concept, a customized lamination process at 45°C was developed prior to this thesis which provided a weak, but functional DFR seal. This process and its parameters are presented in Table 2.1 as Process 0.

When the development of the MEMS filters progressed, longer and more intensive applications (experiments) involving pressurized fluids were necessary. Consequently, a more robust DFR seal was required. We therefore reassessed and optimized Process 0 which lead to three new processes. These processes are included in Table 2.1 as well.

Table 2.1: Customized DFR lamination processes					
#	Step	Process 0	Process 1	Process 2	Process 3
1	Cover film removal	✓			
2	Lamination	manually with roller and hotplate			
	Temperature	45°C	35°C	55°C	45°C
3	Pre-exposure bake	×			45°C
	Time	×			5min
4	Primary exposure	office enviroment			UV
	Time	>3hrs			2min
5	Post-exposure bake	×			45°C
	Time	×			5min
6	Carrier film removal	✓			
7	Hard bake	×			45°C
	Time	×			15min

Process 1 and 2 are variants of Process 0 at different lamination temperatures: 35°C, 55°C and 45°C respectively. By comparing the results of each of these processes, we can determine the influence of the lamination temperature on the quality of the DFR seal.

We found microscopic air gaps on the surface of 35°C and 45°C laminated devices (Figure 2.14). These air gaps seemed to correlate with poor adhesion, because when these devices were submerged in deionized (DI) water for 2 hours, partial delamination of the DFR seal was observed (Figure 2.15 and Figure 2.16). These issues could not be found for 55°C laminated devices, suggesting that high temperature lamination (or at least, thermal energy) is favorable for adhesion.

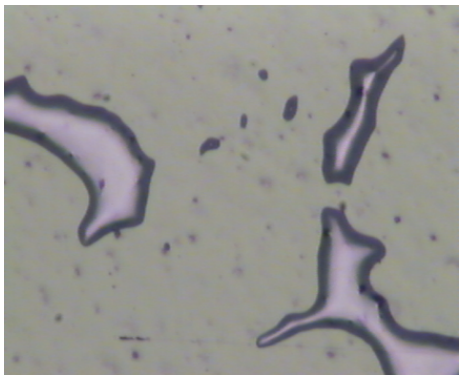


Figure 2.14: Air gaps in DFR.

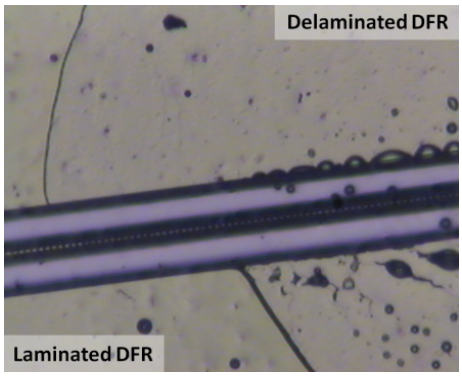


Figure 2.15: Partial DFR delamination.

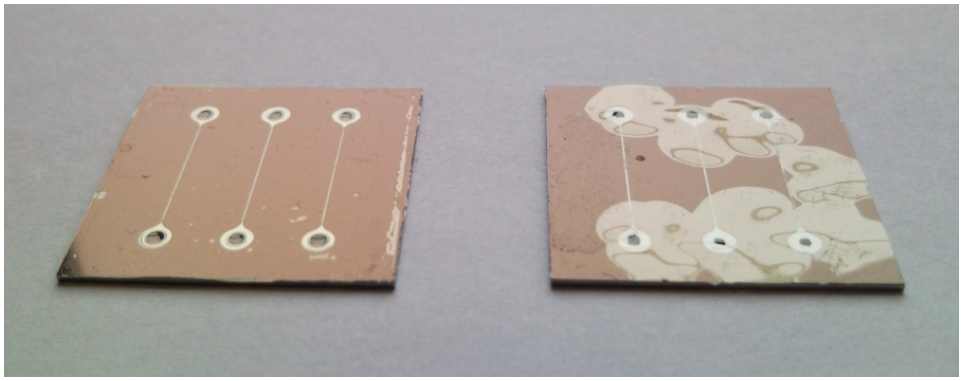


Figure 2.16: DFR laminated V1 device (left).
Partially DFR delaminated V1 device (right).

In spite of improved adhesion, the 55°C laminated devices suffer from blocked channels due to collapsed DFR. This observation indicates that the lamination temperature should be limited to below 55°C.

An issue that all the aforementioned processes share is poor reproducibility. Occasionally during the carrier film removal step, the DFR would show such poor adhesion that it would be removed along with the carrier film, causing an immediate seal failure. We found that the cause was due to the exposure method which was done in an office environment, where the lighting, humidity and temperature conditions were highly unstable. For better reproducibility, exposure parameters should be repeatable and constant over time.

Process 3 was devised with the accumulated knowledge gained from the previous lamination processes. It re-establishes the lamination temperature at 45°C and contains the addition of three baking steps. The first baking step is to enhance the surface adhesion, while the remaining two ensure a proper curing of the DFR. Furthermore, instead of depending on a variable office environment, a well-defined ultraviolet (UV) source was used to expose the negative DFR.

Compared to the other custom lamination processes, DFR seals made with Process 3:

- Do not show signs of air gaps on the laminated surface.
- Do not delaminate in DI water (tested up to 48hrs).
- Do not collapse and obstruct microchannels during lamination.
- Have consistent results.
- Can be finalized within 30 minutes.

Based on the aforementioned, Process 3 was chosen as the standard lamination process for the DFR seals.

2.3.3 Glass reinforced seal

We quickly found that a 30µm thick DFR seal was not sufficient for the V1 devices against applications with pressurized fluids above 40 KPa. When this pressure is exceeded, the DFR seal directly above the device inlet breaks (Figure 2.17).

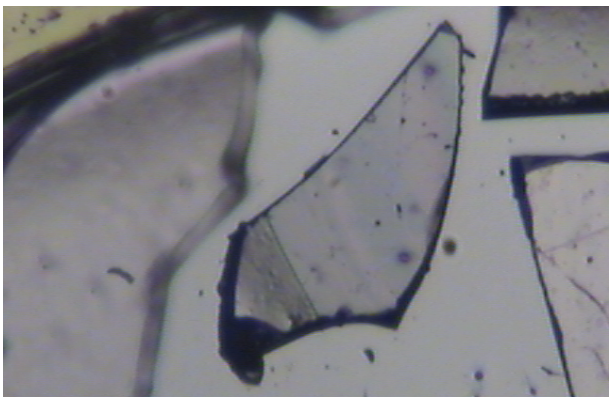


Figure 2.17: Broken DFR seal due to over-pressure.

This poor pressure performance is caused by the size of in- and outlets (Figure 2.18). They are 2mm in diameter and considerably larger than any other components of the V1 device. The DFR seal has to span across large distances to cover these areas and it becomes fragile by doing so. Furthermore, since pressurized fluids are applied from the inlet, peak pressure always persists at the weakest part of the DFR seal, thereby easily causing a failure.

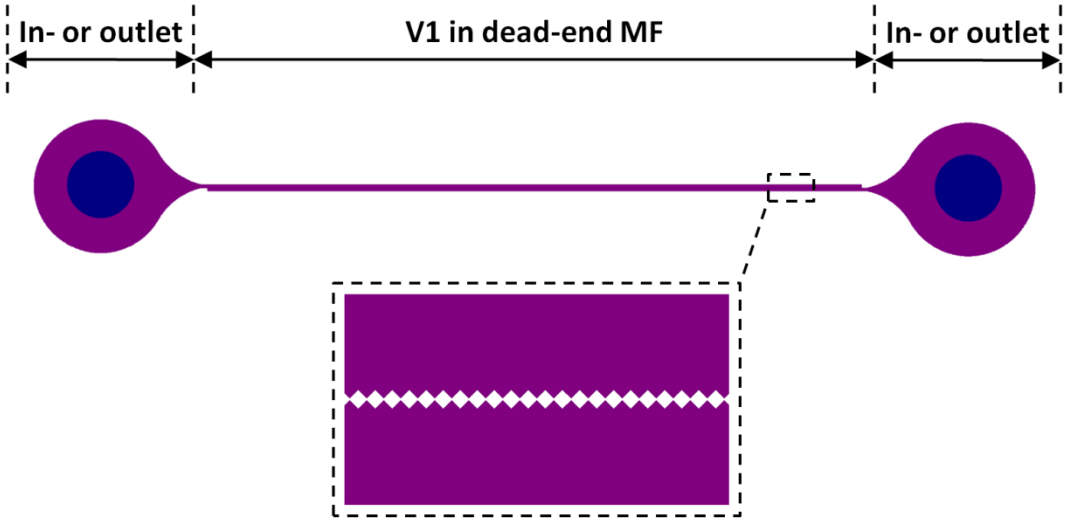


Figure 2.18: Layout of the V1 filter device.

In an attempt to enhance the pressure performance of the V1 devices, we manually fixed a 500µm thick glass substrate on top of the DFR seal, preventing weak areas of the seal from deflecting too much under load and break. To account for the surface roughness at the DFR and glass interface, DI water was used as medium to smoothen the contact plane. This reinforced sealing method showed improved operation pressures up to 400kPa. However, it had the disadvantage that the water medium had to be replenished over time to counter losses due to evaporation.

We found a permanent solution with SU-8, a negative epoxy PR [19-20]. By using SU-8 as adhesive and medium for the glass substrate, the improved operation pressures could be achieved and sustained with minimum effort. Note that SU-8 was chosen specifically, because it has similar mechanical properties as DFR.

The presented SU-8 bonded, glass reinforced, DFR sealing method is quite attractive for the MEMS filter devices discussed in this thesis. In addition, apart from strengthening the DFR seal, this sealing method also strengthens the entire device by increasing the total substrate thickness from 500µm to 1mm which proved to be very beneficial during the mounting of the devices for the fluidic experiments (Subsection 5.1.1).

2.4 Discussion

The main advantages and disadvantages of the V1 design are:

+ Fabrication requires only three materials, all of which are conventional MEMS materials.
+ Pores are defined by PECVD oxide parameters, not by photolithography.
+ Requires one photolithography mask for its structural components.
+ Simple device, easy to integrate within existing MEMS processes.
− High flow resistance due to inefficient use of substrate height.
− DFR seals need to be reinforced with glass for operating pressures higher than 40KPa.

The V1 design proves that it is possible to create vertical MF devices using MEMS technology and seal these with DFR. However, the V1 design suffers from a high flow resistance that cannot be dealt with effectively, without relying on a more area efficient design.

3 The second design: a porous membrane with suspended nitride beams

The second (V2) MEMS filter design [21] is meant to outperform the V1 in the aspect of flow resistance. This chapter will introduce, analyze and present the possible improvements of the V2 design.

3.1 Concept

The V2 design aims at a low flow resistance by adapting a different membrane structure that has more pores per surface area compared to the V1 membrane (Figure 3.1).

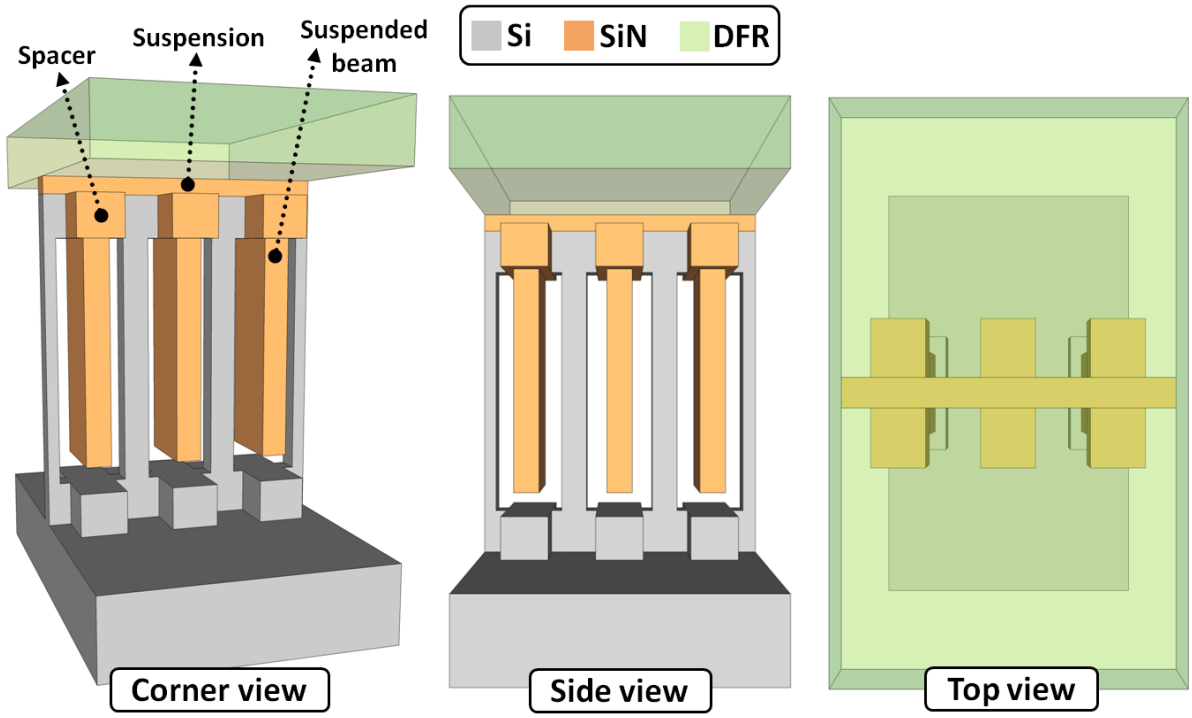


Figure 3.1: Conceptual drawings of the second micro-fluidic filter from different perspective points of view.

The V2 membrane is fabricated using techniques from both bulk and surface micromachining. The identifying feature of the membrane is its long interleaving beam-like structure that alternates between two different materials, silicon and silicon nitride. Between each interleaf, there is a slit-shaped pore at a certain distance from the nitride suspension.

Unlike the V1 membrane, where the pores lie in surface micromachined layers, the V2 pores are located inside the bulk of the silicon substrate. Instead of depositing more surface layers, a lower flow resistance can be achieved by simply extending the slit-shape pores further into the substrate. This high aspect ratio and area efficient concept is a result of truly exploiting the potential of vertically orientated membranes.

Thermal oxidation creates highly uniform, conformal and tunable oxide layers. These properties are quite advantageous for the V2 design as its slit-shaped pores are pre-defined by layers of thermal silicon oxide. Pores released from thermal oxide are uniform and can be purposely varied from tens of nanometers to 1-2 micrometers by simply altering the oxidation parameters.

The main disadvantage of the V2 design is that the suspended nitride beams act as mechanical loads for the membrane structure. The nitride beams can therefore not be made extremely large as this increase the fragility of the membrane. Consequently, a limit exists on the length of the slit-shaped pores.

3.1.1 Dimensions

Devices with 500nm and 1µm pore sizes have been fabricated based on the V2 design. Scaled drawings of a 500nm device are provided in Figure 3.2.

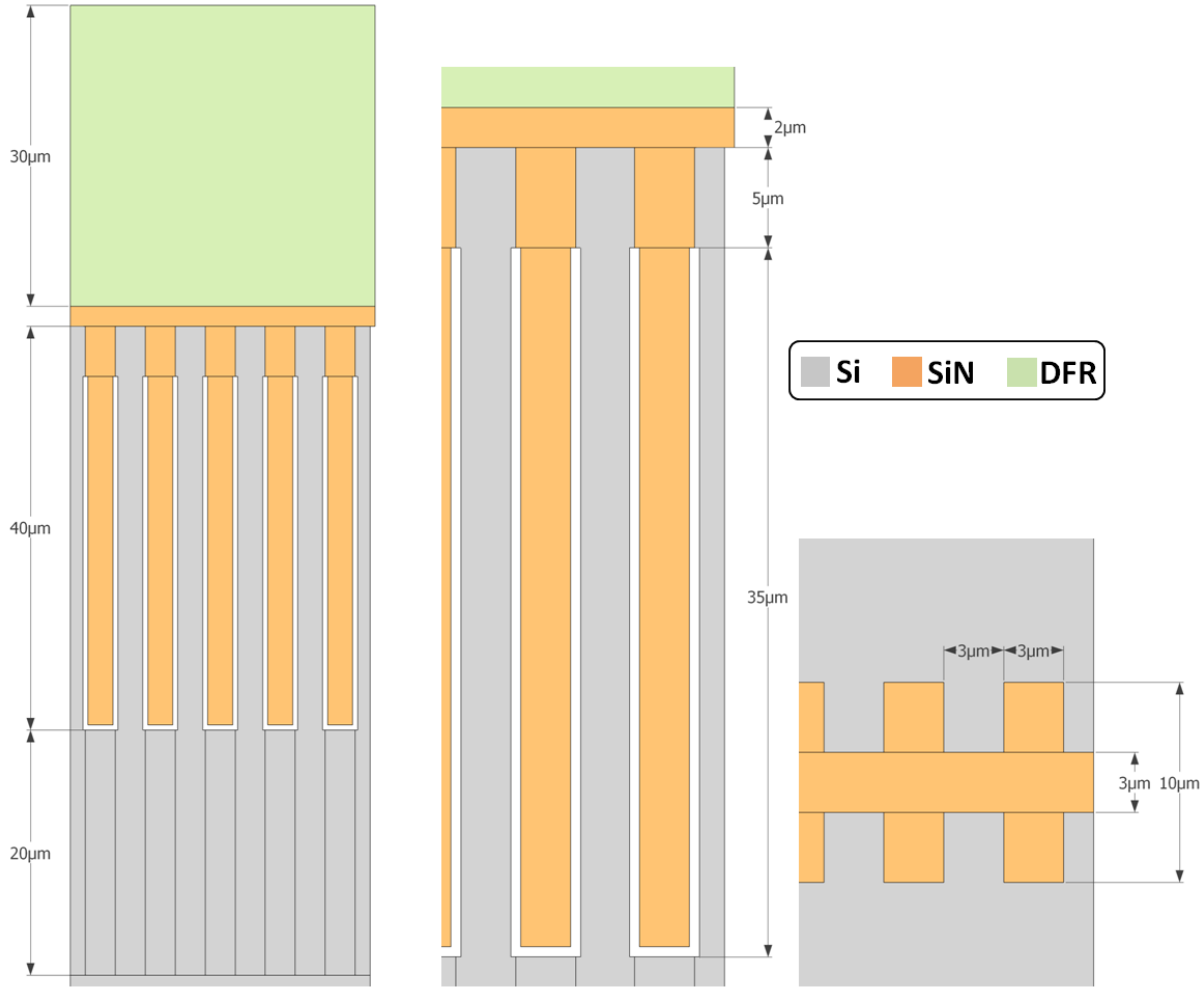


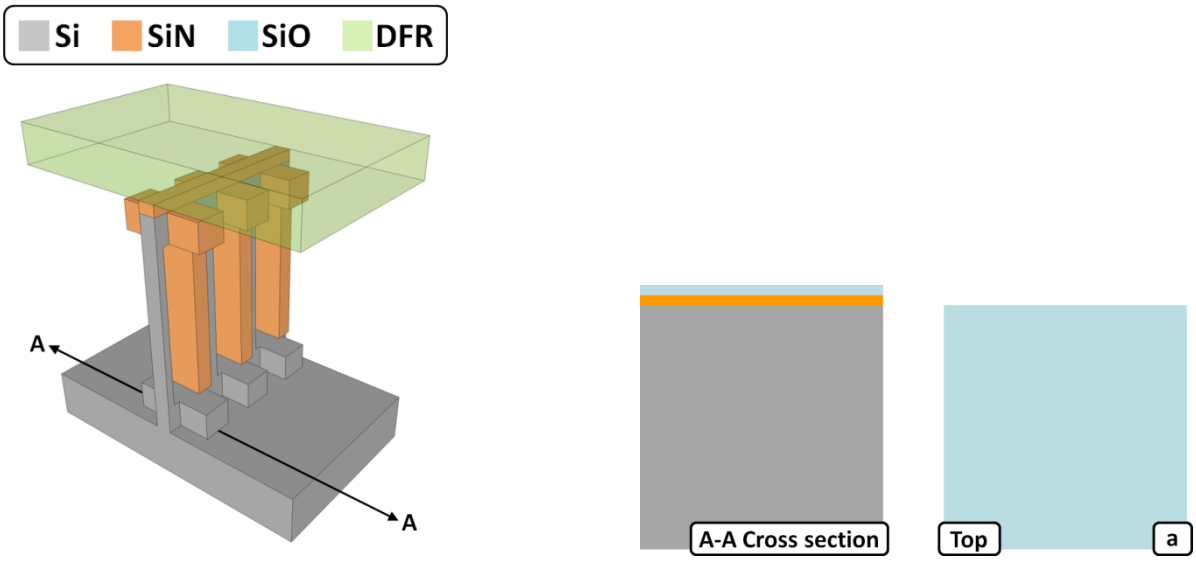
Figure 3.2: Scaled drawings of the second MEMS filter, dimensions included.
Side view (left). Enlarged side view (middle). Top view (right).

For the supply of fluids, there are two rectangular, 50µm wide and 60µm high, microchannels present on either side of the V2 membrane. Each microchannel can be individually addressed as the in- or outlet channel of the filter device.

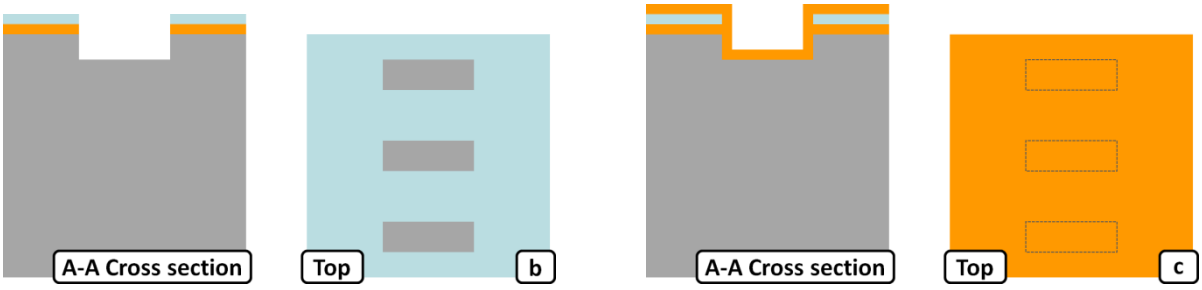
The nitride beams are 3µm wide and 40µm long, spaced 5µm from the 2µm high suspension. Silicon beams interleave with the nitride beams creating the slit-shaped pores. The width of the silicon beams depends on how much of it is consumed during thermal oxidation for the definition of the pores. However, this figure is psychically constrained to be always less than 3µm. The entire V2 membrane is a sequence of basic elements that repeat after every 6µm and is approximately 10mm in length.

3.2 Fabrication process

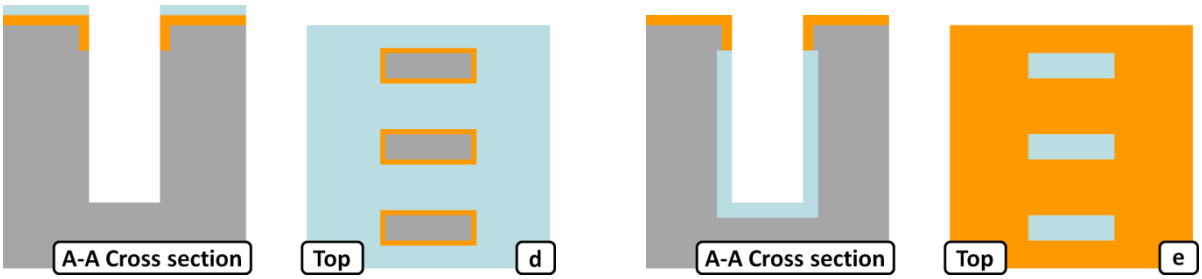
The following section contains the key fabrication steps for a V2 device with 500nm pores. The steps are presented with schematic views and outlined textually. A more detailed and complete process flow is included in Appendix A. The following uncaptioned pictures are referred to as Figure 3.3.



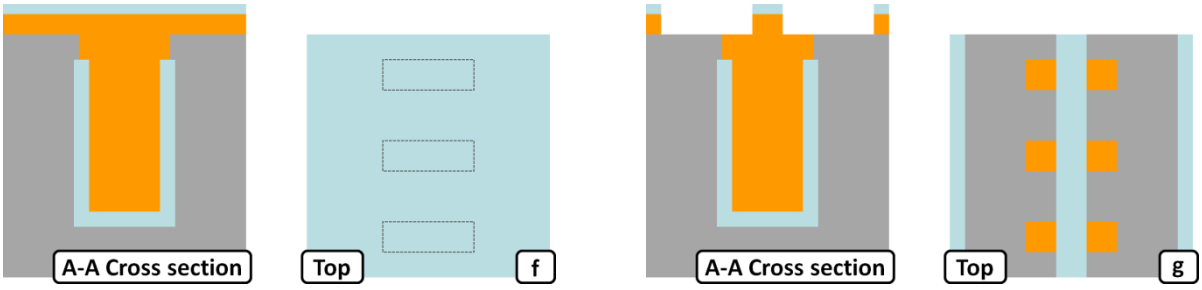
(a) A layer of 500nm low pressure chemical vapor deposition (LPCVD) SiN and a layer of 1µm PECVD SiO are deposited on a 500µm thick Si substrate. The SiN deposition excludes the surface from thermally oxidizing in step *e* and the oxide layer functions as mask during DRIE in step *d*.



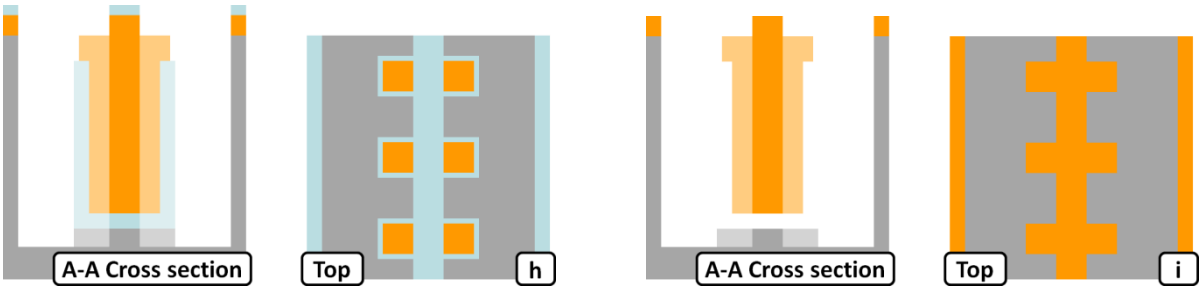
(b) A row of 3µm by 10µm rectangles pitched 6µm are patterned and directionally etched to create 5µm deep trenches. These shallow trenches assist in creating the spacers.
(c) 300nm LPCVD SiN is deposited to prevent the sidewalls of the shallow trenches from thermal oxidation in step *e*. This will effectively bury the slit-shaped pores 5µm deeper inside the substrate since the pores can only be released from oxidized areas.



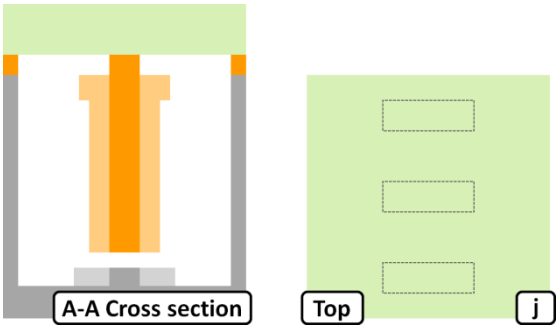
(d) Excess SiN is removed by directional etching. This reveals the oxide mask at the surface of the substrate and silicon at the bottom of the trenches. With DRIE, the trenches are etched 35µm deeper, creating long rectangular molds for the slit-shaped pores and the suspended SiN beams.
(e) The remaining oxide mask and sidewall polymer left by DRIE is removed. The wafer is thoroughly cleaned and then thermally oxidized to form 500nm thermal oxide on the inner Si faces of the molds.



(f) The suspended nitride beams are then finalized by casting 1.5µm LPCVD SiN onto the wafer and into the molds. A 2µm LPCVD silicon oxide layer is deposited as mask for DRIE in step *h*.
(g) In order to gain physical access to the thermal oxide layers, a second photolithography process patterns the 50µm wide microchannels over the casted beams. The pattern is directionally etched into the oxide and nitride layers until it reaches the Si surface.



(h) DRIE etches the pattern 60µm deep which both creates the microchannels and uncovers the thermal oxide layers.
(i) With the thermal oxide layers accessible, the substrate is subjected to a 50 minutes BHF etch to remove all the oxide and release the slit-shaped pores.



(j) The V2 devices are finalized by sealing the microchannels using DFR.

SEM and optical images of a V2 device during fabrication are shown in Figure 3.4 through Figure 3.7.

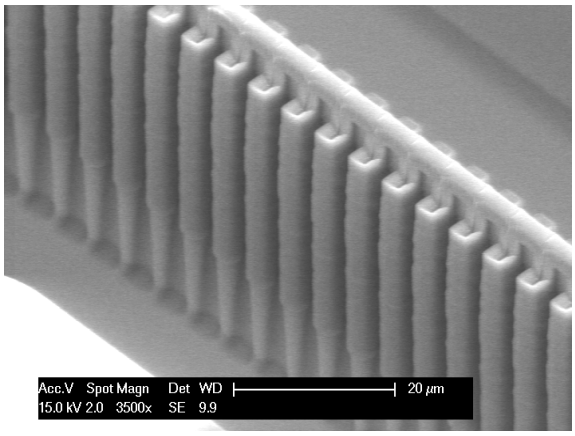


Figure 3.4: V2 device processed through step *h*.
Corner view.

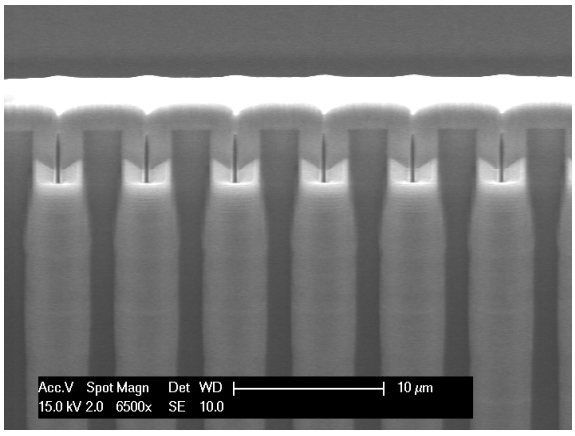


Figure 3.5: V2 device processed through step *h*.
Side view.

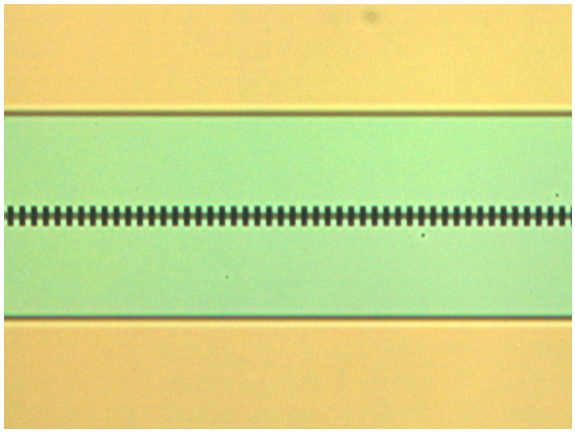


Figure 3.6: V2 device processed through step *g*.
Top view.

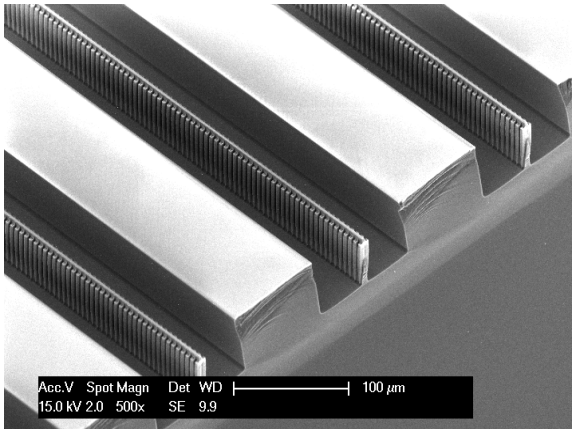


Figure 3.7: Array of V2 devices.
Corner view.

3.3 Design analysis

3.3.1 Spacers

Spacers are present in the v2 design to prevent the slit-shaped pores from extending up close to the surface. This is done to relieve mechanical stress from the nitride suspension when the membrane structure experiences a displacing force during device operation or transportation.

A short section of the V2 membrane, containing two periods (12µm), is modeled with a finite element analysis tool (COMSOL Multiphysics) to illustrate the effectiveness of spacers to relieve mechanical stress. Three models were made and simulated using identical parameters for a qualitative comparison. The simulation parameters are listed in Table 3.1.

Table 3.1: COMSOL stress simulation parameters

Parameters	Si	SiN	Unit
Young's modulus	170e9	250e9	Pa
Poisson's ratio	0.28	0.23	-
Thermal expansion coefficient	2.6e-6	2.3e-6	1/K
Density	2329	3100	kg/m^3
Initial stress	0	150e6	Pa
Load	1e6	1e6	N/m^2

Figure 3.8 shows the simulation results of the first model. This model was made in the image of the v2 design, but with the spacers absent. We can see from the figure that there are concentrations of stress at four distinct spots on the nitride suspension when the membrane is under load. Furthermore, stress gradients also persist in the silicon beams as they contain the only anchoring points for the membrane.

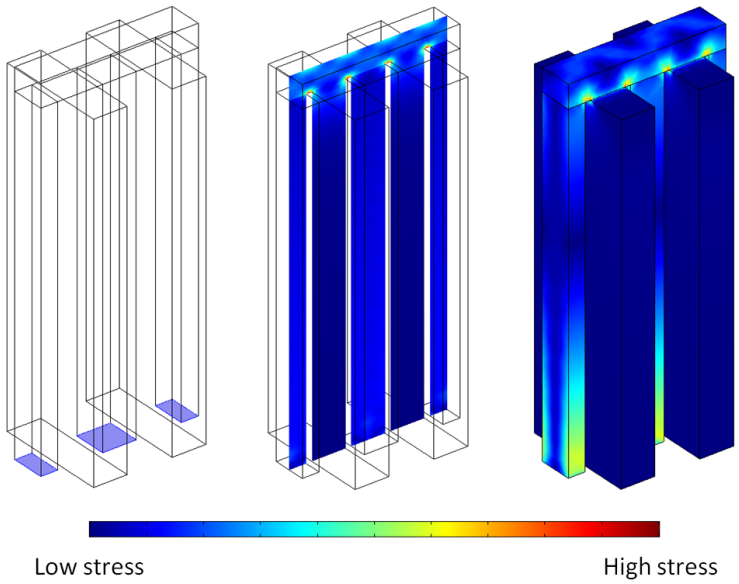


Figure 3.8: Stress simulation of a V2 membrane without spacers.
View indicating the fixed boundaries (left). Cross- sectional view (middle). Surface view (right).

Figure 3.9 shows the simulation results of a V2 model with spacers. In this model, the stress is more uniformly distributed over the nitride suspension. Based on this result, we can state that the addition of spacers can increase the load bearing capacity of V2 membrane structure.

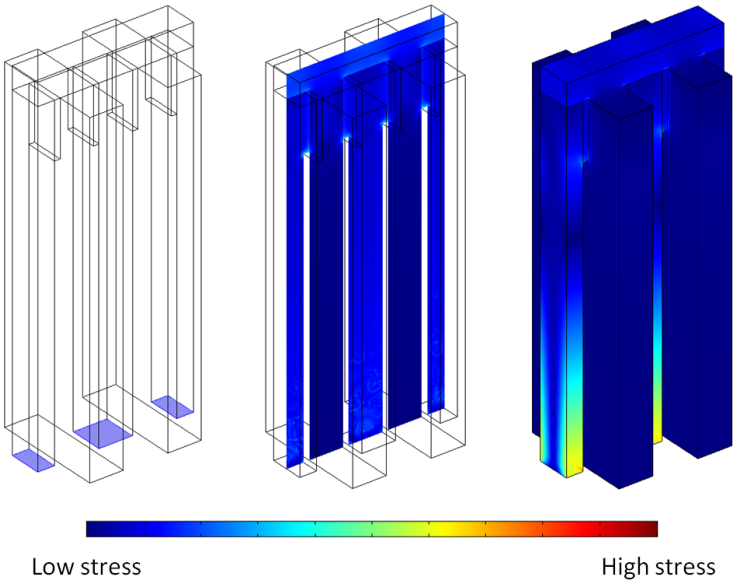


Figure 3.9: Stress simulation of a V2 membrane with spacers.
View indicating the fixed boundaries (left). Cross- sectional view (middle). Surface view (right).

An alternative solution to evenly distribute stress is adding anchoring points on the bottom of suspended nitride beams. This method is referred to as double clamping. The simulation results of double clamping are shown in Figure 3.10. We can see that the stress not only distributed over the nitride suspension, but over the entire membrane. This is an added advantage of double clamping and can greatly increase the overall membrane robustness.

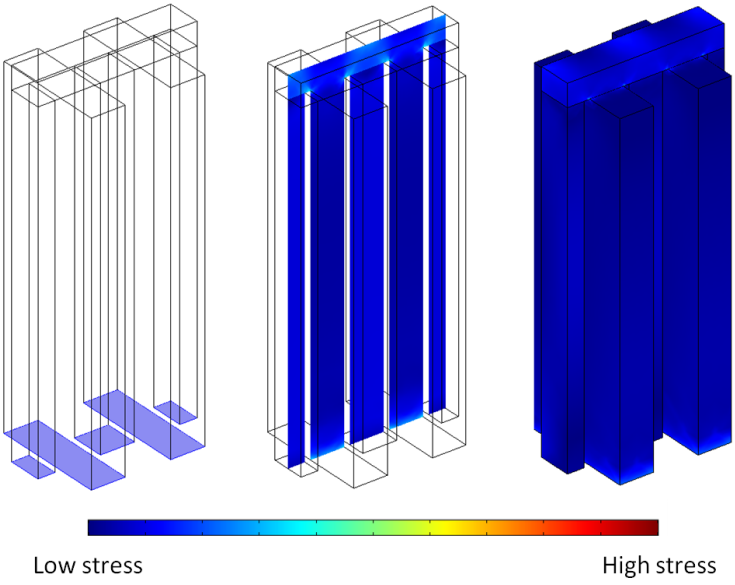


Figure 3.10: Stress simulation of a V2 membrane with double clamping.
View indicating the fixed boundaries (left). Cross- sectional view (middle). Surface view (right).

3.3.2 Voids in the nitride beams

The SiN beams are casted with 1.5µm LPCVD SiN (Figure 3.3f) which is in theory, an adequate amount to fully fill the 3µm wide molds. However in reality, voids persist in the suspended SiN beams after the deposition process and become accessible in the final stages of the fabrication process (Figure 3.11).

The voids in the nitride beams can cause a failure if they are larger than the pore size. Each void will then form a direct bridge between the in- and outlet channel that bypasses the porous membrane, allowing non-intended particles to reach the outlet. We have approximated the size of the entrance to the voids to be 300nm in width. It would therefore pose no problem for our V2 membrane with 500nm pores. However, these voids are a limiting factor for pore downscaling.

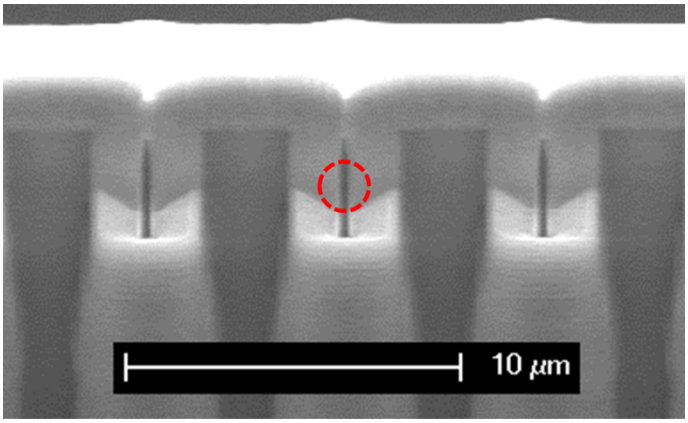


Figure 3.11: Voids in the V2 nitride beams.

The cause of the voids can be traced back to DRIE. DRIE is a process that etches silicon directionally and can create high aspect ratio structures. However, a non-ideality persists in DRIE that etches silicon outside the predefined regions. This non-ideality is commonly known as undercut. Figure 2.13 illustrates how DRIE undercut can cause accessible voids when subsequent LPCVD and dry etch processes are involved.

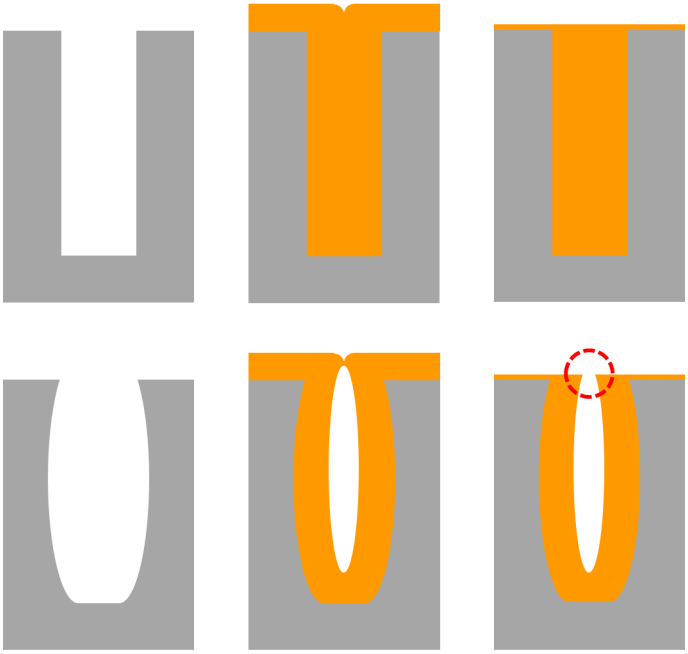


Figure 3.12: Ideal DRIE + LPCVD SiN + dry etch (top series).
Non-ideal DRIE + LPCVD SiN + dry etch (bottom series).

3.3.3 Dry film photo-resist seal

In subsections 2.3.2 and 2.3.3, the standardized DFR sealing method and the possibility of using glass to reinforce the DFR seal are introduced, respectively. With the glass reinforced DFR seal, V1 devices were able to function at operating pressures up to 400kPa. However, this pressure performance could not be achieved using V2 devices.

Figure 3.13 depicts the layout of the V2 device which very much resembles that of the V1 device (Figure 2.18). The main difference is the amount of area above the membrane that is in contact with the DFR seal. The DFR contact area of the V2 membrane is 25% less compared to V1. This reduction has a critical effect on DFR adhesion qualities. Even at the low operating pressures (<5kPa) the DFR seal would locally delaminate from the surface of membrane, causing numerous paths for unintended particles to pass into the outlet channel. This type of defect was both found for V2 devices with and without glass reinforcement.

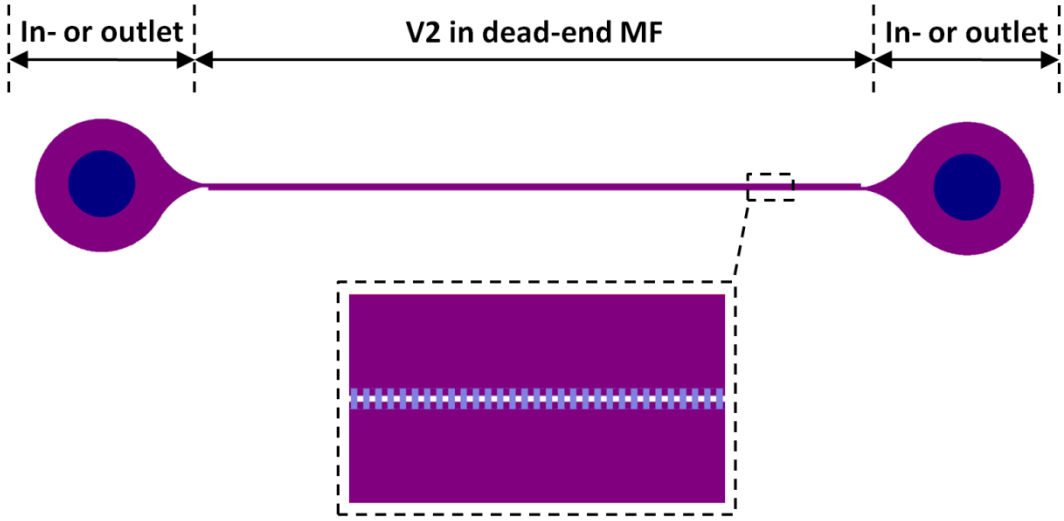


Figure 3.13: Layout of the V2 filter device.

3.4 Discussion

The main advantages and disadvantages of the V2 design are:

+ Fabrication requires only three materials, all of which are conventional MEMS materials.
+ Pores sizes defined by thermal silicon oxide growth parameters, not by photolithography.
+ Requires two photolithography masks for its structural components.
+ Efficient use of area, by extending pores vertically into the substrate.
− The suspended nitride beams limit the length of the pores.
− Relatively fragile membrane, because large stress gradients persist in the silicon beams.
− The minimum pore size is limited to 300nm due to voids.
− The DFR seal fails at operating pressures higher than 5kPa.

The V2 design is a promising concept, but does not reach its full potential. Critical issues from a number of sources degrade and limit its performance to such a degree that it is close to dysfunctional. In order to fully exploit the advantageous aspects presented in this chapter, a redesign of some of the geometrical elements of the V2 membrane is necessary.

4 The third design: a buried porous membrane formed by isotropic etch

A new (V3) vertical filter design was developed during this thesis study based on the knowledge and experience gained from the preceding designs. The V3 design aims to incorporate the advantages of both the V1 and V2 designs while avoiding their disadvantages.

4.1 Concept

At first glance, the V3 design looks similar to the V2 design (Figure 4.1). However, the V3 design actually has many new aspects that make the design unique.

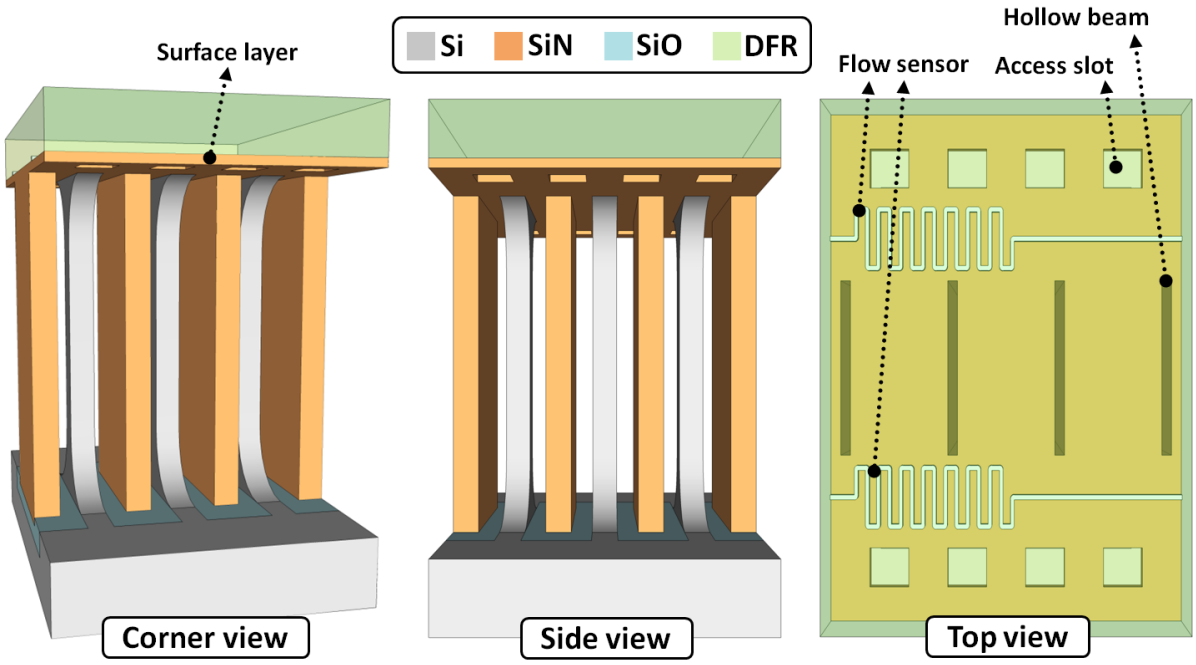


Figure 4.1: Conceptual drawings of the third micro-fluidic filter from different perspective points of view.

The V3 membrane and its microchannels are completely buried below a flat nitride surface layer on which additional features, such as actuation or sensing elements, can be integrated. The nitride layer is perforated with access slots for the formation of the underlying porous membrane during fabrication. These access slots are sealed by DFR.

The top view of Figure 4.1 shows a possible application of the nitride surface layer using a flow sensor. The flow sensor works by heating the incoming fluid at a specific time by means of a dissipative element, e.g. a resistor. The heated fluid passes through the membrane and, at an incremented time, flows by a thermistor that reacts on the temperature change. The fluid flow rate can be resolved from the time between initiation by the resistor and detection by the thermistor.

Under the nitride surface layer lies the V3 membrane which resembles that of the V2 design as it too is made up of alternating silicon and nitride beams with slit-shaped pores in between. However, the V3 membrane differs in:

- The nitride beams are now clamped into a fixed position.
- The fabrication method, the membrane is defined by isotropic etch and not anymore by photolithography.

The main drawback of the V3 design is that several new process parameters had to be introduced and quantified in order to implement the new concepts. This left little room to optimize the process parameters within the available time frame.

4.1.1 Dimensions

Devices with 500nm pore sizes have been fabricated based on the V3 design. Scaled drawings of a 500nm device are provided in Figure 4.2.

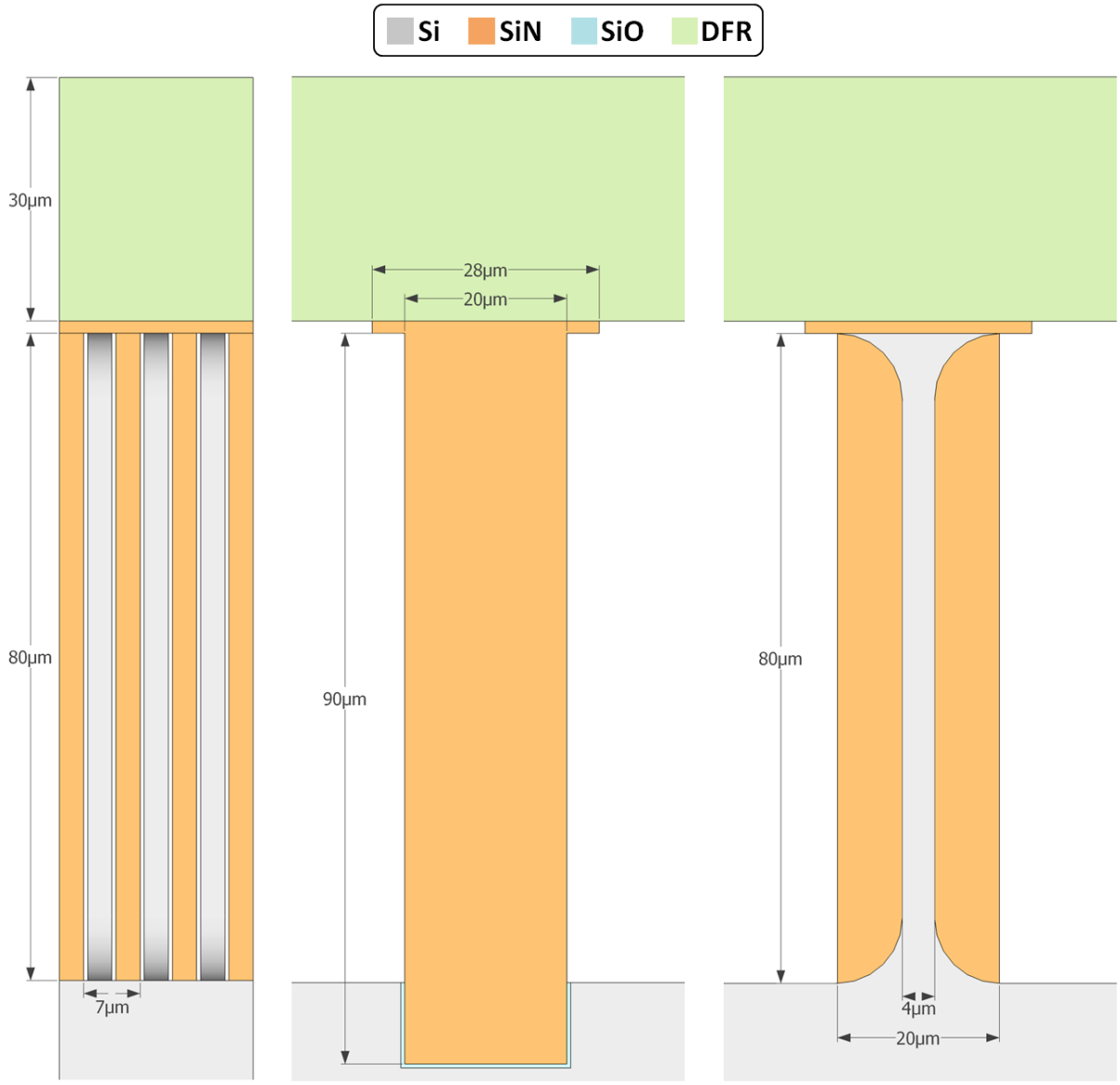


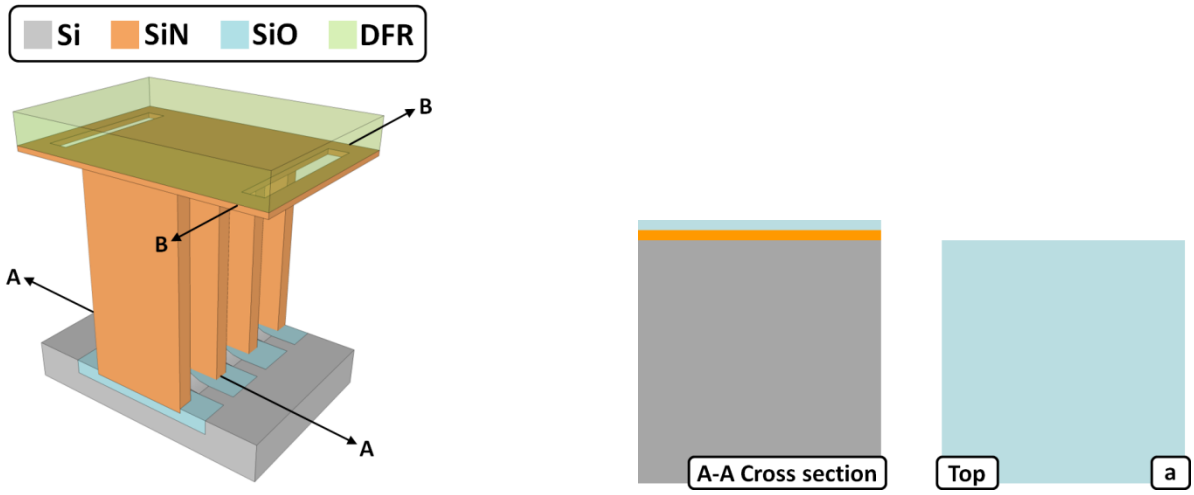
Figure 4.2: Scaled drawings of the third MEMS filter, dimensions included.
Side view (left). Cross-sectional view of nitride beam (middle). Cross-sectional view of silicon beam (right).

The V3 design was fabricated with a number of access slot configurations pitched 4µm from the porous membrane. An overview of these configurations can be found in Appendix B. The standard access slot configuration is an uninterrupted 20µm wide slit running along the length of the membrane. The membrane itself is periodic every 7µm and is approximately 8.4mm in length.

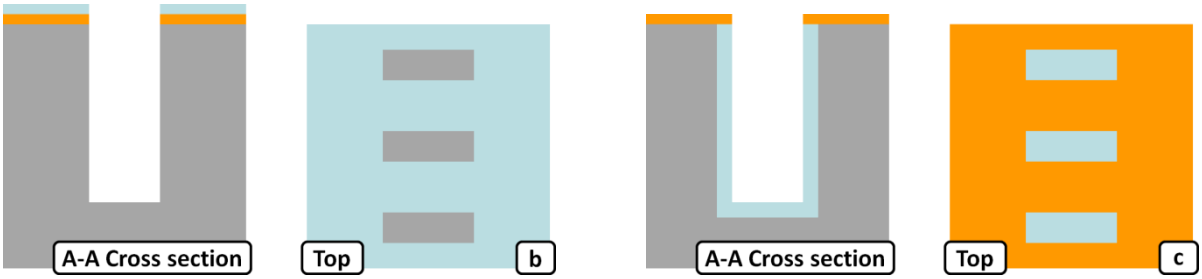
The V3 membrane is significantly larger than the preceding designs. This increase in size is done without sacrificing much of the porosity. Overall, this equates to a reduction of flow resistance, resulting in enhanced flow performances.

4.2 Fabrication process

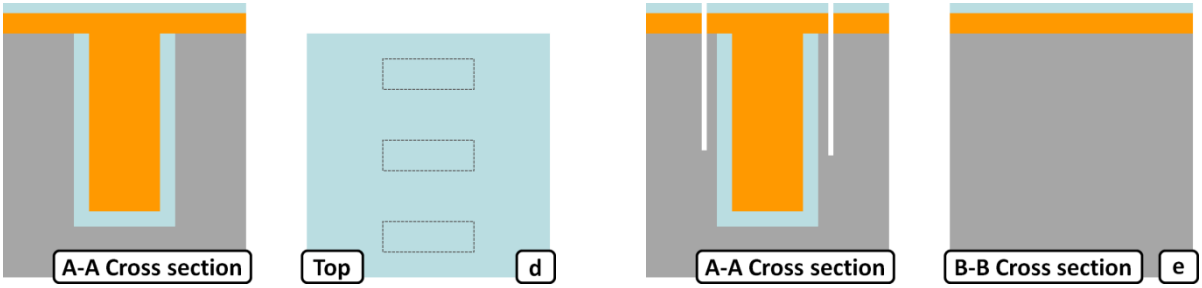
The following section contains the key fabrication steps for a V3 device with 500nm pores. The steps are presented with schematic views and outlined textually. A more detailed and complete process flow is included in Appendix A. The following uncaptioned pictures are referred to as Figure 4.3.



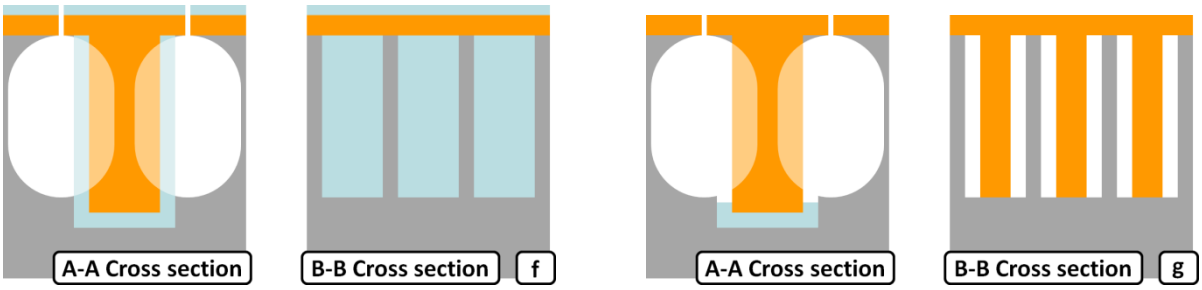
(a) A layer of 500nm LPCVD SiN and a layer of 2µm PECVD SiO are deposited on a 500µm thick Si substrate. The SiN deposition excludes the surface from thermally oxidizing in step *c* and the SiO layer functions as mask during DRIE in step *b*.



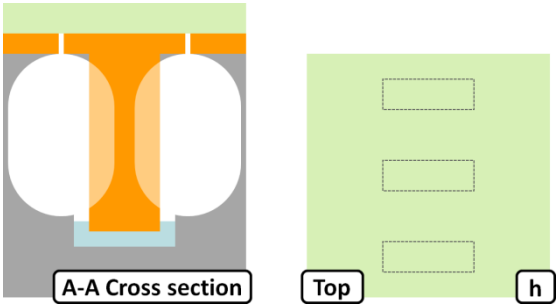
(b) A row of 3µm by 20µm rectangles pitched 7µm are patterned on the substrate. A dry anisotropic etch transfers the pattern onto the SiO mask and the underlying SiN layer. DRIE then follows and etches the Si substrate until 90µm deep molds are formed.
(c) The remaining SiO mask and sidewall polymer left by DRIE is removed. The wafer is thoroughly cleaned and then thermally oxidized to form 500nm thermal oxide on the inner Si faces of the molds.



(d) The oxidized molds are then covered with 1µm LPCVD SiN to create hollow SiN beams, and 2µm PECVD SiO is deposited as mask for DRIE in step *e*.
(e) The substrate is patterned with the access slots and etched in the same manner as step *b* for an etch depth of 70µm inside the Si substrate.



(f) Low biased SF_6 plasma is used to penetrate the SiN surface layer through the access slots and etch the Si substrate isotropically until the membrane reaches the desired thickness of 4µm.
(g) With the membrane etched and the thermal oxide layers accessible, the substrate is subjected to a 1 hour BHF etch to release the slit-shaped pores.



(h) The V3 devices are finalized by sealing the access slots using DFR.

SEM images of a V3 device during fabrication are shown in Figure 4.4 and Figure 4.5.

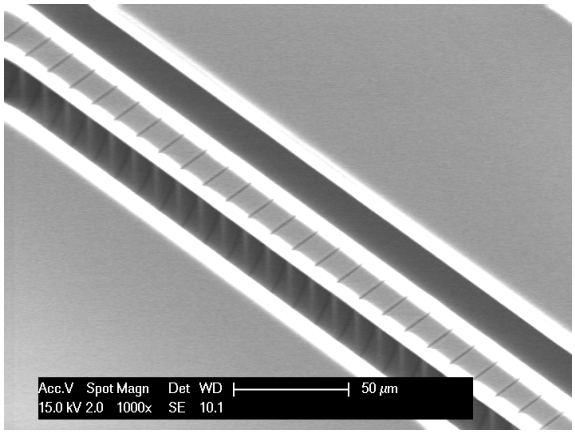


Figure 4.4: V3 device processed through step *f*. Corner view.

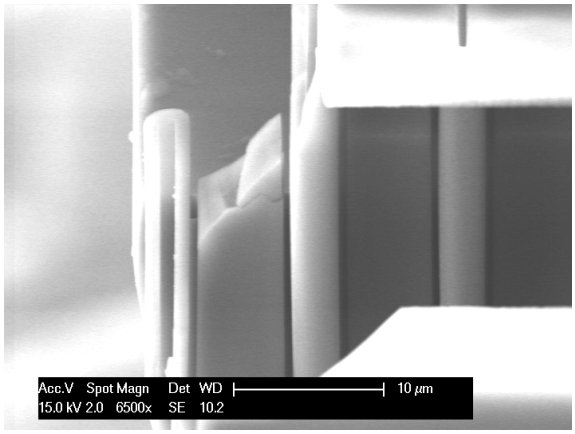


Figure 4.5: V3 device processed through step *g*. Side view.

4.3 Design analysis

4.3.1 Nitride beams

The suspended nitride beams of the V2 design put a strict size constraint on the V2 membrane. In order to prevent this issue in the V3 design, double clamping was applied. Instead of being suspended, the V3 nitride beams are constrained on both ends between the nitride surface layer and the silicon substrate. The effectiveness of double clamping was proven through simulations in subsection 3.3.1. With double clamping, there was no immediate size limitation on the V3 membrane. Confident about this statement, we successfully fabricated and tested V3 membranes have twice the height of V2 membranes.

Another V2 issue concerning the nitride beams was the persisting voids caused by DRIE undercut. These voids offer an undesired path for small particles to directly pass into the outlet channel. The V3 design is free from this issue, because the entrances to the voids are on the same plane as the surface of the microchannels. The voids are therefore sealed together with the microchannels by DFR, effectively eliminating the undesired fluid paths. This advantageous feature is exploited further by intentionally depositing less nitride into the beams, leaving hollow nitride beams as a result (Figure 4.6). While this action has no direct consequences for the functionality of the V3 membrane, it does contribute to cost-saving.

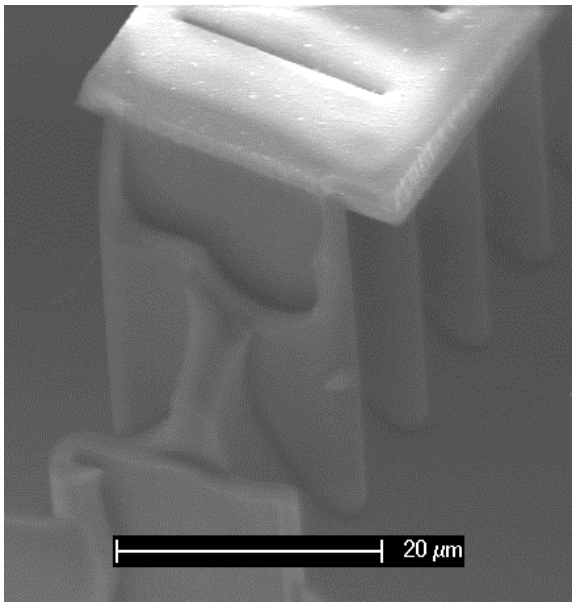


Figure 4.6: Cross section of hollow nitride beams.

Caution must be taken with the hollow nitride beams, because when additional elements are to be integrated on the nitride surface layer, a planar surface should be created. A planar surface is something that the hollow nitride beams does not provide on its own. To overcome this, the nitride beams can be either fully filled with LPCVD SiN, or still remain partially filled and planarized using a relatively non-conformal deposition process, such as PECVD SiO.

4.3.2 Two-stage etch

Figure 4.3e-f presents a two-stage silicon etch that penetrates the nitride surface layer from the access slots to form the V3 membrane and the corresponding microchannels. This two-stage etch is outlined in more detail in Figure 4.7.

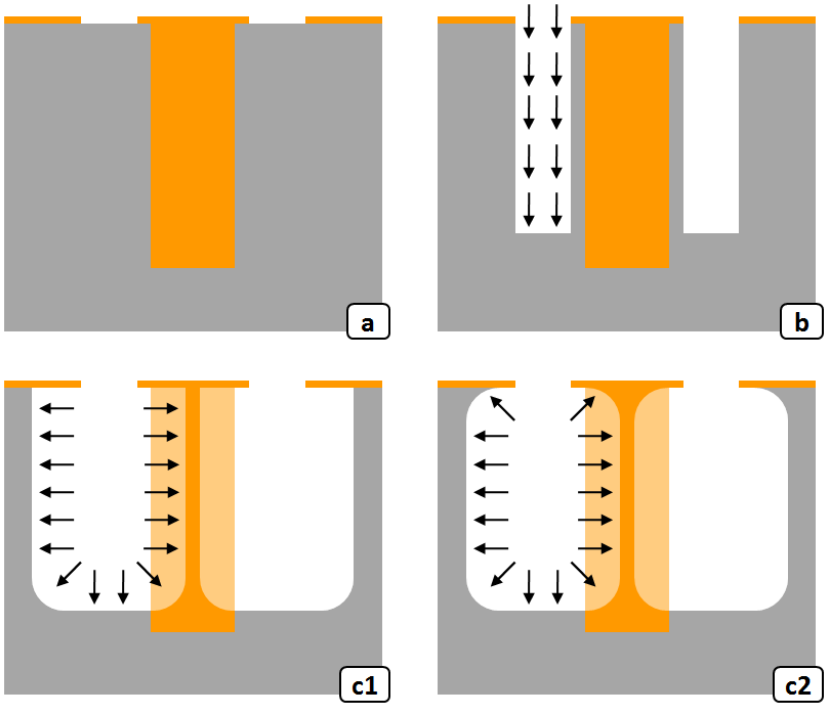


Figure 4.7: Illustration of two-stage etch. Cross section of buried membrane with access slots (a). Directional etch with DRIE (b). Isotropic etch with HNA (c1). Semi-isotropic etch with low biased SF_6 plasma (c2).

During the development of the V3 design, different options were considered in order to choose the best method to perform the two-stage etch. For the first etch stage, it quickly came down to DRIE, because a 70µm high-aspect ratio etch was required. However, for the second etch stage which should be an isotropic etch, there were two equally viable options:

- Wet etching with a solution of hydrofluoric acid, nitric acid and acetic acid (HNA).
- Dry etching with low biased SF_6 plasma (parameters of this etch are included in Appendix A).

Both options were explored and the resulting etch profiles are shown in Figure 4.8 and Figure 4.9, respectively.

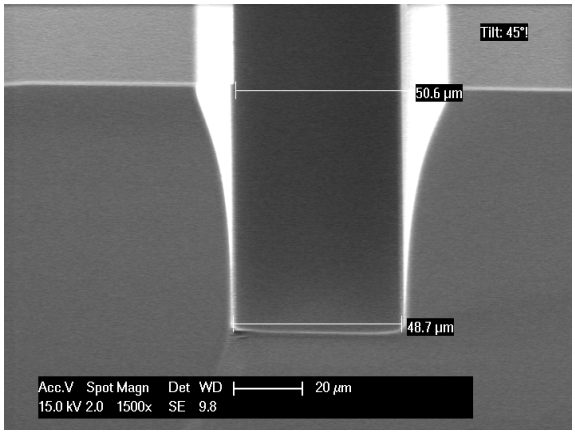


Figure 4.8: Etch profile with HNA.

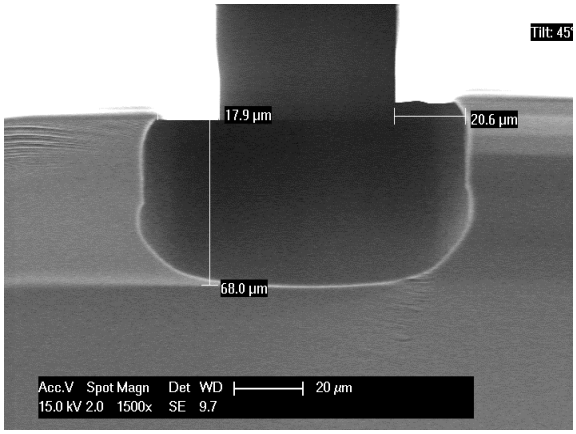


Figure 4.9: Etch profile with low biased SF_6 plasma.

The HNA etch shows an unexpected profile suggesting that the etch rate is non-uniform. The reason for this can be the static bath in which the etch was performed, where the lack of stirring lead to poor local replenishment of HNA. This phenomenon is better known as loading.

The low biased SF_6 dry etch on the other hand, shows good results and was therefore further explored by using a situation closer to reality. Figure 4.10 depicts this situation. We can see that the dry etch is clearly able to form a (non-porous) vertical membrane according to expectations. Based on these observations, the dry etch option was deemed to be the best and was implemented as the second etch stage of the two stage-etch.

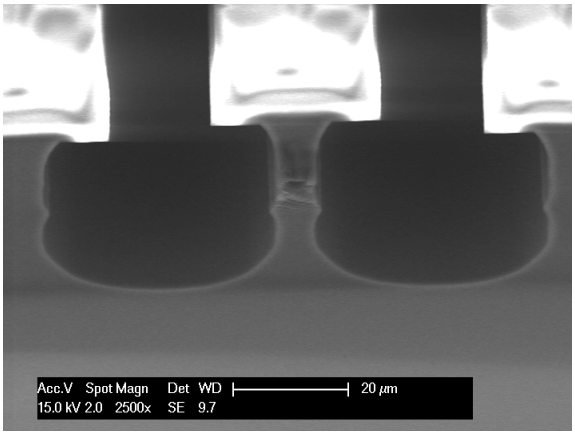


Figure 4.10: Non-porous vertical membrane created by low biased SF_6 plasma as second etch stage.

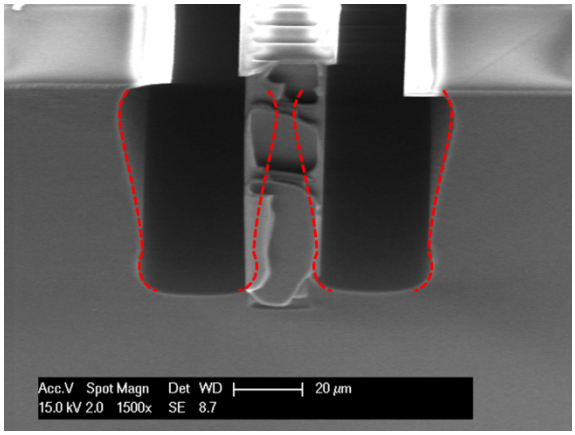


Figure 4.11: Non-uniform membrane thickness due to loading effects. Red lines show the two-stage etch profile.

V3 membranes up to approximately 50µm in height can be repeatedly fabricated using the two-stage etch. However, loading effects become dominant when larger membranes are formed (Figure 4.11). Loading results in a non-uniform membrane thickness with certain regions significantly thicker than others. This leads to an increase in the flow resistance and is therefore highly undesired.

4.3.3 Nitride surface layer

A number of different access slot configurations were designed and fabricated. The V3 SEM pictures shown until now contain only devices with the standard configuration, one that has no individual slots, but a slit extended along the V3 membrane. This standard configuration was intended as proof of concept, while other access slot configurations were meant to implement the nitride surface layer. An overview of these different configurations is included in Appendix B. The real access slot configurations with the most promising results are shown in Figure 4.12 and Figure 4.13.

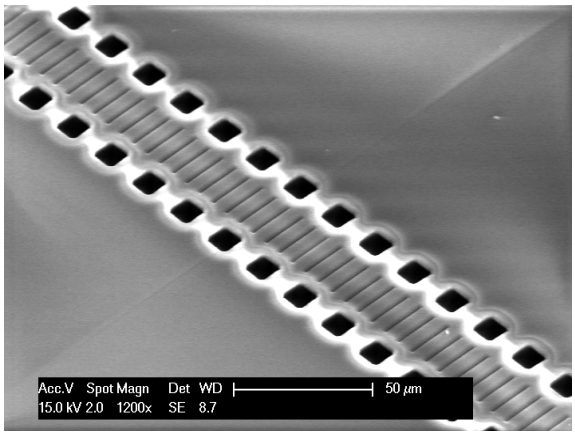


Figure 4.12: Access slot configuration with 10x10µm squares pitched 10µm. Corner view.

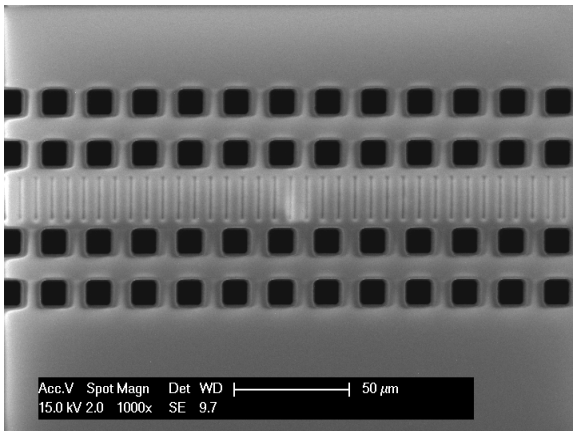


Figure 4.13: Access slot configuration with two rows of 10x10µm squares pitched 10µm. Top view.

Figure 4.14 shows the cross section of another promising configuration. However, the microchannels, created by the two-stage etch, show severe signs of loading. We found that loading is related to the amount of nitride surface layer that remains intact. This is reasonable since the surface layer forms a natural obstruction for the SF_6 plasma required to etch the microchannels.

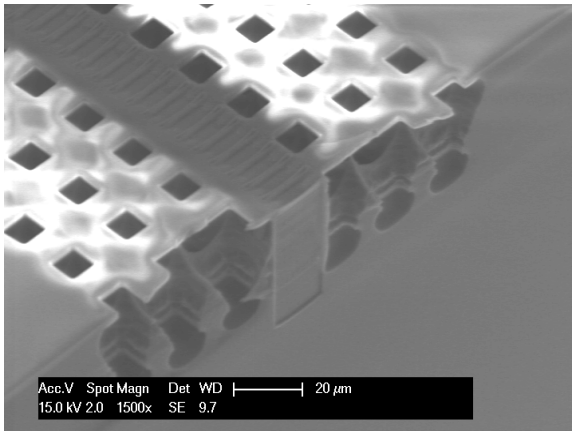


Figure 4.14: Access slot configuration with three rows 10x10µm squares pitched 10µm. Cross-sectional view.

4.3.4 Dry film photo-resist seal

Devices of the preceding designs had issues with the robustness of the DFR seal (Subsections 2.3.3 and 3.3.3). This was mainly because some structural aspects of those designs were not optimized to be sealed with DFR. The V3 design however, was dimensioned specifically to function well with a DFR seal.

Compared to V1, the V3 design has 5 times smaller in- and outlets (Figure 4.15), and about 7 times larger DFR contact area above the membrane. Fluidic experiments showed that these improvements enable V3 devices to operate at pressures up to at least 700kPa without any additional reinforcement.

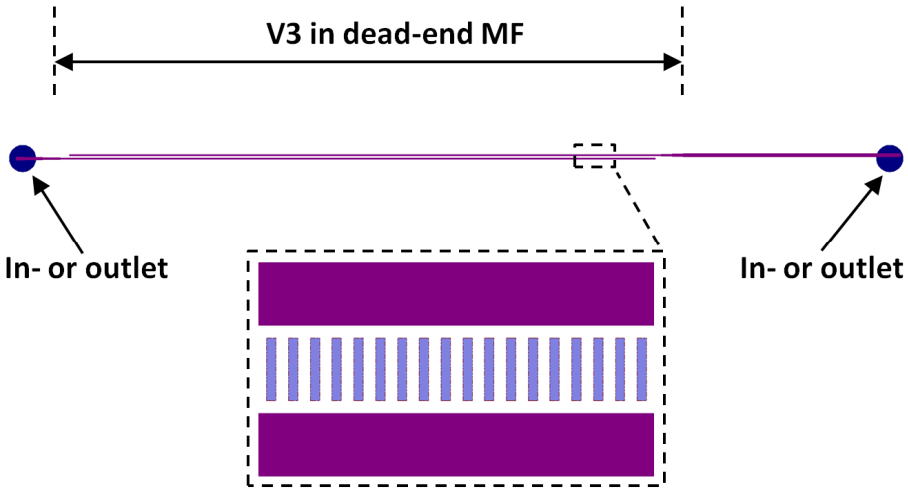


Figure 4.15: Layout of the V3 filter device.

4.4 Discussion

The main advantages and disadvantages of the V3 design are:

+ Fabrication requires only three materials, all of which are conventional MEMS materials.
+ Pores sizes defined by thermal silicon oxide growth parameters, not by photolithography.
+ Requires two photolithography masks for its structural components.
+ Efficient use of area, by extending pores vertically into the substrate.
+ Is buried and allows for integration of additional elements on the surface.
+ Performs at operating pressures over 700kPa without additional reinforcement.
− Non-uniform membrane thickness for large membranes.
− Implementation of access slots leads to poorly shaped microchannels.

The V3 design addresses and solves the problems and limitations encountered in the V2 design. However, the development of this design resulted in new issues that are yet to be addressed. Despite the addition of new issues, we were still able to fabricate V3 devices that are fully functional for fluidic experiments.

5 Validation

We have performed a series of fluidic experiments to verify the functionality and performance of the fabricated filter designs. This chapter contains the results and conclusions of these experiments.

5.1 Experiment setup

During this thesis work, many filter devices with a variety of structural parameters were fabricated. Even amongst the same design, devices can differ in:

- The depth of the microchannels.
- The number of in- and outlets.
- The pore size.
- The periodicity of the membrane.
- The length of the membrane.
- The membrane configuration.
- When applicable, the access slot configuration.

The intension at first was to benchmark all the different filter devices and make a fair comparison amongst the results. However, due to time restrictions, only a select few were eventually tested. The devices under test (DUT) for the experiments in this chapter are limited to MEMS filters:

- With 500nm pores.
- Configured in dead-end filtration.
- Fabricated according to the dimensions given in subsections 2.1.1, 3.1.1 and 4.1.1.

5.1.1 Device preparation

The fabricated wafers containing the DUT were cut into 20mm by 20mm dices for better handling. Each dice contains up to 3 DUT and each DUT has 2 microchannels connected to 2 in- or outlets on the backside of the dice (Figure 5.1).

To prepare the DUT for the experiments, a dice was mounted into a custom crafted poly methyl methacrylate (PMMA) holder and fixed into position with an aluminum frame (Figure 5.2). Rubber spacers were used to create a tight seal between the DUT and holder. The PMMA holder formed the interface between the in- and outlets on the dice and fluorinated ethylene propylene (FEP) tubes in the measurement setup.

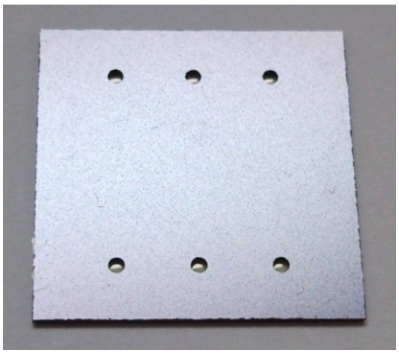


Figure 5.1: Backside of V1 DUT.

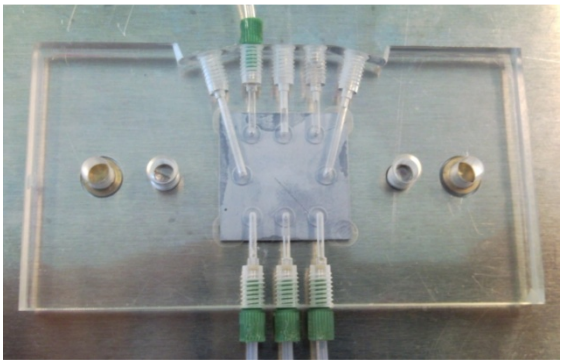


Figure 5.2: PMMA device holder.

5.1.2 Measurement setup

A complete list of the equipment used for the experiments is given below.

- 20mm by 20mm PMMA device holder.
- 0.5mm inner diameter FEP tubes.
- *BD* 5ml plastic syringe.
- *KDScientific* syringe pump.
- *Alltech* 0-100psi (700kPa) differential liquid pressure gauge.
- *Olympus IX71* fluorescence microscope.

The basic configuration for the fluidic experiments is depicted in Figure 5.3. A syringe containing the desired fluid is driven by a pump to output a constant flow rate. The fluid travels through a FEP tube into a pressure gauge. From there, the fluid enters the DUT through another FEP tube.

A fluorescence microscope was used to directly observe the device during the experiments involving fluids with fluorescent particles. Direct observation is possible because the PMMA holder has a window in the aluminum frame and the DUT are sealed using transparent materials.

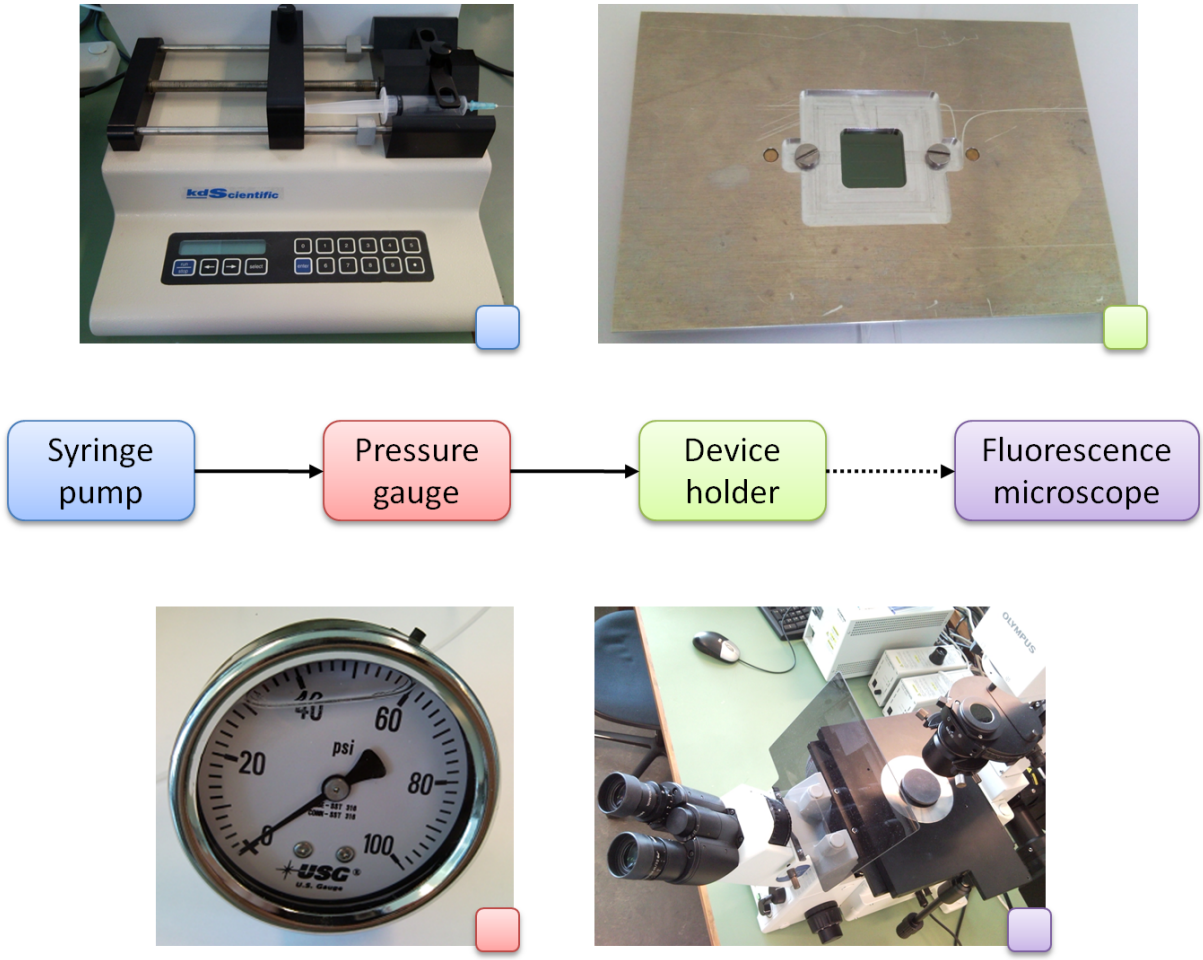


Figure 5.3: Measurement setup for the fluidic experiments.

5.2 Filter function

The most fundamental requirement for a filter is the ability to separate target particles. To confirm that this requirement is met, 2µm yellow fluorescent polystyrene beads were suspended in DI water and let into the DUT. Observations were made with a fluorescence microscope.

5.2.1 Separation experiment

All DUT have membranes with 500nm pores and are configured for dead-end filtration. Therefore, all of the fluorescent particles, which are larger than the pore size, should be blocked by the membrane and remain in the inlet channel.

The results are positive and consistent. As long as the seal and membrane are undamaged, the DUT of each design can provide basic filter functionality as shown in Figure 5.4.

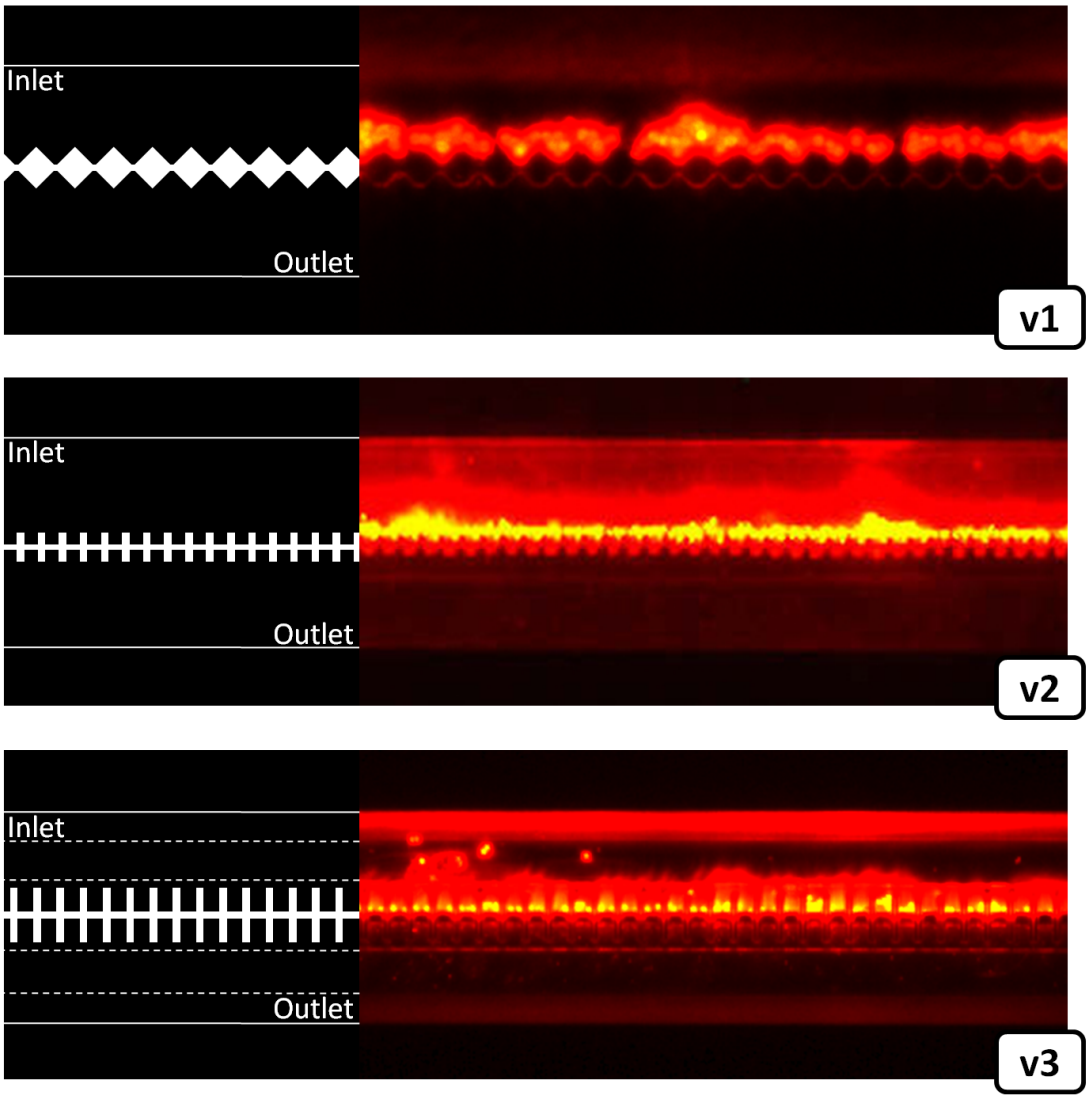


Figure 5.4: Filter experiment with devices from the three studied designs using 2µm yellow fluorescent beads.
Augmented views that outline the respective filter designs (left).
Fluorescent views of functional filters (right).

5.2.2 Clogging experiment

Due to the basic principle of MF, filtered particles remain behind on the membrane. These particles accumulate during separation and will eventually block the flow over time. One simple and commonly applied method to clean a clogging membrane is to feed it with a particle-less fluid in the opposite direction, thereby flushing the particles away through the inlet channel. This cleaning method is called back-flushing.

To demonstrate clogging and back-flushing, we have performed an extended version of the separation experiment. A short (350µm long) V3 device was chosen as DUT.

Figure 5.5 contains several pictures taken during the experiment, with:

a. Normal microscope view.
b/c. Fluorescence microscope views at 30 minute intervals showing the 1st cycle of filtration.
d. Fluid flow reversed for 5 minutes to clean the membrane.
e/f. Fluorescence microscope views at 15 minute intervals showing the 2nd cycle of filtration.

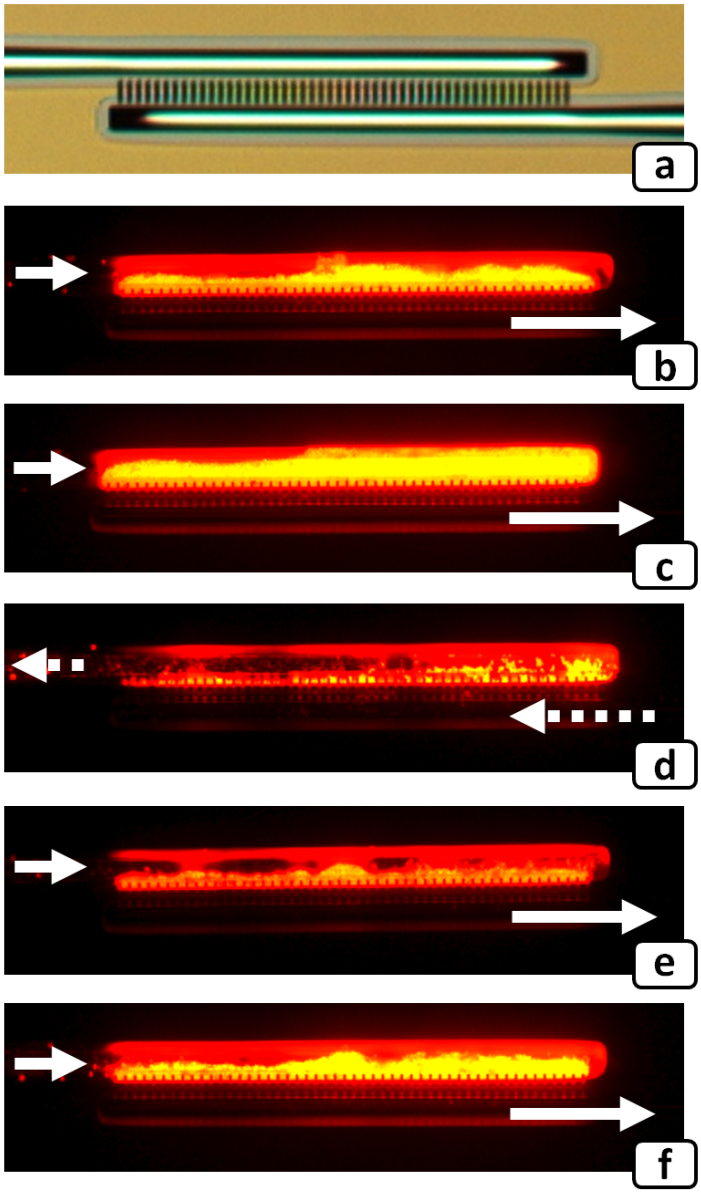


Figure 5.5: Fluidic experiment with 2µm yellow fluorescent beads.
The fluid flow directions are indicated by white arrows.

5.3 Pressure performance

Modern LC systems [14] rely on ultra high pressures (>100MPa) to achieve flow rates in the order of milliliters per minute. These systems emphasize the fact that with a large enough operating pressure, high resistance devices can still perform at decent flow rates. It is therefore interesting to know the pressure limits of our devices. Experiments using pressurized DI water were performed for this purpose. The results are summarized in Table 5.1.

Table 5.1: Results of pressurized fluidic experiments

Design	Glass reinforced DFR seal	Highest operating pressure (kPa)	Breaking pressure (kPa)
V1	✗	<40	40
	✓	400	700
V2	✗	<15	<15
	✓	<15	<15
V3	✗	>700	>700
	✓	>700	>700

When considering the results from devices with the basic DFR seal, the DUT from the V1 and V2 designs perform relatively poor. This is due to their in- and outlets which have dimensions in the order of millimeters. DFR behaves very inadequately and is prone to breakage when it has to span these distances in order to seal the device (Subsection 2.3.3).

Devices with glass reinforced DFR have differing results. The V1 DUT showed improved pressure ratings, an order of magnitude greater than without glass. However, no improvement was found for the V2 DUT even though both the seal and membrane seemed undamaged at first sight. The problem became clear when we traced the fluid flow using fluorescent particles. We found that the 2µm particles were able to cross the 500nm porous membrane at numerous areas along the membrane. Apparently, despite the added glass reinforcement, the DFR seal could not adhere to the small surface area above the V2 membrane at any pressure values within our 2psi (approx. 15kPa) resolution pressure gauge. Even at the lowest measurable settings, the DFR seal would locally delaminate above the V2 membrane, causing the DUT to the malfunction.

The V3 design was made specifically to work well with the DFR seal. The in- and outlets were minimized and the surface area above the membrane was maximized. A good pressure performance was expected and this was indeed the case. For all measured devices, the pressure was limited by our 100psi (approx. 700kPa) pressure gauge rather than by the V3 DUT.

5.4 Flow performance

The flow performances of the filter designs are assessed in this section. Simulations, calculations and experimental validation are reported and compared.

5.4.1 Finite element simulations

The flow resistances for each design were simulated using a finite element analysis tool (COMSOL Multiphysics). The simulation parameters are listed in Table 5.2.

Table 5.2: COMSOL flow resistance simulation parameters

Parameter	Value	Unit
Fluid density	1e3 (water)	kg/m^3
Fluid dynamic viscosity	1e-3 (water)	Pa·s
Wall condition	no slip	-
Inlet	1.1e5	Pa
Outlet	1.0e5	Pa

For short computing times (<hours), the simulation models were simplified by assuming:

- A unit section of a membrane is representative for the entire membrane.
- The flow resistance is proportional to the pressure and inversely proportion to the flow rate.
- There are no pressure losses other than due to the membrane.

Figure 5.6 shows an overview of the simulated models. We can see that the main pressure drop occurs over the membrane and that there are no losses (pressure gradients) in the microchannels.

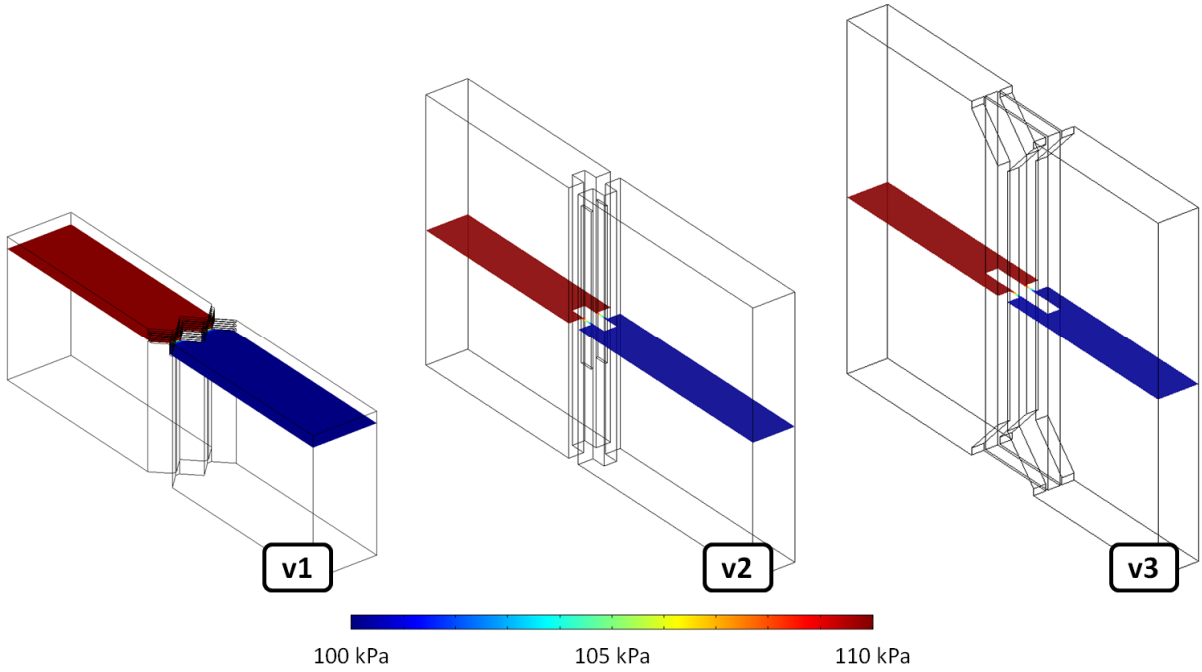


Figure 5.6: Overview of COMSOL simulated models (pressure).

Figure 5.7 contains an expanded view of the simulated models, showing more details of pressure gradient inside the pores.

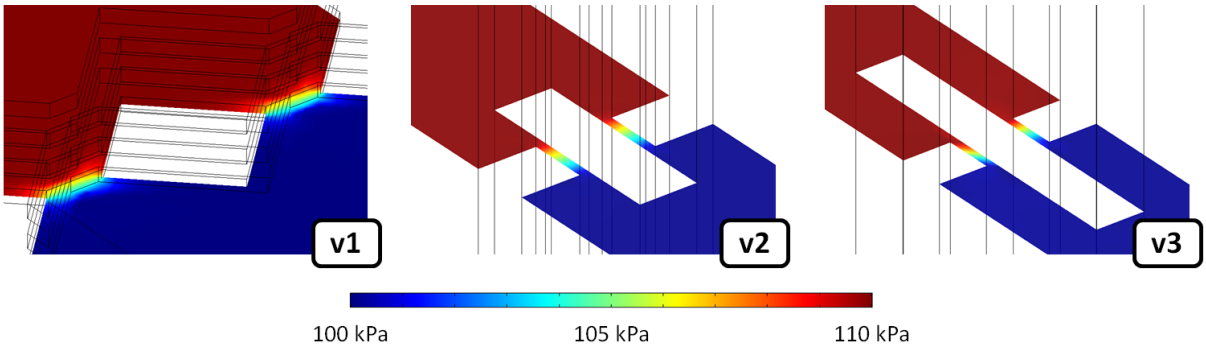


Figure 5.7: Expanded view of COMSOL simulated models (pressure).

Figure 5.8 shows again the same models, but now colored according to the simulated flow velocity. We can see that the flow is laminar and that there are entry and exits effects extending far beyond the geometries of the pores.

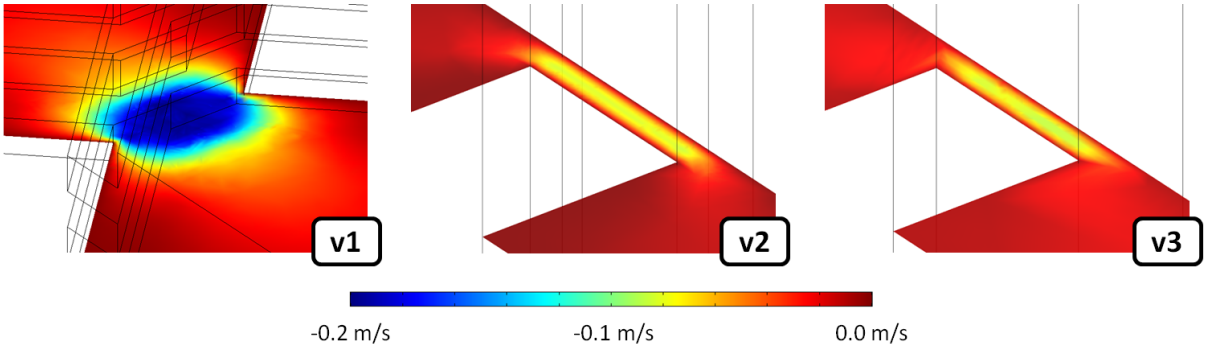


Figure 5.8: Expanded view of COMSOL simulated models (flow velocity).

A sufficiently dense simulation grid was used so that the finite element simulations would converge with a small error. A good indicator of whether or not the error is small, is by comparing the flow rates at the in- and outlet. In any practical scenario, or errorless simulation, the flow rates should be equal.

To make a fair comparison between the different designs, a figure of merit (FOM) is introduced in Equation 5.1. Note that the unit surface area required is not the actual area, but the area of the smallest rectangle that can fit around the membrane. An ideal filter design has a FOM of zero.

$$FOM = \frac{P \cdot n \cdot A_n}{VFR}$$

Equation 5.1: The figure of merit FOM with P the absolute pressure, n the number of units, A_n the unit surface area and VFR the volumetric flow rate.

The simulated flow values along with the FOM are presented in Table 5.3.

Table 5.3: Simulated flow values

Design	Flow rate (m^3/s)	Inlet to oulet ratio	Units	Unit surface area (m^2)	FOM
V1	7.19e-13	0.996	2	64e-12	1.78e6
V2	1.88e-12	0.995	1	60e-12	3.19e5
V3	3.66e-12	0.997	1	140e-12	3.83e5

5.4.2 Analytical calculations

The simulated values of the flow rates are confirmed in this subsection using Equation 5.2 which was derived from the general equations of motion by [22]. The solutions to the equation together with the input parameters are given in Table 5.4.

$$R_{f,sspore} = \left[\frac{-x \cdot y^3}{12 \cdot \eta \cdot z}\left(1 - \frac{192 \cdot y}{\pi^5 \cdot x} \cdot \left(tanh\left(\frac{\pi \cdot x}{2 \cdot y}\right) + \frac{1}{3^5} \cdot tanh\left(\frac{3 \cdot \pi \cdot x}{2 \cdot y}\right)\right)\right)\right]^{-1}$$

Equation 5.2: Flow resistance of a slit-shaped pore with $R_{f,r}$ the flow resistance, x the longest side of the channel, y the shortest side of the channel, z the length of the channel and η the fluid dynamic viscosity.

Table 5.4: Calculated flow values

Design	Approximated x, y, z dimensions (m)	Flow rate (m^3/s)	Units	FOM	FOM simulation to calculation ratio
V1	3e-6, 500e-9, 2e-6	1.40e-13	1/3	1.52e6	1.17
V2	35e-6, 500e-9, 3e-6	1.20e-12	1/2	2.50e5	1.27
V3	80e-6, 500e-9, 3e-6	2.77e-12	1/2	2.53e5	1.51

We can see from the FOM ratio that the calculated values are in good agreement with the simulated values. The differences are mainly due to entry and exits effects that are present when a fluids transits from or to a channel with a smaller cross section. These effects were accounted for in the simulations, but not in the calculations.

5.4.3 Experiments

Real flow values were obtained through experiments (Figure 5.9). This was only done for V1 and V3 DUT, because V2 DUT could not sustain the pressures required for reliable measurements. Figure 5.9 shows that both sets of measurement points indicate a linear relationship between the pressure and volumetric flow rate as predicted by Equation 1.3.

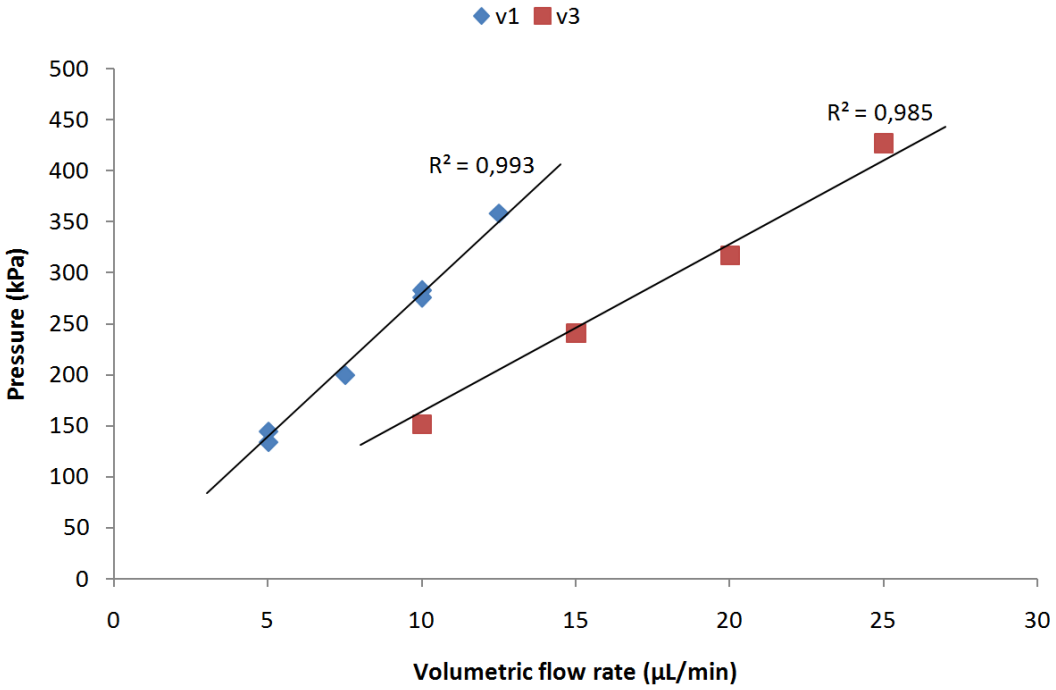


Figure 5.9: Pressure versus volumetric flow rate graph with measured data points.

Table 5.5 combines the experiment results and presents the corresponding FOM. It can be seen that the FOM for both designs are at least an order of magnitude larger than the FOM found by simulations. This is because the real flow resistance suffers from non-idealities, making it much greater than what was predicted by the idealized simulation models.

Table 5.5: Experimental flow values				
Design	Average pressure to flow rate ratio (Pa· s/m^3)	Units	FOM	FOM experimental to simulation ratio
V1	1.67e15	1220	1.30e8	7.30e1
V3	9.63e14	1200	1.62e8	4.23e2

5.4.4 Non-idealities

The V1 and V2 DUT have a number of non-idealities with different origins, ranging from fabrication, to design to fluid mechanics. We have already seen in subsections 2.3.1 and 4.3.2 that the shaping of the membranes is not completely accurate and that there are deviations from the intended design.

The assumption was made that the microchannels would result in no pressure losses, i.e. zero flow resistance. However, a separate set of simulations showed that this is not the case (Table 5.6). According to these simulation results, the flow resistance of the microchannels would equate to a membrane significantly smaller than the actual membrane present on the DUT. If we would have to take this into account in our models, we would have to expand them into complex resistance networks (Figure 5.10). However, without so, we can already qualitatively state that the microchannels are the dominant contributor to flow resistance.

Table 5.6: Simulated microchannel flow values					
Design	Microchannel x, y, z dimensions (m)	Flow rate (m^3/s)	Inlet to oulet ratio	Equivalent units	Actual units
V1	30e-6, 50e-6, 1e-2	6.99e-11	0.999	166	1220
V3	80e-6, 30e-6, 1e-2	1.38e-10	0.996	25	1200

In [23] was reported that the surface roughness of microchannels can degrade the flow performance of fluidic devices. This phenomenon might also have some effect on our DUT because the microchannels present in our devices were created using DRIE which is known to leave somewhat rough surfaces (Figure 5.11) [24].

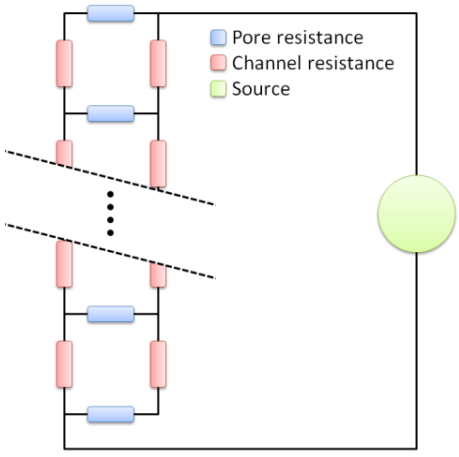


Figure 5.10: Analogous resistor network.

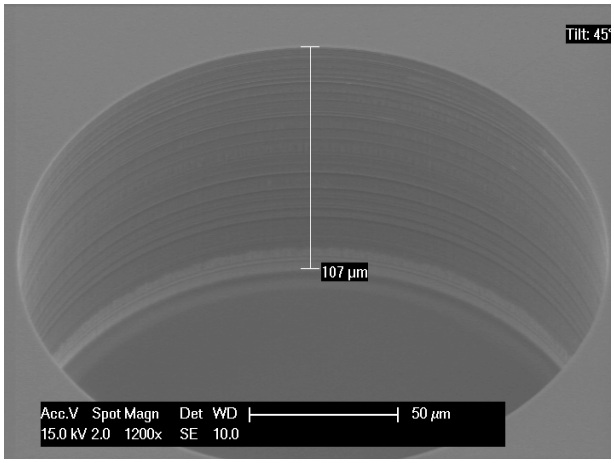


Figure 5.11: Rough side walls left by DRIE.

5.5 Discussion

The ability to separate particles by MF was confirmed for all DUT. However, some issues were found during the pressure and flow rate experiments:

- The V2 devices could not be tested.
- The microchannels form a dominant component of the overall flow resistance.

The aforementioned issues have strong impact on the contents of this chapter. However, they are less important on an overall scale, because:

- The V3 design is based on V2 concepts and can therefore be considered as its replacement, making the need for experimental data on V2 devices redundant.
- The configuration and dimensions of the microchannels are not an integral part of any of the considered filter designs. The option to tune the microchannels independently from the designs is therefore always present.

With this in mind, we can state from the results of this chapter that all MEMS filters designs are functional with the V3 design having the best pressure and flow rate performances.

6 Conclusion

“This thesis study seeks to identify and analyze reoccurring issues in the two MEMS filter designs and from those results, realize a new design that is superior in the aspects of performance, robustness and durability.”

The statement above contains the general problem that was constantly addressed throughout this thesis. In order to conclude to what extent our solution (the V3 design) meets the requirements, we have made a qualitative comparison of the three MEMS filter designs in Table 6.1. The table is color-coded for a better overview, with:

- Red, relatively poor.
- Orange, relatively medium.
- Green, relatively good.

Table 6.1: Comparison of the three filter designs

Category	Characteristic	V1	V2	V3
Pores	Orientation	horizontal	vertical	vertical
	Method of size definition	LPCVD SiO	thermal SiO	thermal SiO
Porous membrane	Thickness uniformity			
	Height	3µm	35µm	80µm
	Robustness			
	DFR contact area			
Filter device	Fabrication complexity			
	Integration capacity			
	Measured FOM	7.30e1		4.23e2
	Breaking pressure (no reinforcement)	40kPa	15kPa	700kPa

From the table above, we can conclude that the problem initially defined has been properly addressed. V3 is a novel design and although further optimization is still possible, it has proven to be the best amongst the three MEMS filter designs.

6.1 Publication

The work and results of the V3 design has been published in the conference proceedings of Eurosensors 2011. The publication can be found in Appendix C.

6.2 Future work

We would like to mention some relevant topics that could not be included in this thesis study, but could be pursued in the future.

6.2.1 Down-scaling

The V3 design is meant to function optimally in the lower range of microfiltration (100nm to 1µm particles). However, it has the capacity to be downscaled since the method of pore definition (thermal oxidation) is accurate for pore sizes down to ultrafiltration (10nm to 100nm).

6.2.2 Membrane configurations

Apart from dead-end MF and cross flow MF, we have included a few other membrane configurations in our photolithography masks that are designed to delay membrane fouling and optimize back-flushing. These configurations have not yet been optimized and tested.

6.2.3 Low flow resistance microchannels

The microchannels that were implemented to supply our porous membranes with fluids have a dominant influence on the overall flow resistance of the filter device. This is highly undesired. The microchannels should therefore be re-designed for low flow resistance.

6.2.4 Optimizing the two-stage etch

The etch profile of the two-stage etch of the V3 design can be greatly optimized by altering the etch parameters [25]. This should be further investigated, because an optimized etch can compensate for the observed loading effects and significantly improve the membrane thickness uniformity of the V3 membrane.

6.2.5 Surface device integration

The buried aspect of the V3 design keeps a considerable amount of the nitride surface layer intact throughout the fabrication process. The integration of additional features, like actuation and sensing elements, should be implemented on the surface layer for added functionalities.

List of abbreviations

AF4	Asymmetric flow field flow fractionation
BHF	Buffered hydrofluoric acid
DFR	Dry film photo-resist
DI	De-ionized (water)
DIMES	Delft Institute of Microsystems and Nanoelectronics
DRIE	Deep reactive ion etch
DUT	Device(s) under test
EFFF	Electrical field flow fractionation
FEP	Fluorinated ethylene propylene
FFF	Field flow fractionation
FOM	Figure of merrit
HNA	Hydrofluoric, nitric, and acetic acid
LC	Liquid chromatography
LPCVD	Low pressure chemical vapor deposition
MEMS	Micro electro mechanical systems
MF	Membrane filtration
PDMS	poly dimethyl siloxane
PECVD	Plasma enhanced chemical vapor deposition
PMMA	Poly methyl methacrylate
PR	Photo-resist
SEM	Scanning electron microscope
SH	Substrate holder
Si	Silicon
SiN	Silicon nitride
SiO	Silicon oxide
SU-8	(A name for a type of photo resist)
UV	Ultraviolet
V1	First MEMS filter
V2	Second MEMS filter
V3	Third MEMS filter

References

[1] S Kuiper, M de Boer, CJM van Rijn, et al., *Wet and dry etching techniques for the release of sub-micrometre perforated membranes*, Journal of Micromechanics and Microengineering 10, 2000, p.171-174.

[2] X Tan, HJ Yoon, J Granneman, et al., *A high-throughput microfluidic chip for size sorting of cells*, Proceedings of MEMS 2011, p.1075-1078.

[3] N Noeth, S Keller, S Fetz, et al., *Micro-particle filter made in SU-8 for biomedical applications*, Proceedings Transducers 2009; p.2034–2037.

[4] FE Regnier, *Microfabricated monolith columns for liquid chromatography*, Journal of High Resolution Chromatography, 2000, p.19-26.

[5] M Hiraoka, P Fiorini, L Zhang, et al., *Integrated fluidic system for bio-molecule separation*, Proceedings of EMBC 2010, p.6514-6517.

[6] NT Nguyen, ST Wereley, *Fundamentals and Applications of Microfluidics*, 2nd edition, ISBN1580539726.

[7] RW Fox, AT McDonald, PJ Pritchard, *Introduction to fluid mechanics*, 6th edition, ISBN9780471202318.

[8] FM White, *Fluid Mechanics*, 5th edition, ISBN9780072402179.

[9] LR Snyder, JJ Kirkland, JW Dolan, *Introduction to modern liquid chromatography*, 3rd edition, ISBN9780470167540.

[10] Z Xuejun, C Xiangwei, C Guojun, *Study on experimentation and simulation of micro-PVC in gravitational field-flow fractionation*, Proceedings of BMEI 2009.

[11] M Graff, AB Frazier, *Resonance light scattering (RLS) detection of nanoparticle separations in a microelectrical field-flow fractionation system*, IEEE Transactions on Nanotechnology, 2006, p.8-13.

[12] Wyatt Technology, http://www.wyatt.de/index.php?id=field_flow_fractionation

[13] Wyatt Technology, http://www.wyatt.de/index.php?id=eclipse

[14] Agilent 1290 Infinity LC System, http://www.chem.agilent.com/en-US/Pages/Homepage.aspx

[15] C Shen, HTM Pham, PM Sarro, *A multifunctional vertical microsieve for micro and nano particles separation*, Proceedings of MEMS 2009, p.383-386.

[16] VRSS Mokkapati, L Zhang, R Hanfoug, et al., *Fabrication and testing of a TMMF S2030 based micro fluidic device for single cell analysis*, ICQNM 2009, p.86-89.

[17] VRSS Mokkapati, MEMS Library, http://memslibrary.com/guest-articles/51-materials/66-dry-film-photoresist-for-microfluidics.html

[18] VRSS Mokkapati, *Micro and nanofluidic devices for single cell and DNA analysis*, ISBN9789090261133.

[19] B Li, M Liu, Q Chen, *Low-stress ultra-thick SU-8 UV photolithography process for MEMS*, Journal of Microlithography, Microfabrication and Microsystems, 2005.

[20] C Liu, Y liu, M Sokuler, et al., *Diffusion of water into SU-8 microcantilevers*, Physical Chemistry Chemical Physics, issue 35, 2010.

[21] C Shen, HTM Pham, PM Sarro, *Nano particle filtration module for lab-on-a-chip devices*, Proceedings of MEMS 2010, p.1067-1070.

[22] RJ Cornish, *Flow in a pipe of rectangular cross-section*, Proceedings of the Royal Society Society A, vol.120, no.786, 1928, p.691-700.

[23] G Gamrat, M Favre-Marinet, S Le Person, *An experimental study and modelling of roughness effects on laminar flow in microchannels*, Journal of Fluid Mechanics vol. 594, 2008, p.399-423.

[24] Y Mita, M Sugiyama, M Kubota, *Aspect ratio dependent scalloping attenuation in DRIE and an application to low-loss fiber-optical switches*, Proceedings of MEMS 2006, p.114-117.

[25] M Dijkstra, MJ de Boer, JW Berenschot, et al., *A versatile surface channel concept for microfluidic applications*, Journal of Micromechanics and Microengineering 17, 2007, p.1971-1977.

Appendix A: Detailed fabrication process flows

V1 process flow

Function	No	Process	Remarks
Layer stack	1	500nm PECVD SiO	Novellus
	2	500nm PECVD SiN	Novellus
	3	500nm PECVD SiO	Novellus
	4	500nm PECVD SiN	Novellus
	5	500nm PECVD SiO	Novellus
	6	500nm PECVD SiN	Novellus
	7	2µm PECVD SiO	Novellus, front DRIE mask
	8	Back 6µm PECVD SiO	Novellus, back DRIE mask
Zero-layer	9	PR coating	Co-SPR3012-zerolayer
	10	Exposure	Wafer-stepper, zefwan, 150 mJ/cm2
	11	PR development	Dev-Single Puddle
	12	Zero-layer etch	Drytek, STDSIN, 1m30s
	13	O_2 plasma stripper	Tepla, recipe 01, endpoint + 2m
In- and outlets	14	Back 3µm PR coating	Co-SPR3017M-3000nm
	15	Back exposure	Contact aligner, 2N, hard and vacuum contact, 20s
	16	PR development	Dev-Double Puddle 3
	17	Back 6µm SiO etch	Drytek, STDOXIDE, 12min
	18	O_2 plasma stripper	Tepla, recipe 01, endpoint + 2m
Channels	19	3µm PR coating	Co-SPR3017M-3000nm
	20	Exposure	Contact aligner, 3N, hard and vacuum contact, 10s
	21	PR development	Dev-Double Puddle 4
	22	Layer stack etch	Drytek, STDOXIDE, 12min
	23	O_2 plasma stripper	Tepla, recipe 01, endpoint + 2m
	24	30µm DRIE	Alcatel , Scribeline RF 20°C, 7m
	25	O_2 plasma stripper	Tepla, 2x recipe 04, 2x 15m
	26	Cleaning	
In- and outlets	27	200nm AL sputter	Sigma, 200nm@50°C with 1% Si
	28	Back through wafer DRIE	Alcatel, Mapper Speeder RF 20°C, 1hr10m
	29	O_2 plasma stripper	Tepla, 2x recipe 04, 2x 15m
	30	200nm Al etch	Al etch bench, 4m + HNA etch bench, 30s
Post-processing	31	Dicing	20x20mm
	32	Cleaning	
	33	SiO wet etch	BHF 1:7, 7m
	34	Cleaning	
	35	DFR lamination	Process 3 in Table 2.1
End of V1 proccess flow			

Addtional remarks for the V1 process flow:

- Requires 2N and 3N masks of P2750-V1 in box 303.

V2 process flow

Function	No	Steps	Remarks
Zero-layer	1	500nm LPCVD SiN	Furnace, prevents surface from thermal oxidation
	2	1µm PECVD SiO	Novellus, frontside DRIE mask
	3	PR Coating	Co-SPR3012-zerolayer
	4	Exposure	Wafer-stepper, zefwan, 150 mJ/cm2
	5	PR development	Dev-Single Puddle
	6	Zero-layer etch	Drytek, STDSIN, 1m30s
	7	O_2 plasma stripper	Tepla, recipe 01, endpoint + 2m
Trenches	8	2µm PR coating	Co-SPR3017M-2000nm
	9	Exposure	Contact aligner, 1N, hard and vacuum contact, 9s
	10	PR development	Dev-Double Puddle 2
	11	1µm SiO etch	Drytek, STDOXIDE, 2m30s
	12	500nm SiN etch	Drytek, STDSIN, 1m30s
	13	O_2 plasma stripper	Tepla, recipe 01, endpoint + 2m
Spacers	14	5µm DRIE	Alcatel, Scribeline RF 20°C, 1m30s
	15	O_2 plasma stripper	Tepla, 2x recipe 04, 2x 15m
	16	Cleaning	
	17	300nm LPCVD SiN	
	18	300nm SiN etch	Drytek, STDSIN, 1m
Molds	19	35µm DRIE	Alcatel, Scribeline RF 20°C, 10min
	20	O_2 plasma stripper	Tepla, 2x recipe 04, 2x 15m
	21	Residual SiO mask etch	BHF 1:7, 10min
	22	Cleaning	
	23	500nm thermal SiO	Furnace, pore definition
	24	1.5µm LPCVD SiN	Furnace
Channels	25	2µm PECVD SiO	Novellus, frontside DRIE mask
In- and outlets	26	Back 2.3µm SiN etch	Drytek, STDSIN 7m
	27	Cleaning	
	28	Back 6µm PECVD SiO	Novellus, backside DRIE mask
	29	Back 3µm PR coating	Co-SPR3017M-3000nm
	30	Back exposure	Contact aligner, 2N, hard and vacuum contact, 20s
	31	Back PR development	Dev-Double Puddle 3
	32	Back 6µm SiO etch	Drytek, STDOXIDE, 12min
	33	O_2 plasma stripper	Tepla, recipe 01, endpoint + 2m
Channels	34	3µm PR coating	Co-SPR3017M-3000nm
	35	Exposure	Contact aligner, 3N, hard and vacuum contact, 13s
	36	PR development	Dev-Double Puddle 3
	37	2µm SiO etch	Drytek, STDOXIDE, 4min
	38	2µm SiN etch	Drytek, STDSIN, 6min
	39	O_2 plasma stripper	Tepla, recipe 01, endpoint + 2m
	40	60µm DRIE	Alcatel, Scribeline RF 20°C, 20min
	41	O_2 plasma stripper	Tepla, 2x recipe 04, 2x 15m
	42	Cleaning	
V2 proccess flow continues on next page			

V2 proccess flow continued from last page			
In- and outlets	43	200nm AL sputter	Sigma, 200nm@50°C with 1% Si
	44	Back through wafer DRIE	Alcatel, Mapper Speeder RF 20°C, 1hr10m
	45	O_2 plasma stripper	Tepla, 2x recipe 04, 2x 15m
	46	200nm Al etch	Al etch bench, 4m + HNA etch bench, 30s
Post-processing	47	Dicing	20x20mm
	48	Cleaning	
	49	SiO wet etch	BHF 1:7, 50m
	50	Cleaning	
	51	DFR lamination	Process 3 in Table 2.1
End of V2 proccess flow			

Additional remarks for the V2 process flow:

- Requires 1N, 2N and 3N masks of P2750-V1 in box 303.

V3 process flow

Function	No	Steps	Remarks
Zero-layer	1	500nm LPCVD SiN	Furnace, prevents surface from thermal oxidation
	2	2µm PECVD SiO	Novellus, frontside DRIE mask
	3	PR coating	Co-SPR3012-zerolayer
	4	Exposure	Wafer-stepper, zefwan, 150 mJ/cm2
	5	PR development	Dev-Single Puddle
	6	Zero-layer etch	Drytek, STDSIN, 1m30s
	7	O_2 plasma stripper	Tepla, recipe 01, endpoint + 2m
Molds	8	2µm PR coating	Co-SPR3017M-2000nm
	9	Exposure	Contact aligner, 1N, hard and vacuum contact, 9s
	10	PR development	Dev-Double Puddle 2
	11	2µm SiO etch	Drytek, STDOXIDE, 5m
	12	500nm SiN etch	Drytek, STDSIN, 1m30s
	13	O_2 plasma stripper	Tepla, recipe 01, endpoint + 2m
	14	90µm DRIE	Alcatel, Scribeline RF 20°C, 50m
	15	O_2 plasma stripper	Tepla, 2x recipe 04, 2x 15m
	16	Residual SiO mask etch	BHF 1:7, 10min
	17	Cleaning	
	18	500nm thermal SiO	Furnace, pore definition
	19	1µm LPCVD SiN	Furnace
Channels	20	2µm PECVD SiO2	Novellus, frontside DRIE mask
In- and outlets	21	Back 1.5µm SiN etch	Drytek, STDSIN 5min
	22	Cleaning	
	23	Back 6µm PECVD SiO	Novellus, backside DRIE mask
	24	Back 3µm PR coating	Co-SPR3017M-3000nm
	25	Back exposure	Contact aligner, 2N, hard and vacuum contact, 20s
	26	Back PR development	Dev-Double Puddle 3
	27	Back 6µm SiO etch	Drytek Triode 384T, STDOXIDE 12min
	28	O_2 plasma stripper	Tepla, recipe 01, endpoint + 2m
Channels	29	3µm PR coating	Co-XI-SPR3017M-3000nm
	30	Exposure	Contact aligner, 3N, hard and vacuum contact, 13s
	31	PR development	DEV-Double Puddle 3
	32	2µm SiO2 plasma etch	Drytek Triode, STDOXIDE 4m
	33	1.5µm SiN etch	Drytek, STDSIN, 5min
	34	O_2 plasma stripper	Tepla, recipe 01, endpoint + 2m
	35	80µm DRIE	Alcatel, Scribeline RF 20°C, 20m
	36	O_2 plasma stripper	Tepla, 2x recipe 04, 2x 15m
	37	Cleaning	
	38	Si isotropic etch	Alcatel, see additonal remarks, 5m
	39	Cleaning	
In- and outlets	40	200nm AL sputter	Sigma, 200nm@50°C with 1% Si
	41	Back through wafer DRIE	Alcatel, Mapper Speeder RF 20°C, 1hr20m
	42	O_2 plasma stripper	Tepla, 2x recipe 04, 2x 15m
	43	200nm Al etch	Al etch bench, 4m + HNA etch bench, 30s
	44	200nm AL sputter	Sigma, 200nm@50°C with 1% Si
V3 proccess flow continues on next page			

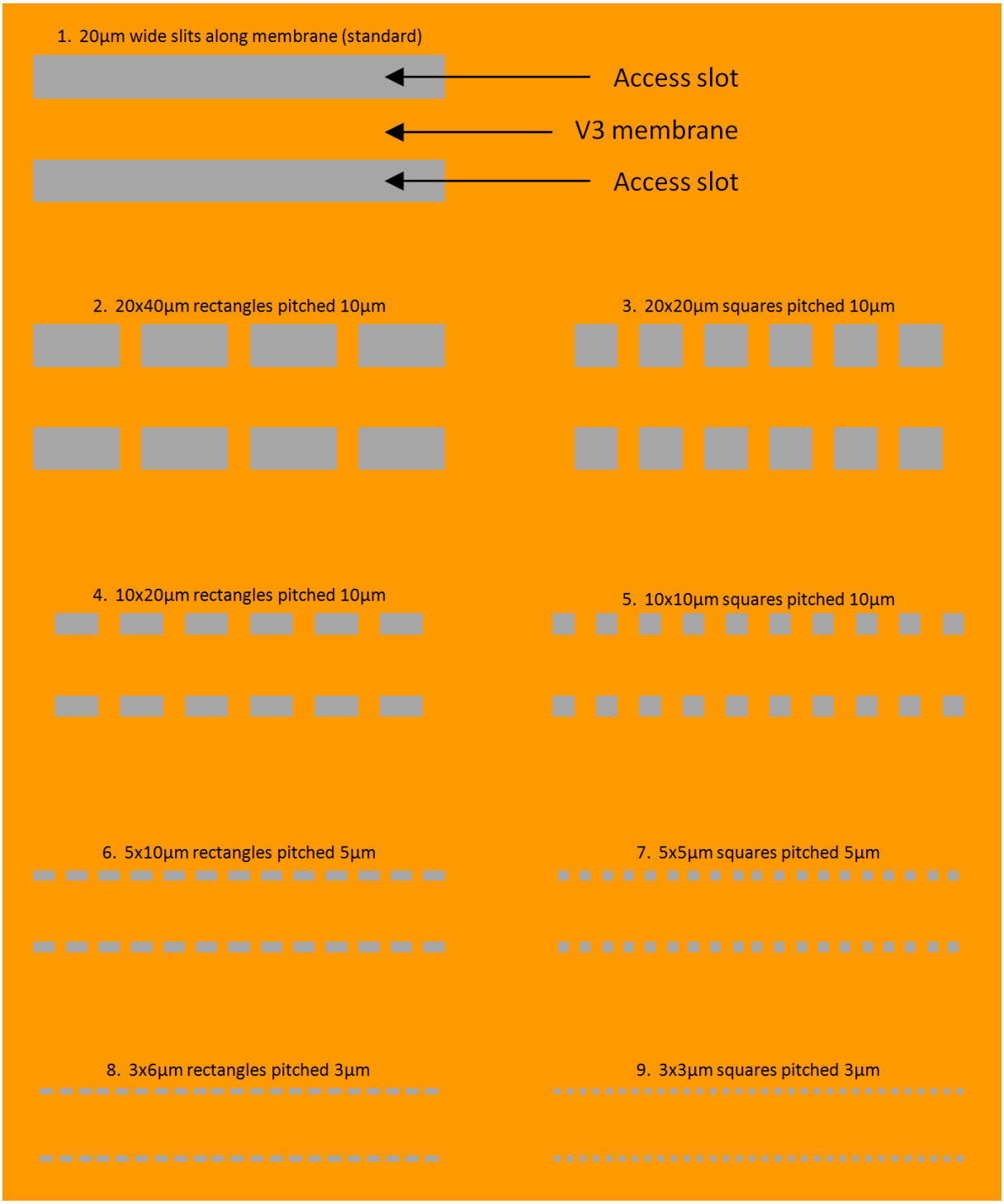
V3 proccess flow continued from last page			
Post-Processing	45	Dicing	20x20mm
	46	Cleaning	
	47	SiO wet etch	BHF 1:7, 1hr
	48	Cleaning	
	49	DFR lamination	Process 3 in Table 2.1
End of V3 proccess flow			

Addtional remarks for the V3 process flow:

- Requires 1N and 3N masks of P3056-V2 in box 303 and 2N mask of P3056-V1 in box 354.
- Step 38, Si isotropic etch, is performed by a custom Alcatel etch process. The non-zero parameters of this etch are: 400 sccm SF_6, 1500 Watt source generator, 20 Watt substrate holder (SH).

Appendix B: V3 access slot configurations

The V3 design was developed with a number of access slot configurations. The basic configurations are depicted in the figure below. Note that wider microchannels were also created by putting multiple rows of access slots, pitched 12µm, in parallel (not shown in figure).



Appendix C: Proceeding for Eurosensors 2011

Note that the presented format in this Appendix might differ from the actual publication due to a template conversion. However, content wise it is identical.

Proc. Eurosensors XXV, September 4-7, 2011, Athens, Greece

A Buried Vertical Filter for Micro and Nanoparticle Filtration

S.J. Li*, C. Shen, P.M. Sarro

DIMES-ECTM, Delft University of Technology, Feldmannweg 17, 2628 CT Delft, the Netherlands

Abstract

This paper presents a silicon micromachined filter for micro- and nanoparticles. The filter is vertical and completely buried beneath the surface. The buried aspect allows additional features to be integrated above the filter, while the vertical aspect allows the creation of highly uniform pores and efficient use of die area. The filter is composed out of a porous membrane released together with the microchannels by isotropically etching the surrounding silicon. Fluidic experiments have confirmed the filtration functionality of fabricated devices using operating pressures up to 400kPa. Moreover, by using a reversed fluid flow, cleansing of the cake layer build-up on the porous membrane is attained.

Keywords: Silicon micromachining; particle filter; porous membrane; vertical; buried.

1. Introduction

Size-based particle separation, or simply “filters”, is a well-known research topic in micro-fluidics. Several solutions have been developed for integrating filters on-chip. For example, porous membranes for high throughput filtration have been micromachined by patterning and etching pores onto a substrate [1]. Filters can also be adapted in polymer cantilevers to enable on-chip collection and off-chip sensing of micro-particles [2]. Size-based sorting of particles can be achieved by driving a micro-filter with time-sequential flows [3]. However, micromachined filters often consume a significant amount of area which limits the option of integrating additional features on the same die. Furthermore, accuracy is limited for the separation of sub-micron particles, because it is rather challenging to uniformly micromachine pores of such small dimensions. Recently, we have presented two types of vertical membrane filters that address these shortcomings [4, 5]. In this paper we present a new design which further builds on our concept of vertical filters, addressing the issues of area consumption and pore size uniformity.

*S.J. Li, tel.: +31-15-278-6234; fax: +31-15-278-7369; e-mail address: s.j.li@student.tudelft.nl

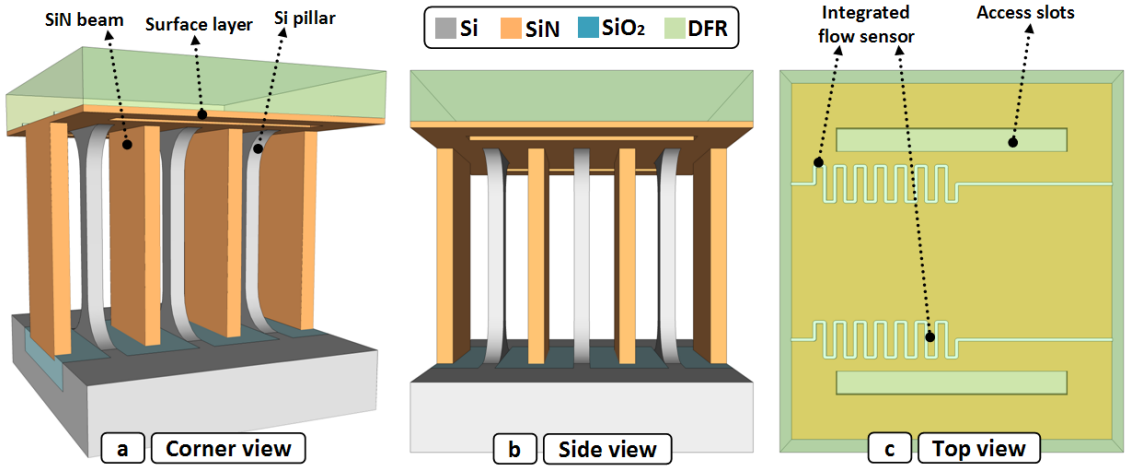


Fig. 1. Conceptual CAD drawing of the buried vertical filter: (a) Corner view showing the silicon pillars, nitride beams and nitride surface layer. (b) Side view showing the slit-shaped pores. (c) Top view showing an integrated flow sensor on top of the filter and access slots sealed by dry film resist.

2. Design Concept

A novel design of a silicon micromachined filter is presented here (Fig. 1). The filter function is implemented by a vertical porous membrane with microchannels alongside. The porous membrane itself is an interdigitated structure composed out of silicon (Si) pillars and silicon nitride (SiN) beams. These pillars and beams are accurately spaced by slit-shaped pores. The filter is completely buried below a flat SiN surface layer on which additional features, such as actuation or sensing elements, can be integrated. The nitride layer is perforated with access slots for the release of the underlying porous membrane during fabrication. These access slots are sealed by dry film resist (DFR).

Thermal oxidation creates highly uniform, conformal and tunable oxide layers. These properties are quite advantageous for the filter design as its pores are pre-defined by layers of thermally oxidized silicon dioxide (SiO_2). Pores released from thermal SiO_2 are uniform and can be purposely varied from tens of nanometers to 1-2 micrometers by simply altering the oxidation parameters. This allows for both a steep and variable particle cut-off diameter without the necessity of a customized photolithography process.

The filter is vertical and the work plane of the porous membrane is perpendicular to the surface. This minimizes the footprint even when the work plane is enlarged into the substrate to accommodate a higher throughput. Moreover, instead of having to face an unusable surface, the buried aspect of the design allows for the integration of subsystems and additional features above the vertical filter, like actuators to extend the device interaction capabilities or sensors for in-situ detection of filtration fluid parameters.

Fabrication process

The filter is fabricated on a 4 inch <100> single crystalline Si wafer. Two layers, 500nm low stress SiN and 2µm SiO_2, are deposited by means of low pressure and plasma enhanced chemical vapor deposition (LPCVD, PECVD), respectively. The nitride layer prevents the surface from oxidizing and the oxide layer acts as a hard mask against the upcoming deep reactive ion etch (DRIE) process. (Fig. 2a)

A row of 3µm by 20µm rectangles are patterned in the aforementioned layers and 100µm deep molds are made by etching these patterns with a Bosch-based DRIE process. The wafer is thermally oxidized to grow SiO_2 inside the molds for defining the slit-shaped pores. The oxide thickness is chosen according to the desired pore size. LPCVD is then used to cast SiN in the molds which finalize the nitride beams. Additional features can be integrated after the casting process as the surface is highly planar and will remain essentially intact. (Fig. 2b-d)

Access slots are patterned in a 2µm PECVD SiO_2 mask and etched 80µm into the substrate using DRIE. SF_6 plasma is then used to penetrate the surface through the access slots and etch the underlying Si. This isotropic etch creates the microchannels, releases the membrane and allows physical access to the thermal SiO_2 layers. Subsequently, the SiO_2 layers are removed by buffered hydrofluoric acid (BHF) for the release of the slit-shaped pores. A device that has gone through all these process steps (Fig. 2e-g) is shown in Fig. 3.

The operating pressure of the filter is greatly dependent on the quality of the seal. Sealing the access slots with simply dry film resist only allows an operating pressure up to 50kPa. This value can be significantly improved by sticking a glass wafer on top of the DFR seal while using SU-8 as adhesive. With this improved sealing method, operating pressures up to 400kPa can be sustained for long periods (>1hr) without signs of damage to the seal or the filter. (Fig. 2h)

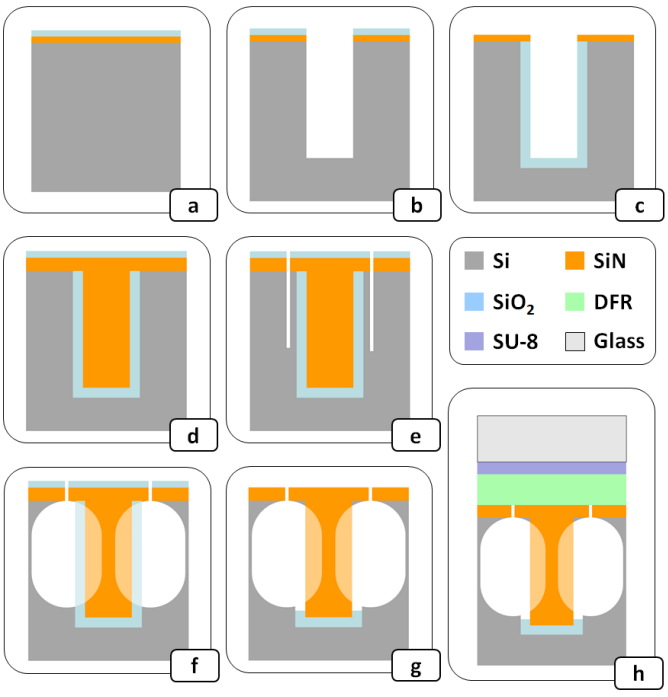


Fig. 2. Schematic view of the fabrication process of the buried vertical filter: (a-d) Definition of slit-shaped pores and SiN beams. (e-g) Release of membrane, microchannels and pores. (h) Sealing of the filter.

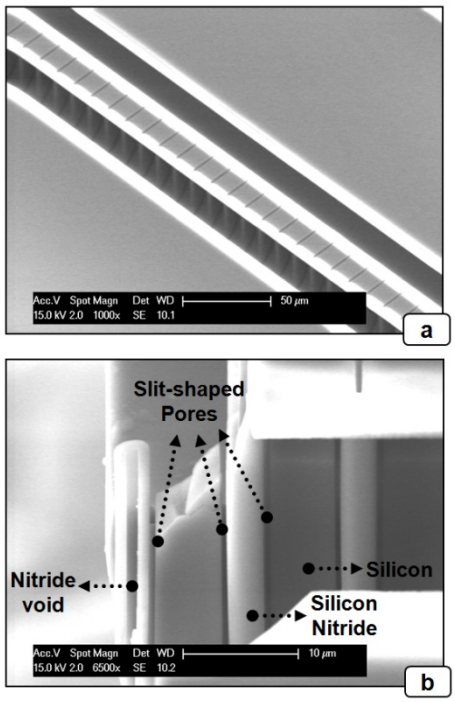


Fig. 3. SEM images of a 500nm pore sized filter: (a) Top view of the buried filter. (b) Close-up view of 500nm slit-shaped pores.

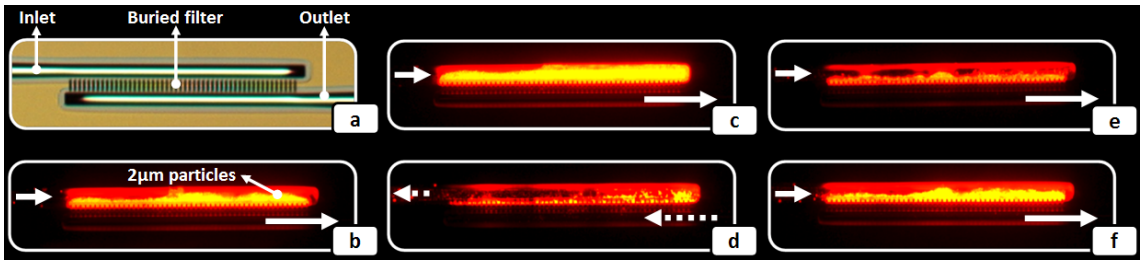


Fig. 4. Fluidic experiment with 2µm fluorescence polystyrene beads. The fluid flow directions are indicated by arrows. (a) Normal microscope view. (b/c) Fluorescence microscope views at incrementing times showing the 1st cycle of filtration. (d) Fluid flow is reversed to clean the membrane. (e/f) Fluorescence microscope views at incrementing times showing the 2nd cycle of filtration.

3. Experiment results

Fluidic experiments were carried out to validate the functionality and performance of the buried vertical filter. For easier access to the inlet and outlet (Fig. 4a), the devices under test were mounted in a custom-made holder with polymer tubing. Fluids were supplied by a syringe pump via the tubing to the device's microchannels. In addition, a gauge was present in the experimental setup for pressure measurements.

Preliminary tests using demineralized water and a single 360µm long porous membrane with 500nm pores showed a volumetric flow rate of 1µl/min at 275kPa. A backflow experiment was conducted using 2µm polystyrene beads and observed through a fluorescence microscope. This experiment confirmed the filter function and demonstrated the ability to self-clean. (Fig. 4b-f)

Acknowledgements

We would like to thank the DIMES clean room staff for their help with the device fabrication and the Electronic Instrumentation Laboratory for providing the equipment for the fluidic tests. This work is funded by MicroNed (SMACT 2-D).

References

[1] Kuiper S, de Boer M, van Rijn CJM, Nijdam W, Krijnen GJM and Elwenspoek MC, *Wet and dry etching techniques for the release of sub-micron perforated membranes*, J. Micromech. and Microeng. 10; 2000, p. 171–174.

[2] Noeth N, Keller S, Fetz S, Geschke O, Boisen A, *Micro-Particle Filter made in SU-8 For Biomedical Applications*, Proc. Transducers 2009; 2009, p. 2034–2037.

[3] Tan X, Yoon HJ, Granneman J, Moore HP, Cheng MMC, *A High-Throughput Microfluidic Chip for Size Sorting of Cells*, Proc. MEMS 2011; 2011, p. 1075–1078.

[4] Shen C, Pham HTM, Sarro PM, *A Multifunctional Vertical Microsieve for Micro and Nano Particles Separation*, Proc. MEMS 2009; 2009, p. 383–386.

[5] Shen C, Pham HTM, Sarro PM, *Nano Particle Filtration Module for Lab-on-a-Chip Devices*, Proc. MEMS 2010; 2010, p. 1067–1070.

Acknowledgements

The first name I would like to mention here is Chenggang Shen. When I started this graduation project, Chenggang was assigned to supervise me. And that he certainly did well with his friendly attitude, patient teaching and daily availability. Besides helping me progress through my work, Chenggang has aided in developing my perspective on academia, device fabrication and research.

Before starting my Master study, I did not think much about my capacity for scientific writing. And unfortunately, this ended up as an unexpected challenge. However luckily, I could count on my professor Lina Sarro who has helped me a great deal in putting words on paper (and effectively also getting work done).

I met Robin van Eijk back when I was doing my Bachelor study at the polytechnic institute of Rijswijk. A friendship out of common interest came to existence when we both decided to continue our studies at Delft University of Technology. This friendship is now greatly cherished because it has evolved substantially from our common academic struggles against the lack of knowledge, motivation and time in the past 3 years.

In the past year, I have probably spent most of my time awake at the University. And I have to admit that I have had difficult times with staying constantly concentrated on my work. Fortunately for those times, I could always count on my office buddies, Ankur Sharma and Tomasso Rossi, for some re-energizing talks and discussions.

Last but not least, I would like to mention some people and organizations that have greatly helped and provided for me during this thesis work.

People: Bianca Knot, Charles de Boer, Jeroen Bastemijer, Marian Roozenburg, Mario Laros, Sharma Mokkapati, Silvana Milosavljevic, Thomas Moh, Wim van Oel and Wim van der Vlist.

Organizations: Delft University of Technology, Delft Institute of Microsystems and Nanoelectronics and MicroNed.

To all whom are mentioned above, and to all whom are not, but should have been: Thank you.

Sheng J. Li,
24 Aug 2011