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A Variable Switching Frequency Front-End Converter for EV Chargers
Enhancing Efficiency and Minimizing Harmonics

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A VARIABLE SWITCHING FREQUENCY FRONT-END CONVERTER FOR EV CHARGERS

ENHANCING EFFICIENCY AND MINIMIZING HARMONICS

A VARIABLE SWITCHING FREQUENCY FRONT-END CONVERTER FOR EV CHARGERS

ENHANCING EFFICIENCY AND MINIMIZING HARMONICS

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology
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chair of the Board for Doctorates
to be defended publicly on
Thursday 10th of October 2024 at 10:00 o'clock

by

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To mom and dad.

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SUMMARY

E-mobility stands as a pivotal part of the roadmap toward a sustainable society, with electric vehicle (EV) charging techniques playing a crucial role in this era of transportation electrification. The integration of numerous EV chargers catering to diverse EVs presents significant challenges, not only in power electronics design but also in interfacing with the power grid.

Over the past decades, various variable switching frequency methods have been explored to design highly efficient, lightweight, and cost-effective power electronics converters. These methods aim to strike a balance between efficiency and the size of magnetic components. Additionally, the proliferation of supra-harmonics in EV charging stations connected to the grid has been increasingly observed and reported. Lastly, ensuring control stability of the grid-tied power-factor-correction (PFC) converter is vital for the operation of both the grid and EV charger.

To tackle the challenges outlined above, this thesis investigates the front-end power-factor-correction (PFC) converter for EV chargers, employing variable switching frequency techniques to enhance efficiency and minimize harmonics. The research topics focus on design of front-end AC-DC PFC converter, variable switching frequency for soft-switching, supra-harmonics modeling under variable switching frequency, and control of the grid-tied PFC converter.

DESIGN OF FRONT-END AC-DC PFC CONVERTER

The front-end power-factor-correction (PFC) converter plays a crucial role in regulating the DC link for the back-end DC-DC stage and transferring power from the grid to the EV battery. This thesis delves into the detailed design of the AC-DC PFC converter, utilizing multi-objective optimization (MOO) techniques. The design process aims to strike an optimal balance between efficiency, power density, and cost by leveraging available core databases in the market. Through experimental validation, the final prototype achieves a power efficiency of 98.6% with IGBT only, demonstrating a well-balanced design approach that considers various trade-offs.

VARIABLE SWITCHING FREQUENCY FOR SOFT-SWITCHING

Variable switching frequency offers a direct and convenient method for shaping the inductor current ripple during operation. While soft-switching can be achieved through triangular-current-mode (TCM) control with variable switching frequency, it leads to significantly larger current ripple, which compromises conduction and inductor losses and complicates the design process. In this thesis, an integrated triangular current mode (i-TCM) control approach is introduced to enhance power density and specific power, allowing for higher switching frequencies to reduce LCL filter size without sacrificing efficiency. By incorporating an additional LC branch, high and low-frequency currents

are separated to minimize inductor losses and optimize the design. The research findings demonstrate the feasibility of the proposed i-TCM and STCM control methods in achieving high power efficiency and alleviating large current stress in the boost inductor.

SUPRA-HARMONICS MODELING UNDER VARIABLE SWITCHING FREQUENCY

Various variable switching frequency methods have been implemented in AC-DC PWM converters to address different objectives, such as achieving soft-switching, minimizing ripple and inductor losses, reducing electromagnetic interference (EMI), and optimizing power efficiency. However, the widespread adoption of variable switching frequency pulse-width modulation (VSFPWM) techniques has led to an increase in switching harmonics clustering in the supra-harmonics range, particularly in EV charging stations. The presence of overlapped harmonic spectra from different switching harmonic bands can amplify harmonic magnitudes due to the wide frequency variation, necessitating additional filtering measures. In this thesis, a fast-acquisition supra-harmonics model under arbitrary Periodic VSFPWM (P-VSFPWM) is proposed based on vectorization, which facilitates the subsequent filter design process. Additionally, interleaved P-VSFPWM is adopted to mitigate harmonics overlap without deviating from the intended purpose of P-VSFPWM. The optimal profiles that minimize required inductance while meeting IEEE-519 standards have been identified through spectral analysis. The research findings validate the correctness and effectiveness of the proposed supra-harmonics model. Furthermore, it has been demonstrated that employing P-VSFPWM methods enhances AC filter power density compared to conventional constant switching frequency continuous PWM strategies.

CONTROL OF THE GRID-TIED PFC CONVERTER

LCL filters play a crucial role in attenuating high-frequency harmonics generated by PFC converters, thereby minimizing current harmonics injected into the grid. However, ensuring system stability is vital, and active damping methods are preferred over passive damping circuits due to lower power losses. This thesis explores the capacitor-current active damping (CCAD) technique, which aims to determine the optimal feedback gain for stability. Additionally, it adopts harmonics compensation for grid voltage distortion by proposing an improved resonator with phase compensation to suppress harmonics while maintaining stability. The effectiveness of the proposed control scheme has been validated through simulation and experimental results.

SAMENVATTING

E-mobiliteit vormt een essentieel onderdeel van de routekaart naar een duurzame samenleving, waarbij oplaadtechnieken voor elektrische voertuigen (EV's) een cruciale rol spelen in dit tijdperk van elektrificatie van transport. De integratie van talrijke oplaadstations voor EV's, die verschillende soorten voertuigen bedienen, brengt aanzienlijke uitdagingen met zich mee, niet alleen op het gebied van vermogenselektronica-ontwerp maar ook bij de koppeling met het elektriciteitsnet.

De afgelopen decennia zijn verschillende methoden voor variabele schakelfrequentie onderzocht om zeer efficiënte, lichte en kosteneffectieve vermogenselektronica converters te ontwerpen. Deze methoden streven naar een balans tussen efficiëntie en de omvang van magnetische componenten. Daarnaast is de toenemende aanwezigheid van supra-harmonischen in EV-laadstations die zijn aangesloten op het elektriciteitsnet steeds vaker geobserveerd en gerapporteerd. Tot slot is het waarborgen van de stabiliteit van de regeling van de netgekoppelde vermogensfactorcorrectie (PFC) converter cruciaal voor de werking van zowel het net als de EV-lader.

Om de bovenstaande uitdagingen aan te pakken, onderzoekt dit proefschrift de vermogensfactorcorrectie (PFC) converter aan de voorzijde van EV-laders, waarbij variabele schakelfrequentietechnieken worden toegepast om de efficiëntie te verbeteren en harmonischen te minimaliseren. De onderzoeksgebieden richten zich op het ontwerp van de front-end AC-DC PFC converter, variabele schakelfrequentie voor zachte schakeling, modellering van supra-harmonischen onder variabele schakelfrequentie, en regeling van de netgekoppelde PFC converter.

ONTWERP VAN DE AC-DC PFC CONVERTER AAN DE VOORZIJDE

De front-end power-factor-correction (PFC) converter speelt een cruciale rol bij het reguleren van de DC-link voor het achterste DC-DC-stadium en het overbrengen van vermogen van het net naar de EV-batterij. Deze scriptie richt zich op het gedetailleerde ontwerp van de AC-DC PFC-converter, waarbij gebruik wordt gemaakt van multi-objective optimalisatietechnieken (MOO). Het ontwerpproces streeft naar een optimale balans tussen efficiëntie, vermogensdichtheid en kosten door gebruik te maken van beschikbare kern databases in de markt. Door experimentele validatie bereikt het uiteindelijke prototype een vermogensefficiëntie van 98,6% met alleen IGBT's, wat een goed uitgebalanceerde ontwerpaanpak aantoont die verschillende afwegingen in overweging neemt. uitgebalanceerde ontwerpaanpak aantoont die verschillende afwegingen in overweging neemt.

VARIABELE SCHAKELFREQUENTIE VOOR ZACHTE SCHAKELING

Variabele schakelfrequentie biedt een directe en handige methode om de inductorstroomrimpel tijdens bedrijf te vormen. Hoewel zachte schakeling kan worden bereikt via de driehoeksstroommodus (TCM) controle met variabele schakelfrequentie, leidt dit tot aanzienlijk grotere stroomrimpel, wat de geleidings- en inductorverliezen compromitteert en het ontwerpproces compliceert. In deze thesis wordt een geïntegreerde TCM (i-TCM) controle-aanpak geïntroduceerd om de vermogensdichtheid en specifiek vermogen te verbeteren, waardoor hogere schakelfrequenties mogelijk zijn om de LCL-filtergrootte te verkleinen zonder de efficiëntie op te offeren. Door een extra LC-tak op te nemen, worden hoge- en lage-frequentiestromen gescheiden om inductorverliezen te minimaliseren en het ontwerp te optimaliseren. De onderzoeksresultaten tonen de haalbaarheid van de voorgestelde i-TCM en STCM controlemethoden aan door het bereiken van een hoge vermogensefficiëntie en het verminderen van de grote stroomstress in de boost-inductor.

SUPRA-HARMONISCHEN MODELLERING ONDER VARIABELE SCHAKELFREQUENTIE

Verschillende methoden van variabele schakelfrequentie zijn geïmplementeerd in AC-DC PWM-converters om verschillende doelstellingen aan te pakken, zoals het bereiken van zachte schakeling, het minimaliseren van rimpel en inductorverliezen, het verminderen van elektromagnetische interferentie (EMI) en het optimaliseren van de energie-efficiëntie. De algemeen verspreide aanneming van variabele schakelfrequentie pulsbreedte modulatie (VSFPWM) technieken heeft echter geleid tot een toename van schakelharmonischen die zich ophopen in het supra-harmonische bereik, met name in EV-laadstations. De aanwezigheid van overlappende harmonische spectra van verschillende schakelharmonische banden kan de harmonische magnitudes versterken door de brede frequentievariatie, wat extra filtermaatregelen noodzakelijk maakt. In deze scriptie wordt een snel-verwervend supra-harmonisch model onder willekeurige periodieke VSFPWM (P-VSFPWM) voorgesteld op basis van vectorisatie, wat het daaropvolgende filterontwerpproces vergemakkelijkt. Bovendien wordt onderling verbonden P-VSFPWM toegepast om harmonische overlapping te verminderen zonder af te wijken van het beoogde doel van P-VSFPWM. De optimale profielen die de benodigde inductantie minimaliseren terwijl ze voldoen aan de IEEE-519 normen, zijn geïdentificeerd door spectrale analyse. De onderzoeksresultaten bevestigen de juistheid en effectiviteit van het voorgestelde supra-harmonische model. Verder is aangetoond dat het gebruik van P-VSFPWM-methoden de vermogensdichtheid van AC-filters verbetert in vergelijking met conventionele constant-schakelfrequentie continue PWM-strategieën.

BEHEERSING VAN DE AAN HET NET GEKOPPELDE PFC-CONVERTER

LCL-filters zijn uiterst effectief in het dempen van hoogfrequente harmonischen die door PFC-converters worden gegenereerd, waardoor de injectie van stroomharmonischen in het net wordt geminimaliseerd. Het waarborgen van de systeemstabiliteit is echter cruciaal en actieve dempingsmethoden worden verkozen boven passieve dempingscircuits vanwege de lagere vermogensverliezen. In deze scriptie wordt de techniek van actieve demping via condensatorstroom (CCAD) onderzocht, met als doel de optimale terugkoppelingsversterking voor stabiliteit te identificeren. Daarnaast wordt de compensatie van harmonischen voor netwerkspanningsvervorming aangepakt door het voorstellen van een verbeterde resonator met fasecompensatie om harmonischen te onderdrukken terwijl de stabiliteit behouden blijft. Het voorgestelde regelschema is gevalideerd door middel van simulatie- en experimentele resultaten.

1

INTRODUCTION

1.1. BACKGROUND

Electric mobility plays a crucial role in addressing two significant challenges: energy scarcity resulting from fossil fuel depletion and greenhouse gas (GHG) emissions. By transitioning to Electric Vehicles (EVs), we can mitigate these risks and pave the way for a sustainable future. The rapid development of EVs is essential for advancing electric mobility, and it has led to a substantial growth in the global EV market. This growth can be attributed to various factors, including policy incentives aimed at promoting sustainable transportation and continuous advancements in battery technology. As depicted in Fig. 1.1, there has been a remarkable increase in the global EV stock, indicating a significant shift towards electric mobility on a global scale. One notable trend in the electric vehicle (EV) market is the continuous increase in battery capacity among new EV models. Data from [23] indicates that the average battery capacity of battery electric

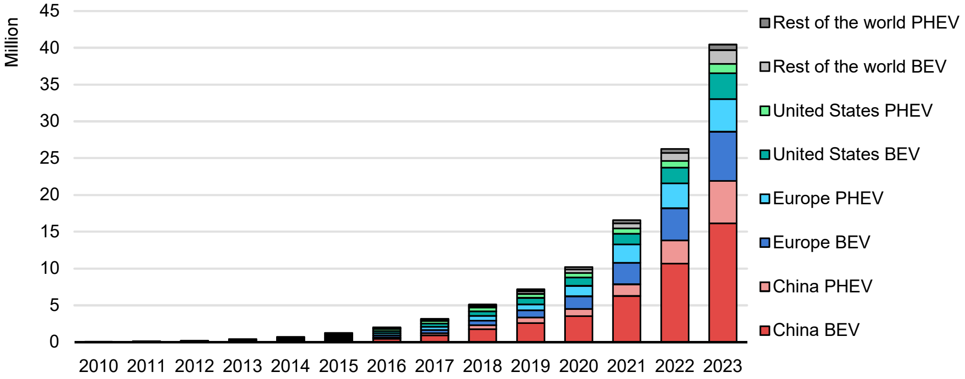


Figure 1.1: Global electric car stock trends, 2010-2023 [1]. Notes: BEV = battery electric vehicle; PHEV = plug-in hybrid vehicle. Includes passenger cars only.

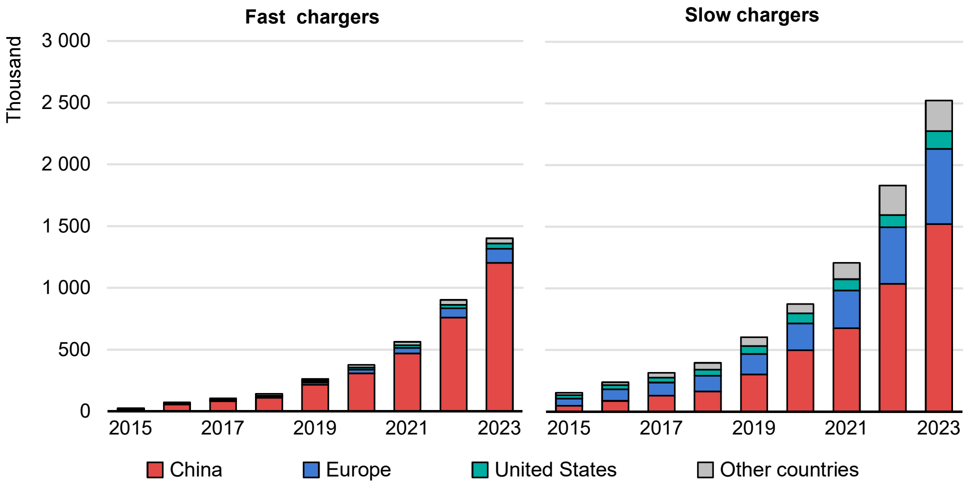


Figure 1.2: Installed publicly accessible light-duty vehicle charging points by power rating and region, 2015-2023 [1]. Note: Values shown represent number of charging points.

vehicle (BEV) models has reached 72.1 kWh, based on currently available and upcoming models. This upward trend in battery capacity can be attributed to two primary factors. Firstly, there is a growing availability of all-electric car models (BEVs) with extended driving ranges, driven by consumer demand for vehicles that offer longer distances per charge. Secondly, there is a rising preference for BEVs over plug-in hybrid electric vehicles (PHEVs), as illustrated in Fig. 1.1, further contributing to the increase in average battery capacity across the EV market. Another trend in the EV market is the gradual increase in the number of publicly accessible chargers, as depicted in Fig. 1.2. While private slow AC-type chargers continue to play a dominant role, there has been a notable rise in the availability of public charging infrastructure. However, as the trend of increasing EV battery capacity continues, there will be a growing need for more publicly accessible fast chargers, as highlighted by a report from the International Renewable Energy Agency (IRENA) [24]. DC fast chargers, known for their high power output, are emerging as an effective solution for alleviating range anxiety among EV drivers. DC fast charging stations are anticipated to be connected to the medium voltage (MV) grid, as illustrated in Fig. 1.3. This connection offers mutual benefits to both the grid and the fast charging stations. By linking to the robust medium voltage distribution grid, these charging stations help alleviate the load on vulnerable low voltage grids and significantly reduce the burden on energy distribution companies. Moreover, charging stations equipped with multiple fast chargers can efficiently serve hundreds of cars per day with just one grid connection to the MV grid network, thereby enhancing the effectiveness of EV charging. Furthermore, integrating renewable energy sources such as solar panels and battery energy storage systems (BESSs) with DC fast charging stations can offer economic and technical advantages. These integrated systems can provide ancillary services and grid support to the MV grid, contributing to its stability and reliability.

In today's EV market, there's a rising demand for affordable, rapid, and easily ac-

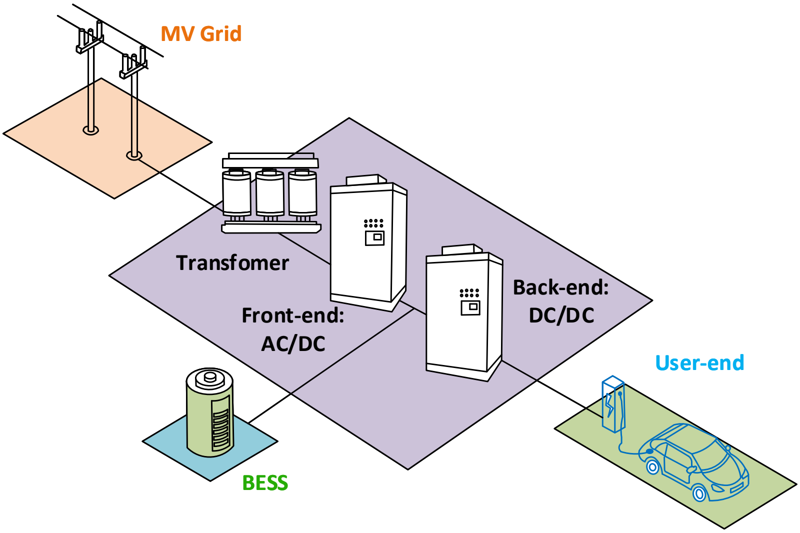
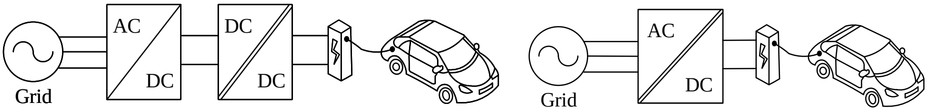


Figure 1.3: Schematic Diagram: A DC fast charging station connected to the MV grid

cessible EV chargers, encompassing both on-board AC chargers and DC fast charging solutions. Lightweight and cost-efficient on-board AC chargers are pivotal for advancing E-mobility, providing EV owners with convenient charging options. Meanwhile, DC fast charging stations, expected to link to the medium voltage grid, offer the benefit of shorter charging times but entail higher costs and larger space requirements compared to slow chargers. Despite these challenges, DC fast charging stations play a crucial role in alleviating range anxiety and enhancing the efficiency of EV charging infrastructure.

The EV chargers, including both on-board AC chargers and DC fast chargers, can be categorized into single-stage and two-stage chargers based on their power conversion architecture. In a single-stage charger, depicted in Fig. 1.4(a), power is directly converted from the grid to the EV battery using only one power conversion stage via an isolated AC-DC converter. On the other hand, the two-stage charger shown in Fig. 1.4(b) consists of a front-end AC-DC converter connected to the grid and a back-end isolated DC-DC converter responsible for delivering power to the EV battery. An intermediate DC link, regulated by the front-end converter, ensures a stable input DC voltage for the DC-DC converter.

In the two-stage EV charger configuration, the front-end AC-DC converter serves as the fundamental power factor correction (PFC) converter connected to the grid. Simultaneously, it ensures stable power delivery to the EV loads or integrated battery energy storage systems through the regulated DC link. For on-board chargers (OBCs) in both conventional grid-to-vehicle (G2V) and vehicle-to-grid (V2G) charging scenarios, the demand for an efficient, compact, and lightweight AC-DC PFC converter is paramount. Despite the moderate efficiency under specific power levels, commercially available OBCs suffer from limited power density. In contrast to on-board chargers, where volume and



(a) Two-stage charger (b) Single-stage charger

Figure 1.4: Diagram of a typical two-stage EV charger with a three-phase AC/DC PFC rectifier as the front-end and an isolated DC/DC converter.

weight are secondary considerations in power electronics design, the primary focus of DC fast charger lies on achieving cost-effective solutions. To avoid the utilization of conventional MV transformers, a modular design architecture employing Power Electronics Building Blocks (PEBBs) has been suggested for the DC fast charger, similar to the design principles of a Solid-State Transformer (SST) [25, 26]. Unlike the parallel power modules in transformer-based DC fast chargers, the modular approach manages high-power charging by serially connecting PEBBs, enabling the utilization of power devices rated for lower voltage and current levels. However, this setup results in increased operational complexity and reduced reliability compared to transformer-based solutions.

Variable switching frequency techniques have become prevalent in various Power Factor Correction (PFC) converter applications, aimed at enhancing efficiency and reducing passive component requirements [2–21]. Through optimized converter designs and advanced modulation techniques, efficiency and power density are significantly elevated, leading to lower costs for energy sustainability. However, there's a growing emphasis on supra-harmonics (frequency range: 2 to 150 kHz) owing to the increased integration of power electronic-based systems such as EV chargers and PV inverters. EV chargers, particularly the PFC converters within them, can introduce supra-harmonic distortions by employing switching frequencies within the supra-harmonics range for cost and efficiency considerations. This practice is especially common in OBCs for electric vehicles, where compactness and lightweight designs are paramount. The power electronics design of front-end PFC converters must address this consideration, as supra-harmonics can have adverse effects on the connected grid [27–30]. Therefore, technological advancements are essential to support e-mobility by making electric vehicle charging more efficient and reliable, contributing to energy sustainability and reducing the environmental impact of transportation.

1.2. THESIS OBJECTIVE AND RESEARCH QUESTIONS

The main objective of this thesis is as follows.

" To research and establish techniques and guidelines for variable switching frequency modulation to enhance the efficiency and power density of front-end converters while mitigating the emission of supra-harmonics to the grid connected to EV chargers."

The main research is subdivided into several research questions with individual objectives, outlined as follows:

Q1 *What are the advantageous PFC converter solutions to the two-stage EV chargers?*

- Conduct the literature study of the existing power electronics topologies for the PFC converters.
- Propose several candidates and conduct further analytical modeling, simulation, and design.
- Apply the multi-objective design procedures for the optimal converter design results.
- Construct and test the prototypes to verify the design.

Q2 *How to improve the efficiency and power density of the front-end AC-DC PFC converter with the approach of variable switching frequency?*

- Review the reported triangular-current-mode (TCM) soft-switching techniques based on variable switching frequency and evaluate their potential in reducing the converter size.
- Study the principle of the integrated-TCM (iTCM) approach and evaluate their pros and cons.
- Model and analyze the different switching frequency profiles in the three-phase iTCM converter system.
- Evaluate the performance of the three-phase iTCM method with experiment.

Q3 *How does the variable switching frequency profile influence the supra-harmonics generated by the PFC converter?*

- Develop the analytical model of the supra-harmonics from the PWM converter under variable switching frequency.
- Propose fast and accurate harmonic acquisition algorithm based on the derived harmonic spectrum model.
- Analyze the harmonic spectral properties under the variable switching frequency.
- Optimize the switching frequency profile to obtain the minimum size of filter with regard the harmonics standard.
- Verify the accuracy of the harmonic spectrum model and the optimal frequency profile with the experimental results.

Q4 *How to ensure the control stability of the grid-connected converter with the LCL filter?*

- Make a survey of the existing control methods for the LCL-filtered grid-connected converter.
- Model and analyze the capacitor-current-feedback based active damping method (CCAD) and the influence of the harmonics controller.
- Derive the analytical boundary of the CCAD method under system delay influence.
- Verify the proposed controller with the experimental tests.

1.3. THESIS CONTRIBUTIONS

The main contributions of this thesis are summarized below:

- The review of different PFC solutions and the preliminary experimental validations of these concept (**Chapter 2**).
- The development of the three-phase iTCM PFC converter system for the high efficiency and lightweight on-board EV charger (**Chapter 3**).
- The analytical model of the harmonic spectrum of the PWM converter under arbitrary periodic variable switching frequency profiles and the proposed fast acquisition algorithm for the harmonic model based on vectorization (**Chapter 4**).
- The insightful spectral analysis of the harmonics generated by the variable switching frequency and frequency profile optimization for redcued filter size (**Chapter 5**).
- The analytical boundary of the capacitor-current-feedback active damping technique in the practical grid-connected PFC system (**Chapter 6**).

1.4. THESIS OUTLINE

The remainder of this thesis is dedicated to addressing the four proposed research questions, with each question forming the basis of one or two chapters.

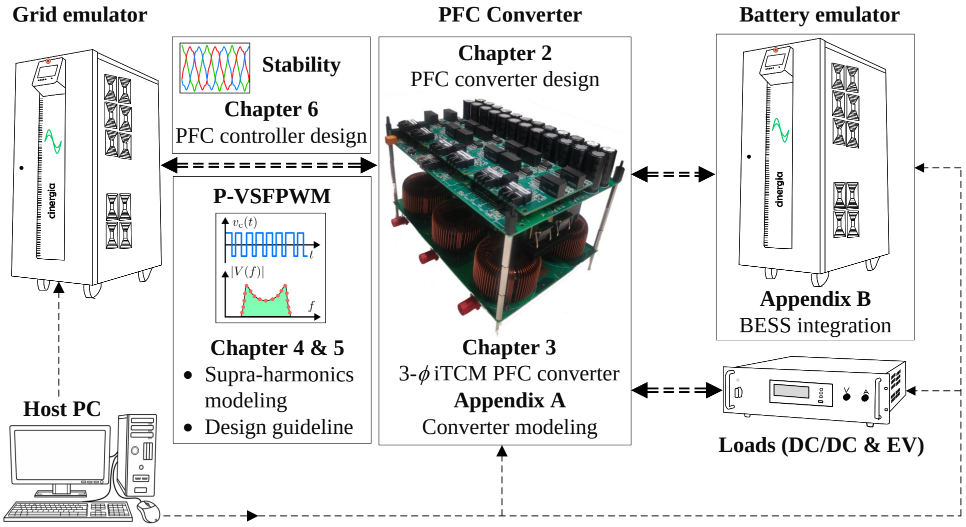

Grid emulator
PFC Converter
Battery emulator
Stability
Chapter 6
PFC controller design
Chapter 2
PFC converter design
P-VSFPWM
$v_c(t)$
t
$|V(f)|$
f
Chapter 4 & 5
Supra-harmonics modeling
Design guideline
Chapter 3
3-ϕ iTCM PFC converter
Appendix A
Converter modeling
Appendix B
BESS integration
Loads (DC/DC & EV)
Host PC
cinergia

Figure 1.5: Outline of the thesis and the connections between the chapters.

The outline and interconnections among the chapters of this thesis are illustrated in Fig. 1.5. Chpater 2 introduces the design of the front-end PFC converter e.g., three-phase 3-level T-type converter and three-phase 2-interleaved 2-level converter, as well as several PFC converter concepts for the heavy-duty EV chargers. Chapter 3 presents the modeling and design of the novel three-phase integrated triangular-current-mode converter for the on-board chargers. Chapter 4 analytically modells the supra-harmonics generated by the PWM converter under arbitrary periodic variables switching frequency profiles and proposes a fast harmonic spectra acquisition algorithm for the derived model. Chapter 5 provides a sightful spectra analysis based on the derived harmonic spectra model and optimizes the frequency profile to reduce the filter size required by the harmonic emission standard. Chapter 6 presents the design of the current controller based on the capacitor-current-feedback active damping and harmonics control and analytically identifies the control boundary for the control stability. Finally Chapter 7 summarizes the thesis by answering the research questions with conclusions and outlining the future work.

2

FRONT-END AC-DC PFC CONVERTER FOR EV CHARGER

This chapter begins with a review of different power electronics topologies for the front-end AC-DC PFC converter in EV chargers. Subsequently, it delves into detailed design methodologies for two specific topologies: the three-phase 3-level T-type converter and the three-phase 2-interleaved converter. Employing multi-objective optimization (MOO) techniques, the design process aims to achieve an optimal balance between efficiency and power density by leveraging available core databases in the market. Additionally, the chapter explores innovative high-power PFC charger solutions, such as the 12-pulse buck rectifier and hybrid rectifier, offering promising alternatives for heavy-duty vehicle chargers. Preliminary experimental results are also discussed to provide insights into the feasibility and effectiveness of these proposed solutions.

This chapter is based on the following research articles:

- D. Lan, Y. Wu, T. B. Soeiro, P. Granello, Z. Qin and P. Bauer, "12-pulse Rectifier with DC-Side Buck Converter for Electric Vehicle Fast Charging," IECON 2022 – 48th Annual Conference of the IEEE Industrial Electronics Society, Brussels, Belgium, 2022, pp. 1-6.
- R. Qiang, Y. Wu, T. B. Soeiro, P. Granello, Z. Qin and P. Bauer, "A New Input-Parallel-Output-Series Three-Phase Hybrid Rectifier for Heavy-Duty Electric Vehicle Chargers," IECON 2022 – 48th Annual Conference of the IEEE Industrial Electronics Society, Brussels, Belgium, 2022, pp. 1-6.

2.1. INTRODUCTION

The focus of this chapter is on the AC/DC converter topologies suitable for the two-stage charger system, which is widely implemented in the current EV charger market. The literature review for a single-stage system (Isolated Single-stage AC/DC converter) is beyond the scope of this chapter. For a two-stage charger, with the AC interface (EMI & harmonics filter) connected to the MV grid, the active front-end converter can be designed as either a transformer-based or transformer-less (modular) structure. This chapter begins with a review of the AC-DC converter topologies for these two scenarios and introduces detailed design methodologies for two specific topologies: the three-phase 3-level T-type converter and the three-phase 2-interleaved converter, employing multi-objective optimization (MOO) techniques. Additionally, two innovative high-power PFC charger solutions, such as the 12-pulse buck rectifier and hybrid rectifier, are studied and researched for heavy-duty vehicle chargers.

2.2. CONFIGURATION FOR DC FAST CHARGER

2.2.1. TRANSFORMER-BASED STRUCTURE

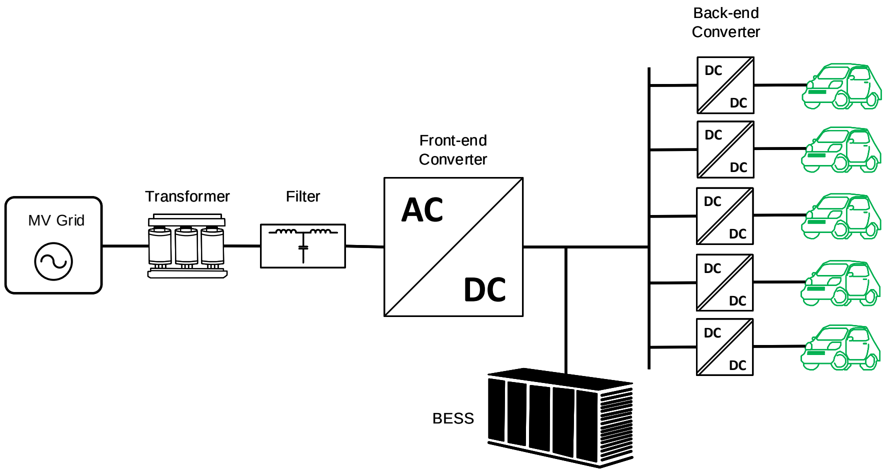


Figure 2.1: Schematic of MV grid-tied DC fast charger with transformer-based front-end converter

The state-of-the-art DC fast charging system, as illustrated in Fig. 2.1, typically incorporates a three-phase distribution transformer to step down medium voltage to low AC voltage, aligning with the input voltage rating of the front-end converter [31]. In this system configuration, the battery energy storage system (BESS) can be directly connected to the DC link capacitor of the AC/DC converter or connected via an additional DC/DC converter. However, a notable drawback of this setup is the bulky and costly nature of the MV transformer, which introduces extra losses and limits the power density of the entire system [32]. Nevertheless, despite these limitations, this conventional system structure remains prevalent in industrial applications due to its simplicity and well-established technology [31, 33].

2.2.2. TRANSFORMER-LESS STRUCTURE

The transformer-less structure, as illustrated in Fig. 2.2, typically employs a modular front-end converter [26, 34–36]. This modular approach eliminates the need for the MV transformer, offering the potential to increase the overall power density of the system. Additionally, the modularity of the AC/DC converter enables scalable output power and voltage, leading to cost advantages in manufacturing (i.e., low cost per kW). With a single-circuit building block design capable of serving multiple business applications, the modular approach offers flexibility and cost-effectiveness. Moreover, it simplifies adaptation to different voltage ratings of the connected AC grid, as modules can be easily substituted, unlike the conventional approach that requires designing transformers accordingly. In addition, due to the requirement for a high number of submodules to block the medium voltage on the grid side, various configurations can be selected at the parallel-connection level to achieve a multiport output capable of charging different vehicles simultaneously [36].

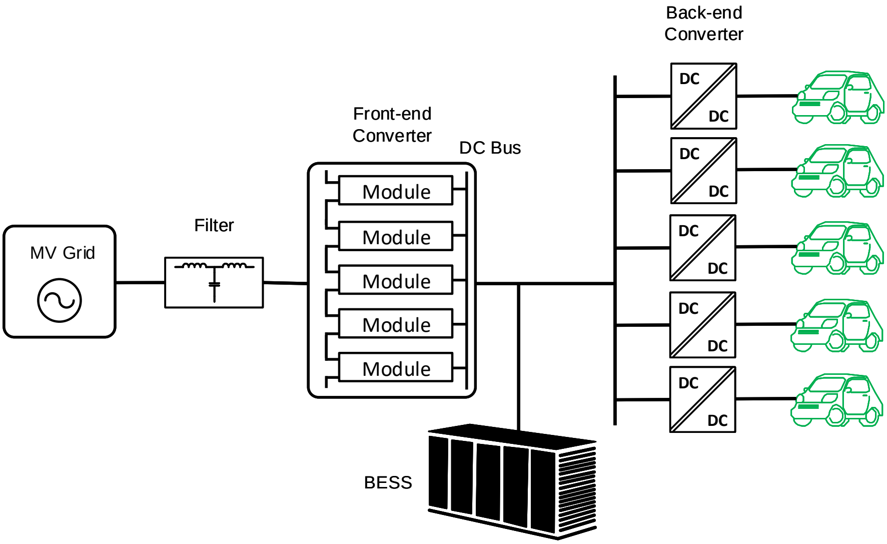
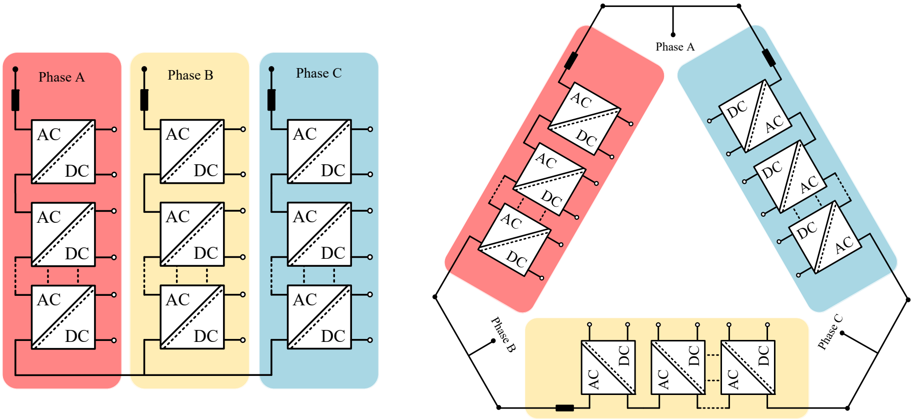


Figure 2.2: Schematic of MV grid-tied DC fast charger with transformer-less front-end converter

DIFFERENT CONFIGURATIONS

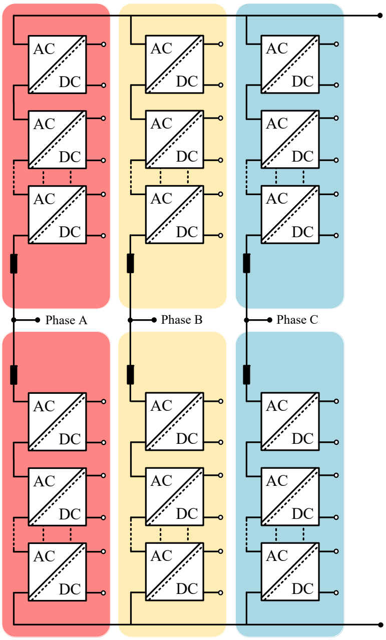
The AC/DC converter can be modularly designed in each phase, with the medium voltage (MV) level phase voltage divided among the AC/DC converter cells by cascading the cells in series. The interconnection possibilities for the phase strings include star, delta, and double-star connections, as illustrated in Fig. 2.3. The modular structure at the phase level implies the adoption of the single-phase converter topology for each converter cell. The dashed line in the module shown in Fig. 2.3 indicates that the cell can implement both two-stage or single-stage isolated topologies.

Typically, when the converter cell in the phase modular AC/DC converter is configured



(a) Star configuration

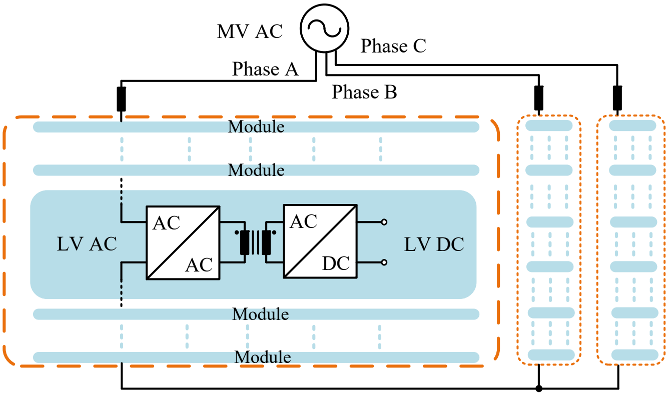
(b) Delta configuration



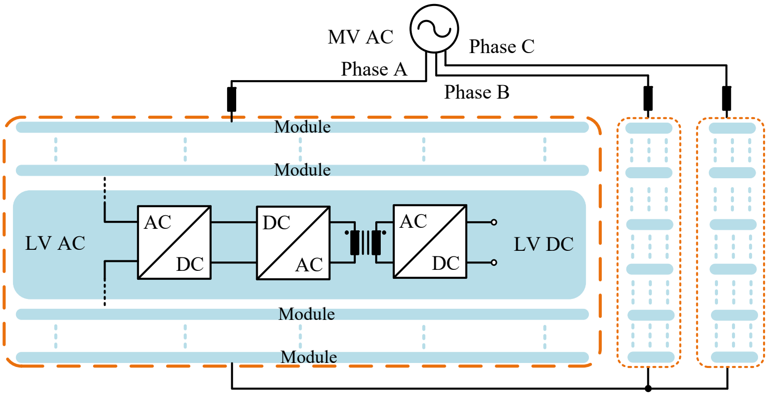
(c) Double-star configuration (MMC structure)

Figure 2.3: Phase Modular AC/DC configurations.

with a two-level Full bridge topology and connected in a star configuration, it forms what is known as a cascaded H-bridge (CHB) topology. In this setup, a medium voltage (MV) DC bus is not directly available, but it can be created by connecting the split DC outputs of the modules in series. However, this is only feasible when the AC/DC converter adopts isolated converter modules. Alternatively, a DC/DC converter can be attached to the DC output of each AC/DC module, and the DC outputs of these DC/DC converters can be linked to establish a common DC bus. With the star connection, the phase string voltage exhibits positive and negative polarity, making bipolar module topologies suitable for this configuration.


MV AC
Phase C
Phase A
Phase B
Module
Module
AC
AC
AC
DC
LV AC
LV DC
Module
Module

(a) Phase modularity with single-stage AC-DC structure.


MV AC
Phase C
Phase A
Phase B
Module
Module
AC
DC
DC
AC
AC
DC
LV AC
LV DC
Module
Module

(b) Phase modularity with two-stage AC-DC structure.

Figure 2.4: Phase Modular AC/DC configurations.

In a delta connection, the suitable module topologies are similar to those used in a star connection. However, the voltage across the converter module is increased by a factor of $\sqrt{3}$ compared to the star connection, while the phase branch current is reduced by a factor of $\frac{1}{\sqrt{3}}$ under the same AC grid conditions. On the other hand, in a double-star connection, the AC/DC converter topology consists of three phase strings, each with two arms, resembling the circuitry characteristic of a modular multilevel converter (MMC). Unlike the star/delta connection, only unipolar module topologies can be used in this configuration, as the AC voltage of the modules exhibits only positive polarity. It's worth noting that a non-isolated MV DC bus connection is provided in the double-star configuration, which differs from the single-star configuration. The phase modularity structure depicted in Fig. 2.4 is limited to adopting a single-phase topology, whether it's a single-stage or two-stage topology. This limitation results in a power ripple of twice the fundamental frequency in the DC output power. To mitigate this ripple, a power decoupling circuit must be implemented, adding extra circuitry and control complexity. An alternative modular solution, illustrated in Fig. 2.5, integrates three AC/AC converters via a multi-ports transformer and the three-phase inputs, allowing for direct implementation. This configuration eliminates the need for additional power decoupling circuits and reduces overall complexity.

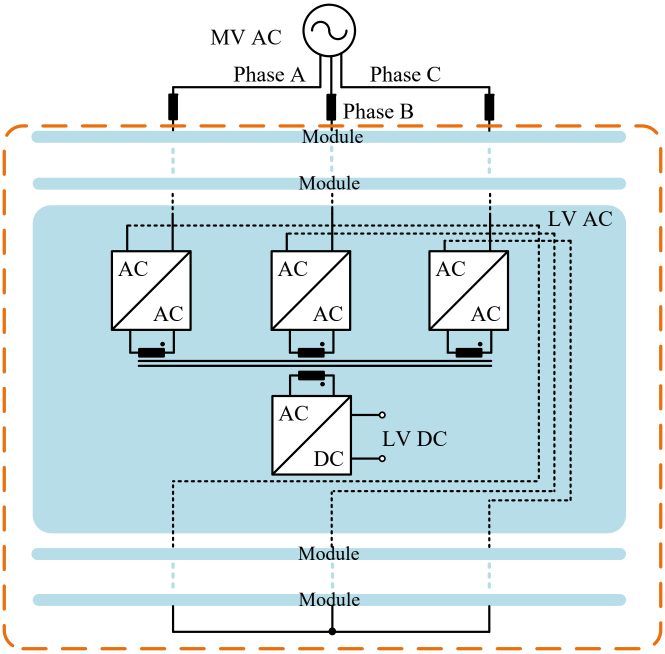
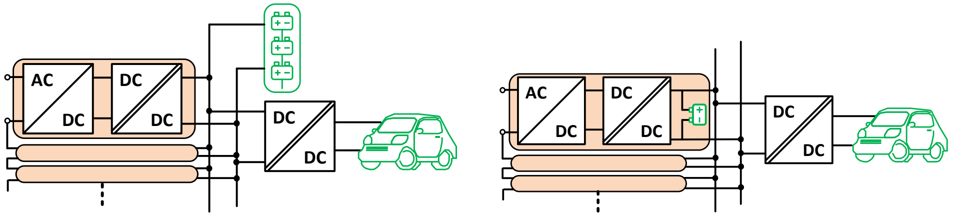


Figure 2.5: Modularity combining the three-phase inputs.

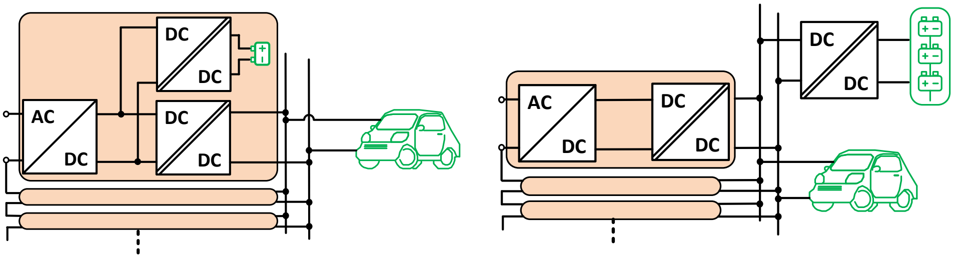
POSITIONING OF THE BESS IN THE MODULAR FRONT-END CONVERTER

In the modular configuration of the charging station, incorporating the battery energy storage system (BESS) introduces various potential arrangements. As illustrated in Fig. 2.6, four possible configurations are depicted. In this setup, an additional DC/DC converter is essential for each module to establish a common DC bus for the BESS. There are two primary reasons for the necessity of these converters:



(a) BESS installed at the DC bus.

(b) Individual BESS unit installed at the DC bus.



(c) Individual BESS unit installed at the DC link of the AC-DC converter via a DC-DC converter.

(d) BESS installed at the DC bus via a DC-DC converter.

Figure 2.6: Possible placement of the BESS in the modular EV charger structure.

- Without the DC/DC converters, there's a risk of direct short-circuiting between the AC/DC converter cells or bridge legs during normal switching operations when their outputs are directly paralleled together.
- The DC/DC converters connected to the DC bus play a crucial role in regulating the voltage and power flow of the BESS, ensuring efficient operation and optimal performance.

2.3. AC-DC FRONT-END CONVERTER TOPOLOGY

Based on the configuration of the active front-end converter, several candidate topologies are viable for the AC/DC converter. For the transformer-based configuration, three-phase converter topologies (Fig. 2.7) are suitable, while single-phase converter topologies depicted in Fig. 2.8 and 2.9 are applicable for the transformer-less configuration.

2.3.1. FOR TRANSFORMER-BASED STRUCTURE.

Table 2.1 compares topology candidates based on voltage, current ratings, and control complexity [37, 38]. Overall, 3-level T-type and 2-interleaved 2-level converters are more efficient than 3-level NPC at low and medium switching frequencies [38].

THREE-PHASE 2-LEVEL CONVERTER

The conventional VSC topology is commonly employed in low voltage and power applications due to its simple circuitry and low component count. However, this topology

Table 2.1: Comparison between Transformer-based AC-DC Converter Topology Candidates.

Topology	2L	3L T-type	3L NPC	3L ANPC	2L INT
Voltage rating	High	Medium	Medium	Medium	High
Current rating	High	High	High	High	Medium
Control complexity	Low	Medium	Medium	High	Medium

suffers from drawbacks such as reduced efficiency at higher switching frequencies and suboptimal output voltage performance [37]. Addressing these issues typically necessitates larger AC filter inductors, resulting in decreased power density.

THREE-PHASE 3-LEVEL NEUTRAL-POINT CLAMPED (NPC) CONVERTER

The 3-level NPC topology offers advantages over the 2-level VSC, notably in terms of output voltage waveform quality. This can translate to a smaller filter size requirement if the same filtering standards are applied. Additionally, operating at higher switching frequencies can significantly reduce total semiconductor losses despite the increased number of semiconductor devices and conduction losses [37, 39]. However, the increased costs and complexity associated with this topology have limited its adoption, particularly in the low-voltage market [40].

THREE-PHASE 3-LEVEL ACTIVE NEUTRAL-POINT CLAMPED (A-NPC) CONVERTER

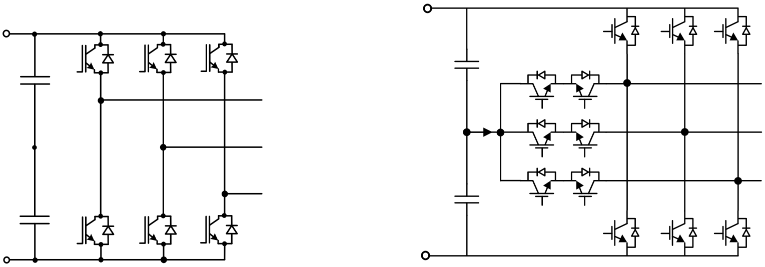
The 3-level A-NPC topology addresses a significant drawback of the 3-level NPC topology, which is the uneven distribution of losses across the semiconductor devices leading to uneven junction temperature distribution [41]. However, the A-NPC topology introduces its own disadvantages, including the requirement for two extra active switches and isolated gate drivers per phase leg [40].

THREE-PHASE 3-LEVEL T-TYPE CONVERTER

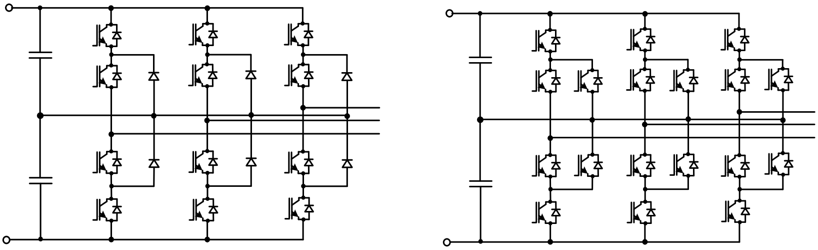
The T-type topology utilizes an active bidirectional switch connected to the DC-link voltage midpoint, offering a simpler alternative to more complex three-level topologies like the active neutral point clamped converter. It combines the favorable characteristics of the two-level converter, such as low conduction losses, a minimal part count, and straightforward operation principles, with the benefits of three-level converters, including reduced switching losses and superior output voltage quality [42]. This advantage is made possible by the use of bidirectional switches with lower ratings [37].

TWO-INTERLEAVED THREE-PHASE 2-LEVEL CONVERTER

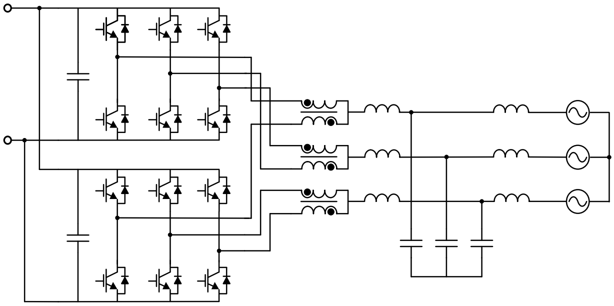
The interleaving structure involves a unique configuration where converters are paralleled with their modulation carriers phase-shifted by 180°. This setup offers improved harmonics performance of the output voltage by leveraging harmonics cancellation between the interleaved converters [43, 44]. Consequently, it allows for a smaller filter size compared to a standard 2-level VSC, maintaining the same filtering requirements and



(a) Three-phase 2-level VSC. (b) Three-phase 3-level T-type VSC.



(c) Three-phase 3-level NPC VSC. (d) Three-phase 3-level APNC VSC.



(e) Three-phase 2-Interleaved 2-level VSC.

Figure 2.7: Topologies for non-modular three-phase AC-DC converter.

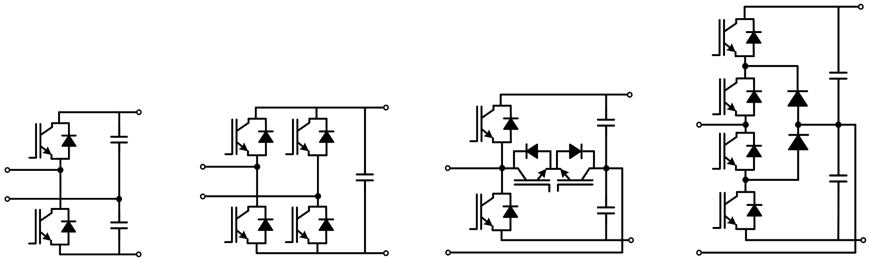
thereby increasing the power density of the converter system [45]. However, a drawback of this topology is the complexity in magnetics design, as the inherent circulating current necessitates hardware efforts such as intercell transformer design [46]. Additionally, paralleling converters require synchronized control [44].

OTHER MULTILEVEL CONVERTERS

Higher-order multilevel converters typically require series connections of diodes or flying capacitors, which introduce significant parasitic issues. As the number of levels increases, the complexity rises while reliability decreases [39].Therefore, these topologies are not included in the comparison.

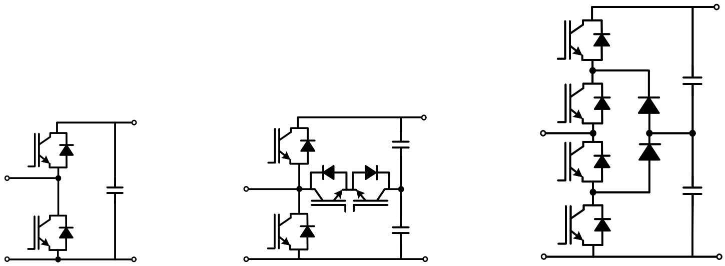
2.3.2. FOR TRANSFORMER-LESS STRUCTURE.

For the star/delta connection, possible module topologies include single-phase bipolar modules, such as the 2-level half-bridge (HB), 3-level full-bridge (FB), 3-level T-type, and 3-level NPC, as shown in Fig. 2.8. This is because each module shares the AC input voltage equally, and the polarity changes according to that of the grid voltage. In the case of a double-star connection, only unipolar modules are required. This is because the polarity of the input voltage of each module changes to a single polarity due to the existence of the MV DC bus. Possible candidate topologies are shown in Fig. 2.9. The modular design solution is not considered in this thesis due to its increased complexity and control efforts compared to the transformer-based structure.



(a) 2-level HB. (b) 2-level FB. (c) 3-level T-type. (d) 3-level NPC.

Figure 2.8: Bipolar topologies for the AC-DC module in star/delta connection.



(a) 2-level HB. (b) 3-level T-type. (c) 3-level NPC.

Figure 2.9: Unipolar topologies for the AC-DC module in double-star connection.

2.4. DESIGN OF THE THREE-PHASE AC-DC PFC CONVERTER

In this section, the three-phase 3-level T-type converter and the 2-interleaved 2-level converter are chosen for design, construction, and testing due to their optimal balance between harmonics performance and efficiency compared to other topologies. Firstly, the modulation strategies to be implemented are elaborated, and the resulting switching harmonics are derived and presented in Appendix A. The magnetics for these two topologies are designed using a multi-objective optimization approach, and the efficiency performance is compared among different design options. Finally, 10 kW prototypes are built and tested for both converters.

2.4.1. MODULATION TECHNIQUES

The modern modulation techniques for AC/DC converters can be broadly categorized into continuous PWM (CPWM) and discontinuous PWM (DPWM). CPWM methods, such as SPWM, THIPWM, and SVPWM, maintain a continuous zero-sequence waveform, while DPWM methods (including DPWM0, DPWM1, DPWM2, DPWM3, DPWMMAX, and DPWMMIN), exhibit a discontinuous zero-sequence signal with phase segments clamped to either positive or negative DC rails [47]. Implementing DPWM methods can effectively reduce the switching loss of semiconductor devices. This reduction occurs because during zero-vector switching cycles, either the upper or lower devices are conducting, leading to no switching actions during this period in the converter [47, 48]. In Fig. 2.10, the modulation waveform and the instantaneous switching power loss (normalized) of SVPWM and DPWM are compared when the power factor angle is 0. It's evident that there is a notch in the switching loss waveform in the DPWM method compared to the CPWM one. The algorithms to realize these different modulations are listed as follows [48]:

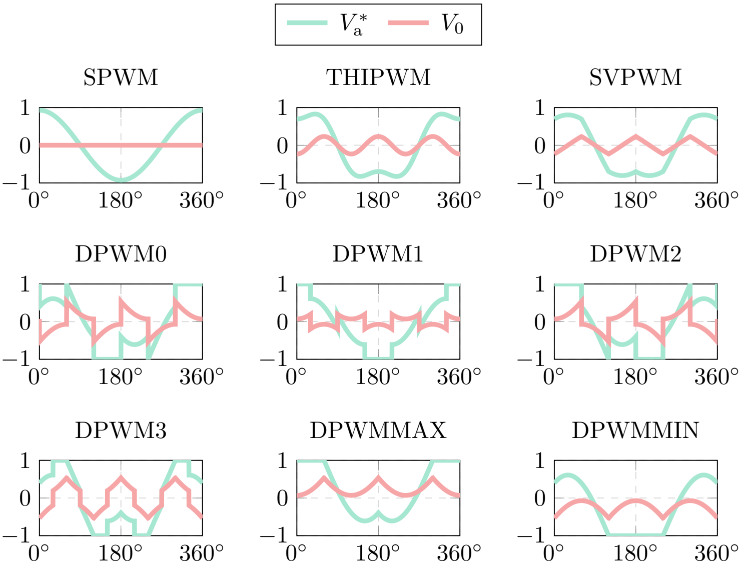


Figure 2.10: Normalized waveforms of the modulation voltage and the zero-sequence voltage under different PWM methods.

SPWM

The reference modulation wave is compared with a triangular carrier wave and the intersections define the switching instants. The zero-sequence signal is zero.

THIPWM

The zero-sequence signals for the 1/6-and 1/4-THIPWM are $v_0 = -\frac{V_\mathrm{m}}{6}\cos(3\omega_\mathrm{m} t)$ and $v_0 = -\frac{V_\mathrm{m}}{4}\cos(3\omega_\mathrm{m} t)$ respectively. V_m is the magnitude under SPWM.

SVPWM

The zero-sequnce signal is obtained by minimum magnitude test [48]. Assume $|v_\mathrm{a}^*| \le |v_\mathrm{b}^*|, |v_\mathrm{c}^*|$, $v_0 = 0.5 \times |v_a^*|$.

DPWMMAX, DPWMMIN

The reference signals with the maximum and minimum value defines the zero-sequence signals of DPWMMAX and DPWMMIN respectively. Assume $|v_\mathrm{b}^*| \le |v_a^*| \le |v_\mathrm{c}^*|$. For the former, $v_0 = 0.5 \times V_\mathrm{dc} - |v_\mathrm{c}^*|$. For the latter, $v_0 = 0.5 \times V_\mathrm{dc} - |v_\mathrm{b}^*|$.

DPWM3

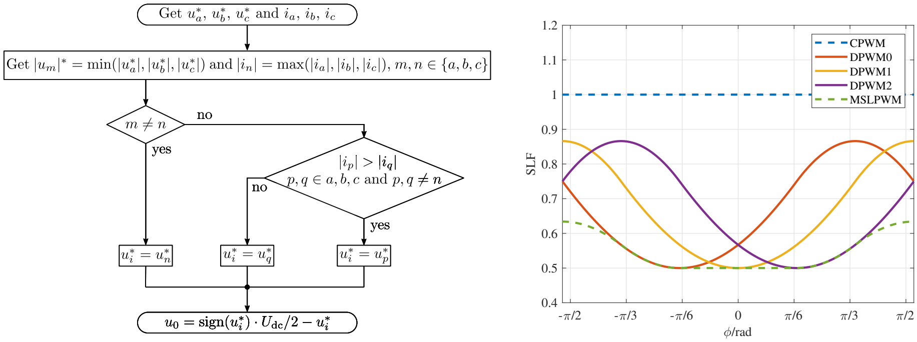
The reference with intermediate magnitude defines the zero-sequence signal. Assume $|v_\mathrm{b}^*| \le |v_\mathrm{a}^*| \le |v_c^*|$, $v_0 = sign(v_\mathrm{a}^*)(0.5 \times V_\mathrm{dc}) - |v_\mathrm{a}^*|$.

DPWM0, DPWM1 AND DPWM2

Define a modulator phase angle ψ and shift the references voltages v_a^*, v_b^* and v_c^* by $\psi - \pi/6$ to obtain v_ax^*, v_bx^* and v_cx^*. Assume $|v_\mathrm{ax}^*| \ge |v_\mathrm{bx}^*| \le |v_\mathrm{cx}^*|$, then $v_0 = sign(v_\mathrm{a}^*)(0.5 \times V_\mathrm{dc}) - |v_\mathrm{a}^*|$. DPWM0, DPWM1 and DPWM correspond to the cases of $\psi = 0, \pi/6$ and $\pi/3$.

MSLPWM

The Minimum Switching-Loss PWM (MSLPWM) functions an optimization of DPWM to minimize switching loss during operation [49]. The algorithm, depicted in Fig. 2.11(a), aims to track the route for minimum switching loss with varying power factor angles. As depicted in Fig. 2.11(b), the switching-loss function of the MSLPWM method consistently follows the path for minimum switching loss compared to other modulations.



(a) Algorithm for MSLPWM.

(b) Switching-loss function (SLF).

Figure 2.11: Realization of MSLPWM and its SLF performance.

2.4.2. CONVERTER OPERATION PRINCIPLES

T-TYPE CONVERTER

The basic structure of the three-phase 3-level T-type converter is depicted in Fig. 2.12, comprising a DC link with split electrolytic capacitors, four switching devices for each phase and a LCL filter to obtain the target ac output voltage. Generally, three different phase relationships are offered to the carrier-based PWM in multi-level converters, namely alternative phase opposition disposition (APOD), phase opposition disposition (POD) and phase-disposition (PD) strategies. It should be noted that the APOD and POD strategies are equivalent for three-level converters. PD and POD strategies are illustrated in Fig. 2.13. It is generally accepted that the PD strategy results in the lowest harmonic distortion in the line-to-line voltage compared to the rest strategies [50, 51]. Therefore, PD strategy is considered in this paper for the development of switching harmonics model for three-level converter. The PWM output states for the T-type converter with PD strategy are listed in Table 2.2. In this configuration, the converter switches are operated as complementary pairs: S_1/S_3 and S_2/S_4. These pairs are controlled to achieve the required switched output voltages of $+V_{dc}/2$, 0, and $-V_{dc}/2$, resulting in a three-level AC output voltage. It is noteworthy that the switching states shown in Table 2.2 achieve the same switched output voltages as an NPC converter but the specific switch usage may differ between the two converter topologies [42, 52]. Based on the spectral analy-

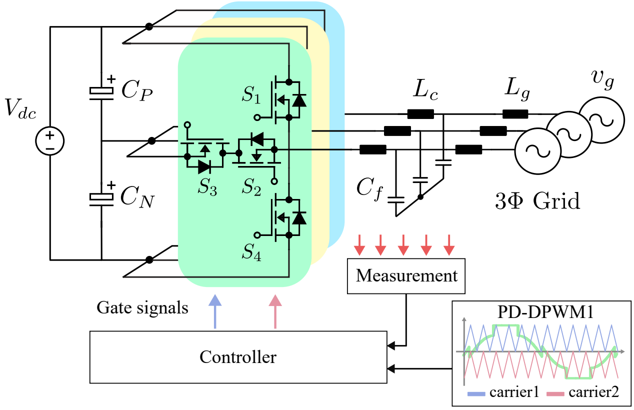
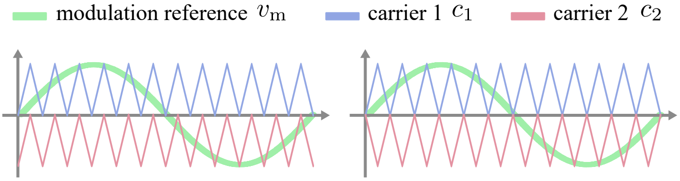


Figure 2.12: Three-phase 3-level T-type converter with a LCL filter.

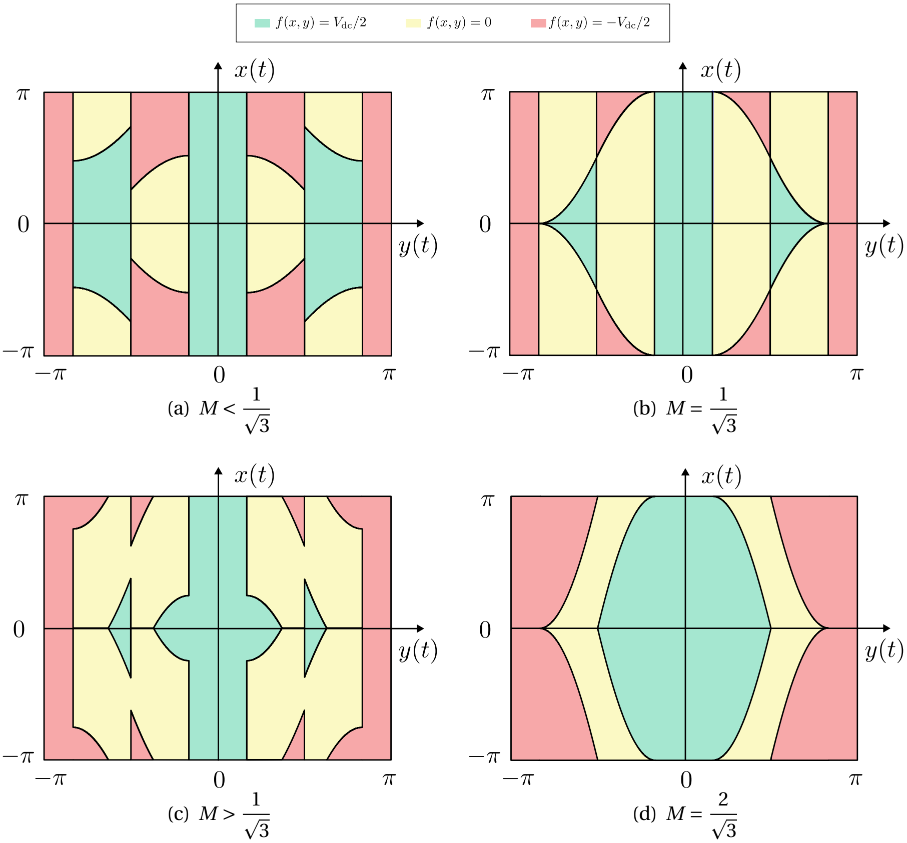


(a) PD (b) POD

Figure 2.13: PD and POD strategy in three-level converter.

Table 2.2: PWM Output States for T-type Converter

Output Voltage	S_1	S_2	S_3	S_4
$V_{dc}/2$	1	1	0	0
0	0	1	1	0
-$V_{dc}/2$	0	0	1	1



(a) $M < \frac{1}{\sqrt{3}}$ (b) $M = \frac{1}{\sqrt{3}}$

(c) $M > \frac{1}{\sqrt{3}}$ (d) $M = \frac{2}{\sqrt{3}}$

Figure 2.14: Contour plot of PD-DPWM1 under different modulation index M.

sis presented in Appendix B, the contour plot for PD-DPWM1 can be also obtained and presented in Fig. 2.15. It can be noted from the contour plot that the expressions of the integral limits are different as M varies. The modulation index M is split into two equal ranges:

Range 1 ($0 \leqslant M \leqslant 1/\sqrt{3}$): the integral limits for the three output states are continuous in the seven individual sectors.

Range 2 ($1/\sqrt{3} \leqslant M \leqslant 2/\sqrt{3}$): the integral limits for the three states output exhibit discontinuity in sectors II, III, V and VI, which further complicates the model derivations. At $M = 2/\sqrt{3}$, the integral limits become continuous again in all sectors.

The harmonic coefficient C_{mn} can be determined by substituting the integral limits depicted by Fig. 2.14 into (B.4) for the full range of M. For base-band harmonics ($m = 0$, $n > 0$), the harmonic coefficient C_{0n} is solved in (B.5). For $m > 0$, $n \geqslant 0$, the harmonic coefficient for carrier and side-band harmonics are derived in (B.6) and (B.7) for the two different M ranges. It should be noted that the base-band harmonics are actually the harmonics of the modulated voltage ($V_{\mathrm{dc}}/2 \times v_{\mathrm{m}}$). It is found that C_{0n} is non-zero only when $n = 6k + 3$, where k is a positive integer. Therefore, there exist low-order order common-mode (CM) harmonics, for instance 3^{rd}, 9^{th}, 15^{th} etc., in three-level converter with DPWM strategy. The coefficient of the carrier and side-band harmonics has a simpler expression in range 1 of M as compared to range 2.

2-INTERLEAVED CONVERTER

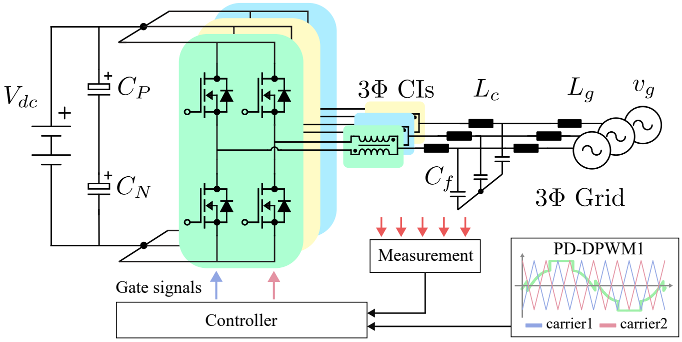


Figure 2.15: Three-phase 2-interleaved 2-level converter with the coupled inductor and LCL filter.

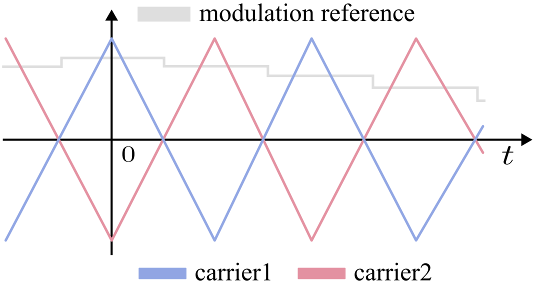
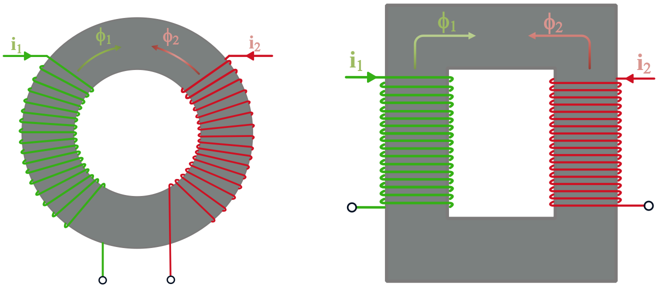


Figure 2.16: carrier-based PWM for interleaved 2-level PWM converter.

Under the carrier-based PWM strategy of the interleaved converter, the two interleaved bridge legs share the same modulation reference signal but adopt the opposite triangle carriers, which are interleaved by 180° as depicted in Fig. 2.16. Hence, we have

$$\begin{cases} x_1 = x_2 + \pi \\ y_1 = y_2 \end{cases} \tag{2.1}$$

where x_1 and x_2 are the phases of the two carrier signals respectively. Additionally, the coupled inductors (CIs) with high coupling factor, for instance the toroidal- and UU-core based CIs as illustrated in Fig. 2.17, are required in the interleaved converter to suppress the unwanted circulating currents and hence avoid the increased stress on the semiconductor devices and extra losses. Take one phase of the interleaved converter as an example, the interleaved bridge legs can be represented by the circuitry shown in Fig. 2.18, where v_{c1} and v_{c2} are output voltages of the interleaved bridge legs. v_{eq} is the equivalent output voltage to the load, which is the concern of the supra-harmonic sources. Based on the Kirchhoff's laws (KVL and KCL), we can obtain the followings:



(a) Toroidal-CI (b) UU-CI

Figure 2.17: The coupled inductors with high coupling factor.

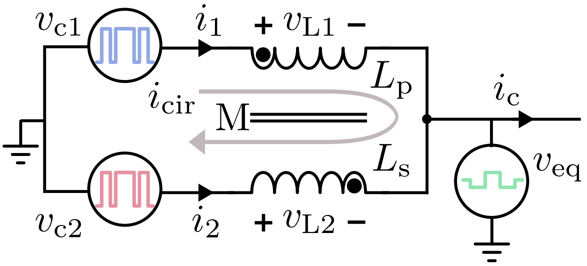


Figure 2.18: Circuit representation with the coupled inductor.

$$\begin{cases} v_{\mathrm{L1}} = v_{\mathrm{c1}} - v_{\mathrm{eq}} = L_{\mathrm{p}} \frac{\mathrm{d}i_1}{\mathrm{d}t} - M \frac{\mathrm{d}i_2}{\mathrm{d}t} \\ v_{\mathrm{L2}} = v_{\mathrm{c2}} - v_{\mathrm{eq}} = L_{\mathrm{s}} \frac{\mathrm{d}i_2}{\mathrm{d}t} - M \frac{\mathrm{d}i_1}{\mathrm{d}t} \\ i_1 = i_{\mathrm{c}}/2 + i_{\mathrm{cir}} \\ i_2 = i_{\mathrm{c}}/2 - i_{\mathrm{cir}} \end{cases} \tag{2.2}$$

where i_{cir} is the circulating current and L_{p}, L_{s} and M are the primary-side, secondary-side and mutual inductance respectively. Assume the symmetrical layout and equal winding turns of both sides, $L_{\mathrm{p}} = L_{\mathrm{s}}$ will be satisfied. Therefore (2.2) can be reduced to:

$$v_{\mathrm{eq}} = \frac{v_{\mathrm{c1}} + v_{\mathrm{c2}}}{2} - \frac{(L-M)}{2} \cdot \frac{\mathrm{d}i_{\mathrm{c}}}{\mathrm{d}t} = \frac{v_{\mathrm{c1}} + v_{\mathrm{c2}}}{2} - L' \frac{\mathrm{d}i_{\mathrm{c}}}{\mathrm{d}t} \tag{2.3}$$

Based on (2.3), the equivalent three-phase circuit of the grid-tied 2-level interleaved converter with CIs is described in Fig. 2.19, where the leakage inductance $L^{'} = L - M$ from the CIs is moved to the filter side and contributes to the filtering of the switching harmonics. From the harmonics point of view, the equivalent voltage v_{eq} now becomes:

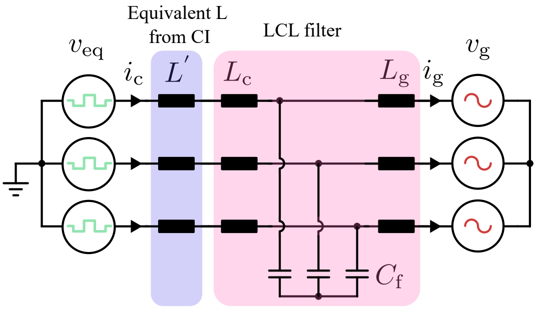
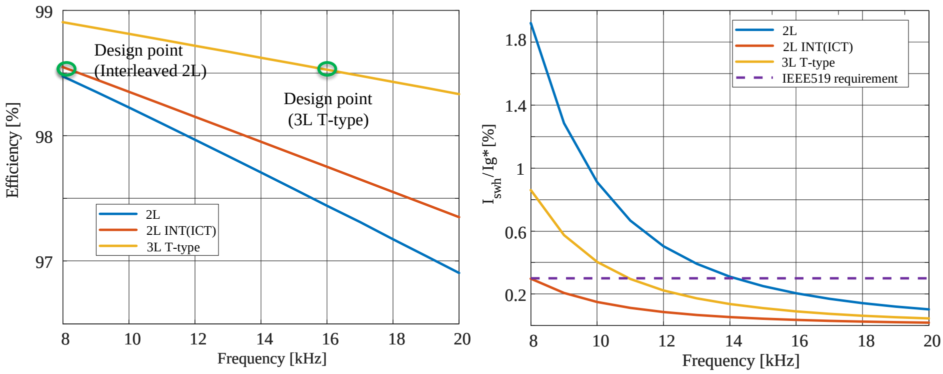


Figure 2.19: Equivalent three-phase circuit representation of the grid-tied interleaved 2-level converter with CIs.

$$v_{\mathrm{eq}} = \frac{v_{\mathrm{c1}} + v_{\mathrm{c2}}}{2} \tag{2.4}$$

COMPARISON BETWEEN T-TYPE AND 2-INTERLEAVED CONVERTERS



(a) Efficiency Curve (only converter loss considered)

(b) Maximum side-band harmonic

Figure 2.20: Comparison between 2-level, 3-level T-type and 2-interleaved 2-level converters (same power rating).

The efficiency curve with respect to switching frequency and the maximum side-band harmonics magnitude are depicted in Fig. 2.20 for three different topologies with the same power rating: two-level, interleaved two-level, and three-level T-type converters. Notably, the efficiency of the interleaved converter at 8 kHz is comparable to that of the T-type converter at 16 kHz. Additionally, the maximum side-band harmonics magnitude in these two cases is also similar. Consequently, the filters required for these converters will need to be designed to similar sizes and costs.

2.4.3. MULTI-OBJECTIVE OPTIMIZATION DESIGN

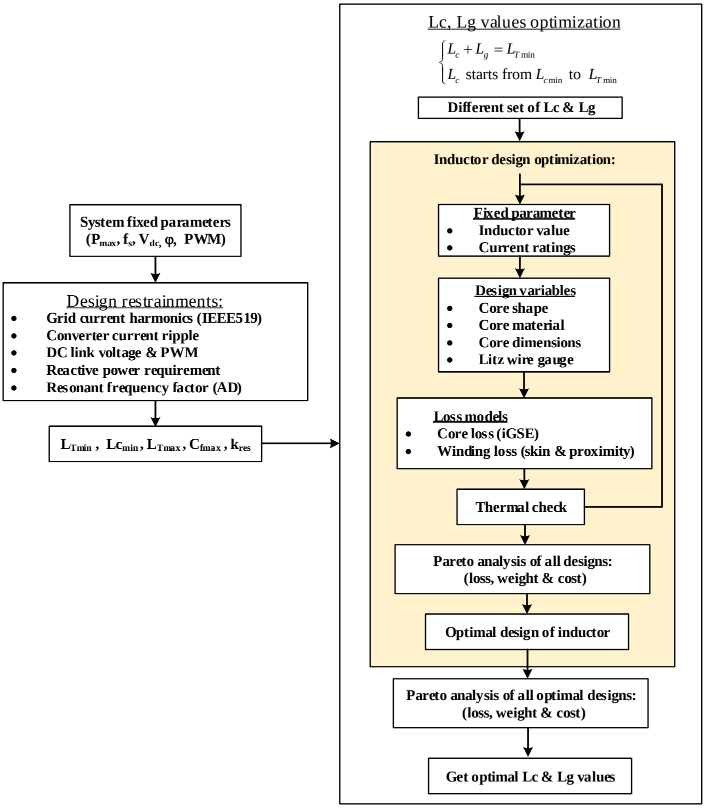
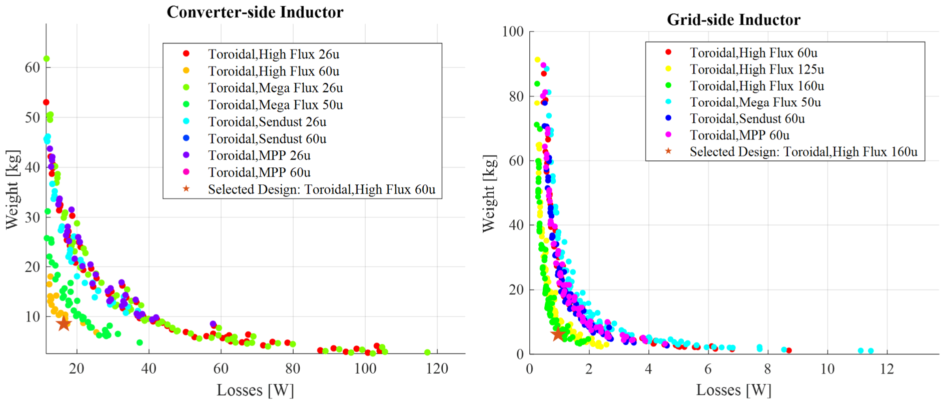

Lc, Lg values optimization
$\begin{cases} L_c + L_g = L_{T\min} \\ L_c \text{ starts from } L_{c\min} \text{ to } L_{T\min} \end{cases}$
Different set of Lc & Lg
Inductor design optimization:
Fixed parameter
Inductor value
Current ratings
Design variables
Core shape
Core material
Core dimensions
Litz wire gauge
Loss models
Core loss (iGSE)
Winding loss (skin & proximity)
Thermal check
Pareto analysis of all designs: (loss, weight & cost)
Optimal design of inductor
Pareto analysis of all optimal designs: (loss, weight & cost)
Get optimal Lc & Lg values
System fixed parameters (P_{max}, f_s, V_{dc}, φ, PWM)
Design restrainments:
Grid current harmonics (IEEE519)
Converter current ripple
DC link voltage & PWM
Reactive power requirement
Resonant frequency factor (AD)
L_{Tmin}, Lc_{min}, L_{Tmax}, C_{fmax}, k_{res}

Figure 2.21: LCL filter design flow chart

The design of the converter follows a structured process outlined as follows. Initially, the main specifications of the AC-DC converter are defined, encompassing parameters such as the input AC voltage level, the desired switching frequency, and any pertinent design constraints (such as maximum filter reactive power absorption, permissible grid current harmonics, and maximum output power and current ratings of the converter). Subsequently, the appropriate values for the inductors (L_c and L_g) and capacitor (C_f) are

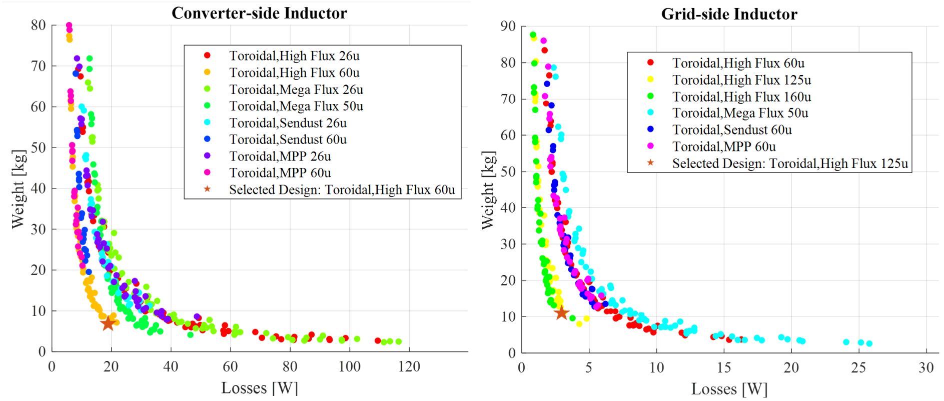


(a) L_c design space.

(b) L_g design space.

Figure 2.22: LCL design space for three-phase 3-L T-type converter at 11 kW and 16 kHz .

determined, taking into consideration factors like current ripple and compliance with grid-side harmonics standards. Finally, the modulation strategy for the selected converter topology is established, alongside the selection of suitable semiconductor components tailored to the power ratings of the converter.

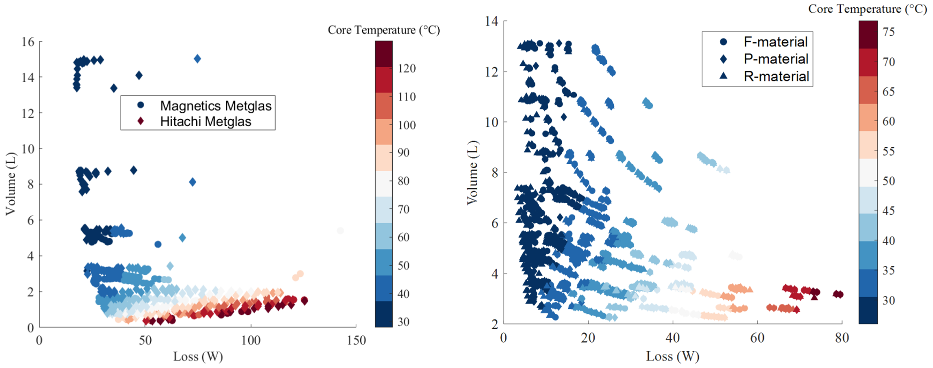


(a) L_c design space.

(b) L_g design space.

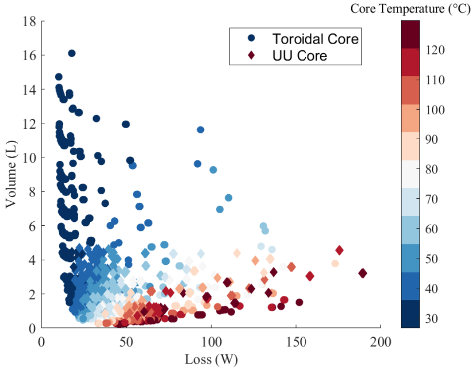
Figure 2.23: LCL design space for three-phase 2-interleaved 2-level converter at 11 kW and 8 kHz.

The selection of the AC filter is guided by a multi-objective design approach, as described in the inductor design optimization process illustrated in Fig. 2.21. In this methodology, the design objectives include weight (linked to cost) and passive losses. During the inductor design phase, various design variables are considered, such as the core material, core shape, and the number of stacked cores. The losses associated with each potential solution are meticulously calculated, encompassing both core loss (evaluated using



(a) With AMCC (Metglas).

(b) With Ferrite-UU core.



(c) With powder-core.

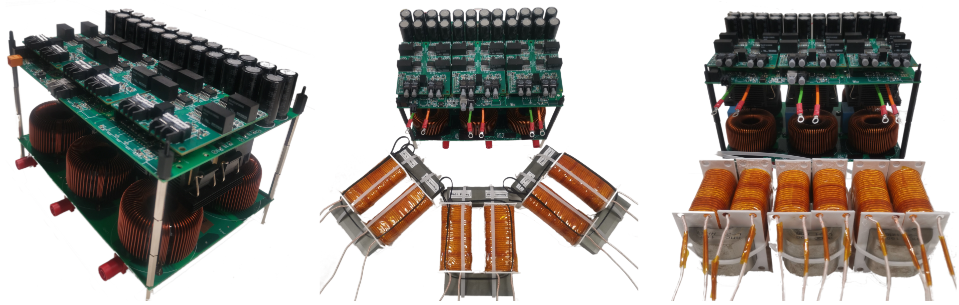
Figure 2.24: Coupled inductor design space for the three-phase 2-interleaved converter at 11 kW and 8 kHz.

the iGSE method) and winding loss (accounting for skin effect and proximity). Subsequently, a thermal assessment is conducted for each candidate solution to ensure thermal stability under operating conditions. From the pool of viable solutions, a design space is established, allowing for the selection of an optimal design that strikes a balance between cost, efficiency, and power density.

To identify the optimal design, the inductor design optimization process is applied to all potential designs. This process involves configuring the core and winding of the inductor to achieve the desired input inductance value. Subsequently, the optimal design is selected through a Pareto front analysis, which considers various design objectives and constraints. Once the optimal inductor designs for different inductance values are determined, they are compared based on loss and weight metrics. This comparison helps in identifying the optimal inductance value that strikes the best balance between performance and efficiency. The design space of the LCL filter for an 11 kW system is depicted in Fig. 2.22 and 2.23 for the T-type and 2-interleaved converters, respectively. In the multi-objective optimization (MOO) design, toroidal cores are exclusively considered for the AC filters due to their design simplicity and higher permeability of power-core materials. The database of the core materials is from Magnetics Powder Core Catalog [53].The T-type converter operates at 16 kHz, while the 2-interleaved converter operates at 8 kHz to facilitate a fair comparison. Analysis of the design space reveals that the grid-side inductor L_g offers significantly lower losses and occupies less space (weight) compared to the converter-side inductor L_c, attributed to the smaller current ripple stress experienced by the former. Additionally, it is evident that the optimal design points of the LCL filter lead to similar total losses and sizes of the filter for both converters.

The design space of the coupled inductors is illustrated in Fig. 2.24 for various materials, including amorphous cut-core (AMCC, also known as Metglas), powder core, and ferrite core. The core temperature is estimated using the approach outlined in [54]. The design analysis reveals that ferrite core exhibits significantly lower losses in the coupled inductors compared to other materials, albeit at the expense of increased size. Conversely, both powder core and AMCC demonstrate a favorable balance between size and losses, making them attractive options for the coupled inductors in terms of overall performance.

2.4.4. PROTOTYPE AND TEST RESULTS



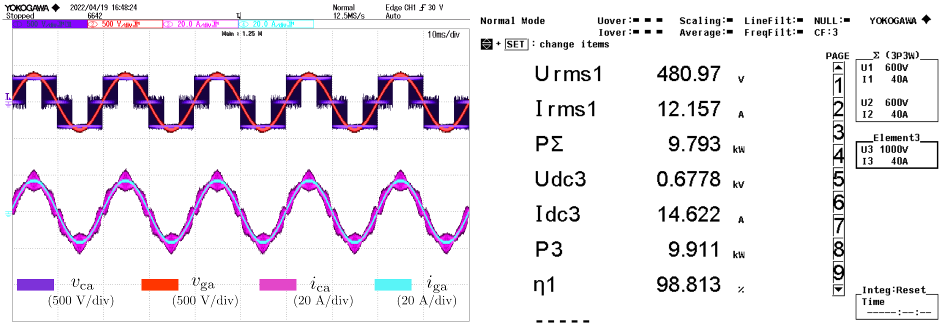
(a) 3-level T-type converter.

(b) 2-interleaved 2-level converter with Ferrite-UU as CIs.

(c) 2-interleaved 2-level converter with AMCC as CIs.

Figure 2.25: 11 kW prototypes of three-phase T-type and 2-interleaved converter.

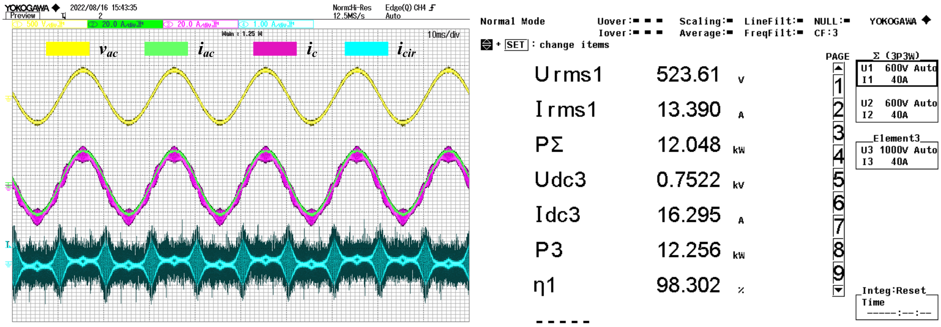
The 11 kW prototypes of the three-phase T-type and 2-interleaved converters are depicted in Fig. 2.25. Both prototypes feature identical PCB designs and layouts since they share the same power specifications and employ the same number of power semiconductors. Discrete IGBT devices are utilized in both prototypes, with the T-type converter employing IKW40N120CS6 (1200 V, 40 A) for the upper and lower switches, and IKW40N65F5 (650 V, 40 A) for the mid-point switching leg. Similarly, the 2-interleaved converter adopts the IKW15N120BH6 discrete IGBT device with a smaller current rating (1200 V, 15 A) across all switching legs. Fig. 2.25(b) and 2.25(c) showcase the two distinct coupled inductors, featuring U-U Ferrite cores and Amorphous Cut-Cores (AMCCs), respectively. These coupled inductors are designed based on the multi-objective optimization results illustrated in Fig. 2.24. They are specifically engineered to effectively



```
Urms1   480.97  V
Irms1   12.157  A
PΣ      9.793   kW
Udc3    0.6778  kV
Idc3    14.622  A
P3      9.911   kW
η1      98.813  %
```

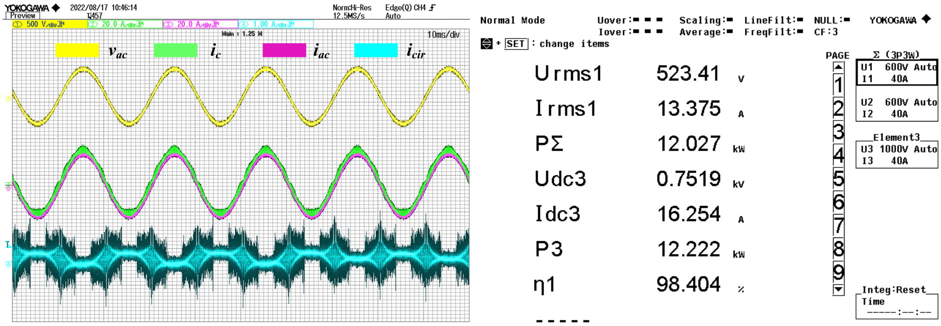
(a) Tested waveforms. (b) Tested efficiency

Figure 2.26: Tested results of 11 kW three-phase T-type 3-level converter prototype.



```
Urms1   523.61  V
Irms1   13.390  A
PΣ      12.048  kW
Udc3    0.7522  kV
Idc3    16.295  A
P3      12.256  kW
η1      98.302  %
```

(a) Tested waveforms with AMCC CIs. (b) Tested efficiency with AMCC CIs.



```
Urms1   523.41  V
Irms1   13.375  A
PΣ      12.027  kW
Udc3    0.7519  kV
Idc3    16.254  A
P3      12.222  kW
η1      98.404  %
```

(c) Tested waveform with Ferrite-core CIs. (d) Tested efficiency with Ferrite-core CIs.

Figure 2.27: Tested results of 11 kW three-phase 2-interleaved 2-level converter prototype.

mitigate the inherent circulating currents resulting from the PWM process and system asymmetry, while ensuring reasonable magnetic loss and compact volume.

The prototypes are tested under open-loop conditions in inverter mode with the resistive loads. The tested results are presented in Fig. 2.26 and 2.27 for T-type and 2-interleaved prototypes respectively. The experimental test recoreded the waveforms and the power efficiency at rated active power. The tested peak efficiency of the T-type prototype reaches 98.813% under DPWM1 method and 480 V AC line-to-line output voltage. Compared to T-type converter, the 2-interleaved converter prototype has a smaller but close peak efficiency 98.404% with the ferrite-UU cores as the coupled inductors. The AMCC CIs result in higher losses as compared to the ferrite cores, which corresponds to the results of MOO shown in Fig. 2.24.

2.5. CASE STUDY OF HIGH POWER HDEV CHARGER

Two PFC converters are proposed as the solutions to the high power charger for heavy-duty electric vehicles (HDEV).

2.5.1. 12-PULSE BUCK-TYPE RECTIFIER

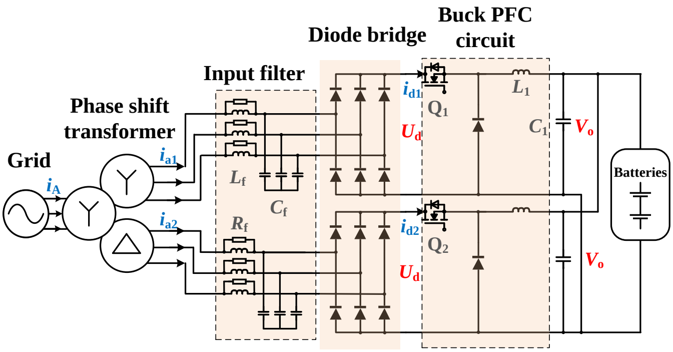
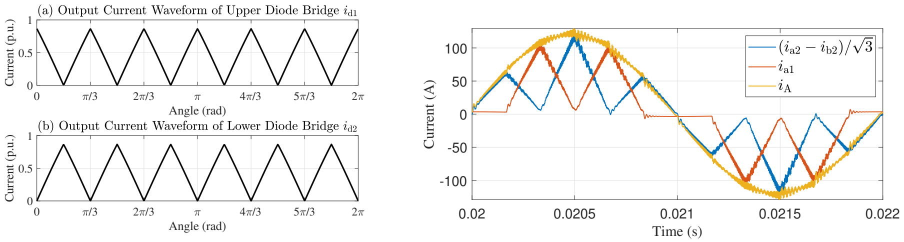


Figure 2.28: HDEV charger based on the buck-type 12-pulse AC-DC converter.

This section presents a study on a HDEV fast charger featuring a 12-pulse rectifier cascaded with two buck-type DC-DC converters, as illustrated in Fig. 2.28. The proposed circuit employs a triangular current shaping method, significantly enhancing the current harmonics performance of the system [55]. This configuration is well-suited for high-power battery charging, offering simplicity in operation, a low count of active semiconductors (only two active switches), and leveraging established circuit technologies in the high-power market. Furthermore, this EV fast charger satisfies requirements for isolation, high efficiency, high output voltage, and good power quality (low THD and unity power factor). As depicted in Fig. 2.29(a), the DC output currents i_{d1} and i_{d2} exhibit a phase shift of $\pi/6$, and their waveform closely resembles a standard triangular waveform. Therefore, assuming a sinusoidal input current, the diode bridge output current manifests as a standard triangular waveform. Conversely, a standard triangular output current from the diode bridge can be decomposed into sinusoidal current on the input



(a) DC output currents of the upper and lower the diode bridge.

(b) Simulated AC input current waveform.

Figure 2.29: Triangular current shaping for PFC operation.

side [56], as illustrated by the simulation waveforms in Fig. 2.29(b). Fig. 2.30 displays the experimental waveforms of a single diode bridge-based PFC buck circuit, comprising the buck output voltage, diode bridge output voltage, input AC current, and buck inductor current under closed-loop control. Notably, the inductor current exhibits a triangular shape, and the input AC current corresponds closely to the simulated waveform. Due to the limited resources and time, tests on the full system will be carried out in future work.

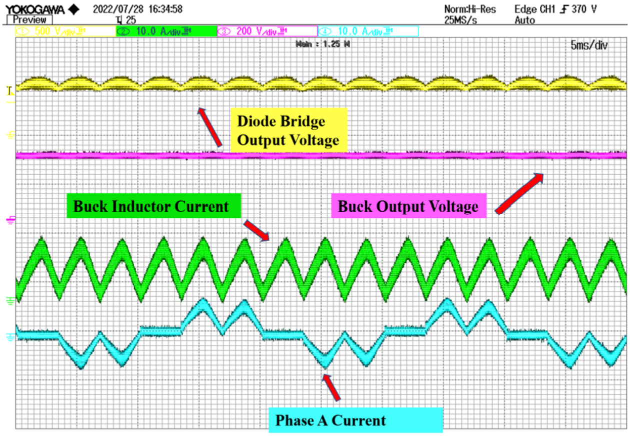


Figure 2.30: Experimental waveforms of the 12-pulse buck PFC converter under the closed loop current control (Only the upper buck PFC circuit).

2.5.2. HYBRID RECTIFIER

In the proposed unidirectional Input-Parallel-Output-Series (IPOS) three-phase hybrid rectifier illustrated in Fig. 2.31, a novel approach is introduced based on the original hybrid rectifier concept [57]. This configuration incorporates a diode bridge-based boost PFC rectifier and a T-type Vienna rectifier followed by an isolated DC-DC converter [58, 59]. The IPOS configuration is specifically designed to cater to ultra-high power ratings,

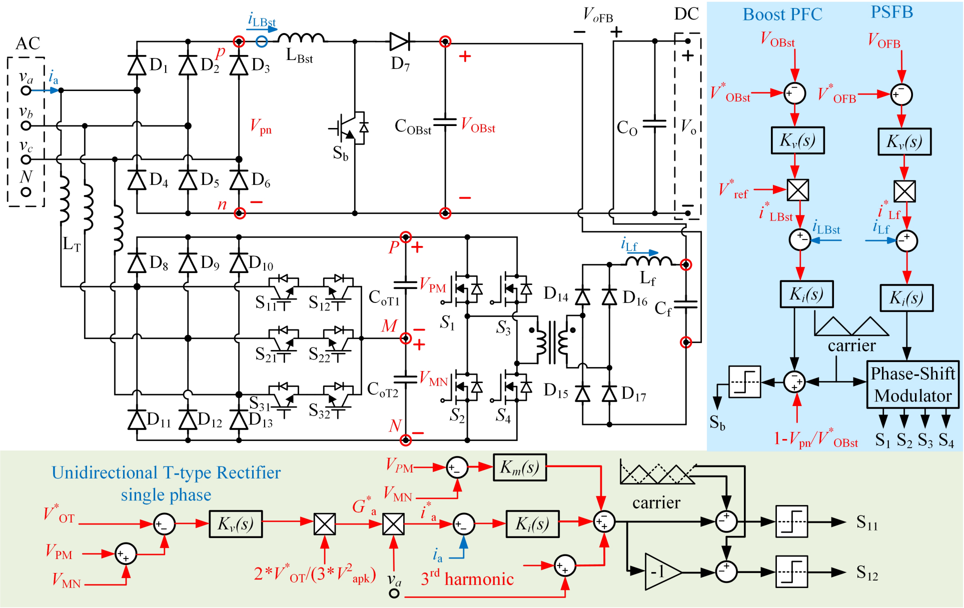

AC
v_a
i_a
v_b
v_c
N
L_T
D_1 D_2 D_3 D_4 D_5 D_6
p
n
V_{pn}
i_{LBst}
L_{Bst}
D_7
S_b
C_{OBst}
V_{OBst}
V_{oFB}
DC
C_O
V_o
D_8 D_9 D_{10} D_{11} D_{12} D_{13}
S_{11} S_{12} S_{21} S_{22} S_{31} S_{32}
P M N
C_{oT1} C_{oT2}
V_{PM} V_{MN}
S_1 S_2 S_3 S_4
D_{14} D_{15} D_{16} D_{17}
i_{Lf}
L_f
C_f
Boost PFC
PSFB
V_{OBst}
V^*_{OBst}
$K_v(s)$
V^*_{ref}
i^*_{LBst}
i_{LBst}
$K_i(s)$
carrier
S_b
$1\text{-}V_{pn}/V^*_{OBst}$
V_{OFB}
V^*_{OFB}
i^*_{Lf}
i_{Lf}
Phase-Shift Modulator
S_1 S_2 S_3 S_4
Unidirectional T-type Rectifier single phase
V^*_{OT}
V_{PM}
V_{MN}
$K_v(s)$
$2*V^*_{OT}/(3*V^2_{apk})$
G^*_a
v_a
i^*_a
i_a
$K_i(s)$
$K_m(s)$
3rd harmonic
carrier
-1
S_{11}
S_{12}

Figure 2.31: Proposed hybrid rectifier topology and the control scheme

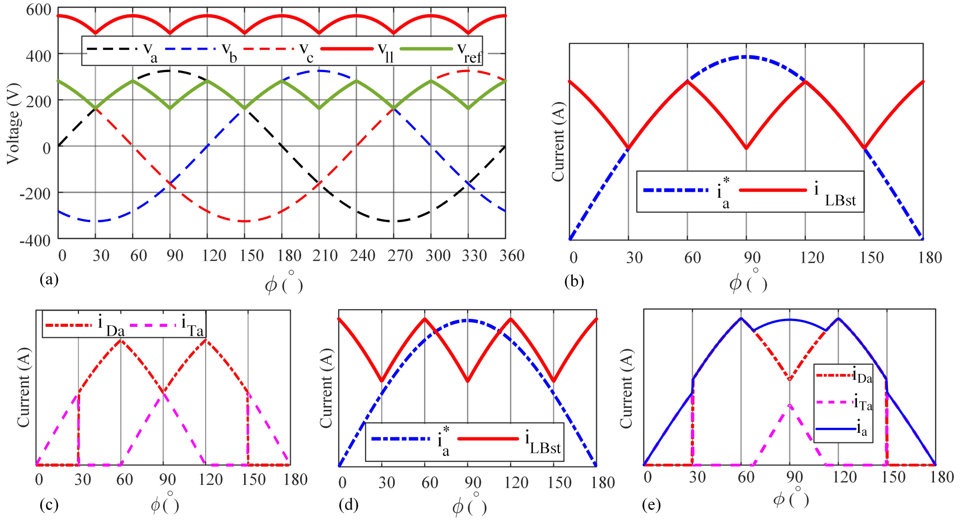


Figure 2.32: Analytical current waveforms: (a) Generation of current reference signal. (b) Mains reference current and Boost inductor current, $\alpha = \alpha_{\text{min}} = 0.23$. (c) Bridge diode current and T-type inductor current, $\alpha = \alpha_{\text{min}} = 0.23$. (d) Bridge diode current and T-type inductor current, $\alpha < \alpha_{\text{min}}$. (e) Bridge diode, mains, and T-type inductor current, $\alpha < \alpha_{\text{min}}$. Note: $\alpha = P_{o2}/P_o$ represents the percentage of power processed by the second rectifier relative to the total system power.

aiming to interface with next-generation HDEV batteries that demand a high and wide output voltage range of 800~1500 V, while utilizing commercially available 600/1200V semiconductors. Additionally, the proposed topology is characterized by its efficiency, cost-effectiveness, and scalability, while ensuring compliance with IEEE-519 standards for grid input current harmonic components through appropriate current-shaping techniques. In the grid current regulation process, the Boost PFC rectifier utilizes current feedback control. The output of the voltage compensator is multiplied by a voltage reference signal v_{ref} derived from segments of the grid voltage to generate the current reference i_{LBst}, as depicted in Fig. 2.32. Subsequently, the inductor current iLBst is sensed and compared to i^*_{LBst}, with the resulting error sent to the current compensator Ki(s). The output of $K_{\text{i}}(s)$ is augmented by a feed-forward signal, which represents the preset duty-cycle obtained from the voltage gain of a Boost converter with the three-phase diode bridge's six-pulse output voltage as the input and a reference DC-link voltage as the output. Finally, the PWM modulator generates the gate signal for the Boost switch, effectively regulating both the inductor current and the input current of the passive diode bridge.

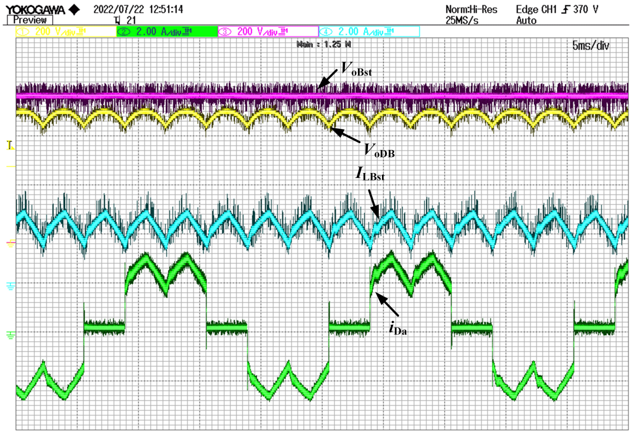


Figure 2.33: Experimental results: PFC closed-loop control

Experimental verification was conducted to validate the active PFC control implemented in the Boost PFC rectifier. The results, depicted in Fig. 2.33, demonstrate the stabilization of the DC-link voltage at its reference value. Additionally, the inductor current is shaped to match the reference waveform and align with the line voltage. These results confirm the effectiveness of the PFC control scheme in the Boost PFC rectifier, delivering desirable DC-link voltage and AC current modulation. While tests on the T-type rectifier and the integration of the IPOS system were not conducted due to resource and time constraints, they are planned for future work.

2.6. CONCLUSION

This chapter provides an overview of various power electronics topologies utilized in the front-end AC-DC PFC converters for EV chargers. Following this review, it delves into the detailed design methodologies for two specific topologies: the three-phase 3-level T-type converter and the three-phase 2-interleaved converter. Leveraging multi-objective optimization (MOO) techniques, the design process aims to strike an optimal balance between efficiency and power density, leveraging available core databases in the market. Subsequently, two 11 kW prototypes based on the three-phase 3-level T-type and 2-interleaved 2-level converters are designed, constructed, and tested. The test results reveal comparable efficiency and size between the two converter topologies, validating the effectiveness of the design methodologies employed. Finally, two PFC converter topologies utilizing a 12-pulse buck PFC converter and a hybrid rectifier are proposed for the HDEV charger. The proposed topologies are introduced along with preliminary analysis and experimental verifications.

3

VARIABLE SWITCHING FREQUENCY METHODS FOR TCM-BASED ZVS OPERATION

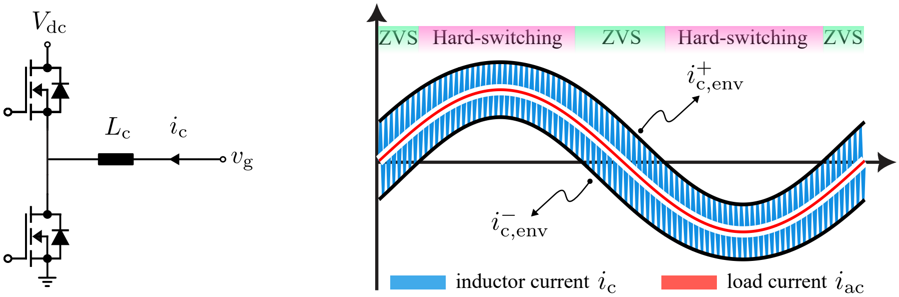
In electric vehicle charging, achieving compact, lightweight, and efficient three-phase AC-DC power factor correction (PFC) converters is essential, especially for on-board chargers (OBCs) in grid-to-vehicle (G2V) and vehicle-to-grid (V2G) scenarios. Existing OBCs exhibit limited power density despite their moderate efficiency. To enhance power density and specific power, integrated triangular current mode (iTCM) control is implemented, enabling higher switching frequencies for reduced LCL filter size without sacrificing efficiency. By incorporating an LC branch, high and low-frequency currents are split to minimize inductor losses and optimize design.

This chapter is based on the following research articles:

- Y. Wu, Z. Qin, T. B. Soeiro and P. Bauer, "Interleaved AC/DC Converter Operating with ZVS Sinusoidal Triangular-Current-Mode (S-TCM) for Reduced Voltage Harmonics Generation," 2023 IEEE Energy Conversion Congress and Exposition (ECCE), Nashville, TN, USA, 2023, pp. 161-167.
- J. Sun, Y. Wu, T. B. Soeiro, Z. Qin and P. Bauer, "ZVS Turn-on integrated Triangular Current Mode Three-phase PFC for EV On-board Chargers," 2022 IEEE 20th International Power Electronics and Motion Control Conference (PEMC), Brasov, Romania, 2022, pp. 285-294.

3.1. INTRODUCTION

The conventional three-phase 2-level PFC converter typically operates in continuous current mode (CCM) at a low switching frequency, typically around 10 kHz, resulting in relatively low efficiency. Although PFC converters utilizing GaN or SiC MOSFET switches can achieve efficiencies of up to 99% with hard-switching CCM operation [60], thermal management and cost constraints limit the maximum achievable switching frequency, thereby impacting the system's maximal achievable power density. In most commercial applications, the power density of PFC systems used in on-board chargers (OBCs) is approximately 3 kW/L, primarily due to the need for extensive filtering to meet current harmonics requirements for grid connection. The volume and weight of the AC filter often dominate the converter, sometimes accounting for over 80% of its size [61]. Consequently, PFC operation in CCM at low switching frequencies typically results in low power density (kW/L) and specific power (kW/kg). To enhance the power density and specific power of the PFC converter, increasing the switching frequency to reduce the size of the input AC filter is necessary. However, higher switching frequencies lead to increased turn-on and turn-off switching losses of semiconductors, affecting both power efficiency and thermal management. Moreover, the inductor waveform shown in Figure 3.1 reveals that under CCM operation with an increased switching frequency, the majority of switching cycles exhibit hard-switching conditions. Therefore, designing the PFC converter requires balancing efficiency with power density and specific power. At relatively high frequencies, soft turn-on switching is crucial for improving converter efficiency, as turn-on losses can account for a significant portion of the total loss, exceeding 70% in wide-bandgap (WBG) semiconductors like SiC MOSFETs [62]. Conversely, turn-off switching and conduction losses represent a smaller portion, especially for WBG devices. Moreover, with next-generation WBG devices, turn-off losses become negligible compared to turn-on losses. Thus, implementing soft turn-on switching is essential to reduce power losses and enhance overall efficiency.

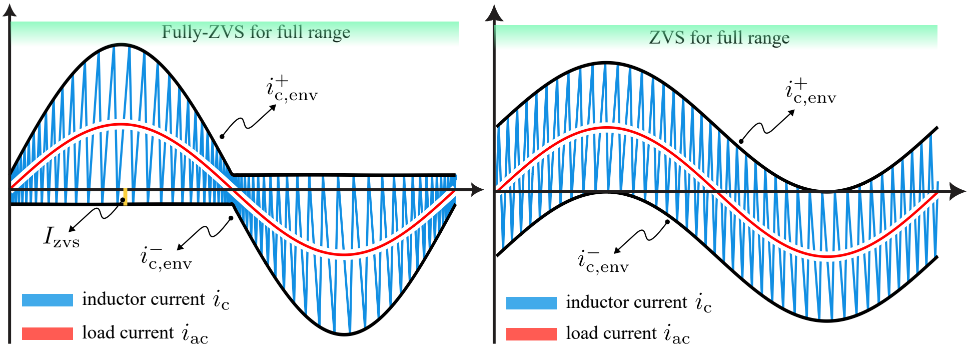


(a) A half-bridge with an inductor

(b) Inductor current waveform under CCM

Figure 3.1: Illustration of CCM in a half-bridge leg.

Various methods can achieve soft switching turn-on, but some involve adding extra components, which can increase physical complexity and potentially compromise the gain of the power density and specific power [61]. State-of-the-art control techniques, such as triangular-current-mode (TCM) control and boundary-current-mode (BCM) control, offer effective alternatives for achieving soft switching via zero-voltage-switching (ZVS) turn-on [63]. The typical TCM control methods, as shown in Fig. 3.2, operate by allowing the semiconductor current to reach a specific value in the opposite direction each switching period, causing the voltage across the parasitic capacitance to drop to zero during the resonance period. This ensures that the anti-parallel diode conducts before turning on the switch, achieving fully-ZVS turn-on. In PFC applications, the filter inductor current in TCM mode, as illustrated in Fig. 3.2, displays a significant ripple comprising both low-frequency and high-frequency components. This characteristic may result in increased losses in both the inductor and semiconductor conduction. To minimize the inductor loss and to achieve a simplified inductor design, the integrated triangular current mode (iTCM) control was first proposed in [64]. The basic idea is to split the high- and low-frequency components of the current by adding an extra LC branch between the bridge leg and DC-link. Due to the high-pass nature of the LC branch, the majority of the high-frequency current is directed through the LC branch, circulating within the PFC circuit. Meanwhile, the low-frequency current components, characterized by relatively minor ripple, traverse through the converter-side line inductor L_c to the AC grid. The current flowing through the semiconductors maintains a similar pattern to that of TCM, ensuring ZVS turn-on. However, the iTCM strategy offers advantages over TCM in terms of AC filter power density. By designing the inductor to handle low-frequency current with a powder iron core, and the high-frequency current with a ferrite core using litz wire, losses can be minimized. Another advantage is that only the low-frequency current, characterized by a small ripple, is directed to the grid, allowing for the use of a smaller input filter. Additionally, the implementation of sinusoidal pulse-width-modulation (SPWM) is simple, eliminating the need for extra wide-band current measurement devices required for accurate zero-cross detection devices. The resonance introduced by the added LC branch could lead to instability issues when integrated with the LCL input filter. Thus, specific damping measures must be implemented to ensure control stability.



(a) TCM with fixed reverse current I_{zvs} (b) TCM with fixed ripple band (STCM)

Figure 3.2: Illustration of different TCM (or BCM) control methods.

In this chapter, an iTCM-modulated three-phase grid-connected AC-DC PFC converter is proposed, and an active damping method is developed to stabilize the system. Additionally, a comparative analysis of three-phase PFC rectifiers operating with CCM, TCM, and iTCM is provided based on derived analytical modeling results. The effectiveness of various TCM operations is further validated through both simulation and experimental results.

3.2. THREE-PHASE iTCM PFC CONVERTER

3.2.1. iTCM OPERATION PRINCIPLES

The circuitry of the conventional three-phase 2-level AC-DC PFC converter for TCM control is shown in Fig. 3.3. The employed LCL harmonic filter using the virtual ground (VG) at the mid-point of the DC-link capacitors. Hence the DC midpoint and AC capacitor neutral point are connected to ensure three phases are decoupled and each phase can operate independently. Independent TCM operation for the three phases is realized by 120° phase shift of the switching frequency (f_{sw}) between phases. Simple sinusoidal PWM (SPWM) method can also be used in this topology, and it can be extended to space vector PWM (SVPWM) or third harmonic injection PWM (THIPWM).

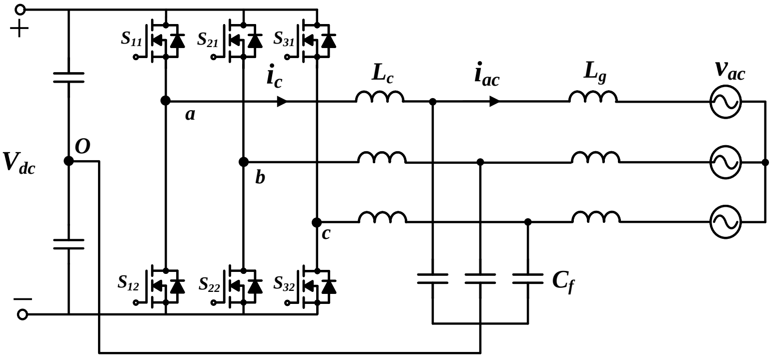


Figure 3.3: Conventional three-phase 2-level AC-DC PFC converter for TCM control.

The inductor current i_{c} flowing into the semiconductors under TCM control is a fundamental-frequency sinusoidal wave superposed with a large triangular high-frequency ripple as shown in Fig. 3.2(a). The upper and lower envelope are denoted as $i^{+}_{\mathrm{c,env}}$ and $i^{-}_{\mathrm{c,env}}$ respectively. The AC current is in phase with the AC voltage, and the three-phase AC voltages and currents can be expressed as:

$$\begin{aligned} v_{\mathrm{ac,x}}(t) &= V_{\mathrm{ac}}\sin(\omega_{\mathrm{o}}t+\theta_{\mathrm{x}}) \\ i_{\mathrm{ac,x}}(t) &= I_{\mathrm{ac}}\sin(\omega_{\mathrm{o}}t+\theta_{\mathrm{x}}+\varphi) \end{aligned} \tag{3.1}$$

where $x = a, b, c$ represents the three phases and φ is the power factor angle of the current. Besides, V_{ac} and I_{ac} are the peak value of the AC voltage and current while ω_{o} is the

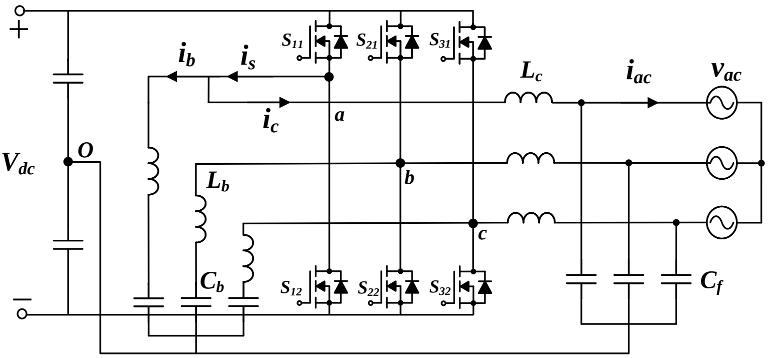


Figure 3.4: Three-phase 2-level AC-DC PFC converter with an additional LC branch for iTCM control.

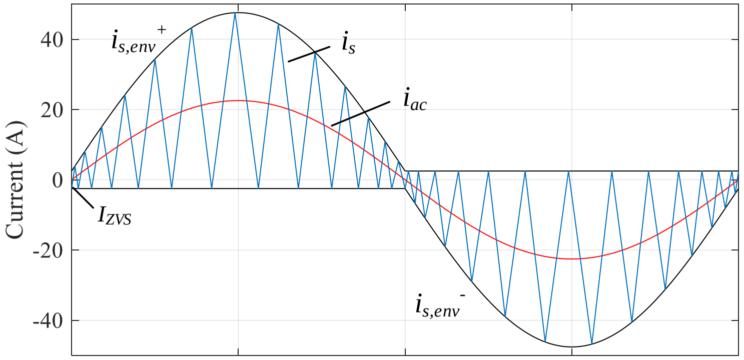
grid angular frequency. The phase angle θ_x under phase *a*, *b* and *c* are expressed as:

$$\begin{cases} \theta_\mathrm{a} = \theta_\mathrm{o} \\ \theta_\mathrm{b} = \theta_\mathrm{o} - \frac{2\pi}{3} \\ \theta_\mathrm{c} = \theta_\mathrm{o} + \frac{2\pi}{3} \end{cases} \tag{3.2}$$

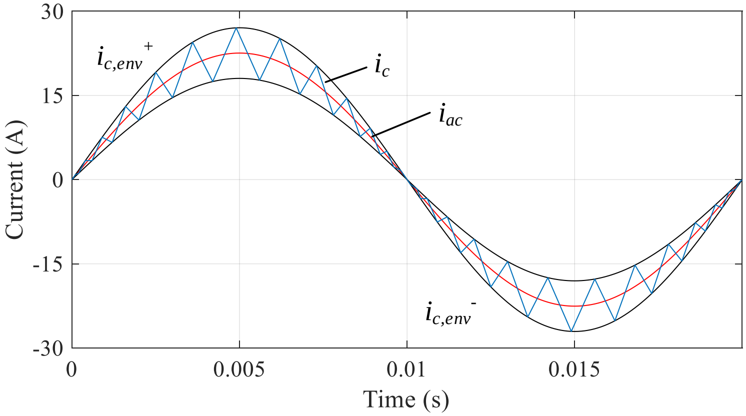
where θ_o is the initial phase of the AC voltage and can be taken as zero in this work. It should be noted that the AC voltage expressed in (3.1) only represent the modulation reference voltages under SPWM operation.

The current i_c goes to the reversal direction at a certain value and crosses the zero during each switching period, which is indicated by $|I_\mathrm{ZVS}|$. The anti-parallel diode of the semiconductor naturally conducts before the turn-on signal so that a fully-ZVS turn-on is achieved. Taking one phase switching leg as an example, when S_{11} is turned off, the resonance occurs between the two parasitic capacitances of S_{11}, S_{12} and the inductor L_c before turning on S_{12}. I_zvs is the desired turn-off current of S_{11} to fully discharge the parasitic capacitance of S_{12} so that the anti-parallel diode can conduct before turning on S_{12}.

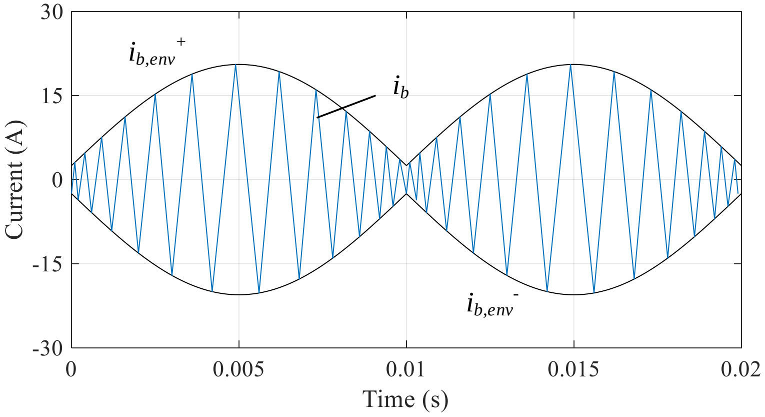
The iTCM three-phase AC-DC PFC converter topology is depicted in Fig. 3.4, where the extra integrated LC resonant branch is added between the mid-point of the switching leg and the virtual ground point. The TCM current i_s flowing into the semiconductors remains still the same as in TCM operation, as shown in Fig. 3.5(a). Under iTCM operation, the TCM current i_s is divided into two parts due to the added LC branch. The capacitance C_b in the LC branch blocks DC and low-frequency current so that most of the high-frequency current components flow into the LC branch (i_b) as shown in Fig. 3.5(c). As a result, the low-frequency current with small current ripple (i_c) flows through the converter-side inductor L_c to the grid as shown in Fig. 3.5(b). The inductance of L_c and L_b need to be properly designed to guarantee that the average value of i_c and i_b are i_ac and 0 respectively. The critical aspect of achieving ZVS turn-on is to charge the output capacitance C_oss of the switch being turned off from 0 V to V_dc and fully discharge the C_oss of the switch being turned on from V_dc to 0 V. The combined charge to be transferred from both the upper and lower half-bridge switches accounts for two output capaci-



(a) The semiconductor current i_{s}.



(b) The boost inductor current i_{c} with a small ripple.



(c) The LC branch current i_{b} with high-frequency component.

Figure 3.5: The current waveform under the iTCM control (Taking one phase and a few switching periods in one positive half main-frequency period as an illustration).

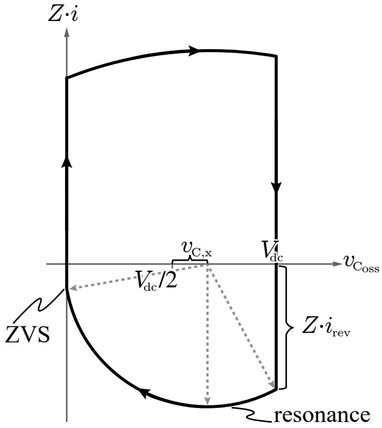


Figure 3.6: V-Zi plot of the studied three-phase system in one switching cycle featuring ZVS turn-on under rectifier mode.

tances, namely a total capacitance $2C_{\mathrm{oss}}$. Based on the V-Zi method described in [65], the ZVS resonance interval for a three-phase system is depicted in Fig. 3.6. Therefore, the minimum reverse conducting current $|I_{\mathrm{zvs}}|$ required to ensure full ZVS can be expressed by the characteristic impedance Z of the LC resonance circuit:

$$Z = \sqrt{\frac{L}{2C_{\mathrm{oss}}}} \tag{3.3}$$

where C_{oss} is the equivalent output capacitance of each half-bridge switch (assuming the identical switches in the bridge). It is important to note that the C_{oss} of the MOSFET exhibits a highly nonlinear nature, and the charge-equivalent of the output capacitance $C_{\mathrm{oss,Q}}$ should be used in the calculation. The equivalent boost inductor L under iTCM operation is calculated by:

$$L = \left(\frac{1}{L_{\mathrm{c}}} + \frac{1}{L_{\mathrm{b}}}\right) = \frac{L_{\mathrm{c}} \cdot L_{\mathrm{b}}}{L_{\mathrm{c}} + L_{\mathrm{b}}} \tag{3.4}$$

In rectifier mode, the minimum current needed to fully discharge the parasitic capacitance when the modulation index $M > 0.5$ is [66]:

$$I_{\mathrm{min}} = \frac{V_{\mathrm{dc}}}{Z} \cdot \sqrt{M} \tag{3.5}$$

where V_{dc} is the DC link voltage. The modulation index for the three-phase TCM/iTCM is expressed as:

$$M = \frac{2V_{\mathrm{ac}}}{V_{\mathrm{dc}}} \tag{3.6}$$

Generally, the switch-on and switch-off time of the one-phase bridge leg during one switching cycle can be expressed by:

$$\begin{aligned} t_{\mathrm{on,x}}(t) &= L\cdot\frac{\Delta i_{\mathrm{s,x}}(t)}{\left(\dfrac{V_{\mathrm{dc}}}{2}-v_{\mathrm{ac,x}}(t)\right)} = \frac{L_{\mathrm{c}}\cdot L_{\mathrm{b}}}{L_{\mathrm{c}}+L_{\mathrm{b}}}\cdot\frac{2\Delta i_{\mathrm{s,x}}(t)}{V_{\mathrm{dc}}(1-m_{\mathrm{x}}(t))} \\ t_{\mathrm{off,x}}(t) &= L\cdot\frac{\Delta i_{\mathrm{s,x}}(t)}{\left(\dfrac{V_{\mathrm{dc}}}{2}+v_{\mathrm{ac,x}}(t)\right)} = \frac{L_{\mathrm{c}}\cdot L_{\mathrm{b}}}{L_{\mathrm{c}}+L_{\mathrm{b}}}\cdot\frac{2\Delta i_{\mathrm{s,t}}(t)}{V_{\mathrm{dc}}(1+m_{\mathrm{x}}(t))} \end{aligned} \tag{3.7}$$

where $m_{\mathrm{x}}(t)$ has the following expression under SPWM operation:

$$m_{\mathrm{x}}(t) = \frac{2v_{\mathrm{ac,x}}(t)}{V_{\mathrm{dc}}} = M\sin(\omega_{\mathrm{o}}t+\theta_{\mathrm{x}}) \tag{3.8}$$

Consequently, the switching frequency required for the iTCM operation is expressed as:

$$f_{\mathrm{sw,x}}(t) = \frac{1}{t_{\mathrm{on,x}}(t)+t_{\mathrm{off,x}}(t)} = \frac{V_{\mathrm{dc}}(1-m_{\mathrm{x}}(t)^2)}{4\cdot\Delta i_{\mathrm{s,x}}(t)}\cdot\frac{L_{\mathrm{c}}+L_{\mathrm{b}}}{L_{\mathrm{c}}\cdot L_{\mathrm{b}}} \tag{3.9}$$

Typically for iTCM operation with fixed reverse current $I_{\mathrm{zvs}} > 0$, the envelope of the semiconductor current i_{s} has the following relations:

$$i_{s,x}(t) \geqslant 0: \quad \begin{cases} i^{+}_{\mathrm{sx,env}} = I_{\mathrm{zvs}} + 2i_{\mathrm{ac,x}}(t) \\ i^{-}_{\mathrm{sx,env}} = -I_{\mathrm{zvs}} \end{cases} \qquad 0 \leqslant \omega_{\mathrm{o}}t+\theta_{\mathrm{x}}+\varphi \leqslant \pi \tag{3.10}$$

$$i_{s,x}(t) \leqslant 0: \quad \begin{cases} i^{+}_{\mathrm{sx,env}} = I_{\mathrm{zvs}} \\ i^{-}_{\mathrm{sx,env}} = -I_{\mathrm{zvs}} + 2i_{\mathrm{ac,x}}(t) \end{cases} \qquad \pi \leqslant \omega_{\mathrm{o}}t+\theta_{\mathrm{x}}+\varphi \leqslant 2\pi \tag{3.11}$$

where (3.10) and (3.11) describe the semiconductor current envelope for the positive and negative cycles of the fundamental current $i_{\mathrm{ac,x}}$, as shown in Fig. 3.5(a). Hence the instantaneous peak-to-peak current ripple $\Delta i_{\mathrm{s,x}}$ of the SiC-MOSFET switch can be obtained by:

$$\Delta i_{\mathrm{s,x}}(t) = i^{+}_{\mathrm{sx,env}} - i^{-}_{\mathrm{sx,env}} = 2I_{\mathrm{zvs}} + 2|i_{\mathrm{ac,x}}(t)| \tag{3.12}$$

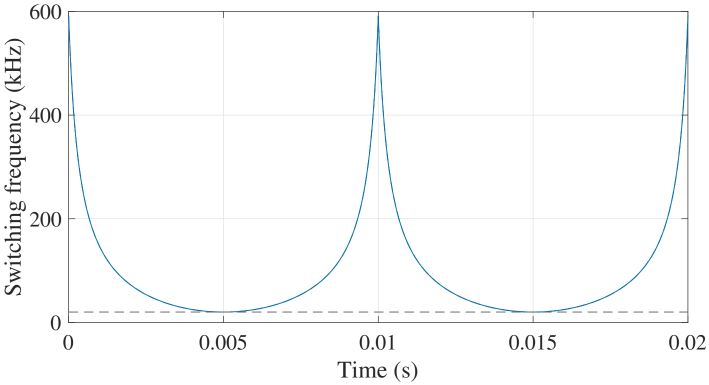
By substituting (3.12) into (3.9), the switching frequency under iTCM can be further derived as:

$$\begin{aligned} f_{\mathrm{sw,x}}(t) &= \frac{V_{\mathrm{dc}}(1-M^2\sin^2(\omega_{\mathrm{o}}t+\theta_{\mathrm{x}}))}{8(\,I_{\mathrm{zvs}}+|I_{\mathrm{ac}}\sin(\omega_{\mathrm{o}}t+\theta_{\mathrm{x}}+\varphi)|)}\cdot\frac{L_{\mathrm{c}}+L_{\mathrm{b}}}{L_{\mathrm{c}}\cdot L_{\mathrm{b}}} \\ &= \frac{V_{\mathrm{ac}}^2\,(1/M - M\sin^2(\omega_{\mathrm{o}}t+\theta_{\mathrm{x}})))}{4I_{\mathrm{zvs}}V_{\mathrm{ac}}+8P/3\,|\sin(\omega_{\mathrm{o}}t+\theta_{\mathrm{x}}+\varphi)|}\cdot\frac{L_{\mathrm{c}}+L_{\mathrm{b}}}{L_{\mathrm{c}}\cdot L_{\mathrm{b}}} \end{aligned} \tag{3.13}$$

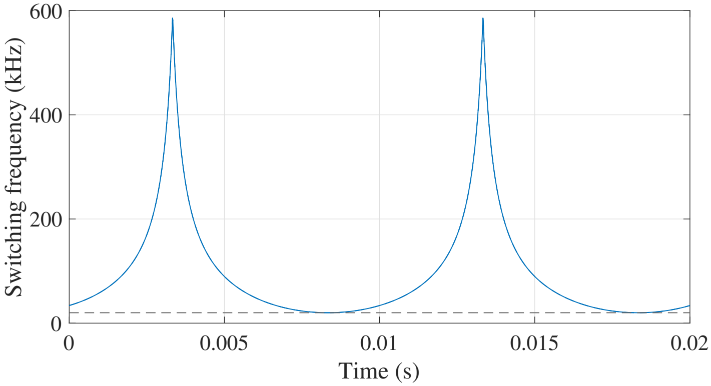
where P is the three-phase rated active power under unity power factor operation and is described by:

$$P = \frac{3}{2}V_{\mathrm{ac}}I_{\mathrm{ac}} \tag{3.14}$$

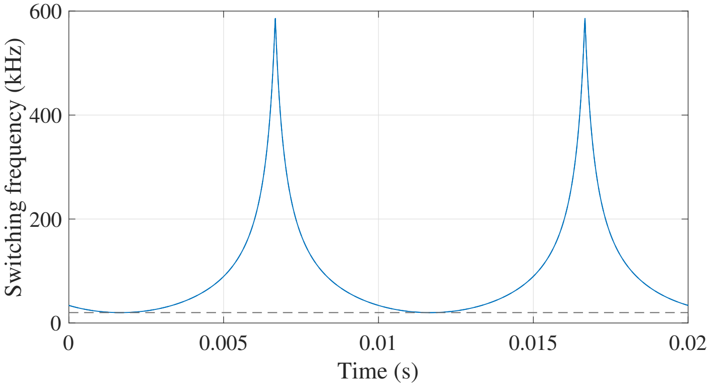
In (3.13) φ is taken as 0 for the unity power factor under PFC operation of the AC/DC converter. Therefore, the switching frequencies for the three phases are depicted in Fig. 3.7



(a) Switching frequency for phase A.



(b) Switching frequency for phase B.



(c) Switching frequency for phase C.

Figure 3.7: The switching frequency f_{sw} of the three-phase iTCM control with a 120° phase shift.

based on (3.13) with the parameters listed in Table 3.2.For both iTCM and TCM, the switching frequency (f_{sw}) presents a periodic profile to achieve a constant reverse current I_{zvs}. For SPWM operation, the minimal and maximal switching frequencies occur at the peak and zero value of $i_{\mathrm{ac,x}}$ and hence can be calculated as:

$$\begin{aligned} f_{\mathrm{sw,min}} &= \frac{V_{\mathrm{dc}}(1-M^2)}{8(\,I_{\mathrm{zvs}}+I_{\mathrm{ac}})}) \cdot \frac{L_{\mathrm{c}}+L_{\mathrm{b}}}{L_{\mathrm{c}}\cdot L_{\mathrm{b}}} \\ f_{\mathrm{sw,max}} &= \frac{V_{\mathrm{dc}}}{8I_{\mathrm{zvs}}} \cdot \frac{L_{\mathrm{c}}+L_{\mathrm{b}}}{L_{\mathrm{c}}\cdot L_{\mathrm{b}}}. \end{aligned} \tag{3.15}$$

The minimum operating switching frequency $f_{\mathrm{sw,min}}$ could be limited to avoid an operation in the range of audible noise. Therefore, $f_{\mathrm{sw,min}}$ could be used to define the maximum values of L, while considering the rated power of the system.

3.2.2. PARAMETER DESIGN FOR PASSIVE COMPONENTS

The current envelopes of the converter-side inductor L_{c}, i.e., $i^{+}_{\mathrm{c,env}}$ and $i^{-}_{\mathrm{c,env}}$, are calculated by:

$$\begin{aligned} i^{+}_{\mathrm{cx,env}}(t) &= i_{\mathrm{ac,x}}(t) + \frac{1}{2}\Delta i_{\mathrm{c,x}}(t) \\ i^{-}_{\mathrm{cx,env}}(t) &= i_{\mathrm{ac,x}}(t) - \frac{1}{2}\Delta i_{\mathrm{c,x}}(t). \end{aligned} \tag{3.16}$$

Therefore, the instantaneous peak-to-peak current ripple $\Delta i_{\mathrm{c,x}}(t)$ is subsequently obtained in (3.17).

$$\Delta i_{\mathrm{c,x}}(t) = \frac{\left(\frac{V_{\mathrm{dc}}}{2} - v_{\mathrm{ac,x}}(t)\right)}{L_{\mathrm{c}}} \cdot t_{\mathrm{on,x}}(t) = \frac{L_{\mathrm{b}}}{L_{\mathrm{c}}+L_{\mathrm{b}}} \cdot \Delta i_{\mathrm{s,x}}(t). \tag{3.17}$$

The current envelopes of L_{b}, i.e., $i^{+}_{\mathrm{bx,env}}$ and $i^{-}_{\mathrm{bx,env}}$, can be also derived in the similar way as expressed by (3.18). Meanwhile the instantaneous peak-to-peak current ripple $\Delta i_{\mathrm{b,x}}(t)$ can be calculated as in (3.19).

$$\begin{aligned} i^{+}_{\mathrm{bx,env}}(t) &= \frac{1}{2}\Delta i_{\mathrm{c,x}}(t) \\ i^{-}_{\mathrm{bx,env}}(t) &= -\frac{1}{2}\Delta i_{\mathrm{c,x}}(t) \end{aligned} \tag{3.18}$$

$$\Delta i_{\mathrm{b,x}}(t) = \frac{\left(\frac{V_{\mathrm{dc}}}{2} - v_{\mathrm{ac,x}}(t)\right)}{L_{\mathrm{b}}} \cdot t_{\mathrm{on,x}}(t) = \frac{L_{\mathrm{c}}}{L_{\mathrm{c}}+L_{\mathrm{b}}} \cdot \Delta i_{\mathrm{s,x}}(t). \tag{3.19}$$

It is noteworthy from (3.17) and (3.19) that the distribution of the inductor current ripples are determined by the values of both L_{c} and L_{b}. To better design the inductance of L_{c} and L_{b}, a design parameter r is introduced and defined as the ratio of the maximum peak-to-peak current ripple allowed for $i_{\mathrm{c,x}}$ ($\Delta i_{\mathrm{cx,max}}$) to the peak AC current on the grid side [67]:

$$r = \Delta i_{\mathrm{cx,max}} / I_{\mathrm{ac}}. \tag{3.20}$$

The factor r becomes a user-design choice that can be utilized to determine the inductance value of L_c. The coefficient r can be selected from 0 to 200%. When r is approximately 200%, the control scheme becomes equivalent to the TCM control, resulting in $L_b >> L_c$. Conversely, when r is approximately 0%, the value of L_c becomes significantly larger than L_b. The optimal value of r depends on the specific design metric being optimized. By incorporating (3.17) into (3.9), one can have:

$$L_c = \frac{V_{dc}(1 - m_x(t)^2)}{4\Delta i_{c,x}(t) \cdot f_{sw,x}(t)} \tag{3.21}$$

As discussed earlier, the minimum switching frequency and highest maximum peak-to-peak current ripple are obtained when $m_{x,t}$ reaches its peak value. Hence, the maximum converter-side inductance L_c can be derived by the following relation:

$$L_c = \frac{V_{dc}(1 - M^2)}{4(\underbrace{I_{ac} \cdot r}_{\Delta i_{cx,max}}) \cdot f_{sw,min}}. \tag{3.22}$$

Similarly, the maximum inductance L_b value is obtained by combining (3.9), (3.12), (3.17), (3.20) and (3.21) together, as expressed by (3.23).

$$L_b = \frac{V_{dc}(1 - M^2)}{4 f_{sw,min}(2|I_{zvs}| + 2I_{ac} - I_{ac} \cdot r)} \tag{3.23}$$

The grid-side inductance L_g is designed to meet the current harmonics standard, such as IEEE 519 - 2014 [68]. The odd harmonics limit is shown in Table 3.1. The even harmonics $I_{IEEE519,even}$ are limited to 1/4 of the odd harmonics. For the harmonics order greater than 50, it is limited to 0.3% and 0.075% of the fundamental current for odd and even harmonics in this work for simplicity. The attenuation of the LCL filter is:

$$\begin{aligned} \text{Att}(\omega) &= \frac{1}{L_T} \cdot \frac{\omega_{res}^2}{\omega \left| \omega^2 - \omega_{res}^2 \right|} \\ L_T &= L_c + L_g \end{aligned} \tag{3.24}$$

where ω_{res} is the resonance frequency of the LCL filter and is expressed as:

$$\omega_{res} = \sqrt{\frac{L_c + L_g}{L_c L_g C_f}} \tag{3.25}$$

The total inductance of the LCL filter L_T has to attenuate the critical current harmonic below the standard current limit $I_{IEEE519}$.

$$L_{T-req} = \frac{\omega_{res}^2 V_{crit}}{\omega_{crit} \left| \omega_{crit}^2 - \omega_{res}^2 \right| I_{IEEE519}} \tag{3.26}$$

where V_{crit} is the critical voltage harmonic of the converter output voltage v_c and ω_{crit} is the critical frequency. Then the grid-side inductance L_g can be determined by:

$$L_g \geqslant L_{T-req} - L_c \tag{3.27}$$

Table 3.1: Individual current odd harmonic limits for 120V - 69kV, $I_{\text{SC}}/I_{\text{L}} < 20$ system (IEEE 519 - 2014)

$I_{\text{SC}}/I_{\text{L}}$	Harmonics values are in % of maximum current I_{max}					TDD
	$3 \leq h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h \leq 50$	
<20	4.0	2.0	1.5	0.6	0.3	5.0

As a constraint for the LCL filter design, the maximum AC filter capacitance (i.e. the sum of C_{f} and C_{b}) is limited by the maximum allowable reactive power consumed by the converter. Hence, the filter capacitance should satisfy:

$$C_{\text{f}} + C_{\text{b}} < q \cdot \frac{S_{\text{N}}}{3\omega_{\text{o}} V_{\text{ac}}^2}. \tag{3.28}$$

where S_{N} is the rated power of the converter and q is reactive power ratio and selected to be 5% in this chapter. The capacitor C_{b} needs to be well-designed to block the DC and low-frequency current so that most of the high-frequency component flows into the LC branch as expected. First of all, it will draw some reactive power at low frequency and reduce the total power factor so that the value of C_{b} should be small. Moreover, C_{b} should be large enough to keep the resonance frequency of the LC branch smaller than the switching frequency f_{sw} to get an inductive behaviour, which is a necessity to achieve ZVS turn-on [64]. The LC resonant frequency $\omega_{\text{LC,res}}$ is chosen as 47000 rad/s in this chapter, and hence the value of C_{b} can be determined by

$$\omega_{\text{LC,res}} = \frac{1}{\sqrt{L_{\text{b}} C_{\text{b}}}} < \omega_{\text{min}} \tag{3.29}$$

where $\omega_{\text{min}} = 2\pi f_{\text{min}}$. Then C_{b} can subsequently be obtained by (3.28). Based on the above design guideline for the LCL filter and LC branch, key circuit parameters for both the simulations and the experiments in later sections are obtained as listed in Table 3.2.

3.3. FREQUENCY-LIMITED TCM METHODS

The switching frequency f_{sw} based on (3.15) varies from 20 kHz to 591.48 kHz. Such a large frequency variation poses some challenges to the practical implementation as well as to the design of the EMI filter. Basically, there are two common approaches to limiting the maximum switching frequency under TCM operation.

3.3.1. BOUNDED TCM (BTCM) OPERATION

First of all, the switching frequency may be constrained to a maximum value. While this ensures ZVS turn-on, the reverse current no longer remains constant at $|I_{\text{zvs}}|$. Consequently, a larger peak-to-peak current ripple occurs near the current zero-crossing point, leading to increased turn-off current compared to the scenario without switching frequency limitation. Given the relatively low turn-off loss of WBG semiconductors and the naturally smaller switched current near the zero-crossing of the phase current, this

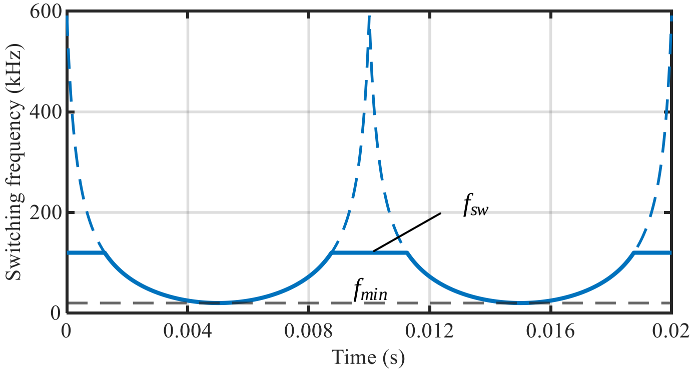


Figure 3.8: The switching frequency f_{sw} with a maximum 120 kHz limitation (the solid line) of the BTCM control

trade-off is deemed acceptable. By means of Bounded-iTCM control, the maximum allowed switching frequency is limited to 120 kHz ($f_{\max}$ = 120 kHz) as the solid line shown in Fig. 3.8. Thus, the switching frequency f_{sw} becomes:

$$f_{\mathrm{sw,x}}(t) = \begin{cases} f_{\max} \cdot \beta & \text{if} \quad \beta < 1 \\ f_{\max} & \text{if} \quad \beta \geq 1 \end{cases} \tag{3.30}$$

where β is the ratio between f_{sw} and $f_{\min}$, expressed as:

$$\beta = \frac{f_{\mathrm{sw,x}}(t)}{f_{\max}} = \frac{1}{f_{\max}} \cdot \frac{V_{\mathrm{dc}}(1 - M^2 \sin^2(\omega_{\mathrm{o}} t + \theta_{\mathrm{x}}))}{8(\, I_{\mathrm{zvs}} + |I_{\mathrm{ac}} \sin(\omega_{\mathrm{o}} t + \theta_{\mathrm{x}} + \varphi)|)} \cdot \frac{L_{\mathrm{c}} + L_{\mathrm{b}}}{L_{\mathrm{c}} \cdot L_{\mathrm{b}}} \tag{3.31}$$

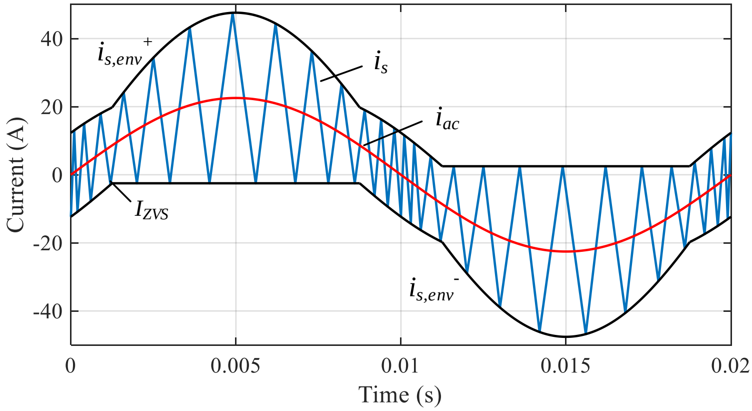
The ripple of $i_{\mathrm{s}}(t)$ becomes:

$$\Delta i_{\mathrm{s}}(t) = \begin{cases} 2I_{\mathrm{zvs}} + 2\hat{i}_{\mathrm{ac}} |\sin(\omega t + \theta_{\mathrm{x}} + \varphi)| & \text{if} \quad \beta < 1 \\ (2I_{\mathrm{zvs}} + 2\hat{i}_{\mathrm{ac}} |\sin(\omega t + \theta_{\mathrm{x}} + \varphi)|) \cdot \beta & \text{if} \quad \beta \geq 1 \end{cases} \tag{3.32}$$

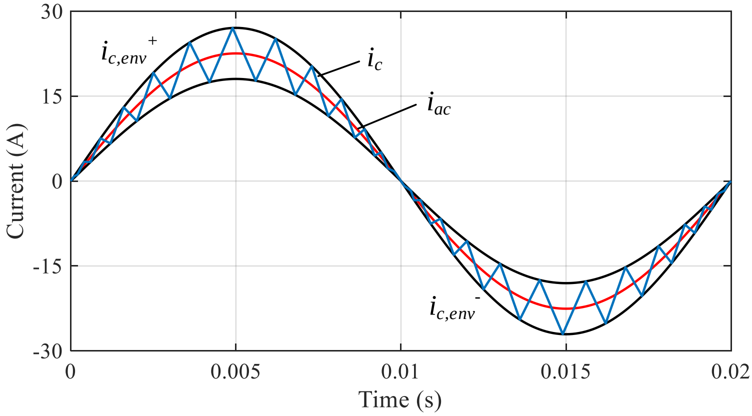
Under the Bounded-iTCM control, ZVS turn-on is still achieved, but the reverse current is not constant due to the frequency limitation, as the i_{s} waveform shown in Fig. 3.9(a). This causes a larger current ripple, a larger turn-off current, and a higher turn-off loss compared to the case without frequency limitation. Since the turn-off loss of the WBG semiconductors is much smaller than the turn-on loss, and due to the fact the switched current is naturally smaller and close to the zero-crossing of the phase current, the trade-off is acceptable. With the switching frequency limitation, the current i_{c} and i_{b} are shown in Fig. 3.9. This Bounded-iTCM control is the simplest and most straightforward way to limit the maximum switching frequency.

3.3.2. SINUSOIDAL TCM (STCM) OPERATION

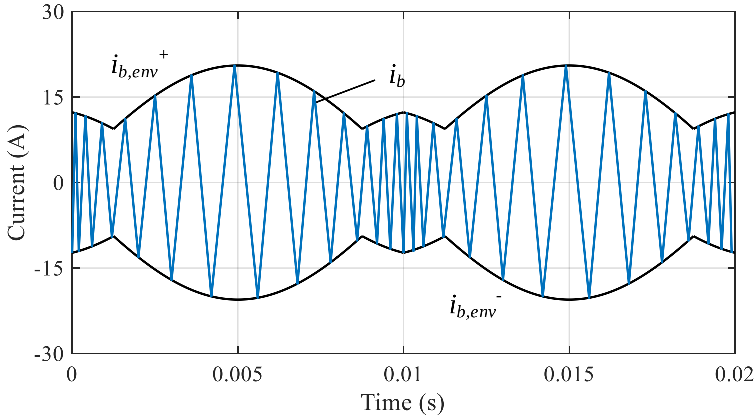
The sinusoidal-TCM (STCM)control was introduced in [8,63] to limit the maximum switching frequency while maintaining ZVS turn-on. The idea is to create a constant current



(a) The semiconductor current i_s



(b) The boost inductor current i_c with a small ripple



(c) The LC branch current i_b with high-frequency component

Figure 3.9: The current waveform of the Bounded-iTCM control with a maximum 120 kHz switching frequency limitation (Taking one phase and a few switching periods in one positive half main-frequency period as illustration).

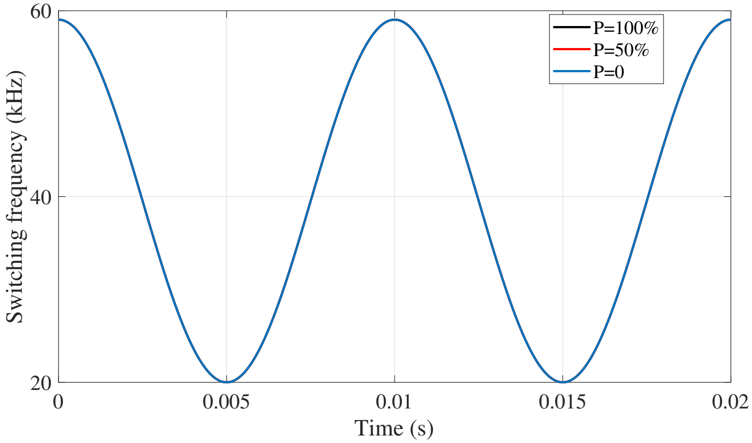


Figure 3.10: The switching frequency f_{sw} of the STCM control

ripple band for the semiconductor current $i_s(t)$ instead of the expression (3.12):

$$\Delta i_s(t) = 2I_{zvs} + 2I_{ac} \tag{3.33}$$

Substituting (3.33) into (3.9), the switching frequency of STCM is expressed as:

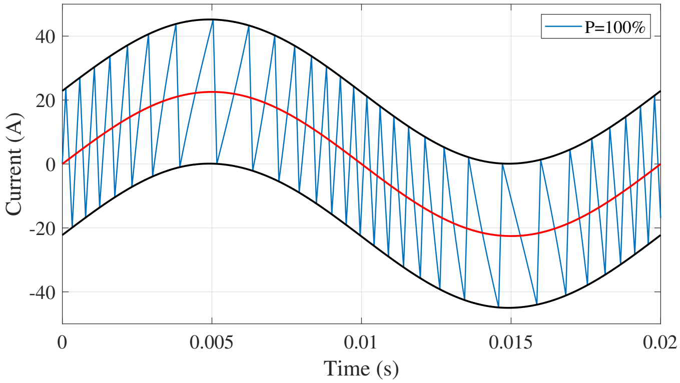
$$\begin{aligned} f_{sw,x}(t) &= \frac{V_{dc}(1 - M^2 \sin^2(\omega_o t + \theta_x))}{8(I_{zvs} + I_{ac})} \cdot \frac{L_c + L_b}{L_c \cdot L_b} \\ &= \frac{L_c + L_b}{L_c \cdot L_b} \cdot \frac{V_{dc}(2 - M^2)}{16(I_{zvs} + I_{ac})} + \frac{L_c + L_b}{L_c \cdot L_b} \cdot \frac{V_{dc}(M^2)}{16(I_{zvs} + I_{ac})} \cos(2\omega_o t + 2\theta_x) \\ &= f_{sw0} + f_{swb} \cos(2\omega_o t + 2\theta_x). \end{aligned} \tag{3.34}$$

From (3.34), the waveform of the switching frequency $f_{sw,x}$ (as depicted in Fig. 3.10) under STCM operation is a constant frequency f_{sw0} superposed with a sinusoidal variation band f_{swb} at the twice fundamental frequency. The semiconductor current i_s under the STCM control are shown in Fig. 3.11 under different load power. It can be seen that the current ripple of the Sinusoidal-iTCM control is larger than the BTCM control in general, which will cause higher switching loss and conduction loss. However, the biggest advantage of the STCM control is that the current band and the switching frequency maintains the same at different load conditions, which means it can handle various charging power without adjustment. In the Bounded-iTCM control, the switching frequency should be adjusted when the EV battery is charging at a different power level. Besides, the frequency of STCM is simpler to calculate and implement in the digital control system.

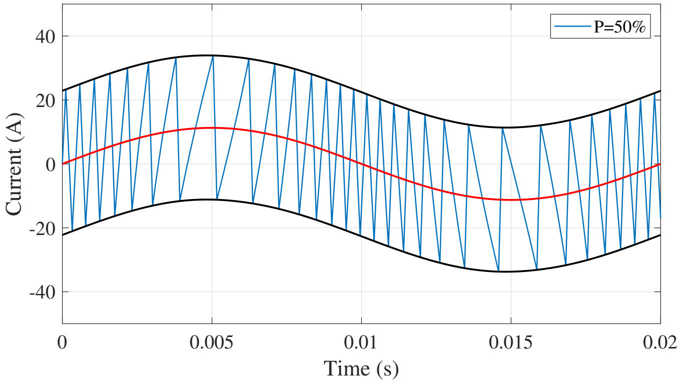
3.4. ANALYTICAL MODELING OF CURRENT STRESSES

The maximum voltage stress across the semiconductors swicthes ($v_{S,max}$) is defined by the maximum DC-link voltage ($V_{dc,max}$):

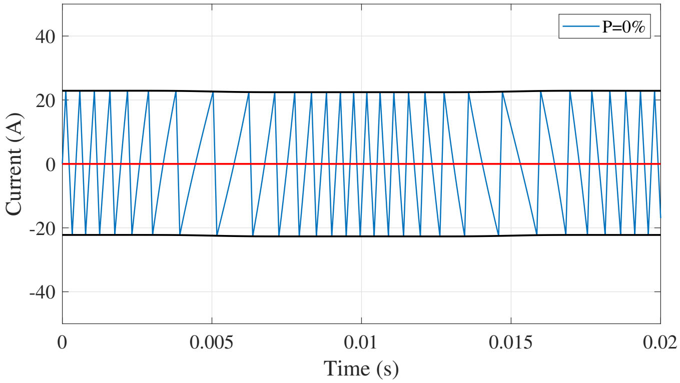
$$v_{S,max} = V_{dc,max}. \tag{3.35}$$



(a) i_s under full load condition P=100%.



(b) i_s under part load condition P=50%.



(c) i_s under zero load condition P=0%.

Figure 3.11: The semiconductor current i_s waveform of the STCM control (Taking one-phase and a few switching periods in one positive half main-frequency period as illustration).

Table 3.2: System Specifications and Key Circuit Parameters

PARAMETER	**SYMBOL**	**VALUE**
RMS AC Phase Voltage	v_{ac}	230 V
Mains Frequency	f_0	50 Hz
DC Voltage	V_{dc}	800 V
Modulation Index	M	0.813
Nominal Output Power	P_{o}	3.174 kW
Reverse Current Reference	$\lvert I_{\mathrm{zvs}}\rvert$	1.5 A
Grid-Side Inductance	L_{g}	325.5 μH
Converter-Side Inductance	L_{c}	325.5 μH
LC Branch Inductance	L_{b}	325.5 μH
LCL Filter Capacitance	C_{f}	1.4 μF
LC Branch Capacitance	C_{b}	1.4 μF
Current Sharing Coefficient	r	1.24

For iTCM operation, the instantaneous RMS current $i_{\mathrm{yx,rms}}(t)$ during each switching period flowing through several circuit components within the phase x can be calculated by (3.36), where the index y represents different circuit components, such as the half-bridge's AC terminal ($i_{\mathrm{sx,rms}}(t)$ with y=s), and the inductors L_{c} ($i_{\mathrm{cx,rms}}(t)$ with y=c) and L_{b} ($i_{\mathrm{bx,rms}}(t)$ with y=b).

$$i^2_{\mathrm{yx,rms}}(t) = \frac{1}{3}\left[i^{+}_{\mathrm{yx,env}}(t)^2 + i^{+}_{\mathrm{yx,env}}(t)\cdot i^{-}_{\mathrm{yx,env}}(t) + i^{-}_{\mathrm{yx,env}}(t)^2 \right]. \tag{3.36}$$

Since the switching periods are negligibly small as compared to the grid period, (3.36) can reasonably be viewed as a continuous function and the total RMS value of a certain components y for phase x over one grid cycle, which is denoted as $I_{\mathrm{y,rms}}$, can be calculated by taking the RMS value of the integral of (3.36) over one grid cycle.

Based on (3.10), (3.11), and (3.36), the RMS value of the semiconductor current $I_{\mathrm{s,rms}}$ can be derived as

$$I_{\mathrm{s,rms}} = \sqrt{\frac{1}{3}\left(2I^2_{\mathrm{ac}} + \frac{4}{\pi}\ I_{\mathrm{ac}}\ I_{\mathrm{zvs}} + I^2_{\mathrm{zvs}}\right)}. \tag{3.37}$$

Subsequently, the RMS current of a single MOSFET switch $I_{\mathrm{sw,rms}}$ can be calculated as in (3.38) due to the symmetrical operation of the upper and lower phase legs over one grid cycle.

$$I_{\mathrm{sw,rms}} = \frac{I_{\mathrm{s,rms}}}{\sqrt{2}}. \tag{3.38}$$

Defining a current-dividing coefficient k as in (3.39), which represents the proportion of $\Delta i_{\mathrm{s,x}}$ that flows through L_{c}, based on (3.12), (3.16), (3.36), and (3.39), the RMS current of L_c (denoted as $I_\mathrm{c,rms}$) can be derived as in (3.40).

$$k = \frac{L_\mathrm{b}}{L_\mathrm{c}+L_\mathrm{b}} = \frac{\Delta i_\mathrm{c,x}}{\Delta i_\mathrm{s,x}} = \frac{\Delta i_\mathrm{s,x}-\Delta i_\mathrm{b,x}}{\Delta i_\mathrm{s,x}} \tag{3.39}$$

$$I_\mathrm{c,rms} = \sqrt{\frac{1}{3}\left(\frac{3+k^2}{2}\, I_\mathrm{ac}^2 + \frac{4\,k^2}{\pi}\, I_\mathrm{ac}\, I_\mathrm{zvs} + k^2\, I_\mathrm{zvs}^2\right)} \tag{3.40}$$

Based on (3.12), (3.18), (3.36), and (3.39), the RMS current of L_b (denoted as $I_\mathrm{b,rms}$) can be derived as

$$I_\mathrm{b,rms} = \sqrt{\frac{(1-k)^2}{3}\left(\frac{1}{2}\, I_\mathrm{ac}^2 + \frac{4}{\pi}\, I_\mathrm{ac}\, I_\mathrm{zvs} + I_\mathrm{zvs}^2\right)}. \tag{3.41}$$

Ideally, it is assumed that the current ripple $\Delta i_\mathrm{c,x}$ is fully absorbed by the LCL filter capacitor C_f. Therefore, the current envelopes of C_f, denoted as $i^+_\mathrm{Cfx,env}$ and $i^-_\mathrm{Cfx,env}$, are given as in (3.42). Based on (3.12), (3.36), (3.39) and (3.42), the RMS current of the LCL filter capacitors C_f, denoted as $I_\mathrm{cf,rms}$, can be derived as in (3.43). By a similar reasoning, the RMS current of the LC branch capacitors C_b, denoted as $I_\mathrm{Cb,rms}$, is equal to $I_\mathrm{b,rms}$ as shown in in (3.44).

$$\begin{cases} i^+_\mathrm{Cfx,env} = \frac{1}{2}\Delta i_\mathrm{c,x}(t) \\ i^-_\mathrm{Cfx,env} = -\frac{1}{2}\Delta i_\mathrm{c,x}(t) \end{cases} \tag{3.42}$$

$$I_\mathrm{Cf,rms} = \sqrt{\frac{k^2}{3}\left(\frac{1}{2}\, I_\mathrm{ac}^2 + \frac{4}{\pi}\, I_\mathrm{ac}\, I_\mathrm{zvs} + I_\mathrm{zvs}^2\right)} \tag{3.43}$$

$$I_\mathrm{Cb,rms} = I_\mathrm{b,rms} = \sqrt{\frac{(1-k)^2}{3}\left(\frac{1}{2}\, I_\mathrm{ac}^2 + \frac{4}{\pi}\, I_\mathrm{ac}\, I_\mathrm{zvs} + I_\mathrm{zvs}^2\right)} \tag{3.44}$$

The precision of the above component stress model is verified by the simulation results obtained in PLECS. The simulation model operates in inverter mode and system specifications are listed in Table 3.2. The calculated current stress based on the aforementioned model is compared with the simulation results in Table 3.3, showing a good accuracy of the model.

Table 3.3: Comparison of Analytical Current Stress Models and Simulation Results

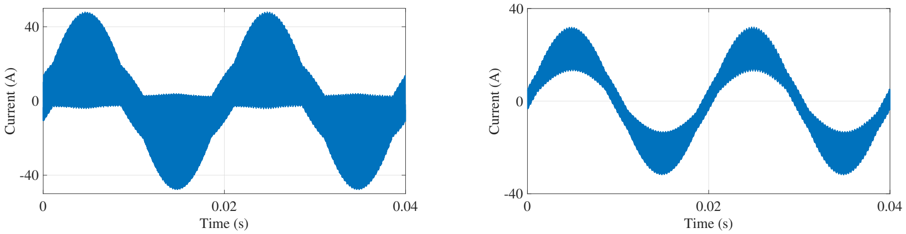
Variable	Model-Based Calculation	Simulation	Deviation (%)
$I_\mathrm{s,rms}$	5.756 A	5.822 A	-1.13
$I_\mathrm{sw,rms}$	4.070 A	4.109 A	-0.949
$I_\mathrm{c,rms}$	4.914 A	4.932 A	-0.365
$I_\mathrm{b,rms}$	1.729 A	1.788 A	-3.30
$I_\mathrm{Cf,rms}$	0.864 A	0.907 A	-4.74
$I_\mathrm{Cb,rms}$	0.864 A	0.894 A	-3.36

3.5. SIMULATION AND EXPERIMENTAL VERIFICATION

3.5.1. SIMULATION RESULTS

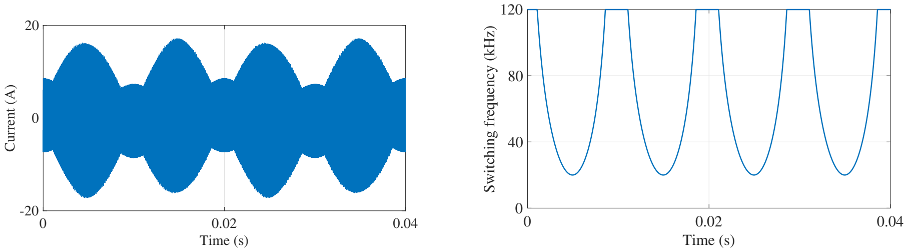
The simulation is conducted to verify the idea of the iTCM control via PLECS. The parameters used for the simulation are for the 11 kW PFC system. In the following simulation, the simplest Bounded-iTCM control is used. The minimum switching frequency is preset to be 20 kHz, while the maximum switching frequency is limited by 120kHz due to the practical constraint and EMI issues. The aforementioned parameter r is selected as 0.4 just as an example. By choosing this r value, the equivalent boost inductance L that needed for ZVS can be calculated as 67.62 μH. Specifically SPWM method is adopted in this work for both analytical modeling and simulation. Both the Bounded-iTCM control and the Sinusoidal- iTCM control are verified in the simulation.

The simulation results of the aforementioned Bounded-iTCM control are shown in Fig. 3.12 and 3.13. Fig. 3.12(a), 3.12(b) and 3.12(c) show the semiconductor current i_s, the converter-side current i_c and the LC branch current i_b, respectively. The semiconductor current i_sm is split into a low-frequency component i_c, and a high-frequency component i_b due to the added LC branch. The low-frequency current satisfies the input power and the high frequency current flows through the LC branch, which stays within the circuit by the midpoint. The additional inductor L_b is well-designed so that the high-frequency current is split correctly. Fig. 3.12(d) shows the switching frequency of the Bounded-iTCM control. The switching frequency is limited to 120 kHz.



(a) The semiconductor current i_s.

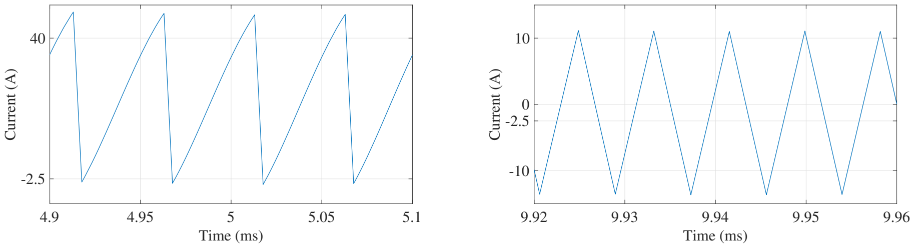
(b) The converter-side current i_c.



(c) The LC branch current i_b.

(d) The switching frequency of the Bounded-iTCM control.

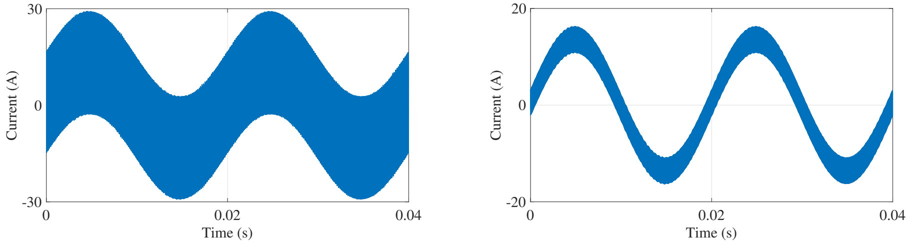
Figure 3.12: The simulation results for the Bounded-iTCM control with a maximum 120 kHz switching frequency limitation.



(a) Several switching cycles illustration of the constant reversal current region.

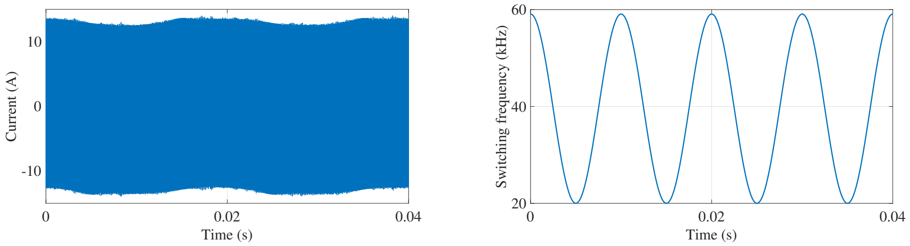
(b) Several switching cycles illustration of the limited-frequency region.

Figure 3.13: The zoom-in simulation waveform of the semiconductor current i_s under Bounded-iTCM control with a maximum 120 kHz switching frequency limitation.



(a) The semiconductor current i_s

(b) The converter-side current i_c



(c) The LC branch current i_b

(d) The switching frequency of the Sinusoidal-iTCM control.

Figure 3.14: The simulation results of current waveform of the Sinusoidal-iTCM control.

Fig. 3.13(a) shows several switching cycles of the semiconductor current i_s. It can be seen that ZVS turn-on is achieved since the semiconductor current is reversed to -2.5 A at each switching period. However, in the limited frequency region, the reversal current goes even larger, as shown in Fig. 3.13(b). ZVS is still achieved in this region but the larger reversal current scarifies the efficiency because of the larger turn-off current and the higher RMS current.

The simulation results of the aforementioned Sinusoidal-iTCM control are shown in Fig. 3.14. Fig. 3.14(a), 3.14(b) and 3.14(c) show the semiconductor current i_s, the converter-side current i_c and the LC branch current i_b, respectively. The semiconductor current i_s is split into a low-frequency component i_c and a high-frequency component i_b. The current ripple remains constant in the Sinusoidal-iTCM control, which is much larger than the ripple in the Bounded-iTCM control. ZVS turn-on is achieved in the main cycle, but the efficiency would be lower than the Bounded-iTCM control.

Fig. 3.14(d) shows the switching frequency of the Sinusoidal-iTCM control. As discussed earlier, the switching frequency is calculated by 3.34. The switching frequency remains constant across different load conditions, resulting in uniform semiconductor current ripple $\Delta i_\mathrm{s,x}$ regardless of the load.

3.5.2. EXPERIMENTAL RESULTS

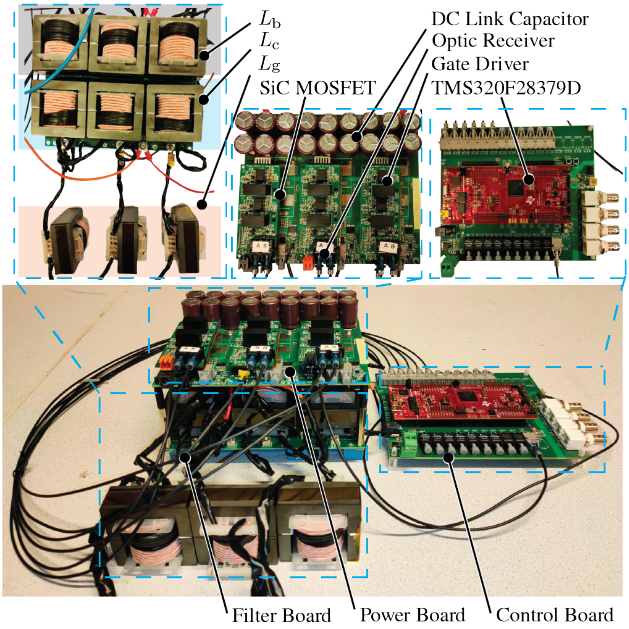


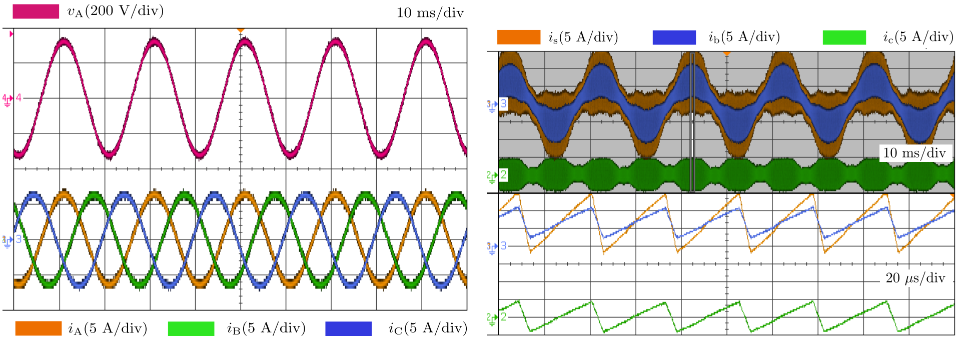
Figure 3.15: Experimental setup for the three-phase iTCM PFC converter.

A 3-kW prototype as shown in Fig. 3.15 is built to verify the feasibility of the studied three-phase three-wire iTCM-operated 2-level converter system shown in Fig. 3.3. During the experiments, the three-phase VSC is operated in inverter mode with the system specifications and key circuit parameters listed in Table 3.2. Table 3.4 lists the design details for the inductors. It is noteworthy that L_c, L_g and L_b adopt the same inductor design with identical parameters. The voltage and current waveforms are captured by the KEYSIGHT InfiniiVision DSOX3024A oscilloscope, and the efficiency of the converter system is measured by the YOKOGAWA WT5000 power analyzer. Fig. 3.16 shows the experimental results with circuit topology in Fig. 3.3 being used. Fig. 3.16(a) shows the output of three phase currents and phase-to-neutral voltage of phase A that have sinu-

Table 3.4: Design specifications of the inductor L_c, L_g and L_b

PARAMETER	**VALUE**
Inductance	325.5 μH
Core Material	N87
Core Dimension	’55/28/21’
Core Shape	EE
Number of Stacks	1
Number of Turns N	28
Coil Length l	2.2 m
Number of Winding Layers k	3
Window Height h	33.4 mm
Airgap Length l_g	1.27 mm
Core Volume V_c	43900 mm^3
Coeff. α	1.7236
Coeff. β	2.7422
Coeff. k	0.07865

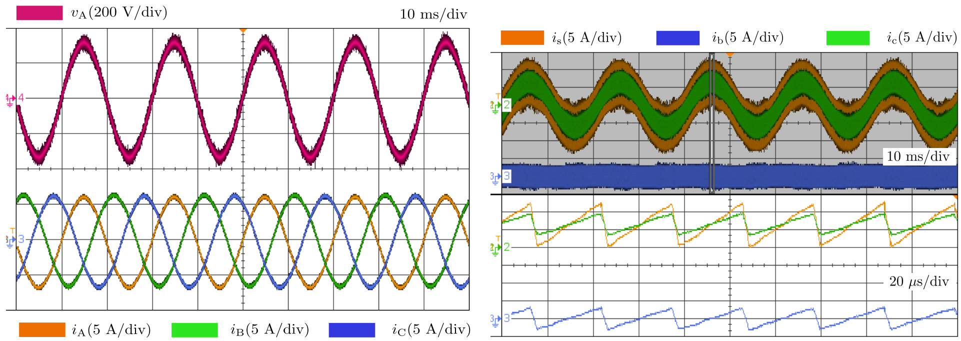
soidal shapes under the Bounded-iTCM control. Fig. 3.16(b) shows the waveform of the semiconductor current i_s, the L_c current i_c and the LC branch current i_b for phase A. It is observed that i_s adopts a triangular shape and in each switching cycle reverses its polarity, where ZVS is achieved. Note that for practical reasons, the maximum switch-



(a) Three-phase output currents i_A, i_B, i_C, and phase-to-neutral voltage of phase A v_A.

(b) Zoomed-in waveform of semiconductor current i_s, L_c current i_c, and LC branch current i_b for phase A.

Figure 3.16: Experimental results of the proposed three-phase three-wire iTCM PFC converter under the Bounded-iTCM control.



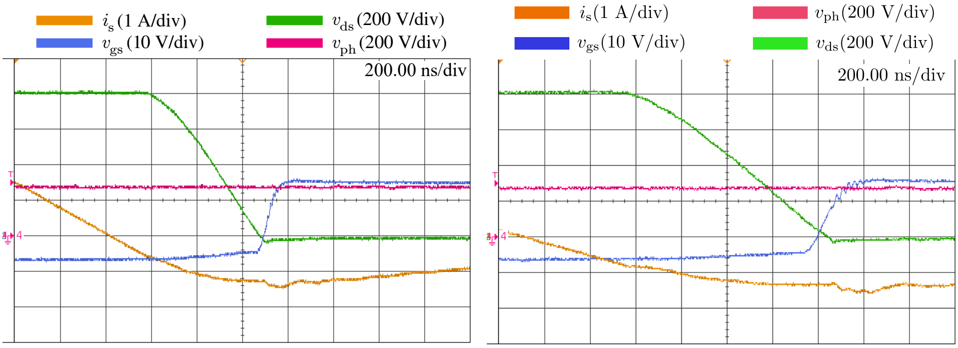
(a) Three-phase output currents i_{A}, i_{B}, i_{C}, and phase-to-neutral voltage of phase A v_{A}.

(b) Zoomed-in waveform of semiconductor current i_{s}, L_{c} current i_{c}, and LC branch current i_{b} for phase A.

Figure 3.17: Experimental results of the proposed three-phase three-wire iTCM PFC converter under the Sinusoidal-iTCM control.

ing frequency $f_{\mathrm{sw,max}}$ is clamped to 120 kHz. Therefore, it can be seen that the current envelopes of i_{s} is slightly enlarged around the zero-crossing region. Moreover, it can be seen that L_{c} and L_{b} are well-designed so that the ripple in i_{s} is approximately equally shared by L_{c} and L_{b}. Similarly, Fig. 3.17(a) shows the waveforms of three-phase currents and phase-to-neutral voltage of phase A under the Sinusoidal-iTCM control. Fig. 3.17(b) presents the waveform of the semiconductor current i_{s}, the L_{c} current i_{c} and the LC branch current i_{b} for phase A. It is observed that i_{s} also adopts the triangular shape and in each switching cycle reverses its polarity, where ZVS is achieved. The semiconductor ripple $\Delta i_{\mathrm{s,x}}$ has a nearly constant band which corresponds to the associated switching frequency design. Since L_{c} and L_{b} share the identical design, i_{s} is also equally shared by L_{c} and L_{b} under the Sinusoidal-iTCM control.

Fig. 3.18 shows the detailed ZVS turn-on process for the upper leg during the positive half mains cycle under both the Bounded-iTCM and Sinusoidal-iTCM control operations. It can be seen that the gate signal v_{gs} applies only after the drain-to-source voltage v_{ds} has fallen to zero, meaning the full-ZVS turn-on is achieved for both cases. During ZVS turn-on, i_{s} steadily discharges the output capacitor of the MOSFETs. Fig. 3.19 shows the comparison between the Bounded-iTCM (cf. Fig. 3.2(a) and the Sinusoidal-iTCM (cf. Fig. 3.2(b) on the measured power conversion efficiency of the studied system for a wide range of output power. For both cases, the full-ZVS turn-on is ensured. Moreover, in Fig. 3.19 the efficiency of the iTCM operation is compared against the conventional continuous current mode (CCM) operation (cf. Fig. 3.1(b), that has a fixed switching frequency equal to the average of that for the iTCM operation and does suffer hard-switching for a considerable operating range. As it can be seen, the measured efficiency for both iTCM operations is higher than that for the CCM operation within the whole range of output power. Further, a substantial improvement in the efficiency for the whole range of output power is observed with the Sinusoidal-iTCM as compared to the Bounded-iTCM during the partial load condition. Specifically, the measured efficiencies at full-load are 97.57% and 97.51% for the the Bounded-iTCM and Sinusoidal-



(a) Bounded-iTCM control

(b) Sinusoidal-iTCM control

Figure 3.18: Zoomed-in waveform of the gate-to-source voltage v_{gs}, the drain-to-source voltage v_{ds}, the semiconductor current i_s, and the phase voltage v_{ph} during the turn-on process for the upper switching leg of phase A.

iTCM cases, higher than the peak efficiency of 97.12% under CCM operation. The difference between the two operations lies not only in the condution losses but also the turn-off switching losses. The swicthing frequencies for both cases are designed for the full power operation with the same system parameters and the Sinusoidal-TCM naturally has a slightly smaller average switching frequency. Hence, the turn-off losses under the Sinusoidal-TCM operation is compensated by the smaller effective switching frequency as compared to the Bounded-iTCM operation. This explains the higher efficiency under the Sinusoidal-iTCM operation.

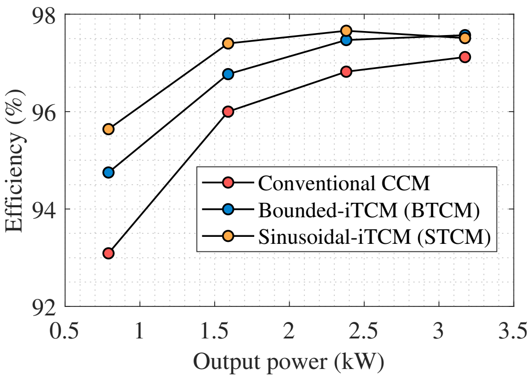


Figure 3.19: Measured power conversion efficiency of the iTCM-operated three-phase three-wire VSC system at different output power with the conventional and the capacitor-split VG connections, as compared to that of the traditional CCM-operated system

3.6. CONCLUSION

The iTCM control method applied to a three-phase AC-DC PFC converter has been proposed in this chapter. ZVS operation in the iTCM strategy eliminates the turn-on switching loss but slight increases the turn-off switching and conduction losses. The inductor loss in iTCM is minimized due to the added LC branch, while the grid-side current ripple is highly reduced compared to the conventional TCM control.

By analytical modeling and simulation, iTCM is proven more efficient, highly compact and lightweight than TCM and CCM at the same effective or average switching frequency. Specifically, the frequency-limited TCM such as the Bounded-iTCM and the Sinusoidal-iTCM are adopted for practical implementation.

In the experiment, both iTCM methods are used and validated. At the full load power, the two iTCM control methods achieves an efficiency of 97.57% and 97.51%, which are higher than the CCM's efficiency (97.12%) at the equivalent switching frequency. Assuming the power density and the specific power are the same, the proposed iTCM control highly improves the system efficiency by 0.45%. Thus, to improve the power density and the specific power, the iTCM control is weighing more effective than increasing the switching frequency of CCM.

4

SUPRA-HARMONICS MODELLING OF PWM CONVERTER

In recent years, significant research and adoption of periodic variable switching frequency PWM (P-VSFPWM) have been observed in AC/DC voltage source converters (VSCs). This technique aims to reduce ripple in AC inductor current and DC capacitor voltage, suppress injected current harmonic amplitudes for EMC compliance, and minimize switching losses. However, the presence of overlapped harmonic spectra from different switching harmonic bands can lead to heightened harmonic magnitudes due to the wide frequency variation, necessitating additional filtering measures. Surprisingly, there is a notable absence of harmonic spectra analysis under P-VSFPWM, despite the growing concern over supra-harmonics (2-150 kHz) emission injected into the grid from the electric vehicle (EV) chargers. To address this gap, this chapter proposes the interleaved P-VSFPWM to mitigate harmonics overlap without deviating from the intended purpose of P-VSFPWM. A fast-acquisition supra-harmonics model under arbitrary P-VSFPWM has been proposed based on vectorization, facilitating the subsequent filter design process.

This chapter is based on the following research articles:

- Y. Wu, J. Xu, T. B. Soeiro, M. Stecca and P. Bauer, "Optimal Periodic Variable Switching PWM for Harmonic Performance Enhancement in Grid-Connected Voltage Source Converters," *in IEEE Transactions on Power Electronics*, vol. 37, no. 6, pp. 7247-7262, June 2022.
- Y. Wu, J. Xu, T. B. Soeiro, P. Bauer and Z. Qin, "Frequency Design of Three-phase Active Front-End Converter with Reduced Filter in EV Chargers," *in IEEE Transactions on Transportation Electrification*, doi: 10.1109/TTE.2024.3381167.

4.1. INTRODUCTION

Enhancing power and gravimetric density holds significant importance for the application of electric-vehicle (EV) battery chargers [69–73]. Pulse-width-modulation (PWM) based voltage source converters (VSCs) are preferably employed as the active front-end (AFE) AC/DC converters in the two-stage EV chargers illustrated in Fig. 4.1, because of their robustness and simplicity [74]. Compared to constant switching frequency PWM (CSFPWM), Variable switching frequency PWM (VSFPWM) is commonly utilized in the Active Front-End (AFE) converter of on-board EV chargers to achieve higher power density. It has been particularly used in AC/DC PWM-based VSCs for diverse applications and purposes such as switching loss minimization [2–5], zero-voltage-switching (ZVS) [6–9], ripple reduction of the converter such as the inductor current and DC-link capacitor voltage [10–13] and improvement of the conducted electromagnetic interfer-

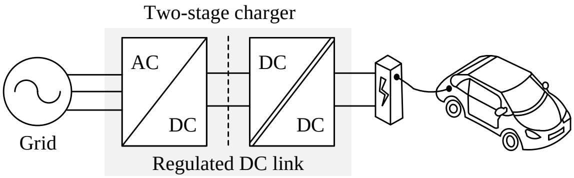


Figure 4.1: Diagram of a typical two-stage EV charger with a three-phase AC/DC PFC rectifier as the front-end and an isolated DC/DC converter

Table 4.1: Summary of the switching frequency profiles from the studied literature [2–21].

Reference	Circuit Type	Switching Frequency Profile						3-Φ* adoption	Purpose of use
		f_c (kHz)	$\Delta f_c/f_{c0}$*	f_m/f_o	$\theta_{k=1}$ (°)	Periodic	Sinusoid		
[2]	3-Φ AC	1.6–12	0.765	2	270	Yes	Yes	No	Switching Loss Optimization
[3]	3-Φ AC	5–15	0.5	2	90	Yes	No	No	
[4]	1-Φ AC	16.7–90	0.687	2	0	Yes	No	No	
[5]	1-Φ AC	2.5–10	0.6	2	270	Yes	No	No	
[6]	3-Φ AC	100–174	0.27	3	90	Yes	No	Yes	Zero-Voltage-Switching (ZVS)
[7]	3-Φ AC	100–146	0.187	3	90	Yes	No	Yes	
[8]	3-Φ AC	48–140	0.49	2	270	Yes	Yes	No	
[9]	1-Φ AC	35–75	0.36	2	90	Yes	No	No	
[10]	1-Φ AC	8–24	0.5	6	90	Yes	No	No	Current Ripple Reduction
[11]	3-Φ AC	6–10	0.25	6	270	Yes	No	Yes	
[12]	3-Φ AC	6–10	0.25	6	90	Yes	Yes	Yes	Voltage Ripple Reduction
[13]	3-Φ AC	6–10	0.25	6	270	Yes	No	Yes	
[14]	DC	75–105	0.167	-	-	Yes	Yes	-	Electromagnetic-Interference (EMI) Improvement
[15]	DC	30–166	0.69	-	-	Yes	No	-	
[16]	DC	108–132	0.1	-	-	Yes	Yes	-	
[17]	DC	140–260	0.3	-	-	Yes	No	-	
[18]	DC	52–148	0.48	-	-	Yes	Yes	-	
[19]	DC	140–260	0.3	-	-	Yes	No	-	
[20]	1-Φ AC	9–11	0.1	2	0	Yes	No	No	
[21]	3-Φ AC	25–50	0.333	6	270	Yes	No	Yes	

* Δf_c refers to the peak deviation of the switching frequency with regard to the centered frequency f_{c0}.

* 3-Φ adoption refers to the three phases of the converter implementing exactly the same frequency profile. 'No' can typically mean that the three phases adopt the switching frequency profile with the same shape but different phase shifts.

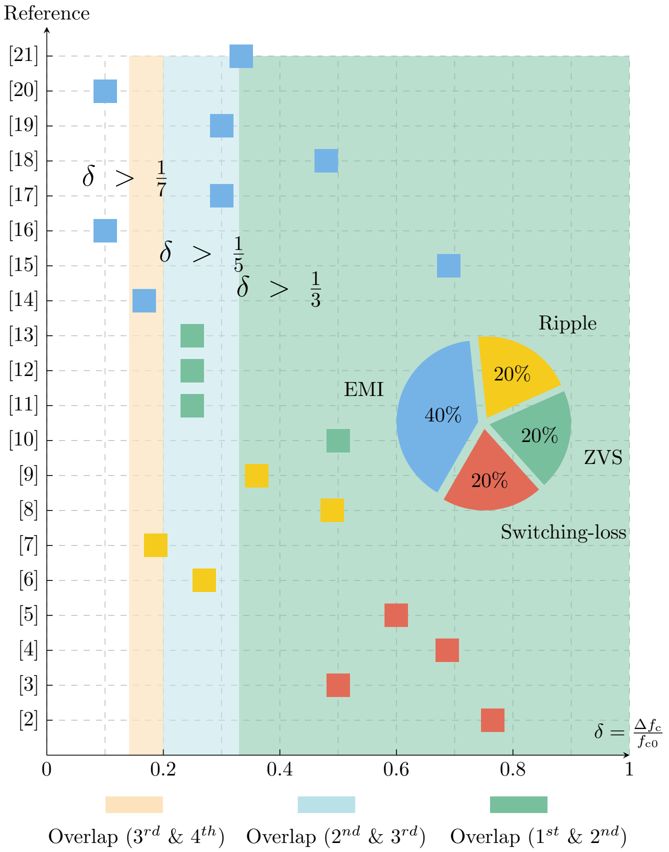


Figure 4.2: The frequency variation coefficient $\delta = \Delta f_c / f_{c0}$ of the studied literature [2–21]: The Overlap of the side-band harmonics of the different carrier-frequency harmonics can be indicated by δ value based on Carson's rule [18].

ence (EMI) [14–21]. Table 4.1 summarizes the information of the implemented VSF-PWM methods from the aforementioned studied literature works. Among all the VSF-PWM methods, the periodicity was exhibited in the variable switching frequency profile. It is important to note that frequency profiles predominantly cluster within the supra-harmonics range (2-150 kHz). In recent studies, supra-harmonics have been reported to significant impact on low-voltage distribution grids during the EV charging process because of the high switching frequency for PWM [27, 28, 30]. This range has gained significant attention from the international standard-setting community due to recent efforts to restrict emissions. EV chargers can potentially introduce supra-harmonic distortions into the power grid, as switching frequencies within this range are frequently employed to achieve efficient and cost-effective power converter designs. This is especially pronounced in the case of on-board chargers, where considerations such as weight and size further drive the adoption of switching frequencies within the supra-harmonic range [29, 30].

More importantly, these periodic VSFPWM (P-VSFPWM) methods also feature a widespread spectrum caused by the wide frequency variation setting Δf_c. The spectrum width of each carrier-frequency harmonic band can be estimated by Carson's rule [18]. Therein, the parameter $\delta = \Delta f_c / f_{c0}$ has been used to quantify the overlap between the different carrier-frequency harmonics bands, as presented in Fig. 4.2. It can be found that the most published VSFPWM methods, unfortunately, result in the overlap between 1st and 2nd harmonic band spectra, which might lead to an increased harmonic peak as depicted in Fig. 4.3. As a result, more filtering efforts are required to comply with the harmonic emission standards in the concerned frequency range. In [14–19], the frequency profile can be designed with restricted frequency variation to avoid the spectra overlap to some extent while trading off the performance of EMI reduction. Besides harmonic spectra overlap, there is also a lack of harmonic spectral analysis for power electronics converters implementing the variable switching frequency at present. The spectra model of a single sinusoidal harmonic modulated by the sinusoidal frequency profile has been given and verified by [75] more than a decade ago. Prior to that, [18] has already analytically derived the output harmonics spectra under the sinusoidal switching frequency profile based on the PWM in a DC/DC converter. However, the derived model is simple in description but difficult for practical use due to the use of the impulse function (Dirac Delta function). In [20], the output harmonic spectra under P-VSFPWM in a single-phase full-bridge converter were investigated and the spectra model has been derived with the description of triple Fourier series. Unfortunately, the derived model is only applicable to the sinusoidal switching frequency profile. Hence, it is unable to deal with the harmonics generated by the rapidly emerging P-VSFPWM applications since the most frequency profiles are non-sinusoidal as indicated by Table 4.1. In [22], the harmonic spectra model under arbitrary P-VSFPWM profiles has been derived based on the triple Fourier summation form for the conventional three-phase two-level converter. However, the proposed algorithm to calculate the harmonic spectra is time-costly and not

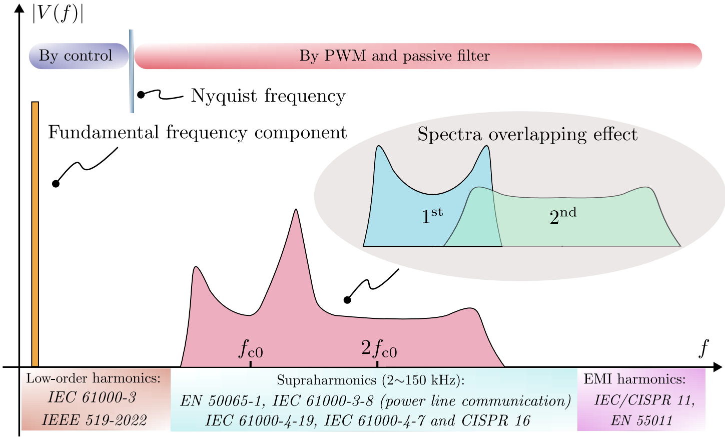

$|V(f)|$
By control
By PWM and passive filter
Nyquist frequency
Fundamental frequency component
Spectra overlapping effect
1^{st}
2^{nd}
f_{c0}
$2f_{c0}$
f
Low-order harmonics:
IEC 61000-3
IEEE 519-2022
Supraharmonics (2~150 kHz):
EN 50065-1, IEC 61000-3-8 (power line communication)
IEC 61000-4-19, IEC 61000-4-7 and CISPR 16
EMI harmonics:
IEC/CISPR 11,
EN 55011

Figure 4.3: Spectra overlap in the supra-harmonics range due to VSFPWM operations.

straightforward for practice since it involves significant times of partition and iterations.

In this chapter, firstly a generic harmonic spectra model under arbitrary periodic variable switching frequency has been analytically derived. Besides, an algorithm based on vectorization has been proposed for fast acquisition of the harmonic spectra. Finally, the accuracy and effectiveness of the proposed harmonic spectra model are verified by both the simulation and experiment results.

4.2. HARMONICS MODEL FOR CONSTANT SWITCHING FREQUENCY

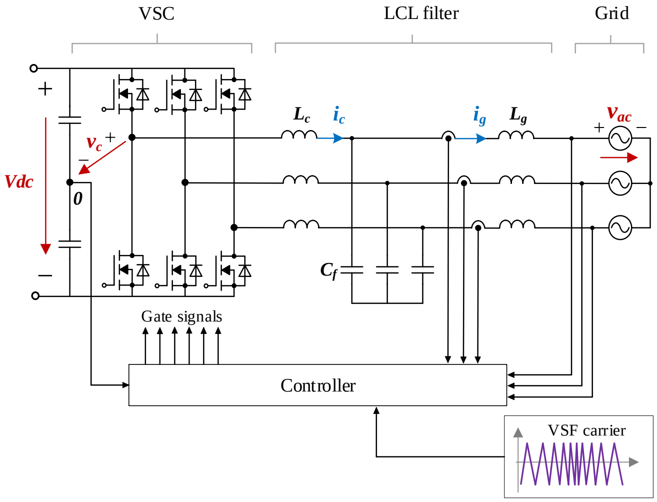


Figure 4.4: Grid-tied VSC with LCL filter adopting VSFPWM.

To simplify the analysis and model derivations, the sinusoidal-PWM (SPWM) is presented in this section. These mathematical derivations built based on the SPWM can be extended to other continuous PWM methods, e.g., THIPWM and SVPWM [50, 76, 77], which are preferably implemented in practical systems because of their higher DC bus voltage utilization. As depicted in Fig. 4.4, the converter output phase voltage v_c of the three-phase two-level converter is determined by the switching states of the semiconductor devices, which are directed by the intersections between the sinusoidal reference and triangular carrier signals, as illustrated in Fig. 4.5. According to the double Fourier analysis (DFA) [50], the output phase voltage $V_c(x, y)$ is the function of two independent variables as expressed by (4.1). In (4.1), m and n are multiples of the carrier and reference signal frequencies while A_{mn} and B_{mn} are the resultant coefficients of the DFA. The first term A_{00} shown in (4.1) represents the DC offset, which is zero for the converter circuit shown in Fig. 4.4. The first summation term is the base-band harmonic components. Numerous approaches have been explored to mitigate base-band harmonic distortion, which is typically a concern due to its impact on the low-frequency harmonic emissions to the grid [78, 79]. The second summation term represents the carrier harmonic components, while the last one represents the side-band harmonic components, which primarily contribute to the supra-harmonics.

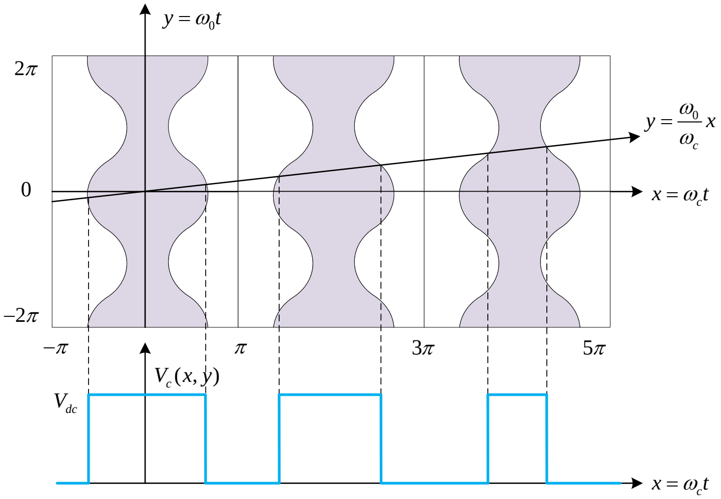


Figure 4.5: Triangular carrier-based CSFPWM (natural sampling).

$$v_c(x,y)=\frac{A_{00}}{2}+\underbrace{\sum_{n=1}^{\infty}(A_{0n}\cos ny+B_{0n}\sin ny)}_{\text{Fundemental Component \& Baseband Harmonics}}+\underbrace{\sum_{m=1}^{\infty}(A_{m0}\cos mx+B_{m0}\sin mx)}_{\text{Carrier Harmonics}}$$
$$+\underbrace{\sum_{m=1}^{\infty}\sum_{\substack{n=-\infty\\ n\neq 0}}^{\infty}[A_{mn}\cos(mx+ny)+B_{mn}sin(mx+ny)]}_{\text{Sideband Harmonics}} \tag{4.1}$$

According to the double Fourier analysis (DFA) [50], the output voltage $v_c(x,y)$ of one bridge leg from the PWM converter depicted in Fig. 4.4 is the function of two independent variables:

$$v_{\mathrm{c}}(t)=\Re\Big(\sum_{m=0}^{\infty}\sum_{n=-\infty}^{\infty}C_{\mathrm{mn}}\cdot e^{\mathrm{j(mx+ny)}}\Big). \tag{4.2}$$

The two variables x and y represent the phases of the carrier and reference signals under the constant carrier frequency modulation respectively, which are expressed as:

$$\begin{cases} x(t)=\omega_c t+\theta_c \\ y(t)=\omega_o t+\theta_o \end{cases} \tag{4.3}$$

where ω_c and ω_o are the angular frequencies for the carrier and reference signals (switching and fundamental frequencies) respectively, and θ_c and θ_o are the phases for the carrier and reference signals. The complex-form coefficients are derived by using the double-integral:

$$
\begin{aligned}
C_{\mathrm{mn}} &= A_{\mathrm{mn}} + jB_{\mathrm{mn}} \\
&= \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} v_c(x,y)e^{j(mx+ny)}\mathrm{d}x\mathrm{d}y
\end{aligned}
\tag{4.4}
$$

Hence the VSC output voltage with CSFPWM under the symmetrical regular sampling can be generally expressed as (4.5) in the time domain:

$$
\begin{aligned}
v_{\mathrm{c}}(t) =& \frac{2V_{\mathrm{dc}}}{\pi}\sum_{n=1}^{\infty}\frac{J_{\mathrm{n}}(n\frac{\omega_{\mathrm{o}}}{\omega_{\mathrm{c}}}\frac{\pi}{2}M)}{(n\frac{\omega_{\mathrm{o}}}{\omega_{\mathrm{c}}})}\sin[n(1+\frac{\omega_{\mathrm{o}}}{\omega_{\mathrm{c}}})\frac{\pi}{2}]\cos n(\omega_{\mathrm{o}}t+\theta_{\mathrm{o}})+ \\
& \frac{2V_{\mathrm{dc}}}{\pi}\sum_{m=1}^{\infty}\frac{J_0(m\frac{\pi}{2}M)}{m}\sin(m\frac{\pi}{2})\cos[m(\omega_{\mathrm{c}}t+\theta_{\mathrm{c}})]+ \\
& \frac{2V_{\mathrm{dc}}}{\pi}\sum_{m=1}^{\infty}\sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty}\frac{J_{\mathrm{n}}[(m+n\frac{\omega_{\mathrm{o}}}{\omega_{\mathrm{c}}})\frac{\pi M}{2}]}{m+n\frac{\omega_{\mathrm{o}}}{\omega_{\mathrm{c}}}}\sin[(m+n\frac{\omega_{\mathrm{o}}}{\omega_{\mathrm{c}}}+n)\frac{\pi}{2}]\cos[m(\omega_{\mathrm{c}}t+\theta_{\mathrm{c}})+n(\omega_{\mathrm{o}}t+\theta_{\mathrm{o}})].
\end{aligned}
\tag{4.5}
$$

Therein $J_{\mathrm{n}}(x)$ is the Bessel function of the first kind, and M is the modulation depth. M is defined as $2V_{\mathrm{ac}}/V_{\mathrm{dc}}$ and V_{ac} and V_{dc} are the magnitude of the AC phase voltage and DC bus voltage respectively [50].

4.3. HARMONICS MODEL FOR PERIODIC VARIABLE SWITCHING FREQUENCY

4.3.1. GENERIC SPECTRAL MODEL FOR ARBITRARY PERIODIC PROFILES

When the periodic VSFPWM is applied, the phases of the carrier and modulation reference signals are modified as:

$$
\begin{cases}
x(t) = 2\pi\int_0^t f_{\mathrm{c}}(\tau)\mathrm{d}\tau + \theta_{\mathrm{c}} \\
y(t) = \omega_{\mathrm{o}}t + \theta_{\mathrm{o}}
\end{cases}
\tag{4.6}
$$

The spectrum model hence becomes more complicated and very difficult to be directly derived with DFA because of the nonlinearity caused by the periodic time-varying variable $\omega_{\mathrm{c}}(t)$ appearing in the carrier angular frequency $x(t)$. Tripple Fourier analysis is also not applicable since variable $x(t)$ and $\omega_{\mathrm{c}}(t)$ are inter-coupled and not linear. To derive the spectrum expression some assumptions are adopted in this work to approximate the derived voltage expression:

1) The ratio between the centered switching frequency and the fundamental frequency $\omega_{\mathrm{c0}}/\omega_{\mathrm{o}}$ should be large enough, where the centered angular frequency ω_{c0} is the average of $\omega_{\mathrm{c}}(t)$ during its period.

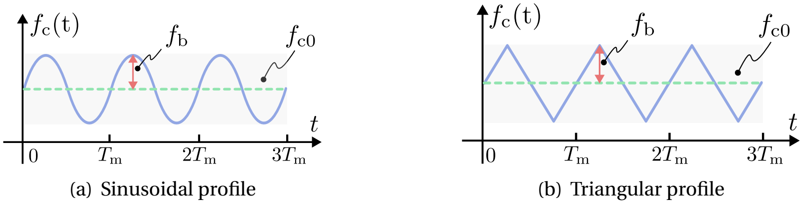
2) The variation band of the switching frequency ω_{b} (or f_{b}), which is half of the peak-to-peak variation of the switching profile, should be relatively small compared to the centered frequency ω_{c0}.

These two assumptions guarantee that the influence of the varying switching frequency on the coefficients presented in (4.2) can be negligible and hence the forms of these coefficients remain unchanged in the following mathematical derivations, except that ω_{c} is replaced by ω_{c0}.

The periodic frequency $f_{\mathrm{c}}(t)$ can be generally expressed with the following Fourier series:

$$f_{\mathrm{c}}(t) = f_{\mathrm{c0}} + \sum_{k=1}^{\infty} C_k \sin(2\pi k f_{\mathrm{m}} t + \theta_{\mathrm{k}}) \tag{4.7}$$

where f_{c0} is the centered switching frequency and f_m is the frequency of the periodic switching profile. Some typical periodic profiles such as sinusoidal and triangular profiles are illustrated in Fig. 4.6, where f_{b} is the peak deviation of the frequency from the centered frequency. Typically $f_{\mathrm{b}} = C_1$ for the sinusoidal profile. The harmonic spectrum model of the converter output voltage under P-VSFPWM hence becomes extremely complicated since the new variable $f_{\mathrm{c}}(t)$ is coupled with $x(t)$ and thus the Tripple Fourier analysis (TFA) is not applicable. By substituting (4.6) and (4.7) into (4.2), the time-domain expression of the bridge-leg output voltage under P-VSFPWM is derived as:



(a) Sinusoidal profile (b) Triangular profile

Figure 4.6: Commonly used periodic switching frequency profiles.

$$\begin{aligned} v_c(t) =& \Re\Big(\sum_{m=0}^{\infty}\sum_{n=-\infty}^{\infty} C_{\mathrm{mn}} \cdot e^{\mathrm{j}(2\pi(\mathrm{m}\int_0^{\mathrm{t}} \mathrm{f_c}(\tau)\mathrm{d}\tau + \mathrm{nf_o t}) + \theta_{\mathrm{mn}})}\Big) \\ =& \Re\Big(\sum_{m=0}^{\infty}\sum_{n=-\infty}^{\infty} \{C_{\mathrm{mn}} \cdot e^{\mathrm{j}(2\pi(\mathrm{mf_{c0}} + \mathrm{nf_o})\mathrm{t} + \theta_{\mathrm{mn}} + \varphi_{\mathrm{m}})} \cdot \underbrace{\prod_{k=1}^{\infty} e^{-\mathrm{j}\frac{\mathrm{mC_k}}{\mathrm{kf_m}}\cos(2\pi\mathrm{kf_m t} + \theta_{\mathrm{k}})}\}\Big)}_{\text{term due to P-VSFPWM}} \end{aligned} \tag{4.8}$$

where

$$\begin{aligned} \theta_{\mathrm{mn}} &= m\theta_{\mathrm{c}} + n\theta_{\mathrm{o}} \\ \varphi_{\mathrm{m}} &= \sum_{k=1}^{\infty} \frac{mC_{\mathrm{k}}\cos(\theta_{\mathrm{k}})}{kf_{\mathrm{m}}}. \end{aligned} \tag{4.9}$$

In (4.8), the multiplication term is contributed by the varying switching frequency. It can be noted that the model is not straightforward from the perspective of harmonic magnitude and indirect to be used for calculation. In [22], therefore, the model has been simplified and derived into the triple summation series form by implementing Jacobi-Anger expansions [50]. The converter output voltage v_c under the P-VSFPWM can be formulated as:

$$v_\mathrm{c}(t) = \Re\left(\sum_{m=0}^{\infty} \sum_{n=-\infty}^{\infty} \sum_{l=-\infty}^{\infty} \{C_\mathrm{mnl} \cdot e^{\mathrm{j}2\pi(\mathrm{mf_{c0}t+nf_ot+lf_mt})}\}\right) \tag{4.10}$$

where

$$C_\mathrm{mnl} = C_\mathrm{mn} \cdot e^{\mathrm{j}(\theta_\mathrm{mn}+\varphi_\mathrm{m})} \cdot h(m,l) \tag{4.11}$$

$$h(m,l) = \sum_{\sum r_k \cdot k = l} \left(\prod_{k=1}^{\infty} J_\mathrm{r}\left(\frac{mC_\mathrm{k}}{kf_\mathrm{m}}\right) \cdot e^{\mathrm{j}(\mathrm{r}(\theta_\mathrm{k}-\pi/2))}\right) \tag{4.12}$$

where $J_\mathrm{n}(x)$ is the Bessel function of the first kind. In (4.11), C_mn can be expressed as follows:

$$C_\mathrm{mn} = \frac{2V_\mathrm{dc}J_\mathrm{n}[(m+n\frac{\omega_\mathrm{o}}{\omega_\mathrm{c0}})\frac{\pi M}{2}]}{\pi(m+n\frac{\omega_\mathrm{o}}{\omega_\mathrm{c0}})} \sin[(m+n\frac{\omega_\mathrm{o}}{\omega_\mathrm{c0}}+n)\frac{\pi}{2}]. \tag{4.13}$$

when the symmetrical sampling is applied with the sinusoidal pulse-width modulation (SPWM) strategy. Specifically, when $f_\mathrm{c}(t)$ is a sinusoid with the frequency f_m, the coefficient C_mnl is reduced to:

$$C_\mathrm{mnl} = C_\mathrm{mn}J_\mathrm{l}\left(\frac{mC_1}{f_\mathrm{m}}\right) \cdot e^{j(\theta_\mathrm{mn}+\varphi_\mathrm{m}+l(\theta_1-\pi/2))} \tag{4.14}$$

which is simpler to calculate. It should be highlighted that the triple-summation series form in (4.10) is also applicable to other PWM methods such as THIPWM (Third-harmonic-injection PWM), SVPWM (Space-vector PWM) and DPWM (Discontinuous PWM) [50]. However, in this work, only SPWM is adopted for the sake of simplicity in analysis. It is noteworthy that the spectrum of the output voltage can be obtained based on (4.10) because of the triple summation series form, and phasor representation. It can be noted that the side-band harmonics are the resultant contributed by the integer variables n and l, which represent the side-band caused by CSFPWM and VSFPWM respectively. It is noted that the triple summation series form presented in (4.10) is valid only when the aforementioned two assumptions are satisfied. The assumptions guarantee that the difference of the coefficient C_mn during the switching frequency variation is negligible and thus the coefficient can be calculated at the centered frequency f_c0 as shown in (4.13) and remain unchanged regardless the switching frequency. The coefficient C_mnl contains the magnitude and phase information of the spectrum. However, for each possible side-band lf_m caused by VSFPWM there are infinite groups of r_k and hence the calculation of (4.11) becomes cumbersome.

4.3.2. DIFFERENTIAL-MODE (DM) HARMONICS

In the three-phase three-wire AC/DC system depicted in Fig. 4.4, only the differential-mode (DM)currents can flow into the three-phase grid or load when considering the

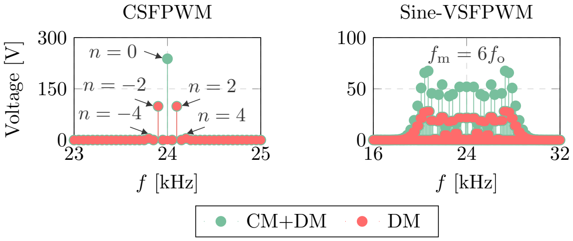


Figure 4.7: Original (CM+DM) and differential-mode (DM) components of the converter output voltage harmonics under CSFPWM and P-VSFPWM.

supra-harmonics frequency ranges. This is due to the inherent large impedance that prevents the common-mode (CM) or zero-sequence currents from flowing into the grid or load. From the interest of harmonics and supra-harmonics emission and the related filter design, only the DM harmonic components are concerned in terms of the grid-side current harmonics. Generally, the DM and CM components satisfy the following relations:

$$\begin{cases} x_{\mathrm{a}} + x_{\mathrm{b}} + x_{\mathrm{c}} = 0 & \text{Differential-mode} \\ x_{\mathrm{a}} = x_{\mathrm{b}} = x_{\mathrm{c}} & \text{Common-mode} \\ v_{j,\mathrm{dm}} = v_j - \dfrac{v_{\mathrm{a}} + v_{\mathrm{b}} + v_{\mathrm{c}}}{3} & (j = a, b, c). \end{cases} \tag{4.15}$$

where j represents the three-phase voltages and currents in the circuit. Alternatively, the terms with n equal to zero and the triple multiples in (4.11) should be rid of from the original harmonics in order to obtain only the DM harmonics components according to to (4.11) and (4.23). However, this approach can be only used when the three phases adopt the same frequency profile. Fig. 4.7 depicts the original and DM components of the converter output voltage under both CSFPWM and P-VSFPWM (sinusoidal profile). It can be seen that DM and CM components are separately lying in the spectrum. Moreover, the DM harmonic spectrum is only part of the original one and has lower magnitudes. Besides, it is noteworthy that the CSFPWM method only generates several considerable harmonics at $n = 0, \pm 2, \pm 4$. This feature can be used in the proposed algorithm to reduce the calculation time by setting $N \leqslant 4$. The DM voltage harmonics can be separated from the original spectrum by discarding the CM components generated by the CSFPWM since P-VSFPWM does not contribute to the generation of CM components. In other words, the use of (4.11) should neglect the terms with n equal to zero and the triple multiples. Besides, for practical use of (4.11) to calculate the voltage harmonic at a specific harmonic order, some simplifications can be adopted to reduce the calculation time with adequate accuracy. Fig. 4.8 describes the procedures for the practical calculation of the specified voltage harmonic. Usually, the first ten terms in the Fourier series expansion of the periodic waveform can give a satisfactory approximation [80]. The same approximation also holds for the Jacobi-Anger expansion because of the rapid roll-off of the Bessel function magnitudes [50]. Hence, the maximum value for both r and k shown in Fig. 4.8 is taken as 10. To validate the correctness of the derived model without losing generality, the voltage spectrum generated by the analytical model is compared with the circuit simulation results under SPWM, THIPWM and SVPWM [50]. Fig. 4.9 shows the

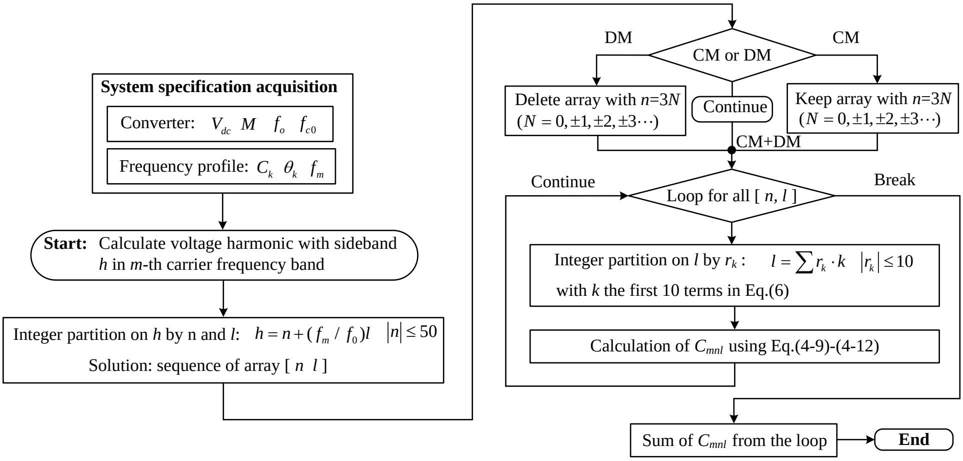

System specification acquisition
Converter: V_{dc} M f_o f_{c0}
Frequency profile: C_k θ_k f_m
Start: Calculate voltage harmonic with sideband h in m-th carrier frequency band
Integer partition on h by n and l: $h=n+(f_m/f_0)l$ $|n|\le 50$
Solution: sequence of array [n l]
CM or DM
DM
CM
Delete array with n=3N ($N=0,\pm1,\pm2,\pm3\cdots$)
Continue
Keep array with n=3N ($N=0,\pm1,\pm2,\pm3\cdots$)
CM+DM
Continue
Loop for all [n, l]
Break
Integer partition on l by r_k: $l=\sum r_k\cdot k$ $|r_k|\le 10$
with k the first 10 terms in Eq.(6)
Calculation of C_{mnl} using Eq.(4-9)-(4-12)
Sum of C_{mnl} from the loop
End

Figure 4.8: Calculation algorithm for the harmonic spectrum.

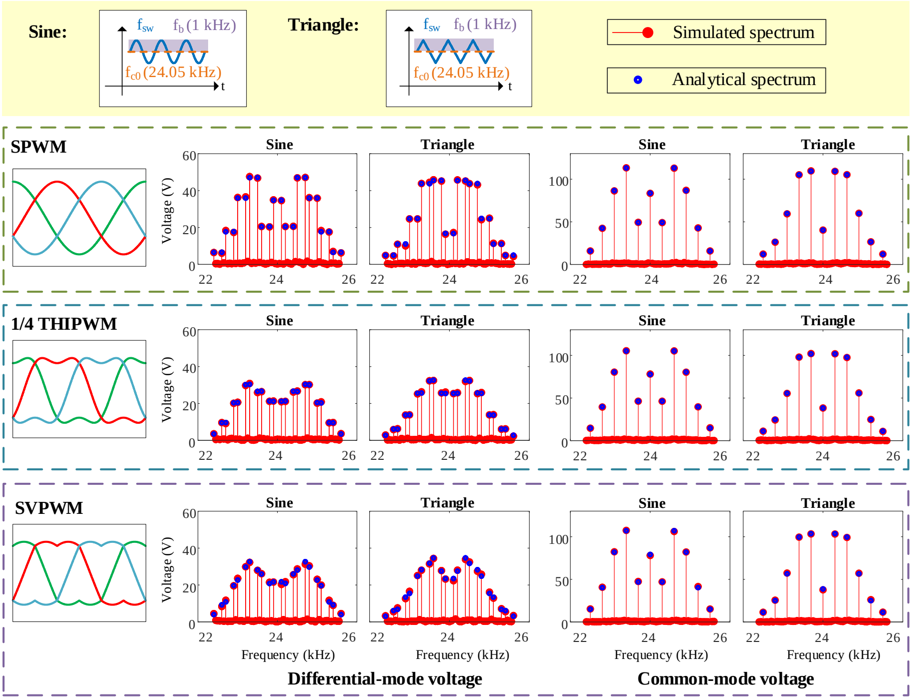


Figure 4.9: The simulated and analytical converter output voltage spectrum under different modulations and frequency profiles.

simulated voltage harmonic spectra compared with the analytically constructed spectrum calculated by (4.11) under sinusoidal and triangle variable frequency profiles in

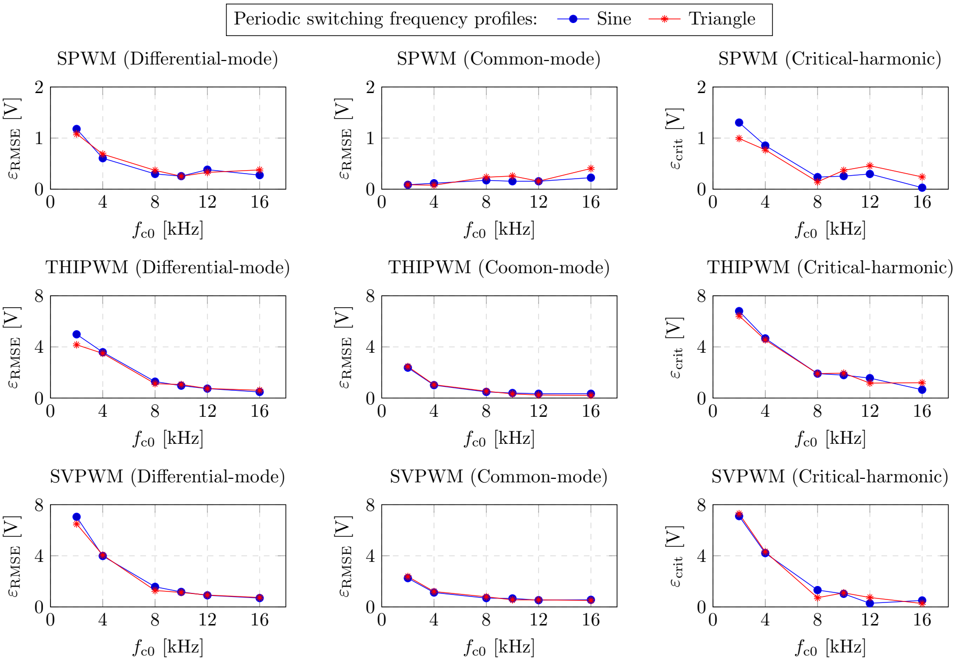


Figure 4.10: Errors between the analytical and simulated results under lower centered switching frequency range.

the three different modulation cases. The profiles are implemented with f_{c0} =24.05 kHz and f_b =1 kHz. The modulation parameters can be found in Table 4.2. Since only the first carrier band spectrum is typically concerned with the design of the AC filter only the first carrier band spectra are shown in Fig. 4.9. In each modulation case, the CM and DM voltage spectra of either simulation or analytical results are separated and compared respectively. The results illustrate that (4.11) can predict the harmonic spectra of the VSC-generated voltage well, which matches the simulated results with relatively good accuracy. The results depicted hence verify the correctness of the model as well as the proposed calculation algorithm.

4.3.3. APPLICABILITY TO LOW SWITCHING FREQUENCY

The two assumptions mentioned in subsection 4.3.1 require a relatively larger centered switching frequency and narrowed variation band of the variable switching frequency to guarantee a reasonable approximation of the coefficient C_{mn} for VSFPWM as described

Table 4.2: Modulation parameters.

V_{dc} [V]	V_{ac} [V]	f_o [Hz]	f_{c0} [kHz]
700	$\sqrt{2}\cdot 230$	50	24.05

in (4.13), where the following substitution is made:

$$n\frac{\omega_\mathrm{o}}{\omega_\mathrm{c}(t)} \Longrightarrow n\frac{\omega_\mathrm{o}}{\omega_\mathrm{c0}} \tag{4.16}$$

Still, it is necessary to quantify the applicable range of the centered switching frequency for the derived analytical spectrum model. In order to assess the accuracy of the model under different centered switching frequencies other than 24.05 kHz, the voltage spectra given by the simulation and analytical results are compared for different cases of f_c0, namely f_c0 = 2 kHz, 4 kHz, 8 kHz, 10 kHz, 12 kHz, and 16 kHz respectively. The variation band f_b is always selected to be one-tenth the centered switching frequency to exhibit a fair comparison between different cases. Fig. 4.10 presents the root-mean-square error (RMSE) and the critical harmonic error between the simulated and analytical spectra under various modulation methods and periodic switching frequency profiles. The root-mean-square error ε_{RMSE} is calculated by

$$\varepsilon_\mathrm{RMSE} = \sqrt{\frac{\sum_{k=1}^{N}(V_\mathrm{simu}(k) - V_\mathrm{analy}(k))^2}{N}} \tag{4.17}$$

where V_simu and V_analy represent the simulated and analytical voltage spectra and N is the total number of harmonics to be calculated in the spectra. Undoubtedly, the voltage error arises with the lower centered switching frequency applied to the analytical spectrum model. Besides, the error is much greater under 1/4 THIPWM and SVPWM methods compared to SPWM. This is because the voltage harmonics spectra generated by 1/4 THIPWM and SVPWM under CSFPWM with regular sampling is more dependent on the term $n\omega_\mathrm{o}/\omega_\mathrm{c0}$ compared to the SPWM method [50]. Hence the model becomes less accurate for 1/4 THIPWM and SVPWM under low centered switching frequency since (4.16) deviates from the assumptions. Lastly, the error in the common-mode voltage components of the spectra is much smaller compared to the differential-mode components. This is because the most common-mode harmonics in the spectra originate from the harmonic from CSFPWM where the side-band n=0. For those harmonics, the (4.16) is always valid since the term becomes zero.

In summary, the derived analytical spectrum model becomes less accurate under low centered switching frequency due to the unavoidable symmetrical regular sampling process of the digital implementation of PWM in practice. However, the error is still acceptable if the centered switching frequency f_c0 is selected to be larger than 4 kHz since the error is less than 4 V, which is relatively small (8%) compared to its critical harmonic magnitude. Usually, a design margin of inductance will be considered for the inductor to deal with the inductance variation under high temperature and drop of permeability caused by current bias. Therefore, the proposed model can still be applicable to low centered switching frequency and the recommended range is $f_\mathrm{c0} \geqslant 4$ kHz.

4.3.4. FAST ACQUISITION HARMONIC SPECTRAL MODEL BASED ON VECTORIZATION

It is noteworthy that (4.10) describes only the individual harmonic content with magnitude and phase at the frequency determined by m, n, and l. However, the harmonic at a certain frequency is the sum of these individual harmonics which share the same frequency due to the different combinations of m, n, and l. Hence, the harmonic spectra of the output voltage in the interleaved 2-level converter can not be directly calculated based on (4.10). The calculation algorithm illustrated in Fig. 4.8 is based on the partition to generate the voltage spectra. However, this algorithm requires a significant amount of partition operations and iterations and hence becomes very complicated for practical use. Instead, a spectra-acquisition algorithm based on the vectorization operation is proposed in this work for faster calculation of the harmonics spectra.

$$
\begin{gathered}
\boldsymbol{C}_{\mathbf{mn}} = \begin{bmatrix} C_{\mathrm{m,N}} & \cdots & C_{\mathrm{m,N}} \\ \vdots & \ddots & \vdots \\ C_{\mathrm{m,-N}} & \cdots & C_{\mathrm{m,-N}} \end{bmatrix} \quad \boldsymbol{\Theta}_{\mathbf{mn}} = \begin{bmatrix} \theta_{\mathrm{m,N}}+\varphi_{\mathrm{m}} & \cdots & \theta_{\mathrm{m,N}}+\varphi_{\mathrm{m}} \\ \vdots & \ddots & \vdots \\ \theta_{\mathrm{m,-N}}+\varphi_{\mathrm{m}} & \cdots & \theta_{\mathrm{m,-N}}+\varphi_{\mathrm{m}} \end{bmatrix} \\
\boldsymbol{H}_{\mathbf{ml}} = \begin{bmatrix} h(m,-L\cdot h) & \cdots & h(m,(-L+1)\cdot h) & \cdots & h(m,(L-1)\cdot h) & \cdots & h(m,L\cdot h) \\ \vdots & \ddots & \vdots & \vdots & \vdots & \vdots & \vdots \\ h(m,-L\cdot h) & \cdots & h(m,(-L+1)\cdot h) & \cdots & h(m,(L-1)\cdot h) & \cdots & h(m,L\cdot h) \end{bmatrix} \\
\boldsymbol{N} = \begin{bmatrix} N & \cdots & N \\ \vdots & \ddots & \vdots \\ -N & \cdots & -N \end{bmatrix} \quad \boldsymbol{L}_{\mathbf{h}} = \begin{bmatrix} -L\cdot h & \cdots & (-L+1)\cdot h & \cdots & (L-1)\cdot h & \cdots & L\cdot h \\ \vdots & \ddots & \vdots & \vdots & \vdots & \vdots & \vdots \\ -L\cdot h & \cdots & (-L+1)\cdot h & \cdots & (L-1)\cdot h & \cdots & L\cdot h \end{bmatrix}
\end{gathered} \tag{4.18}
$$

STEP 1 — MATRICES GENERATION

To start with simply, matrices with the dimension $(2N+1)\times(2h\cdot L+1)$ presented in (4.18), where h is the ratio between f_{m} and f_{o}, are firstly constructed to define harmonics information e.g., magnitude, phase and spectral position of the m^{th} carrier-frequency harmonics. For the convenience of harmonics, h is usually selected to be an integer as observed from Table 4.2. It should be noted that the element in matrices $\boldsymbol{L}_{\mathbf{h}}$ and $\boldsymbol{H}_{\mathbf{ml}}$ only occur every h columns and the rest columns have the elements of 0. Hereafter the matrix $\boldsymbol{C}_{\mathbf{mnl}}$ can be established from the Hadamard product ($\odot$, also called element-wise product) and the sum of these created matrices:

$$
\begin{aligned}
\boldsymbol{C}_{\mathbf{mnl}} &= \boldsymbol{C}_{\mathbf{mn}} \odot e^{j\boldsymbol{\Theta}_{\mathbf{mn}}} \odot \boldsymbol{H}_{\mathbf{ml}} \\
\boldsymbol{R}_{\mathbf{mnl}} &= m\cdot M_{\mathrm{f}} + \boldsymbol{N} + \boldsymbol{L}_{\mathbf{h}}
\end{aligned} \tag{4.19}
$$

where M_{f} is the ratio between f_{c0} and f_{o}.

STEP2 — VECTOR ACQUISITION

The matrices $\boldsymbol{C}_{\mathbf{mnl}}$ and $\boldsymbol{R}_{\mathbf{mnl}}$ contain the spectral information of the harmonics in terms of magnitude and frequency position. Each diagonal of $\boldsymbol{R}_{\mathbf{mnl}}$ indicates a certain frequency, where the corresponding diagonal of $\boldsymbol{C}_{\mathbf{mnl}}$ contains the individual harmonics. To obtain the resultant harmonic vector $\boldsymbol{H}_{\mathbf{m}}$, the elements of the matrices should be summed up according to the diagonals:

$$
\boldsymbol{H}_{\mathbf{m}} = diag(\boldsymbol{C}_{\mathbf{mnl}}) \tag{4.20}
$$

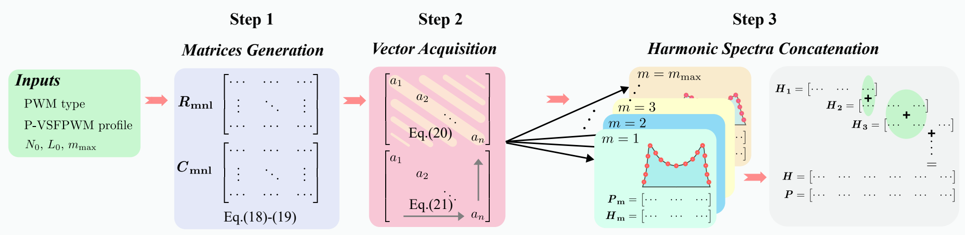

Step 1
Matrices Generation
Step 2
Vector Acquisition
Step 3
Harmonic Spectra Concatenation
Inputs
PWM type
P-VSFPWM profile
N_0, L_0, $m_{\max}$
R_{mnl}
C_{mnl}
Eq.(18)-(19)
a_1
a_2
a_n
Eq.(20)
Eq.(21)
$m = m_{\max}$
$m = 3$
$m = 2$
$m = 1$
$P_{\mathrm{m}} = [\cdots \ \cdots \ \cdots]$
$H_{\mathrm{m}} = [\cdots \ \cdots \ \cdots]$
$H_1 = [\cdots \ \cdots \ \cdots]$
$H_2 = [\cdots \ \cdots \ \cdots]$
$H_3 = [\cdots \ \cdots \ \cdots]$
+
=
$H = [\cdots \ \cdots \ \cdots \ \cdots \ \cdots \ \cdots]$
$P = [\cdots \ \cdots \ \cdots \ \cdots \ \cdots \ \cdots]$

Figure 4.11: Fast harmonic spectra acquisition algorithm based on vectorization.

where the function $diag$ sums up each diagonal of an arbitrary matrix into a vector and can be easily found and implemented on various programming platforms such as Matlab and Python.

Different from $\boldsymbol{H}_{\mathbf{m}}$, the harmonic position vector $\boldsymbol{P}_{\mathbf{m}}$ is formed by the following:

$$\begin{aligned} \boldsymbol{P}_{\mathbf{m}} &= trace(\boldsymbol{R}_{\mathbf{mnl}}) \\ &= m \cdot M_{\mathrm{f}} + \begin{bmatrix} -N-h\cdot L & \cdots & 0 & \cdots & N+h\cdot L \end{bmatrix} \end{aligned} \tag{4.21}$$

where the function $trace$ is to acquire the outest element of the matrix from bottom-left to top-right. This can be done by concatenating either the first column and row or the last row and column with the direction from bottom-left to top-right. The harmonic vectors $\boldsymbol{H}_{\mathbf{m}}$ represent the m^{th} carrier-frequency switching harmonics with their spectral positions (harmonic order) listed in vector $\boldsymbol{P}_{\mathbf{m}}$. The size of the two vectors is $1 \times (2N + 2h \cdot L + 1)$, indicating that the harmonic side-band ranges from $-(N + h \cdot L)$ to $(N + h \cdot L)$ for m^{th} carrier-frequency switching harmonics.

However, the accuracy of $\boldsymbol{H}_{\mathbf{m}}$ decreases with the increase of m if the same N and L are used to calculate the carrier-frequency harmonics for all orders. This is because the harmonics range of $\boldsymbol{H}_{\mathbf{m}}$ naturally expands with multiplication of m and the fixed size of $\boldsymbol{H}_{\mathbf{m}}$ might not include the entire harmonic spectrum scope. The same N and L with large enough values can be applied to all matrices regardless of m to avoid this inaccuracy. Nonetheless, more computational efforts have to be traded off. Therefore, N_{m} and L_{m} are used instead of N and L for matrix generation:

$$\begin{cases} N_{\mathrm{m}} = m \cdot N_0 \\ L_{\mathrm{m}} = m \cdot L_0 \end{cases} \tag{4.22}$$

where N_0 and L_0 are the fixed values independent of m. For instance, by applying (4.22), the matrix dimension for the second carrier-frequency harmonics will be doubled in both the length and width compared to that of the first carrier-frequency harmonics.

STEP 3 — HARMONIC SPECTRA CONCATENATION

Thereafter, the harmonics generated in different carrier-frequency ranges (e.g., 1^{st}, 2^{nd}, 3^{rd} carrier-frequency harmonics) can be easily calculated. To attain the final harmonic spectra, the harmonic vectors $\boldsymbol{H_\mathrm{m}}$ with different m values should be concatenated into a new harmonic vector $\boldsymbol{H}$ with the range defined by the combined position vector $\boldsymbol{P}$:

$$\begin{aligned} \boldsymbol{H} &= cat(\boldsymbol{H_\mathrm{m}}) \quad (m = 1, 2, 3 \cdots m_{\max}) \\ \boldsymbol{P} &= cat(\boldsymbol{P_\mathrm{m}}) \quad (m = 1, 2, 3 \cdots m_{\max}). \end{aligned} \tag{4.23}$$

The $cat()$ function is realized by summing up the elements from all $\boldsymbol{H_\mathrm{m}}$ vectors (same to $\boldsymbol{P_\mathrm{m}}$) at the same harmonic orders. The complete diagram of the proposed algorithm of the harmonic spectra acquisition under P-VSFPWM is demonstrated in Fig. 4.11. Besides, to obtain the voltage harmonic spectra with (4.10), some simplifications are used to accelerate the calculation with adequate accuracy. Usually, the first three terms in the Fourier series expansion of the periodic waveform can give a satisfactory approximation [22].

4.4. EXPERIMENTAL VERIFICATION

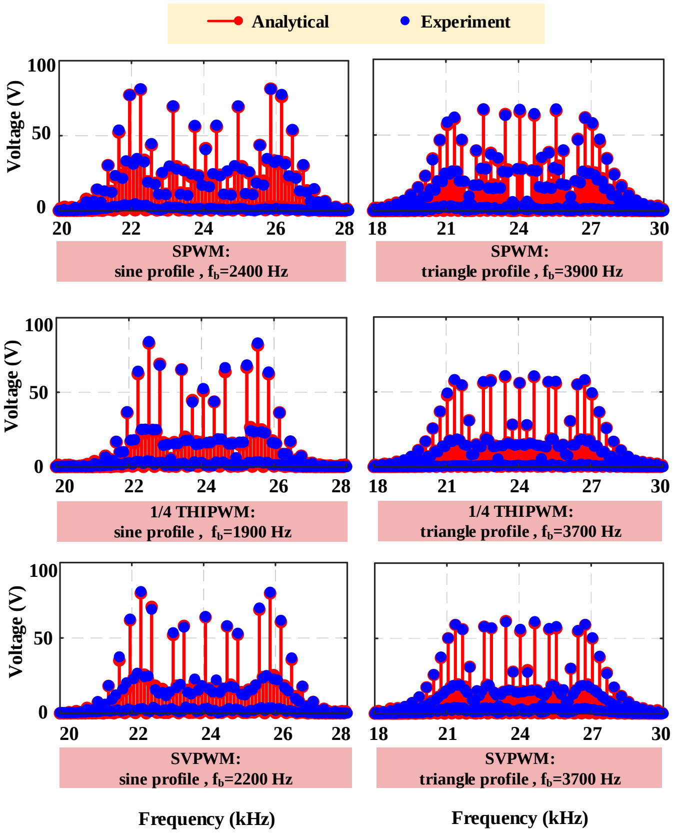


Figure 4.12: Comparison between the analytical and experimental results of the converter output voltage spectra of the 1$^{\mathrm{st}}$ carrier band under various switching profiles and PWM methods.

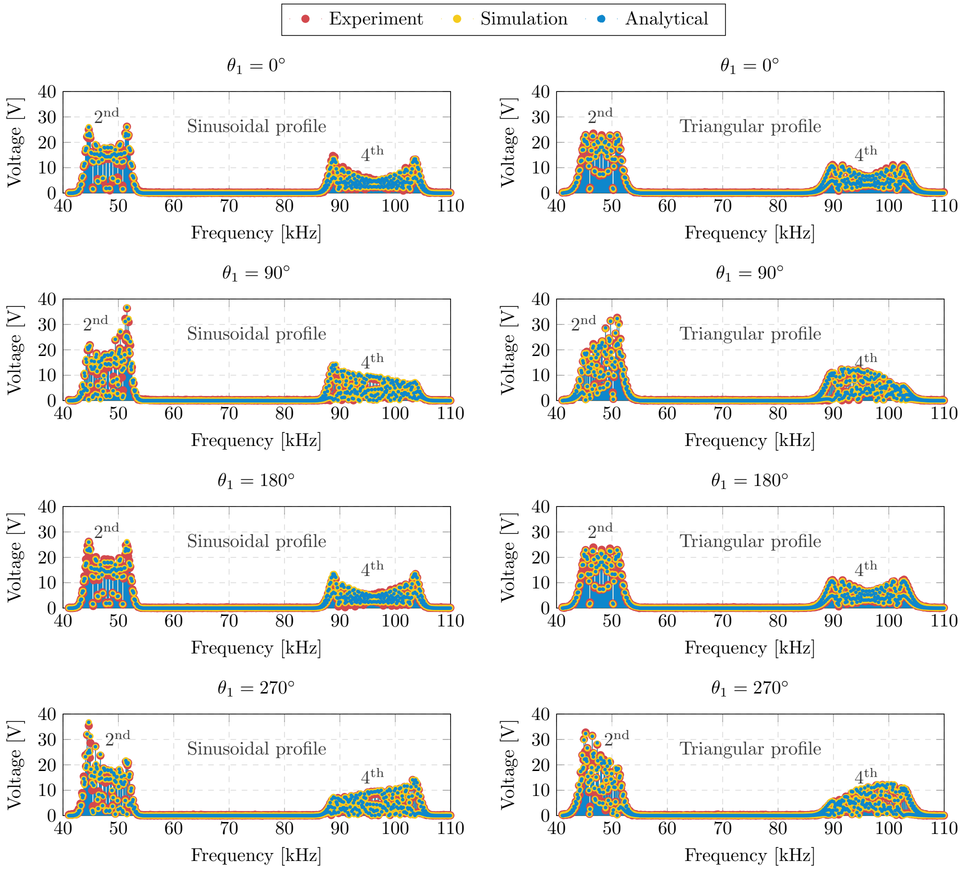
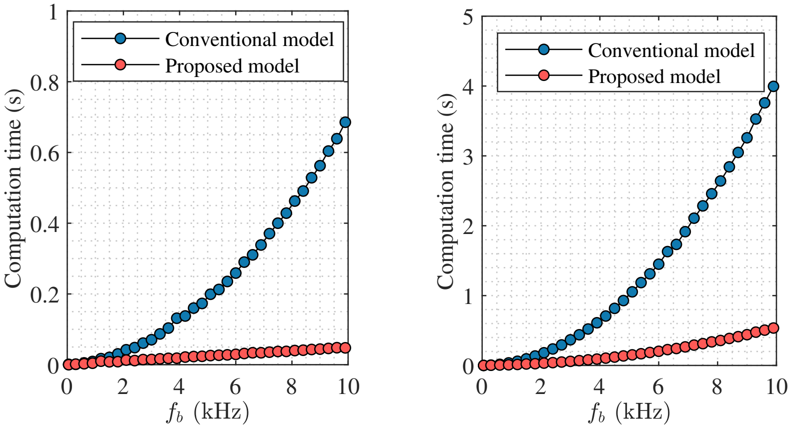


Figure 4.13: Spectra comparison between analytical, simulation and experimental results: The voltage harmonic spectra (Phase A) of the interleaved 2-level converter under SPWM, f_{C0}=24.05 kHz, f_{b}=2 kHz, $f_{\mathrm{m}} = 6f_{\mathrm{o}}$. Both the sinusoidal and triangular periodic profiles were tested at $\theta_1 = 0°$, $90°$, $180°$ and $270°$.

In order to further validate the correctness and feasibility of the proposed harmonics model generated by P-VSFPWM, different switching profiles are experimentally realized in the three-phase two-level converter and interleaved 2-level converter prototypes presented in Chapter. 2.

The correctness of the analytical VSFPWM spectrum model has already been verified by comparing the simulated and analytical converter output voltage spectra, which is shown in Fig. 4.9. The generated output voltage spectra from the experimental results are obtained and presented in Fig. 4.12, in comparison with the analytically constructed harmonic spectra based on Fig. 4.9. It can be noted that the spectra from the experimental results match the analytical ones well in all PWM methods and periodic switching profiles. With the analysis on the spectra, the maximum discrepancy between the two spectra is 1.7 V, which is 0.5% of the fundamental voltage and hence can be regarded to be negligible from the design point of view. From the spectra shown in Fig. 4.12, it can be noted that the triangle profiles in fact exhibit a more evenly spread spectrum compared to the sinusoid profile. This finally results in a smaller critical voltage harmonic requirement to be filtered out. Thereafter, it can be concluded that the analytical model of the periodic VSFPWM spectrum is verified to be correct based on the analysis from the simulation and experimental results.

Beyond the 1st carrier-frequency switching harmonics, the algorithm depicted in Fig. 4.9 is limited by its calculation speed. The effectiveness of the proposed fast acquisition harmonic spectral model based on vectorization has been also verified as compared to the algorithm in Fig. 4.9. The voltage harmonic spectra (Phase A) of the interleaved 2-level converter under f_{C0}=24.05 kHz, f_{b}=2 kHz, $f_{\mathrm{m}} = 6f_{\mathrm{o}}$ was obtained through conducting FFT analysis of the converter output voltage measured from the simulation and experiment under. Both the sinusoidal and triangular periodic profiles were tested at $\theta_1 = 0°$, 90°, 180° and 270°. The correctness of the proposed harmonic spectra acquisition method is validated by comparing the analytical harmonic spectra obtained based on Fig. 4.11 with those acquired from both the simulation and experimental results. Fig. 4.13 presents the harmonic spectra of the interleaved 2-level VSC output voltage (Phase A) from the analytical, simulation and experimental results. Because of interleaving, the harmonic spectra reside around 48.1 kHz (2nd carrier-frequency harmonics) and 96.2 kHz (4th carrier-frequency harmonics). It can be clearly noted that the analytical harmonic spectra based on the proposed algorithm accurately match the simulated voltage harmonic spectra in all cases. Even for the 4th carrier-frequency harmonics components, which cost much longer computational efforts with the algorithm proposed by [22], can be easily calculated with very high accuracy (maximum difference at critical harmonic: 0.2 V, 0.6%) to the simulation results. When compared to the experimental results, the analytical voltage harmonic spectra have a visible but negligible difference (maximum difference at critical harmonic: 1.35 V, 3.8%). The difference between



(a) Sinusoidal profile (b) Triangular profile

Figure 4.14: Comparison of the computational time cost between the model in [22] and the proposed model.

the simulation and experimental results might be caused by the periodic switching frequency discretized by the DSP, whose f_m and f_b values can be slightly offset from the set values. Besides, the difference can be also a result by the variation of the DC link voltage by the DC power source. Lastly, the unbalance between the three-phase load can lead to the asymmetry between the three-phase spectra.

4.4.1. COMPUTATIONAL TIME FOR THE PROPOSED MODEL

The vectorization-based model proposed in this chapter offers a significant computational advantage over the conventional harmonic spectra model by eliminating numerous calculation loops. A comparison of computation time for generating the 1^{st} carrier-frequency harmonic spectrum using both models [22] reveals that the proposed method reduces the calculation time by 8 times for optimal sinusoidal and triangular profiles, as compared in Table 4.3. As shown in Fig. 4.14, computation time increases exponentially with f_b in sinusoidal and triangular profiles with the conventional method, while the proposed model shows a linear relationship for sinusoidal profiles. Triangular profiles exhibit an exponential relationship with a smaller curvature compared to the conventional model. This demonstrates the superiority of the proposed approach.

Table 4.3: COMPUTATION TIME COMPARISON

Switching Profile	Computation time (s)	
	Proposed model	Model in [22]
Sinusoidal: f_b=5400 Hz	0.028	0.252
Triangular: f_b=9300 Hz	0.479	3.630

4.5. CONCLUSION

In conclusion, the quest for enhanced efficiency and power density in PWM converters has led to the widespread clustering of their switching frequencies within the supra-harmonics range. Consequently, significant supra-harmonics are injected into the grid, necessitating the adoption of variable switching frequency methods and other spread-spectrum techniques to meet regulatory standards. However, the absence of a comprehensive model addressing switching harmonics under variable switching frequency remains a gap in current literature.

This chapter fills this gap by introducing a generic supra-harmonics (switching harmonics) model for PWM converters under periodic variable switching frequency modulation with arbitrary profiles. The accuracy of this model has been rigorously validated through both simulation and experimental results. Additionally, a novel generic fast-acquisition harmonic spectra model based on vectorization is proposed, enabling practical implementation in MATLAB/Python environments. Compared to conventional algorithms reliant on partitions and loops, the proposed vectorization-based method boasts an impressive eight-fold increase in calculation speed, rendering it more practical for real-world applications.

5

DESIGN GUIDELINE FOR PWM CONVERTER IMPLEMENTING P-VSFPWM

This chapter explores the impact of periodic variable switching frequency modulation (P-VSFPWM) on the design of AC filters for power factor correction (PFC) converters. By analyzing the harmonic spectrum associated with P-VSFPWM profiles, it provides insights into the design of L and LCL filters commonly used in grid-tied voltage source converter (VSC) applications. The study reveals that employing P-VSFPWM methods enhances AC filter power density compared to conventional constant switching frequency continuous PWM strategies.

This chapter is based on the following research articles:

- Y. Wu, J. Xu, T. B. Soeiro, P. Bauer and Z. Qin, "Frequency Design of Three-phase Active Front-End Converter with Reduced Filter in EV Chargers," *in IEEE Transactions on Transportation Electrification*, doi: 10.1109/TTE.2024.3381167.
- Y. Wu, Z. Qin, T. B. Soeiro and P. Bauer, "Design Guideline for PWM Converter Implementing Periodic VSFPWM —A Comprehensive Analysis on the Harmonics Spectrum," 2023 11th International Conference on Power Electronics and ECCE Asia (ICPE 2023 - ECCE Asia), Jeju Island, Korea, Republic of, 2023, pp. 1509-1516.

5.1. INTRODUCTION

Due to the rapid development of renewable technology and wider adoption of electric vehicles, the pursuit of compact and efficient grid-tied power electronic converters is becoming increasingly important for photovoltaic and wind power generation, and battery fast charging stations. Pulse-width-modulation (PWM) based voltage source converters (VSCs) are widely employed as grid-tied converters because of their robustness and simplicity [81]. Correspondingly, LCL filters are adopted to mitigate the current harmonics generated by the PWM-based VSCs. Typically, the LCL filter is one of the bulkiest and heaviest parts in the high-power converter system. Hence, considerable research efforts in physical design and circuit topology have been devoted to aiming at reducing the filter size and weight.

It is recognizable that the design of a smaller inductor is possible if the application requirements can be fulfilled with the need of less magnetic energy storage, e.g. by reducing the need of inductance value without risking the magnetic core saturation under the same operating conditions [82, 83]. Conventional approaches for reducing the harmonic generated by the VSC, and therefore the required filtering inductance, consist on increasing the switching frequency, adopting interleaved or multi-level converter topologies, and implementing specific modulations [37, 84–88].

Variable switching frequency PWM (VSFPWM), for instance, is an interesting strategy to be implemented in VSCs because of its effectiveness in improving the switching loss, current ripple, EMI, and above all its simple digital implementation [89–94]. More

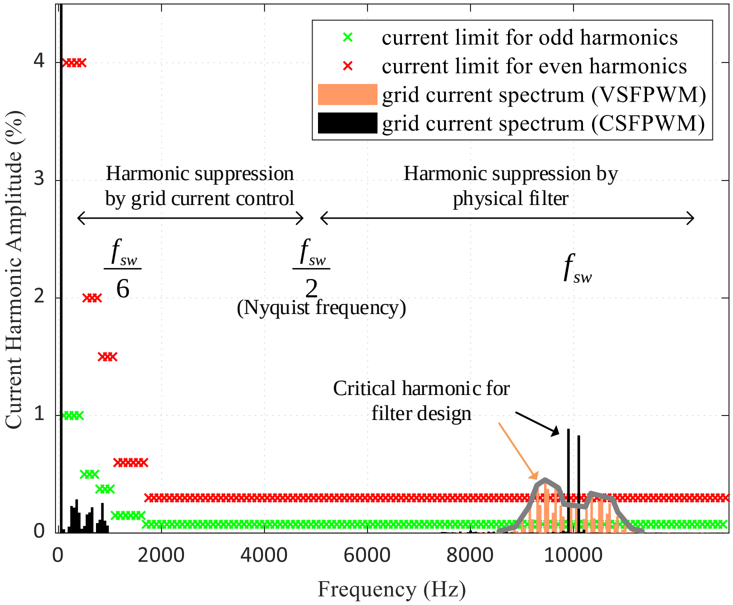


Figure 5.1: IEEE-519 harmonic current standard and typical grid current harmonic spectrum with CSFPWM and VSFPWM.

importantly, the spread spectrum caused by VSFPWM can also benefit the filter design for the VSC. However, there is a lack of research efforts about this concept at present. The filter used for grid-tied converter must be well-designed to comply with the grid connection standard, in particularly the harmonic current standards such as IEEE-519-2014 [84]. As presented in Fig. 5.1, the VSFPWM method spreads out the converter output voltage spectrum, thus giving a similarly wide harmonic spectrum with lower amplitudes for the grid current compared with the normally adopted constant switching frequency PWM (CSFPWM), when an AC filter is applied. The magnitude of the critical harmonic for the filter design is significantly reduced by VSFPWM. In other words, the filtering requirement can be alternatively lowered with the VSFPWM while maintaining the same level of critical current harmonic presented by the CSFPWM. Therefore the compact design of the LCL filter can be realized by the VSFPWM, leading to lower loss and weight in the filter, which can consequently improve the system efficiency and power density.

VSFPWM strategies can be categorized into two types: random (or chaotic) and periodic switching frequency profiles. From the perspective of shaping the spectra of the PWM output voltage for filter design, the periodic patterns are preferred, since random profiles do not provide a tight control on the spectrum band [80, 95, 96]. The critical harmonic for the filter design is found to be closely correlated with the band of the spectrum induced by the periodic VSFPWM. Hence, the LCL filter can be designed in consideration of not only normal design criteria but also the profile of the periodic VSFPWM (P-VSFPWM). Such a design requires the accurate voltage spectrum model of the three-phase PWM converter. The work in [95, 96] firstly studied the band of the spectrum induced by the periodic switching frequency profile in a PWM converter but did not provide further description of the spectrum contents. In [97], the spectrum model was presented in a complex domain for DC/DC PWM converters with the consideration of the sinusoidal switching profile only. Recently, [80] derived the analytical spectrum model for a three-phase PWM converter based on the PWM output voltage expressions described by [50]. However, the derived model only applies to sinusoidal switching profiles and is not valid for generic periodic switching profiles which include several harmonics instead of a single sinusoid.

The research on the filter design with VSFPWM is very limited in the literature. Only the restraint of current ripple on the filter inductance [98,99] or the basic requirement associated with the LCL filter resonance are considered [84, 100]. By contrast, this chapter investigates the influence of the P-VSFPWM profiles on the design of the filter of a three-phase three-wire system which complies with the grid harmonic IEEE-519-2014 standard, illustrated in Fig.5.1. The changing frequency profiles considered here are based on conventional waveform shapes, i.e., triangle and sinusoidal waveforms [95–97], due to their simple implementation in microcontrollers and straightforward identification of the critical current harmonic for the AC filter design. Therefore, the optimal P-VSFPWM profile is identified in this chapter and a guideline for the AC filter design is proposed which maximizes the VSC power density.

5.2. SPECTRAL ANALYSIS OF P-VSFPWM

5.2.1. THREE-PHASE SPECTRA SYMMETRY

The three-phase harmonics are balanced on the condition that the three-phase voltages and currents are balanced. However, the harmonic spectra of the three phases might not be symmetrically balanced, indicating a higher harmonic peak in one of the three phases. This will pose extra filtering efforts compared to the three-phase symmetrical spectra. Thus, it is necessary to investigate the symmetry property between the phases. In most scenarios of the periodic VSFPWM implementation in a three-phase PWM converter, the switching frequency profiles between the three phases are the same in shape but differ from each other in terms of phase. Then the three-phase converter output voltages (CM+DM components) have the same spectra under such a scenario. However, the DM components, which are mostly concerned in terms of the filter design in three-wire three-phase grid-connected applications, might differ from each other depending on the f_m. In the aforementioned situation, the phases of the reference signals under phase *a*, *b* and *c* are:

$$\begin{cases} \theta_{oa} = \theta_o \\ \theta_{ob} = \theta_o - \dfrac{2\pi}{3} \\ \theta_{oc} = \theta_o + \dfrac{2\pi}{3}. \end{cases} \tag{5.1}$$

According to (4.8)–(4.12), each carrier-frequency harmonic spectrum of the converter output voltage is influenced by not only the frequency profile but also the modulation and carrier signals. In other words, the phase angle θ_{mn}, and φ_m determine the shape of the spectrum significantly. Usually θ_k is restricted by the intended P-VSFPWM application and hence cannot be modified. The influence of θ_c can be neglected by aligning the carrier and modulation signals. Since θ_o is inherently 120° phase shifted between three phases as shown in (5.1), the frequency profile for each phase has to be phase-shifted accordingly to have the symmetrical output:

$$f_{cx}(t) = f_{c0} + \sum_{k=1}^{\infty} C_k \sin(2\pi k f_m t + k \cdot \theta_{ox} + \theta_k) \tag{5.2}$$

where $x = a, b, c$. Compared to (4.7), where the three phases adopt the same frequency profile, (5.2) allows the three phases to operate P-VSFPWM independently. The spectra of the first carrier-frequency harmonics of the three-phase output voltages are presented in Fig. 5.2, with the frequency profiles determined by both (4.7) and (5.2) under $f_m = 2f_o$.

It can be noted that the three-phase output voltages are not symmetrical in terms of both original (CM+DM) and DM harmonics with the same frequency profile (obtained through (4.7)) applied to the three phases. By contrast, the three phases exhibit the same original (CM+DM) harmonics if three phase-shifted frequency profiles (obtained through (5.2)) are used for three phases respectively.

Unfortunately, the DM components are still three-phase asymmetrical. In order to maintain three-phase symmetrical for both original (CM+DM) and DM harmonics as shown in Fig. 5.2, f_m should be selected to be triple multiple of f_o [22]. In this case, (4.7)

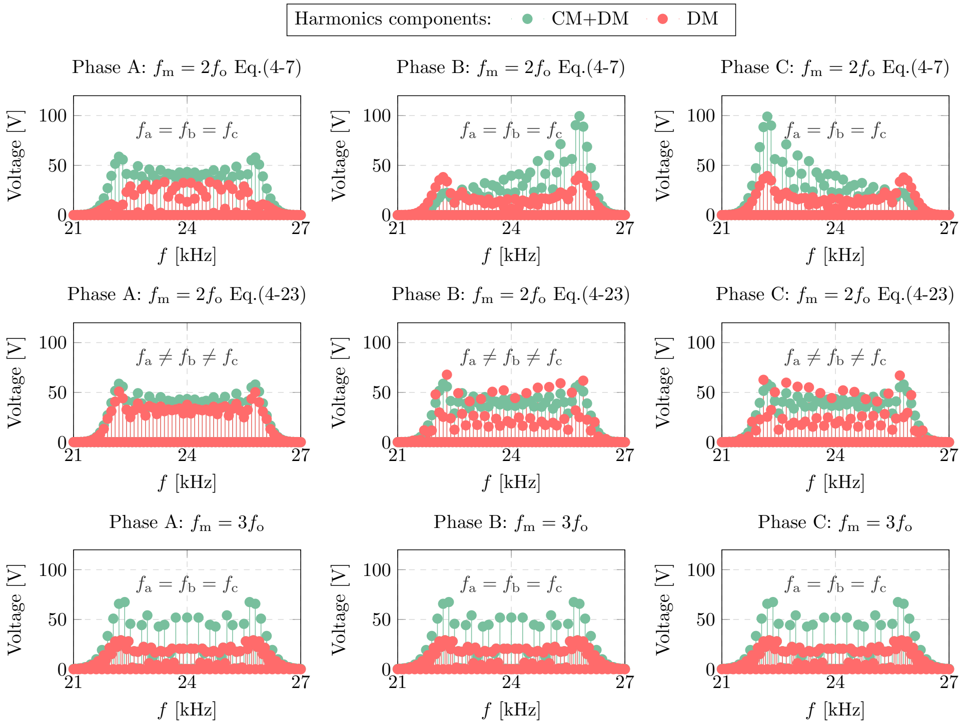


Figure 5.2: Spectra of the three-phase output voltages with the sinusoidal frequency profiles determined by (4.7) and (5.2): f_{C0}=24.05 kHz, f_b=2 kHz.

and (5.2) become the same and the three phases adopt only one frequency profile. However, in other cases where f_m is not triple of f_o, the phase which has the largest critical harmonic [22] should be considered for the filter design.

5.2.2. IMPACT OF SWITCHING PROFILES ON SPECTRUM SYMMETRY

Based on (4.10)-(4.13), the frequency-domain voltage harmonic model implies that a switching harmonic generated by periodic VSFPWM at a certain frequency is a combination of infinite individual harmonic terms with their own magnitudes and phases. Besides, the spreading pattern (height and width) of the spectrum is closely related to the parameters of the switching profile: C_k and f_m, which are selected to be multiples of the fundamental frequency f_o for better compliance with the harmonics standard. For practical use of this model to calculate or predict the spectrum, only limited terms are selected and then calculated since the original harmonic magnitude A_mn generated by the CSFPWM are non-zero at only certain frequencies. Under CSFPWM, the left and right side-band harmonics within the carrier harmonic band exhibit symmetry in the spectrum of the converter output voltage. Under periodic VSFPWM, such a symmetry depends on the frequency of the switching frequency profile f_m and the phases θ_k. The phase shift θ_k plays a significant role in the spectrum shape of the P-VSFPWM output

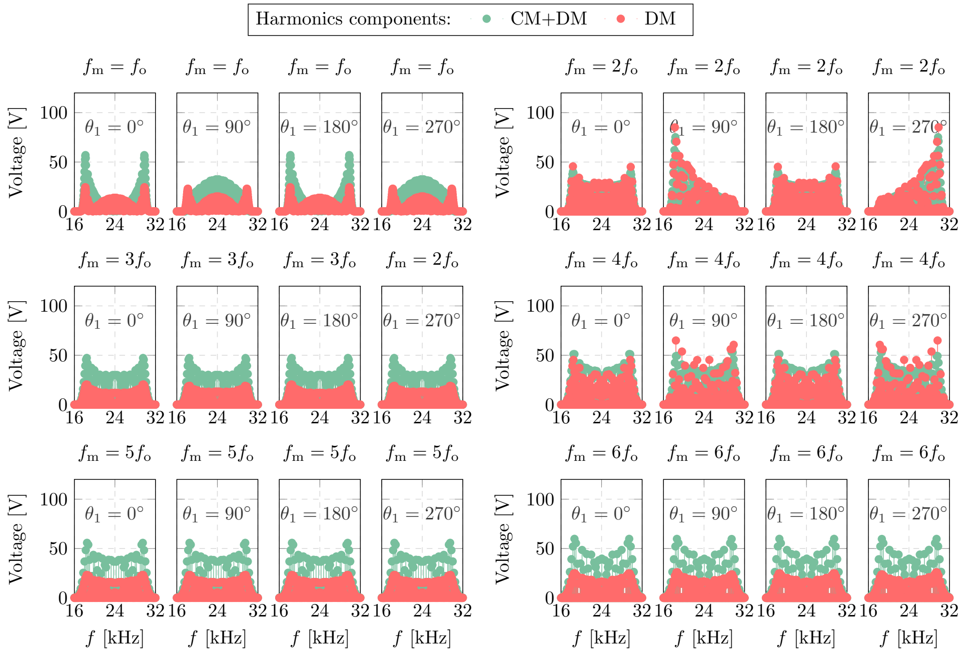


Figure 5.3: 1^{st} carrier-frequency harmonic spectrum of one phase (Phase A) under different f_m and θ_1 with frequency profiles determined by (4.7): f_{C0}=24.05 kHz, f_b=6 kHz.

voltages. More specifically, the value of θ_1 determines the alignment difference between the frequency profile and the modulation reference signals [101]. It can be found in Table 4.1 that θ_1 is usually 0°, 90° and 270° in the previous P-VSFPWM applications.

Therefore, the converter output voltage, expressed as the sum of the common-mode (CM) and differential-mode (DM) components, and its DM components in the first carrier band are depicted in Fig. 5.3 with the purely sinusoidal switching frequency profile, where k=1, C_k=6 kHz, f_{c0} =24 kHz and f_m is selected to be different multiples (from 1 to 6) of f_m. It can be noted from Fig. 5.3 that the symmetry of the voltage harmonic spectrum depends on the phase θ_k.

Several insights can be drawn: (1) The spectrum varies according to θ_k values. (2) At $\theta_\mathrm{k}=0°$ or 180°, the spectral symmetry is still maintained regardless of the ratio between f_m and f_o. (3) When $f+\mathrm{m}$ is even multiple of f_o, the spectrum shows the different levels of asymmetry at other angles.

Apart from θ_k, Fig. 5.3 also shows that the simulated harmonics spectrum is symmetrical with f_m being even multiples of f_o while asymmetric spectrum is presented with odd multiples. Additionally, the asymmetry also degrades with the increase of f_m: the voltage spectra under the case f_m=6f_o are in fact asymmetrical though they appear symmetrical from the figure. To be more specific, the maximum difference between the left and right part spectrum is below 2 V. And this difference will decrease further with higher f_m. The reliance of the spectral asymmetry on f_m can be explained by (4.10) since

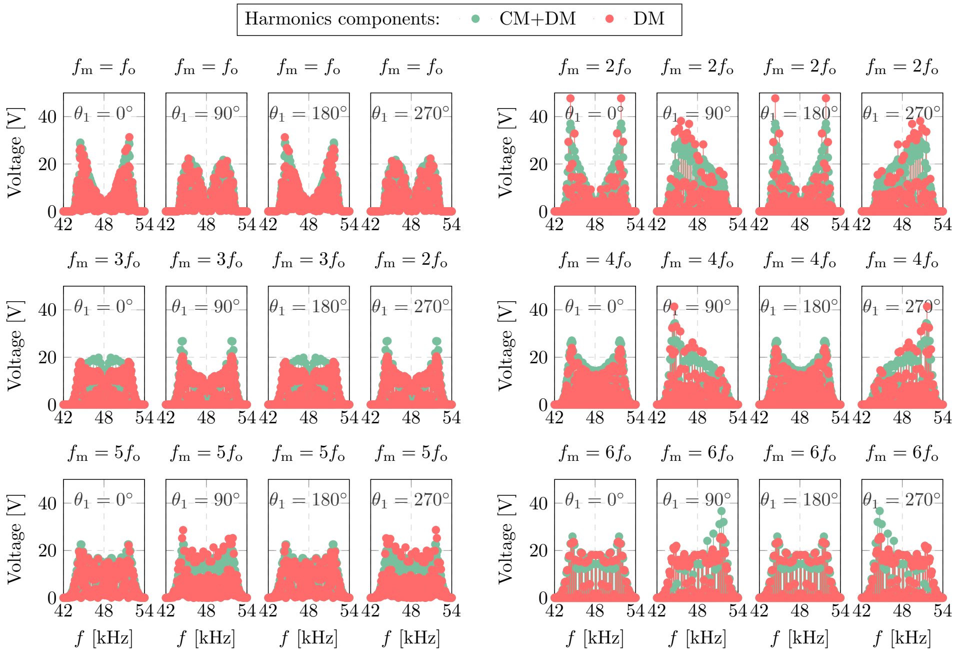


Figure 5.4: 2$^{\mathrm{nd}}$ carrier-frequency harmonic spectrum of one phase (Phase A) under different f_m and θ_1 with frequency profiles determined by (4.7): f_{C0}=24.05 kHz, f_b=6 kHz.

the Bessel function has the following property:

$$J_\mathrm{r}(\zeta) = (-1)^r J_{-\mathrm{r}}(\zeta) \tag{5.3}$$

At the side-band $nf_\mathrm{o} + rf_\mathrm{m}$ and $-nf_\mathrm{o} - rf_\mathrm{m}$, there are infinite combinations of n and k values as expressed by (5.4):

$$\begin{aligned} nf_\mathrm{o} + rf_\mathrm{m} &= n_1 f_\mathrm{o} + r_1 f_\mathrm{m} \\ &= n_2 f_\mathrm{o} + r_2 f_\mathrm{m} \\ &= n_3 f_\mathrm{o} + r_3 f_\mathrm{m} \\ &= \quad \cdots\cdots \\ &= n_i f_\mathrm{o} + r_i f_\mathrm{m} = N f_\mathrm{o} \end{aligned} \tag{5.4}$$

It is noteworthy that the original harmonic band at n is non-zero and has only choices of even numbers [75]. This indicates a new constraint: $\Delta n f_o = -\Delta r f_m$. When f_m is odd multiple of f_o, Δr has to be even numbers which consequently ensures an equal harmonic magnitude at the same positive and negative sidebands based on (4.10) and (5.3). On the contrary, the spectral symmetry is not guaranteed with f_m equal to the even multiple of f_o. For the 2-interleaved PWM converter, odd-order carrier-frequency harmonics are canceled out due to the interleaving operation. Therefore, the symmetry of the even-order carrier-frequency harmonic spectrum is more concerned. The 2$^{\mathrm{nd}}$ carrier-frequency harmonic spectrum of the converter output voltage (phase A) is plotted in

Fig. 5.4 under $\theta_1 = 0°$, $90°$, $180°$ and $270°$ to highlight the differences between Fig. 5.3. It is worth mentioning that (4.7) is adopted for the switching frequency profiles of the three phases. Based on the results, it can be summarized that:

1) The value of θ_1 influences the shape of the voltage harmonics spectrum.

2) Both CM+DM and DM harmonic spectrum of $\theta_1 = 0°$ is symmetrical to that of $\theta_1 = 90°$ with regard to the axis $f = 2f_{c0}$. The same symmetry happens between the spectra of $\theta_1 = 90°$ and $\theta_1 = 270°$.

3) The harmonic spectrum has a larger peak when f_m equals even multiples (2k) of f_o as compared to odd multiples (2k-1).

Specifically for the case $f_m = 6f_o$ depicted in Fig. 5.4, the DM voltage harmonic spectrum generated at $\theta_1 = 90°$ has its peak on the right side of the axis $f = 2f_{c0}$. Consequently, it will lead to smaller current harmonic peaks compared to other cases of θ_1 values under the same filter since the filter attenuates the voltage more with the increase of frequency. Therefore, this shape is preferred from the perspective of minimum filtering inductance for the harmonics emission standard.

5.2.3. IMPACT OF DIFFERENT EV CHARGING POWER CONDITIONS

In a PWM converter connected to a public grid, employing CSFPWM, e.g., SPWM, the switching harmonics are solely governed by the DC link voltage [50], as indicated by (4.13). For both AC on-board and DC off-board fast charging systems, the power electronics structure involves two stages: the grid-connected PFC converter and the isolated DC/DC converter interconnected through the DC link. Charging typically adheres to a CC-CV (constant current-constant voltage) profile, resulting in variable charging power (load power) during operation. Nevertheless, the DC link voltage remains constant during charging, regulated by the PFC rectifier's voltage controller. Consequently, switching harmonics remain consistent across different load power levels.

The PFC converter in the EV charging system is exclusively designed for operation at unit power factor (PF=1), delivering pure active power to the load. Consequently, other power factor scenarios are not addressed in this chapter. Importantly, it should be noted that load conditions with varying power factors have no impact on the generated switching harmonics. This observation can be explained by (4.13), where differences in reactive power under distinct power factors only result in a phase angle shift of the modulation voltage reference, denoted by the shift in θ_o. This shift alters the phase of the switching harmonics as a whole but does not affect the magnitude of the switching harmonics C_{mn}.

Hence, various load conditions exert no influence on the switching harmonics generated through CSFPWM. Consequently, the impact of different load conditions on the switching harmonics generated by P-VSFPWM is identical. This uniform effect arises from the harmonics model of P-VSFPWM, which is established upon and derived from the CSFPWM model, as indicated by (4.10) and (4.11).

5.3. DESIGN GUIDELINE OF P-VSFPWM AND FILTER

Some criteria and guidelines have been developed to assist the AC filter design for the grid-connected VSC using the constant switching frequency PWM [81, 102–104]. The filter parameters are subsequently determined by the constraints defined by the design guidelines. Traditional filter design criteria or guidelines can also be applied with P-VSFPWM although some changes should be adopted due to the spread-spectrum characteristics. In this section, an LCL filter design guideline for P-VSFPWM is devised aiming to not only satisfy the grid harmonic standards but also to keep the good performance of current THD and power efficiency close to what would be attained with the utilization of CSFPWM.

5.3.1. DESIGN CONSTRAINTS FOR AC FILTER

HARMONIC EMISSION STANDARD & CRITICAL HARMONIC

Regarding the standards for supra-harmonics, IEC 61000-4-30 has given informative guidance in Annex C about this frequency range [30]. Useful information about measurement in the supra-harmonics range can be found in IEC 61000-4-7Annex B (2 kHz to 9 kHz) and in CISPR 16 (9 kHz to 150 kHz). Unfortunately, the standard for this frequency range is still evolving and the supra-harmonics emission limits are still under discussion. The suggested harmonic emission limit from the currently available standards such as EN 50065-1 and IEC 61000-3-8 are only used for power line communication. Besides, the IEC 61000-4-19 standard is used for immunity tests for the electrical and electronic equipment against conducted DM disturbances and signaling in the supra-harmonics range but is not especially for the harmonic emission from the power electronic converter [29]. Hence, this work still uses the harmonic emission limits from IEEE 519 for simplicity of demonstration because the main goal of the proposed P-VSFPWM is to show the relative reduction of required inductance under the same standard. The adoption of different standards does not affect this value. In grid-tied applications as a general guideline for harmonic compliance, the AC filters can be designed to meet the harmonic distortion limits established by the IEEE-519-2014, as depicted in Fig. 5.1. In the medium to high switching frequency operated converters the critical spectra content of the grid-side current should be attenuated to be less than the harmonic limit, namely 0.3% and 0.075% of the fundamental current for odd- and even-order harmonics respectively, noted as I_{IEEE519} in this work. The critical harmonic is defined as the most prominent peak harmonic in the current harmonic spectra [105–107]. In constant frequency PWM operation, the output voltage only has a few prominent side-band harmonics appearing in the vicinity of the first switching frequency band (m=1) as depicted in Fig. 5.5. Specifically for SPWM operation, by defining m_{f} as $\omega_{\mathrm{c}}/\omega_{\mathrm{o}}$, the critical frequency is found to be the $(m_{\mathrm{f}}-2)^{\mathrm{th}}$ order of the fundamental frequency since this voltage harmonic results in the largest current harmonic magnitude after the attenuation of the filter. m_{f} is usually selected to be an odd integer so that the critical frequency becomes odd-order harmonic. Thereby, the stricter harmonic limit for the even harmonics can be avoided and the design of the minimum required inductance value is ensured.

Under P-VSFPWM, the voltage harmonics are spread down over a wide frequency range. In a symmetrical (between left and right of the spectrum) carrier-frequency har-

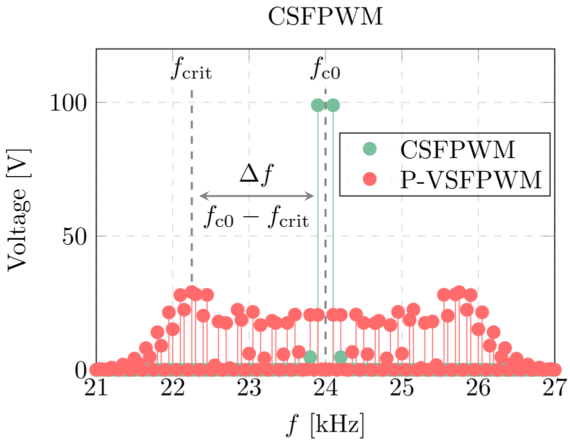


Figure 5.5: Critical harmonic (DM components) under the P-VSFPWM method.

monic spectrum of the converter output voltage, the critical harmonic is the one with the highest magnitude on the left side as depicted in Fig. 5.5 because the filtering attenuation increases with the frequency. However, the spectrum shape might not be symmetrical, due to the various frequency profiles discussed in the previous section. In some extreme cases where the peak voltage harmonic occurs on the right side of the spectrum due to the frequency profile or the harmonics overlap, the critical harmonic is also located on the right side of the centered frequency f_c0. Such a harmonic spectra shape is preferred since it lowers the filtering demand compared to other cases.

CASE OF L FILTER

For L filter, this critical harmonic can be found by:

$$I_{crit} = \left\| i(\omega_\text{crit}) \right\| = max \left\{ \frac{\left\| v_\text{c}(\omega) \right\|}{\omega L} \right\} \tag{5.5}$$

where ω starts from ω_min to infinity. The minimum total required inductance to attenuate the critical harmonic below the emission limit I_IEEE519 set by the supra-harmonics standard is:

$$L_\text{req} = \frac{V_\text{crit}}{\omega_\text{crit} I_\text{IEEE519}}. \tag{5.6}$$

CASE OF LCL FILTER

Neglecting the internal resistance of the inductors and considering no passive damping in the LCL filter, the transfer function from the converter output phase voltage $v_\text{c}(s)$ to the grid-side current $i_g(s)$ is expressed as follows:

$$\begin{aligned}\frac{i_g(s)}{v_c(s)} &= \frac{1}{L_c L_g C_f s(s^2+\omega_{res}^2)} \\ &= \frac{\omega_{res}^2}{L_T s(s^2+\omega_{res}^2)}\end{aligned} \tag{5.7}$$

where L_c and L_g are the converter-and grid-side inductance of the LCL filter respectively. ω_{res} and L_T are the resonance frequency and the total inductance of the LCL filter respectively, and expressed as:

$$\omega_{res} = \sqrt{\frac{L_c + L_g}{L_c L_g C_f}} \tag{5.8}$$

$$L_T = L_c + L_g \tag{5.9}$$

Therefore, the attenuation from the voltage to the grid-side current can be represented by the magnitude of the transfer function (5.7), as follows:

$$Att(\omega) = \left\| \frac{i_g(j\omega)}{v_c(j\omega)} \right\| = \frac{1}{L_T} \cdot \frac{\omega_{res}^2}{\omega \left| \omega^2 - \omega_{res}^2 \right|} \tag{5.10}$$

Equation (5.10) shows the attenuation capability of the LCL filter on the voltage harmonics. The critical current harmonic should be attenuated to be below $I_{IEEE519}$. In other words, the total inductance L_T should be selected to ensure that the critical current harmonic is below the limit set by the standard:

$$Att_{req} = \frac{I_{IEEE519}}{V_{crit}} \tag{5.11}$$

By using (5.10) and (5.11), the minimum required total inductance of the LCL filter for satisfying the standard can be derived as:

$$L_{T-req} = \frac{\omega_{res}^2 V_{crit}}{\omega_{crit} \left| \omega_{crit}^2 - \omega_{res}^2 \right| I_{IEEE519}} \tag{5.12}$$

From (5.12), the minimum required total inductance is proportional to the magnitude of the critical voltage harmonic V_{crit} and approximately inverse to the cubic of the critical frequency. Additionally, the minimum total inductance is also associated with the resonance frequency of the LCL filter. To avoid the instability caused by the filter resonance and to realize a stable grid-side current control, the resonance frequency of the LCL filter should be designed with regard to the so-called critical frequency [108, 109]. The resonance frequency should be larger than one-sixth of the switching frequency to attain the inherent stability without extra damping methods applied [110, 111]. In this work, the resonance-switching ratio $r_f = f_{res}/f_{c0}$ is selected to be 0.219 and remains fixed during the following designs.

As a constraint for the filter design, the maximum AC filter capacitance C_f is limited by the maximum allowable reactive power to be compensated by the VSC which is consumed by this component at the PCC (point-of-coupling). This is important to limit the circulating reactive power which could reduce the converter power efficiency, particularly at partial or low load conditions. Hence, the filter capacitance should fulfill the requirement:

$$C_\mathrm{f} < q \cdot \frac{S_\mathrm{N}}{3\omega_\mathrm{o} V_\mathrm{ac}^2} \tag{5.13}$$

where S_N is the rated power of the system and q is ratio of the device fundamental reactive power and set to 5% in this chapter.

As aforementioned, r_f, namely the ratio between the resonance and switching frequency, is set to be larger than 1/6 to achieve the stability of grid-side current control with the inherent damping under the continuous PWM methods adopted in this chapter [110, 111]. Hence, the extra active damping means can be avoided, which simplifies the potential controller. The converter- and grid-side inductance will be determined subsequently after the value of the total inductance L_T is selected based on (5.12). By combining (5.8) and (5.9), L_c and L_g are derived by:

$$L_\mathrm{c,g} = \frac{L_\mathrm{T}}{2} \pm \sqrt{\frac{L_\mathrm{T}^2}{4} - \frac{L_\mathrm{T}}{\omega_\mathrm{res}^2 C_\mathrm{f}}} \tag{5.14}$$

where the total inductance satisfies

$$L_\mathrm{T} \geqslant \frac{4}{\omega_\mathrm{res}^2 C_\mathrm{f}} \tag{5.15}$$

Besides, the upper limit of the total inductance is constrained by the maximum converter phase voltage and the rated grid-side current by considering the voltage drop of L_T [81].

$$L_\mathrm{T} \leqslant \frac{\sqrt{\frac{V_\mathrm{dc}^2}{6} - V_\mathrm{ac}^2}}{\omega_\mathrm{o} I_\mathrm{g}} \tag{5.16}$$

Usually the larger value in (5.14) is selected for L_c for the purpose of limiting the converter current ripple.

5.3.2. OPTIMIZED DESIGN OF FREQUENCY PROFILE FOR MINIMUM FILTER INDUCTANCE

When P-VSFPWM is adopted, the voltage and consequently the current spectra content across the AC filter are spread differently depending on the switching profiles adopted. Therefore the critical harmonic order $(m_\mathrm{f}-2)^\mathrm{th}$ derived for CSFPWM does not apply to P-VSFPWM due to the varied spectrum. Moreover, the critical frequency can not be found straightforwardly from the non-intuitive spectrum. However, it is noteworthy that the critical frequency is closely associated with the applied switching profile. Fig. 5.5 depicts the critical frequency f_crit and switching frequency variation band f_b in the spectrum plot by using a sinusoidal profile as an example. It is noted that f_crit is related to f_b, and hence, the choice of f_b also influences the design of the total inductance L_T of the LCL filter. Besides, V_crit is not only associated with f_b but also with the periodic frequency f_m. Therefore, the influence of the design variables f_m and f_b on L_T should be investigated before determining the total inductance value.

Based on the spectral analysis in the previous section, the frequency of switching frequency should satisfy:

$$f_\text{m} = 3kf_\text{o} \tag{5.17}$$

where k is a non-zero positive integer value. Similar to the CSFPWM case, the side-band harmonics including the critical harmonic are expected to be placed at an odd harmonic order. If m_f is defined as f_c0/f_o for the P-VSFPWM operation, then the requirement can be expressed as:

$$\begin{cases} nf_\text{o} + lf_\text{m} = (2N-1)f_\text{o} & m_\text{f} \text{ is even} \\ nf_\text{o} + lf_\text{m} = 2Nf_\text{o} & m_\text{f} \text{ is odd} \end{cases} \tag{5.18}$$

where N is the arbitrary integer value. By using (5.17), (5.18) can be simplified as:

$$\begin{cases} n + 3l \cdot k = 2N - 1 & m_\text{f} \text{ is even} \\ n + 3l \cdot k = 2N & m_\text{f} \text{ is odd} \end{cases} \tag{5.19}$$

By analyzing the voltage spectrum with CSFPWM, it has been found that only even side-band harmonics appear in the spectrum, which means that n is an even number. Therefore, the first argument where m_f is eliminated because there exists no such an integer k satisfying the first condition for any values of n and l. The second condition holds if k is selected to be an even number. Hence, the periodic frequency f_m of the switching frequency should satisfy:

$$f_m = 6kf_o \tag{5.20}$$

2-LEVEL CONVERTER WITH LCL FILTER

The critical frequency f_{crit} is obtained by finding the most dominant harmonic by applying a normalized attenuation of the LCL filter to the spectrum of the output voltage. The expression of the normalized attenuation is given by:

$$Att_\text{norm,LCL}(\omega) = \frac{\omega_\text{res}^2}{\omega\left|\omega^2 - \omega_\text{res}^2\right|} \tag{5.21}$$

Hence, the normalized critical harmonic current $I_\text{crit,norm}$ can be found by:

$$I_\text{crit,norm} = max(\left|V_\text{c}(\omega)\right| \cdot Att_\text{norm,LCL}(\omega)) \tag{5.22}$$

The critical voltage harmonic is expressed as:

$$V_\text{c}(\omega) = \sum C_\text{mnl} \tag{5.23}$$

where ω satisfies

$$\omega = 2\pi(mf_\text{c0} + nf_\text{o} + lf_\text{m}) \tag{5.24}$$

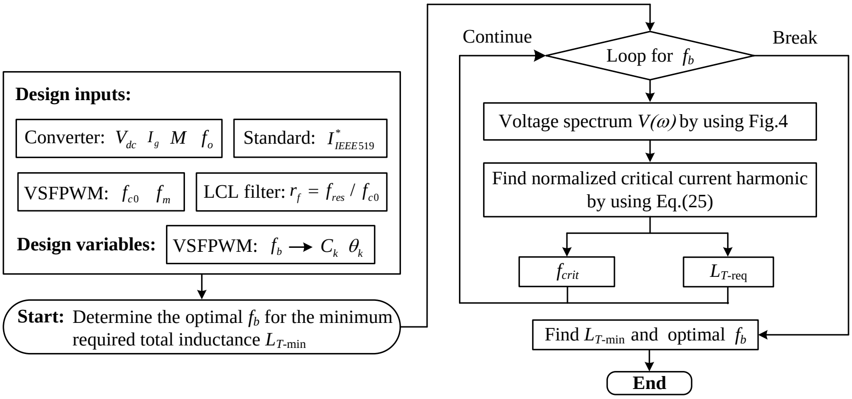

Design inputs:
Converter: V_{dc} I_g M f_o
Standard: $I^*_{IEEE519}$
VSFPWM: f_{c0} f_m
LCL filter: $r_f = f_{res} / f_{c0}$
Design variables:
VSFPWM: $f_b \rightarrow C_k$ θ_k
Start: Determine the optimal f_b for the minimum required total inductance $L_{T\text{-min}}$
Continue
Loop for f_b
Break
Voltage spectrum $V(\omega)$ by using Fig.4
Find normalized critical current harmonic by using Eq.(25)
f_{crit}
$L_{T\text{-req}}$
Find $L_{T\text{-min}}$ and optimal f_b
End

Figure 5.6: Algorithm for optimal f_b to achieve minimum total inductance L_T.

In (5.24), the multiple of the carrier harmonic m is selected to be 1 since the critical harmonic exists in the sidebands of the first carrier harmonic. The critical voltage harmonic then is calculated according to the algorithm described in Fig. 4.11. Finally, the critical frequency f_{crit} hence can be found by retrieving the corresponding frequency from $I_{\text{crit,norm}}$. The distance between the critical frequency f_{crit} and the centered switching frequency f_{c0} is obtained and defined as Δf, as illustrated in Fig. 5.5. The required total inductance $L_{\text{T-req}}$ can be subsequently derived by using (5.12).

In order to find the optimal f_{b} and the consequent minimal $L_{\text{T-req}}$, the algorithm shown in Fig. 5.6 has been proposed. For the certain modulation method and P-VSFPWM profile shape, the algorithm requires the converter specifications such as the rated grid voltage and current V_{g} and I_{g}, the modulation index M and the fundamental frequency f_o. Besides, f_{c0} and f_{m} of the P-VSFPWM, the current harmonic limit, and the filter resonance frequency are also input to the algorithm. The algorithm finds the critical frequency and the associated required total inductance $L_{\text{T-req}}$ for each f_b from a wide range set of values. Finally, the minimum $L_{\text{T-req}}$ can be found by traversing the whole range and the related f_{b}. With the algorithm shown in Fig. 5.6, the relations between f_{b} and Δf are presented in Fig. 5.7. From Fig. 5.7, Δf shows a different staircase quasi-linear relation with f_{b} under the SPWM, 1/4 THIPWM and SVPWM methods. Besides, the minimum required total inductance under various f_b is also found by using the algorithm and presented in Fig. 5.8. Regardless of the modulation method, the required total inductance under the periodic switching profiles always drops with the initial increase of f_{b} and then begins to increase from a certain value of f_{b}. The optimal points giving the maximum inductance drop are summarized in Table 5.1. Compared with the CSFPWM, the sinusoid and triangle periodic profiles lead to a remarkable reduction of the required total inductance. Specifically, the triangle profile can result in a larger reduction compared with the sinusoid profile, which is around 50%–60% depending on the modulation method. Compared with SPWM, both SVPWM and 1/4 THIPWM methods require less total inductance $L_{\text{T-req}}$, but also they feature similar inductance drop tendencies.

Table 5.1: THE DESIGNED OPTIMAL SWITCHING PROFILES FOR A 2-LEVEL CONVERTER WITH LCL FILTER

P-VSFPWM switching Profile	f_b (Hz)	L_{T-req} (μH)
SPWM		
CSFPWM	——	2560
P-VSFPWM sinusoid profile	2400	1115
P-VSFPWM triangle profile	3900	947
1/4 THIPWM		
CSFPWM	——	1330
P-VSFPWM sinusoid profile	1900	772
P-VSFPWM triangle profile	3700	667
SVPWM		
CSFPWM	——	1565
P-VSFPWM sinusoid profile	2200	810
P-VSFPWM triangle profile	3700	710

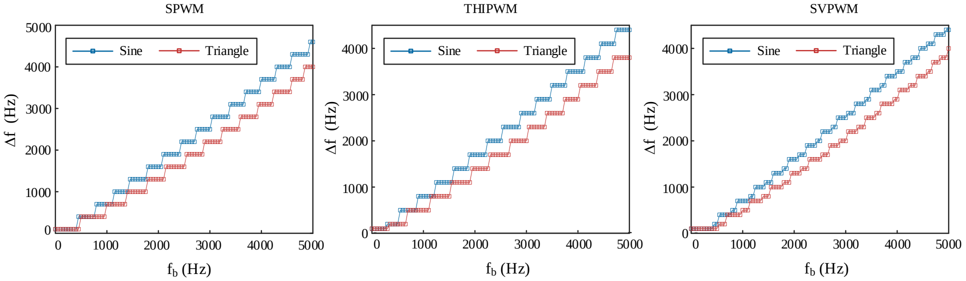


Figure 5.7: The relation between f_b and Δf under various PWM methods and frequency profiles in 2-level converter with LCL filter.

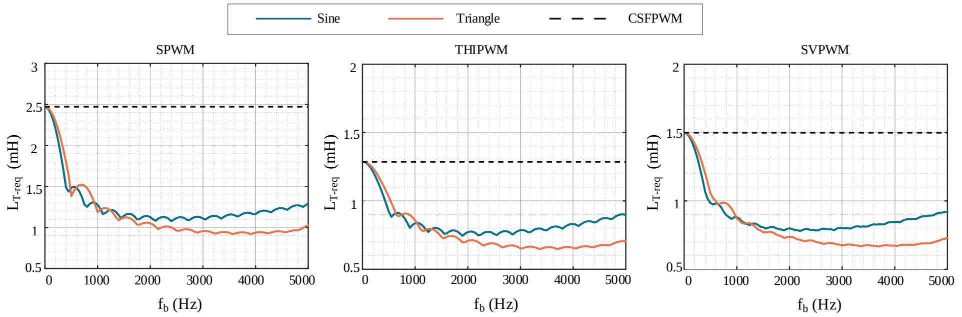


Figure 5.8: The relation between the require total inductance L_T and f_b under various PWM methods and frequency profiles in a 2-level converter with LCL filter.

INTERLEAVED 2-LEVEL CONVERTER WITH L FILTER

The relation between L_{T-req} and f_b is depicted in Fig. 5.9 under the SPWM method with various frequency profiles for interleaved 2-level converter, by using the parameters as

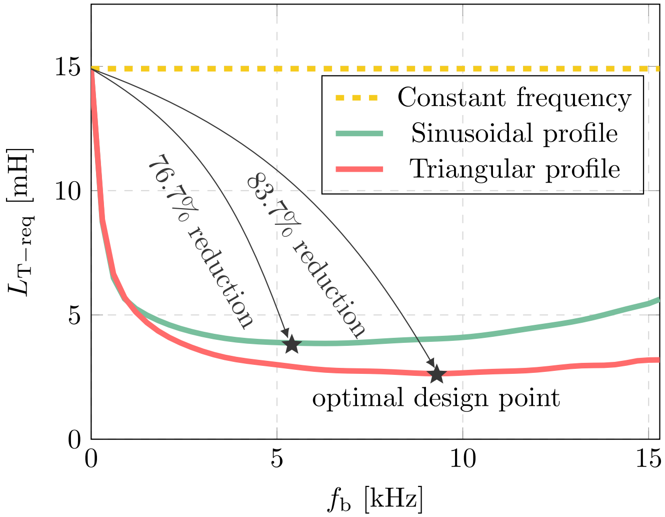


Figure 5.9: The relation between L_T and f_b under the SPWM method with various frequency profiles for interleaved 2-level converter: f_{c0}=24.05 kHz, $f_\mathrm{m} = 6 f_\mathrm{o}$ and $\theta_1 = 90°$.

listed in Table 5.2. It is noteworthy that the required inductance under the periodic switching profiles always begins with a drop and then starts to increase at a certain value of f_b. Therefore, there is a clear minimum $L_{\mathrm{T-req}}$ point for the P-VSFPWM profiles when f_b changes. Both sinusoidal and triangular profiles lead to the reduction of the required inductance compared to the constant frequency profile. More specifically, the triangle profile has a flatter function relation but results in a smaller required inductance value for the L filter compared to the sine profile. The maximum reduction for triangular and sinusoidal profiles are 83.7% and 76.7%, which are achieved at f_b=9300 Hz and f_b=5400 Hz respectively. Although Fig. 5.9 presents only the case of $\theta_1 = 90°$, the value of θ_1 has negligible impact on this relation depicted in Fig. 5.9 based on the analysis in Section 5.2.

TRADE-OFF: CARRIER-FREQUENCY HARMONIC DISTORTION (CHD)

As the trade-off to reshaping the harmonic peak by the P-VSFPWM methods, harmonics that are concentrated at several frequencies are spread over a wide range of frequencies. Based on Carson's rule [18], the energy brought by these harmonics will remain after the frequency changes from CSFPWM to P-VSFPWM. Roughly 98% of the energy is spread over the harmonics residing in the frequency band B_h as depicted in Fig. 5.10, which can be roughly estimated by:

$$B_\mathrm{n} = 2(f_\mathrm{m} + n \cdot f_\mathrm{b}) \tag{5.25}$$

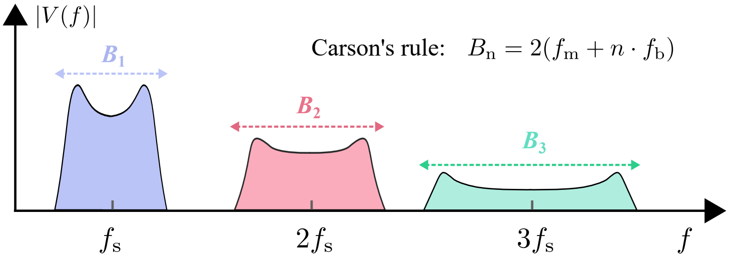

$|V(f)|$
Carson's rule: $B_\mathrm{n} = 2(f_\mathrm{m} + n \cdot f_\mathrm{b})$
B_1
B_2
B_3
f_s
$2f_\mathrm{s}$
$3f_\mathrm{s}$
f

Figure 5.10: Illustration of the Frequency band accommodating 98% harmonics generated by the P-VSFPWM method.

where h is the carrier-frequency harmonic order. In other words, the following relations are satisfied:

$$\begin{aligned} CHD_{\mathrm{v,n}} &= \sum_{h \in B_\mathrm{n}} V^2_{\mathrm{h-VSF}} \approxeq \sum V^2_{\mathrm{h-CSF}} \\ CHD_\mathrm{v} &= \sqrt{\sum_n CHD^2_{\mathrm{v,n}}}. \end{aligned} \tag{5.26}$$

where $CHD_{\mathrm{v,n}}$ measures the voltage carrier-frequency harmonic distortion (CHD) level of certain carrier-frequency harmonic band B_n and CHD_v measures the carrier-frequency harmonic distortion level over the whole frequency range. Under the filter with inductance L, CHD of the current can be similarly derived as:

$$\begin{aligned} CHD_{\mathrm{i,n}} &= \frac{1}{I_1} \cdot \sqrt{\sum_{h \in B_\mathrm{n}} \left(\frac{V_{\mathrm{h-VSF}}}{\omega_\mathrm{h} L}\right)^2} \\ CHD_\mathrm{i} &= \sqrt{\sum_n CHD^2_{\mathrm{i,n}}} \end{aligned} \tag{5.27}$$

where I_1 is the fundamental current component of the converter under the rated power and h is the harmonic order inside the carrier-frequency band B_n. It is important to highlight that CHD essentially reflects the distortion level of the waveform as it encapsulates the root-mean-square (RMS) information of the waveform. Assuming a symmetrical DM voltage harmonic spectrum of the n^{th} carrier-frequency harmonics, by combining (5.25)-(5.27) together it can it can be proved that the $\mathrm{CHD}_{\mathrm{i-n}}$ of the P-SVFPWM is always larger than that of CSFPWM.

In fact, this has also been verified by Fig. 5.11, which sums up the CHD generated by various switching profiles under the SPWM method in the interleaved 2-level VSC till 150 kHz. Since the interleaved 2-level VSC cancels out the odd carrier-frequency harmonics, only second and fourth carrier-frequency harmonics are included in the calculation of CHD considering the supra-harmonics range. It is crucial to emphasize that various P-VSFPWM profiles, including CSFPWM, exhibit an identical level of harmonic distortion in the converter's output voltage, provided they share a centered switching frequency f_{c0}. This has been verified by Fig. 5.11, where the switching frequency (carrier-frequency) harmonics distortion CHD_v remains nearly constant irrespective of the periodic profiles and the frequency variation band f_b. Consequently, voltage harmonics are not a reliable indicator for assessing the harmonics performance of the P-VSFPWM profiles. It can be found in Fig. 5.11 that the $\mathrm{CHD_i}$ under P-VSFPWM is always larger than that of CSFPWM, which corresponds to the previous analysis. With the increase of f_b, $\mathrm{CHD_i}$ always increases, which is the trade-off for the reduced current harmonic peak brought by P-VSFPWM. Therefore, the current instead of voltage harmonics are analyzed in this chapter to evaluate different P-VSFPWM profiles. According to Fig. 5.9, $\mathrm{CHD_i}$ is 2.63% and 2.49% respectively for the selected optimal profiles, which was only increased by 12.4% and 6.4% as compared to 2.34% $\mathrm{CHD_i}$ of CSFPWM.

IMPACT AND LIMITATION OF P-VSFPWM OPTIMIZATION

In addition to addressing CHD, it's important to consider other trade-offs and potential negative impacts associated with this optimization process. These include the possibility of overlapped harmonic spectra and low-frequency resonance issues. Harmonic overlap becomes more likely when the frequency variation band f_b is sufficiently large. Low-frequency resonance can occur when the centered frequency f_c0 is low, and f_b is large enough, potentially leading to interactions between the first carrier-frequency switching harmonic and the LC or LCL filter resonance. Fortunately, these side effects have been effectively mitigated through the adoption of an interleaved topology and the use of an L filter in this work.

The proposed optimization is only applicable to the PWM converter implementing P-VSFPWM or other spread-spectrum techniques. The PWM converters e.g., two-level, multi-level, cascaded H-bridge (CHB), and modular multi-level converters can be analyzed by the DFA approach and the switching harmonic model for CSFPWM can be subsequently obtained in a similar way. The same mathematical manipulations from Eq.4.8

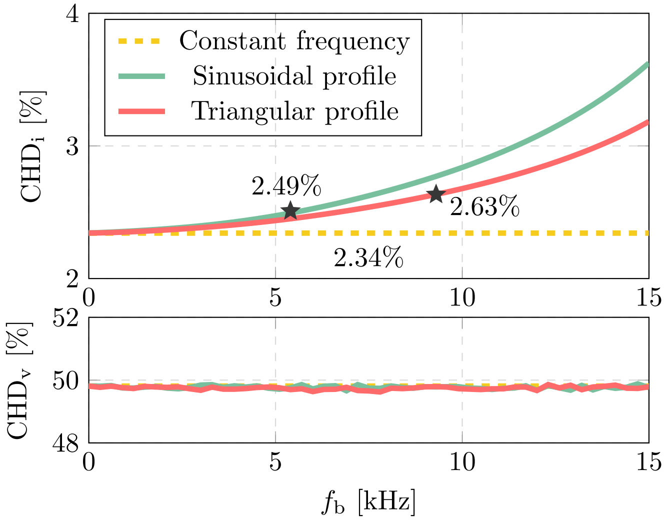


Figure 5.11: The current and voltage CHD of the interleaved 2-level converter under the SPWM method with various frequency profiles: f_c0=24.05 kHz, $f_\mathrm{m} = 6f_\mathrm{o}$ and $\theta_1 = 90°$.

to Eq.4.10 can be used to derive the switching harmonics model in triple-summation form for these topologies implementing P-VSFPWM. The attenuation (or admittance) of the filter e.g, L, LC, LCL, and even higher order types changes opposite to V_{crit} as f_{b} varies, indicating the existence of the minimum $L_{\text{T−req}}$.

LOSS ANALYSIS OF P-VSFPWM PROFILE

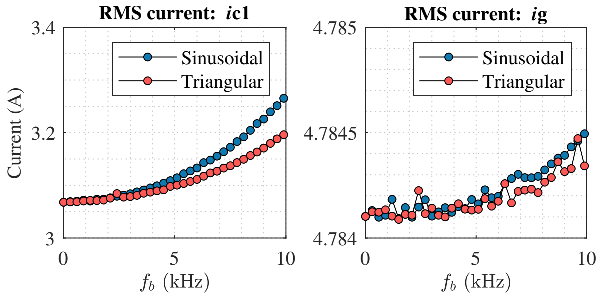
The root-mean-square (RMS) current, semiconductor loss, and inductor loss are obtained based on the time-based simulation results in MATLAB and presented in Fig. 5.12. The adoption of P-VSFPWM results in a higher switching ripple, leading to increased RMS currents. Fig. 5.12(a) demonstrates that P-VSFPWM profiles influence converter-side RMS current similarly to current CHD. The grid-side current i_{g} experiences a negligible change due to the large grid-side filter inductance L_{g}. Conduction loss associated with RMS current follows a similar increasing trend as f_{b}. In contrast, switching losses decrease with increasing f_{b}. The switching energies $E_{\text{on,off,rr}}$ are interpolated from the IGBT datasheet and expressed as second-order polynomial functions, whose coefficients are a, b, and c. Assuming an ideal current $i(t) = I\sin(\omega_{\text{o}}t+\varphi)$, the switching loss under the proposed P-VSFPWM profile can be modeled as:

$$P_{\text{sw}} = P_{\text{sw0}} + \frac{4V_{\text{dc}}}{2\pi V_{\text{b}} b I}\sum_{k=1}^{\infty}\frac{C_{\text{k}}\sin(6k\varphi-\theta_{\text{k}})}{36k^2-1} \tag{5.28}$$

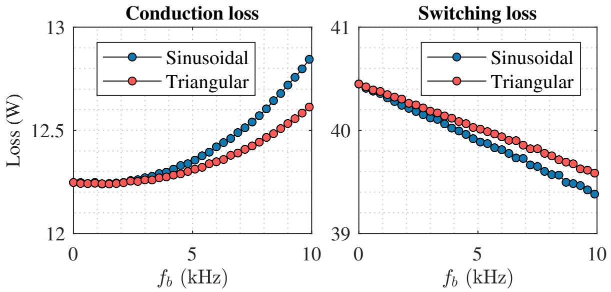
where P_{sw0} is the switching loss under CSFPWM and V_b is the reference voltage in the datasheet. It is noteworthy that P-VSFPWM results in an additional term in the switching loss, which can be negative with certain P-VSFPWM profile and power factor angle. The P-VSFPWM design selected in this chapter leads to a smaller switching loss as compared to CSFPWM as $\varphi = 0$ (PFC operation) and $\theta_{\text{k}} = 90°$, which corresponds to the simulated switching loss. The inductor model incorporates core loss using iGSE (improved Steinmetz equation) and winding loss considering skin effect and proximity effect [112]. Inductor losses increase with f_{b} similar to current CHD, reflecting the relationship between core loss, winding loss, and current harmonics. However, for the grid-side inductor L_{g}, loss increment is minimal, remaining virtually unchanged with increasing f_{b}. Grid-side current, with fewer harmonics, exhibits less influence (minimal increase in RMS current) with f_{b}. Winding loss dominates in the grid-side inductor, primarily determined by winding resistance and the fundamental current component. This clarifies the reason why the measured efficiency of the converter under CSFPWM and P-VSFPWM profiles are quite close, as the decreased switching losses are balanced out due to the increased conduction losses and inductor losses.

5.3.3. SIMULATION AND EXPERIMENTAL VERIFICATION

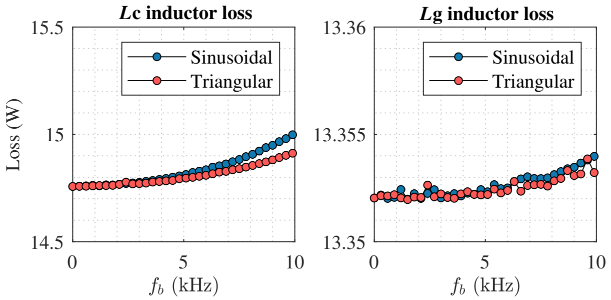
To verify the optimal switching profiles for the minimum required inductance, both simulation and experimental tests are conducted in the three-phase 2-level and interleaved 2-level VSC converters. Firstly, a PLECS-based simulation is carried out. Thereafter, the adopted periodic switching profiles are realized on a digitally-controlled hardware platform as shown in Fig. 5.13 with the DSP TMS320F28379D from Texas Instruments. The key specifications of the converter prototypes can be found in Chapter. 2. The conducted experiments use a 5 kW-rated prototype of the three-phase 2-level converter with an LCL



(a) RMS currents.



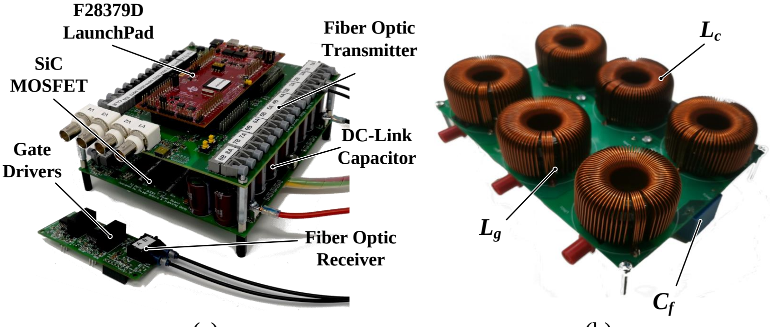
(b) Semiconductor device losses.



(c) Inductor losses.

Figure 5.12: Modeled losses under the P-VSFPWM profiles.

filter shown in Fig. 5.13. Additionally, a 10 kW-rated prototype based on the three-phase interleaved 2-level converter with an L filter was employed, as illustrated in Fig. 5.14. Therein, for the power semiconductors, three hard-paralled SMD packaged 900 V Silicon Carbide (SiC) MOSFETs are used per necessary active switch in the 2-level converter prototype. The power semiconductors employed for the interleaved 2-level converter consist of twelve 1200 V class discrete IGBTs (IKW15N120BH6) provided by Infineon Tech-



(a) (b)

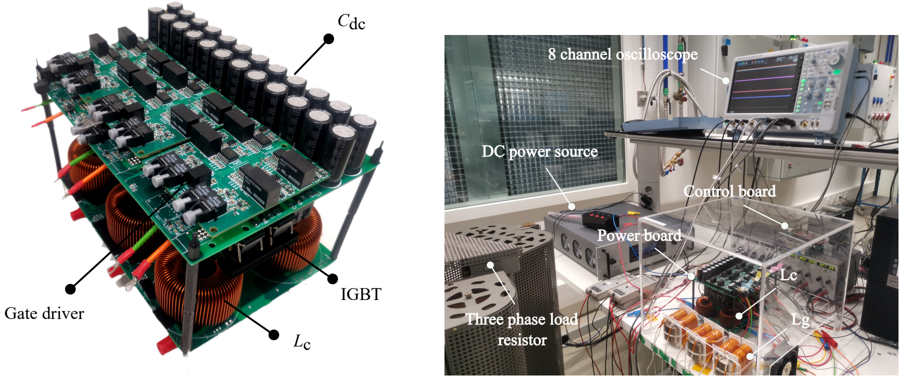
Figure 5.13: Experimental setup: (a) 2-level converter and control board; and (b) LCL filter.

nologies, with anti-parallel diodes. For thermal management, natural convection PCB-mounted heat sinks are employed to maintain safe device junction temperatures. The control system is facilitated by a 200 MHz dual-core Micro Controller Unit (MCU) from Texas Instruments, integrated into a LaunchPad development kit. A master PC controls the programmed operating modes within the MCU through a USB communication link. Importantly, this link is electrically isolated using an XDS100v2 debug probe for safety and precision. Furthermore, to ensure a high Common-Mode Rejection Ratio (CMRR) and prioritize safety, the control and power boards are interconnected via optical fiber links. In implementing the conventional d-q controller, all necessary Analog-to-Digital Conversions (ADC) of inverter-related measurements—such as AC converter and grid-side terminal currents, AC grid voltages, and DC terminal voltages—are carried out on the power board using 10 MHz delta-sigma modulators. The acquired data is then transmitted to the MCU's sigma-delta filter channels via a 50BMd fiber optic transmitter. The

Table 5.2: System parameters for experiment.

Converter	V_{dc}[V]	V_{ac}[V]	f_{o}[Hz]	f_{c0}[kHz]	L_{c}[μH]	L_{g}[μH]	C_{f}[μF]
2-level	700	$\sqrt{2}\cdot230$	50	24.05	370	360	5
Interleaved 2L	700	$\sqrt{2}\cdot230$	50	24.05	340	2280	/

LCL filter board depicted in Fig. 5.13(b) is built with two toroidal-core inductors with 370 μH and 360 μH respectively, which are measured with an impedance analyzer. A film capacitor of 5 μF is used as the AC filter capacitor. The component value selection was devised using the design results presented in Fig. 5.8 while considering the P-VSFPWM strategy employing 1/4 THIPWM and triangular frequency profile. As it will be shown in the following this strategy leads to the smallest requirement of L_T for the operational condition listed in Table 5.1. For the interleaved 2-level converter, the two toroidal-core inductors are adopted as the inductor L_{c} at the output of the bridge leg. The grid-side inductor L_{g} is built with Amorphous cut-core (AMCC, also called Metglas) material and litz wire, and rated as 2.28 mH. The component value selection was devised using the



(a) 10-kW interleaved 2-level converter.

(b) Experimental test-bench.

Figure 5.14: Interleaved 2-level converter prototype and experimental test-bench.

design result presented in Fig. 5.9 while considering only the SPWM method and triangular profile. In experiments, the three-phase two-level converter is operated in the inverter mode operating at full power factor at PCC. All of the experimental waveforms and data used in this chapter are recorded by the oscilloscope YOKOGAYA DLM2054, and the current THD and power conversion efficiency of the converter are tested by the power analyzer YOKOGAYA WT500.

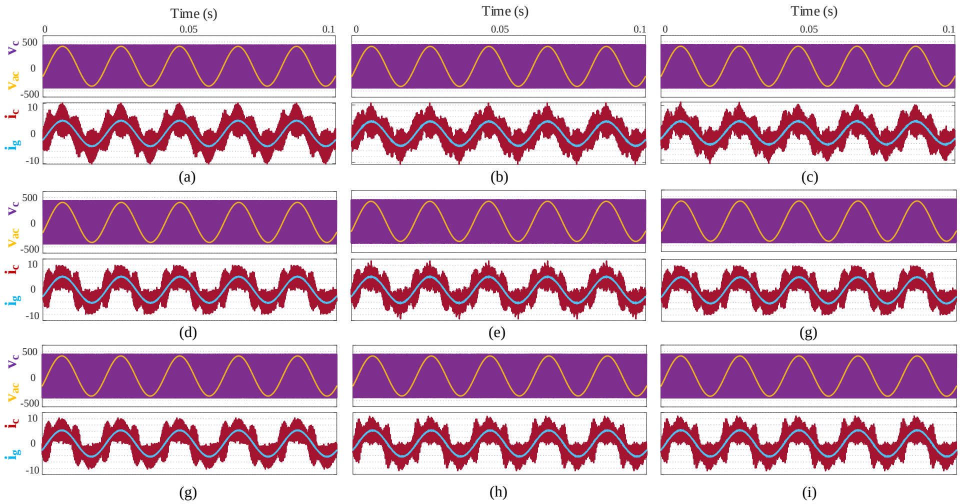
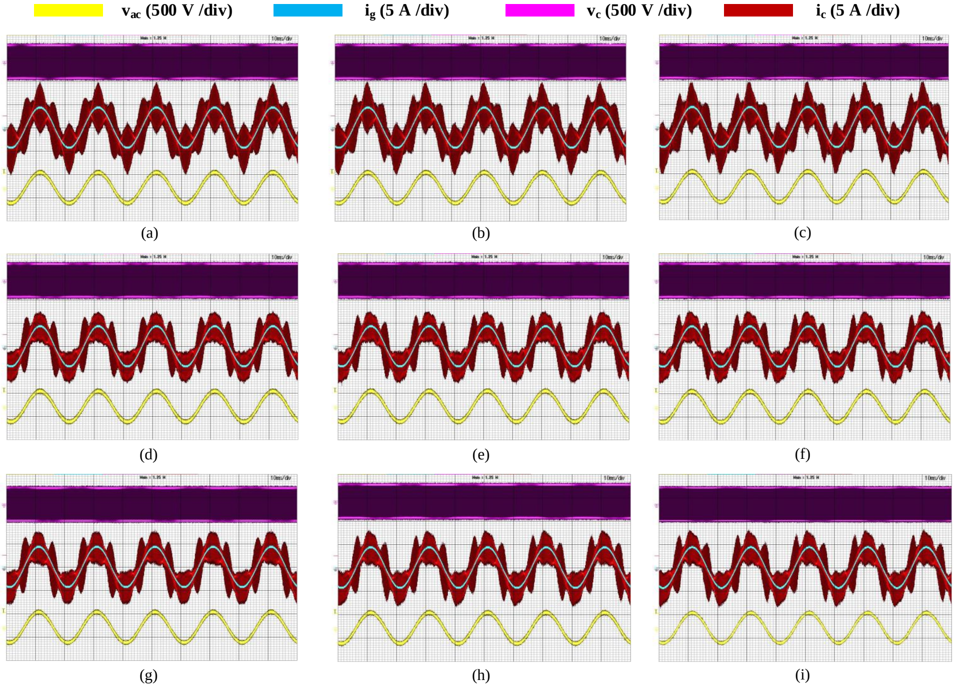


Figure 5.15: Simulation results of the three-phase three-wire two-level converter under various switching profiles and PWM methods: (a) SPWM—constant switching frequency (b) SPWM—sinusoid profile: f_b=2400 Hz (c) SPWM—triangle profile: f_b=3900 Hz (d) THIPWM—constant switching frequency (e) THIPWM—sinusoid profile: f_b=1900 Hz (f) THIPWM—triangle profile: f_b=3700 Hz (g) SVPWM—constant switching frequency (h) SVPWM—sinusoid profile: f_b=2200 Hz (i) THIPWM—triangle profile: f_b=3700 Hz. Note that only one of the three-phase waveforms is recorded.

The correctness of the analytical P-VSFPWM spectrum model has already been verified in Chapter 4 by comparing the analytical harmonic spectra with the simulation and experimental results. Besides the validation of the P-VSFPWM spectrum model, the design of the optimal switching profile is also validated by the simulation and experimental tests. The nine different switching profiles listed in Table 5.1 are examined by both simulation and experiment. The parameters in Table 5.2 are used for both the simulations and experiments.

2-LEVEL CONVERTER WITH LCL FILTER

Fig. 5.15 shows the simulation results of the converter output voltage v_c, converter-side current i_c, grid-side current i_g and the AC voltage v_{ac} under the nine designed switching profiles listed in Table 5.1. The AC voltage v_{ac} has a peak value of 325 V while the grid-side current has a peak value of 4.3 A. It can be seen that the periodic switching profiles work well under various PWM methods. The current ripples in the converter-side inductors are significantly attenuated by the adopted LCL filter and the grid-side current i_g exhibits a good sinusoidal waveform with low THD. Fig. 5.16 presents the experimen-



(a) (b) (c)

(d) (e) (f)

(g) (h) (i)

Figure 5.16: Experimental results of the three-phase three-wire two-level converter under various switching profiles and PWM methods: (a) SPWM—constant switching frequency (b) SPWM—sinusoid profile: f_b=2400 Hz (c) SPWM—triangle profile: f_b=3900 Hz (d) THIPWM—constant switching frequency (e) THIPWM—sinusoid profile: f_b=1900 Hz (f) THIPWM—triangle profile: f_b=3700 Hz (g) SVPWM—constant switching frequency (h) SVPWM—sinusoid profile: f_b=2200 Hz (i) THIPWM—triangle profile: f_b=3700 Hz. Note that only one-phase waveforms are recorded.

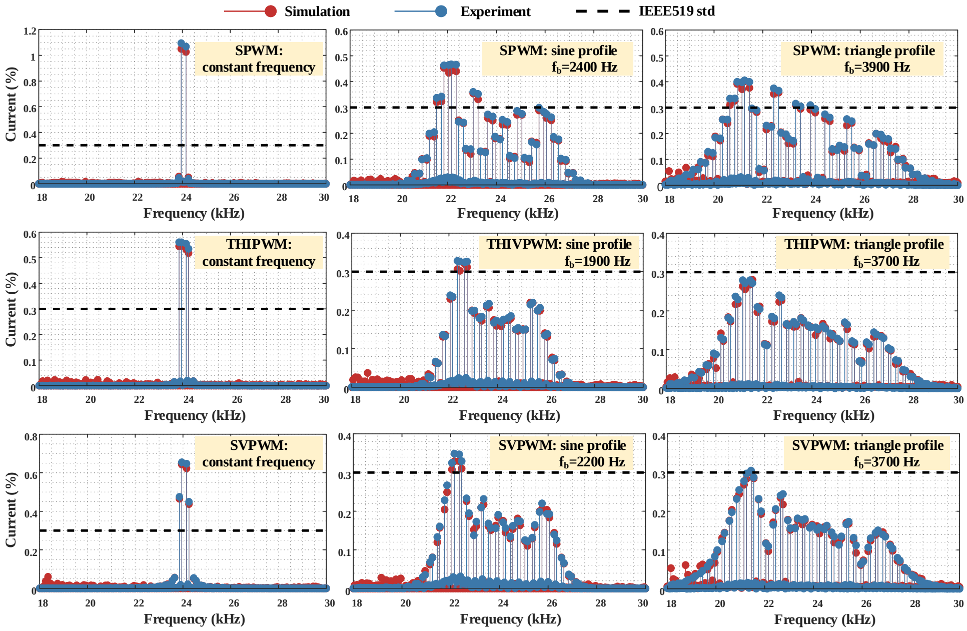


Figure 5.17: The grid-side current harmonic spectrum of the 1st carrier frequency side-bands, derived from the experimental and simulation results.

tal results of the three-phase two-level inverter under the designed switching profiles. The experimental converter output phase voltage v_c, the converter-side current i_c, the grid-side current i_g and the AC voltage v_ac match well the simulation results in terms of waveforms and values. From the results, it can be seen that the switching harmonics in the currents are significantly attenuated by the adopted LCL filter. However, in order to validate the effectiveness of the implemented filter and switching profiles, the grid-side current spectra are required for further analysis. By extracting the data of the grid-side currents from both the simulation and experiment results, their corresponding spectra are obtained and subsequently depicted in Fig. 5.17 in comparison to the limits defined by the current harmonic standard.

First, it can be clearly seen that the two current spectra obtained from the simulation and experiment results match each other with good accuracy under the various PWM methods and switching profiles. The results of the normalized critical current harmonic are summarized in Table 5.3 for the intuitive comparison. By comparing the results for different switching profiles with certain modulation methods, it is found that the critical current harmonic drops significantly with P-VSFPWM profiles compared with CSF-PWM. Specifically, the triangle profile results in the largest reduction (more than 50%) of the critical current harmonic. Besides, a negligible increment of the THD (Total Harmonic Distortion) is observed in the grid-side current when the P-VSFPWM profiles are implemented compared to the relevant CSFPWM. Meanwhile, as shown in Table 5.3, the system efficiency also remains nearly unchanged with the implemented P-VSFPWM profiles. Additionally, it can be noted that the 1/4 THIPWM method has the overall best

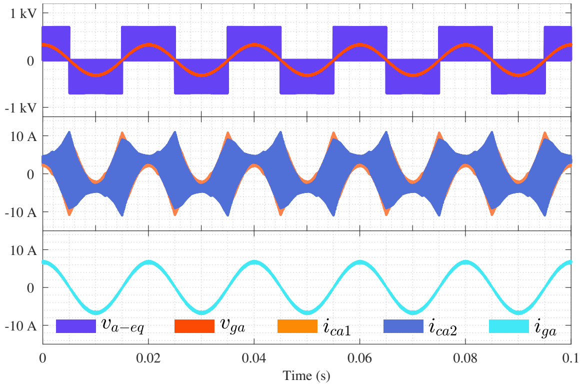
Table 5.3: THE FILTERING INDUCTANCE REQUIRED BY THE IEEE519 STANDARD

Switching Profile	I_{crit} (%)		THD (%)	Efficiency (%)
	Simulation	Experiment	Experimental Measurement	
SPWM				
CSFPWM	1.05	1.07	1.14	98.00
Sinusoid: f_b=2400 Hz	0.453	0.463	1.19	97.86
Triangle: f_b=3900 Hz	0.402	0.408	1.19	97.80
1/4 THIPWM				
CSFPWM	0.545	0.560	1.00	98.00
Sinusoid: f_b=1900 Hz	0.320	0.325	1.07	98.03
Triangle: f_b=3700 Hz	0.267	0.280	1.06	97.94
SVPWM				
CSFPWM	0.642	0.654	1.00	98.05
Sinusoid: f_b=2200 Hz	0.33	0.345	1.04	98.02
Triangle: f_b=3700 Hz	0.292	0.298	1.04	98.07

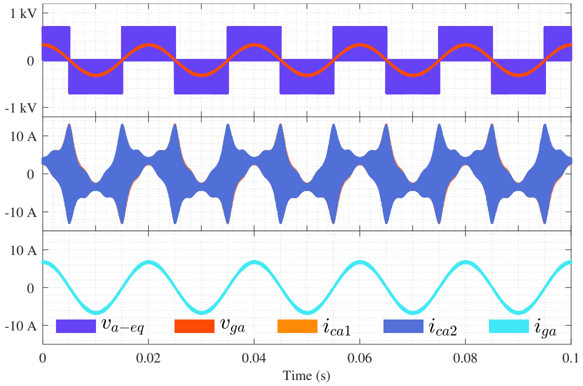
current harmonic performance compared with SPWM and SVPWM when the same filter and switching profile are used. More specifically, the 1/4 THIPWM with the triangle profile (f_b) shows the minimum critical current harmonic compared with the rest switching profiles under the same LCL filter. In other words, 1/4 THIPWM demands the minimum inductance for the LCL filter to achieve the same current harmonic performance. Therefore, the 1/4 THIPWM with a triangle switching profile is regarded as the optimal design choice for the implemented system. Besides, it can be seen that the experimental critical current harmonic values are slightly larger than the simulation ones for all the switching profiles. This implies that the total inductance of the LCL filter used in the experiment is slightly smaller than 730 μH. This small difference is acceptable considering the possible variation of core permeability with the current bias during the practical implementation of the LCL filter. Therefore, it can be concluded that the P-VSFPWM following the suggested LCL filter design guideline developed in the previous section does not substantially influence the THD and efficiency of the system while remarkably lowering the critical harmonic of the grid-side current.

INTERLEAVED 2-LEVEL CONVERTER WITH L FILTER

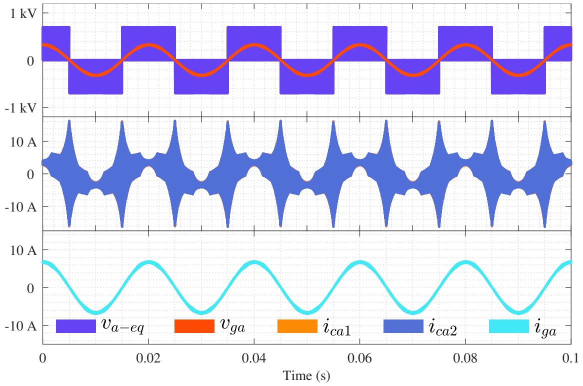
The optimal switching profiles leading to the minimum requirement of L_T are listed in Table 5.4. The simulation and experimental waveforms under the optimal switching profiles at 3.3 kW load power are presented in Fig. 5.18 and Fig. 5.19 respectively. The experimental results closely resemble the simulation waveforms across all profiles. Nevertheless, there is a slight variance between the experimental and simulation results for i_{ca1} and i_{ca2} when the load current reaches its peak. This discrepancy can be attributed to the inherent differences between the two inductors, L_c, in the interleaved bridges. In practice, these inductors are not perfectly identical due to manufacturing and materials variations. Both simulated and experimental harmonic spectra of the grid-side current under the optimal profiles are depicted in Fig. 5.20 for a better comparison against the



(a) Waveforms under CSFPWM.

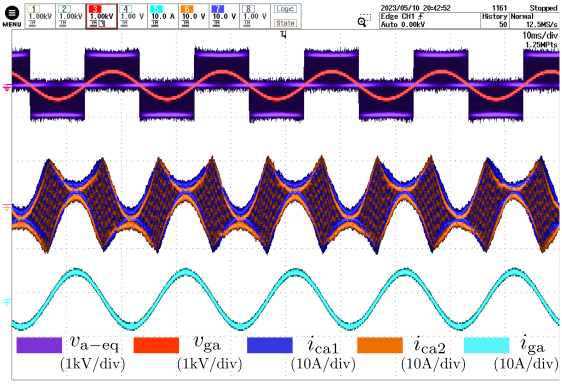


(b) Waveforms under the optimal sinusoidal profile.

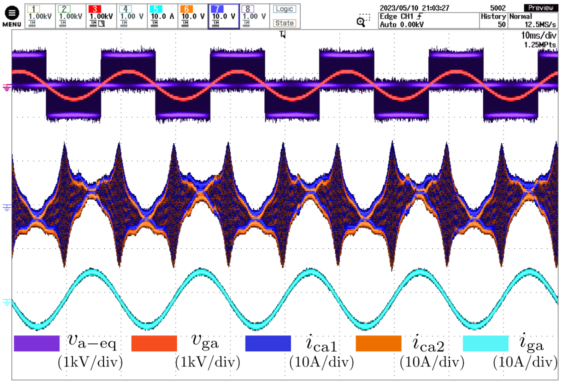


(c) Waveforms under the optimal triangular profile.

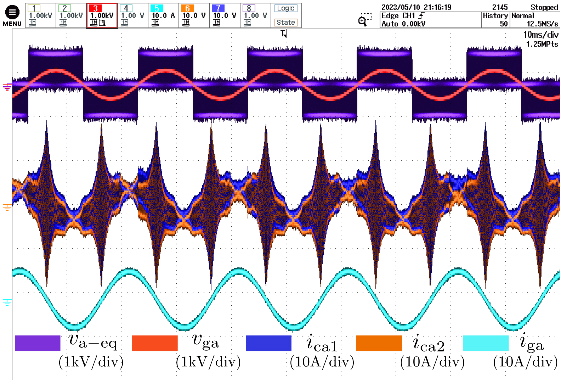
Figure 5.18: Simulation waveforms of the three-phase interleaved 2-level converter under the optimal profiles listed in Table 5.4.



(a) Waveforms under CSFPWM.



(b) Waveforms under the optimal sinusoidal profile.



(c) Waveforms under the optimal triangular profile.

Figure 5.19: Experimental waveforms of the three-phase interleaved 2-level converter under the optimal profiles listed in Table 5.4.

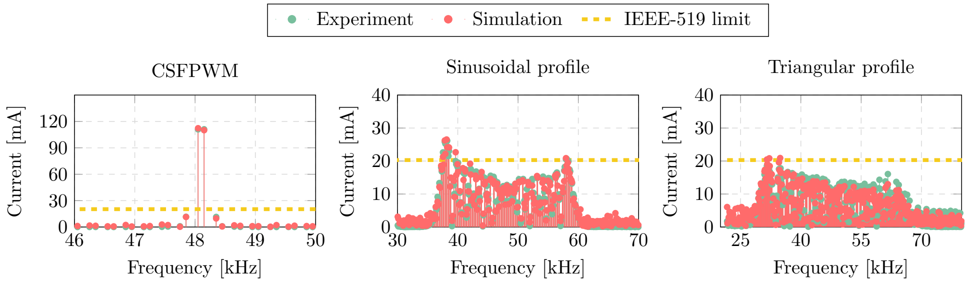


Figure 5.20: Spectra comparison between analytical, simulation and experimental results: The current harmonic spectra (Phase A) of the interleaved 2-level converter under f_{C0}=24.05 kHz, f_b=2 kHz, $f_m = 6f_o$.

IEEE-519 emission limit. Table 5.4 records the critical harmonic with regard to the rated load peak current. Compared to other cases, the current harmonics generated by the triangular profile match the emission limit of 0.3% set by the IEEE-519. The I_{crit} for triangular profile is 5 times smaller than that of CSFPWM. In other words, 5 times smaller inductor can be adopted to the triangular profile to achieve the same critical current harmonic peak compared with CSFPWM. The total rated-current distortion (TRD) [113] is used in this chapter to evaluate the low-order harmonics distortion level, which calculates the total root-sum-square of the current distortion components in percentage of the converter-rated current instead of load current. The measured TRD from experiment results are larger than the simulated ones in all cases. This difference could be caused by the non-ideal DC voltage source, asymmetry of the three-phase circuitry parameters, and slightly unbalanced three-phase load. However, it can be noted that the TRD values for all three cases are close to each other, which indicates a negligible impact on the TRD from the P-VSFPWM methods. Regarding the CHD analysis, it is worth noting that the experimental results show slightly higher values than the simulated ones. This discrepancy may arise from the high-frequency noise that the oscilloscope recorded during the experiments. Similarly, the CHD values for sinusoidal and triangular profiles are marginally higher than those for Constant Switching Frequency PWM (CSFPWM), which is a trade-off for reducing harmonic peaks. Both simulation and experimental waveforms clearly indicate that periodic switching profiles result in higher current ripple in the converter output current (i_{ca1} and i_{ca2}) compared to CSFPWM. This ripple increases as the frequency variation band f_b increases. In summary, it can be concluded that P-VSFPWM significantly reduces the required inductance at a minor expense in terms of CHD and current ripple.

The converter system efficiency under the three switching profiles remains almost unchanged, which are 97.12%, 97.09%, and 97.07% respectively. This indicates that the selected periodic switching profiles will not lead to extra switching losses, which is also proven in [22]. However, the periodic switching profiles result in higher switching ripples which can lead to higher semiconductor conduction loss and inductor loss, which can explain the slight decrease in efficiency under the sinusoidal and triangular profiles.

Table 5.4: RECORDS FOR THE OPTIMAL PROFILES SHOWN IN FIG. 5.9.

Switching Profile	I_{crit}* (%)		TRD* (%)		CHD (%)		η* (%)
	Simu*	Exp*	Simu	Exp	Simu	Exp	Exp
CSFPWM							
f_{c0}=24.05 kHz	1.642	1.756	0.121	0.522	2.478	2.863	97.12
Sinusoidal							
f_b=5400 Hz	0.387	0.392	0.092	0.523	2.543	2.913	97.09
Triangular							
f_b=9300 Hz	0.2844	0.309	0.1183	0.657	2.637	2.948	97.07

* I_{crit} refers to the ratio between the critical current harmonic and the rated load peak current.
* TRD is the total rated-current distortion and calculates the low-order harmonics till 2 kHz.
* Simu and Exp refer to the simulation and experiment results.
* η refers to the tested system efficiency.

5.4. MITIGATION OF HARMONICS OVERLAP

5.4.1. INTERLEAVED P-VSFPWM

The harmonic overlap between different carrier-frequency harmonic bands usually results in an enhanced harmonic peak in the output voltage of the PWM converter. In normal cases, this enhanced harmonic peak is not concerned for quite some cases because the critical harmonic still appears in the left half part of the 1st carrier-frequency harmonic band after the overlap between 1st-and 2nd-carrier frequency harmonic bands. However, in other scenarios for instance the spectrum under $f_m = 2f_o$, $\theta_1 = 270°$ shown in Fig. 5.4, the overlap between the different harmonic bands increases the critical harmonic by a considerable amount as depicted in Fig. 5.21. In fact, several approaches can be adopted to avoid or minimize this effect. Firstly, f_m can be selected to be large enough so that the spectrum shape becomes quasi-symmetrical, which is proved by Fig. 5.4. Hence the critical harmonic is located in the left half-part of the spectra regardless of the overlap. Another alternative method is to adopt the LCL filter instead of the L filter. The

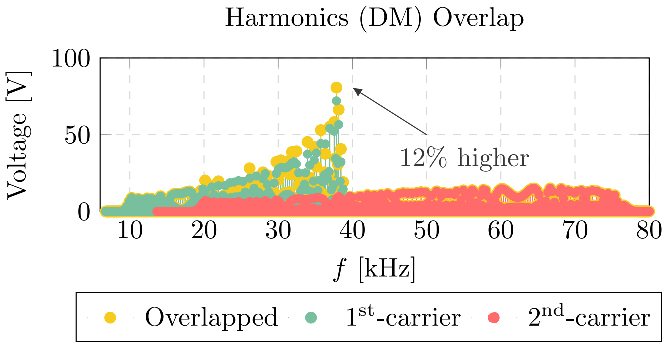


Figure 5.21: Overlap from 1st and 2nd carrier-frequency harmonics.

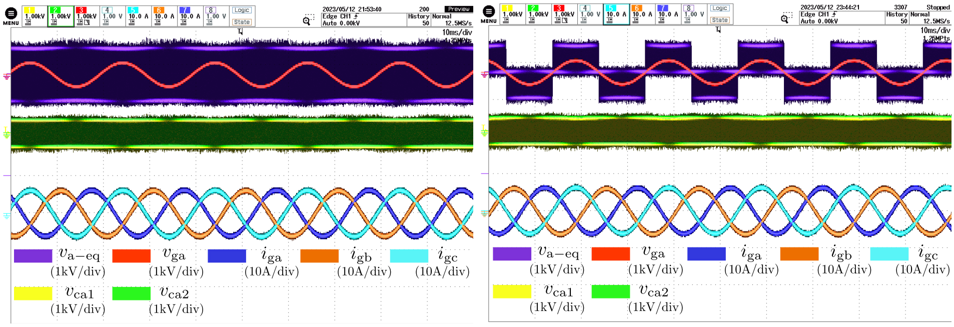
critical voltage harmonic located at the right half-part will be shifted to the left side by the much higher attenuation brought by the LCL filter. Hence, the harmonic increment caused by overlap is not critical for filter design. However, these approaches can not be applied to applications where the profile and passive elements are already selected and fixed for specific purposes such as ZVS operation.

This work adopts the interleaved circuit structure which can cancel out the odd harmonic bands to avoid the harmonics overlap. Meanwhile, the profiles and operations used for the non-interleaved topology still apply to the interleaved circuit. In this interleaved operation, the switching profile used for the original operation should be halved, for instance, f_{c0} = 48.05 kHz, f_b = 32 kHz becomes f_{c0} = 24.05 kHz, f_b = 16 kHz so that the semiconductor switching losses can be minimized for this interleaved operation. Hence, the only trade-off of this method is the circuitry complexity due to the doubled number of switches.

5.4.2. SIMULATION AND EXPERIMENTAL VERIFICATION

In order to verify the effectiveness of the interleaving in mitigating the harmonics overlap due to the large variation of the frequency band f_b under some common P-VSFPWM operations for instance the ZVS operation conducted by [8]. In this case, the sinusoidal switching profile with $f_m = 2f_o$ and $\theta_1 = 270°$ are adopted in order to realize ZVS operation for both positive and negative cycles of the fundamental period. Therefore, $f_m = 2f_o$, f_{C0}=48.05 kHz, f_b=16 kHz and $f_m = 2f_o$, f_{C0}=24.05 kHz, f_b=8 kHz are used for hard-paralleling and interleaving operations respectively. The experimental waveforms are shown in Fig. 5.22 for both operations. By conducting FFT analysis on the harmonic spectra of the three-phase grid currents, the current spectra are obtained and depicted in Fig. 5.23 for a clear comparison.

Firstly, the experimental current harmonic spectra match the simulated ones with quite good accuracy. Besides, the current harmonic peak has been significantly reduced from 65 mA to 16 mA, which is roughly a 75% reduction. Meanwhile, both TRD and CHD



(a) Hard-paralleling: $f_m = 2f_o$, f_{C0}=48.05 kHz, f_b=16 kHz

(b) Interleaving: $f_m = 2f_o$, f_{C0}=24.05 kHz, f_b=8 kHz

Figure 5.22: Experimental waveforms with the sinusoidal switching profile under two different operations: (a) hard-paralleling (b) interleaving.

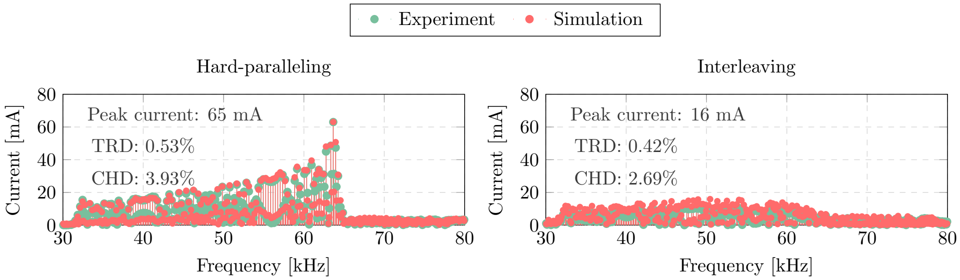


Figure 5.23: Experimental and simulated grid current harmonic spectra under hard-paralleling and interleaved operations.

in interleaved operation have a considerable drop compared with hard-paralleling operation. It is also noteworthy that the semiconductor losses under the two cases will be similar since the switching frequency is halved for interleaved operation and the converter remains to be identical.

It is also worth mentioning that the selected converter might not be the optimized design for the hard-paralleling operation in terms of ratings and semiconductor loss metrics. If the non-interleaving operation is directly applied to an optimized conventional three-phase 2-level VSC based on 6 switches instead of using hard-paralleled topology, the harmonics performance will still remain the same as shown in Fig. 5.23. However, the power losses of the two converters will depend on the selection of the power components.

5.5. CONCLUSION

In summary, this chapter provides a detailed analysis of the impact of periodic variable switching frequency modulation (P-VSFPWM) profiles on harmonic spectra. By conducting a comprehensive harmonic spectral analysis, the influence of different switching profiles on harmonic symmetry is elucidated, leading to the identification of optimal profiles that minimize required inductance while meeting IEEE-519 standards. Simulation and experimental validation confirm the superiority of triangular profiles, requiring significantly smaller inductance compared to CSFPWM. However, implementation of P-VSFPWM results in increased current harmonic distortion (CHD) and other trade-offs. Additionally, experimental results highlight the effectiveness of interleaved operation in reducing harmonic overlap and improving harmonic performance, as evidenced by total harmonic distortion (TRD) and CHD metrics.

6

CONTROLLER DESIGN FOR PFC CONVERTER

The chapter discusses the implementation of LCL filters in grid-tied voltage source converters (VSCs) to meet strict grid standards. LCL filters effectively attenuate high-frequency harmonics generated by power electronics, minimizing grid current noise injection. However, ensuring system stability is crucial, and active damping methods are preferred to passive damping circuits due to lower power losses. The chapter focuses on the capacitor-current active damping (CCAD) technique, aiming to identify the optimal feedback gain for stability. Additionally, it addresses harmonics compensation for grid voltage distortion, proposing an improved resonator with phase compensation to suppress harmonics while maintaining stability. Analytical derivation of the capacitor feedback gain for stability is provided, and the proposed control scheme is validated through simulation and experimental results.

This chapter is based on the following article:

- Y. Wu, T. B. Soeiro, A. Shekhar, J. Xu and P. Bauer, "Virtual Resistor Active Damping with Selective Harmonics Control of LCL-Filtered VSCs," 2021 IEEE 19th International Power Electronics and Motion Control Conference (PEMC), Gliwice, Poland, 2021, pp. 207-214.

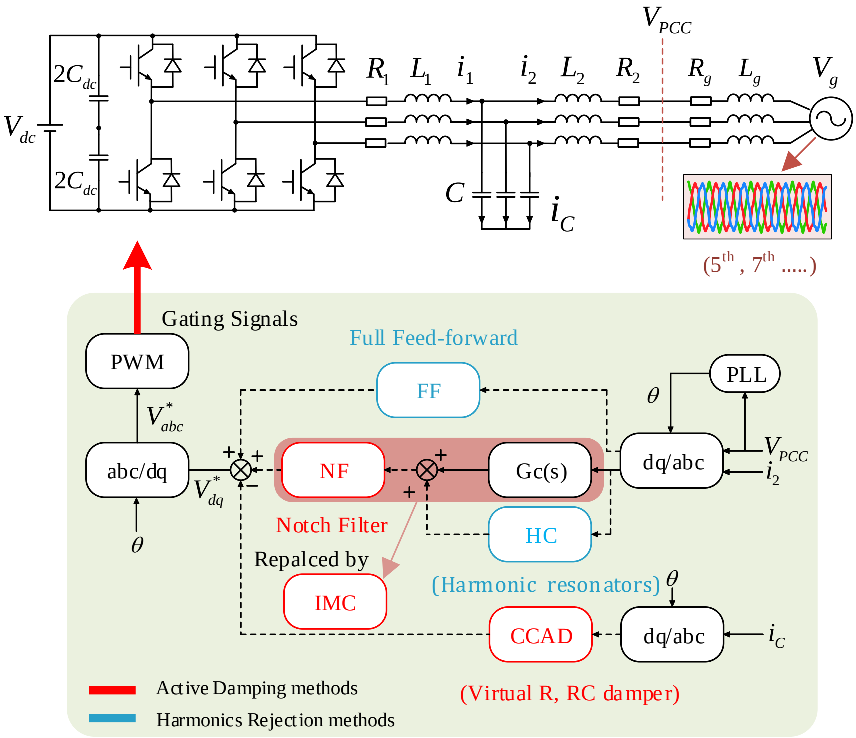

V_{PCC}
$2C_{dc}$
$2C_{dc}$
V_{dc}
R_1
L_1
i_1
i_2
L_2
R_2
R_g
L_g
V_g
C
i_C
(5th, 7th .....)
Gating Signals
PWM
Full Feed-forward
FF
PLL
θ
V^*_{abc}
abc/dq
NF
Gc(s)
dq/abc
V_{PCC}
i_2
V^*_{dq}
+
+
−
+
+
Notch Filter
HC
θ
Repalced by
IMC
(Harmonic resonators)
θ
CCAD
dq/abc
i_C
Active Damping methods
Harmonics Rejection methods
(Virtual R, RC damper)

Figure 6.1: Three-phase grid-tied voltage source converter with a LCL filter.

6.1. INTRODUCTION

Pulse-Width Modulated (PWM) voltage source converters (VSCs) are the main building blocks for interfacing distributed generation (DG) units, power flow control, and emerging smart loads with hybrid ac-dc distribution grids [114–117]. Continuous PWM strategy such as Sinusoidal PWM (S-PWM) is widely used for the modulation of VSCs due to the simplicity and better harmonics performance, instead of discontinuous PWM strategies [118, 119]. LCL filter is preferably adopted in VSCs for attenuating high-frequency harmonics in the output waveforms. However, special attention must be paid to the LCL filter resonance which usually needs to be damped to safeguard the system stability. In renewable generation applications, the grid-connected VSCs are generally controlled in Current-Control Mode (CCM). The choice of the converter or grid-side current control is influenced by the resonance of the LCL filter based on the ratio between the resonance frequency f_r and the PWM sampling frequency f_s [120]. Recently, studies on the single-loop control revealed that the grid-side current control can be more stable if the resonance frequency f_r lies between $\frac{1}{6}\ f_\mathrm{s}$ (critical frequency) and $\frac{1}{2}\ f_\mathrm{s}$ (Nyquist frequency) if the symmetric sampling and single-update PWM pattern is adopted [121]. For the double-update case, the critical frequency shifts to $\frac{1}{4}\ f_\mathrm{s}$ [122]. Correspondingly, stability with converter-side current control can be ensured without any additional means if the f_r is found below the critical frequency.

Achieving stable control is possible while operating in the previously described unstable control region defined by the chosen LCL filter and sampling frequency. However, filter resonance damping measures become necessary for guaranteeing enough stability margin for the system. Passive damping solutions, i.e., parallel or series connection of resistor with the capacitor and/or inductor offer satisfactory performance but have consequences on the overall size and system efficiency [123]. On the other hand, the active damping schemes can improve the stability while not influencing the efficiency [120–122]. These methods can be classified into two main categories [121, 124, 125]: 1) multi-loop control methods; and 2) filter-cascaded methods.

The filter-based active damping methods, shown in Fig. 6.1, are mainly realized by cascading the filter in the current controller loop. The notch filter (NF) method typically employs a second-order digital filter which creates an anti-resonance at the pre-set LCL filter resonance frequency to improve the system attenuation around this frequency [124, 126]. Other filter-based methods, i.e, IMC (Internal Model Control) is derived based on the model of the control plant and are studied in [127]. However, both the NF and IMC models are sensitive to system parametric variations, e.g, the change of the LCL filter component values with the current bias and/or the intrinsic unknown grid impedance (represented by L_g and R_g in Fig. 6.1). The adaptive or self-commissioned filter methods are proposed in [128] to improve the robustness against the circuit parametric uncertainties and dynamic variations, however, at the cost of control complexity. On the other hand, the multi-loop active damping method uses the available state signals in the circuit through feedback control to form an equivalent virtual resistor in series or parallel with the LCL filter elements, e.g., the filter capacitor and inductors. While both capacitor voltage and current feedback-based control have been reported, the cost of the voltage sensor can be lower compared to the high-bandwidth current ones. On the other hand, capacitor voltage active damping (CVAD) [129] requires the implementation of the differentiators in the feedback loop, which is difficult to implement in practice. By contrast, capacitor current active damping (CCAD), shown in Fig. 6.1, only requires a proportional feedback [130]. If the influence of the digital control delay is considered, the proportional feedback of the capacitor current may result in a negative virtual resistor in some cases [125], leading to an undesired non-minimum phase system. However, this negative virtual resistor can be avoided if the resonance frequency is smaller than $\frac{1}{6}$ f_s with maximum possible delay.

Another control issue in a grid-connected VSC system is the control of the current harmonics due to the distorted grid voltage. The full feed-forward (FF) scheme of the grid voltage is reported to be able to effectively compensate the harmonics by fully canceling out the influence of the grid voltage [131]. However, the full FF scheme needs to implement the first and second-order differentiators which is hard to precisely discretize in the digitally controlled system. In contrast, the harmonic resonant controller is widely adopted to realize the selective harmonics compensation, which enlarges the loop gain at the tuned frequency. From the control point of view, the harmonics current can be suppressed due to the infinitely large grid impedance at the harmonics frequencies [115, 132, 133]. However, a resonator controller requires phase compensation [133, 134] to ensure enough phase margin due to the system delay. In this work, an improved harmonics resonator with phase compensation along with a design guideline for capacitor current active damping is presented. The main contributions are 1) The analytical derivation of suitable capacitor current feedback gain ensuring system stability and 2) The derivation of an improved resonator controller with phase compensation.

Section 6.2 presents the system description and basic control scheme. The analysis of capacitor current active damping and harmonics control are introduced in Section 6.3 and 6.4 respectively. Simulations and experimental results are carried out in Section 6.5. Conclusion and future work are presented in Section 6.6.

6.2. SYSTEM MODELING AND CONTROL

6.2.1. CIRCUIT MODELING

The VSC connected to the grid with an LCL filter is depicted in Fig. 6.1. The described grid is assumed to be a stiff grid which contains low-order harmonics such as 5_{th}, 7_{th}, 11_{th} and 13_{th}. Therefore, the grid interface components R_g and L_g are neglected in this work and hence, $V_{\text{PCC}} = V_\text{g}$. The filter resistors R_1 and R_2 represent the internal resistance of the converter-side inductor L_1 and grid-side inductor L_2, respectively. Additionally, the equivalent resistance due to the conduction losses of the VSC is incorporated into R_1. Fig. 6.2 shows the average switched model of the control plant of a VSC with LCL filter, where $V_\text{t}(s)$ is the VSC terminal voltage. The $Z_1(s)$, $Z_2 s$ and $Z_\text{C}(s)$ are the impedance of L_1, L_2 and C and given as:

$$Z_1(s) = sL_1 + R_1 \tag{6.1}$$

$$Z_2(s) = sL_2 + R_2 \tag{6.2}$$

$$Z_C(s) = \frac{1}{sC} \tag{6.3}$$

The transfer function relating the grid-side output current i_2 and the converter terminal voltage V_t is:

$$G_{\text{i}_2}(s) = \frac{i_2(s)}{V_\text{t}(s)} = \frac{1}{\alpha s^3 + \beta s^2 + \gamma s + \delta} \tag{6.4}$$

where, constants are given by $\alpha = L_1 L_2 C$, $\beta = R_2 L_1 C + R_1 L_2 C$, $\gamma = R_1 R_2 C + L_1 + L_2$ and $\delta = R_1 + R_2$. Considering that R_1 and R_2 are negligible, (6.4) can be simplified and given by (6.5).

$$G_{\text{i}_2}(s) = \frac{1}{L_1 L_2 C s}\left(\frac{1}{s^2 + \omega_\text{r}^2}\right) \tag{6.5}$$

where, the resonance frequency (ω_r) of the LCL filter is given by (6.6).

$$\omega_r = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C}} \tag{6.6}$$

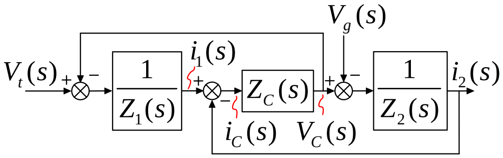


Figure 6.2: Block diagram of the control plant of LCL-filtered VSC.

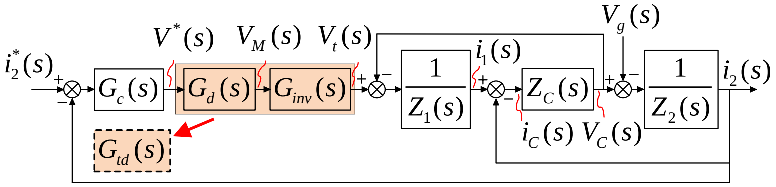


Figure 6.3: Block diagram of the basic VSC grid current control scheme without active damping and harmonic suppression.

6.2.2. Basic Control of the VSC

The block diagram of the grid-side current control of VSC without any active damping and harmonics compensation is shown in Fig. 6.3.

The compensator $G_c(s)$ used for current control is typically a PR (proportional-resonant) controller in stationary $(\alpha\beta)$ frame or a PI controller in rotating (dq) frame [115, 132].

$$\begin{aligned} G_{c(\alpha\beta)}(s) &= k_p + \frac{k_r s}{s^2 + \omega_1^2} \\ G_{c(dq)}(s) &= k_p + \frac{k_i}{s} \end{aligned} \tag{6.7}$$

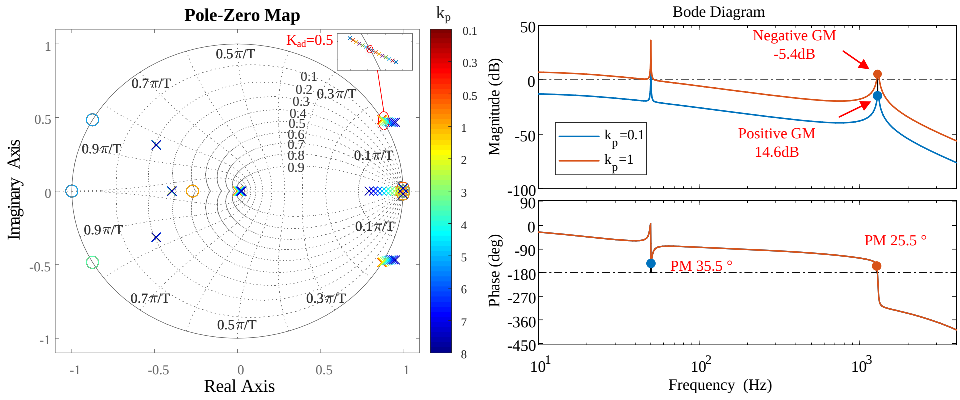
The control and computation delay in the digitally controlled system is noted as $G_c(s)$. The mechanism of the computation delay depends on the sampling and update of the implemented PWM [130]. If the symmetric sampled PWM with a single update (sampling happens at the upper peak of the triangular wave) is adopted, the computation delay is given by $G_d(s) = e^{\text{-sT}_\text{s}}$. f_s and f_{sw} are the sampling and switching frequency respectively such that $T_\text{s} = \frac{1}{f_\text{s}}$ and $T_\text{sw} = \frac{1}{f_\text{sw}}$. $G_{inv}(s)$ is the transfer function representing the PWM process, which is given by (6.8).

$$G_\text{inv}(s) = \frac{K_\text{pwm} G_\text{h}(s)}{T_\text{s}} \tag{6.8}$$

where, the PWM gain K_pwm is the ratio of the dc voltage V_{in} and amplitude of the triangular carrier wave V_{tri} and taken as 1 to simplify the analysis.

The Zero-Order Hold (ZOH) characteristics of the PWM process is modeled as an equivalent transfer function $G_\text{h}(s)$ as approximated by (6.9) using frequency domain analysis.

$$G_\text{h}(s) = \frac{1 - e^{\text{-sT}_\text{s}}}{s} \approx T_\text{s} e^{\text{-}\frac{1}{2}\text{sT}_\text{s}} \tag{6.9}$$



(a) Poles-zeros map (b) Bode Plot

Figure 6.4: Control loop without active damping.

Combining (6.8) and (6.9), the total delay G_{td} can be expressed as (6.10).

$$G_{\mathrm{td}}(s) \approx e^{-\frac{3}{2}sT_s} \tag{6.10}$$

6.3. CAPACITOR CURRENT FEEDBACK ACTIVE DAMPING

6.3.1. VIRTUAL RESISTOR

The allowable gain while ensuring stable operation of a VSC is limited when no active damping is used, as shown in Fig. 6.4 where the maximum controller gain is limited to $K_{\mathrm{ad}} = 0.5$. Table 6.1 lists the used parametric specifications.

Table 6.1: System parameters

L_1 , L_2	R_1 , R_2	C	V_{DC}	k_{p}	k_{r}	k_{rh}	ω_{c}
1.5 mH	0.2 Ω	20 μF	700 V	5	2500	1000	2

As a consequence, the small bandwidth of the closed-loop system leads to an undesired slow system response. Consider the equivalent circuit of the LCL filter with capacitor current i_{c} shown in Fig. 6.5. The feedback of i_{c} is equivalent to adding an impedance ($Z_{\mathrm{ad}} = R_{\mathrm{ad}} + jX_{\mathrm{ad}}$) in parallel with the filter capacitor [125].

In CCAD, the current control loop is modified using feedback of i_{c} via gain $K_{\mathrm{ad}}(s)$ as shown in Fig. 6.6. The relation between Z_{ad} and $K_{\mathrm{ad}}(s)$ is described by (6.11).

$$Z_{\mathrm{ad}}(s) = \frac{L_1}{K_{\mathrm{ad}}(s)G_{\mathrm{td}}(s)C} \tag{6.11}$$

Without consideration of the delay $G_{\mathrm{td}}(s)$, the equivalent impedance behaves like a virtual resistor if the proportional feedback gain K_{ad} is used [125], which is expressed by

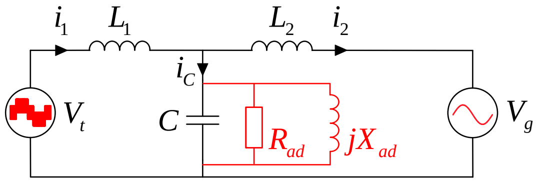


Figure 6.5: Equivalent circuit of the LCL-filter-based integration of the grid-connected VSC.

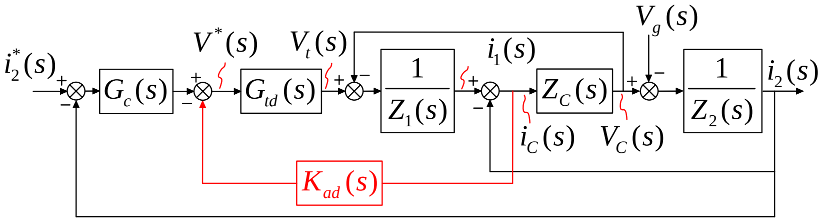


Figure 6.6: Block diagram using CCAD control.

(6.12):

$$R_{\mathrm{ad}} = \frac{L_1}{K_{\mathrm{ad}}C} \tag{6.12}$$

However, the proportional feedback results in the virtual impedance if the system delay is included. By substituting (6.10) into (6.12), the impedance can be derived as (6.13):

$$Z_{\mathrm{ad}}(s) = \frac{L_1}{K_{\mathrm{ad}}C} e^{\text{-sT}_\text{s}} = R_{\mathrm{ad}} e^{\text{-sT}_\text{s}} \tag{6.13}$$

Substituting $s = j\omega$ yields (6.14).

$$Z_{\mathrm{ad}}(j\omega) = R_{\mathrm{ad}}\ [cos(\frac{3}{2}\omega T_{\mathrm{s}}) + j sin(\frac{3}{2}\omega T_{\mathrm{s}})] \tag{6.14}$$

As noted in (6.14), the delay influences both the resistive and inductive (or capacitive) parts. The imaginary term may alter the LCL filter resonance frequency and influence the precision of the control [129]. Meanwhile, it can be proven that the resistive part becomes negative when the frequency f $(\omega/2\pi)$ is above $\frac{1}{6}f_{\mathrm{s}}$, which leads to a non-minimum phase behavior of the grid-side current [125]. Hence, the proportional feedback gain of the capacitor current should be properly designed. Furthermore, the identification of the range of the gain K_{ad} which guarantees the stability of the system is essential for designing a well-tuned controller.

6.3.2. RANGE OF FEEDBACK GAIN FOR STABILITY OF THE SYSTEM

After the capacitor current feedback to the control loop, the equivalent control plant G'_{i_2} can be expressed by (6.15):

$$\begin{aligned} G'_{\mathrm{i}_2}(s) &= \frac{1}{L_1 L_2 C s^3 + G_{\mathrm{td}}(s) K_{\mathrm{ad}} L_2 C s^2 + L_2) s} \\ &= \frac{1}{L_1 L_2 C s} \frac{1}{s^2 + K_{\mathrm{ad}} G_{\mathrm{td}}(s)/L_1 s + \omega_{\mathrm{r}}^2} \end{aligned} \tag{6.15}$$

Based on the previously discussed control elements of the controlled system, the open-loop transfer function from the reference input to the output grid-side current is derived in (6.16):

$$\begin{aligned} G_{\mathrm{ol}}(s) &= G_{\mathrm{c}}(s) G_{\mathrm{d}} G'_{\mathrm{i}_2}(s) \\ &= \frac{G_{\mathrm{c}}(s) G_{\mathrm{td}}(s)}{L_1 L_2 C s (s^2 + K_{\mathrm{ad}} G_{\mathrm{td}}(s)/L_1 s + \omega_{\mathrm{r}}^2)} \end{aligned} \tag{6.16}$$

In order to derive the analytical formulations from the delay-influenced system, the delay $G_{\mathrm{d}}(s)$ can be approximated with the rational polynomial form in (6.17):

$$G_{\mathrm{td}}(s) = e^{-\mathrm{sT_d}} = \left(\frac{1 - \frac{T_{\mathrm{d}} s}{2n}}{1 + \frac{T_{\mathrm{d}} s}{2n}}\right)^{\mathrm{n}} \tag{6.17}$$

where n= 2 can give a precise approximation. Therefore, it can be noted that the pole of the open loop can be located in the right-half part of the s plane or outside the unit circle of the corresponding z plane, with the increase of the feedback gain. Thus, the critical $K_{\mathrm{ad\_c}}$ is defined as the gain which proceeds a imaginary pole $s = j\omega_{\mathrm{x}}$, namely

$$pole(G_{\mathrm{ol}}(j\omega_{\mathrm{x}})) = 0 \tag{6.18}$$

Substitute (6.16) and (6.17) into (6.18), ω_{x} is solved as:

$$\begin{aligned} \omega_{\mathrm{x}} &= \sqrt{\frac{-b - \sqrt{b^2 - 4ac}}{2a}} \\ a &= \left(\frac{T_{\mathrm{d}}}{4}\right)^4, \quad b = -\frac{3}{8} T_{\mathrm{d}}^2, \quad c = 1, \end{aligned} \tag{6.19}$$

and $K_{\mathrm{ad\_c}}$ hence is expressed in (6.20):

$$K_{\mathrm{ad}\_c} = \frac{(\omega_{\mathrm{x}}^2 - \omega_{\mathrm{r}}^2)(1 + \omega_{\mathrm{x}}^2 T_{\mathrm{d}}^2/16)^2 L_1}{\omega_{\mathrm{x}}^2 T_{\mathrm{d}}^2 (1 - \omega_{\mathrm{x}}^2 T_{\mathrm{d}}^2/16)} \tag{6.20}$$

From (6.19) and (6.20), it is observed that the imaginary pole ω_{x} is the new resonance frequency shifted by the delay and it is solely determined by the value of the delay. Meanwhile, the maximum feedback gain K_{ad} allowing non-right-half-plane (RHP) poles is restrained by the LCL filter parameters and delay together. Above $K_{\mathrm{ad\_c}}$, the system can be still stable despite the open-loop poles located in RHP. Since the open-loop system has one pair of conjugate poles in the RHP, the boundary of this gain can be derived by forcing the open-loop system to encircle the point (-1,0) once anti-clock-wisely in the half Nyquist plot, where ω increases from 0 to ∞. Since the $-180°$ crossing occurs at ω_x, it can be mathematically expressed as:

$$|G_\mathrm{ol}(j\omega_\mathrm{x})| \geq 1 \tag{6.21}$$

The upper boundary $K_\mathrm{ad\_u}$ is then derived in (6.22).

$$\begin{aligned} K_\mathrm{ad\_u} &= \frac{(\Delta\omega^2 + \omega_\mathrm{x}^2 - \omega_\mathrm{r}^2)(1+\omega_\mathrm{x}^2 T_\mathrm{d}^2/16)^2 L_1}{\omega_\mathrm{x}^2 T_\mathrm{d}^2 (1-\omega_\mathrm{x}^2 T_\mathrm{d}^2/16)} \\ \Delta\omega^2 &= \frac{\sqrt{k_\mathrm{p}^2 + (k_\mathrm{r}/\omega_\mathrm{x})^2}}{\omega_\mathrm{x} L_1 L_2 C} \approx \frac{k_\mathrm{p}}{\omega_\mathrm{x} L_1 L_2 C} \end{aligned} \tag{6.22}$$

The expression (6.22) shows that the maximum feedback gain for achieving stability of the closed-loop system is altogether determined by the controller parameters, the time delay, and the LCL filter parameters. The difference between this gain and the previously derived $K_\mathrm{ad\_c}$ points out that the controlled VSC with LCL filter can be still stable with the control of the current controller despite the open-loop poles in the RHP. However, such an unstable open-loop system is not preferred in practice and thus $K_\mathrm{ad\_c}$ is taken as the maximum set value:

$$K_\mathrm{ad\text{-}max} = K_\mathrm{ad\_c} \tag{6.23}$$

The minimum value of K_ad can be obtained by forcing the open-loop system to not encircle the point (-1,0) in the Nyquist plot. The $-180°$ occurs at the resonance frequency ω_r, hence it can be mathematically expressed in (6.24):

$$|G_\mathrm{ol}(j\omega_\mathrm{r})| \leq 1 \tag{6.24}$$

which yields (6.25).

$$K_\mathrm{ad\text{-}min} = \frac{\sqrt{k_\mathrm{p}^2 + (k_\mathrm{r}/\omega_\mathrm{r})^2}}{\omega_\mathrm{r}^2 L_2 C} \approx \frac{k_\mathrm{p}}{\omega_\mathrm{r}^2 L_2 C} \tag{6.25}$$

Specifically, $K_\mathrm{ad\text{-}min}$ is equal to $k_\mathrm{p}/2$ when $L_1 = L_2$ is satisfied. Therefore, the suitable range of feedback gain is:

$$K_\mathrm{ad} \in (K_\mathrm{ad\text{-}min}, K_\mathrm{ad\text{-}max}) \tag{6.26}$$

Based on the parameters in Table 6.1, the pole-zero map of the closed-loop system and the bode plot of the open-loop system are drawn in Fig. 6.8, when the controller gain k_p is chosen as 5. $K_\mathrm{ad\_c}$ and $K_\mathrm{ad\_u}$, as well as $K_\mathrm{ad-min}$, are indicated in Fig. 6.8(a), which coincide with the calculated values based on the derived equations. Besides, Fig. 6.8(b) shows the bode plot of the open-loop system with different K_ad, which presents the shifted resonance and the negative $-180°$ crossing. Fig. 6.7 demonstrates the nyquist plot of the open-loop system with the K_ad around $K_\mathrm{ad\_c}$ and $K_\mathrm{ad\_u}$. As the gain exceeds $K_\mathrm{ad\_c}$, a negative $-180°$ along with a resonance (>1 dB) occurs in the bode plot which corresponds the one anti-clockwise encirclement of (-1,0) in the half Nyquist plot.

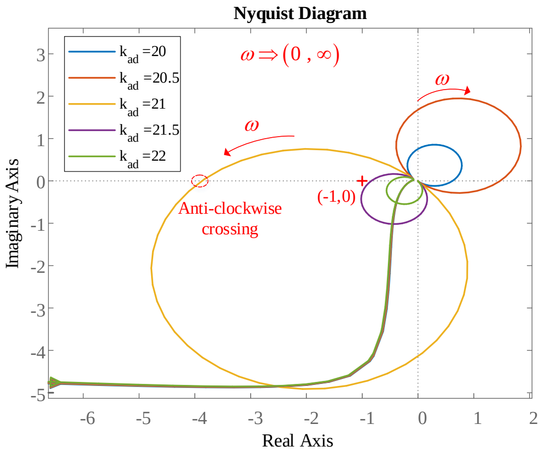
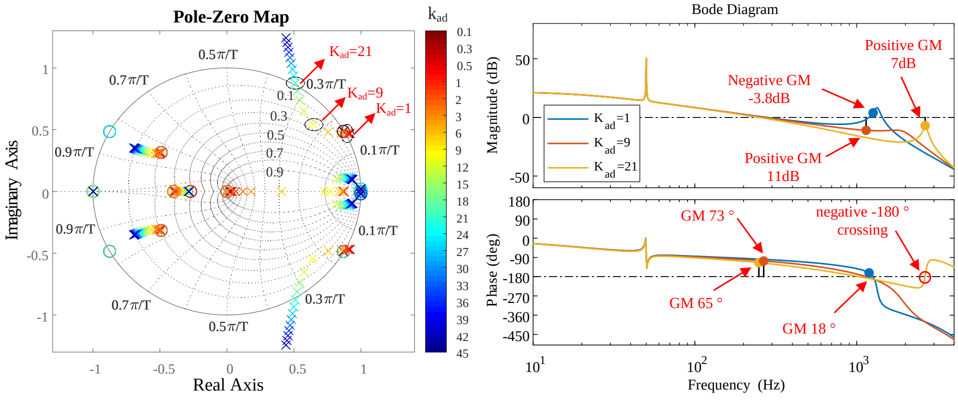


Figure 6.7: Nyquist plot of the open-loop system (half-plot).

Meanwhile, the open-loop system has one conjugate pair of RHP poles. According to the Nyquist stability criterion, the closed-loop system is stable as the numbers of anti-clockwise encirclement equal the number of open-loop RHP poles. However, after k_{ad} becomes larger than $K_{\text{ad\_u}}$, the resonance is smaller than 1 dB which means there is no encirclement of (-1,0). Hence, the close-loop system has the same number of RHP poles as the open-loop system has.

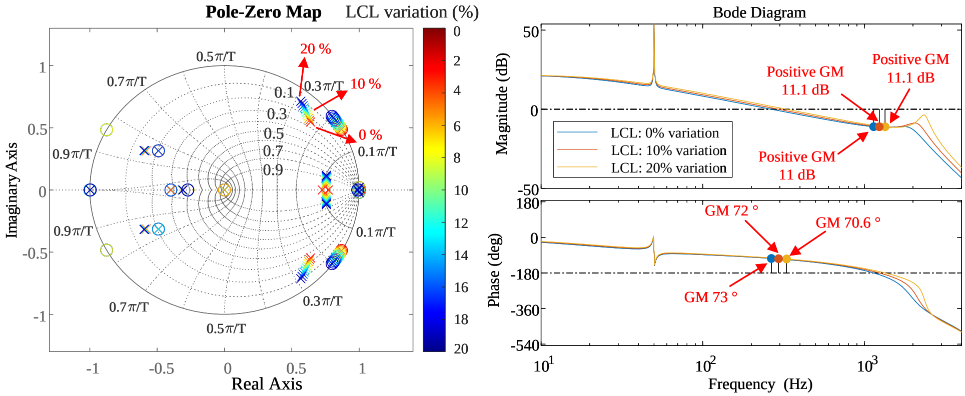


(a) Poles-zeros map

(b) Bode Plot

Figure 6.8: Control loop with capacitor-current feedback ($k_{\text{p}} = 5$).

The pole-zero map of the closed-loop system and the Bode plot of the open-loop system are illustrated in Fig. 6.9, considering a maximum 20% variation in the LCL filter parameters. It is observed that the variation in the LCL filter parameters has a negligible impact on the gain and phase margins.



(a) Poles-zeros map

(b) Bode Plot

Figure 6.9: Control loop with CCAD under variation of LCL filter parameters ($k_\mathrm{p} = 5$ and $k_\mathrm{ad} = 9$).

6.3.3. STABILITY MARGINS

In order to achieve stable control, an appropriate gain and phase margin should be guaranteed by properly setting up the feedback gain K_ad and controller gain k_p. The gain and phase margins of the controlled system are given by (6.27):

$$\begin{aligned} GM &= -20\lg|G_\mathrm{ol}(j\omega_\mathrm{r})| \\ PM &= \pi + \angle|G_\mathrm{ol}(j\omega_\mathrm{co})| \end{aligned} \tag{6.27}$$

where ω_co is the gain crossover frequency where the open-loop gain $|G_\mathrm{ol}(j\omega)|$ reaches 1 and the phase crossover frequency is equal to ω_r. The gain margin can be further expressed in (6.28):

$$\begin{aligned} GM &= -20\lg \\ &\approx -20\lg \\ &\approx 20(\lg(\frac{K_\mathrm{ad}}{k_\mathrm{p}}) + \lg(\omega_\mathrm{r}^2 L_2 C)) \end{aligned} \tag{6.28}$$

It can be noted that for a given LCL filter, the phase margin is proportional to K_ad and inversely proportional to k_p in logarithmic scale. To express the phase margin analytically, the gain crossover frequency is approximated in (6.29):

$$\begin{gathered} \omega_\mathrm{co} \approx \sqrt{\frac{-b+\sqrt{b^2-4ac}}{2a}} \\ a = (\frac{K_\mathrm{ad}}{L_1})^2, \quad b = \omega_\mathrm{r}^4, \quad c = -(\frac{k_\mathrm{p}}{L_1 L_2 C})^2 \end{gathered} \tag{6.29}$$

The phase margin can be further derived in (6.30):

$$\begin{aligned} PM = &\frac{\pi}{2} - \omega_{\mathrm{co}} T_{\mathrm{d}} - tan^{-1}\left(\frac{k_{\mathrm{r}}}{\omega_{\mathrm{co}} k_{\mathrm{p}}}\right) \\ &- tan^{-1}\left(\frac{\omega_{\mathrm{co}} K_{\mathrm{ad}} cos(\omega_{\mathrm{co}} T_{\mathrm{d}})}{L_1(\omega_{\mathrm{r}}^2 - \omega_{\mathrm{co}}^2 - \omega_{\mathrm{co}} sin(\omega_{\mathrm{co}} T_{\mathrm{d}}))}\right) \end{aligned} \tag{6.30}$$

The derived relations are plotted in Fig. 6.10. It is noted that both the gain and phase margin drop with the increase of K_{ad}. Usually, a gain margin of 10 dB guarantees good stability. The corresponding K_{ad} is derived as 8, which indicates a phase margin of 69°.

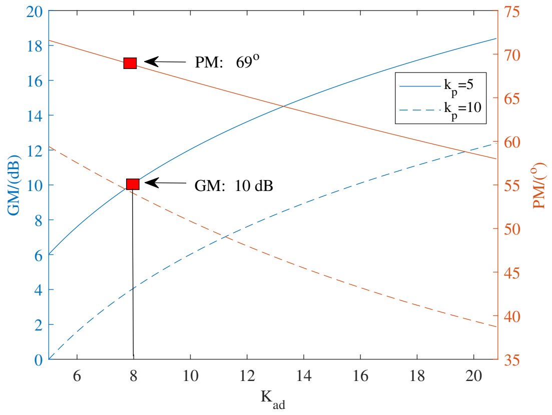


Figure 6.10: Gain and Phase Margin versus K_{ad}.

6.4. HARMONICS COMPENSATION BASED ON RESONANT CONTROLLER

Harmonics resonators are widely used for suppressing the harmonics caused by grid distortions by simply introducing single or multiple resonators tuned at the corresponding harmonics frequencies in parallel with the basic current controller. The generalized non-ideal resonators with two integrators [132] in $\alpha\beta$ frame are expressed in (6.31):

$$G_{\mathrm{h}}(s) = \sum_{h=3,5,7...} K_{\mathrm{ph}} + \frac{2K_{\mathrm{rh}}\omega_{\mathrm{c}} s}{s^2 + 2\omega_{\mathrm{c}} s + (h\omega_1)^2} \tag{6.31}$$

where K_{rh} and ω_{c} represent the resonant controller gain and cut-off frequency (or damping factor) respectively. The bandwidth is adjusted by setting ω_{c} appropriately. A small cut-off frequency is usually chosen for high rejection performance [132]. One typical problem associated with the resonators is the phase deterioration caused by the delay. This can be improved by certain phase compensation methods, for example the introduction of a lead-filter [115] cascaded with the resonant controller. The generalized form of a lead filter (F_{lead}) is given by (6.32)

$$F_{\text{lead}} = \frac{s/\omega_{\text{f}} + 1}{s\alpha/\omega_{\text{f}} + 1} \tag{6.32}$$

where ω_{f} and α are the tuning parameters determined by the required phase compensation ϕ_{max} at the specified frequency ω_{max}, which is described in (6.33).

$$\begin{aligned} \sqrt{\alpha} &= tan(\frac{\pi}{4} - \frac{\phi_{\text{max}}}{4}) \\ \omega_{\text{f}} &= \omega_{\text{max}}\sqrt{\alpha} \end{aligned} \tag{6.33}$$

The bode plot in Fig. 6.11 shows that the phase at the resonance frequency is improved by the lead filters and the phase margin is hence increased.

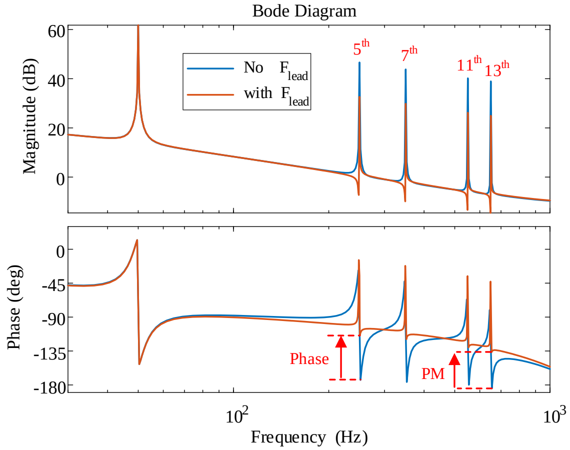


Figure 6.11: Bode plot of the open-loop with harmonics resonators.

6.5. SIMULATION AND EXPERIMENTAL VERIFICATION

6.5.1. SIMULATION RESULTS

To verify the accuracy of the identified range of the capacitor-current feedback gain, simulations are conducted in MATLAB/SIMULINK. The operating parameters are listed in Table 6.1. The system operates in inverter mode at a power $P_{\text{ac}} = 3\,\text{kW}$ with a feedback current control loop connected to a 400 V 50 Hz 3-phase grid. Fig. 6.12 shows the grid-side current waveform with different K_{ad} values under an ideal sinusoidal voltage. At $K_{\text{ad}} = 2.6$, which is close to the theoretical value 2.5, the grid-side current becomes marginally stable and the resonance occurs in the waveform with the frequency of ω_{r} (1300 Hz). With $K_{\text{ad}} = 8$, at which the system is supposed to have a GM of 10 dB and PM of 69°, the grid-side current follows close to a sinusoidal 50 Hz waveform. After the K_{ad} increases to 19.5, the new resonance component arises in the grid-side current, the frequency of which is around the shifted resonance frequency ω_{x} (2800 Hz). Therefore,

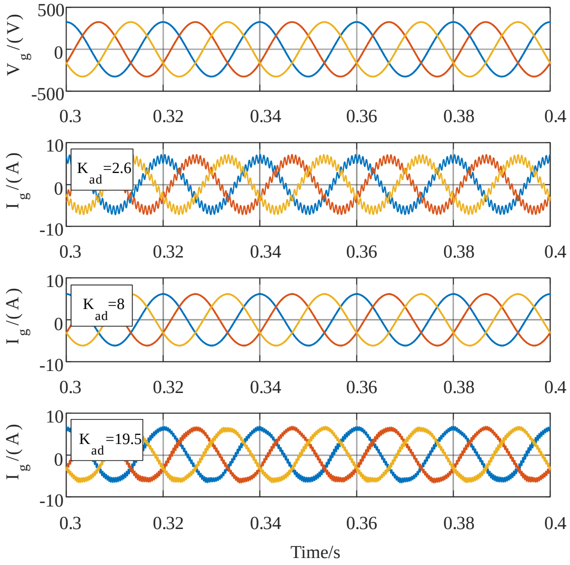


Figure 6.12: Simulation results: grid voltages and grid-side currents under different K_{ad}.

the stability range identified from the simulation is close to the theoretical one [2.5,20.8]. The simulation of the harmonics control is shown in Fig. 6.13, where the distorted grid voltage containing low-order frequency harmonics with amplitudes of 5% of the fundamental rated voltage at the 5^{th}, 7^{th}, 11^{th}, 13^{th} is considered. The proposed resonator parameters are listed in Table 6.1 and the lead filters are designed to provide 60° at each harmonics frequency. The harmonics control is enabled at 0.3 s and the results show

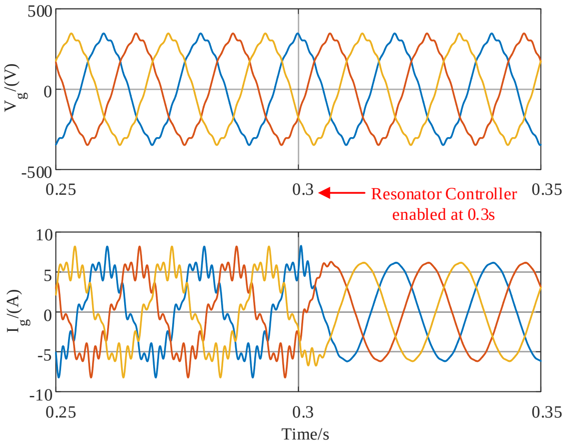


Figure 6.13: Simulation results: grid voltages and grid-side currents with the proposed harmonics control.

that the harmonics components in the grid-side current are quickly rejected by the resonators and the current achieves a satisfactory THD of about 0.5%.

6.5.2. Experimental Verification

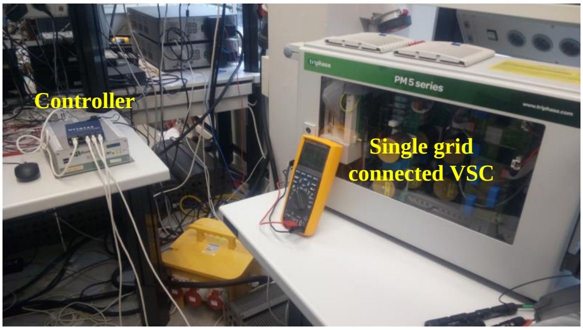


Figure 6.14: Two-level VSC Triphase/PM5F30C used for experimental validation.

The experimental validation is conducted in a commercial 5 kW rated two-level VSC, i.e. Triphase/PM5F30C as shown in Fig. 6.14. The system is set to operate as a shunt active filter generating 1000 VAR reactive power to the distorted grid. The grid voltage is depicted in Fig. 6.15, which contains in relation to the fundamental frequency component: 0.5% 5th, 2% 7th, 0.5% 11th, 0.3% 13th. As expected, the grid-side current is severely distorted due to the considerable filter capacitor, which leads to quite large low-order harmonics in the current. Hence, the results in Fig. 6.15 show the same tendency as the simulation results in Fig. 6.13. Note that the system is still stable even without the capacitor-current feedback ($K_{\mathrm{ad}} = 0$). This is due to the quite large internal resistance of the LCL filter and inherent damping caused by the inefficient semiconductors in the Triphase system (high switching and conduction losses). The resonance (at $\omega_{\mathrm{r}} = 1300\,\mathrm{Hz}$) in the

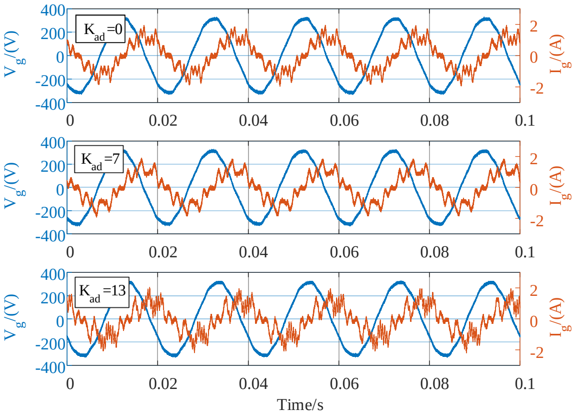


Figure 6.15: Preliminary experimental results: Grid-side current under different K_{ad}.

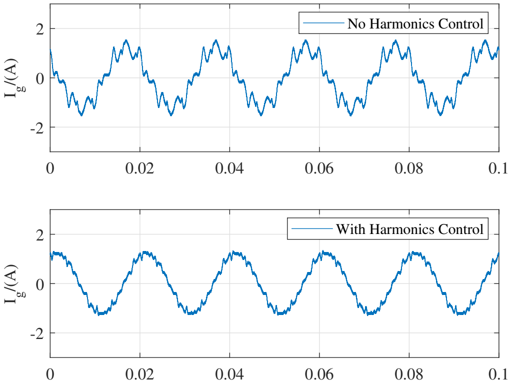


Figure 6.16: Preliminary experimental results: Grid-side current with harmonics control under distorted grid voltage.

grid-side current at $K_{ad} = 0$ shows that the system is close to the marginally stable condition. At $K_{ad} = 7$, only low-order harmonics exist in the grid-side current. After K_{ad} reaches 13, the system becomes marginally stable and the resonance (at $\omega_x = 2800\,\text{Hz}$) quickly arises. The maximum K_{ad} is smaller than the theoretical one and this can be explained by the fact that the delay and the damping characteristics in the system are different from the simulated system. Fig. 6.16 presents the grid-side current with and without the harmonics control under $K_{ad} = 7$. After the implementation of the proposed resonator, the THD of the grid-side current decreased from 32% to 7.5%, which is still quite large. This might be because the insufficient phase compensation limits the further increase of k_{rh} and ω_c.

6.6. CONCLUSION AND FUTURE WORK

This chapter has presented the design of a controller for the grid-connected PFC converter, aimed at ensuring system stability in the face of challenges such as LCL filter resonance and grid harmonics distortion. Firstly, the analytical identification of the boundary for the capacitor-current feedback gain has been discussed to achieve effective active damping. Subsequently, a novel approach employing a harmonics resonator cascaded with a lead filter has been proposed to compensate for selective harmonic components in the grid-side current induced by distorted grid voltage. Both simulation and experimental results have been presented to demonstrate the performance of the proposed control scheme.

However, it is noted that practical results have shown deviations from theoretical and simulation results, primarily attributable to unidentified damping and delay in the Triphase/PM5F30C system. The effectiveness of the resonator has been limited by the achieved phase margin. As a result, future research endeavors will focus on exploring more effective phase compensation methods and other harmonics control techniques, including multiple-axis control and full grid voltage feed-forward strategies.

7

CONCLUSION

The objective of this thesis is to research and establish techniques and guidelines for variable switching frequency modulation to enhance the efficiency and power density of front-end converters while optimizing the emission of supra-harmonics to the grid connected to EV chargers. The research objective has been resolved into four different research questions. In this chapter, the main conclusions of each research question have been summarized, and recommendations for future research directions have been provided.

7.1. CONCLUSION

Q1 *What are the advantageous PFC converter solutions to the two-stage EV chargers?*

The suitable power electronics topologies for the front-end converter vary based on the types of bidirectional EV chargers. Specifically, Chapter 2 categorizes the front-end converter architectures into transformer-based and transformer-less (modular) structures, highlighting their distinct characteristics and applications. The chapter delves into the utilization of conventional PWM-based VSC topologies, such as the 2-level, 3-level (T-type, NPC, and A-NPC), and interleaved topologies, as active front-end converters in both transformer-based DC fast chargers and on-board chargers.

Moreover, Chapter 2 presents detailed design methodologies for two specific topologies: the three-phase 3-level T-type converter and the three-phase 2-interleaved converter. Through multi-objective optimization (MOO) techniques, the design process focuses on achieving an optimal balance between efficiency and power density by leveraging available core databases in the market. Additionally, the chapter explores innovative high-power PFC charger solutions, such as the 12-pulse buck rectifier and hybrid rectifier, offering promising alternatives for heavy-duty vehicle chargers. Preliminary experimental results are also discussed, demonstrating the feasibility and effectiveness of these proposed solutions.

Q2 *How to improve the efficiency and power density of the front-end AC-DC PFC converter with the approach of variable switching frequency?*

The soft-switching technique, such as zero-voltage switching (ZVS), has been widely adopted in AC-DC converters to reduce switching losses. The triangular-current-mode (TCM) method stands out as an effective ZVS technique for virtual-grounded AC-DC PFC converters based on wide-bandgap (WBG) devices, which exhibit relatively low turn-off losses compared to turn-on losses. Chapter 3 introduces the three-phase integrated-TCM (iTCM) PFC converter, which incorporates an additional LC branch between the virtual ground point and the mid-point of the DC link.

In the three-phase iTCM PFC converter, the LC branch effectively absorbs most of the high-frequency current components, allowing the inductor to be designed and built with ferrite cores. This setup relieves the grid-side inductor from high current stress and optimizes losses with other core types, such as powder core and amorphous cut-core. By implementing bounded-iTCM and sinusoidal-iTCM schemes, the switching frequency is effectively limited while maintaining ZVS realization. Experimental validation and comparison with conventional continuous current mode (CCM) approaches indicate significant improvements in efficiency.

Q3 *How does the variable switching frequency profile influence the supra-harmonics generated by the PFC converter?*

The impact of variable switching frequency on supra-harmonics has been largely overlooked despite the widespread application of Variable Switching Frequency Pulse Width Modulation (VSFPWM) techniques and the emergence of supra-harmonics emission standards. Chapter 4 pioneers the derivation of a generic harmonic spectrum model for AC-DC PWM converters under arbitrary periodic switching frequency profiles. To make this model practical, a fast acquisition algorithm based on vectorization is proposed. Both the accuracy of the harmonic spectrum model and the effectiveness of the proposed spectrum acquisition algorithm are validated through simulation and experimental results.

Moreover, Chapter 5 delves into the impact of P-VSFPWM on harmonic spectral properties, offering valuable design guidelines for filter design under P-VSFPWM. By optimizing frequency profiles, filters can be significantly reduced. Similarly, supra-harmonics emission can be curtailed through switching frequency profile optimization. Experimental verification of the optimal design points is conducted for both 2-level converter prototypes and 2-interleaved converter prototypes.

Q4 *How to ensure the control stability of the grid-connected converter with the LCL filter?*

The LCL filter is a common choice in AC-DC PFC converter systems for effectively attenuating switching frequency harmonics. However, its resonance can introduce instability without proper controller design. Chapter 6 addresses this challenge by implementing the capacitor-current feedback active damping technique, which requires only a simple gain feedback. Additionally, incorporating harmonics control into the controller becomes more complex due to the appearance of low-order voltage harmonics from the distorted grid voltage.

Chapter 6 first analytically identifies the stability boundary of the CCAD feedback gain under certain current controller parameters. Design guidelines, considering both gain and phase margin, are provided for proper implementation. The identified boundary is validated through both simulation and experimental tests.

7.2. FUTURE WORK

This thesis focuses on the design and operation of the front-end AC-DC converter of the EV charger under the variable switching frequency method. However, several research gaps still exist in the following areas, which require further investigation:

- **Benchmark between the 3-level T-type and the 2-interleaved converters**

  Chapter 2 compares the T-type and 2-interleaved converters in terms of efficiency and volume but does not analyze their switching harmonics performance. Future research could explore this aspect and extend the application of the TCM-ZVS method to both topologies to identify efficiency and power density limits more comprehensively. Such analysis would provide valuable insights for optimizing these converters for EV charger applications.

- **Impact of the variable switching frequency on the DC link**

  Chapter 4 presents a generic harmonics spectrum model under arbitrary periodic variable switching frequency profiles, including those used in the iTCM described in Chapter 3. The spread of harmonics spectrum with variable switching frequency poses challenges for modeling the DC link, as high-frequency current components flow into the DC link capacitor, leading to ESR and dielectric losses. Future research could focus on deriving these DC link current harmonics under P-VSFPWM to quantitatively analyze the power losses of DC link capacitors. Such analysis would enhance our understanding of the impact of variable switching frequency on DC link performance and guide optimization efforts.

- **Potential impact of the variable switching frequency on the controller design**

  The controller design presented in Chapter 6 assumes constant switching frequency. In digital implementations of variable switching frequency methods, the interrupt time for DSP control remains fixed while the PWM cycle duration varies according to the frequency profile. This dynamic variation in PWM cycle duration can introduce varying PWM delays, potentially affecting the gain and phase margin and leading to instability. Investigating the influence of variable switching frequency from a control perspective would provide valuable insights into addressing these challenges and ensuring stability in variable frequency control schemes.

APPENDIX

A

LOSS MODELING

A.1. SEMICONDUCTOR LOSSES

A.1.1. SWITCHING LOSSES

Assuming N switching cycles T_s in a fundamental period T_o during PWM process, the switching losses of the semiconductor can be modeled as:

$$P_\mathrm{sw} = \sum_{i=1}^{N} \frac{E_\mathrm{sw,i}}{T_\mathrm{o}} = \sum_{n=1}^{N} \frac{E_\mathrm{sw,i}}{N T_\mathrm{s}} = \sum_{i=1}^{N} \frac{E_\mathrm{sw,i} f_\mathrm{sw}}{N} \tag{A.1}$$

$$= \frac{f_\mathrm{sw} V_\mathrm{dc,sw}}{2\pi V_\mathrm{b}} \int_0^{2\pi} E_\mathrm{sw}(i_\mathrm{sw}) \mathrm{d}\theta \tag{A.2}$$

where E_sw is the switching energy (including turn-on energy E_on, turn-off energy E_off or diode reverse recovery energy E_rr), and can be extrapolated as the polynomial function of the switching current I_sw [42]. Besides, the switching losses must be scaled according to the switched voltage $V_\mathrm{dc,sw}$ and the datasheet reference voltage V_b [38].

A.1.2. CONDUCTION LOSSES

The forward characteristics of the power device such as IGBT and diode are approximated by the following linear equations:

$$v_\mathrm{T} = v + r \cdot i \tag{A.3}$$

where v represents the barrier voltage of the pn junction (threshold voltage in the datasheet) in the IGBT and diode, r stands for the on-state resistance of the device, and i is the instantaneous current flowing into the device. The conduction losses in the power semiconductor can be expressed as:

$$P_\mathrm{c} = \int_0^{2\pi} v_\mathrm{T}(\theta) i(\theta) \mathrm{d}\theta = v \cdot I_\mathrm{avg} + r \cdot I_\mathrm{rms}^2 \tag{A.4}$$

I_{avg} and I_{rms} are the average and RMS value of the current flowing through the device. The on-parameters v and r of the devices can be extracted from the current-voltage (I-V) curves provided in the datasheet or determined experimentally [135].

A.2. INDUCTOR LOSSES

The power losses in the inductor can be separated into core losses and winding losses:

$$P_{\text{ind}} = P_{\text{core}} + P_{\text{w}} \tag{A.5}$$

A.2.1. CORE LOSSES

The core losses are mainly comprised of three parts: hysteresis loss, eddy-current loss, and residual loss. The improved Generalized Steinmetz Equation (iGSE) is used to calculate the core losses of the triangular current waveform with the following equations:

$$P_{\text{core}} = \frac{V_{\text{core}}}{T} \int_0^T k_i \left| \frac{\mathrm{d}B}{\mathrm{d}t} \right|^{\alpha} (\Delta B)^{\beta-\alpha} \mathrm{d}t \tag{A.6}$$

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} \mathrm{d}\theta} \tag{A.7}$$

where V_{core} is the core volume, T is the period of the current, k, α and β are the Steinmetz parameters derived from the core material, and ΔB denotes the peak-to-peak flux density [112]. Assuming a toroidal core for the inductor, ΔB can be expressed by:

$$\Delta B = \frac{L I_{\text{pp}}}{N A} \tag{A.8}$$

where L is the inductance, I_{pp} is peak-to-peak current ripple, N is the number of turns, and A is the effective cross area.

In a three-phase AC-DC PWM converter, the boost inductor current comprises two components: a high-frequency component with a piecewise-linear waveform at the switching frequency, and a low-frequency component that exhibits a sinusoidal waveform at the mains frequency. The B-H loop corresponding to the low-frequency fundamental flux is identified as the major loop, while the high-frequency loops are designated as minor loops. This categorization allows for the independent assessment of losses associated with each loop type. Core losses are calculated by aggregating the losses from these individual loops and averaging them across the main period [54]:

A.2.2. WINDING LOSSES

The inductor winding losses are ohmic losses due to eddy currents, categorized into skin effect and proximity effect losses. The skin effect results from self-induced eddy currents reducing the effective cross-sectional area for current flow, while the proximity effect is due to eddy currents induced by the external alternating magnetic field affecting current distribution [112].

SKIN EFFECT

The skin effect losses P_{skin} including DC losses per unit length solid round conductors is:

$$P_{\mathrm{skin}} = R_{\mathrm{DC}} \cdot F_{\mathrm{R}}(f) \cdot \hat{I}^2 \tag{A.9}$$

where $\hat{I}$ is the peak current, f is the frequency of the current, R_{DC} is the DC resistance of the conductor per unit length, which is expressed by:

$$R_{\mathrm{DC}} = \frac{4}{\sigma \pi d^2} \tag{A.10}$$

where d is the diameter of the conductor and σ is the electric conductivity of the conductor material.

F_{R} is the ratio between DC and AC resistance, and can be approximated as:

$$F_{\mathrm{R}} = \frac{\xi}{4\sqrt{2}} \left(\frac{\mathrm{ber}_0(\xi)\,\mathrm{bei}_1(\xi) - \mathrm{ber}_0(\xi)\,\mathrm{ber}_1(\xi)}{\mathrm{ber}_1(\xi)^2 + \mathrm{bei}_1(\xi)^2} - \frac{\mathrm{bei}_0(\xi)\,\mathrm{ber}_1(\xi) + \mathrm{bei}_0(\xi)\,\mathrm{bei}_1(\xi)}{\mathrm{ber}_1(\xi)^2 + \mathrm{bei}_1(\xi)^2} \right) \tag{A.11}$$

where ξ can be calculated by:

$$\xi = \frac{d}{\sqrt{2}\delta}. \tag{A.12}$$

δ is commonly known as the skin depth

$$\delta = \frac{1}{\sqrt{\pi \mu_0 \sigma f}}. \tag{A.13}$$

PROXIMITY EFFECT

The proximity effect losses P_{prox} is modeled as:

$$P_{\mathrm{prox}} = R_{\mathrm{DC}} \cdot G_{\mathrm{R}}(f) \cdot \hat{H}_{\mathrm{e}}^2 \tag{A.14}$$

where $\hat{H}_{\mathrm{e}}$ is the magnitude of the external magnetic field strength and G_{R} is calculated by:

$$G_{\mathrm{R}} = -\frac{\xi \pi^2 d^2}{2\sqrt{2}} \left(\frac{\mathrm{ber}_2(\xi)\,\mathrm{ber}_1(\xi) + \mathrm{ber}_2(\xi)\,\mathrm{bei}_1(\xi)}{\mathrm{ber}_0(\xi)^2 + \mathrm{bei}_0(\xi)^2} + \frac{\mathrm{bei}_2(\xi)\,\mathrm{bei}_1(\xi) - \mathrm{bei}_2(\xi)\,\mathrm{ber}_1(\xi)}{\mathrm{ber}_0(\xi)^2 + \mathrm{bei}_0(\xi)^2} \right) \tag{A.15}$$

Both (A.9) and (A.14) evaluate the winding losses per unit length caused by each individual current harmonic existing in the inductor current. Finally, the winding loss can be obtained by summing up the losses under each harmonic frequency f_i:

$$P_w = l_{\mathrm{w}} \sum_{i=1}^{\infty} P_{\mathrm{skin}}(f_i) + l_{\mathrm{w}} \sum_{i=1}^{\infty} P_{\mathrm{prox}}(f_i). \tag{A.16}$$

where l_{w} is the winding length.

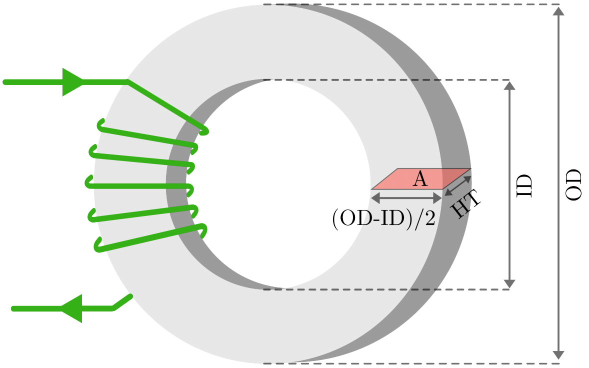


Figure A.1: Dimension of a toroidal core.

A.3. FILTER SIZE REDUCTION UNDER P-VSFPWM

Chapter 5 details the reduction of the required filter value, highlighting that the proposed P-VSFPWM can achieve an inductance reduction of up to 80% compared to the CSFPWM case. This section provides a quantitative analysis of the corresponding volume or size reduction of the inductor that results from the decreased inductance. Considering the inductor design based on a toroidal core as depicted in Fig. A.1, the inductance value L is determined by:

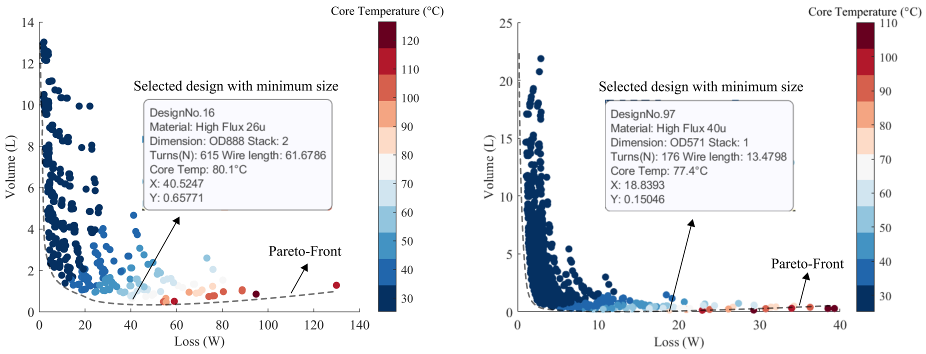
$$L = \frac{\mu_\mathrm{r}\mu_0 A}{l} \tag{A.17}$$

$$A = \frac{(OD - ID)}{2} HT \tag{A.18}$$

where μ_r and μ_0 are relative permeability and permeability in free space and N is the number of turns. A and l are the cross-sectional area and mean path length for magnetic flux. OD and ID are the outer and inner diameter of the toroidal core respectively while HT is the height (or thickness) of the core. Among them, A and l are directly associated with the core dimension in terms of the height and area size of the core. The maximum flux density should satisfy:

$$B_\mathrm{max} = \frac{LI_\mathrm{max}}{NA} = \frac{\mu_\mathrm{r}\mu_0 N I_\mathrm{max}}{l} \leqslant B_\mathrm{sat} \tag{A.19}$$

It can be noted from (A.19) that choosing a smaller core dimension (both A and l) results in an increased flux density. High-saturation core materials such as powder core and Metglas, utilized in this research, support a saturation flux density (B_sat) up to 1.5 T. This high saturation level allows for a significant reduction in core dimensions without risk of saturation. For the proposed P-VSFPWM, the inductor can theoretically be designed using a core that is 80% smaller in height (HT) providing the temperature rise is below the design requirement, leading to a comparable reduction in inductor volume. It is important to note that reductions should focus on core height rather than width (OD and ID), as reducing width does not necessarily decrease core volume. Unfortunately,



(a) Original CSFPWM

(b) Proposed P-VSFPWM

Figure A.2: Inductor design space (a) Original CSFPWM: f_{c0}=24.05 kHz, L=14.9 mH (b) Proposed P-VSFPWM ((triangle profile)): f_{c0}=24.05 kHz, f_b=9300 Hz, L=2.29 mH.

the commercial magnetic cores available on the market may not include a wide range of core heights. So the feasible way to realize this is to stack small core units. The inductor for the proposed P-VSFPWM can be hence realized by stacking fewer core units and this leads to a proportional reduction of volume and size.

An analytical design model for the inductor has been built to quantitatively identify the size reduction brought by the proposed P-VSFPWM. The model includes the converter PWM modeling introduced by Chapter 5, the inductor design and loss modeling from Appendix A.2, and the thermal model from [54, 112, 136]. The core shape is selected to be toroidal for simplicity. The core materials are based on the powder core materials from Magnetics Company such as “High-Flux”, “MPP”, “Kool” and “XFlux” [137]. Design spaces for both the original CSFPWM and the proposed P-VSFPWM are depicted in Fig.A.2, featuring a Pareto-front and color-coded inductor temperatures with a maximum limit set at 80°C. The optimal design point for minimal volume is identified in Fig.A.2, where the smallest inductor size for CSFPWM is 0.657 L (total for three phases) compared to 0.15046 L for P-VSFPWM, achieving a 77.1% reduction. This size reduction closely matches the reduction in inductance, suggesting that P-VSFPWM’s filter value reduction significantly decreases the filter size. Additionally, P-VSFPWM also results in lower inductor losses compared to CSFPWM, enhancing the overall converter performance.

B

INTEGRATING THREE-LEVEL T-TYPE CONVERTER WITH BESS

B.1. HARMONICS OF THREE-LEVEL CONVERTER

B.1.1. PHASE DISPOSITION SPWM (PD-SPWM)

In order to have a better understanding of derivations of the switching harmonics model, the development of analytical harmonic spectral solutions to the three-level converter based on PD-SPWM is revisited in this subsection. The general DFI-based approach to this analytical model has two steps: (1) construction of the two-dimensional (2-D) unit cell from the reference and carrier signals; (2) calculation of DFI based on the integral limits obtained from the first step [50]. The first step aims to determine the integral boundary from geometric insights and the second step is to solve the complex coefficients from DFI.

Generally, the phases of the carrier and reference signals are expressed by two variables x and y (or ω_c and ω_o):

$$\begin{cases} x(t) = \omega_\mathrm{c} t + \theta_\mathrm{c0} = \theta_\mathrm{c} \\ y(t) = \omega_\mathrm{o} t + \theta_\mathrm{o0} = \theta_\mathrm{o} \end{cases} \tag{B.1}$$

where ω_o and ω_o are the angular frequencies for the carrier and reference signals respectively, and θ_c0 and θ_o0 are the initial phases for the carrier and reference signals. A general carrier-based PWM waveform $f(x, y) = f(t)$ can be expressed in double-Fourier series in time domain:

$$f(t) = \Re\left(\frac{C_{00}}{2} + \sum_{n=1}^{\infty} C_{0\mathrm{n}} e^{-jny} + \sum_{m=0}^{\infty} \sum_{n=-\infty}^{\infty} C_\mathrm{mn} e^{-j(mx+ny)}\right) \tag{B.2}$$

The analytical solution to the output voltage of the three-level converter with natural sampling is derived and given in (B.3) by solving the complex-form coefficients C_mn as

$$
\begin{aligned}
v_c(t) = {} & \frac{MV_{dc}}{2}\cos(\omega_o t) + \frac{4V_{dc}}{\pi^2}\sum_{m=1}^{\infty}\sum_{k=1}^{\infty}\frac{J_{2k-1}([2m-1]\pi M)}{(2m-1)(2k-1)}\cos([2m-1]\omega_c t) \\
& + \frac{V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{J_{2n+1}(2m\pi M)\cos(n\pi)}{2m}\cos(2m\omega_c t + [2n+1]\omega_o t) \\
& + \frac{4V_{dc}}{\pi^2}\sum_{m=1}^{\infty}\sum_{\substack{n=-\infty \\ (n\neq 0)}}^{\infty}\sum_{k=1}^{\infty}\frac{J_{2k-1}([2m-1]\pi M)(2k-1)\cos(n\pi)}{(2m-1)(2k-1+2n)(2k-1-2n)}\cos([2m-1]\omega_c t + 2n\omega_o t)
\end{aligned}
\tag{B.3}
$$

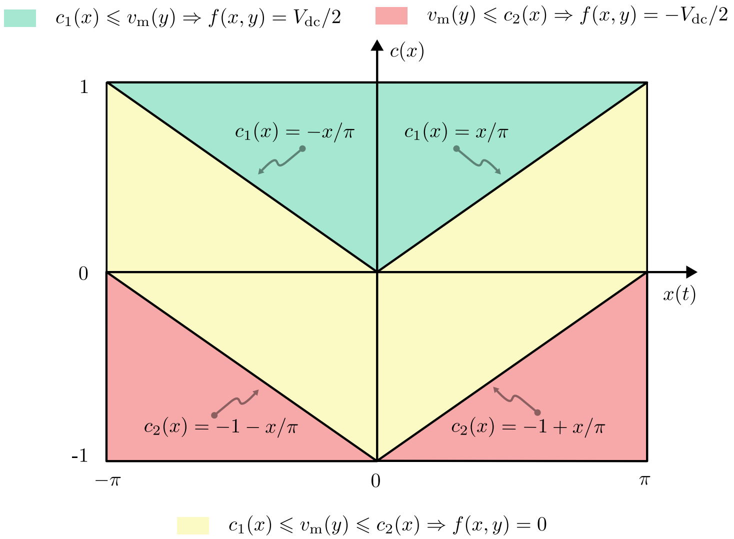

🟩 $c_1(x) \leqslant v_m(y) \Rightarrow f(x,y) = V_{dc}/2$
🟥 $v_m(y) \leqslant c_2(x) \Rightarrow f(x,y) = -V_{dc}/2$
$c(x)$
1
0
-1
$c_1(x) = -x/\pi$
$c_1(x) = x/\pi$
$x(t)$
$c_2(x) = -1 - x/\pi$
$c_2(x) = -1 + x/\pi$
$-\pi$
0
π
🟨 $c_1(x) \leqslant v_m(y) \leqslant c_2(x) \Rightarrow f(x,y) = 0$

Figure B.1: The carrier waveforms over one switching cycle for PD-based PWM.

Table B.1: THE DOUBLE-FOURIER INTEGRAL LIMITS FOR PD-BASED PWM.

$f(x,y)$	$-\pi \leqslant x \leqslant 0$	$0 \leqslant x \leqslant \pi$
$\frac{V_{dc}}{2}$	$v_m \geqslant -\frac{x}{\pi}$	$v_m \geqslant \frac{x}{\pi}$
0	$-1-\frac{x}{\pi} \leqslant v_m \leqslant -\frac{x}{\pi}$	$-1+\frac{x}{\pi} v_m \leqslant \frac{x}{\pi}$
$-\frac{V_{dc}}{2}$	$v_m \leqslant -1-\frac{x}{\pi}$	$v_m \leqslant -1+\frac{x}{\pi}$

follows:

$$
\begin{aligned}
C_{mn} &= A_{mn} + jB_{mn} \\
&= \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} V_c(x,y)e^{j(mx+ny)}\mathrm{d}x\mathrm{d}y
\end{aligned}
\tag{B.4}
$$

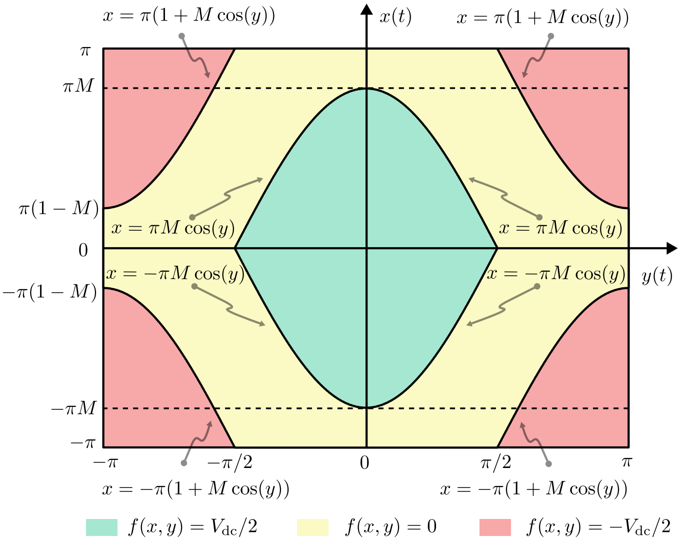


Figure B.2: Contour plot of f(x,y) in unit cell: PD-SPWM with natural sampling.

In (B.3), $J_n(x)$ is the Bessel function of the first kind. The modulation index M is defined as $2V_{ac}/V_{dc}$, ranging from 0 to $2/\sqrt{3}$ to avoid over-modulation. V_{ac} and V_{dc} are the magnitude of the AC phase voltage and DC bus voltage respectively. The successful derivation of (B.3) and (B.4) relies on the identification of the integral limits for C_{mn}. The carrier waveform of PD-PWM strategies is plotted in Fig. B.1 over one switching cycle, where three different regions are marked corresponding to the three output states of the three-level converter. By comparing the modulation reference with the carrier signals, the integration regions of (B.4) can be specified as listed in Table B.1. The contour plot of the PWM waveform in unit cell under PD-SPWM $f(x,y)$ is depicted in Fig. B.2, which also specifies the integral limits for PD-SPWM by simply substituting $v_m = M\cos(y)$ into Table B.1. It should be noted that the contour plot is necessary for the identification of the integral limits especially for the cases of more complicated PWM reference signals.

B.1.2. PHASE DISPOSITION DPWM1 (PD-DPWM1)

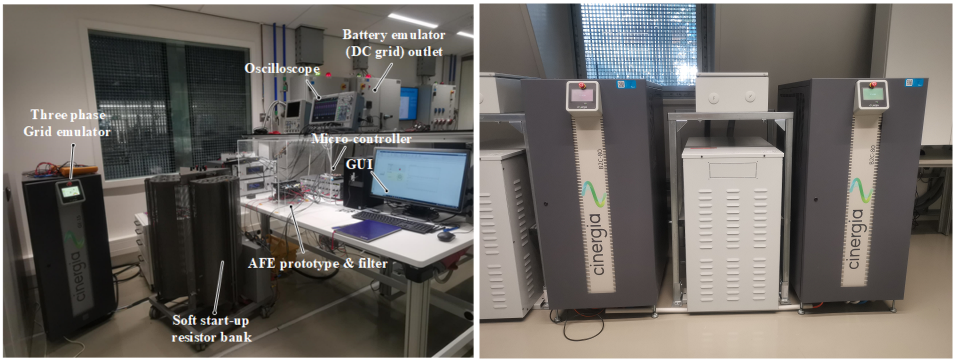
The modulation reference V_m of DPWM1 is analytically solved in six 60° sextants over a fundamental period 2π as summarized in Table B.2. The integral limits for PD-DPWM1 can be similarly derived by substituting v_m from Table B.2 into Table B.1. The contour plot for PD-DPWM1 is hence obtained and presented in Fig. 2.14. It can be noted from the contour plot that the expressions of the integral limits are different as M varies. For base-band harmonics ($m = 0$, $n > 0$), the harmonic coefficient C_{0n} is solved in (B.5). For $m > 0$, $n \geqslant 0$, the harmonic coefficient for carrier and side-band harmonics are derived in (B.6) and (B.7) for the two different M ranges.

Table B.2: MODULATION REFERENCE (PHASE A) FOR DPWM1.

Sector	$\boldsymbol{\theta_o}$	**Modulation reference** $\boldsymbol{v_m}$
I	$\frac{5\pi}{6} \leqslant \theta_o \leqslant \pi$	-1
II	$\frac{\pi}{2} \leqslant \theta_o \leqslant \frac{5\pi}{6}$	$1+\sqrt{3}M\cos(\theta_o+\frac{\pi}{6})$
III	$\frac{\pi}{6} \leqslant \theta_o \leqslant \frac{\pi}{2}$	$-1-\sqrt{3}M\cos(\theta_o+\frac{5\pi}{6})$
IV	$\frac{-\pi}{6} \leqslant \theta_o \leqslant \frac{\pi}{6}$	1
V	$\frac{-\pi}{2} \leqslant \theta_o \leqslant \frac{-\pi}{6}$	$-1+\sqrt{3}M\cos(\theta_o+\frac{\pi}{6})$
VI	$\frac{-5\pi}{6} \leqslant \theta_o \leqslant \frac{-\pi}{2}$	$1-\sqrt{3}M\cos(\theta_o+\frac{5\pi}{6})$
VII	$-\pi \leqslant \theta_o \leqslant \frac{-5\pi}{6}$	-1

B.2. T-TYPE CONVERTER WITH BESS EMULATOR

In order to demonstrate the capability of the prototypes for the integration of the battery storage system (BESS), the three-phase 3-level T-type prototype has been experimentally tested in closed-loop control to regulate the power-factor-correction (PFC) functionality while delivering power between the grid and BESS. Fig. B.3 shows the testbench and the battery emulator equipment for the battery emulation closed-loop test. The control scheme for the closed-loop test is illustrated in Fig.B.4(a), and the resulting test


Battery emulator
(DC grid) outlet
Oscilloscope
Three phase
Grid emulator
Micro-controller
GUI
AFE prototype & filter
Soft start-up
resistor bank
cinergia
B2C-80
cinergia
B2C-80
cinergia

(a) (b)

Figure B.3: BESS integration emulation test (a) Testbench (b) Two Cinergia power source(2X80 kW) as battery emulator

$$C_{0n} = \frac{V_{\mathrm{dc}}}{2}\underbrace{\left(\sin(\frac{n\pi}{2})\left(\cos(\frac{n\pi}{3}) - \cos(\frac{\pi}{3})\right)\left(\frac{8}{n} - \frac{4\sqrt{3}nM}{n^2-1}\right)\Bigg|_{n\geq 1}\right)}_{\text{1-D Fourier series coefficient of modulation reference } v_{\mathrm{m}}} \tag{B.5}$$

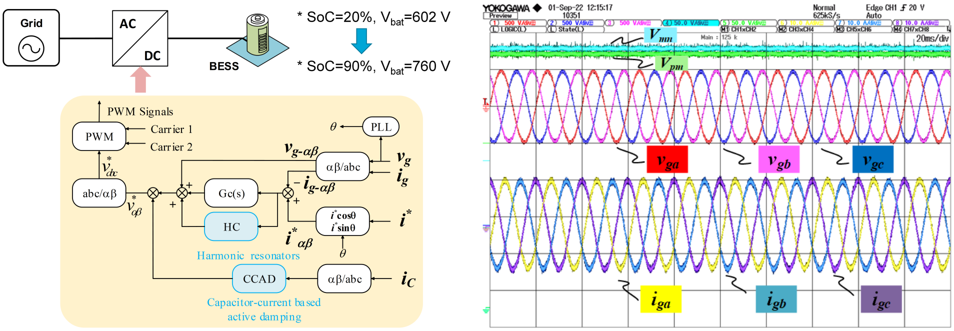
$0 \leqslant M \leqslant \dfrac{1}{\sqrt{3}}$:

$$C_{mn} = \frac{V_{\mathrm{dc}}}{m\pi^2} \times \left\{\begin{aligned}
&\frac{\pi\left(1+\cos(m\pi)\right)}{3}\sin^2(\frac{n\pi}{2})J_n(\sqrt{3}\pi mM)\sin(\frac{n\pi}{3}) + \\
&2\cos(m\pi)\cdot\sum_{k=1}^{\infty}\sin^2(\frac{k\pi}{2})J_k(\sqrt{3}\pi mM)\times \\
&\left[\frac{1}{n-k}\sin(\frac{2n-k}{3}\pi)\sin(\frac{n-k}{6}\pi)\Bigg|_{k\neq n} - \frac{1}{n+k}\sin(\frac{2n+k}{3}\pi)\sin(\frac{n+k}{6}\pi)\Bigg|_{k\neq -n}\right] + \\
&2\sum_{k=1}^{\infty}\sin^2(\frac{k\pi}{2})J_k(\sqrt{3}\pi mM)\times \\
&\left[\frac{1}{n+k}\sin(\frac{n+2k}{3}\pi)\sin(\frac{n+k}{6}\pi)\Bigg|_{k\neq -n} - \frac{1}{n-k}\sin(\frac{n-2k}{2}\pi)\sin(\frac{n-k}{6}\pi)\Bigg|_{k\neq n}\right]
\end{aligned}\right. \tag{B.6}$$

$\dfrac{1}{\sqrt{3}} \leqslant M \leqslant \dfrac{2}{\sqrt{3}},\ \theta = \cos^{-1}(-\dfrac{1}{\sqrt{3}M}) \in (\dfrac{2}{3}\pi, \pi)$:

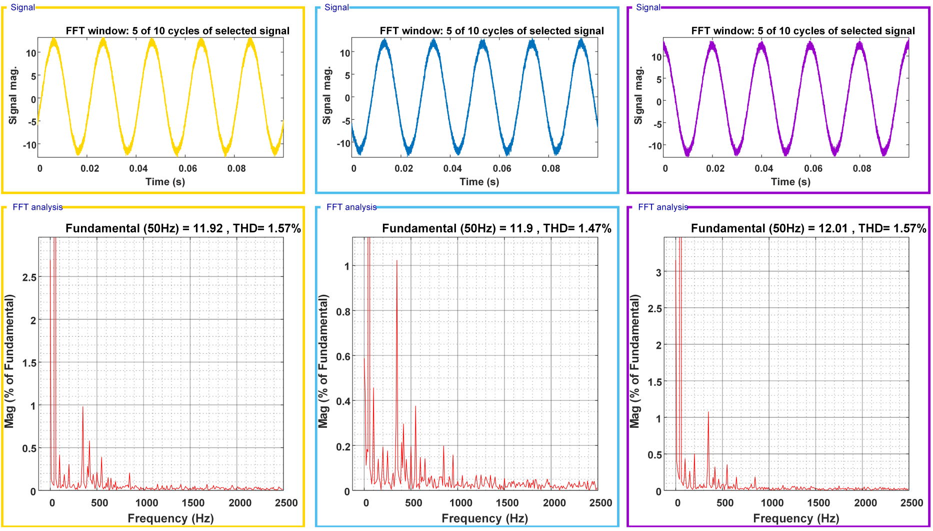
$$C_{mn} = \frac{V_{\mathrm{dc}}}{m\pi^2} \times \left\{\begin{aligned}
&\frac{\pi\left(1+\cos(m\pi)\right)}{3}\sin^2(\frac{n\pi}{2})J_n(\sqrt{3}\pi mM)\sin(\frac{n\pi}{3}) + \\
&2\cos(m\pi)\cdot\sum_{k=1}^{\infty}\sin^2(\frac{k\pi}{2})J_k(\sqrt{3}\pi mM)\times \\
&\left[\frac{1}{n+k}\left(\sin(\frac{n+k}{3}\pi)\sin(\frac{n-k}{6}\pi) - \sin(\frac{n+k}{2}\pi)\sin((n+k)\theta - \frac{2n+3k}{3}\pi)\right)\Bigg|_{k\neq -n} + \right. \\
&\left.\frac{1}{n-k}\left(\sin(\frac{n-k}{2}\pi)\sin((n-k)\theta - \frac{2n-3k}{3}\pi) - \sin(\frac{n-k}{3}\pi)\sin(\frac{n+k}{6}\pi)\right)\Bigg|_{k\neq n}\right] + \\
&2\sum_{k=1}^{\infty}\sin^2(\frac{k\pi}{2})J_k(\sqrt{3}\pi mM)\times \\
&\left[\frac{1}{n+k}\left(\sin(\frac{n+k}{2}\pi)\sin((n+k)\theta - \frac{2n+3k}{3}\pi) - \sin(\frac{2(n+k)}{3}\pi)\sin(\frac{n-k}{6}\pi)\right)\Bigg|_{k\neq -n} + \right. \\
&\left.\frac{1}{n-k}\left(\sin(\frac{2(n-k)}{3}\pi)\sin(\frac{n+k}{6}\pi) - \sin(\frac{n-k}{2}\pi)\sin((n-k)\theta - \frac{2n-3k}{3}\pi)\right)\Bigg|_{k\neq n}\right]
\end{aligned}\right. \tag{B.7}$$

waveforms are shown in Fig.B.4(b). During the test, the DC link voltage was charged to 700 V while delivering 5.8 kW of power from the grid to the battery. The waveforms demonstrate that the three-phase currents are in phase with the grid voltages, affirming the effective power factor correction (PFC) functionality of the three-phase 3-level T-type prototype. The currents maintained sinusoidal shapes, indicating excellent harmonic performance. As depicted in Fig. B.5, the total harmonic distortion (THD) of the three-phase grid currents ranged from 1.47% to 1.57%, significantly lower than the IEEE 519 standard requirement of less than 5%.


Grid
AC
DC
BESS
* SoC=20%, V_bat=602 V
* SoC=90%, V_bat=760 V
PWM Signals
PWM
Carrier 1
Carrier 2
θ
PLL
v_g-αβ
αβ/abc
v_g
i_g
v*_dc
abc/αβ
v*_αβ
Gc(s)
i_g-αβ
HC
i* cosθ
i* sinθ
i*
i*_αβ
Harmonic resonators
θ
CCAD
αβ/abc
i_C
Capacitor-current based active damping
YOKOGAWA
01-Sep-22 12:15:17
Normal 625kS/s
Edge CH1 20 V Auto
20ms/div
V_mn
V_pm
v_ga
v_gb
v_gc
i_ga
i_gb
i_gc

(a) (b)

Figure B.4: BESS integration emulation test (a) Closed-loop control scheme (b) Tested waveforms



(a) (b) (c)

Figure B.5: Total-harmonics-distortion (THD) of the grid-side currents (a) Phase-A (b) Phase-B (c) Phase-C

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LIST OF PUBLICATIONS

PUBLICATION RELATED TO THE THESIS

Journal papers

1. **Y. Wu**, J. Xu, T. B. Soeiro, M. Stecca and P. Bauer, "Optimal Periodic Variable Switching PWM for Harmonic Performance Enhancement in Grid-Connected Voltage Source Converters," *in IEEE Transactions on Power Electronics* vol. 37, no. 6, pp. 7247-7262, June 2022.

2. **Y. Wu**, J. Xu, T. B. Soeiro, P. Bauer and Z. Qin, "Frequency Design of Three-phase Active Front-End Converter with Reduced Filter in EV Chargers," *in IEEE Transactions on Transportation Electrification*, doi: 10.1109/TTE.2024.3381167.

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2. **Y. Wu**, Z. Qin, T. B. Soeiro, and P. Bauer, "Design Guideline for PWM Converter Implementing Periodic VSFPWM —A Comprehensive Analysis on the Harmonics Spectrum," *2023 11th International Conference on Power Electronics and ECCE Asia (ICPE 2023 - ECCE Asia),* Jeju Island, Republic of Korea, 2023, pp. 1509-1516.

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4. J. Sun, **Y. Wu**, T. B. Soeiro, Z. Qin and P. Bauer, "ZVS Turn-on integrated Triangular Current Mode Three-phase PFC for EV On-board Chargers," *2022 IEEE 20th International Power Electronics and Motion Control Conference (PEMC),* Brasov, Romania, 2022, pp. 285-294.

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OTHER PUBLICATIONS

Journal papers

1. A. Shekhar, T. B. Soeiro, **Y. Wu** and P. Bauer, "Optimal Power Flow Control in Parallel Operating AC and DC Distribution Links," *in IEEE Transactions on Industrial Electronics,* vol. 68, no. 2, pp. 1695-1706, Feb. 2021.
2. J. Xu, T. B. Soeiro, **Y. Wu** et al.„ "A Carrier-Based Two-Phase-Clamped DPWM Strategy With Zero-Sequence Voltage Injection for Three-Phase Quasi-Two-Stage Buck-Type Rectifiers," *in IEEE Transactions on Power Electronics* vol. 37, no. 5, pp. 5196-5211, May 2022.

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BIOGRAPHY

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