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Optimal Design of 100–2000 V 4H–SiC Power MOSFETs Using Multi-Objective Particle Swarm Optimization Algorithms

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***Abstract*— This work employed the particle swarm optimization (PSO) algorithm to assess the trade-off between breakdown voltage (BV) and on-state resistance ($R_{DS,on}$) in 4H–SiC metal oxide semiconductor field effect transistors (MOSFET) for power devices. In this work, the numerical model obtained after analyzing the resistance composition is utilized as the objective function in PSO to determine characteristic parameters in double-diffused metal oxide semiconductor field effect transistors (DMOSFET). These equations are input for the PSO algorithm. The derived characteristic parameters include the drift region doping concentration and thickness, cell size, channel length, JFET region length, JFET region thickness, and doping concentration. To adhere to common application constraints, this work optimizes these characteristic parameters to minimize the $R_{DS,on}$ under typical BV ranging from 100 to 2000 V. The $R_{DS,on}$ for some typical applications was extracted and validated through TCAD simulations to ensure algorithm accuracy. The reported results confirm that PSO yields superior outcomes and may be considered when designing devices. This work offers helpful insights into the design of characteristic parameters for 4H–SiC power DMOSFET devices and evaluates the feasibility of using PSO to optimize the characteristic parameters of power devices.**

***Index Terms*— SiC, MOSFETs, multi-objective optimization, particle swarm optimization.**

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I. Introduction

BECAUSE of its excellent physical properties, such as wide bandgap, high breakdown field, high thermal conductivity, and high saturated carrier drift velocity, 4H–SiC is an attractive material for high-power and high-temperature electronic devices [1], [2], [3], [4]. 4H–SiC MOSFETs play crucial roles in many power applications such as automotive controllers [5], on-board chargers [6], DC-to-DC converters [7], and photovoltaic inverters [8]. However, balancing the breakdown voltage and on-resistance remains a challenge when optimizing the key parameters of SiC MOSFETs [9].

Algorithm-based design optimization is used in device design. Although studies have reported the trade-off of middling electrical characteristics in 4H–SiC MOSFETs, these studies are typically limited to combining optimization objectives into a single weighted objective [10], [11], [12]. In contrast to conventional approaches, multi-objective optimization (MOO) excels at thoroughly exploring solutions to identify optimal solutions and providing a set of Pareto fronts [13]. In the context of power MOSFETs, the trade-off between breakdown voltage and on-state resistance necessitates the determination of a solution that minimizes on-state resistance without compromising the breakdown voltage. In this study, we used PSO to investigate the optimization design of 4H–SiC vertical MOSFETs, reduce the complexity and computation time of MOSFET structure design, and minimize the equivalent on-state resistance of devices within the range of 100–2000 V.

II. MOSFET Structure and Theoretical Basis for PSO

A. Resistance Composition for Numerical Models

To achieve accurate and efficient trade-offs among various electrical characteristics in MOSFETs using PSO, a detailed analysis of the numerical relationship between these electrical characteristics and the characteristic parameters was performed, as shown in Fig. 1(a) In this case, the channel resistance R_{Ch} can be expressed as follows:

$$R_{ch} = L_{ch}L_{cell}/2\mu_{ch}C_{ox}\left(V_G - V_{th}\right) \tag{1}$$

where L_{ch} is the channel length; L_{cell} is the cell length; $\mu_{ch} = 20cm^2/V \cdot s$ is the carrier mobility in the channel; V_G is the

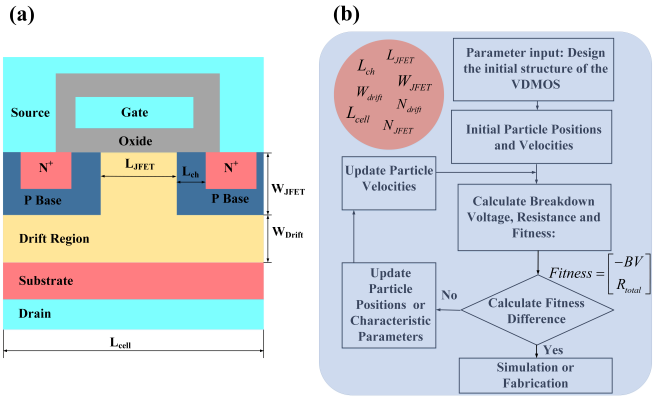

Fig. 1. (a) Cross-section of a 4H–SiC NMOS single cell, and (b) flowchart of the PSO.

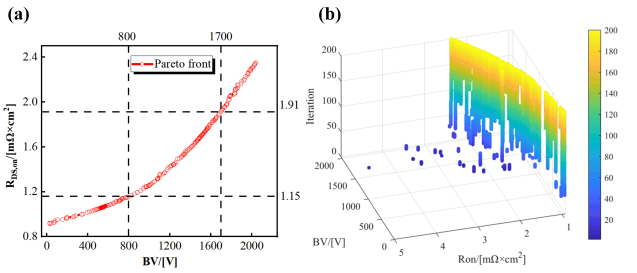

Fig. 2. (a) Pareto front distribution of $R_{DS,on}(X)$ and $BV_{DS}(X)$, and (b) the relationship between the number of iterations and the Pareto front of $R_{DS,on}(X)$ and $BV_{DS}(X)$.

gate voltage; C_{ox} is the gate oxide capacitance, which can be denoted as ε_{ox}/t_{ox}, where $t_{ox} = 40nm$ is the thickness of the gate oxide; and $V_{th} = V_{FB} + 2q\phi_{FB} + 2\sqrt{qN_A\varepsilon_s\phi_{FB}}/C_{ox}$ is the threshold voltage. The on-state resistance of the accumulation layer, drift region, and JFET region can be calculated separately, as follows:

$$R_A = \alpha L_{JFET} L_{cell} / 4\mu_a C_{ox} (V_G - V_{th}) \quad (2)$$

$$R_{JFET} = \rho_{JFET} L_{JFET} L_{cell} / \theta \quad (3)$$

$$R_{Drift} = \beta \rho_{Drift} W_{Drift} L_{cell} / (L_{cell} - \theta) \ln\left(L_{cell}/\theta\right) \quad (4)$$

where $\alpha = 0.6$ is the constant used to represent the losses incurred when current flows from the accumulation layer to the JFET region. L_{JFET} is the distance between the P base regions, μ_a is the carrier mobility in the accumulation layer, and ρ_{JFET} is the resistivity of the JFET region. θ is equal to $L_G\ 2W_{JFET}\ 2W_0$, where $L_G = 2.0\mu m$ is the length of oxide, $W_{JFET}$is the thickness of the JFET region or the P base region, and W_0 is the zero bias depletion width in the JFET region computed using $\sqrt{2\varepsilon_{sic} N_{Pbase} V_{bi}} / qN_{JFET}(N_{JFET} + N_{Pbase})$. V_{bi} can be calculated as $\ln\left(N_{Pbase} N_{JFET}/n_i\right) kT/q$. Here, β =0.8 is the constant used to represent the losses incurred when current flows from the JFET region to the drift region. n_i is the intrinsic carrier concentration, T is the temperature, which is set to room temperature (300 K), and q is the charge of an electron. The total on-state resistance can be expressed by simultaneously considering Equations (1) – (4).

Calculating the precise BV can be expressed as follows [10]:

$$BV = E_{pn} W_{drift} - qW_{Drift}^2 N_{Drift} / 2\varepsilon_{SiC} \quad (5)$$

where E_{pn} is the critical breakdown electric field, ε_{SiC} is the dielectric constant of 4H–SiC, and W_{Drift} is the thickness of the drift region.

PSO exhibits excellent convergence and optimization capabilities for multi-objective problems since it draws inspiration from the social behavior of bird flocks. Moreover, PSO provides a Pareto front consisting of multiple solutions, thereby allowing users to select the optimal solution based on their corresponding preferences. Fig. 1(b) shows a simplified PSO flowchart. In this study, the initial positions of particles correspond to the characteristic parameters of the device. We calculate the fitness and evaluate the termination criteria. Fitness is the quality of the solution set, while the termination criteria are typically based on fitness or the number of iterations. If the termination criteria are not satisfied, then particle velocities and positions are updated, and a new fitness is calculated. This process continues until the termination criteria are satisfied.

III. Optimizing the Characteristic Parameters of 4H–SiC MOSFET

In this section, optimization is based on the following design objective: to minimize $R_{DS,on}$ and simultaneously maximize the breakdown voltage within the range of 100–2000 V.

Two optimization objectives, i.e., $R_{DS,on}(X)$ and $BV_{DS}(X)$, are addressed here, where $X = W_{drift} N_{drift} L_{cell} L_{ch} W_{jfet} N_{jfet} L_{jfet}]$ is a vector of device characteristic parameters. The symbol X_i is used to represent the i-th characteristic parameter in X. Because of the size relationships obtained from the numerical model, X_1 should be greater than X_5; X_3 should be greater than X_7; and X_7 should be greater than X_4. Additionally, due to self-alignment process constraints, $X_4 \geq 0.4$and $X_7 \geq 0.8\ \mu$m. To obtain the $R_{DS,on}(X)$ of smaller-area cells, $X_7 \leq 5.0\ \mu$m. After randomly initializing the initial particles in a particle swarm with a population size of 300, 200 iterations were performed. Fig. 2(a) illustrates the Pareto front distribution of the objective function problem.

In this Pareto, we focused on specific voltage categories by constraining the drift region. By restricting the drift region's thickness to 10 μm, the breakdown voltage was limited to a maximum of approximately 2000 V, which resulted in an on-state resistance of 2.35 m$\Omega\times$cm^2. To confirm that the algorithm converged to the global optimum, a plot illustrating the relationship between the number of iterations and the optimization objectives was generated, as shown in Fig. 2(b) reveals that convergence occurs within the first 100 generations. The optimization with two objectives, seven design variables, and four constraints requires approximately 10 minutes.

In the initial 10 iterations, the two objective functions, i.e., $R_{DS,on}(X)$ and $BV_{DS}(X)$, were randomly distributed in the solution space. As the number of iterations increased, most particles gradually started moving toward higher-quality solutions. To be suitable for 250 and 450 V AC converters, we extracted the solutions with BV_{DS} of 800 and 1700 V.

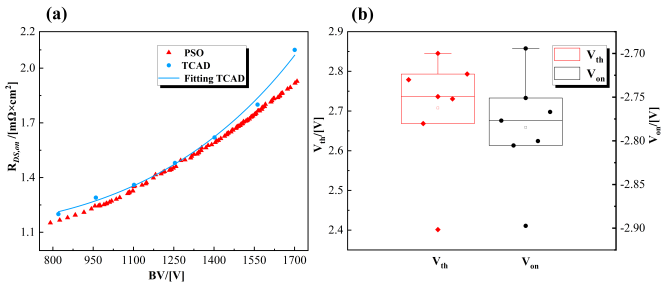

Fig. 3. (a) The difference between PSO and TCAD $R_{DS,on}(X)$ at seven different $BV_{DS}(X)$; (b) the distribution of threshold voltage and body diode conduction voltage for these seven devices.

TABLE I
CHARACTERISTIC SOLUTIONS FOR 800 AND 1700 V

Configuration parameters	BV_{DS} =800 V	BV_{DS} =1700 V
W_{drift} /[μm]	3.52	8.50
N_{drift} /[$\times 10^{16}$ cm^{-3}]	1.99	1.22
L_{cell} /[μm]	5.00	5.00
L_{ch} /[μm]	0.40	0.40
W_{jfet} /[μm]	0.97	1.08
N_{jfet} /[$\times 10^{16}$ cm^{-3}]	1.63	1.33
L_{jfet} /[μm]	0.83	0.80

The corresponding $R_{DS,on}$ values of 1.16 and 1.91 mΩ×cm^2 are shown in Table I.

Additionally, we verified the accuracy of PSO through TCAD simulation. Fig. 3(a) illustrates the $R_{DS,on}$ obtained from TCAD simulation and PSO. The device structure provided by PSO was simulated with a breakdown voltage range of 800–1700 V and a gradient of 150 V. The maximum error of $R_{DS,on}$ was within 0.19 mΩ×cm^2, which is about 8%. Lastly, the average error of $R_{DS,on}$ was within 0.06 mΩ×cm^2, which is about 3%. Compared with devices of the same type with similar BV and applications, the PSO used in this study yielded a lower on-state resistance [14]. Moreover, through TCAD simulations, we extracted the threshold voltage and conduction voltage of the body diode for these devices. The intended device had a threshold voltage of 2.500 V and a body diode conduction voltage drop of −2.800 V. The algorithm yielded solutions with an average threshold voltage of 2.771 V and an average body diode conduction voltage drop of −2.785 V. The solutions obtained from the algorithm closely match our objectives.

IV. CONCLUSION

This work utilized numerical simulations and MOOs to determine the characteristic parameters of power devices within the breakdown voltage range of 100 to 2000 V. A PSO algorithm was employed to investigate the trade-off between breakdown voltage and $R_{DS,on}$ in devices. We were able to determine the minimum on-state resistance corresponding to the breakdown voltage range. Additionally, the $R_{DS,on}$ corresponding to typical application breakdown voltages of 800 and 1700 V were extracted (i.e., 1.16 and 1.91 mΩ×cm^2, respectively). Moreover, we verified the accuracy of the algorithm through TCAD. The average error of $R_{DS,on}$ was within 0.06 mΩ×cm^2 (∼3%) and the maximum error of $R_{DS,on}$ was within 0.19 mΩ×cm^2 (∼8%). Finally, we verified the threshold voltage and the third-quadrant characteristics of the MOSFET through TCAD simulations, and we found excellent alignment between the solutions provided by the algorithm and the objectives. Thus, the proposed PSO-based MOO algorithm can be used in the optimal design of 4H–SiC power MOSFETs.

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