Design of a Current-Mode Rectifier with ESD-Conscious Resonance Management

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CONTENTS

SUMMARY

This work addresses the efficiency loss and waveform clipping that occur in implantable or small-form-factor inductive power transfer (IPT) receivers when the LC tank's negative half-cycle is clamped by the lower-rail ESD diodes. We propose a *lifted-bias* receiver that inserts a series, pre-charged lift capacitor ($C_{\text{lift}} \approx 12\,\text{V}$) beneath the LC tank to raise its DC level, so the resonant waveform swings cleanly within 0–24 V instead of crossing 0 V. The architecture alternates 24 V and 12 V delivery in a four-stage cycle. The tank is tuned to 13.56 MHz with $L \approx 900\,\text{nH}$ and $C \approx 154\,\text{pF}$ ($Q \approx 60$). To minimize I^2R and C_{ds} losses and avoid slow turn-off backflow, two high-side drivers are implemented: SW1 operates with ~ 12–17 V gate drive and ~ 900/700 ps rise/fall times, and SW3 with ~ 7–12 V and ~ 500/300 ps. Control uses amplitude-based termination and a COILP-referenced reset to switch deterministically between the 24 V and 12 V paths while sustaining C_{lift}. Steady-state simulations yield $P_{\text{av}} = 40.00\,\text{mW}$, $P_{\text{in}} = 25.41\,\text{mW}$, and $P_{\text{out}} = 23.28\,\text{mW}$, corresponding to PTE = 55.79% and PCE = 87.82%; compared with representative alternatives, the scheme provides high voltage without a post-boost stage and is intrinsically immune to lower-rail ESD clamping. Limitations include the need for an external ~ 1 μF capacitor and a 7 V Zener bias that add quiescent loss, the use of idealized comparators in simulation, and periodic time slots allocated to replenishing C_{lift}; future work will target low-quiescent biasing, comparator integration, and optimized C_{lift} management.

1

INTRODUCTION

Implantable medical devices (IMDs) are moving toward smaller form factors, longer service life, and higher functional integration across applications from cardiac pacing to neural interfaces and chronic monitoring. These trends elevate power delivery from a peripheral to a defining constraint for clinical usability and patient safety. [1]–[3]

Relying solely on primary batteries is problematic: the cell occupies a large share of the implant volume, has finite lifetime that triggers replacement surgery, and scales poorly as sensing/stimulation workloads and telemetry throughput increase (i.e., average power consumption rises with capability and duty cycle). Consequently, *while non-invasive replenishment is attractive and increasingly explored in selected applications, most IMDs still rely on non-rechargeable primary cells with typical service lives of ~3–12 years*; wireless power is primarily considered to reduce replacement surgeries and/or battery size. [1], [2] Among various options, *near-field resonant inductive coupling (NRIC)—also referred to as inductive power transfer (IPT)—* has emerged as a mature choice for shallow implants, supporting millimeter-to-centimeter link distances within medical safety limits and enabling practical recharging workflows. [1], [2]

Miniaturization, however, compresses the receiver (Rx) coil area (often ≤1–2 cm diameter), pushing the link into a weak-coupling, power-limited regime. Tissue conductivity adds eddy-current and resistive losses that depress Q and power transfer efficiency (PTE), while geometric and orientation tolerances aggravate detuning. *Coil geometry, the matching/compensation networks (e.g., series/parallel compensation, L-match) with frequency tuning, and the operating frequency must therefore be co-designed—and, when needed, actively tuned—to counter resonance-frequency detuning from tissue loading and misalignment while shaping the load seen by the transmitter*, with printed spiral coils (PSCs) and transmitter optimization playing a central role. [1], [4], [5] Within these constraints, simply increasing transmit power is not viable due to specific absorption rate (SAR) and temperature-rise limits; the *receiver-side efficiency* becomes the dominant lever.

Prior work addresses receiver robustness by stabilizing the delivered voltage against misalignment and load variation—via simple two-element network shaping or closed-

loop control—so the implant can remain within both electrical and thermal budgets. [2], [6] For ultra-low incident power, *current-mode* receivers offer a complementary path: by accumulating energy over multiple cycles in a resonant tank and directly charging from inductor current, they can circumvent diode conduction and regulator start-up thresholds, thereby lowering the minimum harvestable input power and improving low-power efficiency. [7] These insights motivate our focus on receiver architectures and parameter choices that maximize end-to-end efficiency under tight size and safety constraints.

Overview of this thesis. Chapter 2 (Literature Review) surveys receiver strategies—including current-mode ideas—and practical issues such as ESD interaction at the LC node. Chapter 3 (Architecture) develops a bias-lifted, receiver-centric solution that mitigates negative half-cycle conduction while targeting MHz operation. Chapter 4 (Implementation) details component selection and circuit realization under implant constraints. Chapter 5 (Evaluation) defines power-flow metrics and reports representative results to validate feasibility in weak-coupling, power-limited conditions.

2

Literature Review

2.1. Current mode inductive Power Receiver: Architecture and Operating Principle

2.1.1. Introduction to Inductive Power Transfer

Wireless Power Transfer (WPT) is a technology that enables energy transmission from a source to a load without physical connections. It is widely used in applications such as medical implants, consumer electronics, and electric vehicles. Among various WPT methods, Inductive Power Transfer (IPT) is commonly employed due to its efficiency and reliability. IPT operates based on electromagnetic induction, where an alternating current in the transmitter coil generates a time-varying magnetic field, inducing an electromotive force (EMF) in a nearby receiver coil to facilitate energy transfer [8] (see Figure 2.1).

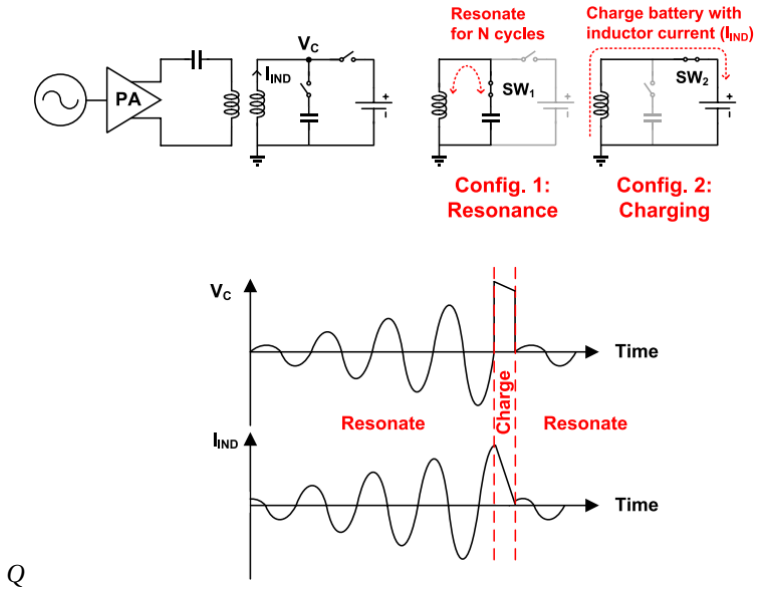
The efficiency of IPT depends on the mutual inductance M between the coils and the coupling coefficient k, defined as:

$$k = \frac{M}{\sqrt{L_1 L_2}}$$

where L_1 and L_2 are the self-inductances of the transmitter and receiver coils, respectively. A higher k and high-quality factor Q contribute to improved power transfer efficiency [8]. Here, Q denotes the quality factor, defined as the ratio of the energy stored in the resonator to the energy dissipated per cycle.

2.1.2. Current-Mode IPT: Resonant Energy Accumulation and Direct Charging

Unlike conventional IPT systems that rely on voltage-mode operation with rectifiers and regulators, Current-Mode IPT improves energy efficiency by leveraging resonant energy storage and direct current transfer. As illustrated in Figure 2.1, this method consists of two primary operational phases [7]:



Q

Figure 2.1: Block diagram of the proposed resonant current-mode wireless power transfer system, showing resonance and energy-delivery modes with corresponding waveforms [7].

1. **Resonance Mode:** The receiver coil is connected to a parallel capacitor to form an LC tank, which resonates for multiple cycles, accumulating energy before transferring it to the load [7].

2. **Delivery Mode:** After sufficient energy accumulation, a switching circuit routes the inductor current (I_{IND}) directly to the energy buffer/load (e.g., a storage capacitor); prior designs often target battery charging [7], but our prototype is batteryless.

This resonant current-mode IPT technique reduces the minimum required input power by eliminating rectifier threshold limitations and optimizing energy transfer cycles. Additionally, by delivering inductor current directly to the energy buffer/load, it enhances power efficiency at low input-power levels—making the approach suitable for implantable, ultra-low-power systems. While many implementations use it for battery charging [7], in this work we explicitly adopt a batteryless receiver that accumulates charge on a storage capacitor and powers the implant via a downstream regulator.

2.1.3. LC RESONANCE AND ENERGY ACCUMULATION

FORMATION OF THE LC TANK

As shown in Figure 2.2, LC parallel resonant circuit consists of an inductor (L) and a capacitor (C) connected in parallel, forming a system where energy oscillates between the electric field in the capacitor and the magnetic field in the inductor. The resonant

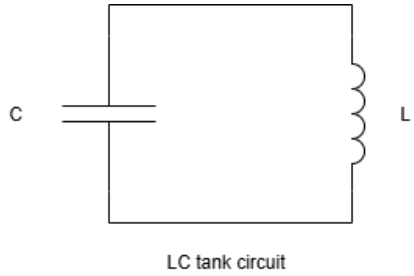


Figure 2.2: Simple LC Tank[9]

angular frequency (ω_0) is determined by:

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

where $\omega_0 = 2\pi f_0$, and f_0 is the resonant frequency.

RESONANT FREQUENCY AND QUALITY FACTOR

The circuit's quality factor (Q) characterizes its energy efficiency and is defined as

$$Q \triangleq 2\pi \frac{\text{energy stored}}{\text{energy dissipated per cycle}}. \tag{2.1}$$

For a lightly damped (*high-Q*) *series* RLC resonator, this reduces to the common approximation

$$Q \approx \frac{\omega_0 L}{R_s} \approx \frac{1}{\omega_0 R_s C}, \tag{2.2}$$

and for the *parallel* RLC form,

$$Q \approx \frac{R_p}{\omega_0 L} \approx \omega_0 R_p C, \tag{2.3}$$

where R_s and R_p denote the equivalent series and parallel resistances, respectively. These closed-form expressions are **approximations valid only for larger** Q. A higher Q-factor minimizes energy losses and enables efficient energy storage and transfer [8].

ENERGY ACCUMULATION

The energy relationship in this system can be divided into two main aspects:
1. Energy Exchange Between Inductor and Capacitor In the LC tank, energy alternates between the capacitor's electric field and the inductor's magnetic field. When the capacitor discharges, electric energy is converted to magnetic energy as current flows into the inductor. As the magnetic field decreases, the inductor generates a back electromotive force (EMF), recharging the capacitor. This cycle continues at the natural resonant frequency, sustaining oscillations within the circuit [7].
2. Energy Amplification Through Resonance Under external excitation, such as electromagnetic induction, the LC circuit resonates at its frequency ω_0. At resonance, the

reactive components largely cancel, so the source primarily supplies the tank's effective losses, enabling efficient accumulation of input energy over multiple cycles. Consequently, the in-tank voltage and current can become significantly larger for a given input. The high Q-factor further enhances this effect, allowing the LC tank to store significant energy before transferring it to the load [7].

2.1.4. SWITCHING CONTROL AND RECTIFICATION

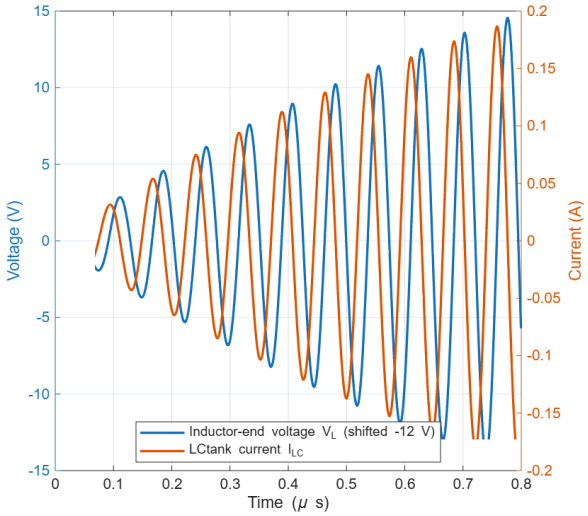


Figure 2.3: Energy accumulation in the LC tank over time (left axis: inductor-end voltage V_L, shifted by -12 V; right axis: LC tank current I_{LC}).

SWITCHING STRATEGY.

In this system, the objective is to accumulate maximum energy within the shortest possible oscillation period, *because dissipative losses accumulate with dwell time (a resonator loses roughly $2\pi/Q$ of its stored energy per cycle).* As shown in Figure 2.3, the energy stored in the LC tank depends heavily on the resonance duration: a longer period generally leads to higher voltages and more stored energy, but also increases parasitic losses—undesirable for applications requiring short, high-power bursts. Thus, there is a trade-off between extending resonance to capture more energy and keeping it brief to reduce losses and rapidly deliver power.

To implement this strategy, the switching device (e.g., a MOSFET) must be triggered at an optimal phase. By detecting when the inductor's energy nears its peak and reaches our requirement, the control logic can terminate the oscillation before significant losses arise. Later sections explore how oscillation period, resonant frequency, and parasitic parameters further refine this methodology.

RECTIFICATION AND DISCHARGE–ENERGY TRANSFER TO THE LOAD.

Once resonance is terminated, the control circuit connects the inductor to the load, steering the previously stored energy through a unidirectional path that charges or pow-

ers the load in a DC manner. As shown in Figure 2.1, the discharge path enforces one-way conduction, which inherently provides rectification. Through repeated oscillation followed by rapid discharge, the system achieves AC-to-DC conversion while maintaining efficiency and fast transient response, and remains compatible with downstream regulation stages.

2.1.5. SUMMARY

Inductive power transfer systems achieve efficient energy transfer and amplification at resonance by optimizing the coupling coefficient k and quality factor Q. The LC resonant circuit alternates energy between the inductor and capacitor, effectively accumulating external excitation energy. Precise switching control shortens oscillation periods, balancing energy storage and minimizing losses. Finally, rectification efficiently transfers the stored energy to the load as a stable DC output, meeting short-burst high-power demands and enabling further filtering or regulation.

2.2. FUNDAMENTALS OF ESD PROTECTION AND CURRENT LIMITATION

2.2.1. INTRODUCTION TO ELECTROSTATIC DISCHARGE (ESD) AND ITS THREATS TO CIRCUITS

Electrostatic Discharge (ESD) refers to the sudden and rapid transfer of electrostatic charge between two objects at different potentials. This phenomenon commonly occurs in both natural and artificial environments, with typical sources including triboelectric charging (e.g., frictional contact between materials) [10].

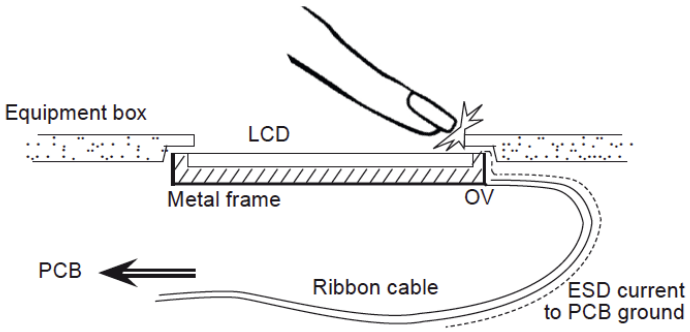


Figure 2.4: ESD entry path with LCD displays [11]

ESD poses a universal challenge in circuit design as it can occur at various stages in a device's lifecycle and across diverse environments. For instance, during manufacturing or handling, operators may accumulate electrostatic charge on their bodies through everyday activities such as walking or interacting with insulative materials. When a charged operator touches a sensitive electronic component, the static electricity rapidly discharges into the circuit, creating a voltage spike that exceed the component's tolerance, leading to damage [11]. Figure 2.4 shows a common ESD entry path via an LCD dis-

play assembly, illustrating how discharge events can reach sensitive components. Additionally, ESD can also be introduced through frictional charging caused by contact with automated equipment or via inductive coupling [12][10].

In semiconductor devices, ESD represents a significant threat to circuit reliability. MOS devices are especially vulnerable due to their thin gate oxides and intricate structures. ESD can result in various types of damage:

Dielectric rupture: When the electric field strength exceeds the dielectric breakdown voltage of an insulating material, it leads to the formation of a conductive path through the dielectric. This phenomenon is not limited to any specific region and can occur in various insulating layers, including but not limited to the gate oxide in MOSFETs [13].

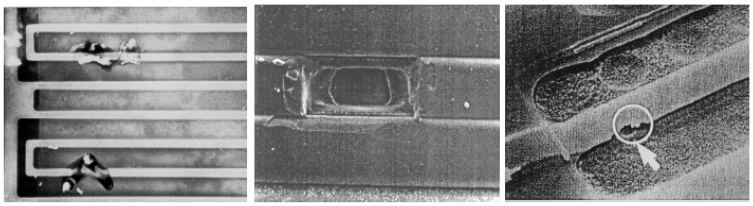


Figure 2.5: ESD Failures in ICs: (a) Junction Breakdown, (b) Metal/Via Damage, (c) Gate Oxide Damage[12]

Junction filamentation: As shown in Figure 2.5(b), high current densities lead to localized heating that melts silicon in p–n junctions, *often initiated when the reverse-biased junction enters breakdown (Figure 2.5(a))*, forming conductive paths that result in short circuits or increased leakage currents [12], [13].

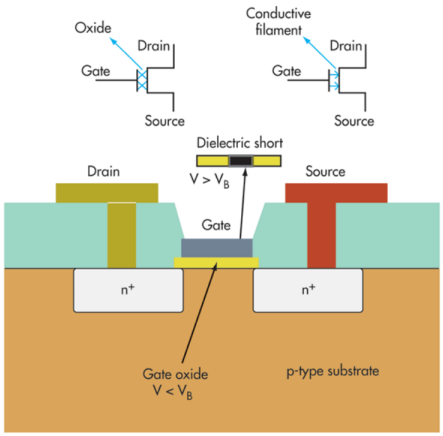


Figure 2.6: Gate Oxide Breakdown in MOSFETs [12]

Gate oxide damage: As a specific form of dielectric rupture, it occurs in MOSFETs when the thin gate oxide is subjected to ESD stress. As shown in Figure 2.5(c) and Figure 2.6, the excessive electric field creates a conductive path through the oxide layer,

resulting in abnormal gate leakage current, an inability of the gate to properly control the channel current, and ultimately complete device failure [12][13].

Given these risks, ESD protection is critical in circuit design. **First,** preventive measures must shield sensitive components from damage. **Second,** the protection mechanisms must ensure the circuit remains functional and reliable under normal operating conditions. **Third,** ESD protection solutions should minimize their impact on circuit performance [12][13].

2.2.2. ESD PROTECTION CHALLENGES IN LC TANK CIRCUIT

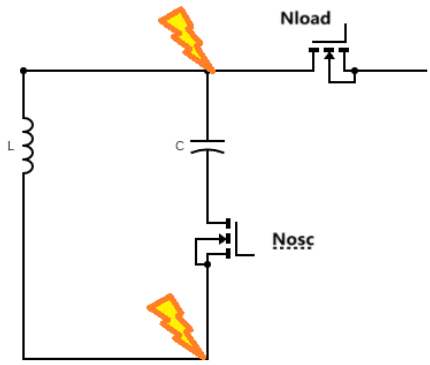


Figure 2.7: Circuit structure and ESD threat

The LC tank circuit consists of an inductor (L) connected in parallel with a branch composed of a capacitor (C) in series with an NMOS transistor (N_{osc}), which controls the on-off state of the oscillating circuit. Additionally, another NMOS transistor (N_{load}) connects the LC node to the load. This N_{load} remains off during oscillation and closes when the oscillation stops, allowing the energy stored in L to discharge into the load.

As the inductor (L) is an external component, it acts as the primary entry point for ESD events, which can propagate through the circuit and directly impact the two NMOS transistors, N_{osc} and N_{load}.

For N_{osc}, the drain is connected to the capacitor while the source is connected to the inductor. ESD events can lead to transient high currents at the source, causing localized heating and potential junction filamentation, while high voltages at the drain can cause gate oxide breakdown or short circuits.

For N_{load}, with its drain connected to the LC node and source connected to the load, ESD events occurring during its conduction phase can couple into the load and induce damage. The resulting current surges can also create conductive paths between the drain and source, degrading the functionality of the transistor.

Key nodes in the circuit require ESD protection to prevent damage and ensure reliable operation. The node between L and C is exposed to transient behavior from the inductor, making it vulnerable to high-energy spikes. Similarly, the connection between L and N_{osc} is critical, as voltage or current surges can disrupt its function. The load con-

nection node involving N_{load} is also sensitive during conduction, where ESD spikes may couple into the load or degrade N_{load}'s performance.

Without adequate ESD protection, failures in N_{osc} or N_{load} could severely impact circuit functionality. If N_{osc} malfunctions, LC ceases, preventing the circuit from generating a stable signal. A failure in N_{load} would hinder energy delivery to the load; more critically, when N_{load} is ESD-damaged (stuck-off or severe leakage), the inductor cannot properly discharge during the charging mode, depriving the circuit of its primary "charging" function. The residual energy then remains trapped in the LC tank and accumulates across cycles, increasing node swing and device stress, and ultimately raising the risk of oxide breakdown, parasitic latch-up, and permanent system failure.

2.2.3. TRADITIONAL ESD PROTECTION METHODS AND THEIR PRINCIPLES

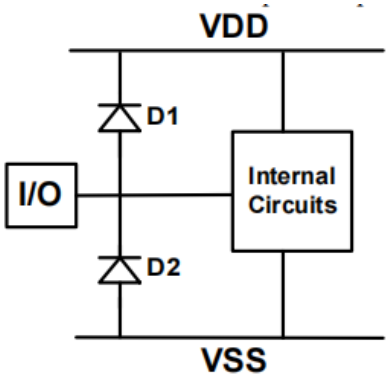


Figure 2.8: Traditional ESD Protection Structures [14]

TRADITIONAL ESD PROTECTION STRUCTURES

Traditional ESD protection circuits are widely used in CMOS integrated circuits to protect sensitive components from ESD events. Among these, the two-diode structure is a fundamental and effective approach for I/O pad protection, as illustrated in Fig.2.8 of the referenced document [14]. During an ESD event, these diodes quickly turn on, providing a low-impedance path for transient currents, thus clamping the voltage at the I/O pad and protecting the internal circuitry [14].

OPERATING PRINCIPLES OF THE TWO-DIODE PROTECTION

When an ESD event induces high-voltage spikes at the I/O pad, the two diodes (D_1 and D_2) change their biasing states according to the polarity of the spike, thereby providing voltage clamping protection.

- If the ESD event causes a positive voltage spike (I/O pad voltage exceeds V_{DD}), diode D_1 switches from reverse bias to forward bias. In this state, D_1 conducts, directing the ESD current from the I/O pad to the V_{DD} power rail. This clamping action effectively limits the I/O pad voltage to within the safe range of V_{DD}, protecting the internal circuitry from damage caused by the voltage spike.

- If the ESD event causes a negative voltage spike (I/O pad voltage drops below V_{SS}), diode D_2 switches from reverse bias to forward bias. Here, D_2 conducts, directing the ESD current from the V_{SS} ground rail back to the I/O pad. This clamping mechanism ensures that the I/O pad voltage remains within the safe range of V_{SS}, preventing damage from negative voltage spikes.

- Under normal operating conditions, the I/O pad voltage remains within the range $V_{SS} \leq V_{I/O} \leq V_{DD}$. In this case, both D_1 and D_2 are reverse-biased, preventing current flow through the diodes. This ensures that the ESD protection circuit does not interfere with normal circuit operation, maintaining the stability and long-term reliability of the system.

ADVANTAGES AND LIMITATIONS

The two-diode structure offers several advantages, including a low trigger voltage, fast response time, and seamless integration with CMOS processes. However, its effectiveness can be constrained by the size of the diodes and their ability to dissipate heat during high-energy ESD events. Additionally, minimizing leakage current under bias is essential to ensure reliability during normal operation. For specific circuits, such as high-frequency or specialized topologies, the parasitic effects and high-frequency characteristics of the diodes may further affect performance, as will be discussed in subsequent sections [15].

2.2.4. CHALLENGES OF APPLYING TRADITIONAL ESD PROTECTION IN LC TANK CIRCUITS

Applying traditional ESD protection methods, such as diodes connected between the LC node and ground, poses significant challenges when used in LC tank circuits. These limitations arise from the inherent characteristics of LC and the high-frequency resonance behavior of the circuit.

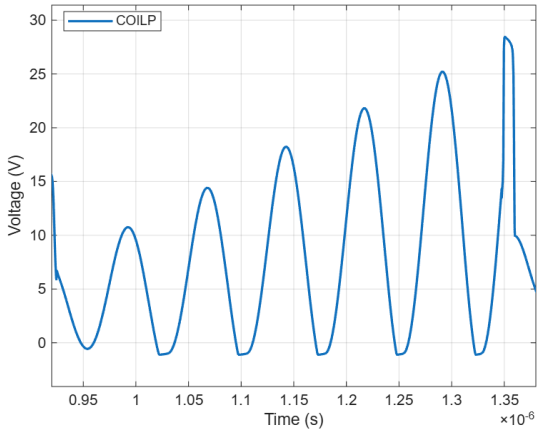


Figure 2.9: LC node voltage with a traditional ESD diode: the negative half-cycle is clamped near −0.7 V

The LC tank circuit in this application is designed to oscillate with a target amplitude of ±12V. During operation, the inductor (L) accumulates sufficient energy, and the circuit

disconnects from the load. However, introducing a traditional ESD protection diode at the LC node significantly disrupts this behavior. Due to the energy exchange between L and C, the oscillating voltage follows a sinusoidal trajectory. During the negative half-cycle, once the voltage drops below approximately -0.7V, the ESD diode to ground becomes forward-biased and conducts, providing a low-impedance discharge path for the tank, as shown in Fig. **??**. Consequently, in the subsequent positive half-cycle, less energy is available and the peak remains below +12V; this limitation is due to the clamp action rather than conduction of the opposite ESD diode (which would only occur if the node approached $V_{\mathrm{DD}} + V_f$).

Additionally, the diode's junction capacitance introduces a parasitic element into the resonance loop, causing slight deviations in the natural oscillation frequency. This effect may interfere with precise frequency control but is secondary to the more significant issue of voltage clamping and energy dissipation.

Given these challenges, traditional ESD protection methods are unsuitable for LC tank circuits. Therefore, to achieve both effective ESD protection and reliable LC , alternative protection strategies are required. These strategies must address the limitations of traditional methods while preserving the critical performance and resonance characteristics of the LC tank circuit. In the following sections, we will explore tailored solutions designed specifically for these requirements.

2.3. ALTERNATIVE ESD STRUCTURES & TECHNIQUES

2.3.1. USING HIGH VOLTAGE ESD PROTECTION DIODES

HIGH THRESHOLD VOLTAGE DIODES: PIN DIODES, ZENER DIODES, AND MORE

To address the limitations of traditional ESD protection methods, higher threshold voltage diodes such as PIN diodes, Zener diodes, and high-voltage diodes can be used [16]. These diodes feature increased forward voltage thresholds, reducing the likelihood of early conduction under normal circuit conditions, particularly during negative oscillations.

DETAILED ANALYSIS OF PIN DIODES

Figure 2.10 shows the cross-sectional structure of a PIN diode. PIN diodes differ from standard PN junction diodes by introducing an intrinsic (I) layer between the P-type and N-type regions, which significantly increases the forward voltage threshold (V_{th}). For example, with an intrinsic layer thickness of 175 μm, a PIN diode exhibits a forward current of only 0.097 μA at a 10 V forward bias, indicating that increasing the intrinsic layer thickness substantially raises V_{th} and delays conduction at lower voltages [18].

This characteristic makes PIN diodes particularly effective in applications requiring higher forward voltage thresholds. For ESD protection, the high threshold voltage of PIN diodes helps prevent charge leakage during negative oscillations.

LIMITATIONS OF PIN DIODES

PIN Diodes and Intrinsic Layer Thickness Figure 2.11 shows that meeting our requirement $V_{\mathrm{th}} > 12$ V demands an intrinsic-layer thickness exceeding ~ 100 μm; in general, a thicker I-layer shifts the forward knee to higher voltages and thus raises V_{th} [18], [19]. However, a $t_i > 100$ μm device is difficult to integrate in standard IC flows—sustaining

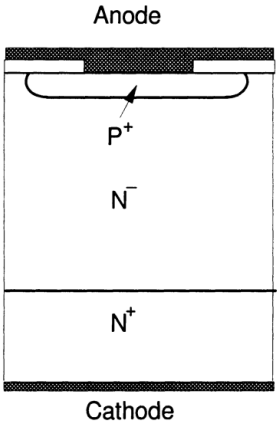


Figure 2.10: Cross-sectional structure of a typical P-i-N diode [17]

ESD surge current without excessive heating typically requires enlarging the device cross-sectional area, which inflates on-chip footprint and conflicts with compact, high-density layouts [18]. Moreover, the thick intrinsic region slows carrier filling; under nanosecond-scale ESD pulses the device can lag in reaching a low-resistance state, delaying clamping and allowing a higher peak stress on the protected node [19]. In summary, while increasing t_i suppresses unintended turn-on at low bias, achieving $V_{\text{th}} > 12$ V by pushing t_i beyond 100 μm carries prohibitive area overhead and degrades transient protection for our application.

High-Threshold ESD Protection Trade-Offs Elevating V_{th} lowers the likelihood of conduction during oscillation, reducing energy leakage. However, higher thresholds decrease ESD protection efficiency by delaying the clamp response to transients [16]. Consequently, the device may fail to suppress sudden voltage spikes promptly, risking overvoltage damage and compromising circuit reliability.

2.3.2. USING TRANSIENT VOLTAGE SUPPRESSION (TVS) DIODES

INTRODUCTION TO TVS DIODES

Transient Voltage Suppression (TVS) diodes are specifically designed to protect circuits from transient voltage spikes, such as those caused by ESD events. TVS diodes are highly efficient in clamping high voltages and are widely used in modern electronic systems due to their fast response times and high energy-handling capabilities [20]. Structurally, TVS diodes resemble Zener diodes but are optimized for transient events rather than steady-state operation [21].

PRINCIPLE AND I-V CHARACTERISTICS OF TVS DIODES

TVS diodes function by clamping excessive voltage surges within nanoseconds when a transient spike occurs. As shown in Figure 2.12, when the reverse voltage exceeds the diode's breakdown voltage (V_B), the device enters avalanche breakdown mode, provid-

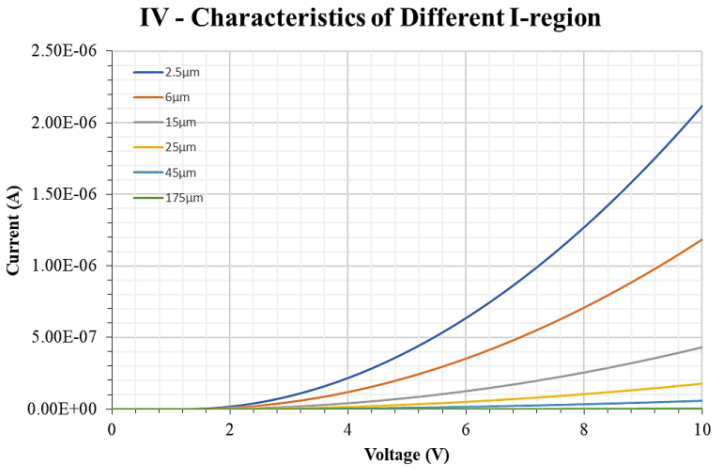


Figure 2.11: I-V curve of Pin diode with different intrinsic layer thickness [18]

ing a low-impedance path to divert transient current away from sensitive components. Unlike Zener diodes, which operate primarily in the deep breakdown region for voltage regulation, TVS diodes leverage the near-breakdown region to suppress transient overvoltages effectively. The I-V characteristics indicate minimal leakage current below V_B, followed by a sharp increase in current when the diode begins clamping[21].

For high-frequency circuits, the performance of TVS diodes depends on their parasitic capacitance [22]. While lower capacitance TVS diodes are available, they may still interfere with high-frequency oscillations in circuits like LC tanks, where the operating frequency can reach tens of megahertz. This interference may shift the resonant frequency and reduce the quality factor [22].

LIMITATIONS OF TVS DIODES

Despite their excellent transient response, TVS diodes present certain challenges when applied to LC tank circuits. One major issue is their physical size. To handle higher voltages and energy levels, TVS diodes require larger junction areas, leading to increased device dimensions [23]. This larger size is not ideal for modern compact and high-density designs, especially in space-constrained applications.

Additionally, the parasitic capacitance of TVS diodes, while low compared to some alternatives, can still affect high-frequency resonance in LC circuits. This capacitance introduces unwanted shifts in the circuit's natural frequency and may degrade quality, which is critical for applications requiring precise frequency control [22].

In summary, while TVS diodes offer a viable solution for ESD protection due to their fast transient response, their size and parasitic effects limit their suitability for high-frequency, high-amplitude LC tank circuits.

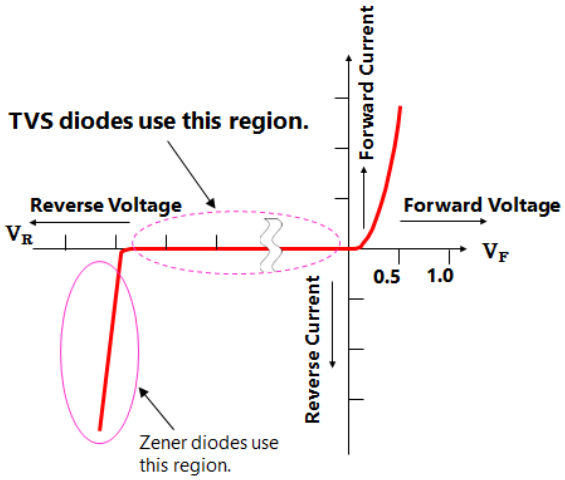


Figure 2.12: I-V Characteristics of TVS and Zener Diodes

2.4. FREQUENTLY SWITCHING MOSFET CLAMPS

2.4.1. INTRODUCTION TO MOSFET CLAMPING TECHNOLOGY AND CIRCUIT ANALYSIS

MOSFET CLAMPING OVERVIEW

MOSFET clamping is widely used in power electronics and resonant circuits to regulate voltage, prevent damaging swings, and enhance efficiency. Their high-speed operation, low on-resistance, and active controllability make them ideal for high-frequency environments such as LC resonators, power converters, and switching circuits [24]. By placing a MOSFET between a critical node and a reference potential, voltage excursions are dynamically limited, reducing conduction losses. Notable applications include[24][25]:

- **Active Clamp Forward Converters**: Employ an auxiliary MOSFET to reset the transformer core and reduce voltage spikes[24].
- **Flyback Converters**: Recycle leakage energy to increase efficiencys[24].
- **Overvoltage Protection Circuits**: Act as active clamps to prevent excessive voltage surgess[24].
- **Resonant Circuit Clamping**: Dynamically regulate voltage waveforms in LC circuits, preventing excessive negative excursions and maintaining stable resonance[24][25].

In contrast to passive diodes, MOSFETs provide dynamic control by adapting to changing conditions, which lowers conduction losses by minimizing body diode operation. Their high-speed switching makes them ideal for RF and resonant circuits. Specifically in LC resonant applications, MOSFET clamping safeguards sensitive components by preventing voltages from dropping below critical levels, thus ensuring stable performance.

Our design leverages this principle to maintain LC resonance stability and avoid detrimental negative voltage swings[24][25].

MOSFET CLAMP CIRCUIT

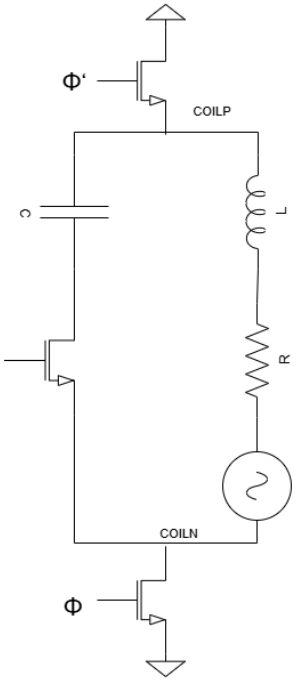


Figure 2.13: Schematic of the MOSFET clamping

Our design implements MOSFET-based clamping in a parallel LC tank circuit to ensure that the voltage at the resonant nodes does not fall below zero. This is achieved by employing two MOSFETs connected to the two junctions between the inductor (L) and capacitor (C). During the positive half-cycle of resonance, the connected MOSFET remains off, allowing the corresponding LC junction to oscillate freely, while the other side of MOSFET turns on, clamping the opposite LC junction to ground. Conversely, in the negative half-cycle, the switching roles reverse. This ensures that the LC tank remains symmetrically oscillating while avoiding negative voltage dips, enhancing the overall system stability and efficiency.

2.4.2. MOSFET CLAMPS CURRENT RECTIFICATION SIMULATION RESULT

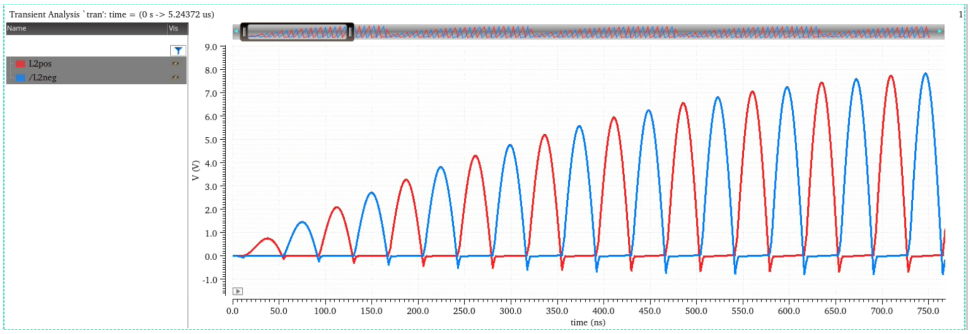


Figure 2.14: Voltage signal at positive side and negative side of LC tank

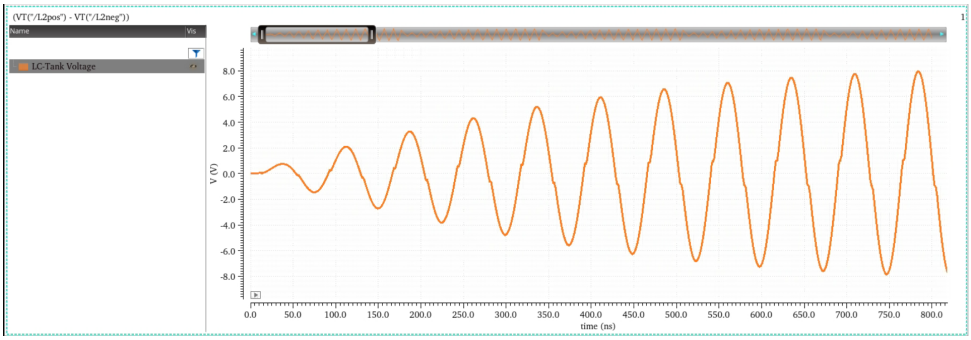


Figure 2.15: Resonant voltage signal of the LC tank with MOS clamping (VLpos-Vlneg)

VOLTAGE CLAMPING

The simulation results shown in Figure 2.14 and Figure 2.15 confirm that V_{Lpos} **and** V_{Lneg} maintain their positive half-cycle signals without interference. During their respective negative half-cycles, both remain above zero due to effective MOSFET clamping. With no charge leakage, the energy easily accumulated in the LC tank, ensuring stable resonance. By computing $V_{Lpos} - V_{Lneg}$, we reconstruct the original LC oscillation signal, free from ESD constraints and faithfully representing the circuit's natural resonance behavior as shown in Figure 2.15

SIGNAL CONTROL

As shown in Figure 2.16 and Figure 2.17, to obtain the desired output above, the control signals of the NMOS transistors used for Clamping are synchronized with the oscillation voltage waveform to ensure proper clamping operation. When the oscillation voltage reaches the negative half-cycle, the control signal of the corresponding NMOS transistor increases, turning it on and pulling the node voltage to ground, thereby preventing it from dropping further. Conversely, during the positive half-cycle, the NMOS transistor is turned off, allowing the node voltage to oscillate freely without interference.

By implementing this clamping mechanism, the two critical ESD protection node voltages are consistently maintained above zero, preventing the ESD protection diodes

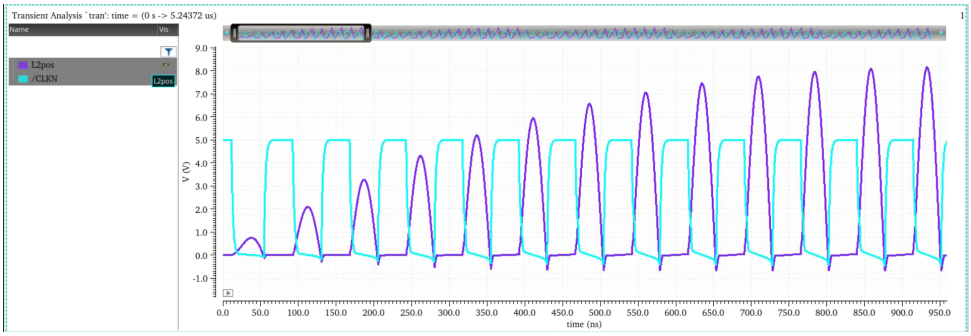


Figure 2.16: Control signal of upper clamping nmos (square wave) and voltage signal at positive side of LC tank (sine wave)

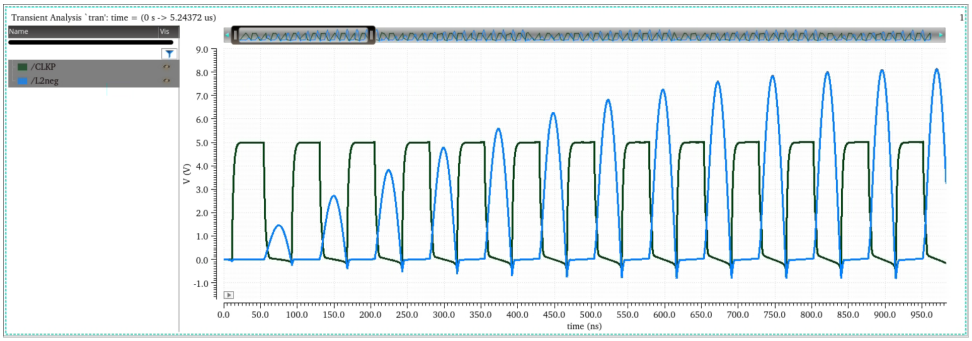


Figure 2.17: Control signal of lower clamping nmos (square wave) and voltage signal at negative side of LC tank (sine wave)

from conducting and avoiding unwanted energy leakage. However, in the simulation, we also observed certain drawbacks of this structure, which will be discussed in the following sections.

ISSUES INTRODUCED BY MOSFET CLAMPING

Although the MOSFET clamps prevent negative voltage swings in the LC tank by periodically grounding each node during its negative half-cycle, this approach necessitates frequent switching. The clamp switches state each half-cycle, requiring the same control signal frequency relative to the LC operating frequency. In our design, with an operating frequency of 13.56 MHz, the control must toggle at 13.56 MHz as well, leading to increased power loss and reduced energy transfer efficiency.

A simplified expression for switching power dissipation in MOSFET gates is:

$$P_{\text{sw}} = \frac{1}{2} C_{\text{gate}} V_{\text{DD}}^2 f_{\text{SW}},$$

where C_{gate} is the effective gate capacitance, V_{DD} is the drive voltage, and f_{SW} is the switching frequency. As f_{SW} grows, dynamic losses rise proportionally, further constraining overall system efficiency at higher operating frequencies. Here, efficiency is defined

as

$$\eta = \frac{\langle P_{\text{out}} \rangle}{\langle P_{\text{in}} \rangle} \times 100\%, \qquad P_{\text{out}}(t) = V_{\text{out}}(t) I_{\text{out}}(t), \quad P_{\text{in}}(t) = V_{\text{coil}}(t) I_{\text{coil}}(t),$$

where $\langle \cdot \rangle$ denotes time-averaging over the steady-state window and $V_{\text{coil}} I_{\text{coil}}$ is the instantaneous power received at the inductor (coil) port. Under this definition, simulation results confirm the detrimental impact of frequent clamp switching on η.

This clamp solution effectively prevents the ESD diode from conducting during the oscillator's negative half-cycles, thereby avoiding unwanted energy leakage. However, its frequent switching causes additional dynamic losses and significantly reduces the overall efficiency of the system.

2.5. TAPPED CAPACITOR FOR VOLTAGE DIVISION

Impedance matching involves adjusting the impedance of components within a resonant power transfer circuit to ensure efficient energy transfer and minimize signal reflections.

2.5.1. CIRCUIT DESCRIPTION

One effective technique for achieving impedance transformation is the tapped capacitor network, which consists of two capacitors (C_1 and C_2) in series with an inductor (L) as shown in Figure 2.18. This structure enables better impedance matching by modifying the voltage distribution across the circuit.

This alternative oscillation structure introduces two capacitors, C_1 and C_2, alongside the inductor L. The circuit operates in two distinct modes: *oscillation mode* and *discharge mode*, controlled by NMOS switches located in the capacitor branch and output path.

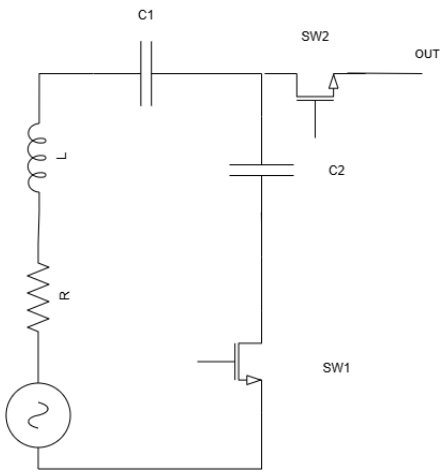


Figure 2.18: Schematic of tapping capacitance resonance circuit

OSCILLATION MODE

- Capacitors C_1 and C_2 are connected in series and together form a parallel resonance with L. - The NMOS in the capacitor branch is closed, creating the C_1-C_2-L parallel structure for oscillation. - The NMOS in the output path is open, isolating the load from the circuit during resonance.

DISCHARGE MODE

- Capacitor C_2 is disconnected, and C_1 forms a series connection with L to drive the load. - The NMOS in the capacitor branch is open, preventing current flow to C_2. - The NMOS in the output path is closed, connecting C_1 and L to the load, enabling energy transfer to the output.

The output terminal is positioned between C_1 and C_2, ensuring that charge leakage issues associated with traditional ESD protection during oscillation are mitigated.

2.5.2. TRADITIONAL ESD PROTECTION WITH TAPPED CAPACITOR CIRCUITS

In the traditional LC tank design, ESD protection diodes connected to the LC node can cause charge leakage during negative oscillation phases. By modifying the circuit structure as described, this issue is mitigated in the following ways:

SERIES CONFIGURATION OF C_1 AND C_2:

During oscillation, the series connection of C_1 and C_2 reduces the voltage amplitude across each capacitor, limiting the potential for ESD diode conduction. By changing the ratio of C_1 and C_2, the division of voltage ensures that the remains within the safe range of the ESD diodes' conduction thresholds.

ISOLATION OF C_2 IN DISCHARGE MODE:

In discharge mode, C_2 is entirely disconnected, ensuring that it does not contribute to leakage paths or additional parasitic effects. This structural separation allows C_1 to focus on delivering energy to the load without interference.

The combination of these configurations ensures that traditional ESD protection remains effective without causing charge leakage that disrupts oscillation performance.

2.5.3. ANALYSIS OF LIMITATION OF TAPPING CAPACITANCE RESONANT CIRCUIT

MATHEMATICAL MODELING AND OBSERVATIONS

To analyze the tapping capacitance resonant circuit, we developed a mathematical model using Mathematica (modeling code is provided in the appendix). The model captures the behavior of the circuit in both oscillation and discharge modes, allowing us to observe how energy is exchanged between the inductor (L) and capacitors (C_1, C_2) across multiple cycles.

One critical issue identified is the impact of C_1's position in the inductor's discharge path. Since C_1 remains in the discharge loop, it accumulates residual charge after each cycle, leading to a progressive offset shift in subsequent oscillations. This phenomenon is evident in the inductor voltage waveforms.

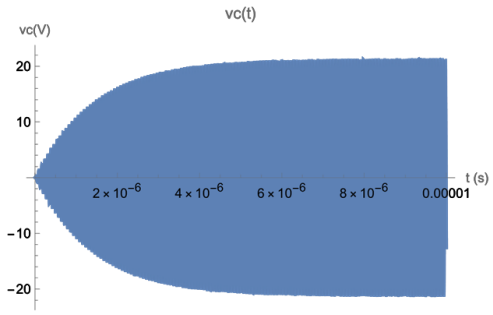


Figure 2.19: Inductor voltage in the first cycle resonance mode, centered around 0V.

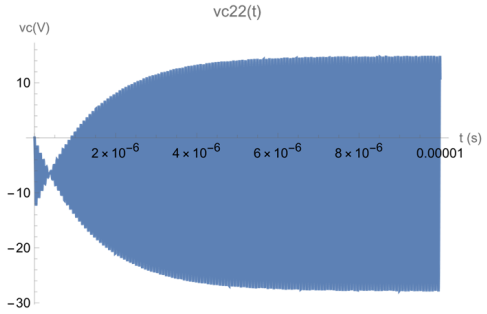


Figure 2.20: Inductor voltage in the second cycle resonance mode, shifted to -6.5V.

As shown in Figure 2.19, during the first resonance cycle, the oscillation starts from 0V, with output voltage and amplitude gradually increasing to 12V. However, in Figure 2.20, by the second resonance cycle, the baseline has shifted to -6.5V, requiring larger amplitude and more time to reach 12V output.

This progressive offset causes several efficiency-related problems. With each cycle, more time is needed for the oscillation to reach full amplitude, reducing the system's ability to sustain efficient energy transfer. The shifted baseline distorts the expected symmetry of voltage and current waveforms, leading to phase imbalance. Over time, the circuit deviates from its intended resonance behavior, impacting stability and predictability.

STRATEGY FOR ADDRESSING THE ISSUE

To counteract this issue, we propose modifying the mode transition strategy. The original method switches from discharge mode back to resonance mode when the inductor current (I_L) reaches zero. Instead, we suggest switching when C_1's voltage (V_C) reaches zero. This approach ensures that any residual charge on C_1 is neutralized before entering the next oscillation phase. A comparison of these two switching strategies is shown in Figure 2.21. Figure 2.21(a) illustrates the original switching method (at $I_L = 0$), where C_1 accumulates charge over multiple cycles, causing an increasing voltage offset. Figure 2.21(b) shows the proposed method (at $V_C = 0$), which effectively resets C_1 each cy-

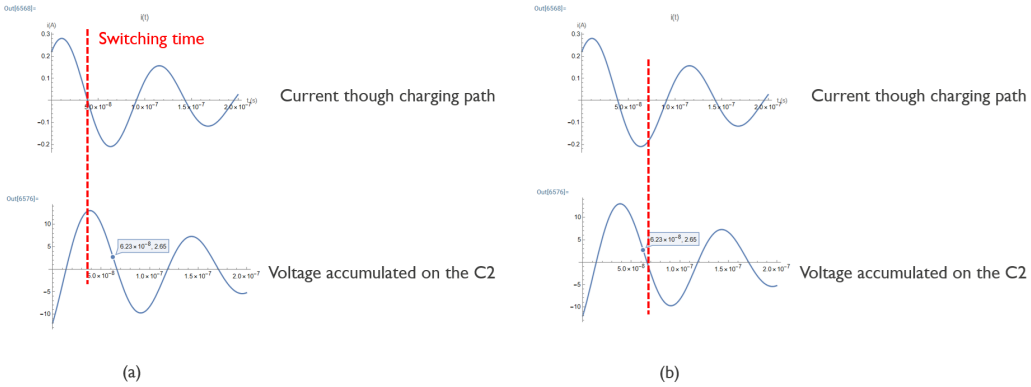


Figure 2.21: Inductor current and C1 voltage under two switching strategies (a)original strategy; (b)suggested strategy

cle, preventing offset accumulation.

However, while this strategy prevents charge buildup and stabilizes the oscillation waveform, it introduces a major drawback. Since the circuit now switches modes when $V_C = 0$, less energy is stored and transferred per cycle. To ensure $V_C = 0$, a portion of the charge must be returned from the load to balance the charge on C_1. This feedback process prevents the complete transfer of energy to the load, effectively reducing the overall power delivery efficiency. Calculation results confirm that this modification significantly lowers the energy transfer capability of the circuit. Specifically, the original switching strategy ($I_L = 0$) achieves an energy transfer efficiency of approximately 0.8 (80%), whereas the alternative strategy ($V_C = 0$) reduces efficiency to below 0.4 (40%).

2.5.4. CONCLUSION

The tapped capacitor solution mitigates charge accumulation and voltage drift by modifying the resonance structure, effectively stabilizing oscillations. However, due to the need for charge balancing, it introduces a trade-off between maintaining a stable oscillation baseline and energy transfer efficiency, with the revised switching strategy significantly reducing power delivery.

2.5.5. TAPPED INDUCTOR

Besides the tapped capacitor, we can also make use of the tapped inductor. In traditional IPT (Inductive Power Transfer), we want to get a higher output voltage at the load end, we often need to let the resonant voltage rise to the target amplitude (for example, 12 V) before switching to discharge.

In this scheme, the tapped inductor is formed by two inductors, L_1 and L_2, which are connected to a capacitor C and a load through a switch network. By reconfiguring the connections, the circuit operates in two distinct modes:

1. Resonant Mode (Energy Storage) In this mode, L_1 and L_2 are connected in parallel with the capacitor C, so that a lower peak voltage (e.g., 6 V) can accumulate sufficient energy.

2. Discharge Mode (Output) Once enough energy has been stored in the resonant tank, the capacitor C is bypassed or disconnected, and inductors L_1 and L_2 are switched into series connection, thereby adding their voltages together (e.g., from 6 V to 12 V) and delivering this higher voltage to the load over a short interval to rapidly transfer the stored energy.

ADVANTAGES OVER A SIMPLE LC TANK

This design offers several advantages: it reduces the required resonant peak voltage (e.g., 6 V instead of 12 V), minimizing waiting time; improves energy transfer efficiency by shortening resonant cycles and lowering voltage swings while boosting the output voltage through parallel-to-series inductor switchings.

LIMITATION OF TAPPED INDUCTOR

Despite its advantages, this structure has notable drawbacks. First, it requires a more complex switch network and control signals. In the original circuit, only two switches were needed to alternate between operating modes, whereas the introduction of additional switches significantly increases MOSFET driving losses due to higher dynamic power consumption. Second, unlike the tapped capacitor approach, this circuit does not resolve the charge leakage issue in the negative half-cycle caused by the ESD diode. To mitigate this, the previously proposed MOSFET clamp structure shown in Figure 2.13 is still necessary, further exacerbating dynamic losses. Due to these limitations, this structure is not considered for implementation.

2.6. SUMMARY

This chapter explored various circuit architectures to improve Inductive Power Transfer (IPT) efficiency while addressing charge leakage caused by Electrostatic Discharge (ESD) diodes. The primary challenge stems from negative half-cycle oscillations, which unintentionally activate ESD diodes, leading to energy dissipation and reduced efficiency. Several alternative methods were analyzed, each with distinct advantages and limitations.

Comparison of Existing Solutions The following table summarizes the key characteristics of these methods:

Conclusion Each method offers trade-offs: high-voltage ESD diodes reduce early conduction but compromise transient response, while TVS diodes provide fast protection but interfere with resonance. The tapped capacitor mitigates charge leakage but sacrifices power efficiency, and the tapped inductor reduces resonant voltage but adds complexity and switching losses. MOSFET clamping effectively prevents negative voltage swings but suffers from high dynamic losses.

Method	Advantages	Disadvantages
High-Voltage ESD Diodes (PIN/Zener)	Higher conduction threshold, reduces leakage	ESD threat, large size, parasitic resistance/capacitance issues
TVS Diodes	Fast transient response, effective ESD protection	Parasitic capacitance affects resonance, large physical size
Tapped Capacitor	Reduces charge leakage, improves impedance matching	Unstable resonance status, lowers power transfer efficiency
Tapped Inductor	Lowers resonant voltage, boosts efficiency	Complex switching, increased MOSFET losses, still needs clamp
MOSFET Clamping	Prevents negative voltage swings, stabilizes resonance	High switching frequency, increased dynamic power loss

Table 2.1: Comparison of Circuit Structures

Since none of these approaches fully resolve all issues, in Chapter 3, we propose a novel circuit structure to achieve efficient energy transfer while addressing the identified drawbacks.

3

ARCHITECTURE

Building on the literature review of Chapter 2—which highlighted that the LC tank in the IPT receiver's oscillation power supply is undesirably clamped by the ESD protection diodes—this chapter introduces a targeted solution: by placing a pre-charged 12 V capacitor in series beneath the resonant tank, the entire oscillation waveform is offset from 0 V to 12 V, ensuring an ideal oscillation range of 0 V to 24 V without diode clamping. In parallel, we adopt the system context of an *imec* design that already provides 1.8 V, 5 V, and 12 V outputs; our contribution adapts this platform to also furnish a 24 V rail. Because the 1.8 V and 5 V rails are relatively straightforward to implement with existing *imec* IP, we assume those supplies to be present and do not focus on them during the design phase. The remainder of this chapter concentrates on the architecture of each module—explaining how the series capacitor resolves the clamping issue and optimizes energy transfer—and concludes with a summary that prepares for Chapter 4, where the detailed implementation, parameter selection, and component-level design are presented.

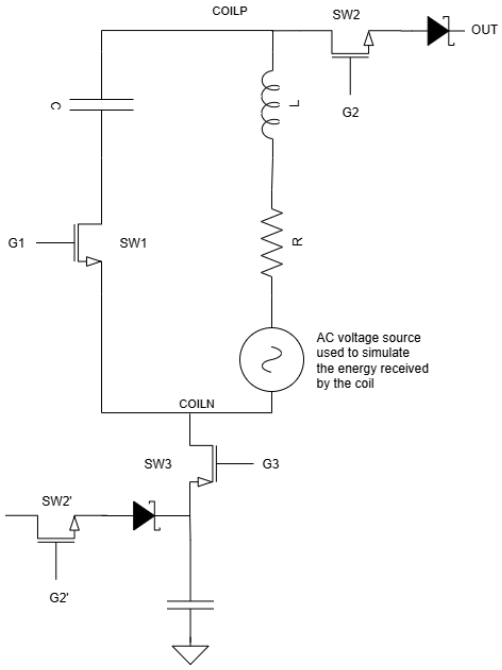


Figure 3.1: Proposed Circuit Topology

Figure 3.1 illustrates the complete lift-capacitor receiver architecture, in which the receiver-side inductor of the LC tank continuously harvests energy from the external IPT link and exchanges charge with the tank capacitor for oscillation and storage. The lift-capacitor offset network then biases this by 12 V, preventing ESD diode clamping and enabling a full 0 V to 24 V swing. The control and timing logic performs two critical roles: first, it directs the inductor between oscillation and output modes—connecting it to the tank capacitor for AC oscillation and energy accumulation, then disconnecting and routing it to discharge DC energy into the load for rectification—and second, it engages the lift capacitor only when a 24 V output is required, isolating it during 12 V operation. Finally, the rectifier and output stage deliver both a 12 V line, primarily used to recharge the lift capacitor, and a 24 V line, ensuring stable power delivery to downstream circuits.

3.1. INDUCTIVE RESONANT TANK MODULE AND ENERGY HARVESTING

3.1.1. SYSTEM-LEVEL REQUIREMENTS

The LC tank must reliably at 13.56 MHz with a peak amplitude of 12 V after few cycles. On the IPT receiver's side, the LC tank must minimize conduction and switching losses to maximize energy-transfer efficiency. To ensure stable and maximum energy transfer, the tank's quality factor—set by the fixed inductance L and its parasitic resistance R—and the tuning capacitor C are chosen for exact resonance at 13.56 MHz, while winding resis-

tance and MOSFET switching are optimized to minimize I^2R and C_{ds} losses each cycle.

3.1.2. SWITCH (SW1) REQUIREMENTS

In the capacitor branch of the LC tank, SW1 functions as a transmission gate: it closes during resonance to connect capacitor C in parallel with inductor L, and opens during discharge to let the inductor feed the load from the COILP node. The conventional parallel NMOS–PMOS transmission gate—where each transistor conducts on complementary levels to achieve full-rail switching—cannot be used here because its body diodes create an unintended L–C–body-diode loop from COILP back to COILN when switched off (see Figure 3.2), preventing the LC tank from fully stopping and degrading output efficiency.

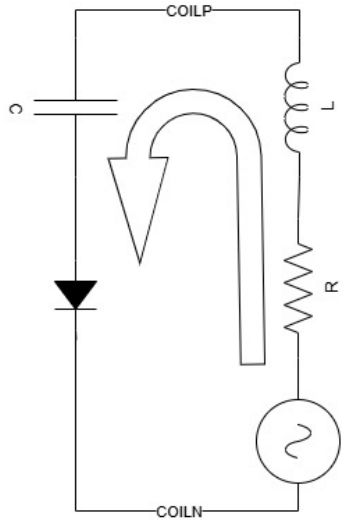


Figure 3.2: Reversed SW1 Configuration Causing an Unintended L–C–Body-Diode Loop

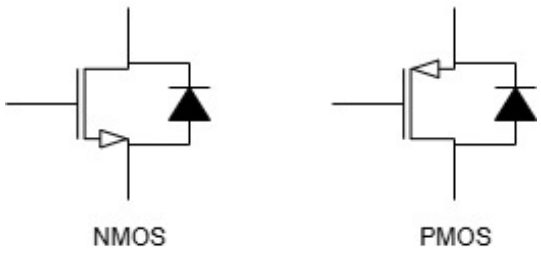


Figure 3.3: Body diode direction of nmos and pmos

To eliminate this reverse path, the chosen device's body diode must conduct only from COILN toward COILP. As shown in Figure 3.3, two single-device wiring options sat-

isfy this: an NMOS with its source tied to COILN (body diode from source/COILN to drain/COILP), or a PMOS with its drain tied to COILN (body diode also toward COILP). Since COILN is biased at approximately 12 V most of the time and precise V_{GS} control is essential for reliable shut-off, we select the NMOS with its source at COILN for SW1. This configuration prevents the unwanted L–C–body-diode loop and, because the majority carriers in NMOS are electrons whose mobility is higher than the hole mobility in PMOS for the same process, achieves a lower $R_{DS(on)}$ at a given overdrive and thus faster switching and reduced conduction loss at 13.56 MHz resonance.

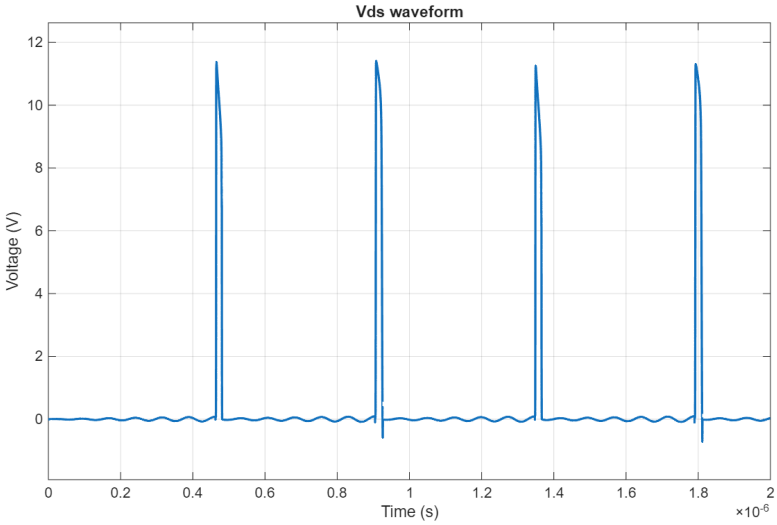


Figure 3.4: Waveform of V_{DS1} Showing Peak Voltage of Approximately 12 V

During discharge, SW1's source is clamped at COILN (12 V) while its drain follows COILP up to 24 V.As shown in Figure 3.4, this imposing roughly 12 V of V_{DS} stress. Consequently, we select a high-voltage NMOS rated for at least 12 V to provide adequate margin. With the lift capacitor connected beneath the LC tank, the source potential of SW1 is elevated by 12 V, so its gate-drive voltage V_{GS} must be controlled relative to this shifted source node. To fully turn on SW1, the gate voltage V_G must swing between 12 V (off) and approximately 17 V (on), corresponding to the 12 V to 17 V control window. Standard logic outputs, limited to 0 V to 5 V and unable to source the high peak currents required, cannot directly drive the large gate capacitance of such a device. Therefore, a dedicated high-side gate driver is employed to isolate the low-voltage control domain and deliver the necessary peak currents for robust SW1 switching.

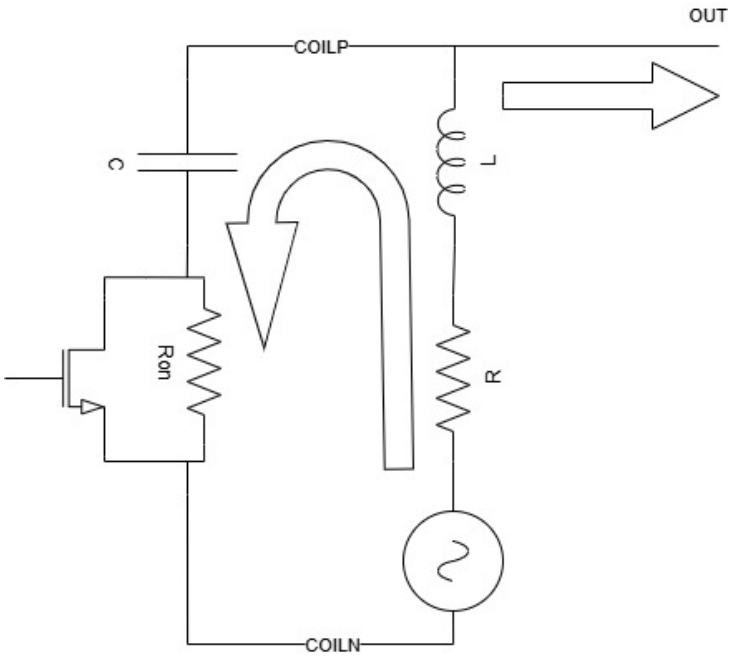


Figure 3.5: Slow-off SW1 Causing an Unintended COIL–Cap–SW1 Loop

Moreover, the combined dynamic response of the driver and SW1 must be considered. If SW1's gate-voltage fall time is too slow, three loss mechanisms arise: first, a "dual-path" condition occurs when the inductor L discharges to the output while C is still connected, causing part of the stored energy to flow back into the capacitor branch and reducing P_{out} as shown in Figure 3.5; second, during the fall interval of V_{GS1} signal, $R_{DS(\text{on})}$ does not rise instantly, so substantial current continues through SW1, incurring I^2R conduction losses; third, as V_{DS} transitions from near 0 V to 12 V over a prolonged interval, the MOSFET's parasitic output capacitance C_{ds} dissipates additional switching energy, approximately

$$E_{\text{sw}} \approx \tfrac{1}{2}\, C_{ds}\, (\Delta V_{DS})^2 = \tfrac{1}{2}\, C_{ds}\, (12\,\text{V})^2.$$

Therefore, SW1's turn-off speed critically affects system efficiency and must be limited to a few hundred picoseconds. In contrast, a slightly slower turn-on merely delays the next oscillation cycle and does not introduce comparable power loss.

3.1.3. RESONANT TANK COMPONENTS REQUIREMENT AND SETTINGS

The LC tank is composed of three elements: the fixed receiver-coil inductance L, the tuning capacitor C in parallel with L, and the coil's parasitic resistance R_p. Since the inductance value is fixed (selected from an off-the-shelf receiver coil) and the operating frequency must lie within the 13.56MHz ISM band, the capacitor C is chosen according to the relationship between L and f so that the circuit resonates precisely at 13.56 MHz.

The coil's quality factor is then defined by

$$Q = \frac{\omega L}{R_p},$$

where R_p is taken from the coil's datasheet and used in simulation to model insertion loss and bandwidth. Beyond ensuring the correct resonance frequency and Q value, there are no additional design constraints in this section—using the real R_p value in simulation is sufficient to guarantee stable oscillation at 13.56 MHz.

3.2. PRE-CHARGED OFFSET-CAPACITOR NETWORK

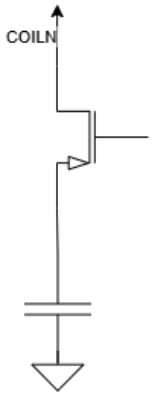


Figure 3.6: Lift-Capacitor Branch Schematic

Figure 3.6 shows that offset-capacitor branch consists of four elements: a ground reference, a charge-storage capacitor, a control switch (device selection discussed in the next section), and the COILN node of the LC tank. The capacitor provides a steady 12 V bias at COILN, shifting the resonant waveform to swing between 0 and 24 V and preventing bottom-rail clamping. The switch selectively connects or disconnects this bias depending on the operating mode, enabling seamless transition between the 12 V and 24 V output levels.

3.2.1. S3 SWITCH AND DRIVER REQUIREMENTS

The pull-up switch must elevate COILN to the charged capacitor potential during resonance, so we choose a PMOS device. PMOS transistors excel as high-side pull-up switches: with their source tied to the stable 12 V capacitor node, pulling the gate low toward 7 V fully enhances the channel,efficiently applying the bias to COILN.

Since the PMOS source is fixed at 12 V, its gate must toggle between 7 V (on) and 12 V (off) for precise control of switch S3. Standard logic outputs (0–5V) cannot span this range, nor can they source the peak currents needed to charge the PMOS gate capacitance quickly. Therefore, a dedicated high-side driver is required to isolate the low-voltage control domain and provide the necessary drive strength.

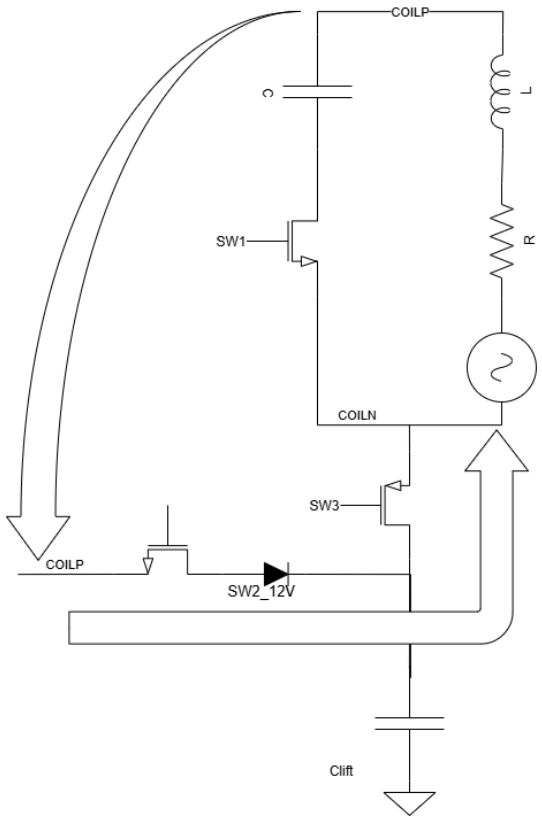


Figure 3.7: Slow-off S3 Causing an Unintended COIL–S3 Loop

During resonance and 24 V output modes, S3 remains closed to maintain the 12 V bias at COILN; in the 12 V output (or lower) mode, S3 must open rapidly. For example, if S3 fails to turn off promptly at 12 V output, as shown in Figure 3.7, an unintended loop (COILP $\rightarrow$ S3 $\rightarrow$ COILN) forms, short-circuiting the inductor's discharge current that should charge the lift capacitor and severely degrading efficiency. Hence, S3's turn-off speed is critical and should be minimized to the few-hundred-picosecond range. In contrast, a slightly slower turn-on merely delays the biasing transition without significant power loss and can be traded off for faster turn-off when necessary.

3.2.2. LIFT-CAPACITOR SELECTION

The lift capacitor must hold the 12 V bias with minimal voltage droop during discharge. As COILP discharges, a small leakage path through ground, the capacitor, and the output causes charge loss that can destabilize COILN. To mitigate this, a large capacitance is chosen so that any charge loss ΔQ results in a negligible voltage change, according to

$$\Delta V = \frac{\Delta Q}{C}.$$

From the on-chip perspective, capacitance density limits make it impractical to in-

tegrate values larger than a few hundred picofarads. Even at the upper bound ($C_{max} \approx 500\,pF$), the corresponding voltage variation during a single discharge cycle would exceed the 100 mV tolerance, as confirmed by simulation (Figure 3.8). This makes an entirely on-chip solution unsuitable for maintaining a stable 12 V bias.

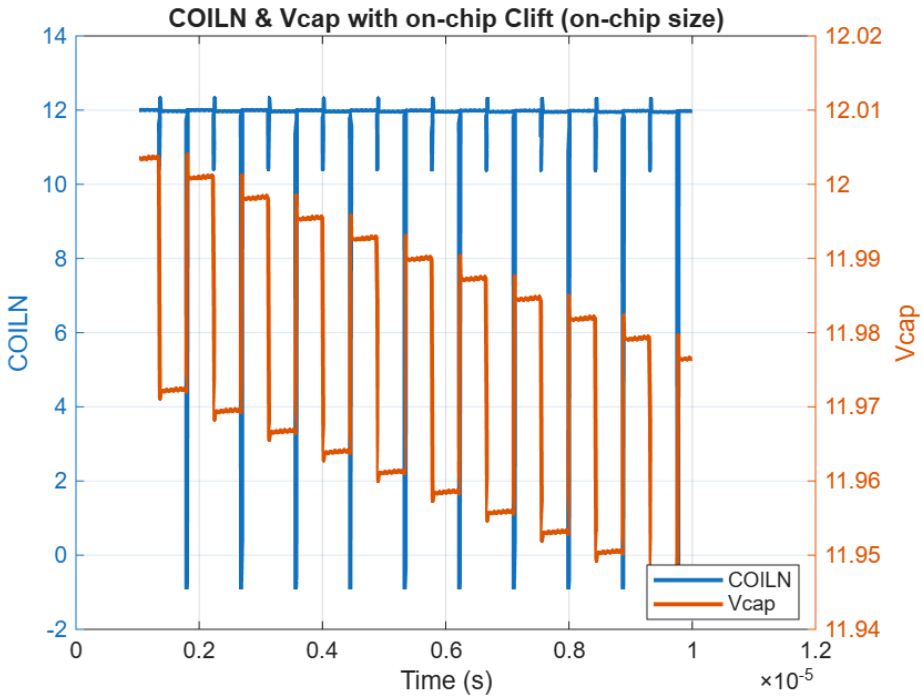


Figure 3.8: Waveform of the voltage on the capacitor and COILN with $C_{lift} = 500\,pF$.

Conversely, placing the lift capacitor off-chip removes the silicon area constraint, allowing the use of high-value capacitors that keep ΔV well below the stability limit. Since the capacitor is external, it does not impact the integrated receiver's form factor, enabling robust bias retention without compromising chip area. Two practical drawbacks remain: the external capacitor stores nontrivial energy, and an additional bond pad/package pin is required. Even so, we adopt the off-chip implementation in this work after weighing these trade-offs, as it provides a pragmatic path to the required performance and form factor while keeping integration options open for future revisions.

3.3. MODE-SWITCHING CONTROL & TIMING LOGIC

3.3.1. SW1 CONTROL LOGIC: LC TANK OSCILLATION GATING

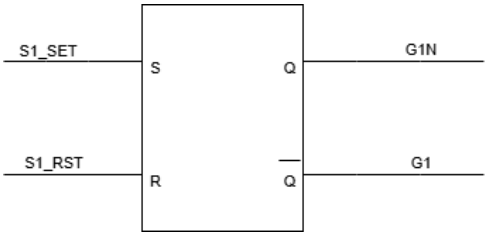


Figure 3.9: SR Latch-Based SW1 Control Logic

SW1 controls whether the LC tank is in resonance or discharge, implemented by an SR latch with set and reset inputs (Q→G1N, $\overline{Q}$→G1).A high set input breaks the switch to halt oscillation; a high reset input closes the switch to resume resonance. This dual-input latch cleanly toggles between resonance and charging modes.

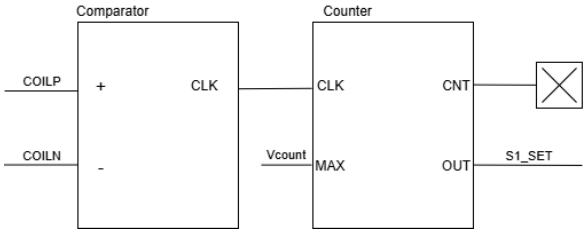


Figure 3.10: Cycle-Counting Based LC Tank Oscillation Termination Scheme

To realize this strategy, we first generate an appropriate `set` signal. The objective of `set` is to halt oscillation promptly once the LC tank reaches a prescribed amplitude, thereby entering the inductor–discharge phase. Prior work [7]—via system modeling and experimental optimization—indicates that there is an optimal number of oscillation cycles, maximizing energy accumulation while minimizing circuit losses. Accordingly, a common approach places comparators across the tank nodes (COILN and COILP) to detect oscillation polarity and produce a period-synchronous clock; a counter then accumulates the cycle count and, upon reaching the preset N, asserts `set` to open the switch.

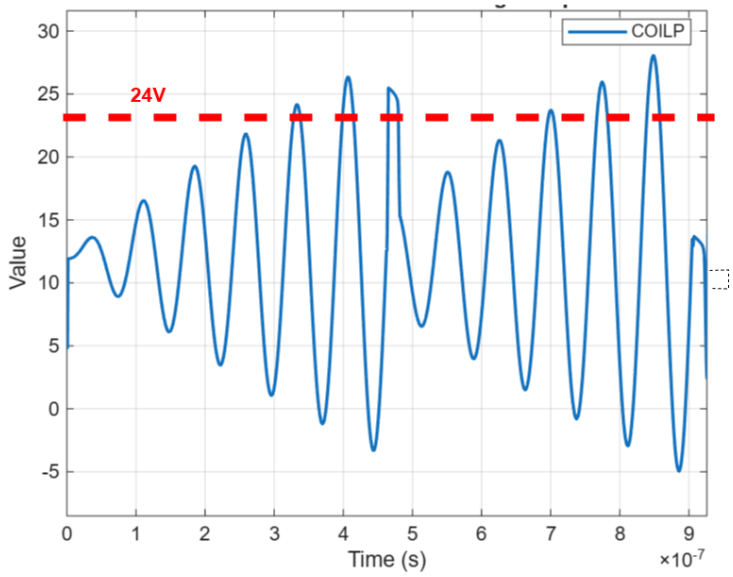


Figure 3.11: COILP waveform with fixed resonance cycle N

However, this fixed-cycle strategy has notable shortcomings. In wireless power transfer, the received power varies with the environment and coupling conditions. A fixed N can cause the tank to accumulate excess energy in certain cycles (Figure 3.11), pushing the amplitude beyond the target (e.g., a 12 V amplitude corresponding to a 0–24 V swing). The surplus is then dissipated during a *dwell* interval—additional oscillation of COILP after the target amplitude is reached and before the next switching action—through the tank's inherent damping and device conduction.

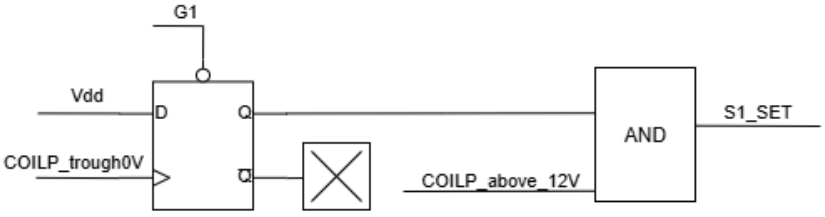


Figure 3.12: Amplitude-Triggered LC Tank Termination Scheme

To address this, we adopt an adaptive termination mechanism. During oscillation, a comparator monitors whether the minimum of COILN reaches 0 V (with a 12 V bias, reaching 0 V implies a 12 V amplitude). Once this condition is met—signaling that the energy target has been achieved—we wait until COILP enters its positive half-cycle, i.e., the moment just before discharging to the output, and then assert `set` to interrupt oscillation. This control scheme both guarantees sufficient energy accumulation and avoids

losses from maintaining an unnecessarily high amplitude, enabling a more dynamic, energy-aware switching strategy.

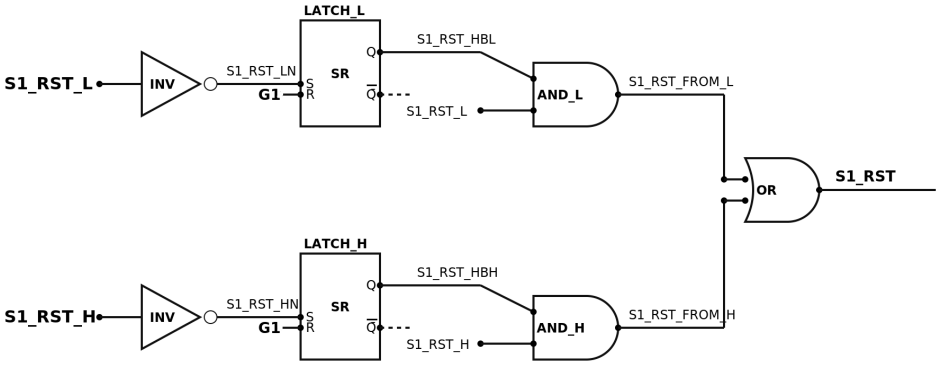


Figure 3.13: Reset logic for G1 signal

The reset signal is produced by a second comparator monitoring COILP; once COILP falls below the target output voltage (12 V or 24 V), reset signal `S1_RST_L` or `S1_RST_H` is asserted, closing SW1 and beginning the next resonance period.In Figure 3.13, signal `S1_RST_HBL` and `S1_RST_HBH` are provided to ensure that the detected event is `COILP` falling below 12 V or 24 V during discharge, rather than `S1_RST_L`/`S1_RST_H` triggered by the voltage drop across the oscillator elements.

3.3.2. SW3 CONTROL LOGIC: OUTPUT-LEVEL SEQUENCING

SW3 selects whether the lift capacitor is connected to the LC tank (S3 closed) or isolated (S3 open), thereby alternating the output level between 24 V and 12 V. In this design, G3 is driven by the count of the G1 signal cycles: each time SW1 completes one resonance–discharge cycle we derive a short trigger pulse from a single chosen edge of the G1 signal (edge detector + pulse shaper) and use that pulse to update G3. Two realizations are practical.

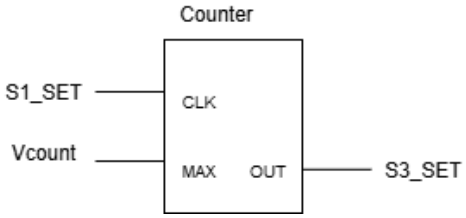


Figure 3.14: Using Counter to set G3 (G3 is turned on once every Vcount resonance-output cycles)

A programmable counter can count these pulses and change G3 at preset counts, enabling arbitrary ratios and sequences between 24 V and 12 V intervals.

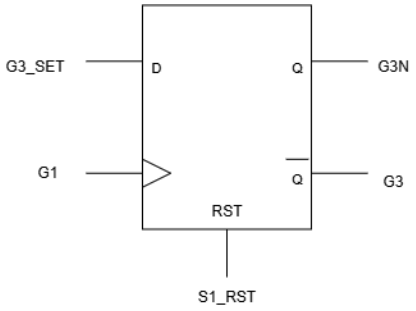


Figure 3.15: Final stage to set and reset G3 by D-flip-flop

Alternatively, G3 signal reset is determined by S1_RST as well: a comparator monitors COILP, and when the 12 V discharge is complete (COILP falls below 12 V) it asserts reset to force G3 into the "S3 closed" state, preparing the next 24 V cycle and keeping the sequence phase-aligned.

3.3.3. SW2 Control Logic: 24 V Path Enable

SW2 is the NMOS that connects COILP to the 24 V output. Its gate is driven by a simple AND of the mode and phase signals:

$$G2 = \overline{G1} \wedge G3,$$

so SW2 turns on only when the tank is in the discharge phase ($\overline{G1} = 1$) and the lift capacitor is engaged ($G3 = 1$). Otherwise SW2 remains off.

3.4. Dual-Voltage Rectifier & Output Stage

As shown in Figure 3.16, the output stage comprises two complementary discharge paths—one delivering 24 V and the other 12 V—which are activated in an alternating fashion across successive operation cycles. As outlined in the previous section on control logic, the system alternates between two main modes: an LC tank resonance phase for energy accumulation, followed by a discharge phase to the load. The discharge phase itself alternates between the 24 V branch and the 12 V branch on successive cycles, effectively switching between the two output levels. Each path is implemented with its own MOSFET switch, and these two devices form the core of the output stage.

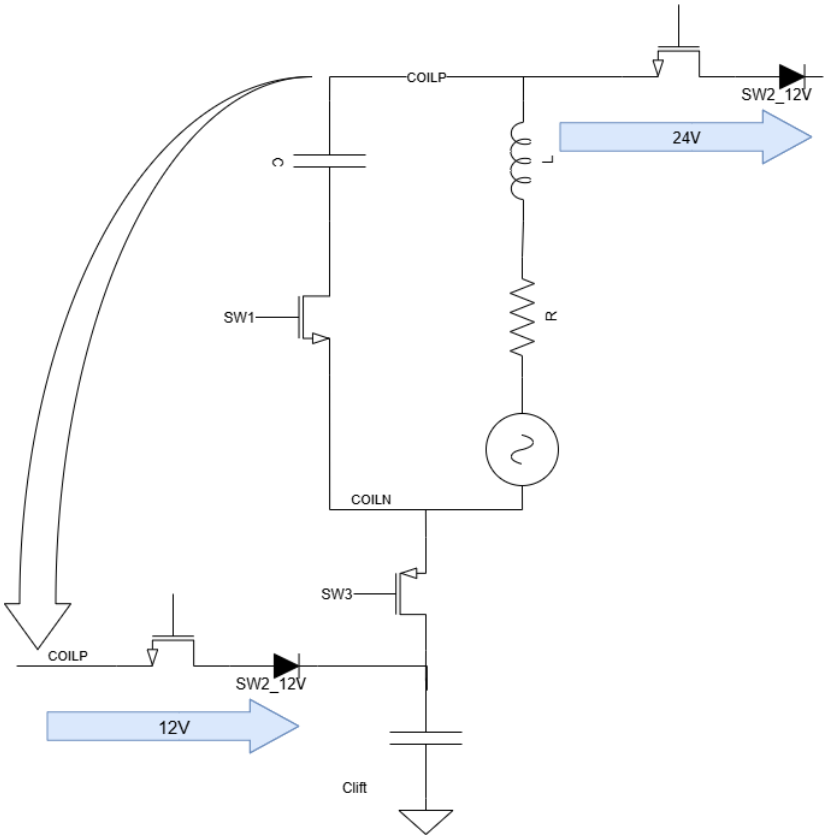


Figure 3.16: Main Schematic Highlighting 12 V and 24 V Output Paths

3.4.1. S2 SWITCH AND DRIVER REQUIREMENTS

To prevent unintended conduction between COILP and the 12/24 V outputs during resonance and discharge, we insert an anti-series diode pair in the COILP–OUT path. As shown in Fig. 3.11, COILP swings above and below the output levels; with only a single diode, there will be instants during the oscillation when it forward-biases and conducts. The anti-series pair ensures that at any given moment one diode is reverse-biased, keeping the path open for both polarities. Two candidate topologies are shown in Figure 3.17:

Figure 3.17: Two Diode Connection Topologies for Output Isolation

(a) Two series diodes with cathodes facing each other

(b) Two series diodes with anodes facing each othe

Topology (b) is preferred because fixing the central node at ground potential allows the right-hand diode (ground → anode–cathode → OUT) to be an ordinary low-voltage device in low-output applications (e.g., 5 V or 3.3 V)—a pattern that can be replicated when multiple low-output rails are desired—whereas topology (a) would forward-bias one diode whenever COILP exceeds ground.

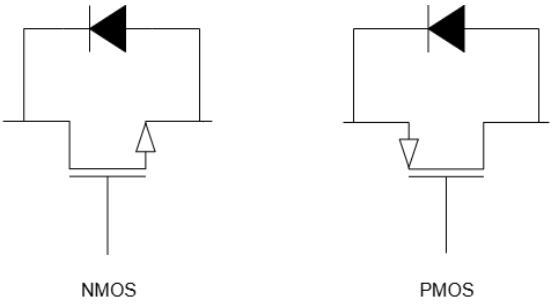


Figure 3.18: Body Diode Orientations of NMOS and PMOS Devices

Having chosen topology (b), the output side uses a standard diode to conduct when COILP exceeds OUT during charging mode. For the input side switch, both PMOS and NMOS options can meet the required body-diode orientation (as illustrated in Figure 3.18), but we opt for an NMOS. Its source is tied to the stable midpoint, ensuring reliable blocking when off and proper conduction when on.

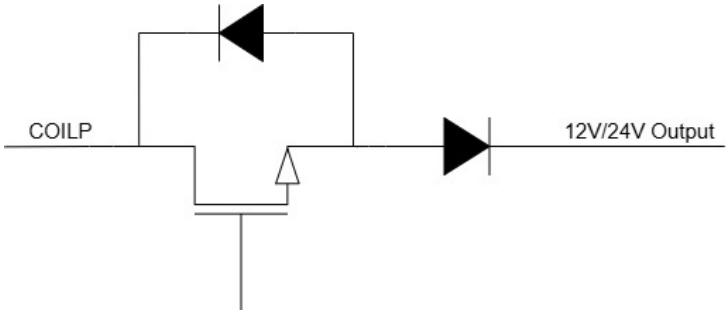


Figure 3.19: Final Output Path Topology

Thus, the final output path (Figure 3.19) consists of an NMOS in series with a diode, ensuring reliable isolation of COILP from the output during resonance and preventing any unintended conduction—and thereby energy leakage—while still supporting both 12V and 24V discharge modes.

4

IMPLEMENTATION

This chapter concentrates on the implementation of main LC tank(including SW1 driver) and Lift Capacitor path (including SW3 driver) and their simulation result. For the control logic, simulation work centers on the comparator functionality that governs mode transitions; due to schedule constraints, a custom comparator has not yet been completed, and the simulations therefore employ ideal comparators and ideal Verilog-A logic circuit. For the output (discharge) path, the implementation effort focuses on the SW2 gate driver; because a functionally equivalent high-voltage driver/IP is available at imec, that solution is adopted without further redesign in this work. The chapter closes with a system-level power-consumption assessment derived from circuit-level simulations

4.1. LC TANK IMPLEMENTATION

4.1.1. PASSIVE COMPONENT SELECTION IN THE LC TANK

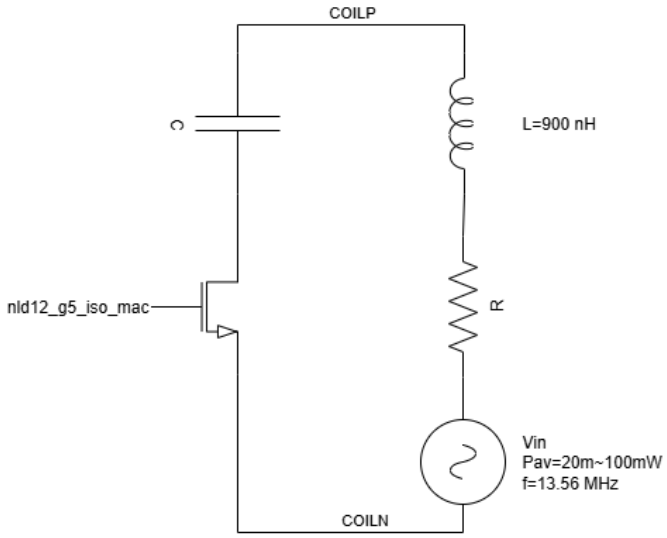


Figure 4.1: LC tank Schematic in simulation

Figure 4.1 shows the LC-tank schematic used in the simulations, with application-set component values annotated.

The LC tank in our design uses an inductor of $L = 900\,\text{nH}$, selected based on the target operating frequency of 13.56 MHz for inductive power transfer. Given the desired resonant frequency f_0, the required capacitance is

$$C = \frac{1}{(2\pi f_0)^2 L},$$

which yields $C \approx 154\,\text{pF}$ for our parameters. In simulation, the effective capacitance is adjusted downward by 3 pF–5 pF to account for the parasitic capacitance introduced by the series lift capacitor and SW3.

The inductor's quality factor Q is specified as 60, from which the *series* parasitic resistance can be obtained as

$$R_s = \frac{\omega L}{Q},$$

where $\omega = 2\pi f_0$. Substituting our values gives $R_s \approx 1.28\,\Omega$. This series resistance is included in simulations to represent copper losses and other winding-related dissipation within the coil.

For the input excitation in simulation, an AC voltage source is used to emulate the energy received via inductive coupling from the transmitter; this approximation is appropriate only for low coupling factors (low-k). The frequency of this source is fixed at

13.56 MHz, and its amplitude is varied between 20 mV and 100 mV to model different coupling strengths.

The main switching device S_1 is implemented using the `NLD12_G5_ISO_MAC` NMOS transistor. The "ISO" designation indicates the presence of an isolation ring in the layout, which improves noise immunity and reduces substrate coupling—beneficial in mixed-signal environments. This device was chosen for its adequate voltage rating ($\geq$ 12 V V_{DS}), low $R_{\mathrm{DS(on)}}$ to minimize conduction loss, and moderate gate charge, enabling fast switching transitions at the target frequency. A 24 V output can be realized with 12 V-rated devices because a 12 V bootstrap is applied at the source, producing a lift at both terminals, so the device stresses V_{DS} and V_{GS} remain within the 12 V rating, avoiding over-voltage breakdown.

4.1.2. HIGH-SIDE GATE DRIVER DESIGN FOR S1

SW1 requires a 12 V–17 V gate drive in the LC-tank path; since standard logic is only 0 V–5 V, a boosted, high-speed driver is required. The proposed SW1 driver consists of three key components: a bootstrap structure for voltage boosting; a chain of cascaded inverters with progressively increased transistor sizes to enhance the driving capability; and a capacitive level shifter, which translates the logic signal into the boosted voltage domain. These three parts operate together to achieve stable and efficient driving of SW1. In the following sections, the design principles and implementation details of each component will be discussed, followed by the encountered implementation issues and corresponding simulation results.

BOOTSTRAP

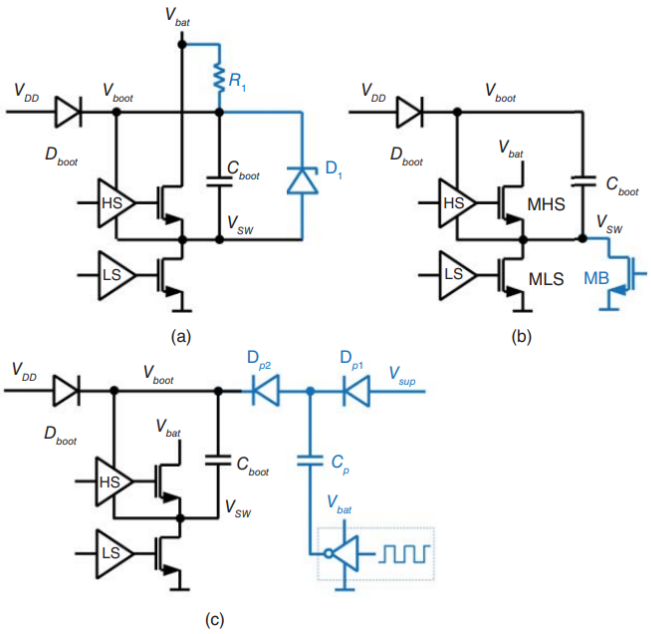


Figure 4.2: Bootstrap supply with a) recharge path from Vbat, b) pull-down transistor MB, and c) charge pump to recharge Cboot [24]

The bootstrap circuit is a common technique for high-side gate driving, enabling sufficient overdrive for n-type transistors [24]. Figure 4.2 shows some common examples for the bootstrap structure. In this design, SW1 is an nMOS with its source fixed at about 12 V, so the gate must exceed this level by the required overdrive to ensure conduction. The bootstrap uses a diode and capacitor: when the low-side switch is on, the capacitor charges from V_{drv}; when the high-side turns on, the diode is reverse-biased and the stored charge provides about 12 V+V_{DD}, ensuring proper drive for SW1.

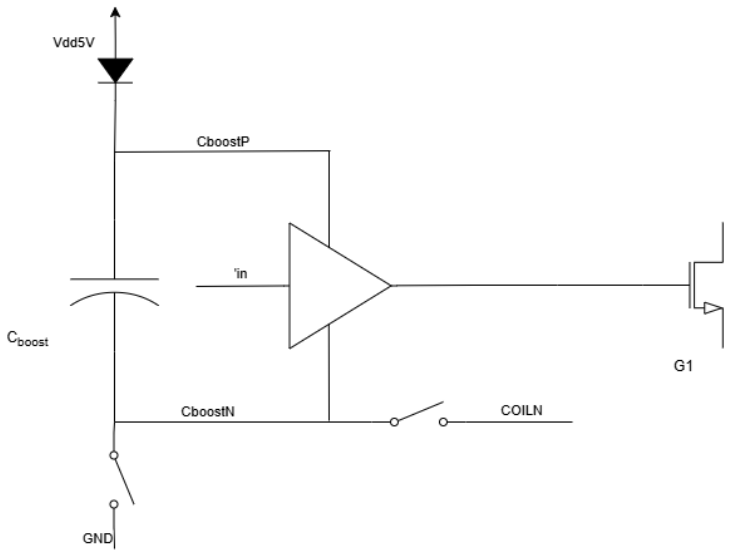


Figure 4.3: Bootstrap schematic in this design

As shown in Figure 4.3, the bootstrap circuit consists of a diode and a capacitor. The diode provides unidirectional conduction: during the charging phase, it allows the capacitor to be charged from V_{DD}, while in the operation phase it prevents the boosted driver V_{DD} node from back-feeding the elevated voltage (e.g., 17 V) into the actual 5 V V_{DD} supply. The capacitor ensures that, once charged, the voltage difference between the driver's V_{DD} and V_{SS} remains approximately 5 V. During the charging phase, CboostN is switched to ground, and the capacitor charges through the diode from V_{DD}, establishing a voltage difference of about 5 V between CboostP and CboostN. In the operation phase, CboostN is reconnected to coil_n (at 12 V), and the maintained voltage difference lifts CboostP to approximately 17 V, thereby providing the driver with the required boosted supply to reliably drive the gate of SW1.

CASCADED INVERTER DRIVER

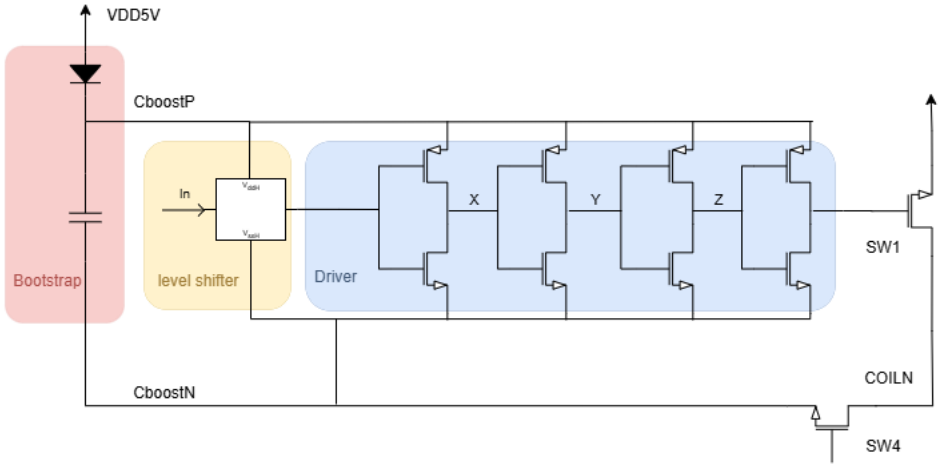


Figure 4.4: Cascade Inverter schematic

Cascaded inverter drivers are widely used to improve drive strength and reduce delay for large capacitive loads, outperforming a single oversized inverter [24]. Starting from a minimum-size stage, successive stages are scaled by a fixed factor α, making the input/output capacitances roughly proportional and keeping the per-stage delay nearly equal; jointly optimizing α and the number of stages n minimizes total delay. Analysis and simulations show that geometric scaling achieves a favorable speed–power trade-off, with 4–6 stages in common practice [24].

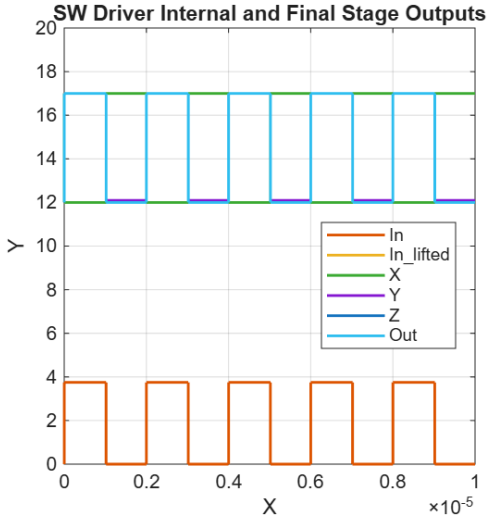


Figure 4.5: Cascade inverter input and output at each level and final output

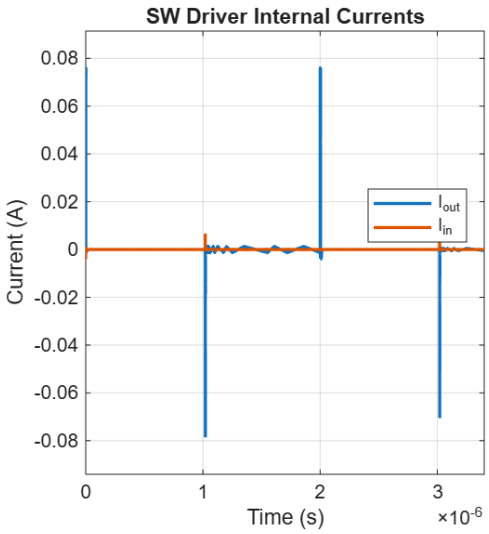


Figure 4.6: Cascade Inverter Input current and Output Current

In this design, the cascaded inverter driver uses $V_{DD} = 17\,V$ from the bootstrap (CboostP) and $V_{SS} = 12\,V$ at coil_n; hence its input must lie within 12 V–17 V and is provided by the level shifter. A four-stage, geometrically sized chain is adopted so the overall transfer is non-inverting while delivering higher drive current to SW1. As shown in Figure 4.5, the control waveform propagates through nodes $X \rightarrow Y \rightarrow Z$ across successive inverters: each stage inverts the signal and, with increasing device widths, the gate drive current grows (Figure 4.6); the cost is added delay that slightly distorts the control edges. This configuration preserves level compatibility and enables fast, reliable switching of SW1.

LEVEL SHIFTER

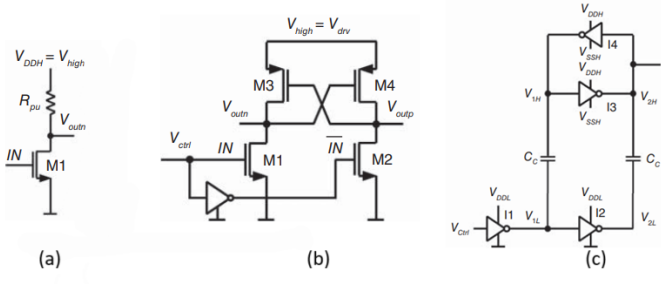


Figure 4.7: Common level shifter (a) resistor-based; (b) cross-coupled; (c) capacitive level shifter [24]

Level shifters bridge low-voltage logic and high-voltage drivers; common topologies are resistor-based, cross-coupled, and capacitive [24]. Resistor types are simple and provide a default state but suffer RC-limited speed and static loss. Cross-coupled types achieve rail-to-rail outputs with regenerative switching and ideally zero static current; however, when the high-voltage domain is far above the logic domain they require protection (thick-oxide devices or stacked transistors, gate/source clamps, source followers). These protections (i) increase C_{gs}/C_{gd} and reduce effective overdrive in stacked devices, slowing regeneration and lengthening crowbar intervals; (ii) to regain speed, devices must be upsized, which raises dynamic power $P_{dyn} \approx C_{eff} V_H^2 f$; and (iii) clamp/bias networks introduce extra switching charge and leakage, so the "zero static current" advantage erodes. Consequently, the attainable speed and low-power operation of cross-coupled shifters degrade as the voltage difference grows. For this design, we therefore choose a capacitive topology: edges are translated via coupling capacitors into a latch, yielding fast transitions and near-zero static current with smaller effective switched capacitance at the high-voltage node—while we accept its greater sensitivity to noise and sizing—whereas resistor solutions remain too lossy/slow.

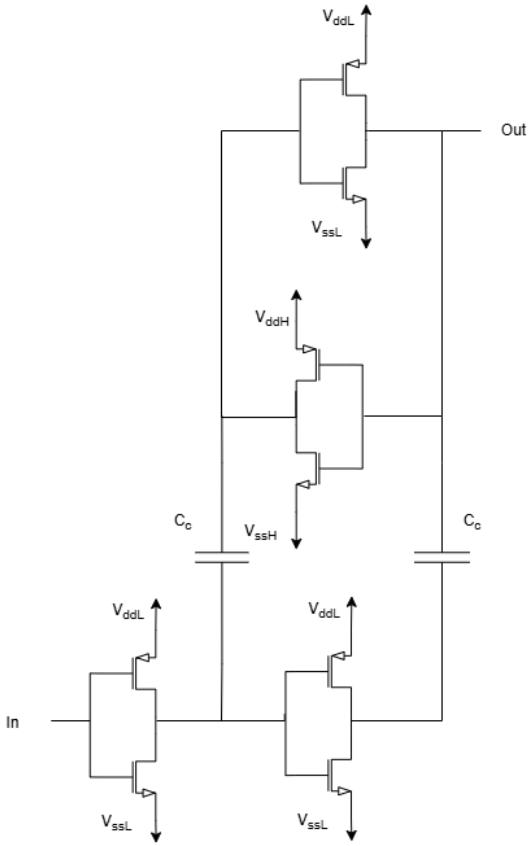


Figure 4.8: Capacitive Level Shifter Schematic

In this design (Figure 4.8) , a two-stage low-voltage inverter produces complementary edges that are AC-coupled through capacitors to the two inputs of a high-voltage cross-coupled latch (structure similar to the left half of Fig. 5.37). During each transition, one capacitor delivers a positive pulse that drives its latch input beyond the switching threshold, while the other delivers a negative pulse that pulls the opposite input away from threshold. The latch's regenerative feedback then resolves to the new state and holds it on the 17 V/12 V rails, thereby translating the 0 V–5 V input without any DC path between the low- and high-voltage domains. The simulated input and output waveforms illustrating this operation are shown in Figure 4.9.

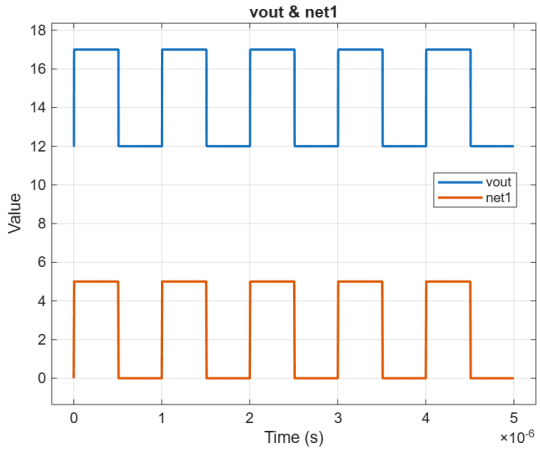


Figure 4.9: Input (net1) and output (vout) waveform of level shifter

PARAMETER DESIGN, MODIFICATIONS, AND SIMULATION

In the previous sections, the principles of the bootstrap supply, cascaded inverter driver, and capacitive level shifter were introduced. However, during circuit implementation and simulation, several issues were observed that prevented the original design from meeting the desired performance. To address these challenges, structural modifications and parameter adjustments were applied. This section discusses the encountered problems, the corresponding improvements, and the parameter choices validated through simulation.

Cascaded Inverter Driver Modification In the initial design, the four-stage cascaded inverter driver was supplied with V_{DD} and V_{SS} taken directly from the C_{boostP} and C_{boostN} nodes of the bootstrap circuit. Simulation result shown in Figure 4.10 revealed that this configuration led to waveform irregularities, with the driver output showing a plateau during rising transitions leading to a longer fall time/ rise time. According to the simulation results shown in Figure 4.10, this behavior was attributed to charge injection: when the NMOS devices switched off, channel charge was injected into the floating V_{SS} node, disturbing its potential and causing the output to stall.

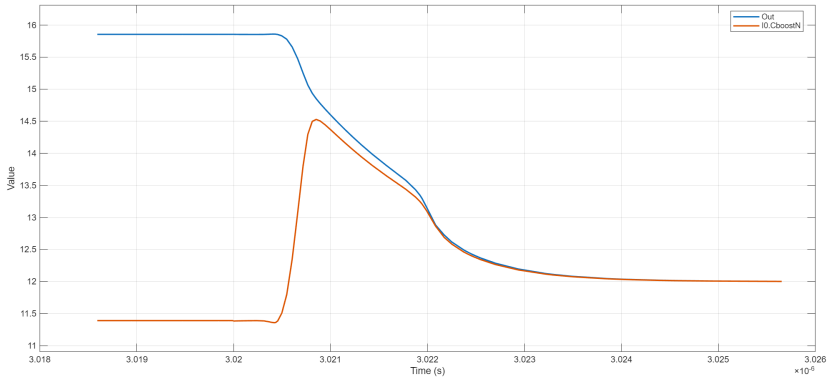


Figure 4.10: Plateau on V_{OUT} (blue) during the rising edge—caused by charge injection into the floating V_{SS} via C_{boostN} (orange).

To mitigate this issue, the driver's V_{SS} was tied to the COILN node instead of C_{boostN} node, as shown in Fig. 4.11. This node is stabilized by a large lift capacitor ($C_{lift} \approx 1\,\mu F$) (as discussed in 3.2.2. LIFT-CAPACITOR SELECTION), so its potential remains nearly constant during switching, suppressing the platform in the fall time we observed in Figure 4.10. In addition, the bootstrap gating is *self-timed* using a signal derived from the cascaded inverter output, so no extra externally timed control is required. We simply reuse the driver gate signal and define

$$G_4 = \overline{G_1}$$

(i) When the system is in charging mode (12-V output): COILN $\approx 0\,V$, SW1 is open, $G_1 = 0 \Rightarrow G_4 = \overline{G_1} = 1$; the G_4-controlled switch closes, tying C_{boostN} to COILN$\approx 0\,V$, and the bootstrap capacitor C_{boot} is charged via the $5\,V$ V_{dd} through a diode.

(ii) When the system is in resonance mode or in charging mode (24-V output): COILN $\approx 12\,V$; irrespective of whether G_4 is on or off, C_{boostN} remains near $12\,V$, C_{boot} provides the bootstrap lift for the high-side drive.

This modification yields two practical benefits: (i) referencing the cascaded inverter to the more stable COILN reduces charge-injection effects and removes the output plateau; and (ii) reusing existing driver signals to generate G_4 avoids additional bootstrap-control signals and timing.

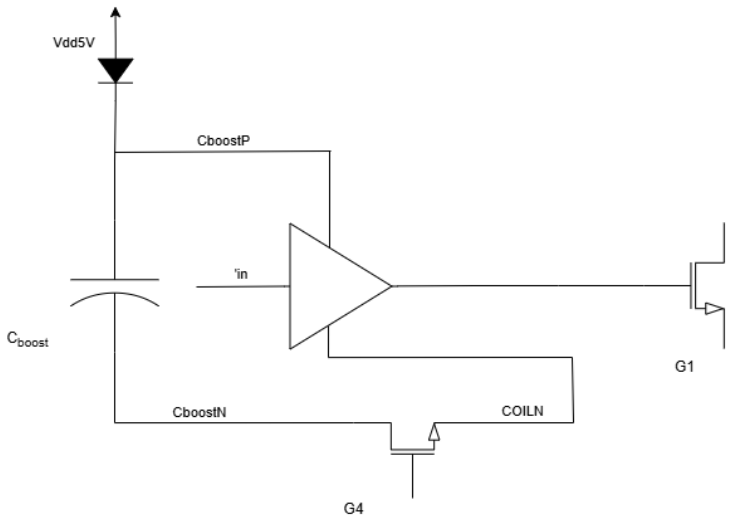


Figure 4.11: Driver V_{SS} tied to COILN and self-timed bootstrap gating: $G_4 = \overline{G1}$ controls the connection of C_{boostN} to COILN.

Discharge Path Compensation With the modified connection, simulations further revealed an undesirable *AC* discharge mechanism during the main circuit's off-state:

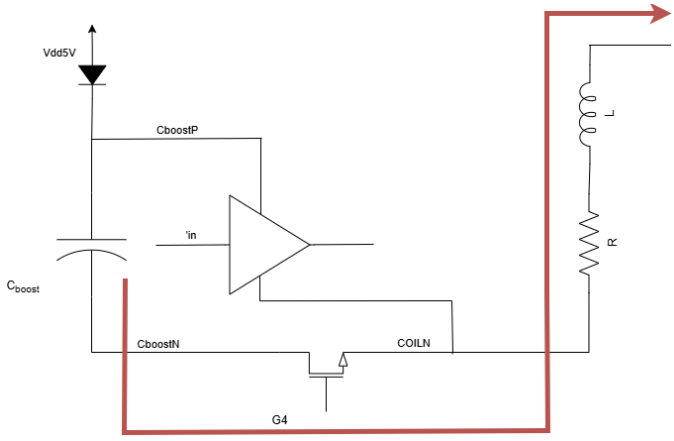


Figure 4.12: Undesired off-state discharge path.

$$C_{\text{boostN}} \longrightarrow SW4 \longrightarrow \texttt{COILN} \longrightarrow L \longrightarrow \texttt{output}.$$

Although the capacitor blocks DC discharge current of inductor, when the switch opens the inductor current cannot change instantaneously and therefore excites a strong flyback/ringing *AC pulse*. This pulse drives an alternating displacement current through

the $C_{\text{boostN}} \rightarrow G4 \rightarrow$ `coil_n` loop, siphoning charge from the bootstrap capacitor and lowering its stored voltage. As a result, the nominal 12–17 V driver supply becomes destabilized. To counter this, a diode was added between ground and C_{boostN}. During the discharge phase, this diode provides an alternative path:

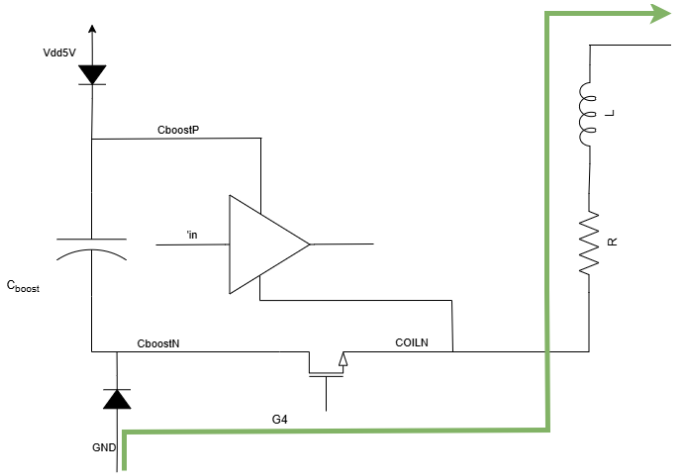


Figure 4.13: Mitigation with ground–C_{boost} diode.

$$ground \longrightarrow diode \longrightarrow C_{\text{boostN}} \longrightarrow SW4 \longrightarrow coil\_n \longrightarrow L \longrightarrow output,$$

which compensates for charge loss and helps maintain the bootstrap voltage. Simulation confirmed that this modification improved output stability and preserved the intended drive levels.

C_{boost} Capacitor Selection The bootstrap capacitor C_{boost} must sustain the gate drive; if too small, charge sharing with the MOSFET input causes voltage droop, approximated by $\Delta V_{\text{bs}} \approx (C_{\text{iss}}/C_{\text{boost}})\, V_{\text{bs}}$. Parametric simulations (Figure 4.14) show that for C_{boost} <50 pF, the output cannot stay within 12 V–17 V, whereas larger values keep the bootstrap voltage stable. We therefore select ~50 pF as the minimum C_{boost}.

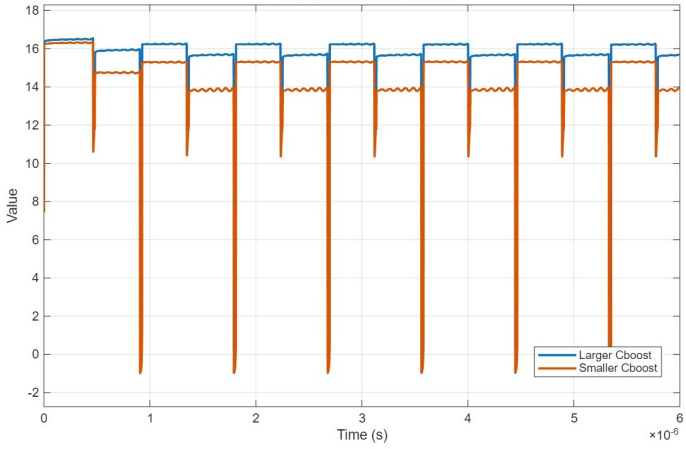


Figure 4.14: Simulated driver output voltage versus time for two bootstrap-capacitor values: $C_{\text{boost}} = 50\,\text{pF}$ and $C_{\text{boost}} = 20\,\text{pF}$.

Level Shifter: Mechanisms and Design Guidelines As shown in Figure 4.8, this work employs a capacitive level shifter. Correct operation fundamentally depends on the matching of three elements: (i) the low-side inverter sizing, which sets the transient drive capability and edge rate; (ii) the coupling-capacitor value, which determines the injected amplitude; and (iii) the high-side latch sizing, which sets the effective input capacitance and the difficulty of crossing the switching threshold.

(1) Low-side sizing and edge/injection capability. During an input transition, the low-side final stage injects transient charge into the coupling capacitor C_c. The drive current can be approximated by

$$I_{\text{LV}} \simeq \tfrac{1}{2}\,\beta_{\text{low}}\,(V_{\text{DD,LV}} - V_{th})^2, \qquad \beta_{\text{low}} = \mu C_{\text{ox}}\frac{W_{\text{low}}}{L_{\text{low}}},$$

leading to an edge rate

$$\frac{\mathrm{d}v_{\text{LV}}}{\mathrm{d}t} \approx \frac{I_{\text{LV}}}{C_{\text{node}}},$$

and a peak injected current

$$i_{\text{inj,peak}} \approx C_c\,\frac{I_{\text{LV}}}{C_{\text{node}}}.$$

Thus, increasing $W_{\text{low}}/L_{\text{low}}$ boosts β_{low} and I_{LV}, steepens the edge, and strengthens injection, but also increases gate/interconnect capacitance C_{node} and dynamic power $P_{\text{dyn}} \approx f\,C_{\text{tot}}\,V^2$.

(2) Coupling capacitor and cross-domain partition. The voltage pulse coupled to the high-side node is well captured by the capacitive-divider approximation

$$\Delta V_{\text{HV}} \approx \frac{C_c}{C_c + C_{\text{in,HV}}}\,\Delta V_{\text{LV}},$$

where ΔV_{LV} is the low-side transition amplitude. Larger C_c (or smaller $C_{in,HV}$) increases the coupled pulse, while an excessive C_c raises switching energy, coupling noise, and area.

(3) High-side latch sizing and effective input capacitance. Larger device sizes in the high-side inverters make the latch input "heavier": the effective input capacitance grows with total gate width, so more transient charge is required to push the NMOS/PMOS gates across the switching threshold. A balanced sizing keeps the latch hold capability while allowing reliable triggering from the coupled low-side pulses.

(4) Overall trade-off and optimization. Subject to the requirement that the coupled high-side pulse crosses the latch threshold, we enumerate feasible combinations of (i) the sizing of the final low-voltage stage INV_{L1} and INV_{L2}, (ii) the coupling capacitors C_X and C_Y, and (iii) the sizing of the high-voltage latch inverters INV_{H_A} and INV_{H_B}. From these combinations, we select the one that minimizes dynamic power P_{dyn} while achieving the fastest response (smallest t_p).

W_{low}	W_{high}	C_c
8μm	900nm	40fF

Table 4.1: Optimized parameter combination of the level shifter

Rise time	Fall time	Delay
900ps–1.2ns	700ps–1ns	500ps–800ps

Table 4.2: Performance of the SW1 driver under optimized level shifter parameters

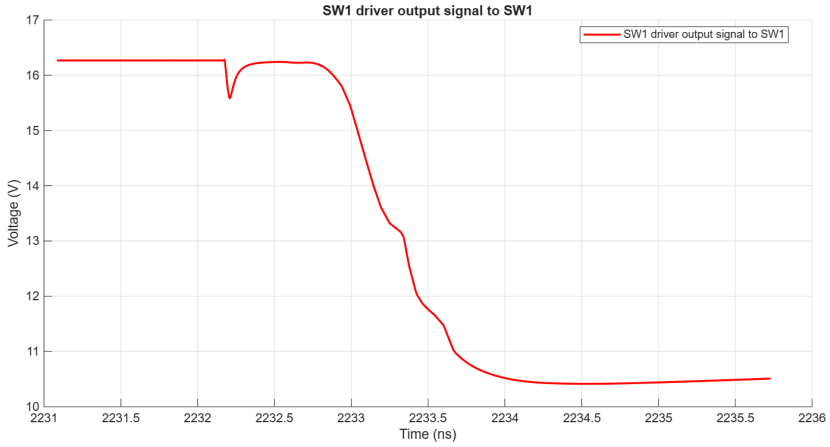


Figure 4.15: Final output signal (fall period) of SW1 driver combined with level shifter

Cascaded Inverter Sizing After fixing the finalized connectivity, supply rails, and component values, we swept the sizing of the four-stage cascaded driver (INV_{D1}–INV_{D4}),

which is supplied by $V_{DDH} = 17\,V$ (CboostP) and $V_{SSH} = 12\,V$ (coil_n), takes its input from the level shifter, and drives the SW1 gate. The sweep varies stage widths (with geometric scaling across stages) and compares the resulting response time at the SW1 gate and the associated dynamic power, targeting the fastest edges at the lowest power while keeping the load seen by the level shifter acceptable. Figure 4.16 plots the driver output waveforms for the different sizing options. During the 12-V recharge mode, `COILN` is temporarily de-biased from the lift capacitor; as the inductor current decays, the discharging inductor drives `COILN` slightly below ground (negative undershoot). This explains why the lower bound of the waveform in Fig. 4.16 dips below 0 V.

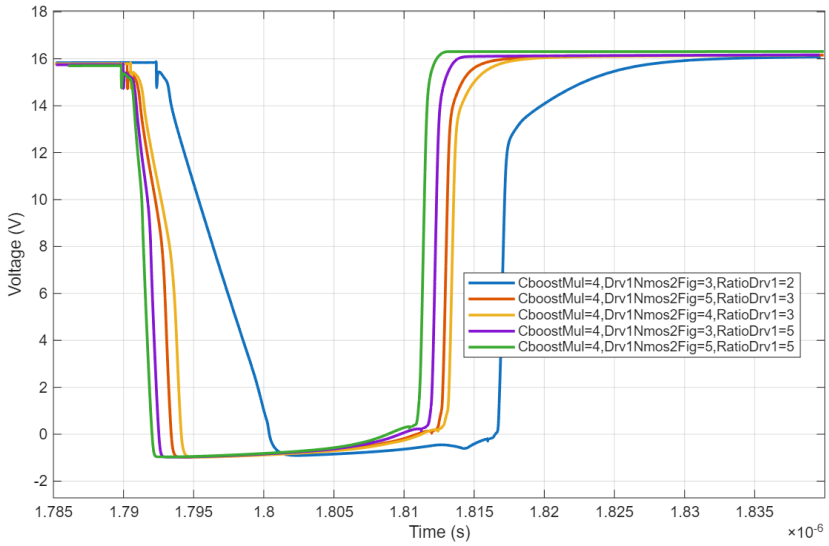


Figure 4.16: Response time vs. sizing parameters for the cascaded inverter driver.

Legend parameters: `CboostMul`—multiplier on the baseline C_{boost}; `Drv1Nmos2Fig`—NMOS finger count of the *second* driver stage; `RatioDrv1`—per-stage fan-out (FO) / geometric upsizing ratio between successive inverter stages.

After finalizing the bootstrap supply, cascaded inverter chain, and capacitive level shifter together with the connectivity fixes and sizing sweeps discussed in Sec. 2.1.2—the SW1 high-side driver is fully specified. The consolidated structure is shown in Fig. 4.17; it operates in the 12–17 V domain referenced to `COILN`, provides fast, rail-to-rail gating for the NMOS switch, and suppresses charge-sharing plateaus through the revised V_{SS} tie and the compensated bootstrap recharge path. The corresponding performance, summarized in Table 4.3, confirms sub-nanosecond edge rates and propagation delay with acceptable dynamic power across the 13.56 MHz operating window, validating the use of the driver for control of SW1 in the target application'.

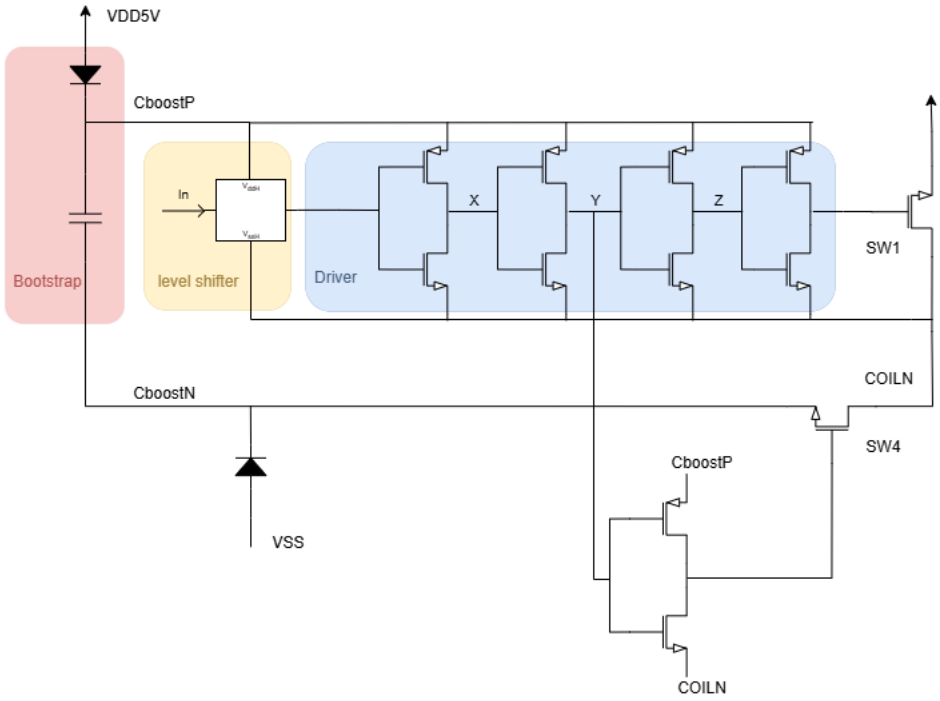


Figure 4.17: Final schematic of the SW1 high-side driver

Rise time	Fall time	Delay	Power loss
800ps-1ns	700ps-900ps	600ps-700ps	650uW

Table 4.3: Simulated performance of the SW1 driver under optimized sizing and parameter settings.

* *Power loss*: power drawn by the implemented driver from V_{DD} and I_{bias} (gate-drive/control overhead).

4.2. LIFT CAPACITOR IMPLEMENTATION

This section describes the implementation of the *lift* circuit beneath the LC tank. As shown in Figure 4.18, the network comprises an off-chip lift capacitor C_{lift} and a PMOS switch (SW3) used to stabilize the COILN node and buffer energy between operating phases. Since the capacitor is external, its value is fixed at 1 µF to minimize ripple, and the design effort focuses on the PMOS device and its driver within the 12 V–17 V domain. We evaluate the trade-offs between on-resistance and gate charge, define an appropriate gate-drive amplitude and timing strategy, and present the selected device sizing, driver scheme, and key simulation results.

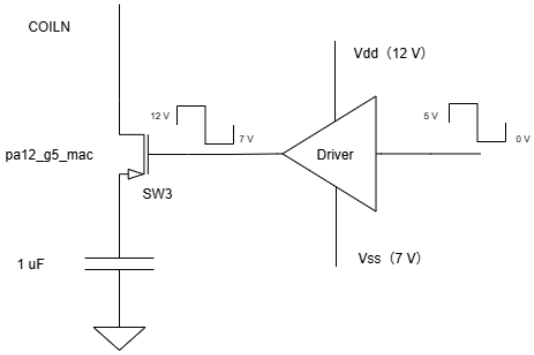


Figure 4.18: Lift capacitor circuit with SW3 and its driver

4.2.1. SW3 AND ITS DRIVER IMPLEMENTATION

SW3, as a high-side PMOS switch, pulls the COILN node up to the 12 V bias of the pre-charged capacitor during resonance and thus requires a reliable high-side driver. When SW3 is off, the inductor discharges through the load (certain path can be found in Figure 3.1), driving COILN (its drain) toward 0 V, while the capacitor positive terminal (its source) stays near 12 V. Under this condition, SW3 must tolerate almost 12 V across its terminals while keeping a safe gate bias. To meet these requirements, the PMOS device chosen is **pa12_g5_mac**, where `pa12` denotes a 12 V-rated P-type device.

SW3 DRIVER IMPLEMENTATION

The SW3 driver must provide two gate levels: 12 V (OFF) and approximately 7 V (ON). Since a stable 12 V node is already available at `Vcap` (The voltage on the positive terminal of the lift capacitor), the main challenge is to generate a reliable 7 V bias. Two approaches were investigated:

(A) Switched-capacitor voltage method. By utilizing the existing 1.8 V and 5 V supplies—both derived from the system V_{DD} setting in this design—capacitors are precharged and then, under controlled non-overlapping timing, connected in series so that their voltages add to about 7 V (see Figure 4.19). This is essentially a charge-pump style conversion, relying on alternate charging and discharging cycles to synthesize the desired level.

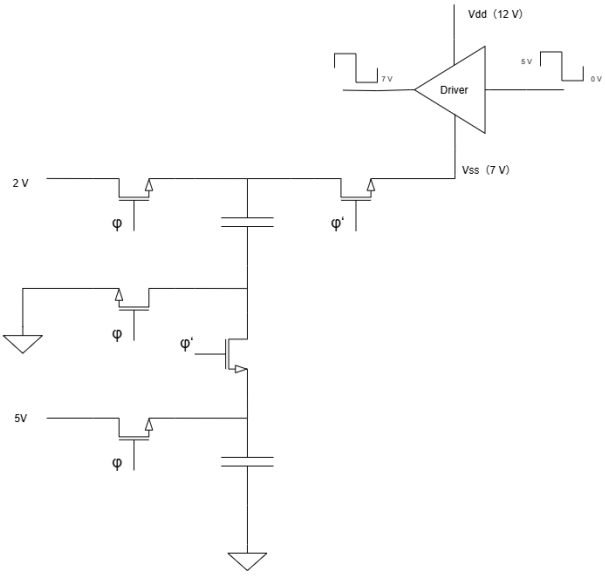


Figure 4.19: Switched-capacitor voltage scheme for generating the 7 V gate bias of SW3.

(B) AC-coupled gate drive. In this method, the control signal G3 is coupled through a capacitor to the PMOS gate, while a resistor network referenced to the 12 V source establishes a DC bias (see Figure 4.20). The AC component superimposes on this bias and temporarily pulls the gate to around 7 V, thus enabling conduction.

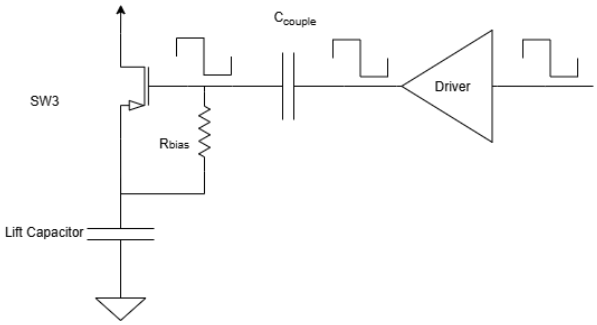


Figure 4.20: AC-coupled gate-drive scheme with resistive biasing for SW3

However, simulations revealed clear limitations in both approaches. As shown in Figure 4.21, SW3 must remain ON for most of the 1.3 µs operating cycle, with only a brief 20 ns OFF interval during the 12 V output phase. Under this condition: - The switched-capacitor method suffers from leakage when the switching state is held for long periods; maintaining a stable 7 V would require large capacitors, while additional control switches add power loss and timing complexity. - The AC-coupled approach cannot sustain a stable DC level, since the gate bias is limited by the RC time constant. It is effective

only for short transients, not for the long ON intervals required here. Furthermore, the added coupling capacitor and bias resistors introduce extra area overhead.

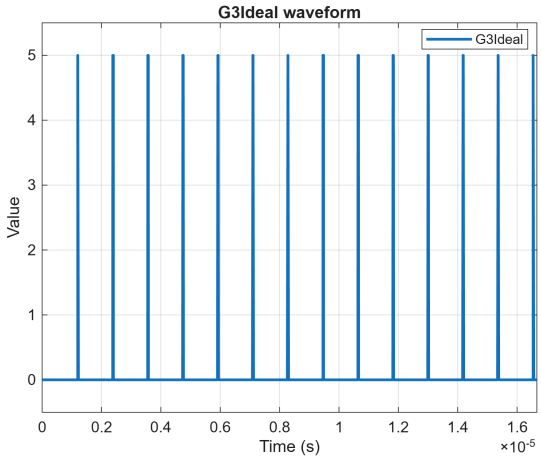


Figure 4.21: Idealized G3 control signal illustrating the normally-on operation of SW3

(C) Zener-diode stabilization (final solution). To overcome these limitations, we adopted a simple and robust scheme based on the reverse breakdown characteristic of a Zener diode as shown in Figure 4.22. By inserting a Zener diode (with breakdown voltage close to 7 V) between ground and the driver's VSS terminal, the driver is biased at approximately 7 V. With `COILN` connected to the driver's VDD terminal at 12 V, the driver naturally produces the required 7 V–12 V control signal for SW3. This approach eliminates the stability issues of the previous methods and provides a compact, low-overhead solution.

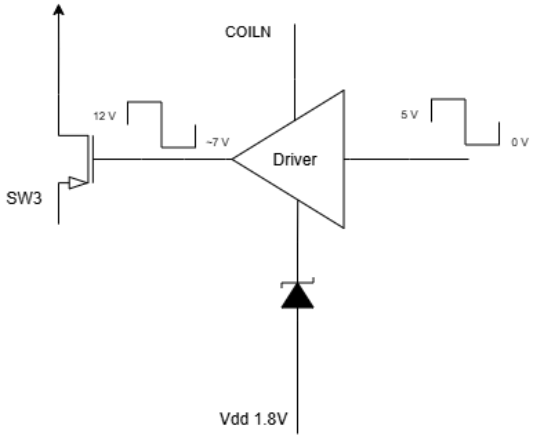


Figure 4.22: Zener-diode based driver providing a stable 7–12 V control signal for SW3.

The advantage of this scheme lies in its simplicity and the stable bias it provides. Its drawback is the static power loss introduced by the Zener diode during reverse conduction. However, the two earlier methods also suffer from comparable drawbacks: the switched-capacitor approach incurs additional switching and control overhead, while the AC-coupled scheme introduces continuous bias resistor dissipation and dynamic charging losses in the coupling capacitor. Considering these trade-offs, the Zener-diode stabilization was selected as the most practical and reliable solution for our design.

4.2.2. FINAL SCHEMATIC AND SIMULATION RESULTS

To generate the required 7 V bias for the SW3 driver, we adopt the Zener-diode stabilization scheme introduced in the previous section. The Zener is fed by a simple bias network—a current-limiting element (series resistor or current source) and a local reservoir capacitor—that (i) provides a modest DC bias current to keep the diode in regulation, and (ii) supplies/absorbs the brief pulsed current drawn during driver switching so the Zener node remains stable. This avoids tying the Zener to a low-impedance source (which would force excessive current whenever the upstream voltage exceeds the Zener voltage) and minimizes average power, since the capacitor services the fast, infrequent transients while the bias current merely restores charge between events.

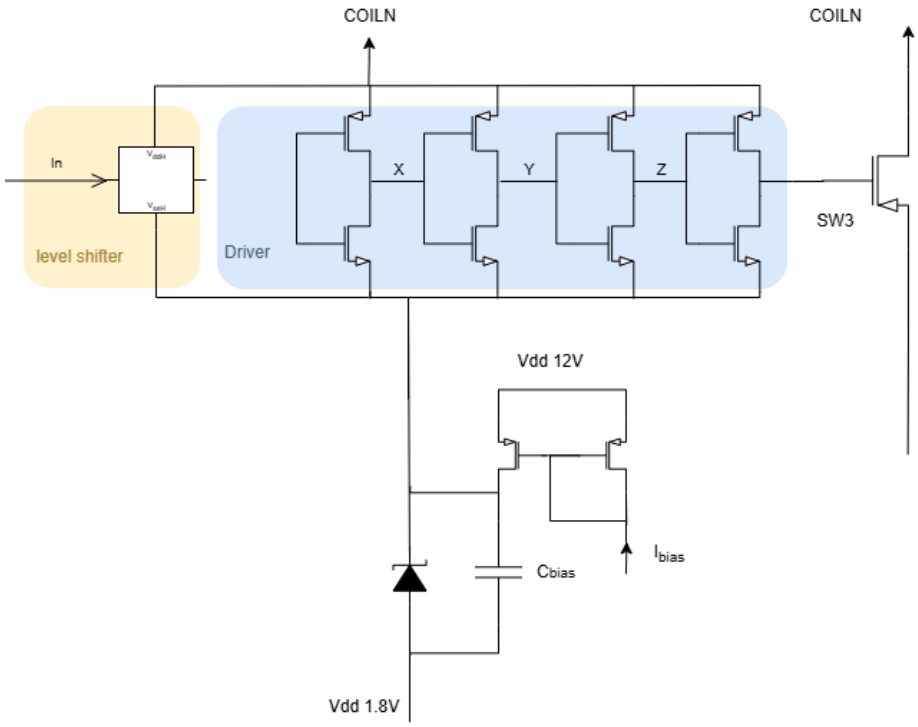


Figure 4.23: SW3 Driver Final Schematic

Except for this modification, the driver architecture largely follows the SW1 design—namely a cascaded inverter chain for drive strength and a capacitive level shifter for voltage-domain translation—with the supply rails changed to 7 V–12 V rather than 12 V–17 V. Because SW3 is a PMOS operating in this altered supply domain, the cascaded-inverter sizing was re-swept to balance delay, power, and edge sharpness. Figure 4.24 illustrates a representative rise-time sweep of the driver output for several stage-ratio choices, revealing the trade-off between slew and waveform fidelity that guided the final sizing. The finalized SW3/driver schematic is presented in Figure 4.23.

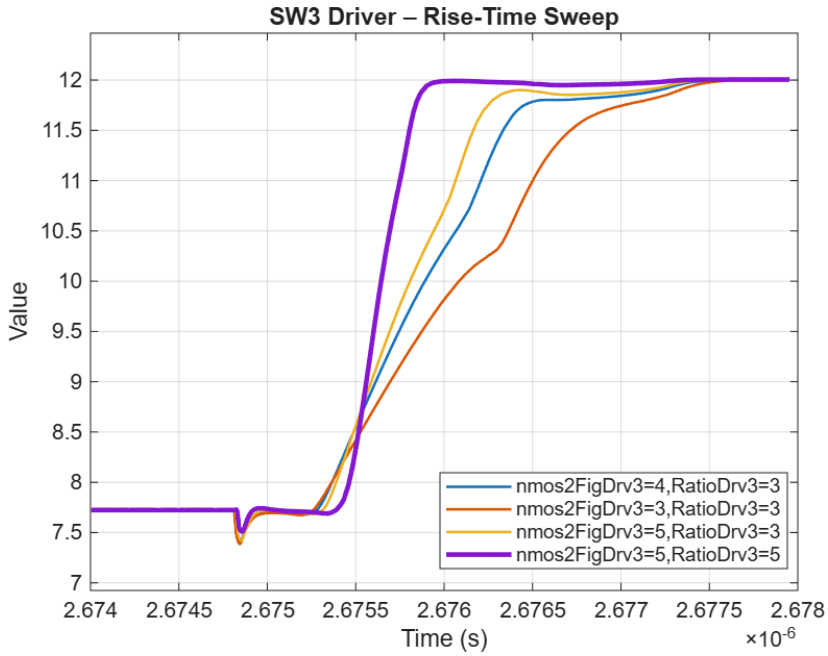


Figure 4.24: SW3 driver output (rise time) vs. cascaded-inverter sizing.

Legend parameters: `nmos2FigDrv3`—NMOS finger count of the *third* driver stage (SW3 chain); `RatioDrv3`—per-stage fan-out (FO) / geometric upsizing ratio within the SW3 cascaded-inverter chain.

With the Zener-stabilized bias and the built-in capacitive level shifter, the SW3 driver translates the 0 V–5 V logic input into the 7 V–12 V gate domain while maintaining fast edges. This enables rapid turn-off when switching from the oscillation mode to the 12 V output mode, reducing charge loss along the COILN → S3 → S2'→COILP path and thereby preserving efficiency. Figure 4.26 and Figure 4.25 show clean gate transitions and a stable ≈7 V bia. Table 4.4 summarizes the performance of optimized SW3 driver output.

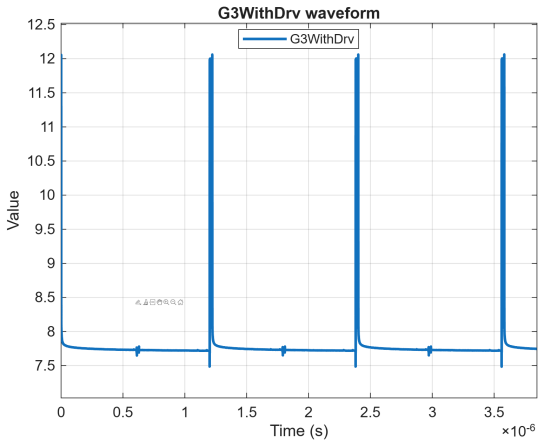


Figure 4.25: Final output signal of SW3 driver

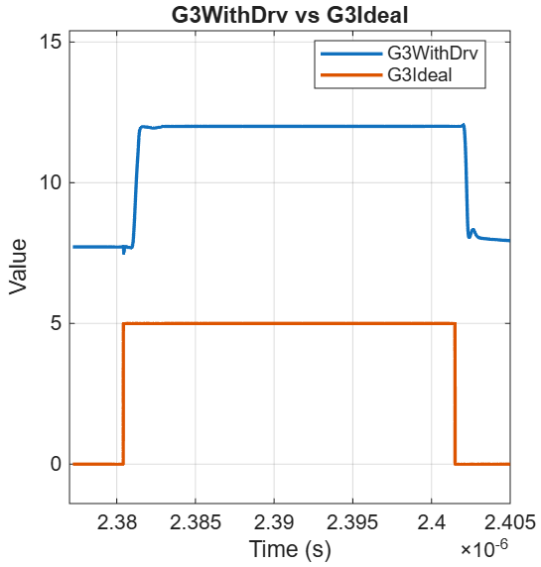


Figure 4.26: Control Signal given by SW3 driver compared to ideal logic signal

Rise time	Fall time	Dealy	Power loss
500ps-700ps	300p-400ps	600ps-700ps	500uW

Table 4.4: Simulated performance of the SW3 driver under optimized sizing and parameter settings.

* *Power loss*: power drawn by the implemented driver from V_{DD} and I_{bias} (gate-drive/control overhead).

4.3. SYSTEM EFFICIENCY: SIMULATION SETUP AND RESULTS

(1) Metrics and definitions For an IPT receiver, the primary system-level metrics are the *power-transfer efficiency* (PTE) and the *power-conversion efficiency* (PCE):

$$\mathrm{PTE} = \frac{P_{\mathrm{output}}}{P_{\mathrm{received}}} \times 100\%, \qquad \mathrm{PCE} = \frac{P_{\mathrm{output}}}{P_{\mathrm{input}}} \times 100\%. \tag{4.1}$$

PTE expresses how effectively the magnetic link delivers power to the receiver, whereas PCE expresses how efficiently the received electrical power is processed into the regulated outputs.

With the power-flow definitions in Fig. 4.27, the useful load power equals the regulated output power minus on-chip driver losses, and the transmitted/available power is set by the coil source. Hence,

$$\mathrm{PTE} = \frac{P_{\mathrm{out}} - P_{\mathrm{loss}}}{P_{\mathrm{av}}} \times 100\%, \qquad \mathrm{PCE} = \frac{P_{\mathrm{out}} - P_{\mathrm{loss}}}{P_{\mathrm{in}}} \times 100\%. \tag{4.2}$$

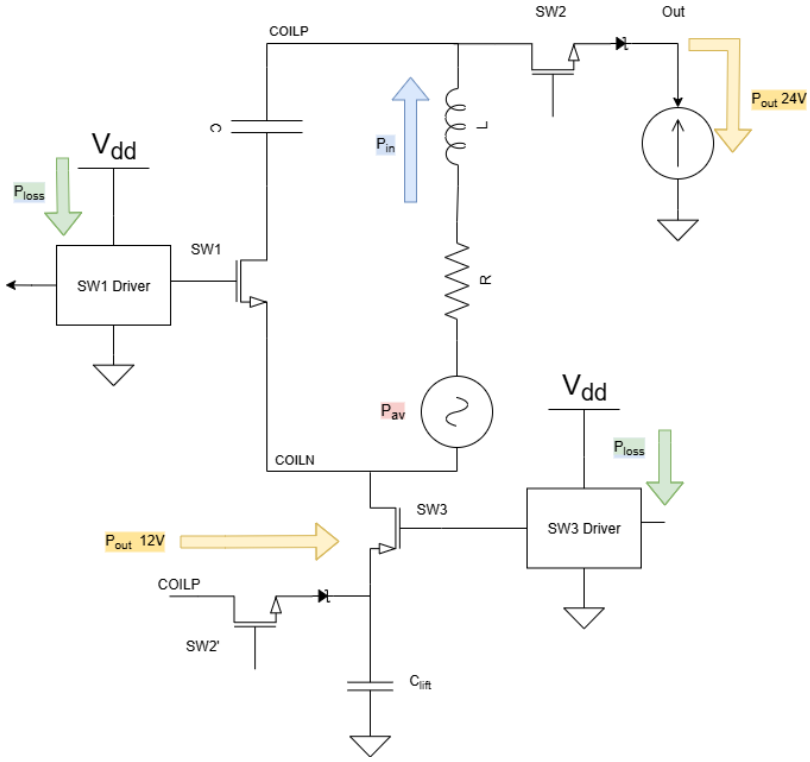


Figure 4.27: Power-flow map in the receiver: available power P_{av}, input power P_{in}, total regulated output power P_{out}, and driver losses P_{loss}.

(2) Where each power is measured and how it is integrated All powers are evaluated as cycle averages over one steady-state switching period T:

$$P_{\text{in}} = \frac{1}{T}\int_{t_0}^{t_0+T} v_{\text{coil\_p}}(t)\, i_{\text{coil\_p}}(t)\, dt, \tag{4.3}$$

$$P_{\text{out}} = \sum_{k\in\{12\text{V},24\text{V}\}} \frac{1}{T}\int_{t_0}^{t_0+T} v_k(t)\, i_k(t)\, dt, \tag{4.4}$$

$$P_{\text{loss}} = \sum_{d\in\{\text{Drv1},\text{Drv3}\}} \frac{1}{T}\int_{t_0}^{t_0+T} \big(V_{DD} - V_{SS}\big)\, i_d(t)\, dt. \tag{4.5}$$

Here $v_{\text{coil\_p}}, i_{\text{coil\_p}}$ are taken at node `COILP`; v_k, i_k are the port voltage and load current of the two regulated rails (12 V and 24 V); and $i_d(t)$ is the instantaneous current drawn from the driver supply. The available power P_{av} is the set power of the ac source representing the coupled coil. Additional bias or auxiliary blocks, if present, can be included in P_{loss} by adding terms of the form in (4.5).

(3) Numerical results and summary table Steady-state, cycle-averaged simulation results are:

$$P_{\text{av}} = 40.00\,\text{mW}, \quad P_{\text{in}} = 25.41\,\text{mW}, \quad P_{\text{out}} = 23.28\,\text{mW},$$
$$P_{\text{lossDrv1}} = 0.6702\,\text{mW}, \quad P_{\text{lossDrv3}} = 0.2948\,\text{mW}, \quad P_{\text{loss}} = 0.9650\,\text{mW}.$$

From (4.2): PTE = 55.79 %, PCE = 87.82 %.

The above definitions and cycle-averaged results are summarized in Table 4.5.

Quantity	Value
P_{av}	40.00 mW
P_{in}	25.41 mW
P_{out}	23.28 mW
P_{lossDrv1}	0.6702 mW
P_{lossDrv3}	0.2948 mW
P_{loss}	0.9650 mW
PTE	55.79 %
PCE	87.82 %

Table 4.5: System power and efficiency (cycle-averaged steady state).

5

CONCLUSION

5.1. PROBLEM AND OVERALL APPROACH

The core issue at the receiver-side oscillating supply is the lower-rail clamp imposed by the ESD protection diodes. This clamp prevents the resonant waveform from swinging below ground and crossing 0 V, which limits energy exchange and degrades the efficiency of the discharge phase.To remove this constraint, we place a lift capacitor C_{lift} in series beneath the LC tank and pre-charge it to 12 V.

With the "lifted-waveform" architecture, the cycle consolidates into four alternating stages:

$$\text{Resonance} \rightarrow \text{Output (24 V)} \rightarrow \text{Resonance} \rightarrow \text{Output (12 V, recharge } C_{\text{lift}}\text{)}.$$

During both *Resonance* stages, the waveform builds around the 12 V midpoint with a 24 V swing. The Output (24 V) stage delivers energy to the 24 V rail. The Output (12 V) stage supplies the 12 V rail while simultaneously replenishing the charge on C_{lift}, preparing the system for the next 24 V output stage.

5.2. ARCHITECTURE & KEY CIRCUITS SUMMARY

LC tank and targets. The receiver uses an LC tank tuned to 13.56 MHz with $L = 900\,\text{nH}$ and $C = ((2\pi f_0)^2 L)^{-1} \approx 154\,\text{pF}$. A coil quality factor $Q = 60$ implies $R_s = \omega L/Q \approx 1.28\,\Omega$. To cover coupling variation, the 13.56 MHz excitation is swept from 20 mV to 100 mV. The main commutating switch S_1 is an NMOS selected for adequate voltage rating, low $R_{\text{DS(on)}}$, and moderate gate charge.

SW1 high-side driver (12–17 V). S_1 is a floating high-side NMOS whose source rides on the resonant node; a 0 V–5 V logic signal cannot provide the required 12 V–17 V gate swing nor sub-nanosecond edges. The driver therefore uses a bootstrap supply (~ 17 V referred to COILN ≈ 12 V), a capacitive level shifter, and a four-stage cascaded-inverter chain. Simulated results: rise ~900 ps, fall ~700 ps, propagation delay ~700 ps, power ~650 µW.

SW3 high-side driver (7–12 V). S_3 is a high-side PMOS that must pull COILN to 12 V; a logic domain cannot generate a clean, controlled ~7 V gate bias relative to a moving source or ensure fast transitions. The driver adopts a Zener-stabilized ~7 V bias, plus a capacitive level shifter and a re-optimized cascaded-inverter chain for the reduced 7 V–12 V span. Simulated results: rise ~500 ps, fall ~300 ps, propagation delay ~700 ps, power ~500 µW.

Driver	Domain	Rise (ps)	Fall (ps)	Delay (ps)	Power (μW)
SW1 (NMOS gate)	12–17 V	900	700	600	650
SW3 (PMOS gate)	7–12 V	500	300	600	500

Table 5.1: Summary of simulated high-side driver performance

5

5.3. CONCLUSION & COMPARATIVE EVALUATION

Summary of this work. After comparing multiple candidate remedies mentioned in Chapter 2, we adopt a receiver architecture that combines a *12 V lifted bias* (via a pre-charged lift capacitor) with *dual-voltage time multiplexing* (24 V / 12 V output windows). This choice directly removes the otherwise limiting ESD lower-rail clamp and keeps the tank operating stably within a 0–24 V window. With two dedicated high-side drivers (SW1: 12–17 V, SW3: 7–12 V), the system meets the timing and edge-rate requirements at 13.56 MHz. Aggregate results are summarized in Table 3.2: receiver power-conversion efficiency **PCE ≈ 82%** and end-to-end transfer efficiency **PTE ≈ 51%** for a $P_{\text{av}} = 40$ mW.

Positioning vs. representative works (key differences). Table 3.2 summarizes this work alongside eight representative receiver designs, organized by *technology, operating frequency, rectification mode (voltage vs. current), output voltage, peak efficiency, notes, and required off-chip components*. The table provides a compact reference to position our approach in terms of output level, efficiency, and implementation choices.

Work	Tech (μm)	Freq (MHz)	Mode	V_{out}	Max Eff. @ P_{in}	Other notes	Off-chip
This work	0.13	13.56	Voltage	24/12 V (alt.)	PTE~55%; PCE~87%	ESD clamp avoided; dual-window output	L, C
Choi *JSSC'16* [7]	0.18	0.05	Current	Battery (≥1.2 V)	67.6% @ 4.2 μW	LC link; sub-μW start	L, C
Ki/Tsui *ISSCC'15* (R3+PE) [26]	0.35	13.56	Voltage	3.7 V (reg.)	92.5% @ 59.45 mW	Regulating rectifier + primary equalizer; system eff. up to 62.4%	L
Moh *ISSCC'15* (6 W) [27]	N/A	6.78	Voltage	4.2–5.8 V (5 V target)	84.6% @ 7.09 W	Resonant WPT; rectifier + buck; up to 6 W receive	N/A
Kang *RFIC'15* (UWB SoC) [28]	0.065	2400	Voltage	0.78 V (reg.)	see paper	Rectifier sensitivity −30.7 dBm for 1 V	L
Yakovlev *TB-CAS'12* [29]	0.065	1860	Voltage	1.2/0.7 V	31.9% @ 500 μW	Synchronous self-driven rectifier + LDO; mm-sized implant	L
Stoopman *VLSI'13* [30]	0.09	868	Voltage	1.0 V	31.5% @ −15 dBm	Self-calibrating rectifier + resonant matching; long-range demo	L
Le *JSSC'08* [31]	0.25	906	Voltage	1–9 V (cond.-dep.)	60% (peak)	36-stage passive rectifier; far-field	L
Martins *TCSI-I'21* [32]	0.18	403.5	Voltage	1.8 V (reg.)	40.2% @ −9.1 dBm	Rectifier + adaptive match + MPPT buck-boost; sensitivity −24 dBm	L, C

Table 5.2: Receiver comparison (this work vs. representative prior art).

- **High-voltage delivery at 13.56 MHz.** Unlike most entries in Table 3.2 that target 0.6–5 V rails for battery charging or low-voltage PMUs, our receiver *directly* supplies **24 V / 12 V** windows without a post boost/charge-pump, which is advantageous for high-voltage loads and drivers.
- **Immunity to ESD clamping.** By lifting the tank's DC level by 12 V, the design is intrinsically robust to the ESD lower-rail clamp—an issue rarely addressed explicitly in prior art—allowing consistent 0–24 V resonance and controlled energy release.
- **Efficiency–complexity balance.** Without adaptive matching/MPPT, the receiver attains **PCE ≈ 82%** with **PTE ≈ 51%**. While this does not match the very highest end-to-end efficiencies of watt-level near-field systems, it offers a practical trade-off of *high-voltage output* with *lightweight control and implementation complexity*.

Limitations and notes. The lifted-bias requires an **off-chip large capacitor** (~1 μF) to stabilize the 12 V level and suppress ripple. The **7 V Zener stabilization** used in the SW3 driver incurs static loss; moreover, many efficiencies in Table 3.2 are from *measured* silicon in prior works, whereas our figures are primarily from *post-layout/system-level simulations*, so cross-paper numerical comparisons should be regarded as indicative rather than absolute. Finally, the architecture **periodically allocates a recharge slot** to replenish the lift capacitor.

5.4. FUTURE WORK

Planned directions include three closely related tracks. First, completing *layout and post-layout signoff* for the entire receiver. To date, only the two SW high-side drivers

have undergone layout and post-layout verification; the remaining blocks (control logic, comparator front-end, output stage, and the lift-capacitor interface) still require full layout, parasitic extraction (PEX), and verification across PVT corners.

Second, replacement of the *ideal comparators* used in simulations with an integrated *low-latency, low-power comparator* to support mode transitions based on COILP thresholds (0 V, 12 V, 24 V). Excessive comparator delay directly degrades the SW turn-off instant: if threshold detection lags the intended *voltage peak* of COILP, the LC tank is disconnected on the down-slope of Vcoil, by which time part of the magnetic energy has already flowed back into the tank capacitor. The inductor current available at hand-off is therefore smaller, lowering discharge efficiency and increasing losses. Consequently, minimizing comparator delay under a tight power budget is critical.

Third, *power and efficiency optimization.* The 7 V Zener-stabilized gate-bias in the SW3 path introduces static loss; the bias could consider to be duty-cycled and enabled only when SW3 is active (e.g., a duty-cycled switched-capacitor pre-regulator with a gate clamp, or a bootstrapped charge-sharing scheme) to reduce average dissipation. Management of C_{lift} should lengthen the interval between recharges (i.e., recharge less frequently), shorten the recharge duty, and trigger predictive recharge only when needed. After these steps, measured PTE/PCE, edge timing, and V_{lift} ripple should be calibrated against the post-layout models used in this work. In addition, the design should be extended with on-chip 1.8 V and 5 V outputs from the existing *imec* IP so that the converter does not require external supplies.

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