Optimizing generator protection by developing an islanding tripping scheme with Siemens SIPROTEC 5 IED's for DOW Industrial network

by Mihaela Petcu

to obtain the degree of Master of Science

at Delft University of Technology,

to be defended publicly on 8th of September, 2025

Student number:	5843758	
Thesis committee:	Prof. dr. ir. M. Popov,	TU Delft, supervisor
	Dr. ir. M. G. Niasar,	TU Delft
	Ir. S. de Clippelaar,	DOW Energy System Technology Center (ESTC)
	Dr. ir. K. Polat,	Siemens PTI

TU Delft

Abstract

Dow Terneuzen, the second-largest site of Dow Chemical, relies on the ELSTA cogeneration plant to supply electricity and steam to its production facilities while contributing to the Dutch national grid. Ensuring stable operation is critical for safety and reliability. While internal disturbances are managed by existing protections, external grid faults pose challenges for detection and for enabling a controlled transition to islanded operation.

This thesis develops and validates an islanding tripping scheme for Dow Terneuzen. The objectives are to design a protection logic based on frequency and undervoltage detection, establish a load shedding strategy to maintain generator stability during islanding and validate the protection logic using online simulations and hardware testing. A dynamic model of the power system was created in ATP-EMTP, including synchronous machines with governors and excitation systems, transformers, and dynamic loads. Fault scenarios were simulated to assess stability, determine critical clearing times, and validate the protection logic. The protection logic was then programmed into a Siemens 7UM85 relay using DIGSI5 and tested with an Omicron CMC 356+, where COMTRADE signals from simulations were replayed into the relay. Relay responses were analyzed using the Fault Record tool SIGRA and compared with the online simulation results.

The results show how generator dynamics affect stability, confirm the need for rapid load shedding, and highlight challenges in designing a reliable islanding tripping scheme. The comparison between ATP-EMTP simulations and relay tests demonstrates the effectiveness of the proposed scheme and provides practical guidance for implementing reliable islanding protection at Dow Terneuzen.

Contents

List of Figures

List of Tables

Acknowledgement

I would like to thank my thesis supervisor, Professor Dr. Marjan Popov for his support, shared knowledge and patience during the completion of the master thesis project.

Also, I would like to thank Ir. Steven de Clippelaar for his continuous support during the thesis project, from the power system model to the relay testing. I am very grateful for the time and knowledge that you have shared with me.

I would like to thank my Siemens mentor, Dr. Keysan Polat for his support as well as the Protection, Automation and Control team of Siemens Zoetermeer for the technical support and kindness.

Thank you, everyone!

1

Introduction

Dow Chemical is one of the world's leading materials science companies with significant operations in the Netherlands, including its second-largest facility worldwide located in Terneuzen. Established in 1965, Dow Terneuzen produces essential plastics and chemicals used across various industries such as electronics, automotive, renewable energy, and construction materials. As the largest employer in Zeeuws-Vlaanderen, Dow significantly contributes to regional economic growth, employment, and social initiatives [3].

Dow Terneuzen owns the ELSTA power plant, a cogeneration plant that has been supplying both electricity and steam to the Terneuzen Industrial Park since 1998 and contributes to the national electricity grid of TenneT [15]. The chemical plant's electrical stability is of highest importance because downtime and unplanned events pose potential risks to the plant, personnel, and environment. Effective protection schemes involving relays and specialized devices are already in place to manage internal faults of the power system. However, external faults originating from the national grid's side present significant challenges in accurate detection and isolation, making it difficult for the facility to safely transition into an independent, islanded operation mode during disturbances.

This thesis project focuses on the development of a reliable island tripping scheme to ensure quick and safe isolation of Dow's facility during external grid faults.

1.1. Problem definition and objectives

The gas turbines at the Dow power plant are providing steam and electricity for the production plants. An islanding tripping scheme is required at the three incoming feeders 150/50 kV. The research objectives are defined by Dow:

- developing an islanding tripping scheme based on frequency and reverse current with under voltage or new developments;
- developing the load shedding basis by defining the amount of load that needs to be tripped to keep the machines stable when switched to island;
- making use of the existing ATP-EMTP model to verify settings, predict machine behavior and check against stability;
- performing sensitivity studies on important parameters, such as fault duration, frequency decay, how fast to swop from droop to isoc and trip the second machine;
- testing the islanding tripping scheme dynamically with Comtrade files generated by ATP-EMTP;
- testing the new Siemens df/dt and frequency detection relay 7UM85 for islanding detection and load shedding of non-critical loads.

1.1.1. Research questions

Based on the previously defined research objectives, the thesis project needs to answer the following research questions.

1. How do machine dynamics influence the power system stability?
2. What measures need to be taken to ensure stability of the power system in an islanded scenario?
3. What are the challanges when designing an islanding tripping scheme at the MV substation level?
4. What are the fault response differences between the protection scheme programmed with ATP-EMTP vs with DIGSI5 in the 7UM85 relay?
5. Does the protection scheme programmed with the 7UM85 relay handle the dynamic behavior of the power system correctly?

1.2. Research Methodology

The flowchart presented in Figure 1.1 ilustrates the steps followed to fulfill the thesis objectives and answer the research questions.

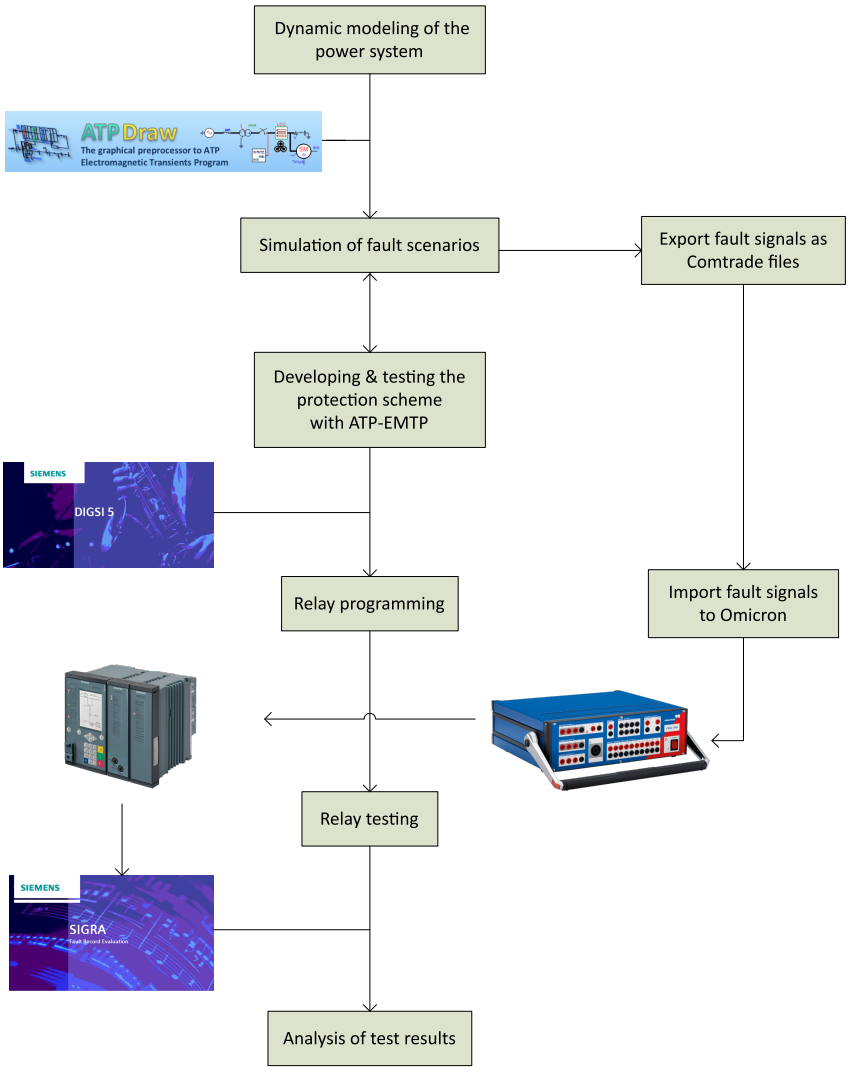


Figure 1.1: Processes used to fulfill the thesis objectives

1. The power system is dynamically modeled using ATPDraw and it includes the synchronous machines (generators) with their control systems (governor and excitation system), transformers (two and three winding transformers and saturable transformer to simulate the tap changer functionality) and dynamic loads such as induction motors. TACS (Transient Analysis of Control Systems) and MODELS (a simulation language) interfaces enable modeling of control systems and components with nonlinear characteristics.
2. Test cases are defined according to fault location, fault type and load condition. They are simulated in ATPDraw and used for stability analysis, as well as testing and validation of the protection scheme. The output voltage and current plots are exported in Common format for Transient Data Exchange (COMTRADE .CFG file).
3. The development of the protection logic is performed in ATPDraw using both TACS and MODELS interfaces. The fault scenarios are simulated again to test and validate the protection logic.
4. The same protection scheme is then programmed in the 7UM85 relay using the DIGSI5 software available from Siemens.
5. The programmed protection logic is then tested in the physical relay with the Omicron CMC +356. The previously exported fault signals (.CFG files) are imported into Omicron: an Omicron Control Centre (.OCC) file is created and the fault signals are played back into the relay by using the Advanced TransPlay Module.
6. The fault log is recorded into the relay and exported for further analysis using SIGRA - the fault record evaluation tool provided by Siemens.

1.3. Thesis Layout

The thesis report consists of seven chapters, each focusing on a specific aspect of the research objectives and related findings. A brief overview of each chapter is provided in this section.

Chapter 2 provides an overview of protection practices related to islanding of industrial networks by analyzing the reliability of different protection settings in the development of an islanding tripping scheme. Optimization algorithms of the relay protection settings are discussed, as well as advantages and shortcomings of current practices.

Chapter 3 describes the power system topology and the characteristic parameters of the synchronous generators. The methodology used to model the power system for transient stability analysis is introduced and the power system components are explained according to the ATP-EMTP software.

Chapter 4 analyzes the stability of the power system for three independent load scenarios. The power system behavior is studied for each scenario under different fault conditions: three types of faults (three-phase to ground, two-phase to ground and single-phase to ground) are simulated at four different locations. The stability limits are identified by analyzing rotor angle oscillations, voltage and frequency variations. Finally, the critical clearing time is determined per fault type, location and load scenario. The electro-mechanical behavior of the synchronous generators is explained for a better understanding of how machine dynamics are influencing the power system stability. Finally, the system level stability is studied at the MV busbar by analyzing the change in voltage and currents at outgoing feeders.

Chapter 5 explains the development and validation of the protection logic using the ATP-EMTP software. A disconnection from the national grid demands compliance with the Dutch NetCode requirements which are provided at the beginning of this chapter, followed by a description of the individual protection settings as per the relay manual. The developed models of the protection settings are explained and the code is attached to Appendices. Finally, the islanding tripping scheme is validated by simulating eight different test cases and the results are discussed.

Chapter 6 describes the implementation of the protection logic in the 7UM85 relay using DIGSI5 software and the testing setup used to validate the protection scheme. The testing system includes an Omicron CMC 356+ device connected to the 7UM85 relay and a laptop. The Advanced Transplay Module is used to import the fault signals from ATP-EMTP into the Omicron CMC 356+ and from the Omicron into the relay. The fault records are exported from the relay into SIGRA and the results are discussed. A comparison between the results obtained with ATP-EMTP vs the relay is provided and a discussion is added based on the findings and explanations provided by Siemens.

Chapter 7 summarizes the outcomes of the thesis project by providing the conclusions and recommendations for future works.

2

State of the art and research goal

The increasing penetration of distributed generation (DG) and on-site generation in industrial facilities has created significant challenges for power system protection and control. When these facilities become electrically isolated from the utility grid, rapid detection and appropriate system response are critical to prevent equipment damage, maintain power quality, and ensure operational continuity [17], [6], [2].

The consequences of undetected islanding are severe and multifaceted. From a safety perspective, utility personnel may be exposed to hazardous conditions if they believe a section is de-energized when it remains powered by DG [6]. From an equipment protection point of view, if the utility attempts to reclose onto a not synchronised island, the resulting mechanical stress can cause significant damage to rotating machinery. Besides, the power quality issues of an islanded system can affect sensitive industrial processes and connected loads [2].

This overview examines the current state of research and practical implementations for islanding detection and control systems in power systems with on-site generation and utility grid connection.

2.1. Classification of Islanding Detection Methods

Topology-based islanding detection schemes represent the earliest approach to this problem, relying on breaker communication and state information to determine system configuration [2]. These schemes use hardwired signals or dedicated communication channels to transmit the status of critical switching devices to generator protection systems.

The primary advantage of topology-based schemes is their simplicity and direct correlation with actual system conditions. However, as demonstrated in [2], these systems become increasingly complex and unreliable as system topology evolves. The addition of new transmission lines, substations, or switching configurations requires corresponding updates to the communication infrastructure and logic, which are often deferred or inadequately maintained.

2.1.1. Local-Area Measurement-Based Schemes

Frequency-based detection methods represent the most widely implemented approach to islanding detection, leveraging the fundamental relationship between active power balance and system frequency [9]. Traditional over/underfrequency protection (81O/81U) provides basic islanding detection capability but suffers from slow response times due to the need for time delays to prevent operation during transient conditions [2].

Rate-of-change-of-frequency (RoCoF) methods, particularly the 81RF element, offer significant improvements in detection speed and sensitivity [17]. The 81RF characteristic combines frequency deviation from nominal with the rate of frequency change, enabling faster detection than conventional

frequency elements. As demonstrated in [17], 81RF elements can detect islanding conditions within milliseconds while maintaining security against false operation during system faults.

RoCoF methods face significant challenges in discriminating between islanding and system events that cause rapid frequency changes. [4] demonstrates through dynamic modeling that standard RoCoF relays experience security problems during system faults, with failure rates exceeding 80% even at relatively insensitive settings. This has led to research of adaptive frequency estimation methods, such as the Kalman filter approach proposed by [7], which significantly improves relay security by desensitizing frequency measurements during detected fault conditions.

Voltage-based islanding detection methods are based on the changes in terminal voltage that occur when synchronous generators are disconnected from the grid. The effectiveness of these methods depends heavily on the reactive power mismatch between generation and load. When generation exceeds the load capacity, overvoltages occur. Conversely, a higher load than generation leads to undervoltage [2].

The primary limitation of voltage-based methods is their susceptibility to operation during utility system faults, which also cause voltage deviations. Additionally, modern excitation control systems may initially compensate for voltage changes, delaying detection and reducing method effectiveness. Beacuse of this, voltage-based methods are used as supplementary elements rather than primary detection mechanisms.

Vector shift relays (VSR) detect the instantaneous phase-angle changes that occur when a generator transitions from grid-connected to islanded operation [6]. These relays measure the duration of voltage cycles and compare consecutive measurements to detect phase jumps.

Paper [6] demonstrates that while VSRs can provide very fast detection (within one cycle) for significant power mismatches, they suffer from a large non-detection zone (NDZ) for small power imbalances and are susceptible to false tripping during network disturbances. The study reveals that current IEEE and EN standards requiring 2% power mismatch detection are incompatible with commercially available VSR settings, as the required sensitivity levels result in unacceptable false trip rates during normal system events.

Advanced vector shift algorithms have been developed to address these limitations; [11] presents an enhanced algorithm that adapts to steady-state frequency variations and includes comprehensive blocking logic to prevent operation during faults and other disturbances. This approach demonstrates improved stability during various non-islanding events while maintaining detection capability for both small and large power imbalances.

Impedance-based detection methods monitor the effective system's impedance as seen from the generator terminals [2]. During grid-connected operation, the parallel combination of utility and plant impedances results in relatively low effective impedance. When islanded, the effective impedance increases substantially as only the series combination of plant elements remains. However, these methods require additional signal injection equipment and complex impedance calculation algorithms, limiting their practical application.

2.1.2. Wide-Area Measurement-Based Schemes

Wide-area measurement systems leverage synchronized phasor measurements to detect islanding by comparing phase angles between the industrial facility and utility system [2]. These schemes calculate slip frequency and acceleration based on time-synchronized measurements from phasor measurement units (PMUs) installed at both locations.

The primary advantage of wide-area schemes is their independence from power balance conditions and system topology. They can reliably detect islanding regardless of the active and reactive power mismatch, addressing the fundamental NDZ limitation of passive methods. However, they require sophisticated communication infrastructure, precise time synchronization, and cooperation from utility companies to provide remote measurements. The cost and complexity of implementing such systems often make them impractical for smaller industrial facilities, limiting their application to large and crucial installations.

Advanced Multi-Principle Approaches

Recognizing the limitations of single-parameter detection methods, recent research has focused on approaches that combine multiple detection techniques with voting supervision logic. The islanding detection logic developed in [2] combines fast RoCoF detection with directional power monitoring, supervised by voting logic that considers multiple relay inputs and communication channel statuses.

This approach addresses both security and dependability concerns through redundancy and intelligent decision-making. The voting supervision logic accounts for equipment failures, communication channel outages, and various system operating conditions to make reliable islanding decisions. For primary detection, the system requires three out of four transformer communication channels to be operational, two out of four transformers to detect the islanding condition, and one out of two generators to confirm the event.

The secondary detection scheme provides backup capability and accounts for breaker failure scenarios by monitoring directional power flow in transformer feeders. The integration of these multiple detection principles with supervision logic significantly enhances both the security against false trips and the dependability for actual islanding events.

Paper [14] describes a complete network disconnection solution that combines 81RF based detection with coordinated generator shedding, load shedding, and generator runback control.

This integrated approach recognizes that successful islanding requires not only rapid detection but also immediate corrective action to maintain power balance and system stability. The system uses decremental reserve margin (DRM) concepts to determine appropriate generator shedding and runback levels, with coordination logic to prevent oscillatory behavior between generation and load shedding systems.

Traditional frequency estimation methods used in RoCoF relays are susceptible to security issues during system disturbances. [7] proposes an adaptive frequency estimation method based on Kalman filtering that significantly improves RoCoF relay performance. This approach uses fault detection based on DC offset and negative sequence current measurements to adjust the frequency estimation during disturbed conditions adaptively.

The results demonstrate substantial improvements in relay security, with the adaptive method achieving 100% security for adjacent feeder faults at 0.5 Hz/s settings, while standard methods failed even at 1.0 Hz/s settings. This enhanced security enables more sensitive relay settings, thereby reducing the non-detection zone (NDZ) without compromising operational security.

2.2. Current Research Gaps and Future Directions

Despite significant advances in islanding detection technology, several research gaps remain. The fundamental NDZ problem persists across most passive detection methods, necessitating either acceptance of detecting the blind spots or the implementation of more complex active or communication-based solutions. The trade-off between detection sensitivity and security remains a challenge for power system engineers. Emerging areas of research include machine learning approaches for pattern recognition in islanding detection, integration with advanced distribution management systems, and development of standards for multi-principle detection schemes.

2.3. Conclusion

The literature reveals a clear evolution in islanding detection from simple single-parameter schemes toward complex multi-principle approaches with integrated control capabilities. While traditional methods such as RoCoF and vector shift detection continue to play the important role, their limitations necessitate improved algorithms, adaptive techniques, or supplementary detection principles.

The most successful modern implementations combine multiple detection methods with comprehensive supervision logic and integrated control systems. These approaches address both the technical challenges of reliable detection and the operational requirements for stable islanded operation. However, they require significant engineering expertise, testing resources, and system integration capabilities.

3

Description and Modeling of the Studied Power System

This chapter outlines the methodology used to model and simulate the power system for transient stability analysis. The study utilizes ATP-EMTP, a powerful time-domain simulation tool that can represent detailed electrical networks, control systems, and fault scenarios. The modeling includes the generator, control systems, the transmission infrastructure, loads, and measurement blocks.

3.1. Power System Description

The power system to be studied is part of a double-feeder radial network with a connection to the utility grid through three main transformers at the point of common coupling (PCC) and generation on site using a single shaft combined-cycle steam and gas power plant (ELSTA), as shown in Figure 3.1.

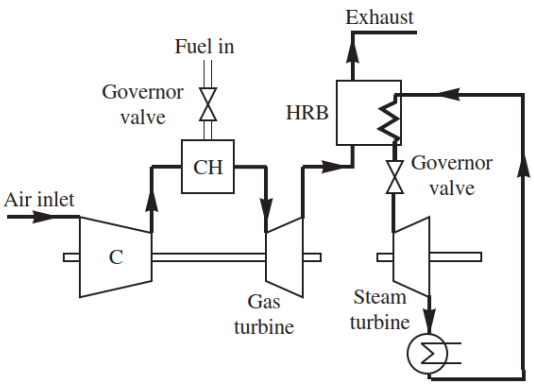


Figure 3.1: Example of a Combined-Cycle Gas Turbine [12]

The ELSTA power plant supplies steam and electricity to Dow Benelux, as well as electricity to the local TenneT power grid. ELSTA produces steam and electricity using three gas turbines (referred to as GTG-101, GTG-201, GTG-301) with a maximum power of 123 MW and a steam turbine (STG-001) with a maximum power of 90 MW. Behind each gas turbine, a heat recovery boiler (HRB) with additional duct burners is installed, and the generated steam (90 bar) is supplied to Dow's chemical facility.

Synchronous generators are connected to the high voltage (HV) transmission network via a step-up transformer that forms the generator-transformer unit. The power system load contains induction motors, meaning the load operates at a lagging power factor and consumes positive reactive power. For this reason, the generators are overexcited, operate at a lagging power factor, and supply positive

reactive power to the system [12]. The parameters concerning the design data of the synchronous generators are presented in Table 3.1.

Parameter	Value
Rated power	139 MVA
Rated voltage	11.5 kV
Rated power factor	0.85
Rated frequency	50 Hz
Rated speed / Overspeed (test for 2 minutes)	3000 / 3600 rpm
Voltage variation range	± 10%
Frequency variation range	-4 / +2 %
Maximum combined variation voltage/frequency	± 10%
Phase number / Phase connection	3 / Star
Rated current	6978 A
Excitation system	Static
Prime mover	Gas / Steam Turbine

Table 3.1: Generator Specifications

The synchronous generators are driven by a prime mover, which is the gas turbine for this project. Each turbine is equipped with a governing system to provide a means by which the turbine can be started, run to the operating speed, and operate on a load with the required power output. The DC excitation (or field) current produces the magnetic field inside the generator. The excitation current and, consequently, the generator's terminal voltage, are controlled by the automatic voltage regulator (AVR).

The characteristic parameters of the generators can be seen in Table 3.2.

Description	Unit	Value
Inertia constant H	s	0.89
Short - circuit ratio	-	0.5
REACTANCES:		
Synchronous d-axis reactance (unsaturated) X_{di}	p.u.	2.15
Synchronous q-axis reactance (unsaturated) X_{qi}	p.u.	2.05
Transient d-axis reactance (unsaturated) X'_{di}	p.u.	0.29
Transient q-axis reactance (unsaturated) X'_{qi}	p.u.	0.48
Subtransient d-axis reactance (unsaturated) X''_{di}	p.u.	0.22
Subtransient q-axis reactance (unsaturated) X''_{qi}	p.u.	0.24
Transient d-axis reactance (saturated) X'_{d}	p.u.	0.29
Subtransient d-axis reactance (saturated) X''_{dv}	p.u.	0.167
Negative sequence reactance (saturated) X_2	p.u.	0.22
Zero sequence reactance (saturated) X_{0i}	p.u.	0.09
Armature leakage reactance (unsaturated) X_a	p.u.	0.14
TIME CONSTANTS (at 75 °C):		
Transient d-axis time const. at no load T'_{do}	s	5.25
Transient d-axis time const. at short circuit T'_{d}	s	0.71
Subtransient d-axis time const. at no load T''_{do}	s	0.022
Subtransient d-axis time const. at short circuit T''_{d}	s	0.017
Armature time constant T_a	s	0.54

Table 3.2: Characteristic Parameters

3.2. Modeling Environment

The Electromagnetic Transients Program (EMTP) is a simulation program used to predict variables of interest within electric power networks as functions of time, typically following a disturbance such as the switching of a circuit breaker or a fault [5]. The Alternative Transients Program (ATP) is a widely used program for digital simulation of transient phenomena of electromagnetic and electromechanical nature in electric power systems.

EMTP simulates transients of the electrical power network by solving the algebraic, ordinary, and/or partial differential equations that are associated with an interconnection of the following components:

- Lumped resistance, inductance, capacitance
- Multiphase Pi-equivalents
- Multiphase distributed-parameter transmission lines
- Nonlinear resistors
- Nonlinear inductors
- Time-varying resistance
- Switches
- Voltage or current sources
- Dynamic rotating electric machinery
- Control system dynamics

Trapezoidal-rule (second-order) implicit integration is used on the defining equations of most elements that are described by ordinary differential equations. The result is the formation of an associated set of real, simultaneous, algebraic equations that are solved at each time step. These equations are placed in nodal-admittance form, with new unknown voltages as variables, and are solved by ordered triangular factorization. Program output consists of component variables (e.g., branch currents or voltages, machine torques or speeds, etc.) as functions of time [5].

In [13], the details of ATP modeling capabilities can be studied; this chapter focuses only on the models relevant to the thesis project.

3.3. Power System Configuration

The studied power system of Dow's industrial network is modeled in ATPDraw, a graphical interface for ATP-EMTP. ATPDraw enables the construction of network schematics, while ATP handles the underlying numerical simulation. Interfacing capability to the program modules TACS (Transient Analysis of Control Systems) and MODELS (a simulation language) enables modeling of control systems and components with nonlinear characteristics [8].

The single line diagram (SLD) of Dow's power system modeled with ATPDraw is shown in Figure 3.2.

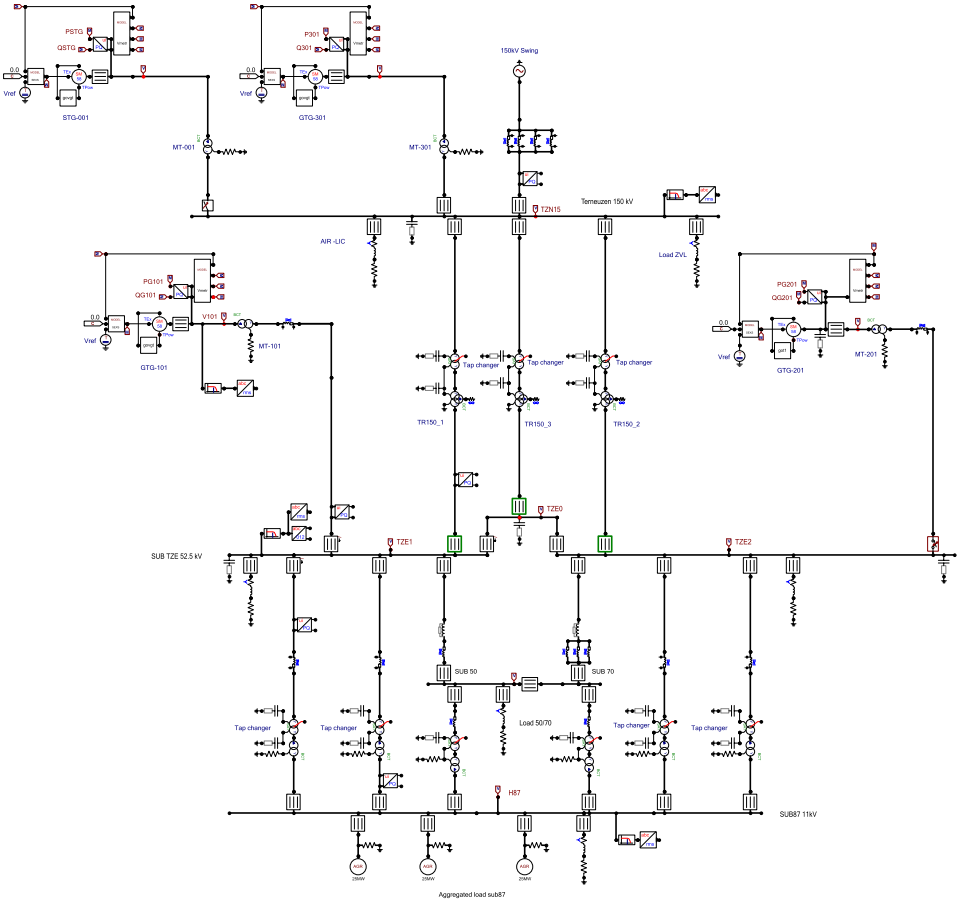


Figure 3.2: Single line diagram of Dow's Industrial Network

The system consists of three synchronous generators connected to the utility grid through three transformers and transmission lines. Both static and dynamic loads are included. The generators are supplied with an excitation system, a governor and measurement devices to monitor dynamic variables.

3.4. Component Modeling in ATPDraw

3.4.1. Synchronous Generator (SM58)

The synchronous machine is modeled using the SM58 block, which represents a round-rotor generator. Based on the system under study, parameters such as rated power, voltage, reactances, and time constants are specified. The generator includes mechanical input and electrical excitation terminals.

Figure 3.3 shows an overview of the components connected to provide a complete representation of the generating unit.

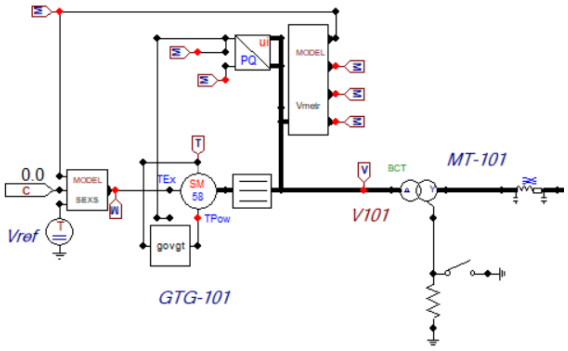


Figure 3.3: Synchronous machine & control systems

First, the modeling of the synchronous machine is explained. The synchronous generator prime mover is modeled using the SM58 component available in the ATPDraw library and can be seen in Figure 3.4.

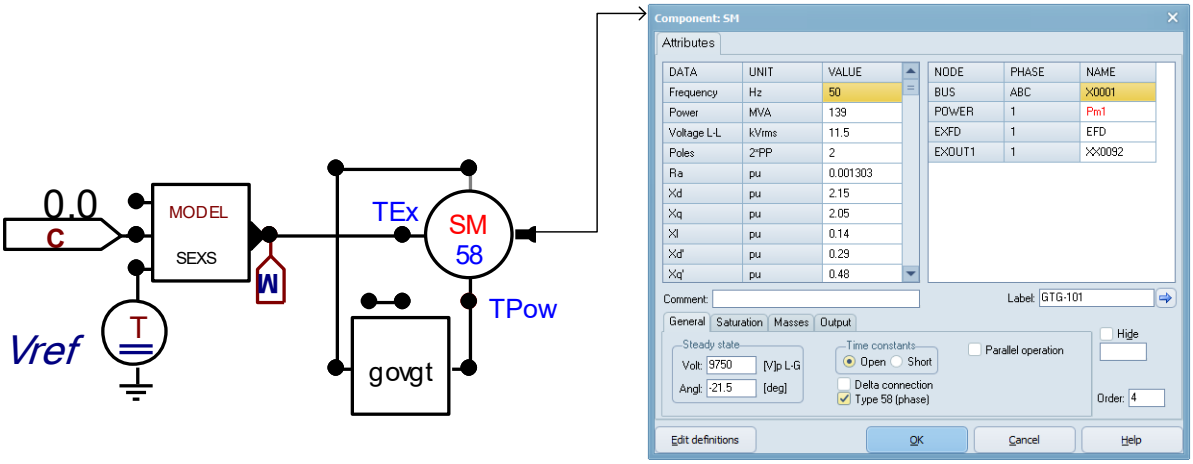


Figure 3.4: Rotating Machine model

The section “DATA” includes the generator design data, as well as characteristic parameters, that were extracted from the Generator Data Sheet and can be seen in Tables 3.1 and 3.2. The output parameters that can be selected from the SM58 component are provided in Table 3.3.

Parameter	Unit	Description
ID	A	current in the d-axis armature winding
IQ	A	current in the q-axis armature winding
I0	A	armature winding zero sequence current
IF	A	field winding current
IKD	A	current in the d-axis damper winding
IG	A	current in the eddy-current winding
IKQ	A	current in the q-axis damper winding
IA	A	current in phase ”a” of the armature winding
IB	A	current in phase ”b” of the armature winding
IC	A	current in phase ”c” of the armature winding
VF	V	voltage applied to the field winding
MFORCE		the total mmf in the air-gap of the machine
MANGLE		angle between the q- and d-axis components of the total mmf
TEG		electromagnetic torque of the machine
TEXC		electromagnetic torque of the exciter
ANGLE		mechanical angle deviations of the mass
SPEED	rad/ s	deviation in mass speed from synchronous speed
TORQUE	1e6*Nm	mechanical torque between masses

Table 3.3: Output parameters of the SM58 component

3.4.2. Excitation System and AVR (MODELS)

The Excitation System and Automatic Voltage Regulator (AVR) are modeled using the MODELS language in ATP-EMTP and follow the model of a Simplified Excitation System (SEXS) [10]. The block diagram of the SEXS model is shown in Figure 3.5 and the system’s parameters are provided in Table 3.4.

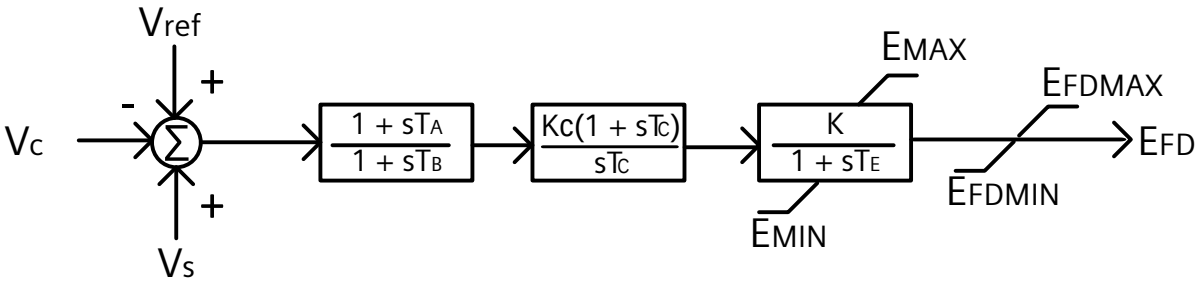


Figure 3.5: Simplified Excitation System (SEXS) block diagram

NAME	Type	Description
TATAB	Float	Ta/Tb - gain reduction ratio of lead-lag element
TB	Seconds	Time constant
KC	PU	PI controller gain
TC	Seconds	PI time constant
K	PU	Gain
TE	Seconds	Time constant
EMIN	PU	Minimum field voltage output
EMAX	PU	Maximum field voltage output
EFDMIN	PU	Field voltage clipping minimum limit
EFDMAX	PU	Field voltage clipping maximum limit

Table 3.4: Excitation System and AVR Parameters

The implemenattion of the excitation system in ATP-EMTP is provided in Figure 3.6.

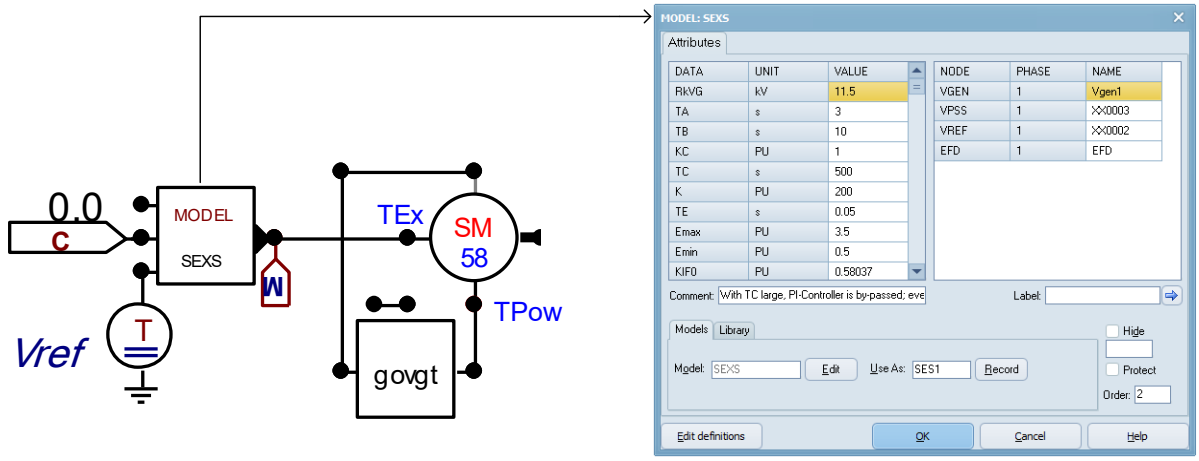
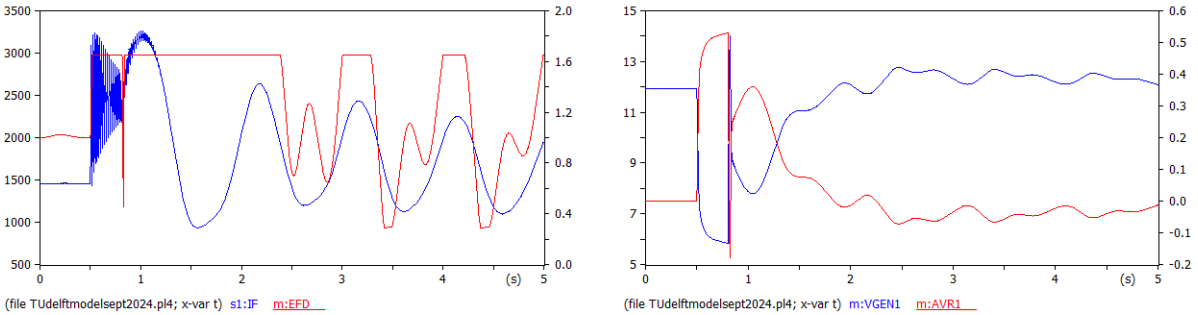


Figure 3.6: Exitation System & AVR MODEL in ATP-EMTP

The DC excitation (or field) current that produces the magnetic field inside the generator, is provided by the exciter. The excitation current and generator's terminal voltage are controlled by the automatic voltage regulator (AVR) [12]. To simulate the voltage drop at the generator's terminal, a three-phase fault is simulated. It can be observed in Figure 3.7a that the field current increase by the AVR results in an increase of the voltage at the generator's terminal. In Figure 3.7b, it can be seen how the voltage (VGEN1) is regulated by the AVR (AVR1) response.



(a) Field current-field voltage

(b) Generator terminal voltage - AVR

Figure 3.7: AVR & Excitation System

3.4.3. Governor System (TACS)

A governor system is implemented using TACS to model the turbine control actions. It responds to frequency deviations by adjusting the mechanical input power to the generator.

The governor system MODEL follows the GAST model shown in Figure 3.8. The GAST gas turbine governor model [10] represents the basic characteristics of a gas turbine driving an electrical generator connected to the bulk power system. The GAST model uses rotor speed as the governor input signal and the load reference, defined as the shaft mechanical power (Pm) is the output signal.

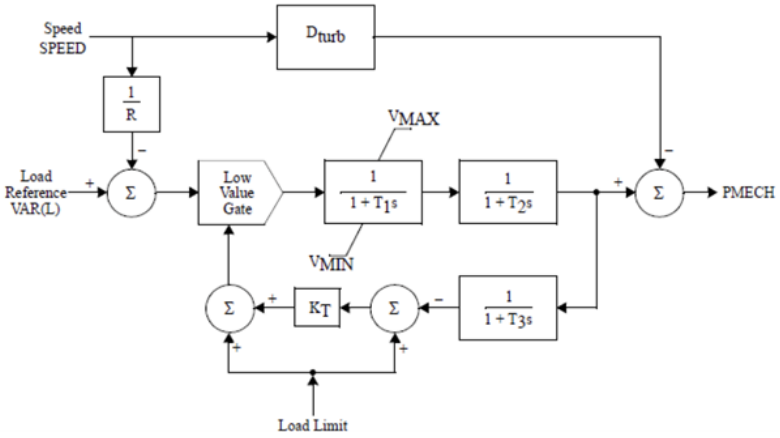


Figure 3.8: GAST MODEL [10]

The GAST model parameters are explained in Table 3.5.

Parameter	Unit	Description
T1	s	governor time constant
T2	s	combustion chamber time constant
T3	s	load limit time constant (exhaust gas measurement time)
KT	-	load limit feedback gain
R	%	droop; reciprocal of the proportional gain (e.g., R = 0.05 pu is Kp = 20)
Dturb	-	speed damping coefficient of gas turbine rotor
Vmax	pu	operational control high limit on fuel valve opening
Vmin	pu	low output control limit on fuel valve opening

Table 3.5: Governor System Parameters

The implementation of the governor system using TACS language in ATP-EMTP is presented in Figure 3.9.

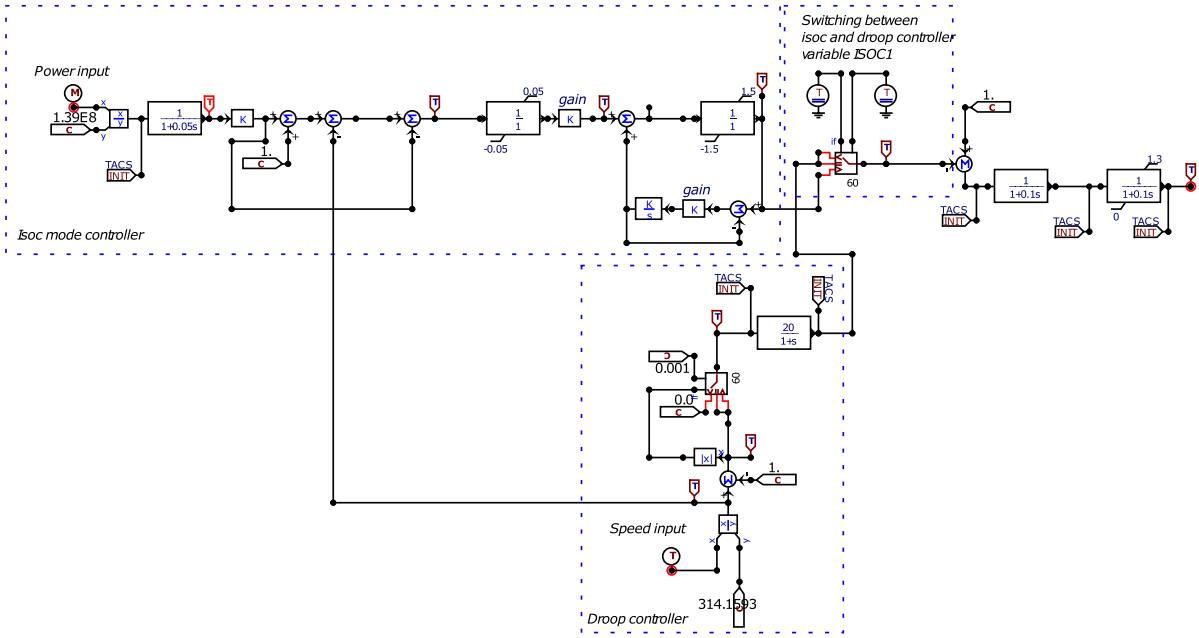


Figure 3.9: Governor Model with TACS

In Figure 3.10, the working principle of the governor system is presented by simulating a three-phase fault: the governor adjusts the mechanical power (Pm1 - blue line) based on the speed deviation from synchronous speed (VEL1 - red line).

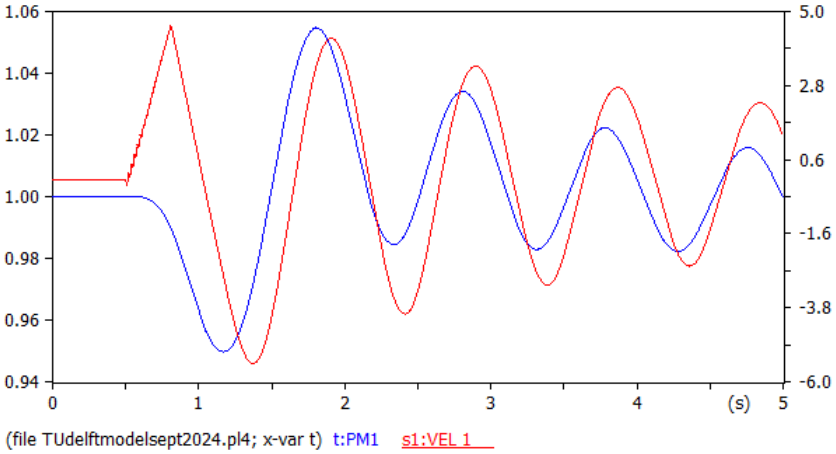


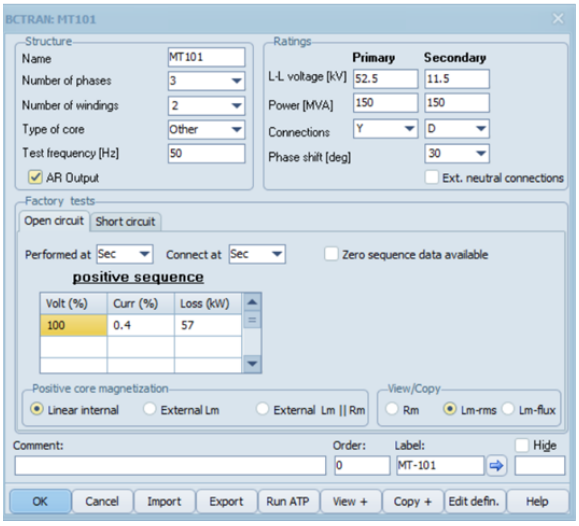
Figure 3.10: Governor Working Principle

3.4.4. Transformers (BCTRAN and SATTRAFO)

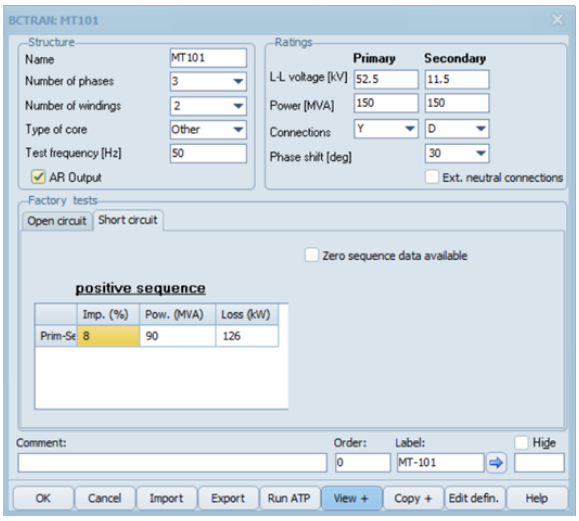
Two types of transformers are used:

- **BCTRAN**: Linear model for steady-state and normal operation.
- **SATTRAFO**: Nonlinear model capturing core saturation during fault transients.

The BCTRAN model is developed based on the transformer factory test data for open circuit - Figure 3.11a and short circuit - Figure 3.11b.



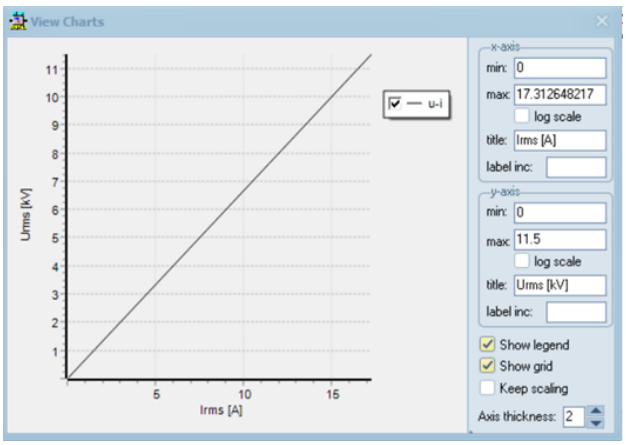
(a) BCTRAN Open circuit



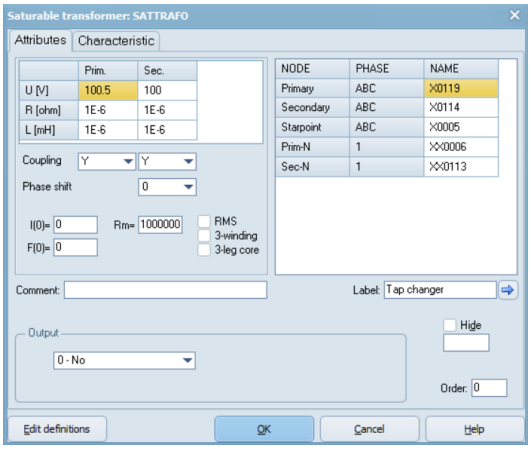
(b) BCTRAN Short circuit

Figure 3.11: MT-101 unit transformer BCTRAN model

The voltage-current characteristic is also provided by the BCTRAN model and can be seen in Figure 3.12a. The SATTRAFO MODEL that can be seen in Figure 3.12b, is used as a tap-changer mechanism located on the primary side of the three-winding transformers at the PCC and two-winding transformers at the outgoing feeders towards the LV Substation.



(a) BCTRAN V-I Curve

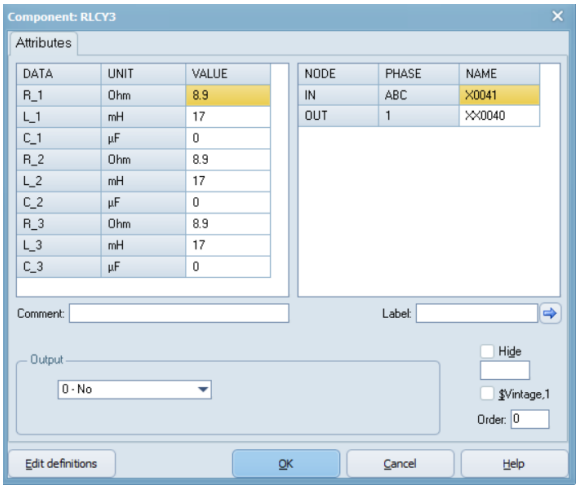


(b) SATTRAFO - Tap Changer

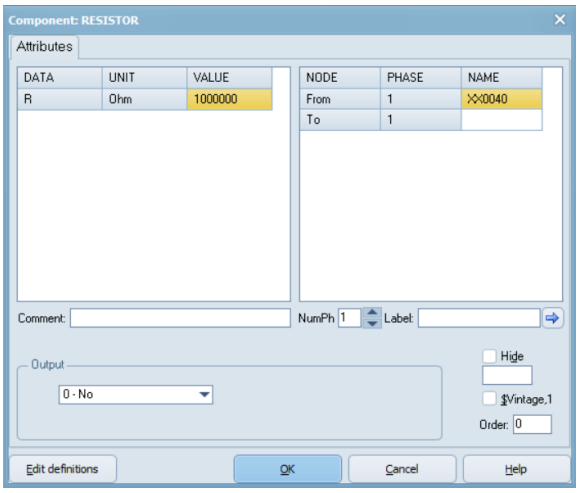
Figure 3.12: Transformer Models

3.4.5. Aggregated Load

Static Load: Modeled using the RLC3Y block in series with a resistive element, as per Figure 3.13.



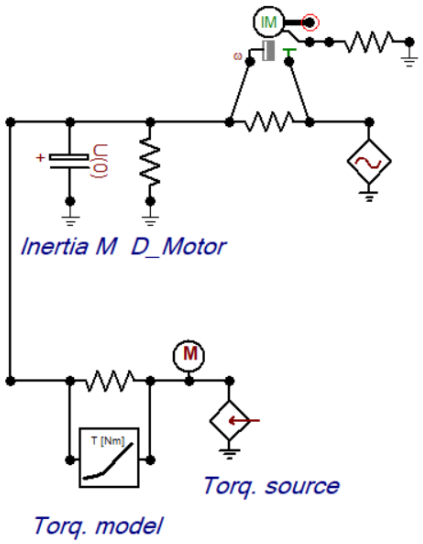
(a) RLC branch 3-phase, Y-coupling



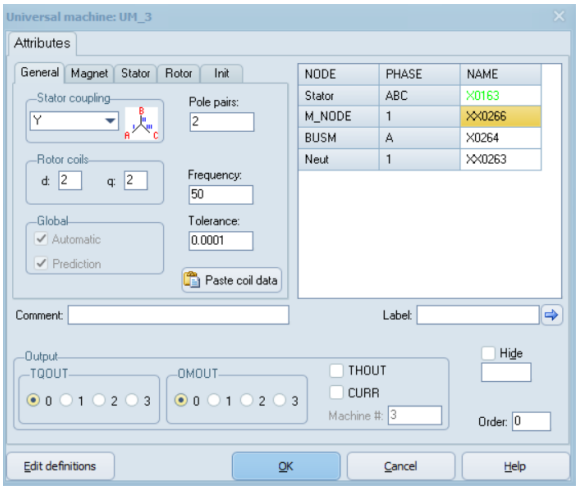
(b) Resistor

Figure 3.13: Static Load Model

Dynamic Load: the 3-phase AC induction machine (cage rotor) is modeled using the Universal Machine model (UM-3), as shown in Figure 3.14. The UM-3 module does not have a built-in model for the mechanical part, so the mechanical system is converted into an equivalent electrical network with lumped parameters [13], as per subfigure 3.14a. The electromagnetic torque appears as a current source in this network, which is treated by the ATP as part of the overall network. Subfigure 3.14b shows the electrical part of the machine which includes the stator and the rotor.



(a) SLD of Induction Motor in ATPDraw



(b) Universal Machine MODEL

Figure 3.14: Dynamic Load Model

The following rules were used for creating the equivalent mechanical network:

- For each mass of the shaft (one in this case), a node is created in the equivalent network with a capacitor to ground to represent the moment of inertia.
- To represent the mechanical torque acting on the mass, a current source is connected to the corresponding mass node.
- A resistor is located in parallel with the corresponding capacitor to include damping proportional to speed on the mass.

The electrical parameters are introduced as per the technical specifications extracted from the data sheet. For the stator, the resistance and inductance are specified in Park transformed quantities (d- q- and 0- system). For the rotor, the resistances and leakage inductances for each coil are specified.

3.4.6. Transmission Lines and Branches

Transmission lines are modeled using the LINEPI3S block, which represents a distributed PI-section line. The MODEL can be seen in Figure 3.15. The PI model can be used while the events are 50Hz related.

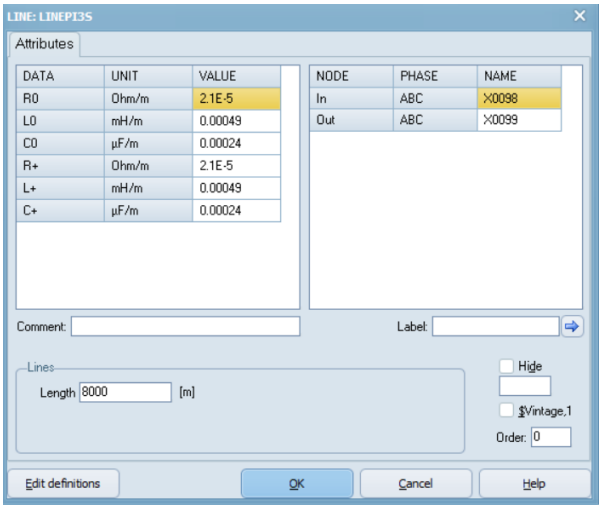
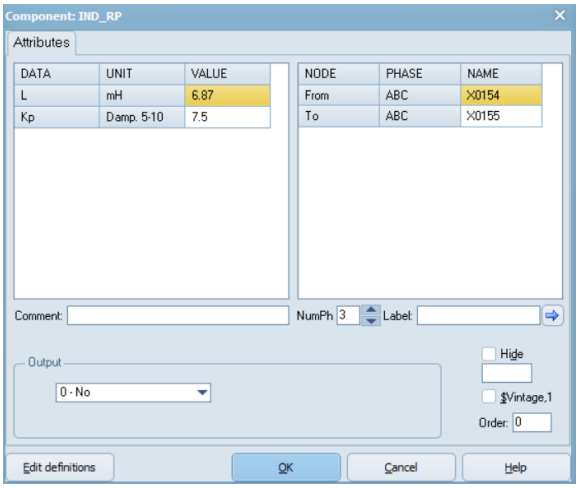


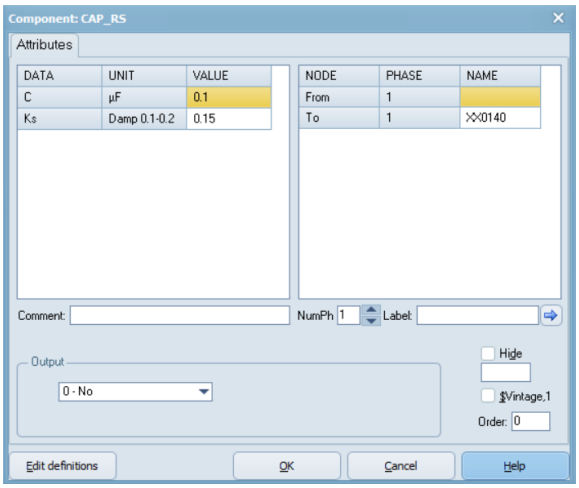
Figure 3.15: Line Model

Additional branch component models include:

- **IND-RP**: Series inductor with parallel resistance as per Figure 3.16a.
- **CAP-RS**: Shunt capacitor as per Figure 3.16b.



(a) Series inductor with resistance



(b) Shunt Capacitor

Figure 3.16: Branch Models

3.4.7. Utility Grid Connection

The utility grid is modeled using an AC source configured as a swing bus, representing a stiff voltage source for frequency reference and infinite inertia.

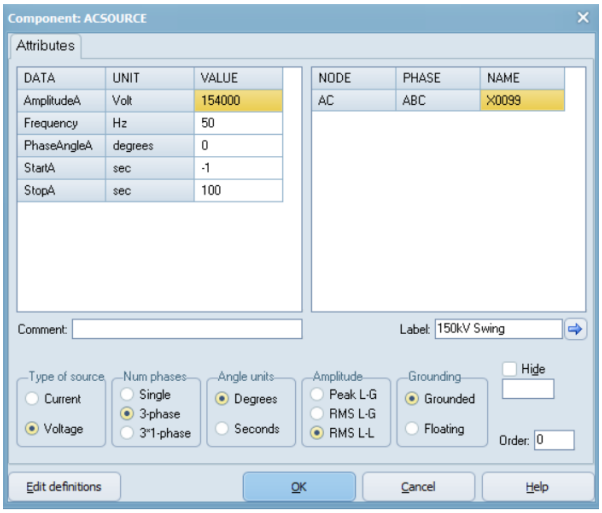


Figure 3.17: Utility Grid

3.5. Fault Modeling and Simulation Scenarios

Faults are modeled via controlled switches by introducing a fault impedance or a zero-impedance path. The following types of faults are considered:

- Three-phase to ground (3LG)
- Two-phase to ground (2LG)
- Single line-to-ground (1LG)

Each fault is applied at a specific bus or transmission line segment, with variation in clearing times to analyze the system response. The Critical Clearing Time (CCT) is determined by incrementally increasing the duration of the fault until instability occurs.

3.6. Measurement and Monitoring Systems

In ATP-EMTP several components are used to monitor the system's dynamic behavior as explained below.

VMETER Block: The VMETER provides measurements of:

- Voltage magnitude (Vgen)
- Frequency
- Electrical angle
- ROCOF (Rate of Change of Frequency)

PQ Measurement Block: Active and reactive power are calculated using a PQ block that takes inputs of voltage and current and outputs instantaneous power flow.

Butterworth low and high pass filters:

Separate components for analogue filtering are available in ATPDraw tollbox. These are 3-phase Butterworth low and high pass filters of selectable order 1 to 3. A low-pass filter is used for anti-aliasing, with a filter frequency less than the half of sampling frequency. The high-pass filter can be used to

remove sub-harmonics. In both components the user sets a Gain, filter frequency FilterFreq, an order (1-3) FilterOrder, and a frequency for amplitude correction ScaleFreq [8].

abc-to-rms Conversion Block: To simplify analysis, abc voltage signals are converted to their RMS equivalents, using a peak detector or moving window method.

3.7. Simulation Setup

- Time step: 50 µs
- Total simulation time: 2–5 seconds
- Outputs: Voltage, current, angle, frequency, power

4

Stability Analysis

This chapter evaluates the dynamic behavior of the power system under different fault conditions, with a focus on assessing system stability and determining the Critical Clearing Time (CCT). The study involves simulating large disturbances, specifically three-phase to ground (3LG), double-line to ground (2LG), and single line-to-ground (1LG) faults, and analyzing the system response before, during, and after each disturbance. Key parameters such as rotor angle, generator voltage, frequency, rate of change of frequency (RoCoF), and speed deviation from synchronous speed are monitored to evaluate the system's stability margins.

The primary goal is to understand how the system reacts to network disturbances, determine the maximum allowed fault-clearing time before instability occurs (CCT), and ultimately use these findings to develop a reliable island tripping scheme.

4.1. Test Scenarios and Simulation Parameters

Three different loading scenarios are considered, representing 100%, 75%, and 50% of the rated active power output. These are summarized in Table 4.1. While the voltage is maintained constant across scenarios through transformer tap adjustments, the active power output is varied by adjusting the generator rotor angle. This setup allows analysis of system response under varying load conditions.

Scenario	P (MW)	Q (MVAR)	Voltage and Angle Settings
Scenario 1	110	30	$V_{\text{LL}} = 1.038V_n$, $V_{\text{L-G}} = 9750V$, ANG $= -22°$
Scenario 2	90	30	$V_{\text{LL}} = 1.038V_n$, $V_{\text{L-G}} = 9750V$, ANG $= -24.7°$
Scenario 3	60	30	$V_{\text{LL}} = 1.038V_n$, $V_{\text{L-G}} = 9750V$, ANG $= -28.5°$

Table 4.1: Stability Analysis for Three Independent Load Scenarios

Simulation settings:

- Total simulation time: $T_{\text{max}} = 5$ s
- Fault initiation time: $T_{\text{start-fault}} = 0.5$ s
- Time step: $\Delta T = 5 \times 10^{-5}$ s

4.1.1. Fault locations

To assess angle stability and determine the CCT, three types of faults (3LG, 2LG, and 1LG) are applied at four critical locations, as provided in Figure 4.1. These fault simulations are conducted for each of the three scenarios listed in Table 4.1.

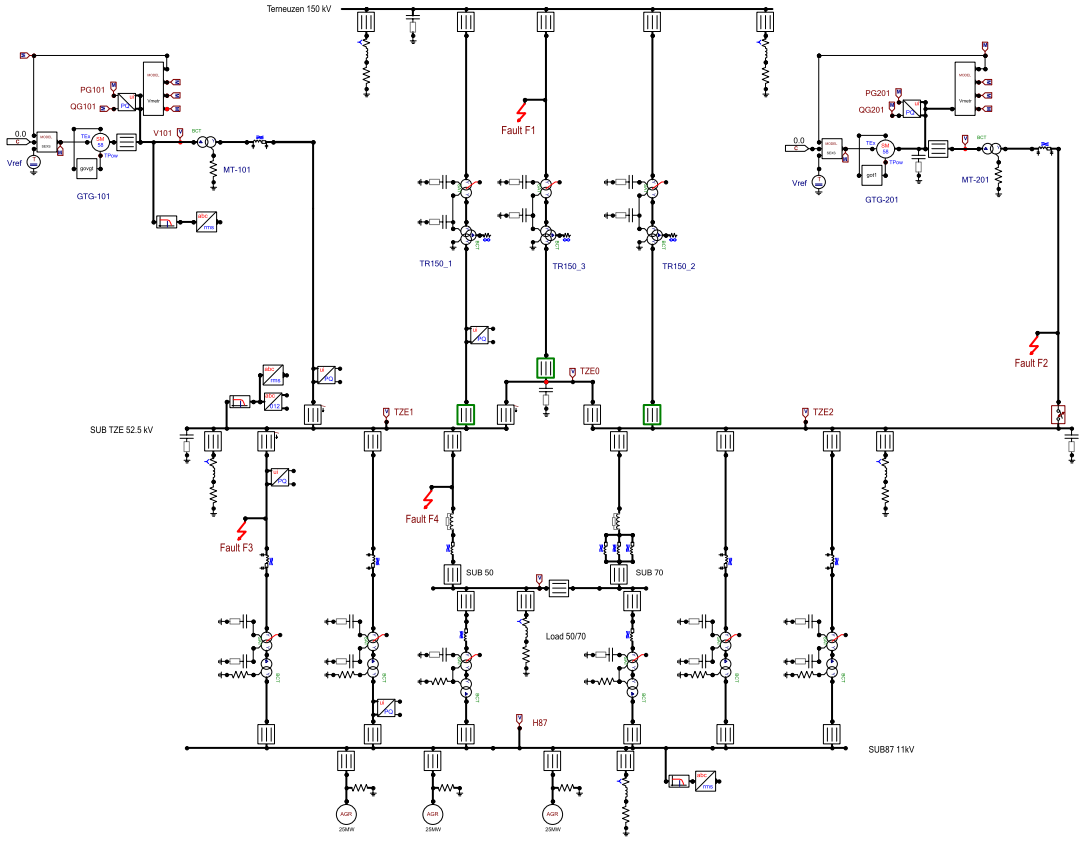


Figure 4.1: Fault locations as per ATP-EMTP SLD of DOW industrial network

Fault	Location Description
F1	Utility grid connection
F2	GTG-201 (one of the two synchronous generators operating in parallel)
F3	Outgoing feeder to LV-XFM
F4	Outgoing feeder to Substation 50

Table 4.2: Fault Location Description

4.2. Determining the Critical Clearing Time (CCT)

The point at which the system loses synchronism is identified by gradually increasing the fault clearing time. This time value represents the critical clearing time (CCT) of the system for the given scenario and fault location. This analysis is conducted for three fault types: three-phase to ground (3LG), double-line to ground (2LG), and single line-to-ground (1LG), across all three load scenarios (S1, S2, and S3) per Table 4.1 and at four different fault locations (F1, F2, F3, F4), as per Figure 4.1.

Three stability criteria are evaluated for each case: rotor angle stability, voltage stability, and frequency stability. The maximum allowed variation ranges of voltage and frequency, according to the generator data sheet, are provided in Table 4.3.

Parameter	
Voltage variation range	± 10 %
Frequency variation range	$-4/+2$ %
Maximum combined variation (voltage / frequency)	$+10$ %

Table 4.3: Voltage and Frequency Variation Ranges

4.2.1. Three-phase fault (3LG)

Rotor Angle Stability: Figures 4.2, and 4.3 show the evolution of rotor angles under a 3LG fault, at the four locations F1-F4 and for all three independent scenarios (S1, S2, S3).

It can be observed that when the fault is cleared quickly the rotor angles of the machines oscillate but remain within synchronism and the system settles into a new equilibrium point. If the fault lasts too long, due to the accelerating energy the rotor angles exceed the critical angle (δmax), at which point synchronism is lost and the machines can no longer remain in step.

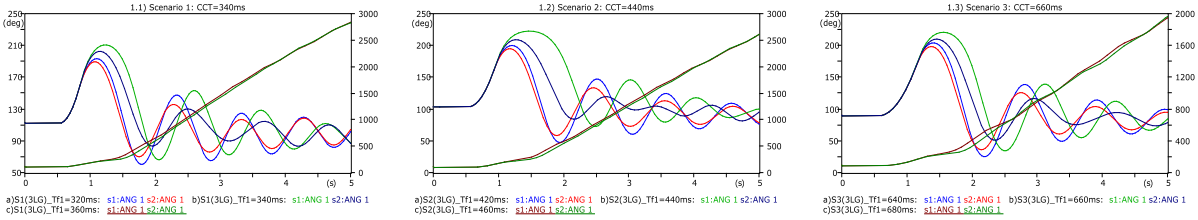


Figure 4.2: Fault location F1: CCT-S1=340ms, CCT-S2=440ms, CCT-S3=660ms

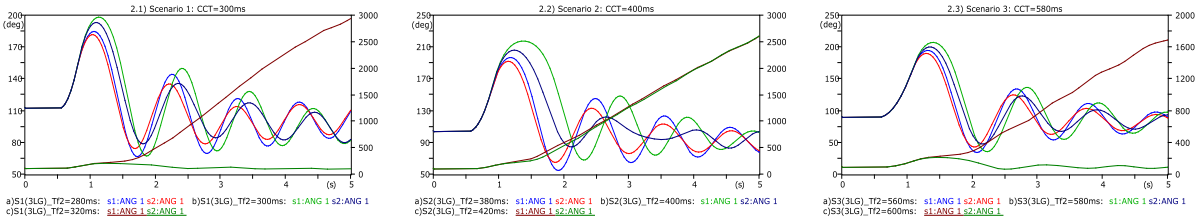


Figure 4.3: Fault locations F2-F4: CCT-S1=300ms, CCT-S2=400ms, CCT-S3=580

Voltage & Frequency Stability: Figures 4.4, 4.5, 4.6, 4.7 and 4.8 show the voltage and frequency dynamics under a 3LG fault, at the four locations F1-F4 and for all three independent scenarios (S1, S2, S3).

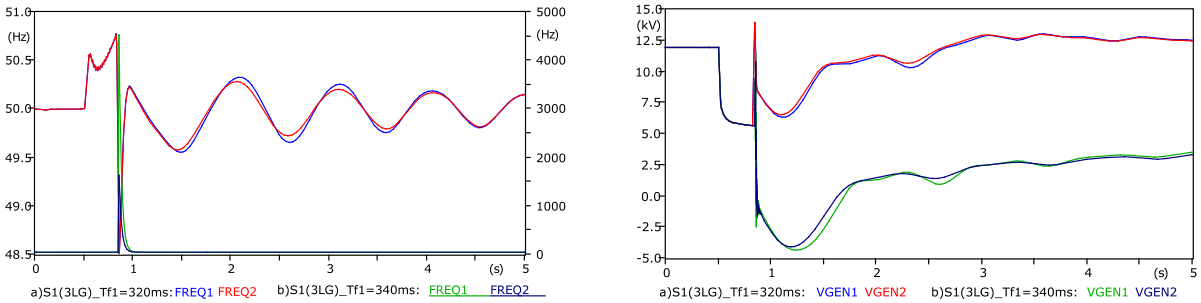


Figure 4.4: Scenario 1 - Fault location F1: CCT = 320 ms

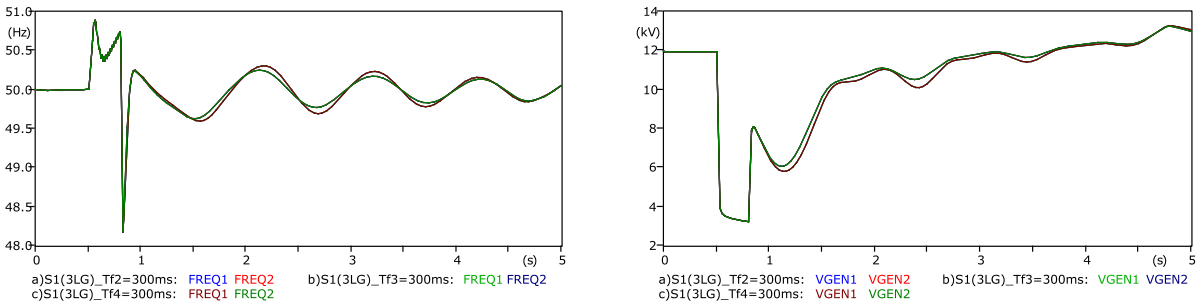


Figure 4.5: Scenario 1 - Fault location F2-F4: CCT = 300 ms

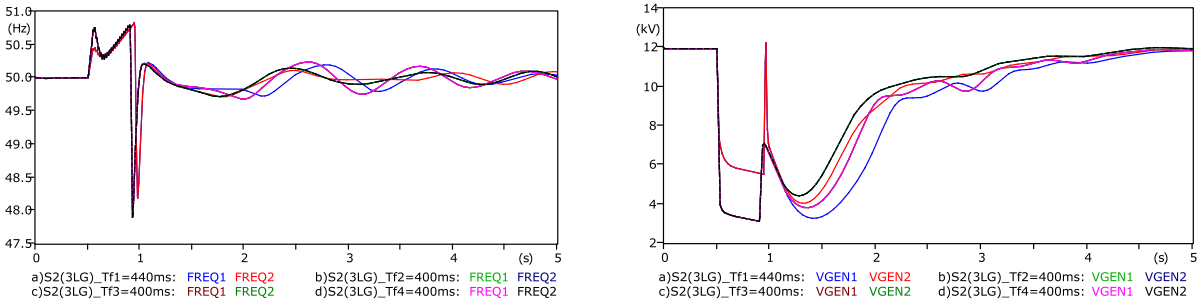


Figure 4.6: Scenario 2 - Fault location F1: CCT = 440 ms, Fault location F2-F4: CCT = 400 ms

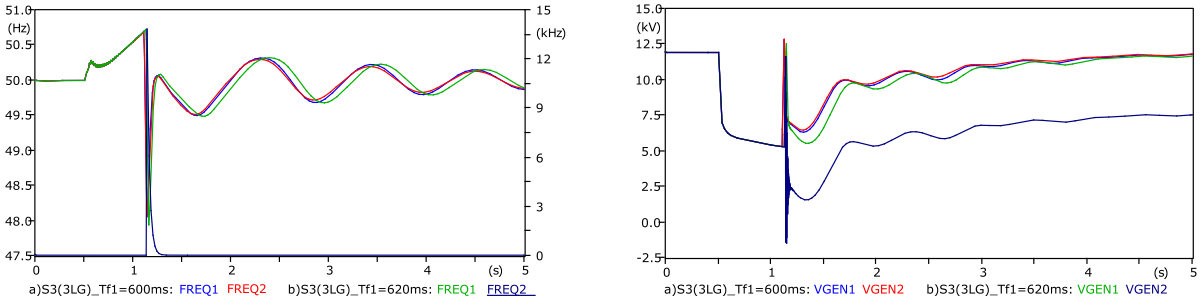


Figure 4.7: Scenario 3 - Fault location F1: CCT = 600 ms

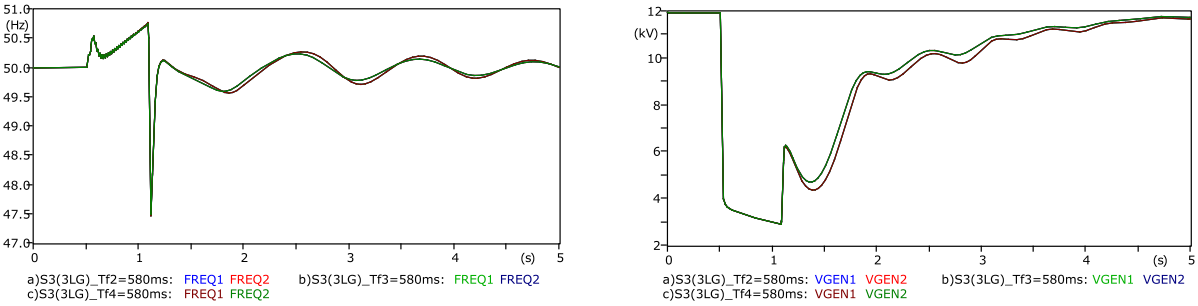


Figure 4.8: Scenario 3 - Fault location F2-F4: CCT = 580 ms

The stability analysis results for a three-phase fault are provided in Table 4.4.

Scenario	Fault Type	Fault Location	CCT (ms)
Scenario 1	3LG	F1	320
Scenario 1	3LG	F2	300
Scenario 1	3LG	F3	300
Scenario 1	3LG	F4	300
Scenario 2	3LG	F1	440
Scenario 2	3LG	F2	400
Scenario 2	3LG	F3	400
Scenario 2	3LG	F4	400
Scenario 3	3LG	F1	600
Scenario 3	3LG	F2	580
Scenario 3	3LG	F3	580
Scenario 3	3LG	F4	580

Table 4.4: Critical Clearing Time (CCT) of a Three-Phase Fault

For fault location F1 in Scenarios 1 and 3, the rotor angles continue to exhibit oscillatory motion until 340 ms and 660 ms, respectively. However, when voltage and frequency stability are also considered, both signals exceed the maximum allowable variation ranges (Table 4.3) by that time. The CCT based on voltage and frequency criteria - 320 ms for Scenario 1 and 600 ms for Scenario 3 - is shorter than the CCT derived from rotor-angle stability alone.

4.2.2. Two-phase fault (2LG)

Rotor Angle Stability: Figures 4.9 and 4.10 show the rotor angles evolution under a 2LG fault, at all four locations F1-F4 and for all three independent scenarios (S1, S2, S3).

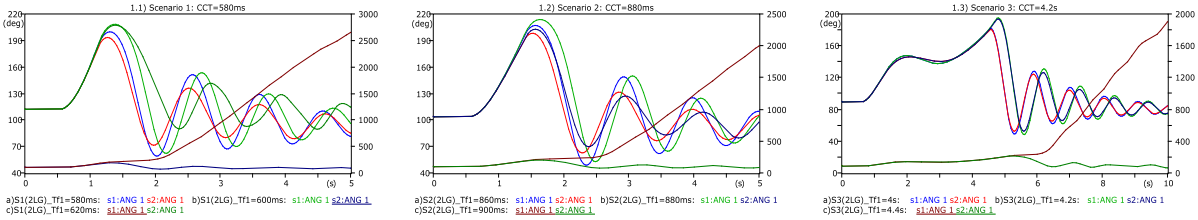


Figure 4.9: Fault location F1: CCT-S1 = 580 ms, CCT-S2 = 880 ms, CCT-S3 = 4200 ms

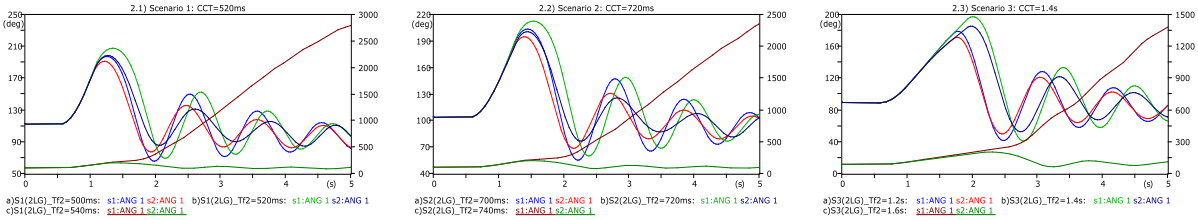


Figure 4.10: Fault locations F2-F4: CCT-S1 = 520 ms, CCT-S2 = 720 ms, CCT-S3 = 1400 ms

Voltage & Frequency Stability: Figures 4.11, 4.12, 4.13 and 4.14 show the voltage and frequency dynamics under a 2LG fault, at the four locations F1-F4 and for all three independent scenarios (S1, S2, S3).

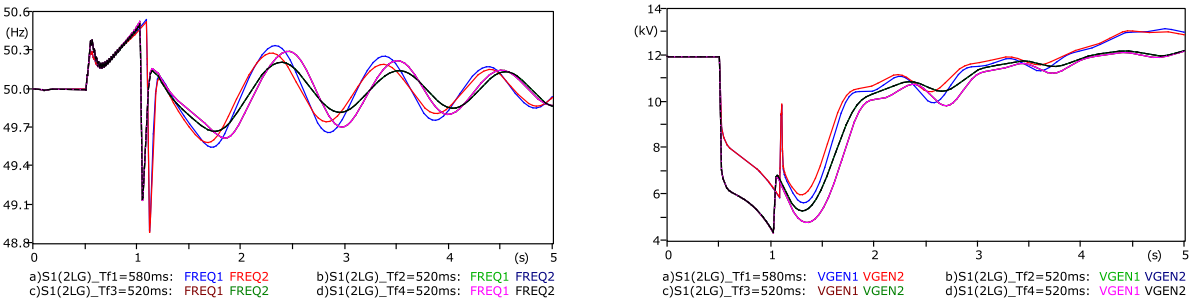


Figure 4.11: Scenario 1 - Fault location F1: CCT = 580 ms, F2-4: CCT = 520 ms

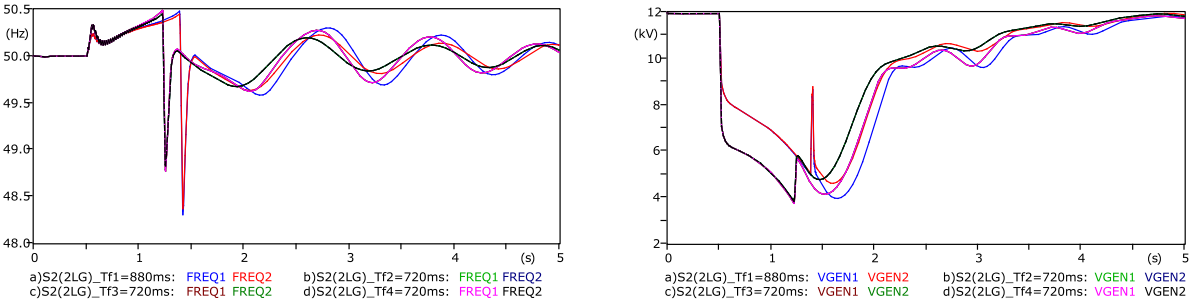


Figure 4.12: Scenario 2 - Fault location F1: CCT = 880 ms, F2-4: CCT = 720 ms

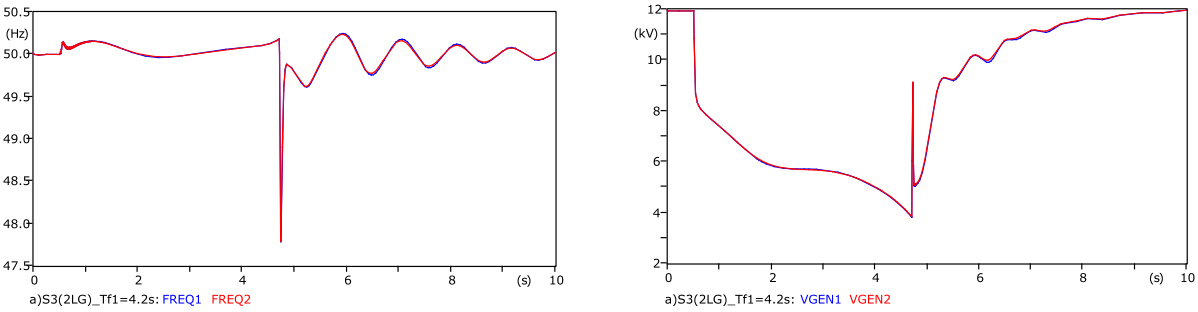


Figure 4.13: Scenario 3 - Fault location F1: CCT = 4200 ms

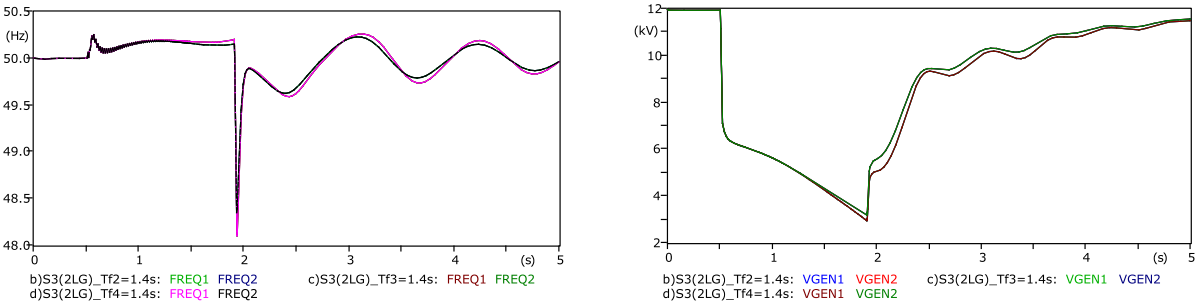


Figure 4.14: Scenario 3 - Fault location F2-4: CCT = 1400 ms

The stability analysis results for a 2LG fault are provided in Table 4.4.

Scenario	Fault Type	Fault Location	CCT (ms)
Scenario 1	2LG	F1	580
Scenario 1	2LG	F2	520
Scenario 1	2LG	F3	520
Scenario 1	2LG	F4	520
Scenario 2	2LG	F1	880
Scenario 2	2LG	F2	720
Scenario 2	2LG	F3	720
Scenario 2	2LG	F4	720
Scenario 3	2LG	F1	4200
Scenario 3	2LG	F2	1400
Scenario 3	2LG	F3	1400
Scenario 3	2LG	F4	1400

Table 4.5: Critical Clearing Time (CCT) of a Two-Phase Fault

4.2.3. Single-phase fault (1LG)

The simulation time is increased to 15 s and the fault duration to 10 s.

Rotor Angle Stability: Figures 4.15 and 4.16 show the rotor angles evolution under a 1LG fault, at all four locations F1-F4 and for all three independent scenarios (S1, S2, S3).

The left side of Figure 4.15 shows that for all three scenarios (S1, S2, S3), the rotor angles oscillate back to a point of equilibrium for a fault clearing time of 10 s. The duration of the fault is increased to 20 s for the most critical scenario (S1) and the simulation runs for 30 s. The right side of Figure 4.15 shows that the system is still able to recover after a 20 s fault duration.

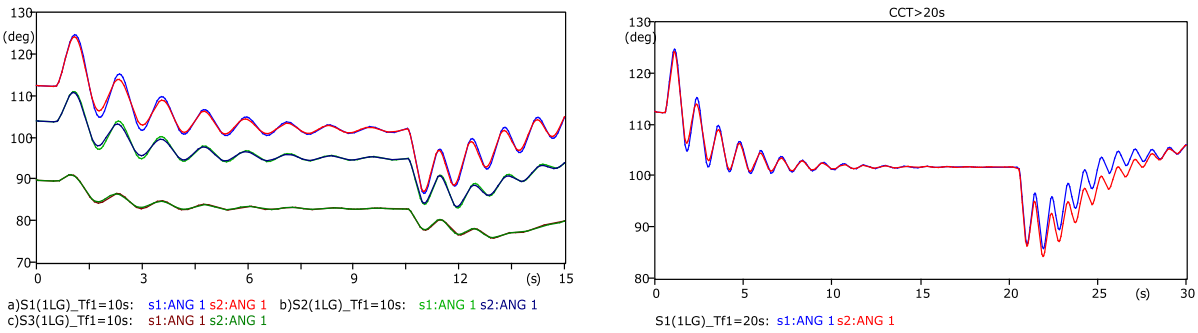


Figure 4.15: Scenario 1-3 - Fault location F1: CCT > 10 s

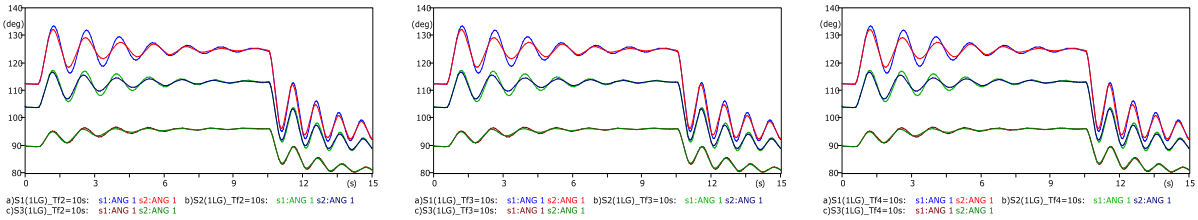


Figure 4.16: Scenario 1-3 - Fault location F2-4: CCT > 10 s

Voltage & Frequency Stability: Figure 4.17 shows the voltage and frequency dynamics under a 1LG fault, at the four locations F1-F4 and for all three independent scenarios (S1, S2, S3).

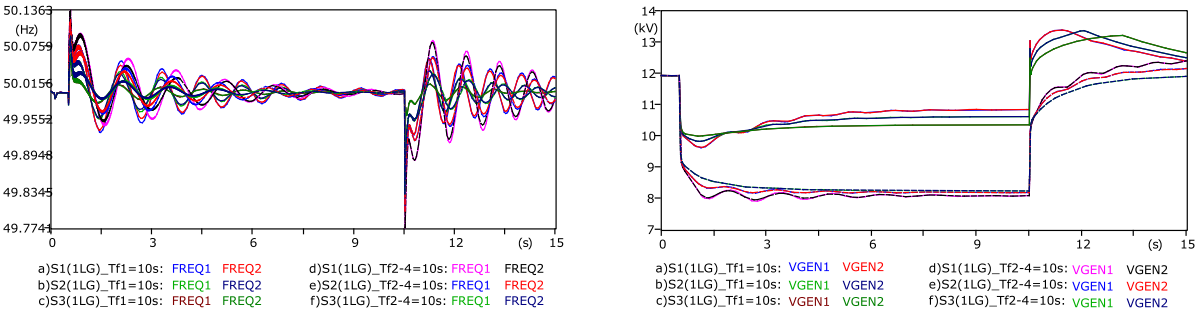


Figure 4.17: Scenario 1-3 - Fault location F1-4: CCT > 10s

4.2.4. Conclusions

In conclusion, the fault type, fault location and machine's active power output significantly influence the power system stability.

A balanced three-phase (3LG) fault is the most severe type of fault, reducing CCT more aggressively than two-phase (2LG) or single-phase (1LG) faults.

The closer the fault is to the generators, the shorter the CCT. Faults at locations F2, F3 and F4 (near the generators) yield lower CCTs, while the most distant fault (location F1) produces the highest CCT.

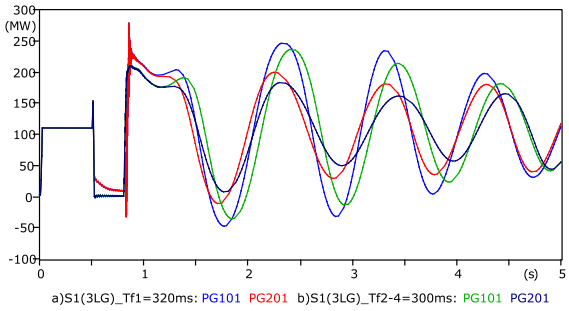
The CCT decreases as system load increases. Scenario 1 (100% rated load) exhibits the shortest CCT of 300 ms, whereas Scenario 3 (50% rated load) remains stable up to 580 ms for the same fault type and location.

The phase-to-ground fault gives the same results for different fault locations and under different load scenarios. It can be concluded that this type of fault is the least critical, due to the system's ability to maintain synchronism even with an increased fault duration of 20 s.

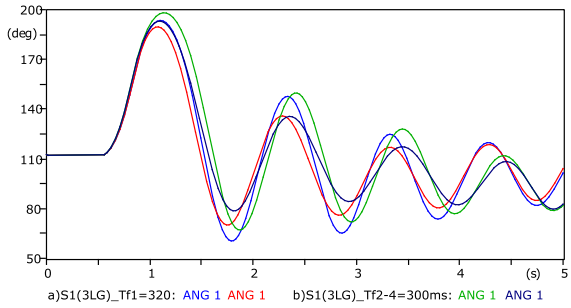
4.3. Machine Dynamics and Control Response

With the most critical fault type (3LG) and load scenario (S1) identified, this section analyzes how machine dynamics and control systems influence power-system stability.

The Power-Angle relationship provided in Figure 4.18 shows that during the fault, the sudden loss of load causes an excess of electrical power generation, so the surplus energy is stored as kinetic energy causing the rotor to accelerate/ overspeed. Figure 4.19 shows that the governor system responds to the resulting speed deviation from synchronous speed by decreasing the mechanical power input to dissipate the excess kinetic energy and restore balance. Due to inertia, the rotor angle oscillates back and forth around the new equilibrium point, as seen in Figure 4.18b.

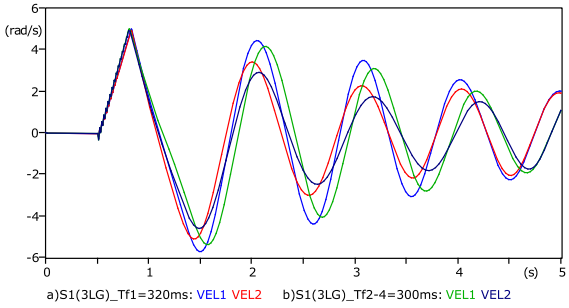


(a) Active Power Generation

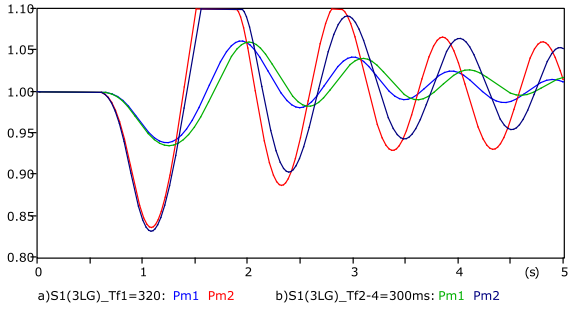


(b) Rotor Angle oscillations

Figure 4.18: Power-Angle Relationship



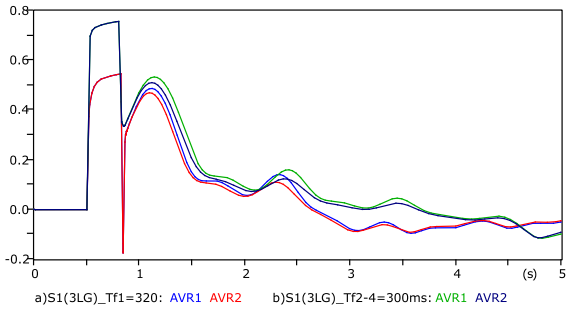
(a) Speed Deviation from Synchronous Speed



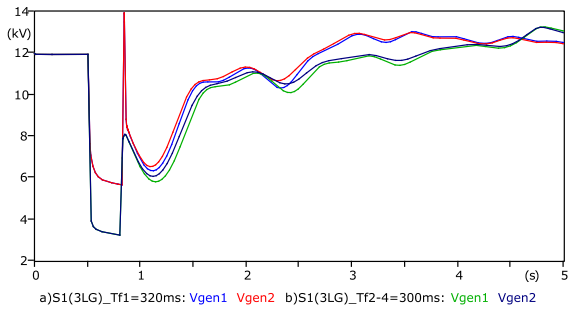
(b) Mechanical Power Input

Figure 4.19: Governor System Response

Figure 4.20 shows the excitation system response: the Automatic Voltage Regulator (AVR) continually monitors the generator's terminal voltage against its setpoint and adjusts the DC field current (increasing it when voltage falls below the reference and decreasing it when it rises above), thereby altering the internal EMF to drive the terminal voltage back to its desired value.



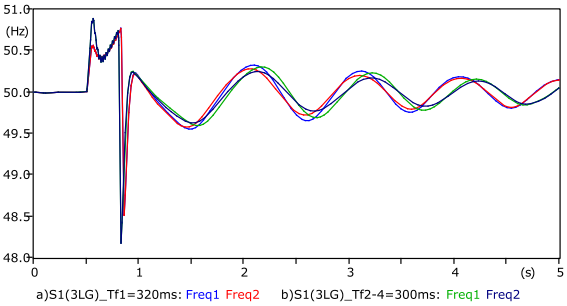
(a) Automatic Voltage Regulator



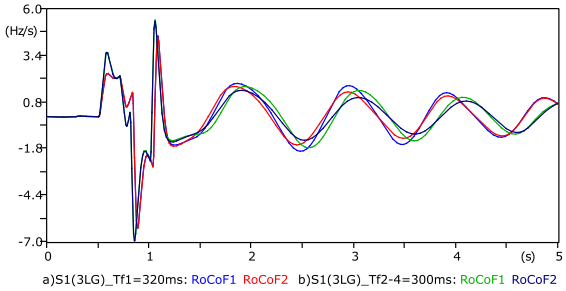
(b) Generated Voltage

Figure 4.20: Excitation System Response

During the fault, the rotor acceleration increases the system frequency above 50.5 Hz as shown in Figure 4.21. After the AVR and governor system overcome their inherent time delays, the AVR boosts field current while the governor reduces mechanical input, causing the frequency to oscillate between 50.2 and 50.5 Hz as the two control loops interact. When the fault clears, the switching transient and sudden return of load produce a sharp frequency dip below 50 Hz. Then the excitation and governor systems work together to rebalance voltage and power, resulting in only small, decaying oscillations around the nominal frequency until steady-state is restored.



(a) Frequency



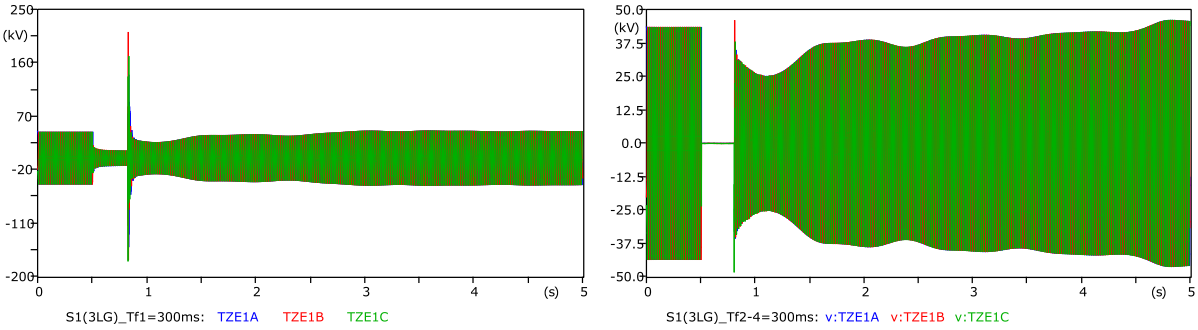
(b) Rate of Change of Frequency

Figure 4.21: Frequency Stability

4.4. System-Level Stability at MV Busbar

The system-level impact of fault location is evaluated by monitoring parameters at the MV substation referred to as SUBTZE. Scenario 1 and 3LG faults are simulated for all four locations. The voltage at the MV busbar and the currents through feeders to the LV transformer (LV-XFM) and Substation SUB50 are plotted.

The change in voltage measured at the MV busbar can be seen in Figure 4.22. Depending on the fault location, the busbar voltage either drops or entirely collapses. External faults, further from the busbar, cause the voltage to drop significantly, as can be seen in Subfigure 4.22a , while internal faults (fault locations F2-4) cause the voltage to collapse to zero, as per Subfigure 4.22b.

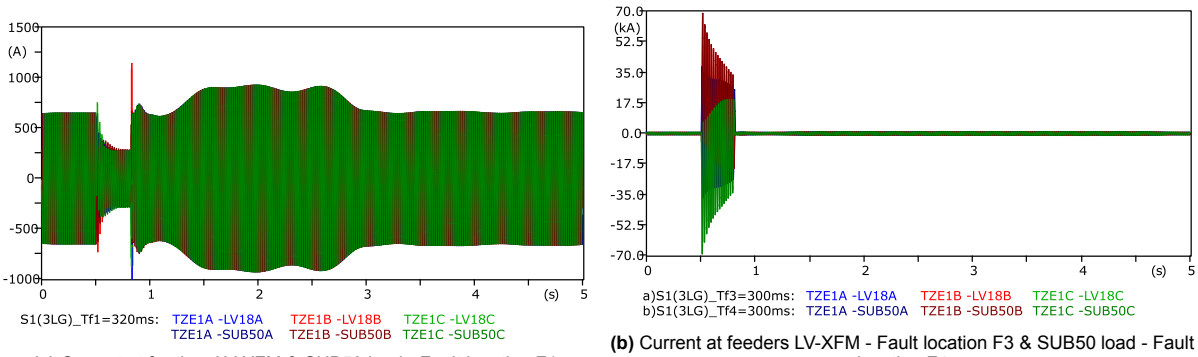


(a) Fault location F1

(b) Fault location F2-4

Figure 4.22: Voltage measured at the MV busbar during a 3LG fault

The currents measured at the outgoing feeders are provided in Figure 4.23. It can be seen that a fault at the utility side creates an undercurrent condition at the outgoing feeders as per Subfigure 4.23a, this is due to the increase in the system's impedance when losing the strong support of the grid. During internal faults, a high short-circuit current can be seen at the faulted feeder, as per Subfigure 4.23.

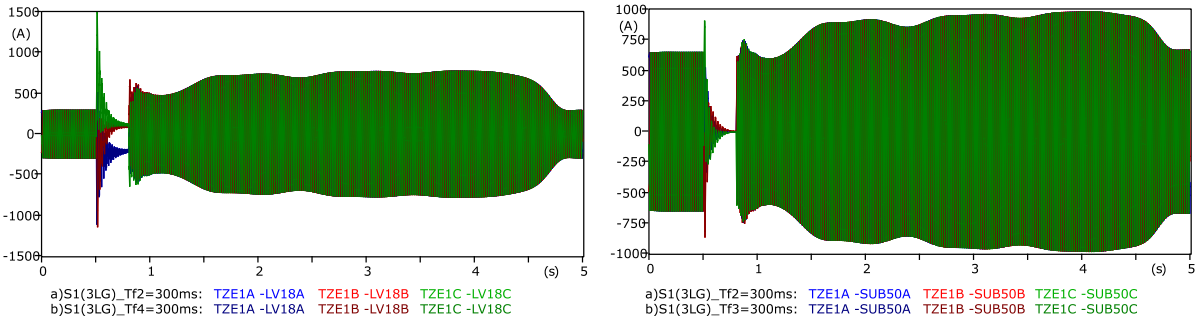


(a) Current at feeders LV-XFM & SUB50 load - Fault location F1

(b) Current at feeders LV-XFM - Fault location F3 & SUB50 load - Fault location F4

Figure 4.23: Currents measured at the outgoing feeders during a 3LG fault

Figure 4.24 shows the currents of the two non-faulted outgoing feeders during an internal fault. As the MV bus voltage collapses to zero during the fault, the currents also drop close to zero, recovering after the fault is cleared.



(a) Current at outgoing feeder LV-XFM - Fault location F2 & F4

(b) Current at feeder SUB50 load - Fault location F2 & F3

Figure 4.24: Currents measured at non-faulted feeders for an internal fault

In conclusion, at the MV busbar an internal three-phase-to-ground (3LG) fault causes the bus voltage to drop to zero. The faulted feeder carries high short-circuit current, while the current of the non-faulted feeder drops with the bus voltage. For an external 3LG fault on the HV side of the three-winding transformer (fault location F1), a similar voltage-current reduction is observed. Due to the fault location, the transformer's leakage impedance limits the fault current transferred to the MV side, so the voltage at the MV busbar does not fully collapse.

4.5. Conclusion

The Stability Analysis shows that the critical clearing time (CCT) is strongly influenced by generator loading, fault type, and fault location. A reduction of the generator active power output increases the CCT by approximately a factor of 1.5. The most severe condition is identified when a three-phase-to-ground fault is applied closest to the generators, where the CCT is as low as 300 ms. The system stability depends on whether the rotor angle remains within the critical angle and if this limit is exceeded, the machines lose synchronism with the rest of the system.

The dynamic response of the machine's control systems helps to restore equilibrium after disturbances. The turbine governor regulates mechanical power input based on rotor speed deviations, reducing the mechanical input during acceleration and increasing it during deceleration. This helps to reduce frequency deviations. In parallel, the Excitation System and Automatic Voltage Regulator (AVR) maintain the generator terminal voltage by adjusting the field current. By increasing the excitation current, the AVR increases the internal EMF of the machine, which raises the synchronizing power and the restoring torque acting on the rotor, improving transient stability margins.

Finally, the MV busbar analysis shows that internal faults near the substation cause a full voltage collapse, with the faulted feeder carrying a high short-circuit current. External faults can be identified by partial voltage collapse, as well as the absence of overcurrent at outgoing feeders. These differences will be used for the design of the islanding tripping scheme.

5

Protection Study

In this chapter, an islanding tripping scheme is developed using the ATP-EMTP software. The protection functions are chosen based on the Literature Review and the results of the Stability Analysis which were discussed in Chapter 4. The protection logic is validated in ATP-EMTP by simulating the same type of fault conditions at four different locations in the power system. The expected result is that the protection logic correctly identifies an islanding condition, trips the incomer breakers to isolate the system and ensures island stability by sending load/generation-shedding signals to the distributed control system (DCS).

First, the Dutch NetCode requirements must be considered when developing the islanding tripping scheme. Then the functions used for the scheme are modeled according to the 7UM85 Siemens manual to replicate the relay behavior as accurately as possible. Then, the scheme is validated by being tested for all fault locations and types of faults previously discussed in Chapter 4.

5.1. Dutch NetCode Requirements

The Dutch Netcode (Netcode Elektriciteit) [16] specifies the frequency range within which generators must stay connected and defines trip settings outside that range.

Normal and Extreme Frequency Bands:

If grid frequency moves beyond 47.5 Hz or above 51.5 Hz, generators will be disconnected to protect equipment and grid stability. In practice, protection relays operate when the frequency drops below 47.5 Hz or rises above 51.5 Hz.

Rate of Change of Frequency (RoCoF) Limits:

The Netcode defines df/dt (RoCoF) withstand capability requirements to ensure generators do not falsely trip during rapid frequency changes (for instance, after major faults). The limits and their implications are as explained below.

RoCoF Thresholds: Generators must endure fast frequency changes up to certain rates without disconnecting. For synchronous generators (e.g. large conventional units), the required withstand is 1 Hz per second (measured over 500 ms window).

The code allows the RoCoF setting for a synchronous unit to be made more conservative (lower than 1 Hz/s) in consultation with the grid operator. This means when a particular generator or local grid condition warrants it, the trip setting can be set to detect smaller df/dt (for islanding protection, for example) only with operator agreement. However, by default, generators must at least handle the above rates.

Implications: These RoCoF limits ensure that generators remain connected during typical grid disturbances. They prevent generators from tripping on small disturbances, thus improving overall grid

stability. Only exceptionally high RoCoF events (exceeding 1 or 2 Hz/s as applicable) would allow generators to disconnect, which corresponds to very severe grid conditions.

Frequency Stability and Response Requirements

Beyond just staying connected, generators must actively support frequency stability. The Dutch Netcode(aligned with EU network codes) imposes requirements for frequency control capabilities and other stability related features. Notably, Article 3.13 (lids 1–6) [16] details:

Frequency Response Capability – Overfrequency (LFSM-O): Generators must automatically reduce the output when system frequency exceeds nominal frequency. The Netcode requires an overfrequency droop control (Limited Frequency Sensitive Mode – Overfrequency) with the following settings: a threshold frequency between 50.2 Hz and 50.5 Hz (default set at 50.2 Hz) at which the response begins, and a droop (static) adjustable between 4% and 12% (default 5%). In practice, this means when frequency exceeds 50.2 Hz, the generator will start decreasing its active power output proportionally with the frequency increase, helping to arrest overfrequency conditions. The generator should continue to run at its minimum output (and not shut down) if that minimum is reached.

Continuous Primary Control: For the largest units, the Netcode mandates full Frequency Sensitive Mode (FSM) around 50 Hz. Type C and D generators must be capable of continuously adjusting power with small frequency deviations (not just in emergency thresholds). The code specifies parameters for this FSM: a narrow deadband (insensitivity) around 50 Hz (default ±10 mHz, adjustable up to 500 mHz) and a droop setting in the range 4–12% (5% default). They must be able to modulate at least 1.5% to 10% of their output in response to frequency changes as part of normal operation. This means high inertia or high capacity plants will continuously help fine tune system frequency, not only during large excursions but also during small fluctuations.

Industrial Process Exception: A special provision (Article 3.13 lid 3) exists for generators embedded in an industrial process where modifying the generator output would disrupt the process. In such cases, the Netcode allows Frequency Sensitive Mode (FSM) activation to be based on the net output at the connection point rather than directly changing the prime mover's setpoint. This effectively provides some flexibility in frequency response so that the industrial process is not disrupted when the grid still obtains the required frequency support from the site.

The Island Protection settings agreed with the network operator TenneT for the 50 kV MV substation Terneuzen (SUBTZE) are provided below:

1. When the voltage is lower than 30 kV the fault ride-through (FRT) is equal to 0.2 s with energy direction to 150 kV Utility Network.
2. If the frequency drops below 47.5 Hz or rises above 51.2 Hz, the FRT is equal to 100 ms.

Disconnection takes place by opening the 50 kV switches of the three 150/50 kV transformers at the PCC (point of common coupling). As soon as the ELSTA control system detects that the 50 kV substation is in island mode, the GTG-101 and GTG-201 machines are very quickly regulated with an "emergency ramp down" rate to a combined power equal to the sum of the DOW and ELSTA's own company.

5.2. Protection Settings

The protection functions chosen for the islanding tripping scheme are based on the conclusions derived from the Stability Analysis detailed in Chapter 4 and on the Literature Review. The protection functions of 7UM85 relay were modeled in ATP-EMTP as accurate as possible. The protection scheme includes Overfrequency (ANSI81O), Undervoltage (ANSI27), Rate of Change of Frequency (ANSI81R) and Vector-jump (ANSI78). These functions are described as presented in the relay manual [1].

5.2.1. Overfrequency Protection Function (ANSI81O)

The Overfrequency protection function is used to:

- Detect over frequencies in electrical power systems or machines
- Monitor the frequency band and output failure indications
- Disconnect generating units when the power frequency is critical
- Provide additional turbine protection if the speed limiter fails

An overfrequency condition can be seen when the active power generated exceeds the active power demand. This happens during load shedding (island network), power system disconnection or disturbances of the frequency controller.

The overfrequency protection function is used in protection function groups (FG) based on voltage measurements. Two functional configurations are available in the relay library, based on two different frequency measurement methods.

Angle difference method (method A): if the frequency protection stage is used for the protection of machines. The angle-difference method determines the phasor of the positive-sequence voltage in multiphase systems. Since the change of angle of the voltage phasor over a given time interval is proportional to the frequency change, the current frequency can be derived from it.

Filtering method (method B): if the frequency protection stage is used in an electrical power system. The filtering method processes the instantaneous voltage values and determines the current frequency using a suitable combination of filters. The frequency protection function selects automatically the largest voltage as the measurement value. In a multiphase connection, the phase-to-phase voltage is always the largest.

For increased reliability of the protection both functions can be used (Overfrequency A and Overfrequency B). It is possible to implement a 2-out-of-2 decision by connecting the operate indications of both functions in a continuous function chart (CFC) using a logical AND gate.

Application and Setting Notes

Parameter: Minimum Voltage For the Undervoltage blocking, Siemens recommends 65% of the rated voltage of the protected object as the setting value. In the angle-difference method, the setting value relates to the positive-sequence voltage.

Parameter: Dropout Differential Due to the high-precision frequency measurement, the recommended setting value for the dropout differential is 20 mHz. If a later dropout is needed, the setting value can be increased. For example, if the pickup value (parameter threshold) of the stage is set to 51.5 Hz and the dropout differential to 100 mHz, the stage will drop out at 51.4 Hz.

Operating Times The expected pickup times for the Overfrequency protection function are extracted from the Technical Data of the relay manual and provided below.

Angle-difference method PU: approx. 70 ms + OOT*

Filtering method PU: approx. 79 ms + OOT

OOT = Output Operating Time: additional delay of the output medium used, for example 5 ms with fast relays.

5.2.2. RoCoF Protection Function (ANSI81R)

The function Rate of frequency change protection is used to:

- Detect a frequency change quickly
- Prevent the system from not secure states caused by unbalance between the generated and consumed active power
- Network decoupling
- Load shedding

The function RoCoF can be used in protection function groups containing a 3-phase voltage measurement.

Two function block types are available:

- df/dt rising
- df/dt falling

This function uses the frequency calculated via the angle difference algorithm. The frequency difference is calculated over a settable time interval (default setting: 5 periods). The ratio between the frequency difference and the time difference reflects the frequency change which can be positive or negative.

A stabilization counter works to avoid overfunction. This counter is increased if the set threshold value is exceeded. If the value drops below the threshold value, the counter is reset immediately. The counter is set to 8 internally and is activated at each half-system cycle.

Application and Setting Notes

Parameter: Minimum voltage For the undervoltage blocking, 65% of the rated voltage of the protected object is recommended. The method of measurement uses the phasor of the positive-sequence voltage. When determining the setting value, the absolute value of the sound positive-sequence voltage is equal to the absolute value of the phase-to-ground voltage. The default setting is referred to this value.

Parameter: Measuring window The measuring window parameter can be used to optimize the measuring accuracy or the pickup time of the function. The default setting is 5 periods because it provides maximum measuring accuracy.

Frequency rising/falling The stage df/dt falling is used to detect frequency falling and the stage df/dt rising is used to detect frequency rising. The threshold value should be set as an absolute value and the frequency-change direction is defined via the selected stage type.

Parameter: Threshold Default setting: Threshold = 3.000 Hz/s

The pickup value depends on the application and is determined by power-system conditions. In most cases, a network analysis is necessary. A sudden disconnection of loads leads to a surplus of active power. The frequency rises and causes a positive frequency change. On the other hand, a failure of generators leads to a lack of active power. The frequency drops and results in a negative frequency change.

Parameter: Dropout differential The dropout differential parameter is used to define the dropout value. The recommended value is 0.10 Hz/s.

Operating Times The expected pickup time for the Rate of change of frequency protection function is extracted from the Technical Data of the relay manual and provided below.

df/dt PU time: approx. 160 ms + OOT to 220 ms + OOT (depends on the measuring window length).

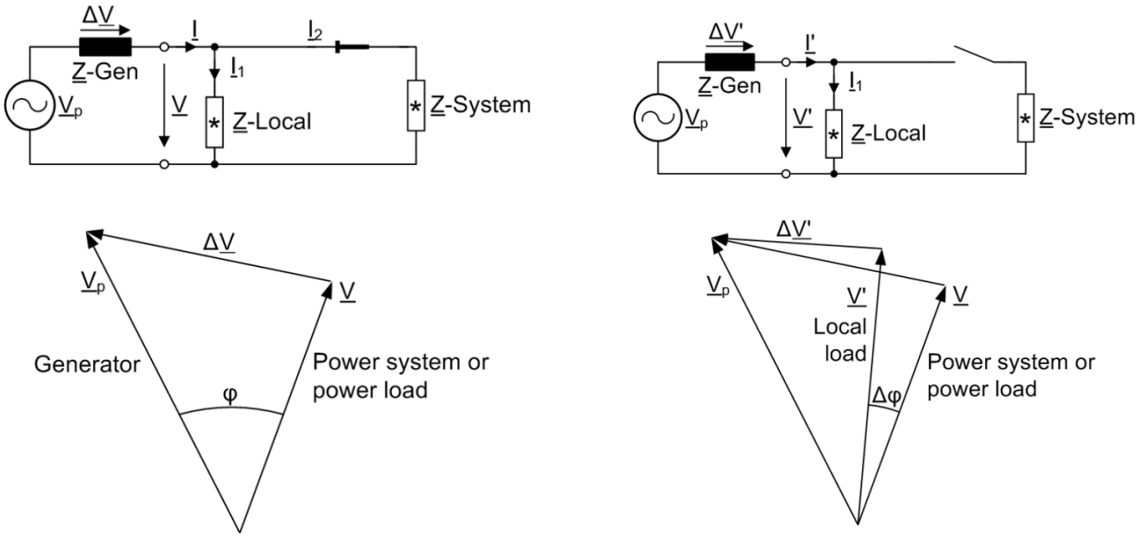
OOT = Output Operating Time: additional delay of the output medium used, for example 5 ms with fast relays.

5.2.3. Vector-jump protection function (ANSI78)

The Vector-jump protection function is used for:

- Network decoupling of the power generating unit in case of a load loss
- Evaluate the phase-angle jump of the voltage phasors

Figure 5.1 shows the basic principle of the function Vector-jump protection. Figure 5.1a shows the voltage vector of the steady state condition. Figure 5.1b shows the vector change after load shedding.



(a) Voltage Vector of the Steady State

(b) Vector Change after Load Shedding

Figure 5.1: Basic Principle of Vector Jump protection [1]

A phase-angle jump occurs with load loss and is the evaluation criterion for the function Vector-jump protection. If the phase-angle differential exceeds a set threshold, the generator circuit breaker or the circuit breaker of the system switch opens. Therefore, the generator unit can be protected against unacceptable stress.

The following measures are applied to avoid unwanted tripping:

- Correction of steady-state deviations from rated frequency
- Frequency operating range limited to $f_{\mathrm{rated}} \pm 3$Hz
- High measuring accuracy by using frequency-tracked measured values and evaluation of the positive-sequence phasor
- Enabling the minimum voltage for the function Vector-jump protection
- Blocking the function when the primary voltage is switched on or off as switching can lead to a phase-angle jump.

Phase-Angle Calculation The phase-angle differential is calculated at different time intervals (t–T, t–2T, t–3T[2]) from the vector of the positive-sequence voltage via a delta-interval measurement. With

the current measured power frequency, the measuring errors of the angle measurement caused by frequency deviations are compensated.

Voltage and frequency tolerance range If the measured frequency or voltage is below the set threshold, the function Vector-jump protection is blocked. The threshold of the voltage band is configurable. The frequency band range is fixed from $f_{\text{rated}} - 3$Hz to $f_{\text{rated}} + 3$Hz.

Measurand The general functionality calculates the phase-angle displacement $\Delta\phi$ and sends it to the Δφ stage. $\Delta\phi$ is used for comparison with the parameter Threshold Δφ. $\Delta\phi$ is displayed in the functional measured value and can be routed in a fault record and displayed in the fault log.

Application and Setting Notes

Parameter: T_Block The parameter T Block sets the dropout delay of the Δφ stage. When voltages are connected or disconnected, the overfunction can be avoided with the timer T_Block which should always be set to 2 cycles more than the measuring window for vector-jump measurement.

Pickup The Δφ stage compares the value of the vector jump $\Delta\phi$ with the Threshold Δφ. If the value of the Threshold Δφ is exceeded, the pickup delay starts. The vector jump $\Delta\phi$ is stored in an RS flip-flop. Trippings can be delayed by the associated time delay.

Parameter: Threshold Δφ The parameter value to be set for the vector jump depends on the supply and load conditions. Load changes cause a jump in the voltage vector. The value to be set must be established in accordance with the particular power system. An estimation can be done based on the system equivalent circuit in Figure 5.1b. If the setting for the parameter Threshold Δφ is too sensitive, every time loads are connected or disconnected, the protection function performs a network decoupling. Therefore, if no other calculated value is applicable to the setting of this parameter, Siemens recommends using the default setting Δφ = 10°.

Parameter: T_Reset Used to reset the time for the Pickup indication stored in the RS flip-flop. When the timer T_Reset expires, the protection function is reset automatically. The reset time depends on the decoupling requirements and must expire before the circuit breaker is reclosed. The default setting is 5.00 s.

Operating Times The expected pickup time for the Vector-jump protection function is extracted from the Technical Data of the relay manual and provided below.

Vector-jump PU time: approx. 80 ms + OOT.

OOT = Output Operating Time: additional delay of the output medium used, for example 5 ms with fast relays.

5.2.4. Undervoltage Protection with Positive Sequence Voltage (ANSI27)

- Monitors the permissible voltage range
- Protects equipment (for example, plant components and machines) from damages caused by under voltage
- Protects motors and generators from inadmissible operating states and a possible loss of stability in the event of voltage dips

Two-phase short circuits or ground faults lead to an unbalanced voltage collapse, however such events have no noticeable impact on the positive-sequence voltage. This makes this function particularly suitable for the assessment of stability problems.

Method of Measurement The stage uses the positive sequence voltage calculated from the measured phase-to-ground voltages according to the defining equation.

Application and Setting Notes

Parameter: Threshold For the default setting, the lower limit of the voltage range to be monitored is assumed to be 80% of the rated voltage of the protected object.

Parameter: Pickup delay The Pickup delay parameter is only available if the current flow criterion of the function is used. The parameter Pickup delay is set to delay the pickup of the stage by approximately 40 ms or not. The delay avoids possible brief pickup of the stage when the circuit breaker opens.

Parameter: Dropout ratio The recommended setting value of 1.05 is sufficient for many applications. To obtain extremely accurate indications, the Dropout ratio can be reduced.

Operating Times The expected pickup time for the Undervoltage protection function is extracted from the Technical Data of the relay manual and provided below.

Undervolt. pos. seq. PU time: approx. 25 ms + OOT to 30 ms + OOT

OOT = Output Operating Time: additional delay of the output medium used, for example 5 ms with fast relays.

5.3. Protection Logic Development with ATP-EMTP

This section describes the design and implementation of the islanding protection logic in ATP-EMTP. First the measured values used as inputs are listed, then the two main detection stages of the protection logic are explained, followed by details of the ATP model. Finally, the test scenarios are conducted to verify correct operation of the tripping scheme.

5.3.1. Measured Values

The island condition is detected at the MV substation SUBTZE busbar and the tripping logic uses as input only the voltage measured at this location. The currents at the outgoing feeders LV transformer and substation SUB50 can be used for further improvement of the protection logic reliability (if needed). The following measuring points are defined:

- **VTZE (A, B, C)**: Busbar voltage at SUBTZE used for protection trips.
- **CT18 & CT15 (A, B, C)**: Feeder currents to LV-XFM & SUB50 monitored for further improvement of the protection logic.

5.3.2. Logic Architecture

The protection logic consists of two sequential stages: Loss-of-Mains and Load Shedding.

Stage I: Loss-of-Mains Trip

Issues an OPEN command to the utility breakers, based on a 4-out-of-4 decision logic, as seen in Figure 5.2.

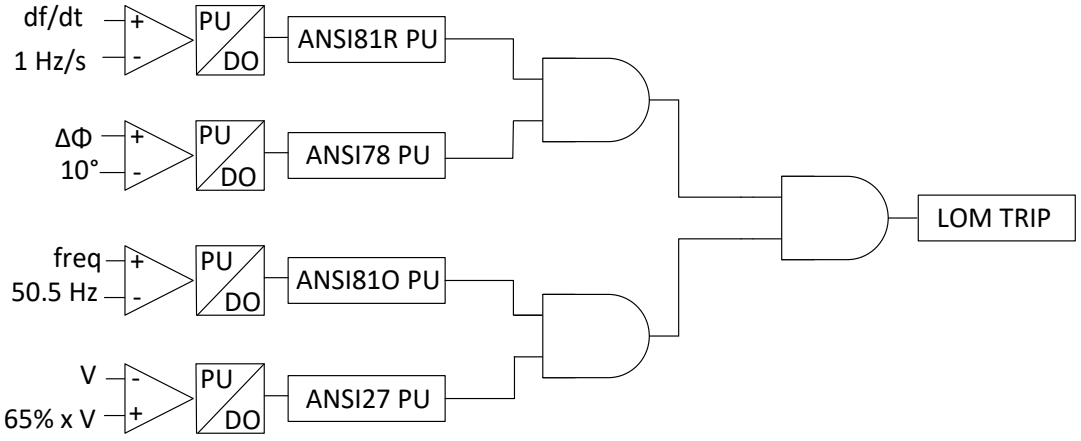


Figure 5.2: Logic Diagram for Loss-of-Mains Protection Trip

- Required Signals: dfdt rising stage (PU signal `DFDTR`), vector jump (PU signal `VJTRIP`), undervoltage stage I (PU signal `UV1`), overfrequency stage II (PU signal `OF2`).
- Condition: Fault-Ride-Through (FRT) time delay expired.
- Actions: Send OPEN/TRIP Command to the incomer breakers.

Stage II: Load-Shedding Trip

Ensures island stability by shedding load and/ or generation, similarly based on a 4-out-of-4 decision logic, as provided in Figure 5.3.

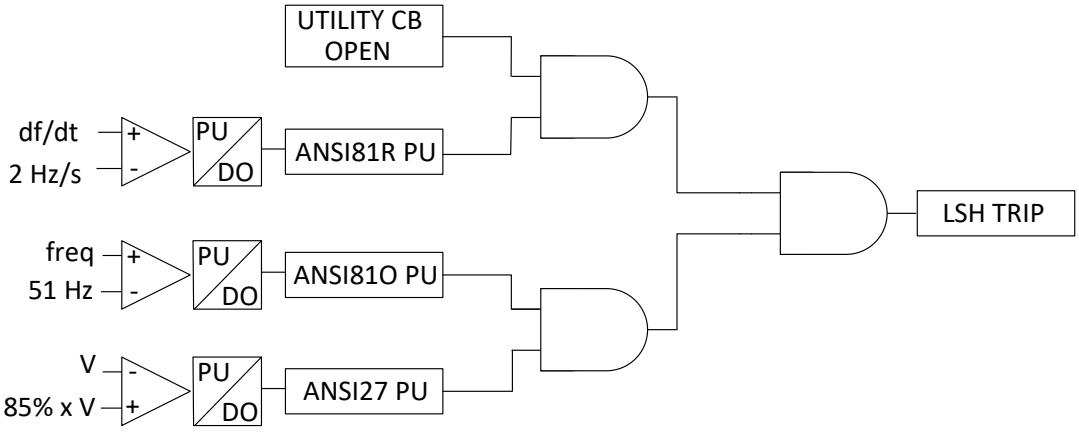


Figure 5.3: Logic Diagram for Load Shedding Protection Trip

- Required Signals: undervoltage stage II (PU signal `UV2`), overfrequency stage III (PU signal `OF3`), dfdt falling stage (PU signal `DFDTF`).
- Condition: Utility breaker status confirmed to be OPEN.
- Actions: Trip load/generator breakers (e.g. GTG-201) and send ISOC mode swap signal to GTG-101 governor controller.

5.3.3. Signal Processing Models

The protection logic is implemented in ATP-EMTP as per the block diagram provided in Figure 5.4. The MODELS component that creates IEEE COMTRADE C7.111, 1999 format output is used to route both analog (voltage and current curves) and digital (trip/ open command, breaker status) signals for further test results analysis.

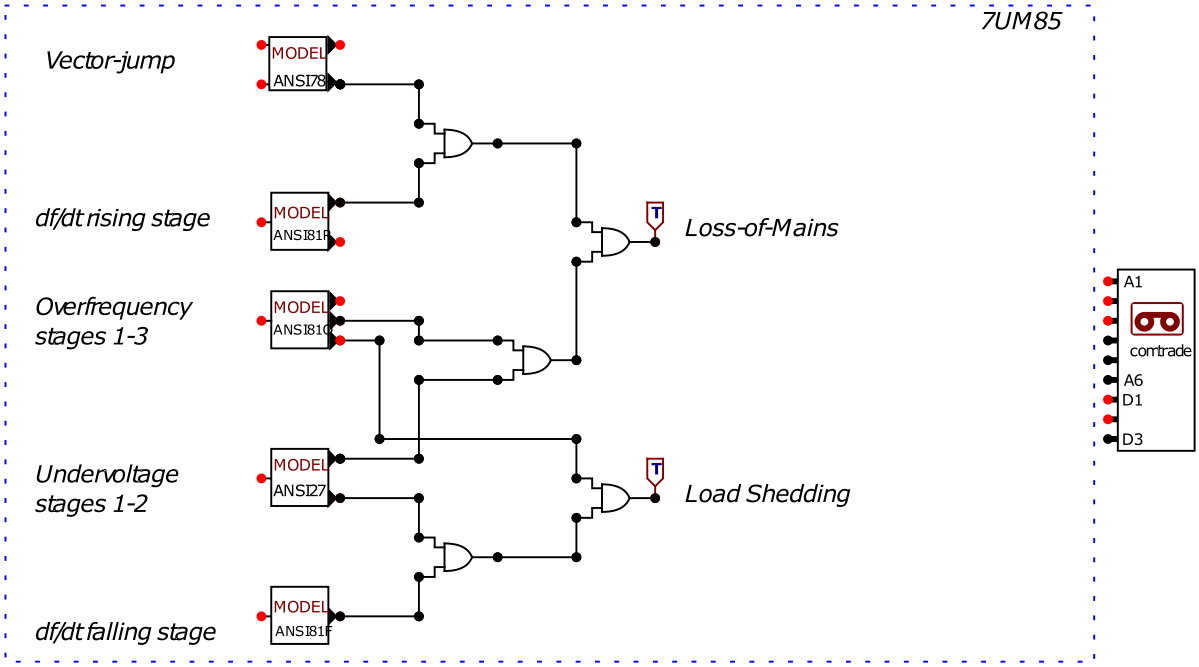


Figure 5.4: Block diagram of islanding detection and load-shedding logic in ATP-EMTP.

The tripping functions are developed using MODELS language in ATP-EMTP, with the code provided in Appendices and the logic explained below.

RoCoF Model - ANSI81R: the voltage measured at the MV busbar is passed through a Butterworth low-pass filter and used as input for the frequency calculation model. The frequency is estimated by means of a PLL (phase-locked loop) Model which operates using dq-components of measured voltages. The frequency output of the PLLDQ Model is used as input to the RoCoF Model. The df/dt value is calculated over an adjustable measuring-window of 5 periods, with a stabilization-counter set at 4 half-cycles.

- **ANSI81R - Rising Stage:** The model uses a pickup threshold of 1 Hz/s and it operates within a nominal frequency ± 3 Hz window. The function uses a dropout differential of 0.5 Hz/s to reset.
- **ANSI81R - Falling Stage:** This model determines the falling-stage threshold as an absolute value; the pickup is set at 2 Hz/s. The resulting signal is used for load or generation shedding, and is intended to activate only after the utility breakers have opened and the system has transitioned into island mode. To restore stability, one of the two generators must be disconnected.

Overfreq. MODEL - ANSI81O: receives the system frequency from the PLL Model and operates in three stages. Stage I detects frequency between 50.2 Hz and 50.5 Hz, Stage II from 50.5 Hz to 51 Hz, and Stage III above 51 Hz. Stages II and III are used for tripping: Stage II targets loss-of-mains detection, marking the point when machine control systems have completed their response, while Stage III supports load shedding, indicating a sustained frequency rise after grid disconnection. To confirm stability, the model uses half-cycle counting, requiring the frequency to remain above the threshold for a set duration before tripping. Trips are reset if frequency drops below a margin (DO = 0.02 Hz), and an automatic reset occurs after a timer (T_Reset). To avoid false positives, the operation is blocked during startup (T_block) and whenever the frequency falls outside a valid range of ±3 Hz around nominal (fb_tol).

Vector-jump MODEL - ANSI78: monitors the voltage phase angle (Theta) and compares it with delayed samples taken 1, 2, and 3 cycles earlier, computing three angle shifts (delta1, delta2, delta3). The largest shift (max_delta) represents the vector jump. If this exceeds the defined threshold (Vect_Thrs = 10°), the pickup signal (vect_pickup) is activated. Detection is blocked during startup (T_block) and when the frequency is outside the ±3 Hz tolerance band (fb_tol). The model also accounts for normal system rotation by compensating for expected angular shifts over full cycles (360 × n_cycles), ensuring only abrupt, abnormal jumps trigger the protection.

Undervoltage pos. seq. MODEL - ANSI27-V1: uses the positive-sequence line-to-line voltage from the Vmeter Model to detect undervoltage conditions through two stages. Stage I activates when the measured voltage is between 5% and 65%, and Stage II triggers if voltage rises above 65% but stays below 85% of nominal. The model resets outputs at each cycle unless the input meets the trip criteria. Voltage levels below 5% of nominal are considered invalid and the function is blocked.

5.3.4. Thresholds and Settings

The tripping thresholds are provided in Table 5.1.

Prot. Function	Stage	PU Threshold	Dropout Diff.
ANSI81R	df/dt rising	$1\,\mathrm{Hz/s}$	$0.5\,\mathrm{Hz/s}$
	df/dt falling	$2\,\mathrm{Hz/s}$	
ANSI78	Δφ	$10\,\mathrm{Deg}$	
ANSI27-V1	Stage I	$65\,\%$ Vrated	
	Stage II	$85\,\%$ Vrated	
ANSI81O	Stage II	$50.5\,\mathrm{Hz}$	$20\,\mathrm{mHz}$
	Stage III	$51\,\mathrm{Hz}$	

Table 5.1: Protection Settings thresholds

5.3.5. Simulation Scenarios

The protection scheme is tested and validated for the following fault scenarios:

- *Island formation:* Three-phase, two-phase, single-phase fault at Utility.
- *Internal faults:* Three-phase and two-phase fault at the outgoing feeders LV18 and SUB50.
- *Generation Loss:* Three-phase fault at GTG-201.

The test cases will be referred to as:

- **Test Case F1:** Three-phase fault at Utility
- **Test Case F2:** Three-phase Fault at GTG-201
- **Test Case F3:** Three-phase Fault at LV18-XFM
- **Test Case F4:** Three-phase Fault at SUB50
- **Test Case F5:** Two-phase fault at Utility
- **Test Case F6:** Two-phase Fault at LV18-XFM
- **Test Case F7:** Two-phase Fault at SUB50
- **Test Case F8:** Single-phase Fault at Utility

The expectation is that the Loss-of-Mains logic will reliably identify an island condition and will trip the incomer breakers only for an external three-phase fault at the Utility side (Test Case F1). The incomer breakers shall not be opened before the FRT time delay has passed (FRT = 200 ms from fault inception), but no later than the CCT for the fault type and location (CCT = 320 ms).

5.4. Protection Scheme Testing and Validation

5.4.1. Test Case F1

Figure 5.5 shows that the LOM stage trips the incomer breaker (CBLOM) after 258.5 ms from fault start. The LSH stage trips the generator breaker (CBG2) after another 324.5 ms from the LOM Trip. The signals that contribute to the protection logics are explained below.

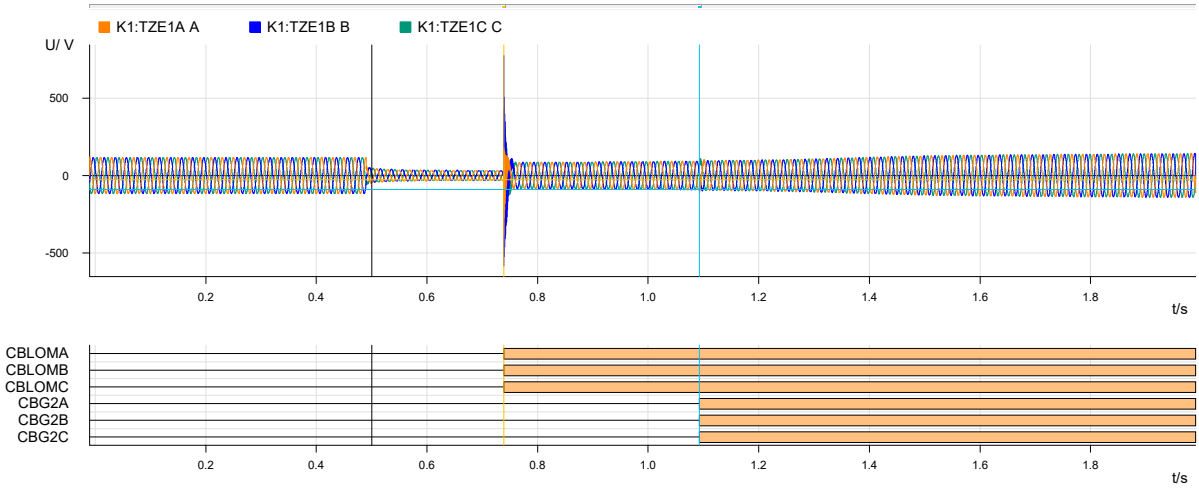
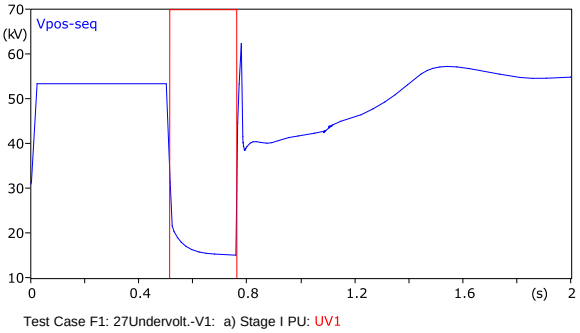
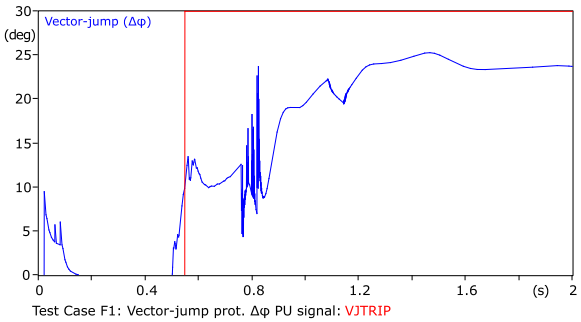


Figure 5.5: Test Case F1: 3LG at Utility

The positive sequence voltage curve can be observed in Figure 5.6a; the undervoltage protection function (ANSI27-V1) has two stages and the tripping signal for Stage I (red line - UV1) is plotted on top of the voltage curve. It can be observed that when the fault starts, the positive sequence voltage drops below 20 kV, thus the undervoltage protection function UV1 picks up in 12 ms. Figure 5.6b shows the phase-angle of the positive sequence voltage. After the fault starts, the load loss causes the phase-angle to jump above the acceptable limit of 10°. The vector-jump protection function (ANSI78) picks up in 47.5 ms and the tripping signal is plotted on top of the phase-angle curve (red line - VJTRIP).



(a) UV1 PU time = 12 ms

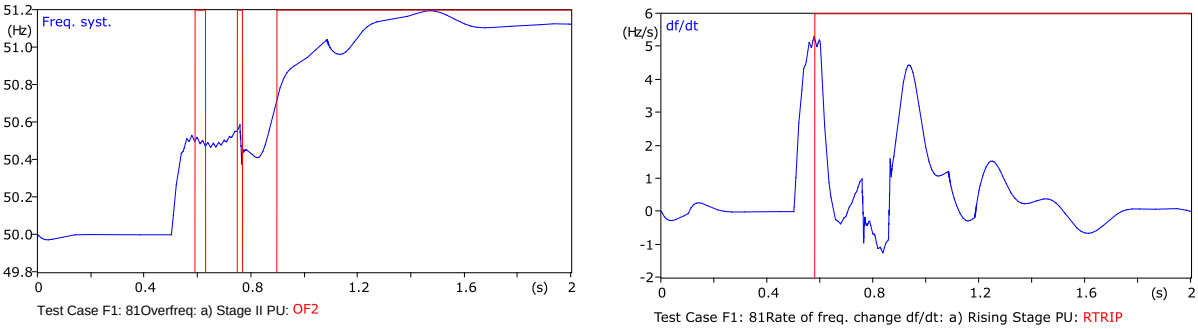


(b) Vector-jump PU time = 47.5 ms

Figure 5.6: LOM TRIP: Voltage-based Tripping Signals

The frequency curve is shown in Figure 5.7a. The Overfrequency protection function (ANSI810) consists of three stages and the tripping signal of Stage II (red line - OF2) is plotted on top of the frequency curve. After fault initiation, the frequency exceeds the Stage II threshold twice, causing the OF2 signal to pick up and quickly drop out. This happens due to the control systems of the synchronous machines that work to stabilize the frequency by reducing the machine's mechanical input, as previously explained in Chapter 4. Due to the fault severity and sustained duration, the frequency exceeds the Stage II threshold and the OF2 signal picks up at 248 ms, without dropping out. The rate of change of frequency is plotted in Figure 5.7b. The rising stage PU signal of the 81RoCoF protection function is

plotted on top of the df/dt curve. The PU threshold is 1 Hz/s and the measuring-window is 5 periods, thus the rising stage picks up in approx 80 ms from the fault start because the measured df/dt exceeds the PU threshold almost as soon as the fault starts.



(a) OF2 PU time = 248 ms

(b) RTRIP PU time = 79.5 ms

Figure 5.7: LOM TRIP: Frequency-based Tripping Signals

After the LOM TRIP opens the utility breaker the system is islanded. The Load Shedding stage checks the required PU signals to stabilize the island, if needed. Undervoltage Stage II, Overfrequency Stage III and RoCoF Falling Stage are explained below.

The positive sequence voltage curve can be seen in Figure 5.8. After opening the utility CB, the voltage rises above 65% but doesn't fully recover due to the loss of reactive support from the grid. The Undervoltage Stage II signal (green line - UV2) is plotted on top of the voltage curve and the pickup happens at t= 283.5 ms.

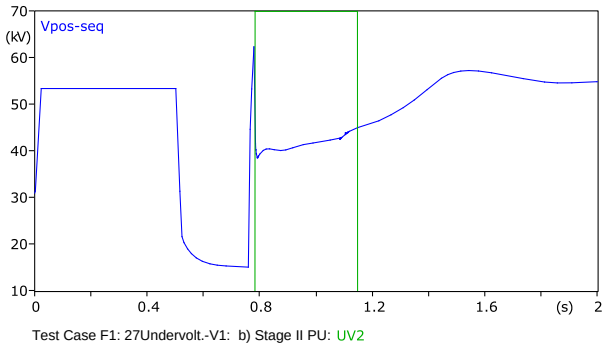
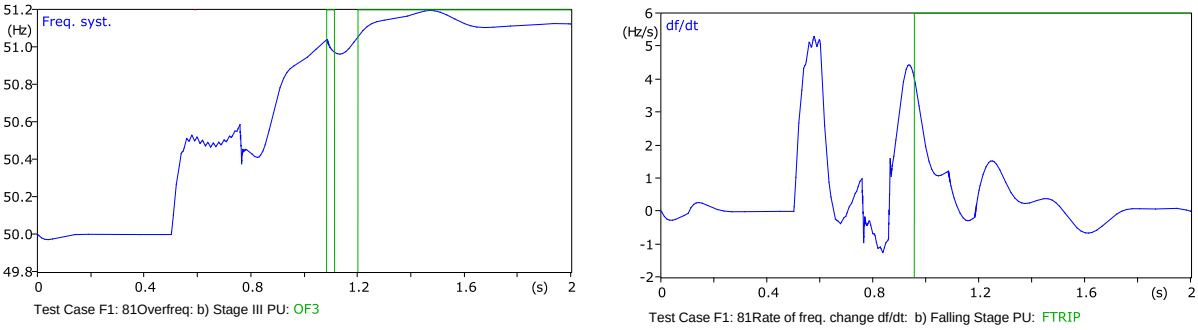


Figure 5.8: LSH TRIP: UV2 PU time = 283.5 ms

The frequency plot can be seen in Figure 5.9a. Because the generated power exceeds the load demand, the frequency continues to increase after islanding. The Overfrequency protection function Stage III is plotted on top of the frequency curve (green line - OF3). The 51 Hz threshold is exceeded but the OF3 PU signal quickly drops out, due to the control systems of the generators that reduce the speed of the machines by reducing the active power output. This is not enough to stabilize the island, because the generation vs load demand is too high, thus the 51 Hz threshold is exceeded once again and the Overfrequency Stage III function picks up without dropping out at t= 583 ms.

The df/dt curve can be seen in Figure 5.9b. The RoCoF Falling Stage PU signal (green line - FTRIP) is plotted on top of the df/dt curve and the absolute value of 2 Hz/s needs to be exceeded consequently for at least 4 half-cycles for the signal to pickup. Due to the switching transient from opening the utility CB, the frequency drops and the df/dt falls below zero. Due to the imbalance of load demand vs active power generation, df/dt starts rising again and the falling stage picks up at t= 455 ms.



(a) OF3 PU time = 583 ms

(b) FTRIP PU time = 455 ms

Figure 5.9: LSH TRIP: Frequency-based Tripping Signals

As explained above, the LOM TRIP opened the incomer CB after approx. 250 ms from fault start. Consequently, the LSH TRIP signal becomes active after approx. 325 ms from the LOM TRIP. The LSH TRIP signal is used to send the Trip/Open Command to the CB of GTG201. The LSH TRIP signal is also sent to the distributed control system (DCS).

The DCS uses the LSH TRIP signal for the following actions:

- send a command to LV Load Shedding System to trip non-critical load (one induction motor) at the same time that the GTG201 CB opens;
- send a command to the governor system of generator GTG101 to swap from DROOP mode to ISOC operation;
- send a close command to the star-point of the step-transformer of GTG101 to keep the island solidly grounded.

5.4.2. Test Cases F2-4

The protection logic uses the measured voltage at the MV busbar to calculate the frequency, rate of frequency change, and vector jump with the minimum requirement of V measured = 5% * Vrated. An internal three-phase short circuit collapses all three phase-to-ground voltages to zero as can be seen in Figure 5.10, so the measured signal doesn't reach the 5 % validity threshold and the protection settings are not active.

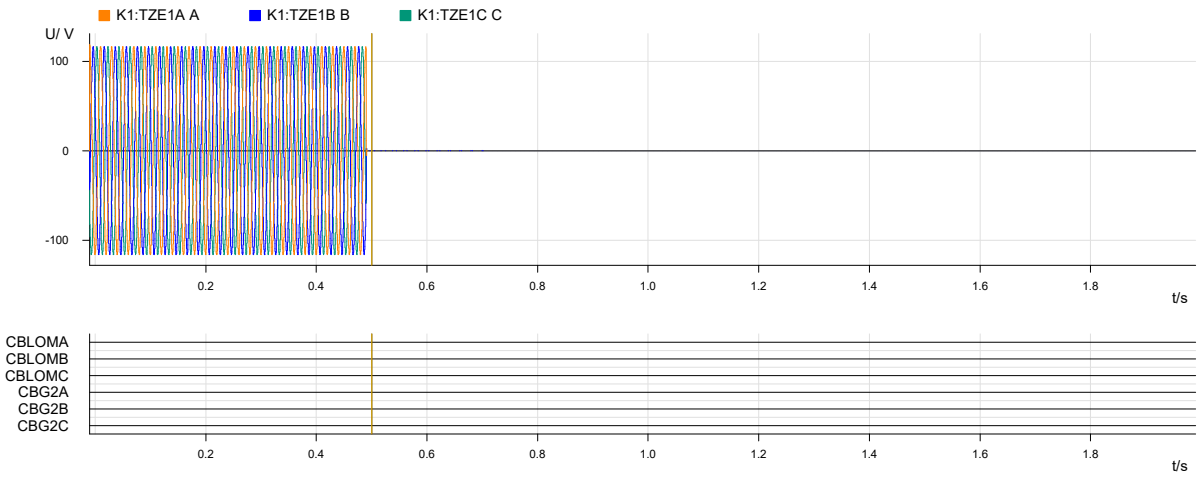


Figure 5.10: Test Cases F2, F3, F4: internal 3LG fault

5.4.3. Test Case F5

The LOM stage trips the incomer breaker (CBLOM) after 1083 ms from fault start, as can be seen in Figure 5.11.

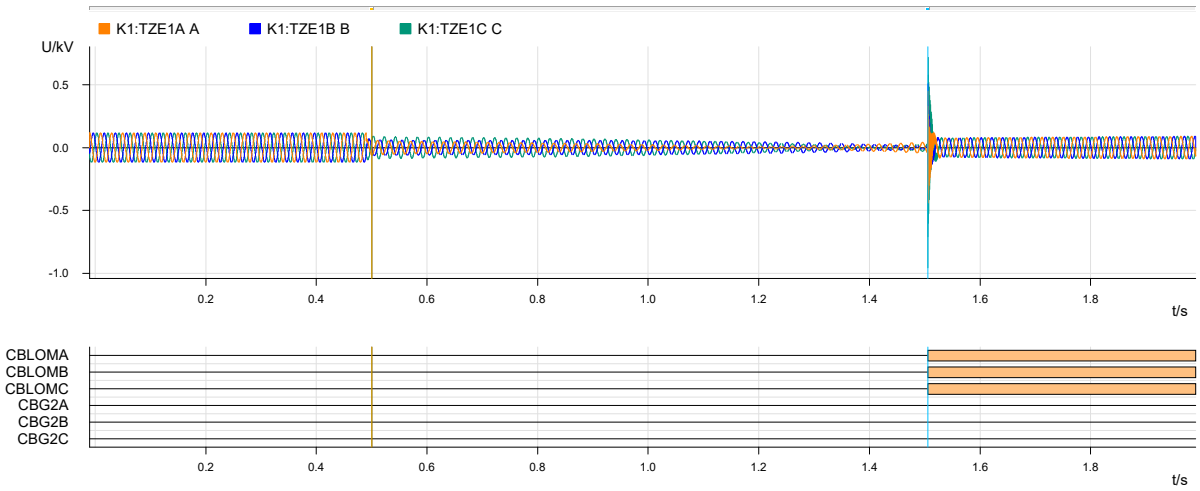
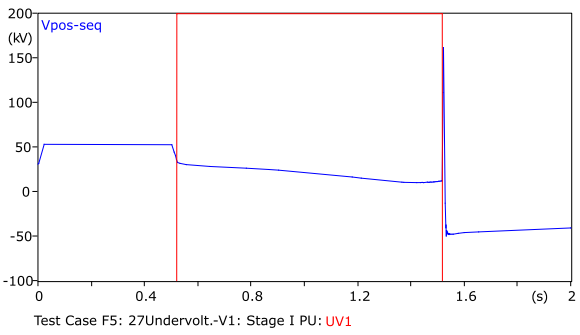
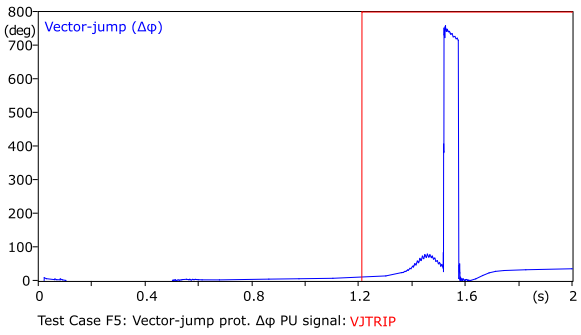


Figure 5.11: Test Case F5: 2LG at Utility

The tripping signals for the LOM stage are explained below. During an unbalanced fault (2LG), the positive sequence voltage drops to 65% of the rated value, so the Undervoltage Stage I (red line - UV1) protection picks up at t= 20 ms, as can be seen in Figure 5.12a. During the 2LG fault, the voltage phase-angle jump doesn't exceed the tripping threshold of 10 Deg, as can be seen in Figure 5.12b. After the fault duration exceeds the critical clearing time of 580 ms, the generators fall out of step, losing synchronism with the grid. Thus, the voltage phase-angle jumps above the acceptable limit, and the Vector-jump protection picks up at t= 711 ms.



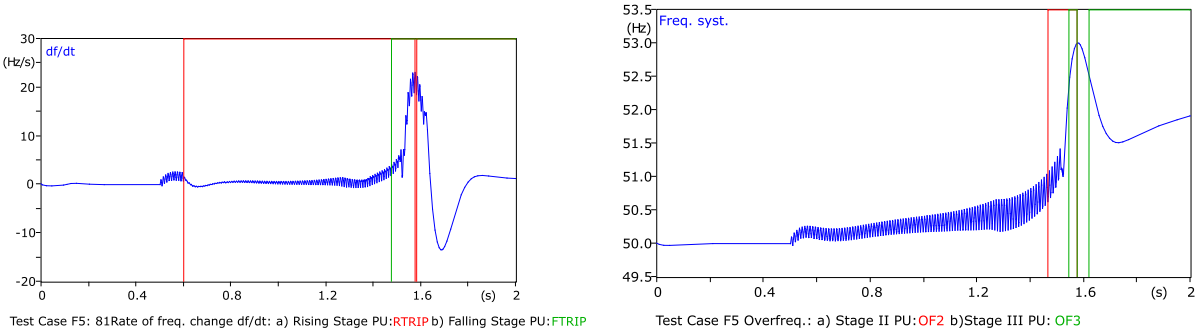
(a) UV1 PU time = 20 ms



(b) Vector-jump PU time = 711 ms

Figure 5.12: LOM TRIP: Voltage-based Tripping Signals

The df/dt curve is shown in Figure 5.13a. The 2LG fault causes the frequency to oscillate between 50.2 and 50.5 Hz due to the corrective actions of the control systems of the generators. While the Overfrequency threshold of 50.5 Hz is not exceeded, the fast rate of change of frequency exceeds the 1 Hz/s threshold and the Rising Stage of the RoCoF protection picks up in 100 ms from the fault start. After the system loses synchronism, the frequency rises above 50.5 Hz and the Overfrequency Stage II protection function also picks up at t= 965 ms, as can be seen in Figure 5.13b.



(a) RTRIP PU time = 100 ms, FTRIP PU time = 975 ms

(b) OF2 PU time = 965 ms, OF3 PU time = 1.04 s

Figure 5.13: LOM TRIP: Frequency-based Tripping Signals

After the LOM TRIP opens the incomer CB, the voltage doesn't rise to 85% as for Test Case F1, because in this case the generators are out of step and have fallen outside the capability curve. Thus, the voltage continues to drop and the LSH TRIP signal doesn't become active, as this stage requires a minimum voltage of 85% of the rated value.

5.4.4. Test Cases F6-7

During an internal 2LG fault, the LOM and LSH Stages of the protection logic are inactive, as can be seen in Figure 5.14. While a 2LG fault causes disturbances and some of the required signals pickup, the condition is not severe enough for the protection functions to become active in the same time and to issue a Trip/ Open Command to the incomer breaker.

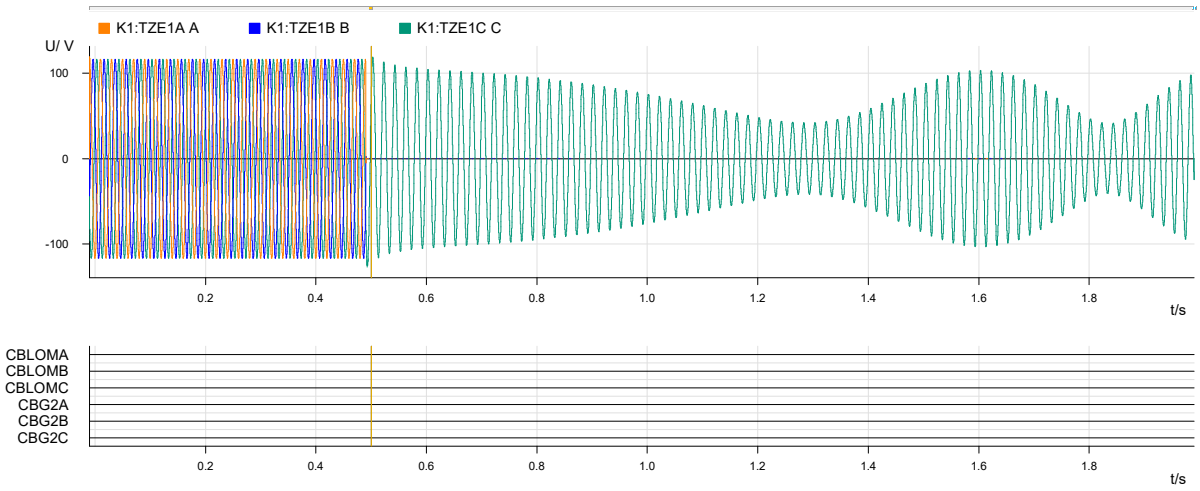


Figure 5.14: Test Cases F6, F7: internal 2LG fault

5.4.5. Test Case F8

The phase-to-ground fault is not severe enough for the designed protection logic to pickup, thus no trip command is issued, as observed in Figure 5.15.

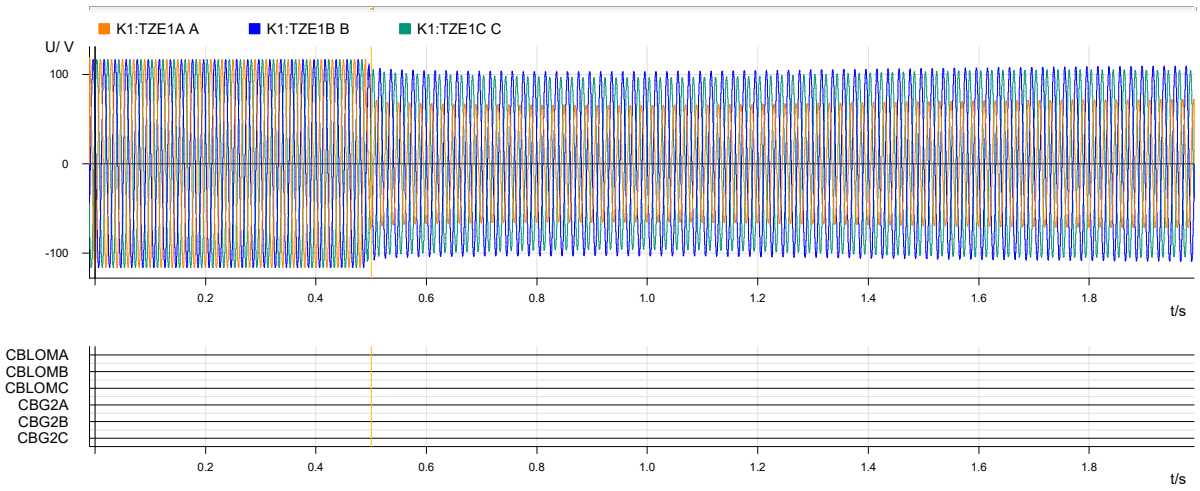


Figure 5.15: Test Case F8: 1LG at Utility

5.5. Results ATP-EMTP

The results of the testing cases are presented in Table 5.2.

Test Case	*LOM TRIP*	*LSH TRIP*	*Result*
F1	258.5 ms	LOM TRIP + 324.5 ms	Passed
F2	NO TRIP	NO TRIP	Passed
F3	NO TRIP	NO TRIP	Passed
F4	NO TRIP	NO TRIP	Passed
F5	1083 ms	NO TRIP	Failed
F6	NO TRIP	NO TRIP	Passed
F7	NO TRIP	NO TRIP	Passed
F8	NO TRIP	NO TRIP	Passed

Table 5.2: Islanding Tripping Scheme Test Results

Test case F1: The protection logic correctly identifies an island condition and issues the open command to the incomer breakers in the required time frame: FRT = 200 ms < TRIP = 260 ms < CCT = 320 ms. The Load Shedding signal follows after an additional 325 ms, effectively stabilizing the island by opening the generator GTG201 CB and sending the signal further to the DCS.

Test cases F2, F3, and F4: The protection logic uses the measured voltage at the MV busbar to calculate the frequency, rate of frequency change, and vector jump with the minimum requirement of Vmeasured = 5% * Vrated. An internal three-phase short circuit collapses all three phase-to-ground voltages to zero, so the measured signal doesn't reach the 5 % validity threshold and the protection settings are not active.

Test Case F5: the protection logic is designed for balanced faults, thus it uses protection functions that are based on the positive sequence voltage (ANSI27-V1, ANSI81O-A, ANSI78). The logic is very effective during a 3LG fault, but it can't be used for a 2LG fault. The functions that pick up before the system loses synchronism (so before the critical clearing time of the fault is exceeded) are Undervoltage Stage 1 and RoCoF Rising Stage.

Test Cases F6, F7: for the same reasons mentioned for Test Case F5, the protection logic is inactive during an internal 2LG fault. Considering the current thresholds of the protection settings, the tripping

signals don't pickup in the same time, but because the busbar voltage is stable enough for the functions to be calculated, Overcurrent Blocking can be used to eliminate the risk of a false pickup.

Test Case F8: the fault is not severe enough to create a pick up of the protection functions.

5.6. Conclusions

When designing the protection logic, the most severe scenario is considered: three-phase to ground fault with the machines operating at rated power. The DutchNetcode requires that the machines stay connected to the utility grid for at least 200 ms after the fault starts. In conclusion, an islanding tripping scheme should consider the power system's stability margins, as well as the requirements of the transmission system operator.

The control systems of the machines respond during the first 200 ms after the fault initiation. This causes the frequency to oscillate between 50.2 Hz and 50.5 Hz. The Overfrequency protection function is programmed to include both stages: stage I (f > 50.2 Hz) identifies the beginning of the control systems response and stage II (f > 50.5 Hz) identifies the end of the corrective actions. If the frequency keeps rising after the control systems finished their response, it means that the system is unstable and additional measures need to be taken. In conclusion, when designing an islanding tripping scheme the effectiveness of the control systems action can be identified by using Overfrequency stages.

When using a PU threshold of 1 Hz/s, the rate of change of frequency picks up during the first 200 ms of the fault, so during the response of the control systems of the machines. When increasing the PU threshold to 1.5 Hz/s, the function picks up at approx 300 ms which is very close to the CCT of the fault. In practice, the opening time of the CB should also be considered, which is around 50 to 100 ms. If the Trip/ Open command is sent at t= 300 ms, the CB will open after the machines lost synchronism. In conclusion, df/dt PU threshold should be kept under 1.5 Hz/s.

The protection logic is specific to balanced faults. During an unbalanced fault, the logic is inactive. This means that for a 2LG fault at the utility side, additional parameters that consider negative sequence components should be included.

It is observed in Test Case F5 (unbalanced fault) that both RoCoF and Undervoltage functions pick up; while it is expected that df/dt would pick up, the Undervoltage function shouldn't pick up because this function is based on the positive sequence voltage, which is not affected during an unbalanced fault. It can be concluded that the Undervoltage Positive Sequence MODEL developed for this study needs to be improved.

6

Hardware Testing

In this chapter, the islanding-tripping scheme developed and tested with ATP-EMTP, is configured in the SIPROTEC5 relay software and tested with the Omicron Test System. The protection device configuration is explained first, then the test results are provided and explained.

6.1. Test Overview & Setup

For the actual testing of the protection logic discussed in Chapter 5, a combination of software and hardware is used: the 7UM85 generator protection relay is configured in DIGSI5 and the logic is tested with the Omicron Test System consisting of the CMC356+ device as well as Omicron Test Universe for the software part. The setup can be seen in Figure 6.1.

Figure 6.1: Hardware testing setup

The fault signals are exported from ATP-EMTP as .cfg files using the Comtrade component available in ATP-EMTP. The exported fault signals corresponding to each one of the eight test cases are played back into the relay using the Advanced Transplay Module available in Omicron Test Universe.

6.2. Protection Device Configuration

The protection logic programmed with the ATP-EMTP software is configured similarly in the protection device 7UM85 using DIGSI5 software. The single line diagram (SLD) of the Power System is configured in the 7UM85 relay and can be seen in Figure 6.2.

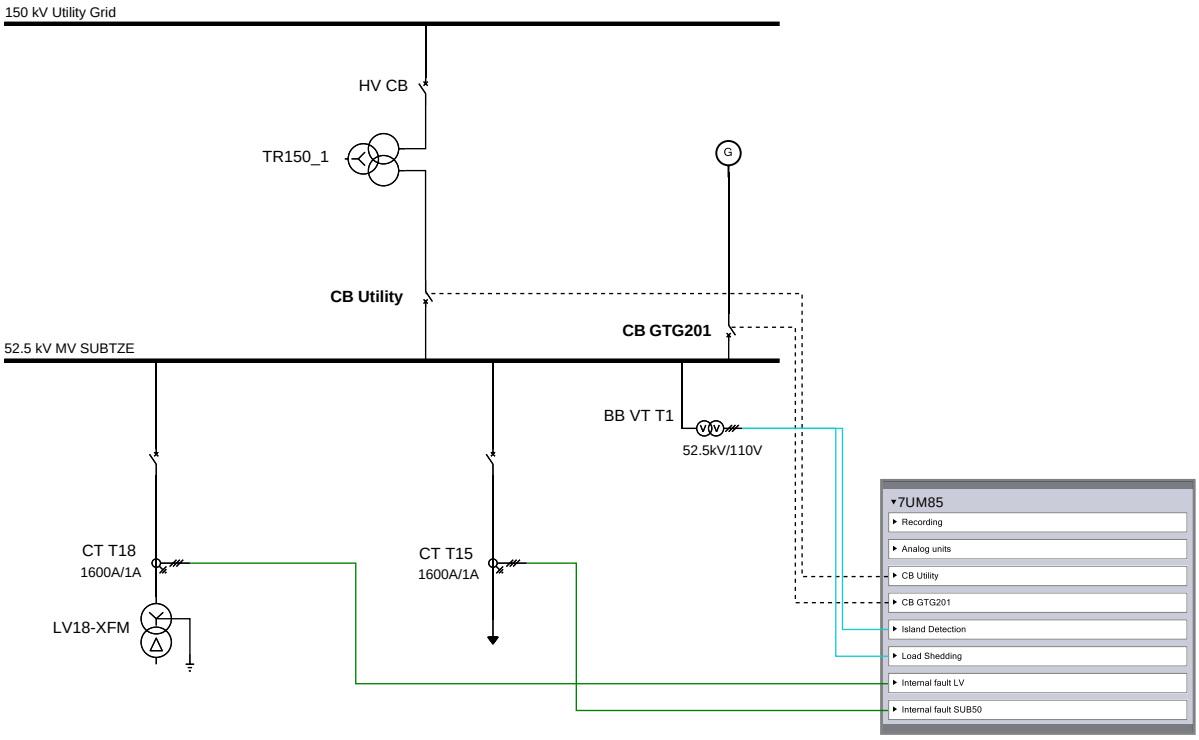


Figure 6.2: Single Line Diagram of the Power System with DIGSI5

6.2.1. Measuring-points

The measured values used as input for the protection settings are the voltage at the MV busbar of substation SUBTZE (VT T1) and the currents at the outgoing feeders LV18-XFM (CT T18) and SUB50 (CT T15), as per Figure 6.3.

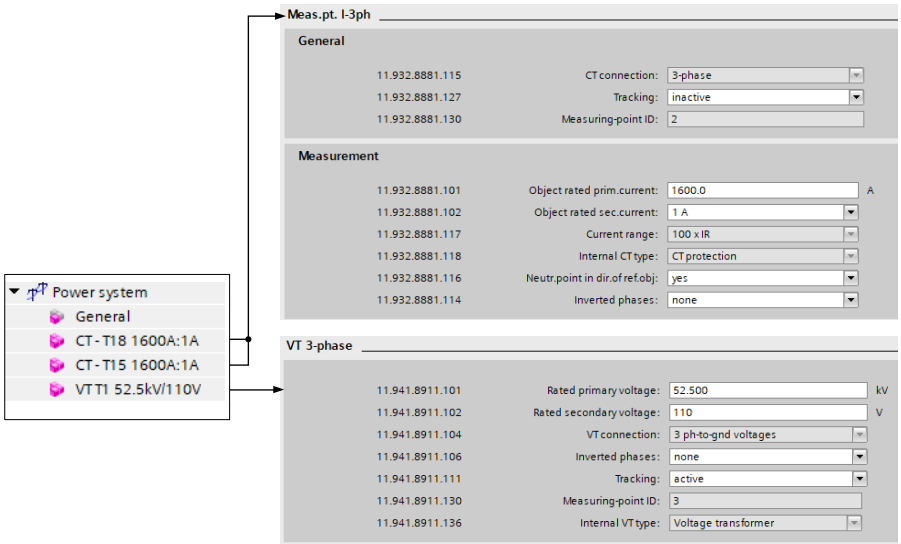


Figure 6.3: 7UM85 Device Configuration - Measuring Points

6.2.2. Protection Settings

Similarly to the implementation in ATP-EMTP, two function groups (FG) are configured in the relay: Island Detection and Load Shedding. The function groups and their respective protection settings can be seen in Figures 6.4 and 6.5. The individual protection settings are not routed to the circuit-breaker interaction to avoid false trips of the corresponding circuit breakers.

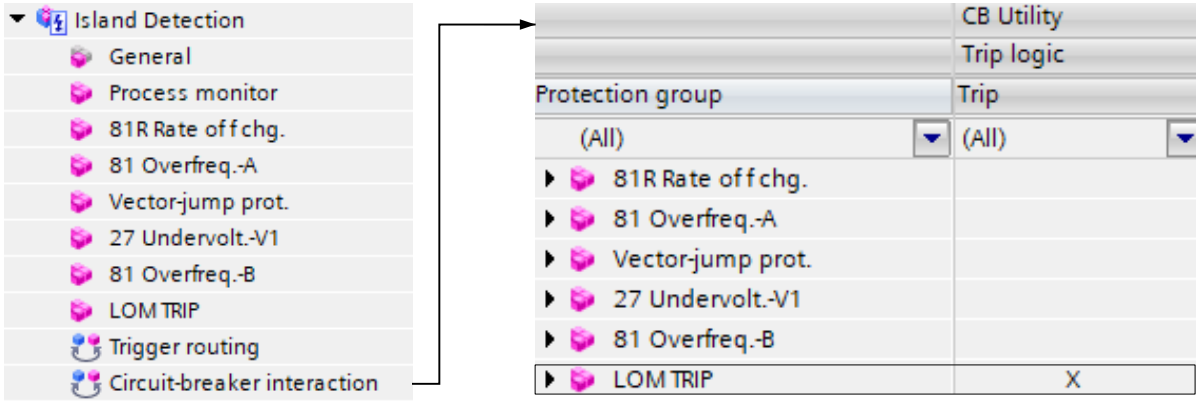


Figure 6.4: 7UM85 Device Configuration - FG Island Detection

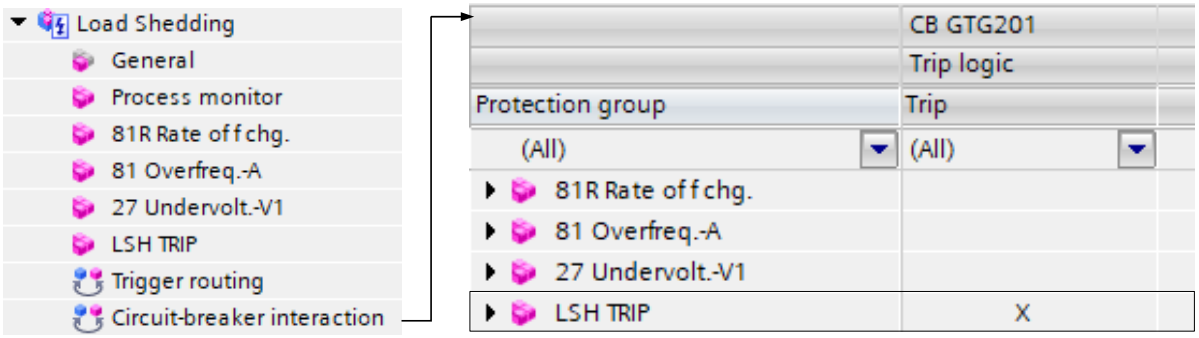


Figure 6.5: 7UM85 Device Configuration - FG Load Shedding

The pick-up (PU) and drop-out (DO) thresholds of the protection settings are presented in Table 6.1, as configured in the protection relay.

Protection Setting	**FG Island Det. PU**	**FG Load Shed. PU**	**DO Differential**
81R Rate of f chg.: df/dt rising	$1\ Hz/s$	$2\ Hz/s$	$0.5\ Hz/s$
81 Overfreq.: Stage 2	$50.5\ Hz$	N/A	$20\ mHz$
81 Overfreq.: Stage 3	N/A	$51\ Hz$	$20\ mHz$
Vector-jump prot.: $\Delta\varphi$	$10°$	N/A	N/A
27 Undervolt.-V1	$30\ V$	$40\ V$	1.05

Table 6.1: Protection Settings Thresholds

6.2.3. Overcurrent blocking

Based on the conclusions from Chapter 5, the protection logic is further improved by Overcurrent blocking of the Loss-of-Mains tripping logic. Two additional function groups are created: Internal Fault LV and Internal Fault SUB50. The Overcurrent protection setting (ANSI51) uses an inverse-time characteristic. The function groups and their respective protection settings can be seen in Figure 6.6.

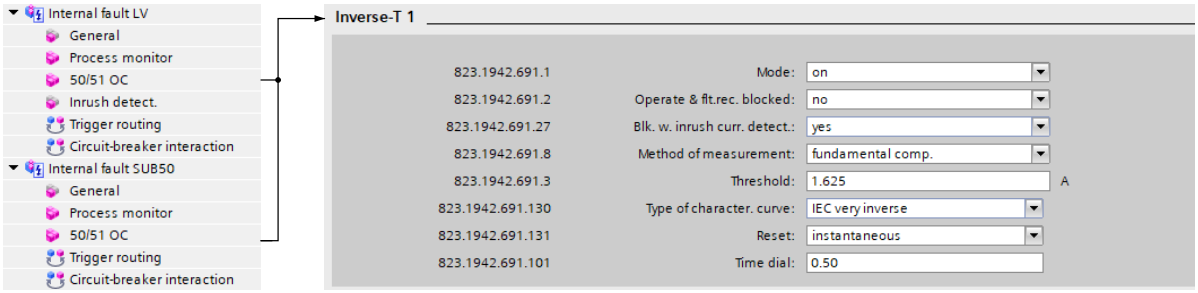


Figure 6.6: 7UM85 Device Configuration - FG Internal Faults

6.2.4. Protection Logic

The protection logic is configured using Continuous Function Charts (CFC) in DIGSI5 software.

The Loss-of-Mains tripping logic, responsible for opening the incomer's circuit breaker, is presented in Figure 6.7. The LOM TRIP signal becomes active only when all of the protection settings pick-up (ANSI81R, ANSI81O, ANSI78 and ANSI27-V1). If an overcurrent condition is detected at either one of the two outgoing feeders LV18-XFM or SUB50, the LOM TRIP signal is blocked.

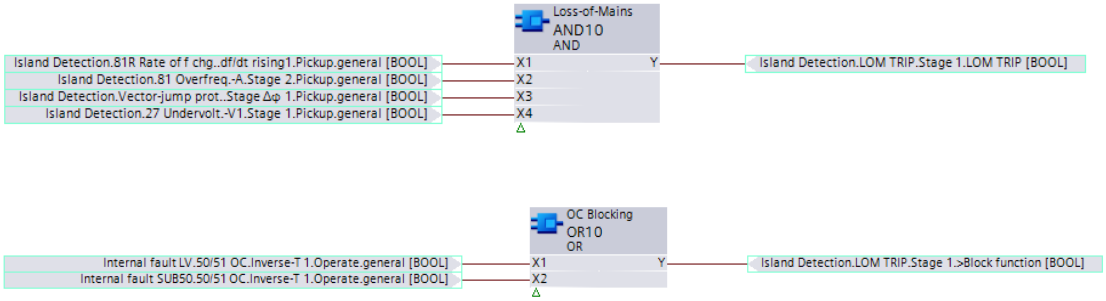


Figure 6.7: CFC Logic - Loss-of-Mains TRIP

The Load-Shedding tripping logic, responsible for opening the circuit breaker of generator GTG-201, is presented in Figure 6.8. The LSH TRIP signal becomes active only when all of the protection settings pick-up (ANSI81R, ANSI27-V1, ANSI81O) and the incomer's circuit breaker is in OPEN position.

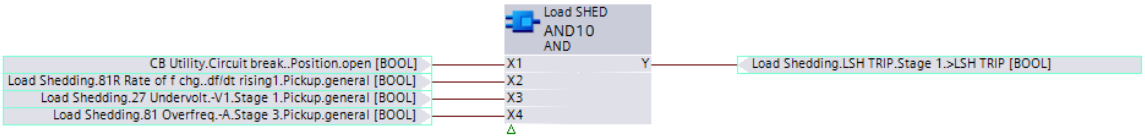


Figure 6.8: CFC Logic - Load Shedding TRIP

6.3. Omicron Testing

The physical setup, consisting of the Omicron CMC356+ device and the 7UM85 protection relay can be seen in Figure 6.9.

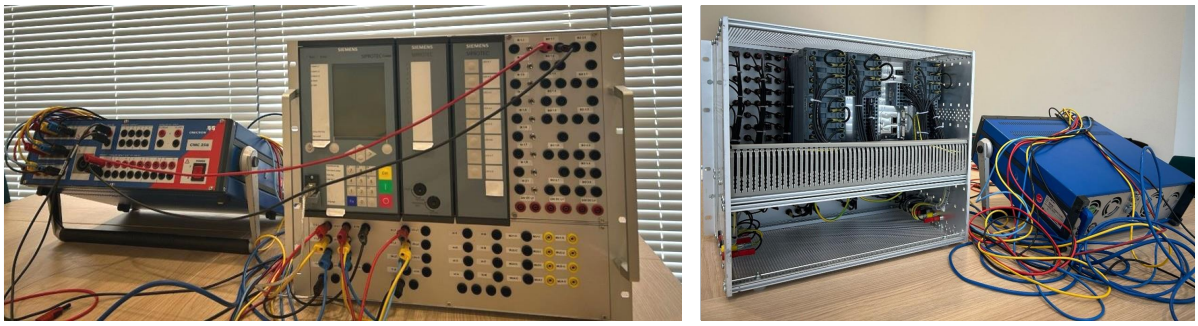
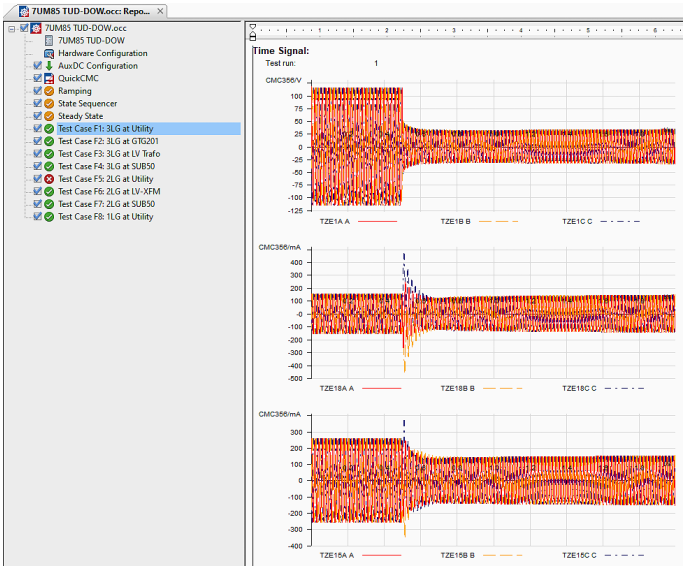
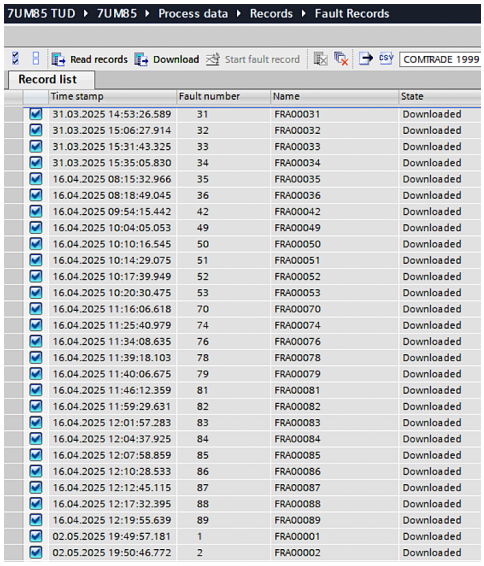


Figure 6.9: Omicron & 7UM85 hardware setup

The Test Cases exported from ATP-EMTP are imported into the Omicron Control Center file using the Advanced Transplay Module, as can be seen in Figure 6.10a. The Omicron will inject the same signal curve into the relay, no additional intervention is needed to replicate the fault scenario. The relay behavior under the test scenarios is then registered as a fault record in DIGSI5, as can be seen in Figure 6.10b and can be exported to be viewed and analyzed with SIGRA/ Comtrade Viewer.





Time stamp	Fault number	Name	State
31.03.2025 14:53:26.589	31	FRA00031	Downloaded
31.03.2025 15:06:27.914	32	FRA00032	Downloaded
31.03.2025 15:31:43.325	33	FRA00033	Downloaded
31.03.2025 15:35:05.830	34	FRA00034	Downloaded
16.04.2025 08:15:32.966	35	FRA00035	Downloaded
16.04.2025 08:18:49.045	36	FRA00036	Downloaded
16.04.2025 09:54:15.442	42	FRA00042	Downloaded
16.04.2025 10:04:05.053	49	FRA00049	Downloaded
16.04.2025 10:10:16.545	50	FRA00050	Downloaded
16.04.2025 10:14:29.075	51	FRA00051	Downloaded
16.04.2025 10:17:39.949	52	FRA00052	Downloaded
16.04.2025 10:20:30.475	53	FRA00053	Downloaded
16.04.2025 11:16:06.618	70	FRA00070	Downloaded
16.04.2025 11:25:40.979	74	FRA00074	Downloaded
16.04.2025 11:34:08.635	76	FRA00076	Downloaded
16.04.2025 11:39:18.103	78	FRA00078	Downloaded
16.04.2025 11:40:06.675	79	FRA00079	Downloaded
16.04.2025 11:46:12.359	81	FRA00081	Downloaded
16.04.2025 11:59:29.631	82	FRA00082	Downloaded
16.04.2025 12:01:57.283	83	FRA00083	Downloaded
16.04.2025 12:04:37.925	84	FRA00084	Downloaded
16.04.2025 12:07:58.859	85	FRA00085	Downloaded
16.04.2025 12:10:28.533	86	FRA00086	Downloaded
16.04.2025 12:12:45.115	87	FRA00087	Downloaded
16.04.2025 12:17:32.395	88	FRA00088	Downloaded
16.04.2025 12:19:55.639	89	FRA00089	Downloaded
02.05.2025 19:49:57.181	1	FRA00001	Downloaded
02.05.2025 19:50:46.772	2	FRA00002	Downloaded

(a) Omicron Control Center File

(b) Fault Records DIGSI5

Figure 6.10: Advanced Transplay Test Cases & Fault Records

6.3.1. Test Case F1

The fault record extracted from the protection relay can be seen in Figure 6.11. The incomer (CB Utility) receives the Trip/Open Command from the LOM TRIP at t= 190 ms. The generator (CB GTG201) receives the Trip/Open Command from the LSH TRIP at t= 428 ms. The fault record is triggered by the Undervoltage protection that picks up in 20 ms from the fault start.

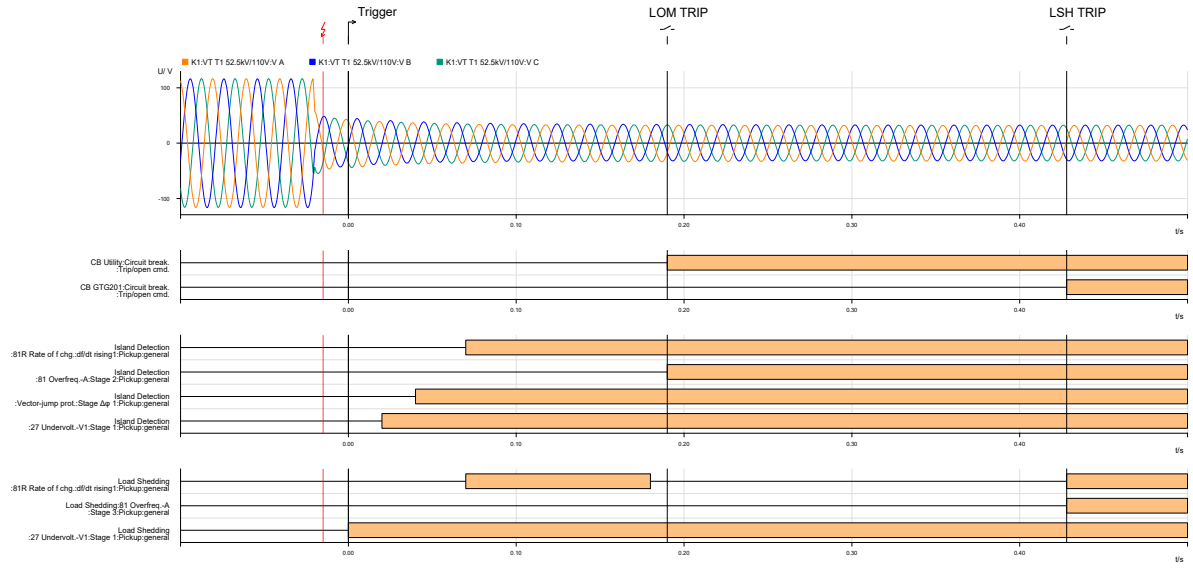


Figure 6.11: Test Case F1: 3LG at Utility

6.3.2. Test Case F2

The fault record provided in Figure 6.12 is triggered by the Undervoltage protection function. Due to the fault location and severity, the voltage at the MV busbar collapses to zero, thus the protection functions (ANSI81R, ANSI81O and ANSI78) are inactive (5% * Vmeasured validity threshold).

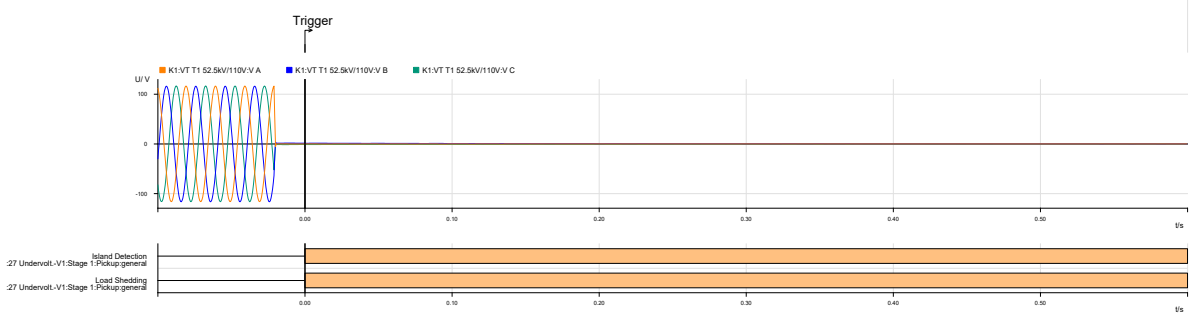


Figure 6.12: Test Case F2: 3LG at GTG-201

6.3.3. Test Case F3-F4

The fault record is provided in Figure 6.13 for both test cases F3 and F4, respectively. The trigger is given by Overcurrent protection in 5 ms from fault start. The voltage at the MV busbar collapses to zero, thus the islanding tripping logic is inactive.

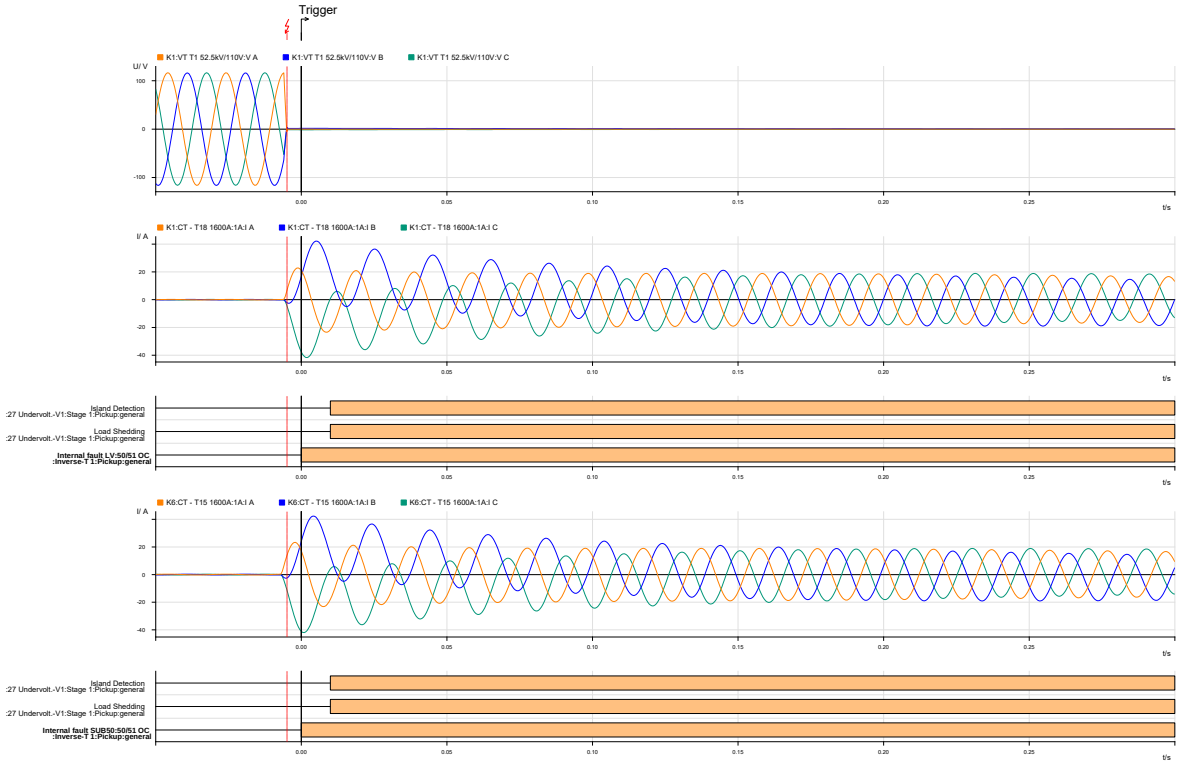


Figure 6.13: Test Case F3-4: 3LG at Outgoing Feeders

6.3.4. Test Case F5

The fault record is provided in Figure 6.14 and it can be seen that the LOM TRIP signal is issued at t= 1300 ms. The relay behavior for this test case is consistent with the protection logic developed in ATP-EMTP. The protections settings pick up after the CCT is passed.

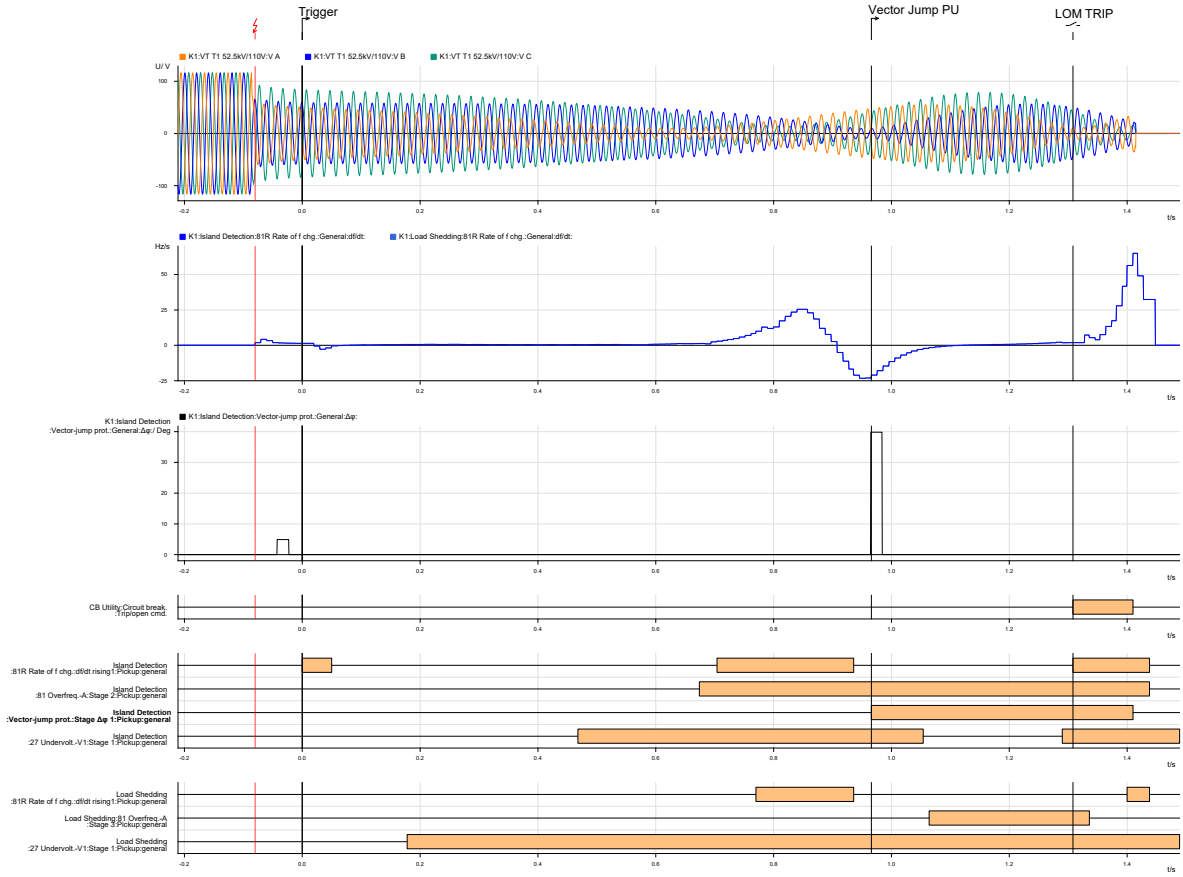


Figure 6.14: Test Case F5: 2LG at Utility

6.3.5. Test Cases F6-7

The fault record is provided in Figure 6.15 and the trigger is given by Overcurrent. No trip/ open command is issued to the incomer.

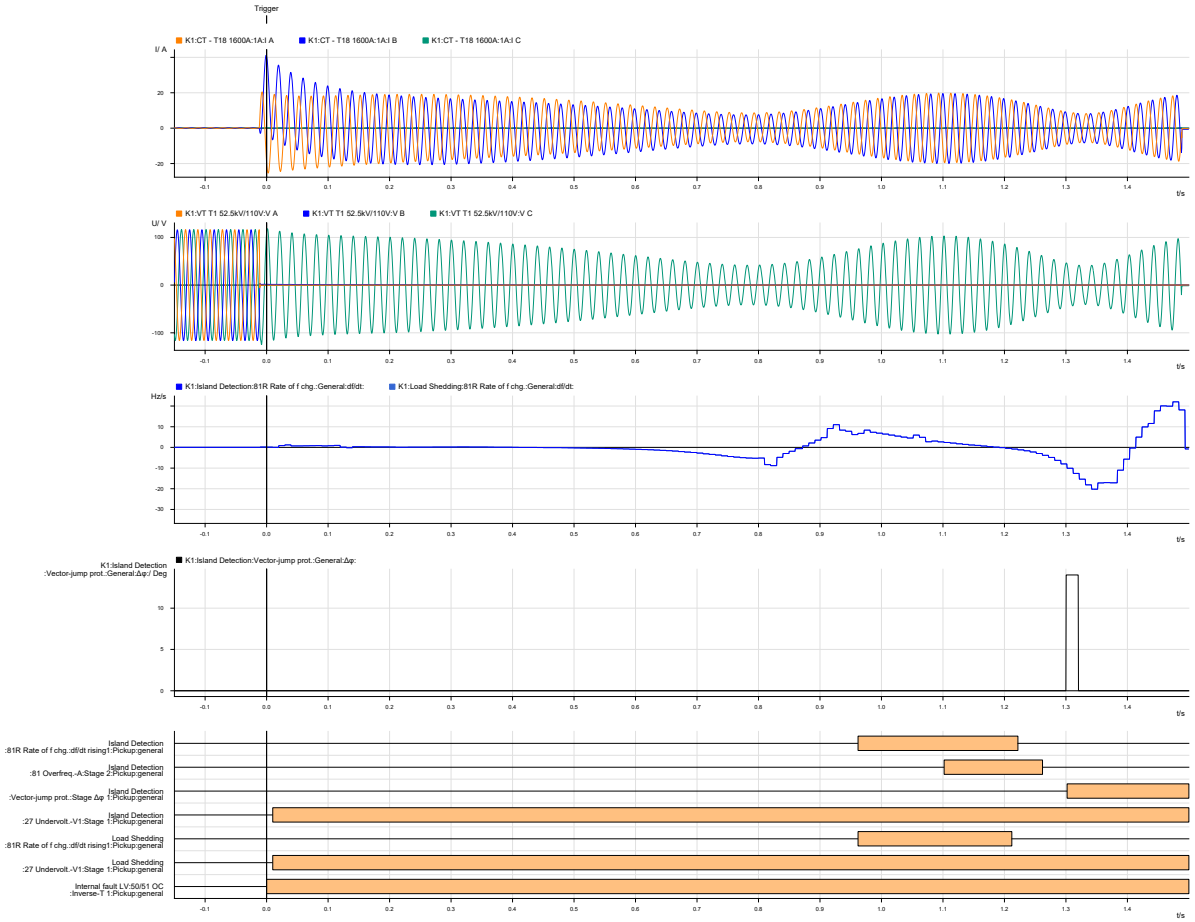


Figure 6.15: Test Cases F6, F7: internal 2LG fault

6.3.6. Test Case F8

The single-phase to ground fault doesn't trigger the fault record.

6.4. Results 7UM85

The test results are provided in Table 6.2.

Test Case	*LOM TRIP*	*LSH TRIP*	*Result*
F1	190 ms	LOM TRIP + 238 ms	Passed
F2	NO TRIP	NO TRIP	Passed
F3	NO TRIP	NO TRIP	Passed
F4	NO TRIP	NO TRIP	Passed
F5	1292ms	NO TRIP	**Failed**
F6	NO TRIP	NO TRIP	Passed
F7	NO TRIP	NO TRIP	Passed
F8	NO TRIP	NO TRIP	Passed

Table 6.2: Islanding Tripping Scheme Test Results

6.5. Results comparison

The protection scheme has been tested with both configurations: ATP-EMTP and SIPROTE5 Relay 7UM85. The results will be compared for the test cases that generate a trip signal: Test Case F1 and Test Case F5.

LOM Prot. Function	**PU Threshold**	**PU Time ATP**	**PU Time SIP**	**PU Value ATP**	**PU Value SIP**
ANSI81R: df/dt rising	1 Hz/s	79.5 ms	70 ms	5.2497 Hz/s	5.3135 Hz/s
ANSI27-V1: Stage I	65 % * Vrated	12 ms	20 ms	19.327 kV	82.326 V
ANSI810: Stage II	50.5 Hz	248 ms	190 ms	50.556 Hz	50.546 Hz
ANSI78: Vector-Jump	10 Deg	47.5 ms	40 ms	10.113 Deg	14.367 Deg
LSH Prot. Function	**PU Threshold**	**PU Time ATP**	**PU Time SIP**	**PU Value ATP**	**PU Value SIP**
ANSI81R: df/dt rising	2 Hz/s	455 ms	428 ms	4.0248 Hz/s	2.2145 Hz/s
ANSI27-V1: Stage II	85 % * Vrated	283.5 ms	17.3 ms	22.573 kV	82.326 V
ANSI810: Stage III	51 Hz	583 ms	428 ms	51.041 Hz	51.099 Hz

Table 6.3: Results comparison ATP/SIP Test Case F1

LOM Prot. Function	**PU Threshold**	**PU Time ATP**	**PU Time SIP**	**PU Value ATP**	**PU Value SIP**
ANSI81R: df/dt rising	1 Hz/s	100 ms	90.7 ms	1.3949 Hz/s	1.3303 Hz/s
		1.083 s	1.292 s	3.194 Hz/s	2.2238 Hz/s
ANSI27-V1: Stage I	65 % * Vrated	20 ms	1.272 s	20.818 kV	34.187 V
ANSI810: Stage II	50.5 Hz	965.5 ms	658 ms	50.641 Hz	50.602 Hz
ANSI78: Vector-Jump	10 Deg	711 ms	950 ms	10.006 Deg	43.745 Deg

Table 6.4: Results comparison ATP/SIP Test Case F5

Undervoltage protection function PU values are different between the model developed with ATP-EMTP and the 7UM85 Undervoltage function because the software model uses primary voltage (52.5 kV) while the relay uses secondary voltage (110V).

The differences in Vector-Jump pickup values are given by the fact that the relay uses a delta measurement for the vector shift and picks up on the maximum value. In the ATP model the same multi-cycle concept was intended, but the simulation results indicate the ATP Vector-Jump function picks up the moment the 10 Deg threshold is crossed, instead of waiting to compare shifts over three time-windows.

6.6. Discussion

The ATP simulation is dynamic, so when the Loss-of-Mains (LOM) circuit-breaker opens, the busbar voltage rises. The Undervoltage Model is configured to pick up when the voltage is greater than 5% but lower than 65%. After the incomer breakers are opened, the voltage rises and the second Undervoltage stage picks up when the voltage is greater than 65% but lower than 85%. In the relay, the Undervoltage Stages operate from the higher threshold to the lower one. So, with stages set at 85% Vrated and 65% Vrated, the relay transitions from the steady-state voltage to an 85% drop, then to a 65% drop. The different algorithm that the two functions use is the main reason for the differences between the ATP and the relay. Second, the Test Files replayed in the relay are static, so no changes take place when the incomer circuit-breaker opens. The absence of dynamic feedback is the second reason that the Undervoltage function behaves differently than the ATP study.

Overcurrent (OC) blocking is not relevant for the protection logic. During a three-phase fault, the busbar voltage collapses to zero, preventing both frequency and vector-jump calculations, so the associated protection functions cannot operate and no trip signal is sent. During a two-phase fault, sufficient voltage remains for these functions to operate, but because the functions are based on the positive sequence voltage they will not pick up during an unbalanced fault. If different protection functions are used to include unbalanced faults, the overcurrent blocking can be useful.

When comparing the relay test results with the expected pickup times stated in the relay manual, it was observed that RoCoF and Vector-Jump pickup in half the expected time. To identify the cause for the RoCoF function, four additional simulations were performed with the 7UM85 relay using the same fault signals and PU thresholds while varying the df/dt measurement window length from 2 to 5 periods. Results revealed that: df/dt calculations performed over a shorter measurement window (2–3 periods) delayed pickup to about 270 ms, whereas longer measuring-window calculations (4–5 periods) advanced pickup to approximately 70–100 ms. A shorter measuring window increases the PU time, due to the stabilization counter that needs to be exceeded for at least 8 half-cycles. Therefore the relay needs to calculate the df/dt at least twice to include 8 half-cycles. A longer measuring window of 5 periods only requires the df/dt to be calculated once, therefore the PU time can be as fast as 8 half-cycles (70-100 ms) if the threshold is exceeded over the entire measuring-window. However, the expected PU times stated in the manual start from 160 ms. Siemens has provided an explanation for the differences between the expected pickup time and the actual pickup time when performing dynamic testing: the continuous signals used to test the dynamic functions (RoCoF and vector-shift) do not trigger the stabilization counters of the relay's algorithm, thus the functions might pickup faster than the expected PU time. When testing RoCoF or Vector-Jump with the Ramping Module available in Omicron, the minimum timestep allowed is 1 ms, therefore the relay behaves as stated in the manual. When using the Advanced Transplay module, the signals are imported from the ATP-EMTP simulation, which uses a timestep of 50 micro-seconds, thus the stabilization counter is not triggered and the relay picks up faster than the value stated in the manual.

The ATP model of the RoCoF function was updated to use a 5-period measuring window and a stabilization counter of four half-cycles (instead of eight half-cycles as specified in the relay manual). With these adjustments the simulated RoCoF element reproduced the relay's pickup times within experimental tolerance, bringing the ATP-EMTP representation into close alignment with the physical device's performance.

7

Conclusion

7.1. Conclusion

The scope of the master thesis project was to optimize generator protection by developing an islanding tripping scheme that correctly identifies an islanding event, isolates the system from the faulty grid and ensures the island is stable.

Under normal operation, the power system exports active power to the grid and imports reactive power from the grid. During an islanding event, the active power generation exceeds the system's demand, and voltage instability occurs due to the loss of reactive support from the grid.

In order to identify an islanding event, the behavior of the power system under disturbances was studied. To realize this, the power system was dynamically modeled using the ATP-EMTP software and a Stability Analysis was performed. The stability analysis revealed that, for an external fault, the most critical type of fault (three-phase to ground) has the shortest critical clearing time (320 ms) when the machines operate at rated power output. **Therefore, the islanding tripping scheme needs to operate in less than 320 ms.**

Since the power system is connected to the utility grid, the Dutch NetCode was studied to identify the requirements for disconnection. It was concluded that during disturbances, the generators must remain connected to the utility grid for at least 200 ms (Fault-Ride Through time). **Therefore, the islanding tripping scheme should not operate faster than 200 ms.**

During this time, the control systems of the machines also respond to the fault. When the active power generation exceeds the demand, the generators start speeding up, and the overall frequency of the power system increases. The governor systems decrease the mechanical input to slow down the machines, while the excitation system increases the field current in order to increase the generator's terminal voltage, thus providing sufficient "decelerating" power for the rotor angles to remain synchronized to the system. These actions cause the system frequency to oscillate between 50.2 Hz and 50.5 Hz, until the system regains stability and the frequency returns to nominal. If the frequency continues to increase after the control systems have finished their response, the system must be disconnected from the grid. **Therefore, the islanding tripping scheme uses an Overfrequency threshold of 50.5 Hz to identify the end of the control response.**

Because the system needs to be disconnected before exceeding the critical clearing time, the frequency doesn't increase above 51.2 Hz, which is the Dutch NetCode threshold for disconnection from the utility grid. Therefore, the rate of change of frequency will be used to identify the severity of the fault. According to the Dutch NetCode, a rate of change of frequency above 1 Hz/s allows the generators to disconnect. **Therefore, the islanding tripping scheme uses rate of change of frequency protection with a df/dt threshold of 1 Hz/s.**

As mentioned, during an external fault the system loses the reactive support from the grid, causing the

voltage at the distribution level to drop. **Therefore, the islanding tripping scheme uses Undervoltage protection to identify the island.**

When the grid is lost, the equivalent load impedance increases, so the line current drops. Since the network/ source impedance remains the same, the voltage drop across the network impedance shrinks instantly. At this moment, the source voltage is unchanged so the measured voltage phasor moves from V to V'. This movement has a magnitude increase as well as a phase change. **Therefore, the islanding tripping scheme will use vector-jump protection to detect a sudden step change in the positive sequence voltage angle, identifying the moment that the grid is lost.**

When the islanding tripping scheme opens the incomer circuit breaker, the switching transient causes the frequency to drop, increasing the absolute value of the rate of change of frequency. Because the island is unstable (generation > load), the frequency rises above 51 Hz and the rate of change of frequency increases above 2 Hz/s. The load shedding scheme uses both of these values to identify the instability, as well as Undervoltage and the Open position of the incomer CB.

The Load Shedding signal disconnects one of the 2 generators and is sent further to the DCS for shedding non-critical load. Since the island operates with only one generator, the DCS uses the signal to swap the governor system from DROOP control to ISOC operation. To maintain the system grounded while in island mode, the DCS uses the signal to close the star point of the unit transformer of the generator left online.

This protection scheme was programmed in the 7UM85 relay using DIGSI5 software and tested with the Omicron CMC356+ using the Advanced TransPlay Module.

The protection scheme correctly identifies an islanding event and disconnects the system in the required time-frame. The protection scheme is only effective for balanced faults because it uses the positive sequence voltage to calculate the protection functions.

The protection relay 7UM85 behavior under the fault scenarios is not consistent with the expected behavior stated in the manual. The functions Vector-jump and RoCoF pickup in half the time mentioned in the manual. The conclusion is that when relay testing is performed using continuous signals, the stabilization counters that the relay uses for these dynamic functions can't be effectively triggered, thus the functions pickup faster than the expected pickup time.

7.2. Recommendations for future work

It is recommended to perform dynamic simulations in order to understand the power system behavior and to correctly test the protection logic under realistic fault scenarios.

Dynamic functions such as RoCoF and Vector-Jump should be used as part of a combined logic, because the pickup times are very fast (under 100 ms) and disconnection might occur before the desired tripping time.

When testing the relay, the Advanced TransPlay Module is a great tool for replicating realistic fault signals, as it can be used to import the signals from the dynamic simulations.

If Overcurrent blocking is used on an outgoing feeder that consists of a distribution transformer, inrush current detection and blocking should be considered to avoid false pickup of the Overcurrent protection.

When programming for a combined logic, the individual protection settings should not be routed to the circuit breaker interaction because different faults can trigger the same protection functions and the risk of false tripping is very high.

Further testing of protection settings should be performed to increase the reliability of the available protection devices by providing the required information to the relevant industries.

References

[1] Siemens AG. *SIPROTEC 5, Generator Protection, Manual*. 06.2025. Siemens AG, 2025.

[2] RadhaKiranMaye Anne et al. “Reliable generator islanding detection for industrial power consumers with on-site generation”. In: *IEEE Transactions on Industry Applications* 52.1 (2015), pp. 668–676.

[3] DOW Benelux. *DOW Netherlands*. 2025. URL: https://nl.dow.com/en-us.html.

[4] Rafal Bugdal et al. “Performance analysis of the ROCOF and vector shift methods using a dynamic protection modelling approach”. In: *15th International Conference on Power System Protection*. 2006, pp. 139–144.

[5] Dr. Tsu - huei Liu Dr. W . Scott Meyer. *Alternative Transient Program (ATP) Rule Book*. Oregon, USA: Canadian / American EMTP User Group, 2016.

[6] Alcedir Luis Finkler et al. “Challenges on the Use of Vector Shift Relays in Distributed generation: a Brazilian case study”. In: *Electric Power Systems Research* 204 (2022), p. 107688.

[7] Maciej Grebla, Jaya RAK Yellajosula, and Hans Kristian Høidalen. “Adaptive frequency estimation method for ROCOF islanding detection relay”. In: *IEEE Transactions on Power Delivery* 35.4 (2019), pp. 1867–1875.

[8] Francisco Peñaloza Hans Kristian Høidalen László Prikler. *ATPDraw User Manual*. version 7.5. Norway: NTNU, 2023.

[9] H.-J. Herrmann. “PRINCIPLES AND TECHNICAL SOLUTIONS OF DISCONNECTING COGENERATION PLANTS AND NETWORKS”. In: (2008).

[10] Siemens Power Technologies International. *Model Library PSS/E*. 34.7.0. NY, USA: Siemens Industry, Inc., Siemens Power Technologies International, 2019.

[11] Murali Kandakatla, Hannu Laaksonen, and Sudheer Bonela. “Advanced vector shift algorithm for islanding detection”. In: *CIRED 2015* (2015), pp. 15–18.

[12] Jan Machowski et al. *Power system dynamics: stability and control*. John Wiley & Sons, 2020.

[13] Juan A. Martinez-Velasco. *Transient analysis of power systems : a practical approach*. 1st ed. Barcelona, Spain: WILEY, 2020.

[14] Asad Mohammad et al. “How To Safely Island A Chemical Facility”. In: *2022 IEEE IAS Petroleum and Chemical Industry Technical Conference (PCIC)*. IEEE. 2022, pp. 457–464.

[15] DOW Netherlands. *Dow and TenneT explore the use of ELSTA power plant*. 2024. URL: https://nl.dow.com/nl-nl/news/intentieovereenkomst-voor-aanpak-netcongestie.html (visited on 12/10/2024).

[16] Overheid Netherlands. *Netcode elektriciteit*. 2025. URL: https://wetten.overheid.nl/BWBR0037940/2025-09-01#Hoofdstuk3 (visited on 04/05/2022).

[17] Ashish Upreti and Asad Mohammed. “Developments in System Islanding and Synchronization Systems”. In: (2022).

A

Source Code

```
1
2  MODEL Vjump -- Vector-Jump Protection Function Model
3
4  DATA
5    f_nom       {DFLT:50.0}    -- Nominal frequency [Hz]
6    fb_tol      {DFLT:3.0}     -- Frequency band tolerance [Hz]
7    Vect_Thrs   {DFLT:10.0}    -- Voltage Phase Angle shift threshold [deg]
8    T_block     {DFLT:0.1}     -- Blocking period after switching [s]
9    Vect_OpDel  {DFLT:0.01}    -- Operate delay [s]
10   Vect_TReset {DFLT:5}       -- Reset time [s]
11
12 INPUT
13   Theta   -- [deg] from Vmeter
14   Freq    -- [Hz]  from PLL Model
15
16 OUTPUT
17   Max_Delta    -- maximum angle jump
18   vect_pickup
19
20 VAR
21   T_cycle, delta1, delta2, delta3, max_delta
22   expected_shift, compensated_delta, n_cycles, temp_delta
23   vect_block, vect_pickup, vect_timer, vect_resetTimer
24
25
26 DELAY CELLS (THETA): 1/timestep
27
28 HISTORY
29   vect_pickup     {DFLT:0}
30   vect_timer      {DFLT:0.05}
31   vect_resetTimer {DFLT:0.08}
32   max_delta       {DFLT:0}
33   n_cycles        {DFLT:1}
34   theta           {DFLT: 0}
35   T_cycle         {DFLT: 1/f_nom}
36
37 INIT
38  vect_pickup := 0
39  vect_block  := 0
40 ENDINIT
41
42 EXEC
43
44
45   IF (Freq < (f_nom - fb_tol)) OR (Freq > (f_nom + fb_tol)) THEN
46       vect_block  := 1
47       vect_pickup := 0
48
49
```

```
  IF T < T_block THEN
      vect_block  := 1
      vect_pickup := 0
    ENDIF
   ENDIF

  IF Freq > f_nom AND Freq < (f_nom + fb_tol) THEN
    T_cycle := 1.0 / Freq

  IF Freq = f_nom THEN
    T_cycle := 1.0/ f_nom
  ENDIF
 ENDIF



  -- angle differences for 1, 2, 3 actual cycles

  delta1 := Theta - Delay(Theta, 1.0*T_cycle, 2)
  delta2 := Theta - Delay(Theta, 2.0*T_cycle, 2)
  delta3 := Theta - Delay(Theta, 3.0*T_cycle, 2)


  IF delta1 > 180 THEN delta1 := delta1 - 360 ENDIF
  IF delta1 < -180 THEN delta1 := delta1 + 360 ENDIF

  IF delta2 > 180 THEN delta2 := delta2 - 360 ENDIF
  IF delta2 < -180 THEN delta2 := delta2 + 360 ENDIF

  IF delta3 > 180 THEN delta3 := delta3 - 360 ENDIF
  IF delta3 < -180 THEN delta3 := delta3 + 360 ENDIF


  -- max angle diff

  max_delta := ABS(delta1)

  IF ABS(delta2) > max_delta THEN max_delta := ABS(delta2) ENDIF
  IF ABS(delta3) > max_delta THEN max_delta := ABS(delta3) ENDIF

  compensated_delta := max_delta - 360

 IF ABS(delta1) = max_delta THEN
   temp_delta := delta1
   n_cycles := 1.0
  ENDIF
  IF ABS(delta2) = max_delta THEN
    temp_delta := delta2
    n_cycles   := 2.0
  ENDIF
  IF ABS(delta3) = max_delta THEN
    temp_delta := delta3
    n_cycles   := 3.0
  ENDIF

   expected_shift := 360.0 * n_cycles
   compensated_delta := temp_delta - expected_shift


       -- Check threshold
 IF ABS(max_delta) > Vect_Thrs THEN
         vect_pickup := 1
 ENDIF

 ENDEXEC
ENDMODEL
```

```
MODEL ANSI81R -- ANSI81Rate of freq. change: df/dt rising MODEL
DATA

  f_nom        {DFLT: 50}     -- nominal frequency [Hz]
```

```
  Stab_Counter {DFLT: 8}      -- stabilization counter limit (8 half-cycles per relay manual)
  ncycle       {DFLT: 5}      -- measuring-window for dfdt calculation
  dfdt_thr     {DFLT: 1.5}    -- pick-up threshold [Hz/s]
  fb_tol       {DFLT: 3.0}    -- frequency band block (+/- nominal freq.)
  T_block      {DFLT: 0.5}    -- blocking period [s]
  T_Reset      {DFLT: 1.5}    -- if trip pending times out, reset
  dfdtR_DO     {DFLT: 0.1}    -- dropout differential [Hz/s]

INPUT
  Freq --from PLL Model

OUTPUT
  dfdt_trip
  dfdt_value

VAR
  ---------- For df/dt logic ----------
  freq_old, dfreq, dfdt_value, dfdt_window
  half_cycle_timer, half_cycle_count, dfdt_pickup
  T_cycle

  --------- For blocking and timers ----------
  block_flag
  latch_resetTimer

 ---------- final output latch ----------
  dfdt_trip, dfdt_DO

DELAY CELLS (Freq): 1/Timestep

HISTORY

  half_cycle_timer {DFLT:0.0}
  half_cycle_count {DFLT:0}
  dfdt_window      {DFLT: ncycle/f_nom}
  dfdt_pickup      {DFLT:0}
  freq             {DFLT: f_nom}
  freq_old         {dflt: f_nom}
  latch_resetTimer {DFLT:0.3}
  dfdt_trip        {DFLT:0}
  dfdt_value       {DFLT: dfdtR_DO}
  dfdt_DO          {DFLT: 0.1}
  T_cycle          {DFLT: 1/f_nom}

INIT
T_cycle := 1/f_nom
dfdt_window := ncycle * T_cycle
latch_ResetTimer := 0
ENDINIT

EXEC
  block_flag := 0
  IF T < T_block THEN
    block_flag := 1
  ENDIF
  IF (Freq < f_nom)  OR (Freq > (f_nom + fb_tol)) THEN
    block_flag := 1
  ENDIF
  IF (Freq > f_nom) AND (Freq < (f_nom + fb_tol)) THEN
    T_cycle := 1.0 / Freq
  ENDIF

  freq_old := Delay(Freq, dfdt_window, 2)
  dfreq := freq - freq_old
  dfdt_value := dfreq / dfdt_window

  half_cycle_timer := half_cycle_timer + Timestep

  IF half_cycle_timer >= (0.5 * T_cycle) THEN
    half_cycle_timer := half_cycle_timer - (0.5 * T_cycle)

```

```
  IF T > T_block AND ABS(dfdt_value) < (dfdt_thr - dfdtR_DO) THEN
    dfdt_DO := 1
    ELSE dfdt_DO := 0
  ENDIF

    IF ABS(dfdt_value) >= dfdt_thr THEN
      half_cycle_count := half_cycle_count + 0.5
    ELSE
      half_cycle_count := 0
    ENDIF
    IF half_cycle_count >= Stab_Counter THEN
      dfdt_pickup := 1
    ELSE
      dfdt_pickup := 0
      latch_resetTimer := 0
    ENDIF
  ENDIF

  IF dfdt_pickup = 1 THEN
    latch_resetTimer := latch_resetTimer + Timestep
    IF latch_resetTimer < T_Reset THEN
     dfdt_trip := 1
     ELSE dfdt_trip := 0
    ENDIF

  IF block_flag = 1 THEN
    dfdt_trip := 0
  ENDIF

 ENDIF
ENDEXEC
ENDMODEL
```

```
MODEL ANSI810 -- ANSI810 Overfrequency Protection Function

DATA
  f_nom         {DFLT: 50}     -- Nominal frequency [Hz]
  fb_tol        {DFLT: 3.0}    -- Frequency band block (+/- nominal freq)
  OF_1          {DFLT: 0.2}    -- Stage 1 threshold: fnom + 0.2 Hz
  OF_2          {DFLT: 0.5}    -- Stage 2 threshold: fnom + 0.5 Hz
  OF_3          {DFLT: 1.0}    -- Stage 3 threshold: fnom + 1.0 Hz
  DO            {DFLT: 0.1}    -- Dropout diff for ALL stages (Hz)
  Stab_Counter  {DFLT: 8}      -- Stabilization counter limit (8 half-cycles as per relay
      manual)
  T_block       {DFLT: 0.5}    -- Initial block period [s]
  T_Reset       {DFLT: 1.5}    -- Auto-reset time [s]

INPUT
  Freq --from PLL Model

OUTPUT
  OF1, OF2, OF3     -- Overfrequency stage PU signals

VAR
  stage1_thr, stage2_thr, stage3_thr
  stage1_DO, stage2_DO, stage3_DO
  block_flag
  half_cycle_timer, T_cycle
  OF1_count, OF2_count, OF3_count
  OF1_latch, OF2_latch, OF3_latch
  latch_resetTimer
  OF1, OF2, OF3

HISTORY
  half_cycle_timer  {DFLT:0.0}
  OF1_count         {DFLT:0}
  OF2_count         {DFLT:0}
  OF3_count         {DFLT:0}
  OF1_latch         {DFLT:0}
  OF2_latch         {DFLT:0}
  OF3_latch         {DFLT:0}
```

```
  latch_resetTimer  {DFLT:0.0}
  T_cycle           {DFLT:1/f_nom}
  OF1               {DFLT:0}
  OF2               {DFLT:0}
  OF3               {DFLT:0}

INIT
  stage1_thr := f_nom + OF_1
  stage2_thr := f_nom + OF_2
  stage3_thr := f_nom + OF_3
  stage1_DO  := stage1_thr - DO
  stage2_DO  := stage2_thr - DO
  stage3_DO  := stage3_thr - DO
  T_cycle := 1.0 / f_nom
  OF1_count := 0
  OF2_count := 0
  OF3_count := 0
  OF1_latch := 0
  OF2_latch := 0
  OF3_latch := 0
ENDINIT

EXEC
  block_flag := 0

  -- Block for startup and out-of-band frequency
  IF T < T_block THEN
    block_flag := 1
  ENDIF
  IF (Freq < f_nom) OR (Freq > (f_nom + fb_tol)) THEN
    block_flag := 1
  ENDIF

  -- Update cycle duration (for half-cycle logic)
  IF (Freq > f_nom) AND (Freq < (f_nom + fb_tol)) THEN
    T_cycle := 1.0 / Freq
  ENDIF

  -- Half-cycle timing
  half_cycle_timer := half_cycle_timer + Timestep
  IF half_cycle_timer >= (0.5 * T_cycle) THEN
    half_cycle_timer := half_cycle_timer - (0.5 * T_cycle)

    -- Stage 1 logic
    IF (Freq > stage1_thr) AND (Freq < stage2_thr) THEN
      OF1_count := OF1_count + 0.5
    ELSE
      OF1_count := 0
    ENDIF
    IF OF1_count >= Stab_Counter THEN
      OF1_latch := 1
      latch_resetTimer := 0
    ENDIF

    -- Dropout logic stage 1
    IF (OF1_latch = 1) AND (Freq < stage1_DO) THEN
      OF1_latch := 0
      OF1_count := 0
    ENDIF

    -- Stage 2 logic
    IF (Freq > stage2_thr) AND (Freq < stage3_thr) THEN
      OF2_count := OF2_count + 0.5
    ELSE
      OF2_count := 0
    ENDIF
    IF OF2_count >= Stab_Counter THEN
      OF2_latch := 1
      latch_resetTimer := 0
    ENDIF

```

```
    -- Dropout logic stage 2
    IF (OF2_latch = 1) AND (Freq < stage2_DO) THEN
      OF2_latch := 0
      OF2_count := 0
    ENDIF

    -- Stage 3 logic
    IF (Freq > stage3_thr) AND (Freq < (f_nom + fb_tol)) THEN
      OF3_count := OF3_count + 0.5
    ELSE
      OF3_count := 0
    ENDIF
    IF OF3_count >= Stab_Counter THEN
      OF3_latch := 1
      latch_resetTimer := 0
    ENDIF

    -- Dropout logic stage 3
    IF (OF3_latch = 1) AND (Freq < stage3_DO) THEN
      OF3_latch := 0
      OF3_count := 0
    ENDIF
  ENDIF

  -- Output assignment and auto-reset timer
  IF (OF1_latch = 1) OR (OF2_latch = 1) OR (OF3_latch = 1) THEN
    latch_resetTimer := latch_resetTimer + Timestep
    IF latch_resetTimer >= T_Reset THEN
      OF1_latch := 0
      OF2_latch := 0
      OF3_latch := 0
      OF1_count := 0
      OF2_count := 0
      OF3_count := 0
      latch_resetTimer := 0.0
    ENDIF
  ENDIF

  -- Blocking overrides everything
  IF block_flag = 1 THEN
    OF1_latch := 0
    OF2_latch := 0
    OF3_latch := 0
    OF1_count := 0
    OF2_count := 0
    OF3_count := 0
    latch_resetTimer := 0.0
  ENDIF

  -- Outputs
  OF1 := OF1_latch
  OF2 := OF2_latch
  OF3 := OF3_latch

ENDEXEC
ENDMODEL
```

```

MODEL ANSI27 -- ANSI27 Undervoltage protection function MODEL

DATA
VLL {DFLT: 53.5}    -- Positive Sequence Voltage input [kV]
UV0 {DFLT: 0.1}     --min required voltage 5-10 % * VLL
UV1 {DFLT: 0.65}    --Stage 1 UV threshold VLL percentage %
UV2 {DFLT: 0.85}    --Stage 2 UV threshold VLL percentage %
T_block {DFLT:0.5}  --Blocking period [sec]

INPUT

VLL1 --positive sequence line-to-line voltage from Vmeter

```

```
OUTPUT
stage1, stage2

VAR
stage1, stage2, U0, U1, U2

HISTORY
U0 {DFLT:0}
U1 {DFLT:0}
U2 {DFLT:0}


INIT
  U0 := VLL * UV0
  U1 := VLL * UV1
  U2 := VLL * UV2
  stage1:=0
  stage2:=0

ENDINIT

EXEC
stage1:=0
stage2:=0

 IF T > T_block AND VLL1 > U0 AND VLL1 < U1 THEN
   stage1 := 1

  ENDIF

  IF T > (T_block + 0.05) AND VLL1 > (U1 + 0.02) AND VLL1 < U2 THEN

   stage2 := 1

 ENDIF

ENDEXEC
ENDMODEL
```