Super-growth of CNTs based on ZrN for TSV application

Sourish Banerjee

TU Delft
Delft University of Technology

Delft Institute of Microsystems and Nanoelectronics
dimes

Challenge the future

SUPER-GROWTH OF CNTs BASED ON ZrN FOR TSV APPLICATION

MASTERS THESIS

BY

SOURISH BANERJEE
BORN ON THE 24TH OF JUNE 1988 IN KOLKATA, INDIA

10TH APRIL, 2014

SUPERVISORS:

DR. R. ISHIHARA
DR. S. VOLLEBREGT
PROF. DR. P.M. SARRO

DELFT UNIVERSITY OF TECHNOLOGY
FACULTY OF ELECTRICAL ENGINEERING, MATHEMATICS AND COMPUTER SCIENCE
DELFT INSTITUTE OF MICROSYSTEMS AND NANOELECTRONICS
LABORATORY OF ELECTRONIC COMPONENTS, TECHNOLOGY AND MATERIALS

DELFT UNIVERSITY OF TECHNOLOGY
DEPARTMENT OF MICROELECTRONICS

The undersigned hereby certify that they have read and recommend to the Faculty of Electrical Engineering, Mathematics and Computer Science for acceptance of the thesis entitled "Super-growth of CNTs based on ZrN for TSV application" by Sourish Banerjee in partial fulfillment of the requirements for the degree of Master of Science.

Dated: 10th April, 2014

Chairperson:

....
prof. dr. P. M. Sarro

Advisor:

....
dr. R. Ishihara

Committee Members:

....
prof. dr. G. C. A. M. Janssen

....
dr. S. Vollebregt

Acknowledgements

This thesis is a result of a year of research work performed as a part of my MSc. curriculum. Although officially I am the author of this, but without the contribution of several people, the thesis would not have seen the light of completion. Indeed, a research work is never successful without the active participation of a group of enthusiastic people, who think alike.

I would first like to thank the members of my MSc. thesis committee, prof. dr. P. M. Sarro, dr. R. Ishihara, prof. dr. G.C.A.M. Janssen and dr. S. Vollebregt, for taking the time and pain to evaluate this report, and participate in the defense.

The list of acknowledgement would start by thanking my direct supervisor, dr. Ryoichi Ishihara. Thank you for giving me the opportunity to do a summer internship first, and then this MSc. thesis in the TFT group under your supervision. You had always been a very easy-to-approach professor, and had unlimited patience in tolerating my crazy ideas, and also the occasional delays during this work.

The name which closely follows is my student supervisor, dr. Sten Vollebregt. Without your help and support, in virtually every stage of the thesis, I would have been nowhere this day. Your lively spirit, sense of discipline, and dedication to the work had been a constant source of inspiration to me. It was a great experience to have worked with you Sten! Wish you the best for your Post-Doc carrier!

An experimental work like this could have never been achievable without the support of the DIMES Technology Center, and I would like to give my sincere thanks to all the engineers and staff members. Especially, I would like to thank Hugo Schellevis and Silvana Milosavljevic for training me in IC processing, Johan van der Cingel for his sincere efforts in keeping the BlackMagic running, Gregory Pandraud for his direct involvement in fabricating the final IC-prototype for this thesis, Mario Laros for his commitments to maintain the (problematic) SEM at all times and fixing it a.s.a.p. whenever it was down, Tom Scholtes for his sense of discipline and supervision in the cleanroom, Wim Wien for keeping the evaporator up and running, Jan Cornelis Wolff for fabricating the masks, Michiel van der Zwan for the technical discussions, Peter Swart for helping with the electrical measurements, and Wim Tiwon for catering to all the computer and IT problems.

Life would never have been better without the company of friends and colleagues, who kept a wonderful atmosphere in the ECTM group! Thanks to all the members of the TFT group (for the nice barbecues and coffee-corner discussions), the MEST group (for organizing the Nanoelectronics symposium) and all the students of ECTM. However, I would like to specifically thank Fabio (the 'chill-out' dude), Bruno (the 'helpful' dude) and once again, Gregory (the 'c'est la vie' dude)! You had made a special effort to keep the spirits high, during the long no-result periods. Thanks also to my friend and office-mate Dhariyash, former and current house-mates (Andy, Amit, Maulik, Kollol, Genani and Joy), and the Couchsurfing community of Delft, for all the fun we had!

Finally, I would give sincere thanks to my parents and grandparents for their uncompromising guidance and support, whenever I needed them.

Sourish Banerjee
Delft, April 2014

Abstract

Semiconductor technology is a fast-evolving field. It progresses from one technology to the next, in order to pack in more and more transistors in the chip, with the aim of increasing performance and reducing prize. However, this comes at a cost. With the successive down-scaling, the delay of interconnects increases. To avoid this and other present technological problems, the 3D-integration technology is a viable solution. Moreover, the standard interconnect material (copper) is predicted to give an increasing number of problems with future technology nodes. The carbon nanotube (CNT) is a material that has the potential to replace copper. In this thesis, we have investigated the growth of CNT by chemical vapor deposition process, on a new substrate combination (Fe/ZrN) that has the potentiality to support super-growth of CNT. We intend to use our technology to integrate CNT as through-silicon vias (TSV) in a 3D-integrated circuit.

This thesis is organized into seven chapters. In chapter 1, a brief overview on interconnect technology will be given, and we will justify the use of CNT as a replacement for Cu. We will further detail about the CVD growth process, and see how the substrate combination plays an important role in determining the CNT growth height. We will then motivate the selection of the novel Fe/ZrN combination for high growth lengths. However, this material combination will be found to give several problems with the standard CVD growth recipes. For this we are going to re-design the recipes by a design of experiments (DOE) approach.

In chapter 2, we will compare the different DOE methods available in literature and then select the Taguchi method, due to its advantages in our experiments. This method will further be used to generate an optimum recipe for super-growth of CNT. We will also study the theory behind this method, and finally, briefly consider another statistical tool, which can be used to optimize many recipes at the same time.

Chapter 3 will show us the first growth results with the Taguchi recipes. CNT growth will be performed on continuous, un-patterned catalyst layers. We will thoroughly analyze these results, and try to understand how the different growth conditions have played their role in CNT growth. We will then verify the Taguchi-optimized recipe, and see that it is successful in growing CNT bundles of almost a millimeter height. We will also comment on how the catalyst layer thickness still remains a sensitive growth parameter.

CNT growth on patterned catalyst islands will be investigated in chapter 4. We will first standardize a cleanroom procedure for patterning the catalyst layer, and then look at the CNT growth results. We will observe how the growth is affected by the size and distribution of the catalyst islands; and then have a detailed analysis, to understand this effect. Finally a Taguchi-generated recipe will be used to uniformly grow CNT bundles on the islands.

In chapter 5, the electrical properties of CNT will be studied. Starting with a brief discussion about electron transport through CNT, we will analyze two equivalent circuit models, using which, the CNT resistance can be calculated. In order to calculate the resistivity of our growth samples, a simple model will then be developed.

Chapter 6 will deal with the aim to minimize the CNT resistivity. First, we will physically characterize our growth samples by different measurement methods, and then use the results to calculate their resistivity, with our developed model. We will find that the values are orders lower than resistivity of copper. In order to improve this, a Taguchi analysis will be performed, in an attempt to increase the density and quality of the CNT samples, and the results will be discussed.

In the final chapter 7, we will be using our knowledge of CNT growth mechanism, and attempt to integrate CNT as a TSV in a 3D-IC prototype. We will discuss about the growth results, and recommend ways in which the process can be made successful in the future.

Contents

Chapter 1

Introduction and background work

1.1 Scaling down in IC-technology: An interconnect perspective

The driving force behind majority of research in the semiconductor industry today still follows the Moore's Law. Formulated back in 1965, it states that the number of transistors in a given area of a chip approximately doubles every two years. Undoubtedly, the motivation for this is to pack an increasing number of transistors in a given chip area, thus bringing the cost of production down. This means that the transistor sizes aggressively scale down over different generations of semiconductor technology. As added benefits to this, their speed of operation increases and power consumption decreases.

The situation, however, is not so bright for interconnects [1]. Reduction in dimension causes increase in their RC-delay, which means that a signal takes an increasing amount of time to propagate through a given distance. The delay is proportional to the interconnect length. This effect is already severe for global interconnects [2], which are long transmission lines connecting different areas of a chip. The delay problem was not so much of a concern until the mid-1990s, and semiconductor industries were happily scaling down technology. Unfortunately we are now at a time, where the interconnect delay has surpassed the logic delay by a significant margin (fig. 1.1). One more concerning factor is the increase in power consumption by interconnects as they scale down [3], leading to increased heat dissipation eventually. This can have serious implications on their lifetime. According to ITRS 2012 [4], at present the interconnect length in a high-end IC is 4.167 Km/cm², and is predicted to double by the year 2020! All these facts mean that unless some significant technological improvement is made in the interconnect side, further scaling down will only be detrimental to the device performance.
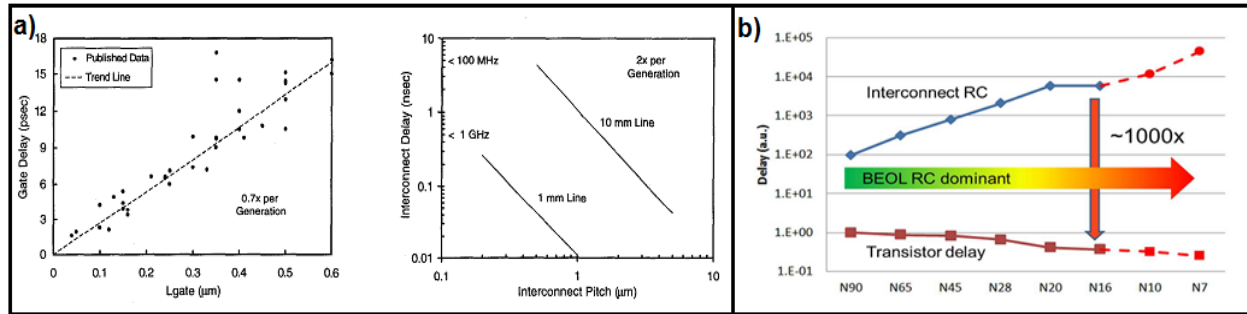
Figure 1.1: Logic delay versus interconnect delay between a gap of eighteen years: (a) State-of-the-art technology of Intel in 1995 (IEDM '95) already showing higher delay of interconnect than gate [1]; (b) Eighteen years since, a publication from Qualcomm (IEDM '13) predicts worsening of the trend [5].

To address some of these issues, the industry in 1997 decided to shift from aluminum to copper as the interconnect material [6], primarily because copper has a lower resistivity. At a similar time, low-dielectric materials were also beginning to be considered in place of SiO_2, which had been the standard [7]. This has been the industry norm for almost two decades now. Fig. 1.2 represents the interconnect scaling trend discussed so far.
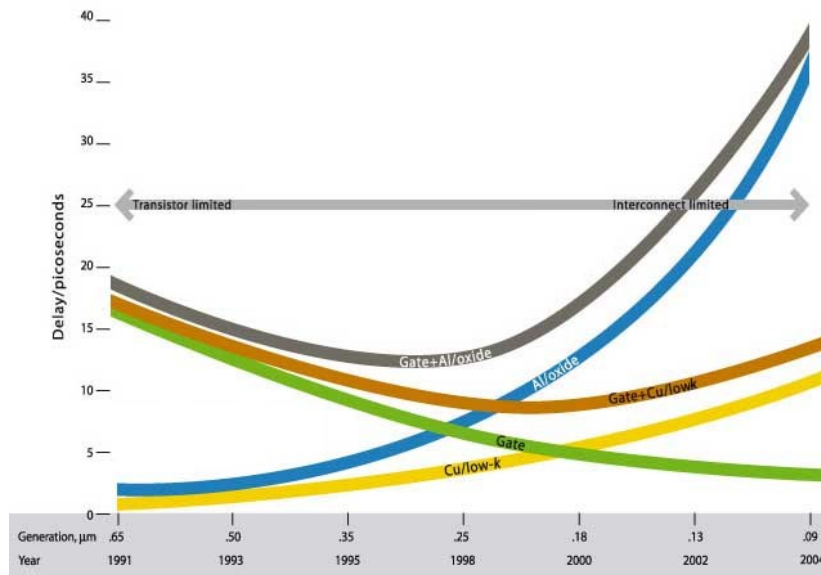
Figure 1.2: Different interconnects and dielectric materials used by the industry, and their performances at the various technology nodes [7]. The gate performance is given for reference. At present, we are far into the interconnect-limited regime.

With continuous downscaling, problems with copper have already begun to surface as well. The most concerning one is the increase in resistivity at small dimensions, due to grain boundary and surface boundary scatterings [8]. Indeed, resistivity is expected to increase to almost four times of the bulk value for the present 22 nm node technology [9]. In the process side, the big disadvantage that Cu has, is its tendency to diffuse into the neighboring electronics. To prevent this, a barrier layer is required; which implies that this layer also needs to be scaled down with each technology, a difficult task for most dielectric materials. Further the downscaling has been causing an increase in the current density. This again poses a limitation on the use of Cu, as it is prone to suffer from reliability issues at these high current density levels [10].

1.1.1 Move to 3D-IC technology and problems faced with Cu interconnects

In order to address the worsening issues of interconnect delay, the fast-approaching resolution limits of fabrication instruments and the physical limits of process conditions, the industry has been focusing on 3D-integration for the last few years [11-13]. 3D-integration is a simple concept of stacking chips one over the other, to pack more transistors in a given area, while keeping their dimensions constant. This offers two advantages: not only the fabrication instruments can be used for a longer period of time (before their resolution 'runs out'), but the interconnect lengths can also be shortened, hence reducing the delay. This technology has a lot of promise as the future of the semiconductor industry, since, by creating the extra dimension, it solves a lot of technological problems of each nm-node; and is thus expected to keep Moore's law running. The second advantage it promises, is the possibility to integrate different functionalities in the same chip. For instance, a chip may be packed with a multitude of functionalities like sensors/actuators, antennas, power devices, passives and I/O capability, in addition to the existing electronics. This new trend of diversifying the functionalities of a chip is termed as More-than-Moore.

3D integrated circuits can be made either by chip-stacking or by monolithic integration [14, 15]. In chip stacking, two or more pre-fabricated dies are bonded on top of each other, and they are connected by through-silicon-vias (TSV) (fig. 1.3b, c). A TSV is basically a hole etched through the bulk of a die, through which the interconnect 'connects' the top and the bottom dies. The other type of approach is monolithic integration, where transistors are fabricated in the bulk of a wafer in different layers, with short interconnections (vias) between them (fig 1.3d). As clear from the figure, this technology offers the highest level of integration of transistors.
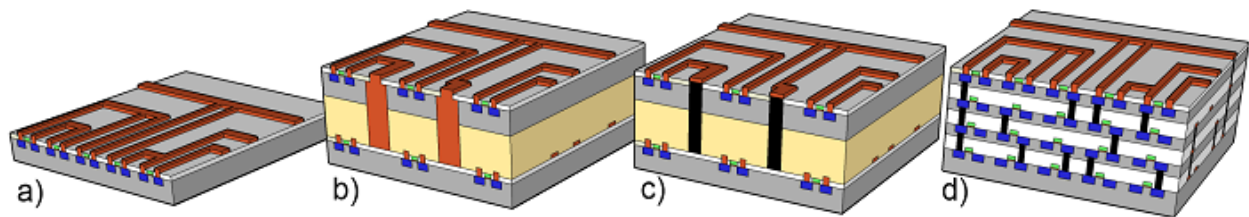
Figure 1.3: Current and future integrated circuits: (a) Conventional planar 2D technology; (b) 3D stacked IC with copper TSV; (c) Same IC with CNT-based TSV; (d) Monolithic 3D-IC showing dense network of transistors and vias. Source: [52].

The 3D-integration is a promising technology and is under considerable research attention. However, there are several problems that need to be addressed before its actual commercialization. For monolithic integration, stacking and isolating transistors on top of each other is a challenge; so is the fabrication of high-aspect-ratio (HAR) vias. Use of copper as via material creates problems as well. Process-wise, filling TSV with an aspect ratio greater than 10 is a major difficulty, and often leads to incomplete and non-uniform fills [16]. To solve this, the TSV needs to be widened at the cost of transistor space. Further the risk of contamination to neighboring electronics increases, as the vias are placed much closer to each other [17]. Finally, 3D-integration suffers from a major problem; that of heat dissipation. At present, VLSI chips tend to operate several degrees above room temperature. Packing many more transistors into the same volume would result in a huge increase in power dissipation, worsening the situation. There could be severe problems from difficulty in thermal management, as the heat from the middle layers would have no way of escaping. The vias would then have to transport the heat out of the system. Even though copper does have a high thermal conductivity, it also has a high coefficient of thermal expansion, compared with silicon. This mismatch would also lead to formation of internal stresses and cracks, thereby compensating with the reliability once again.

All these technological problems have led the industry to consider using materials other than copper. These materials are termed 'novel-materials' and are a subject of frantic research activity. As usual, research on improving the existing Cu-technology is still being carried out; but looking at the many recent ITRS predictions [4, 18, 19] it is becoming clear that the industry is encouraged to actively research on new materials as well. The most researched materials include metallic or semiconducting nanowires, nanocomposites, and carbon allotropes like carbon nanotube (CNT) and graphene. In this thesis work, the carbon nanotube has been the subject of our research.

1.2 Carbon nanotubes for TSV application

The CNT offers exceptional promise as interconnect material, and is being widely researched for more than a decade, by universities and industries alike. The plethora of publications available on this topic is evidence to this fact. CNT has some excellent inherent physical properties which, if utilized optimally, can solve a major share of the interconnect problems in 3D-integration technology.

Firstly, for the fabrication of low resistance, high aspect ratio, through-silicon-vias (HAR-TSV), CNT could be an excellent option [20-23]. A single nanotube has a diameter of only a few nanometers, but may have a length of micro- or even millimeters, which means an aspect ratio of thousands to millions! This feature comes to great advantage in the process side, as CNT can be grown vertically in deep vias. So for the HAR interconnects, where Cu-filling is a problem, CNT can be used. Another advantage closely associated with this is, CNT poses lesser contamination threats compared to copper. Secondly, in the material side, CNT offers excellent electrical conduction. Short CNT, which are a few nm long, are known to offer ballistic electron transport, which means that they have a constant resistance that does not depend on the length. At these regimes, CNT far outperforms copper electrically. Besides, it can tolerate exceptionally high current densities of the order of 10^9 A/cm^2, almost three orders of magnitude higher than copper, which holds true even at higher temperatures [24]. These properties are especially useful for short vias in the monolithic technology. Simulations have shown that even at large length scales, vias of high quality CNT can have lower resistivity than copper (as discussed in Chapter 6). Finally, another crucial advantage is the exceptionally high thermal conductivity of CNT, with measured values reaching up to 3500 W/mK [25], almost nine times higher than copper. This also strongly motivates the use of CNT for 3D-ICs, as a better way to conduct the heat out of the chip. All these properties make CNT a very interesting candidate for via material.

There are a few shortcomings as well. Primarily, all the facts discussed above stand for individual, high quality nanotubes. However, performance decreases sharply when we shift from an individual CNT to a bundle of CNT. Maintaining the superior properties is then a challenge. Also, the mass-production of high quality CNT bundles is not an easy task either. Further, as the CNT-technology is still under development, the growth conditions are not standardized, which often results in a large variation of the properties for the different conditions. Finally, the prospect of using CNT specifically for TSV applications requires them to be hundreds of microns long, whereas research has focused so far mostly on short, a few-micrometers-long CNT material. Thus, it is clear that a lot of research work is still needed before standardizing CNT for interconnect materials, and this thesis is a tiny step in that direction.

1.2.1 CNT growth by chemical vapor deposition

The first widely reported identification of CNT was done by Sumio Ijima (NEC Corporation, Japan), when he accidentally synthesized the material by an arc-discharge method [26]. After that, the laser-ablation [27] and CVD processes [28] were also developed for CNT growth. Since this thesis has only worked with CVD-grown CNT, the first two methods will not be discussed.

CNT growth by the CVD process requires three ingredients: the precursor gas (also called feedstock), a catalyst surface, and a source of energy. The energy source may be generated thermally or by plasma; accordingly plasma-enhanced CVD (PECVD) or thermal CVD (TCVD) can both be used. We prefer using TCVD for our process (as CNT is prone to be damaged by the plasma [29] which reduces their electrical performance). Further the growth takes place at low pressures, in the order of mbar, which classifies our CVD process as thermally-assisted LPCVD. From here on, our discussions will be based on this kind of CVD system. In a nutshell, the essence of CVD CNT growth is, the precursor gas diffuses onto the catalyst surface, and if the right energy condition is available, it breaks down into elemental carbon, depositing as a nanotube on the catalyst.

The catalyst layer does this job of breaking down the feedstock gas. Transition elements like Fe, Co and Ni [30-32] are the most popular choice as catalysts, however Pd, Pt, Cu or Au are also used occasionally [33, 34]. The catalyst is deposited as a thin film of a few nanometers, and is itself unable to initiate the reaction. The film has to be first activated by heat treatment. When exposed to heat, the continuous layer breaks down into lumps of nanoparticles by minimization of the surface energy. This process is known as catalyst activation or annealing. The precursor gas, which is usually a lower order hydrocarbon, is now introduced into the CVD chamber under the right pressure. Occasionally an inert carrier gas may also be used in conjunction. CH_4, C_2H_4 and C_2H_2 are the most preferred precursors for the purpose of CNT growth [35-37]. The carrier gas also serves as an etchant for the excess amorphous carbon that may be deposited, reconverting it into hydrocarbon. The precursor then diffuses onto the surfaces of the nanoparticles. If the right temperature is available, then it undergoes a series of reaction with the nanoparticles, ultimately breaking down into elemental carbon, which deposits (or nucleates) on the nanoparticle surface. Due to surface energy minimization again, the layer of carbon atoms fold up to form a nanotube. This marks the growth of the CNT. Additional molecules of the precursor diffuse on the catalyst seed and nucleate into carbon atoms, which then attach to the growing CNT front. In the growth process, the reaction may either start from the top surface or the bottom surface of the nanoparticle. In the first case, the catalyst stays at the bottom, with a CNT growing upwards from it (base-growth); while in the second case, the CNT itself pushes the nanoparticle upwards, which then stays on top of the growing CNT (tip-growth). Fig. 1.4 illustrates the growth process of a CNT in a conceptual manner.
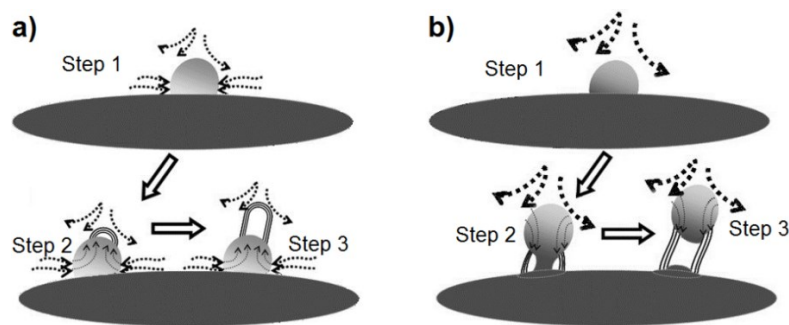
Figure 1.4: Growth mechanism of CNT: (a) Base-growth; (b) Tip-growth. Source: [38].

The different CVD growth conditions largely govern the properties of the CNT. Table 1.1 qualitatively shows how the CNT growth rate, density and quality depend on them. As we'll see later in this thesis, these properties are essential in determining how appropriate they would be in functioning as TSV materials. From the table, it is clear that they have varying degrees of interaction with the growth conditions, which is further complicated by the fact that different research results often predict different behaviors. All of these make it a quite challenging task to find out the optimum growth condition for producing CNT with a desired property.

Table 1.1: Qualitative relationship between some of the CNT properties with the CVD growth parameters, as reported in literature. (+) indicates a positive effect; (-) indicates a negative effect; (o) indicates the existence of an optimum value; (x) indicates no influence.

CNT properties	Growth parameters			
	Temperature	**Pressure**	**Gas ratio**	**Time**
Growth rate	+ [39] or o [40]	+ [41]	o [42]	+ [42]
Density	o [43]	+ [44]	+ [40]	o [43]
Quality	+ [45] or o [43]	o [46]	+ [46] or o [41]	x or - [43]

CNT growth during this work had been done by AIXTRON BlackMagic Pro, a LPCVD reactor. Being a commercial reactor, it had some standard set of growth conditions (or recipes) installed, and a few of them were used for the early growth experiments. One such recipe, which was used a lot of times before and during the initial stages of the thesis, offered CNT growth at standard LPCVD conditions at 650 ^OC. This recipe will be encountered several times in the next few chapters, and we would be referring it as the Nominal recipe. A brief description is given below, and the complete recipe may be found in appendix A.

Nominal recipe: The wafer is loaded on the chuck of the BlackMagic, and the reactor pressure pumped down until it reaches 0.1 mbar. Next, H_2 and N_2 are introduced at 700 sccm and 200 sccm flow rates, and the temperature and pressure are ramped up until they reach 500 ^OC and 80 mbar respectively. At this temperature annealing of the catalyst takes place for 3 min. After this, the temperature is further ramped up to the growth temperature, which is 650 ^OC. Now the feedstock gas C_2H_2 is introduced in the reactor at 50 sccm flow, for a duration of the CNT growth time (which is usually 5 to 10 min). Once growth is complete, both the H_2 and C_2H_2 flows are cut off, and the heater turned off. As a final step, N_2 is introduced into the reactor as a purging gas, and a purging cycle occurs until the heater cools to 400 ^OC. The process is now complete, and the chamber pressure may be vented to atmospheric level, and the sample taken out.

1.3 Prior research activities and direction of this thesis

1.3.1 Past research work by the group

CNT growth had already been attempted successfully by our research group in the past. Research had been directed towards using CNT-vias for monolithic integration. This meant that the growth heights were of the order of a few microns. This thesis is the first time that we started focusing on ultra-long CNT bundles for TSV applications; which meant that the growth heights were to be a few hundred microns. This attempt to increase height up to 100 times required that a serious re-engineering had to be done with the growth process.

It was identified that selecting the right combination of catalyst and support layers was one of the key ingredients for increasing height; the other being designing optimum growth recipes (CVD conditions). Accordingly various kinds of substrate combinations were experimented with. From the growth results, it was clear that the substrate indeed played an important role in CNT growth. The results of some these experiments, as published by our group earlier, are presented in table 1.2. Although these publications were

aimed at CNT vias (as opposed to TSV), this will give us, nonetheless, an idea about our position at the start of this thesis work. From the table it is clear, that a different substrate and catalyst combination was surely needed to increase the growth height by orders of magnitudes.

Table 1.2: Different CNT growth heights and densities, as observed previously by our group, from various combinations of catalysts and support layers.

Catalyst	Support layer	Growth height (µm)	Growth density (x 10^{10} cm^{-2})	Reference
Ni	Ti	2	10^9	[47]
Pd		2	10^{12}	
Co, Fe		Random growth[1]		
Fe	TiN	70	10^{11}	[37]
Fe	Ti	70	10^{10}	[48]
Ni		< 2	10^9	
Co	TiN	< 2	10^{10}	[49]
Co-Al		< 1	10^{10}	

1.3.2 CNT growth on a novel Fe/ZrN substrate combination

The first task to identify the right catalyst and support layers, was to look at their surface energies; higher the difference between surface energy of the two materials, better would be the dewetting (or sintering) of the catalyst film into nanoparticle [50]. To understand this, we may think of water on the surfaces of leaves, which would cause some to get completely wet, while some would only have droplets. In fact, according to [51], there should be an optimal difference in the surface energies for the perfect de-wetting to take place. Once the catalyst film is dewetted, it can support a high-density, high-length CNT growth. Given below is a description on how we managed to find the right combination of these two materials.

1. Catalyst layer: Several catalyst materials, which allow CNT growth, could have been used. However before deciding on the right material, the following guidelines were followed [52]:

- *High surface energy:* A high surface energy material is beneficial to maintain the large difference between the substrates. For this purpose, transition elements are routinely used as catalysts [53]. Fe, Ni and Co were found to have high surface energy values.
- *Low activation energy:* The lower the activation energy, the lower is the temperature required for the growth reaction to initiate [49]. Fe and Co were found to meet this criterion.

So we were left with two choices; Fe and Co. Among them, Fe was chosen to be used for this work. Co has been scheduled to be used for future research work.

2. Support layer: A variety of different support layers existed in literature; for instance, oxides of Al, Si and Mg [30, 54, 55] , nitrides of Ti and Si [37, 56], silicides of Co and Ni [50, 57], and metals like Ti and Ta [37, 58]. We had to follow certain guidelines this time as well, before deciding on the right support layer. The properties of a good support are listed below in [52], according to our order of preference.

- *Diffusion barrier capability:* The primary function of the support layer is to prevent diffusion of the catalyst into the substrate, at the high anneal and growth temperature conditions.

---

[1] A discussion on random growth may be found in section 3.1.1.

- *Low surface energy:* Low surface energy materials were preferable in our case, so as to increase the surface energy difference as much as possible.
- *Electrical conductivity:* For interconnect purposes; conductive layers are always preferable, since they improve the overall conductivity of the system.
- *Resistance to oxidation in air:* The layer should not oxidize when handling under ambient conditions. Formation of native oxide would change its physical properties.

Considering all these factors, we started our search for the right support layer. TiN was already familiar to our group; but due to its very high surface energy (1.6 J/m^2), it had produced low growth heights as had been shown in table 1.2. Al_2O_3 had a much lower surface energy (0.038 J/m^2), and was thus was a better candidate in this respect. However, its biggest problem was that, it was an insulator. The other options available to us were MoN, MoO_3 and ZrN. Among them, the surface energy of ZrN (0.048 J/m^2) was found to be of the order of Al_2O_3. The surface energies of the Mo-compounds were not available in literature, but it was expected that they were quite high, since no growth was observed when CNT growth was attempted with a Fe/MoN or Fe/MoO_3 combination.

On the other hand, a Fe/ZrN combination worked brilliantly; it repeatedly produced high CNT growth of more than 200 μm (fig. 1.5). We believed that the key to this was definitely the large surface energy difference between Fe and ZrN. Although the resistivity of ZrN (5500 μΩ-cm) is an order higher than that of TiN (200 μΩ-cm), we were willing to make this sacrifice in order to increase the growth length. So, the Fe/ZrN combination was finalized to be used for growing ultra-long CNT. Table 1.3 revises some of the materials discussed for support and catalyst layers used for CNT growth; and may serve as a beginner's guide for finding the right material. In reality, the surface energy and resistivity values may differ up to an order of magnitude depending on their deposition parameters; so it is best to perform an in-situ measurement of the two parameters, before starting with growth experiments.
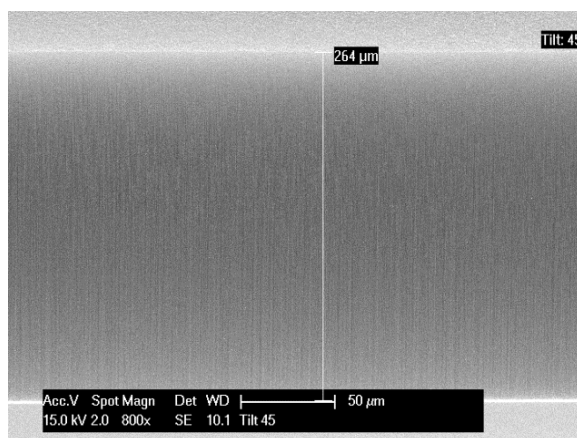
Figure 1.5: Growth heights in excess of 250 μm achieved on a Fe/ZrN substrate with a standard LPCVD growth recipe (Nominal) at 650 °C.

Table 1.3: Common catalyst and support layer materials used for CNT growth. The surface energy and resistivity values are presented here for a starting guide. These values may differ up to an order of magnitude depending on their deposition conditions.

Catalyst		Support layer		
Material	**Surface energy (J/m²)**	**Material**	**Surface energy (J/m²)**	**Resistivity (μΩ-cm)**
Fe	2.12	Al_2O_3	0.04	Insulator
Ni	2.08	SiO_2	0.04	Insulator
Co	2.22	ZrN	0.05	200
Pd	2.05	TiN	1.60	98
Pt	2.48	$CoSi_2$	0.72	60
Cu	2.76	$TiSi_2$	1.12	15
Au	1.50	Ti	1.75	56

1.3.2.1 Search for an improved growth recipe: A design of experiments approach

Having finally identified the right substrate combination[2], more growth experiments were carried out using the Nominal recipe. We soon realized that there were a lot of issues which needed to be tackled before these materials could be successfully used. This essentially marked the birth of this thesis work.

In contrast with the Fe/TiN or Co/TiN substrates, which had produced almost equal growth heights for 2 – 5 nm Fe layer thickness [37, 49], the Fe/ZrN substrate was found to be far more sensitive to this. Indeed a difference of even a few angstroms resulted in hundreds of microns difference in the growth height. The optimum thickness was found to be located somewhere between 0.5 – 1 nm (fig. 1.6a), and the growth rate at the optimum level was as high as 100 μm/min. When the layer thickness was increased to 1.3 nm (a difference of just a few Fe atoms), the rate decreased to 10 μm / min (fig. 1.6b) producing low CNT growth again. Besides, from time to time it was observed that growth was taking place only at some random locations on the substrate, even though the entire surface was covered with catalyst (fig. 1.6c). All these observations pointed out to the fact that, these growth conditions were actually unstable. Also, we intended to bring down the growth temperature to lower values, as 650 °C was too high for CMOS processes. Finally, we also observed that the growth height reduced significantly when the islands were patterned (fig. 1.6d). Besides these four targets, it was also kept in mind to attempt to increase the density and quality of the nanotubes from their present values, which were presently at moderate levels. For all these reasons, it was decided to optimize the catalyst/support layer thicknesses as well as the CVD conditions, so as to find the right combinations of parameters which would improve the above-mentioned problems.

---

[2] ZrN support layer was deposited by sputtering, using the TRIKON SIGMA sputter coater.
 Fe catalyst layer was deposited by e-beam evaporation, using the CHA Solution evaporator.
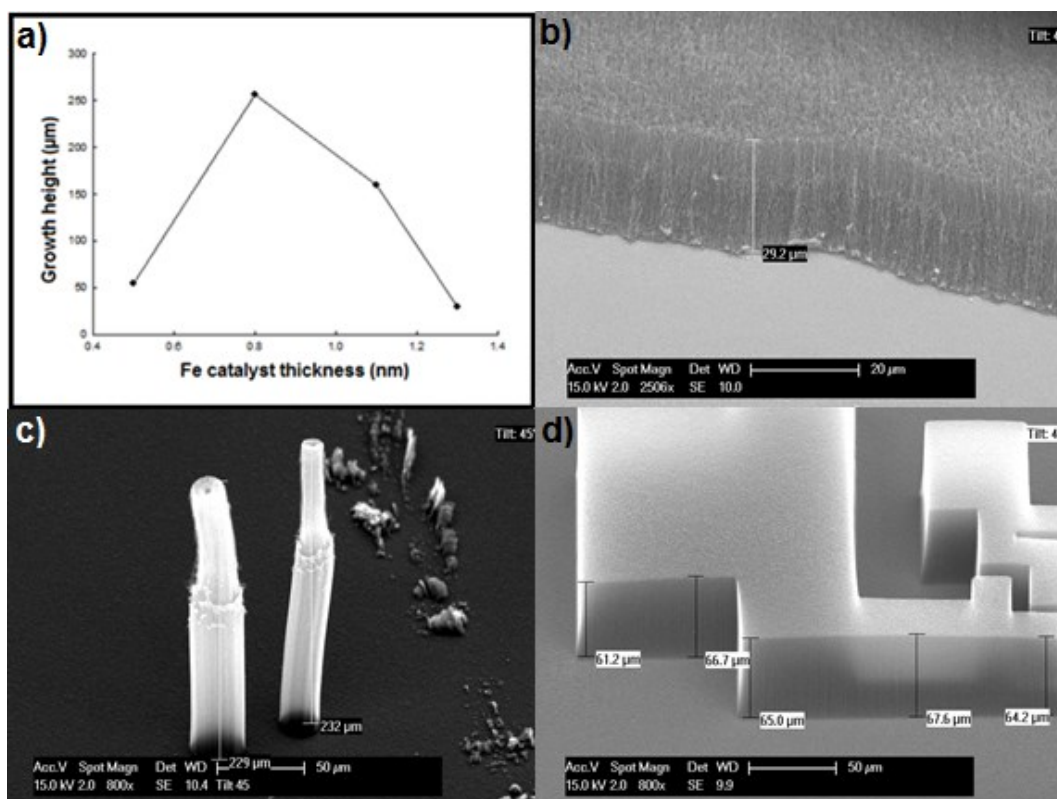
Figure 1.6: Growth results from preliminary experiments: (a) Plot of growth height with catalyst thickness shows the existence of an optimum thickness value for high growth; (b) Decrease of growth height when a 1.3 nm thick Fe layer is used; (c) High CNT growth at random substrate locations; (d) Decrease of growth height on litho-patterning the catalyst layer.

Considering the Nominal recipe as the starting point, we were left with six CVD conditions to optimize for. These were: the catalyst anneal temperature and time, CNT growth temperature and pressure, and C_2H_2 and H_2 flow levels. Added to these six, were two substrate parameters; the ZrN and Fe layer thicknesses. We intended to test all these parameters and check which of their values would give the desired growth properties. At this point, it also had to be decided, how many values (or levels) of each parameter we would use. Using values at random did not make much sense, as we intended to conduct an organized set of experiment. Keeping two levels for each of the parameters (that is, a high and a low value) was a possible option. However, keeping three levels (high, medium and low value) was a better option, as it would allow us to test if there existed an optimum region between the high and low values. So finally we ended up with having 8 parameters to test for, and each with 3 levels.

Brute-force experimentation with each parameter and level would have required us to perform 3^8 (= 6561) number of experiments! Needless to say, this was an impossible figure. A different and more intelligent approach had to be followed in order to perform a much lesser number of experiments. This called for using a Design of Experiments (DOE) approach, and it is the crux of this thesis work. In the subsequent chapters, we will be studying in details about how we had used this approach, and how it helped us reduce the number of experiments to only 18, while at the same time, predicting the right recipe for an optimized CNT growth.

1.4 Summary

This chapter serves as the introduction to the thesis and discusses about the current status of semiconductor technology and the background research work in the field of carbon nanotubes. We looked at the reasons of the industry-trend to move to 3D-integrated circuits technology from the planar 2D-technology from an interconnect point of view, and discussed the advantages of using CNT over copper for interconnects. We then studied about the CVD growth process of CNT, and saw how the different substrate and process conditions determine its properties. We looked at the previous research work of the group in fabricating short CNT vias, of the order of a few microns. To integrate CNT as TSV, they needed to be a few hundred microns of length. We identified that the right catalyst-support layer combination was required for producing ultra-high growth lengths, and a Fe/ZrN substrate was identified to be the right one. From the initial experiments, we saw that there were several growth problems, which had to be corrected, by optimizing the growth recipes. Finally, considering our large number of growth parameters, we chose take a design of experiments (DOE) approach for the optimization process. In the next chapter, we are going to look at three classes of DOE tools, compare their merits and demerits, and finally chose the Taguchi method for experimentation.

Chapter 2

CNT growth recipe optimization by statistical Design of Experiments method

2.1 Design of experiments: What and why?

It is appropriate to think of an experiment as a system; so that the laboratory and its various equipment constitute the system, which are under the effect of one or more sources of inputs, interacting with one or more sources of external factors, producing one or more outputs. The inputs to the system, which can also be referred to as *parameters*, may be set at different values (or *levels*) by the experimenter. However, the external factors (or sources of *noise*) are uncontrollable. Let us compare this scenario with our case. The system is the CVD reactor, which has various process conditions as inputs, which may interact with some spurious noise sources, finally producing CNT growth as the output.

In the world of experimentation, the experimenter is interested to observe how the outputs change as the inputs are changed. Further she would also like to see which combination of input levels would help in optimizing the output. For this purpose, she must perform a number of experiments, setting each of the inputs at different levels. Thus, the more the number of inputs or levels, the higher is the number of experiments needed to be performed in order to understand the nature of the system. If there are P no. of inputs, each set at L no. of levels, then the total number of possible experiments is L^P. For small values of P and L, it is possible to conduct every experiment. However, we can easily see what would happen if these values get large! Luckily, statistics saves us in these situations.

Design of experiments (DOE) is a statistical tool, which intelligently curtails the huge number of experimental runs needed to understand the dynamics of a system, and thereby gives us information about which input levels must be set so as to optimize the response. Instead of the brute force experimentation of trying out every combination of parameter levels (this process is also called Full factorial design), it gives us only a selective set of combinations, resulting in much lesser experiments. Although a bit of accuracy is lost in this process, but considering the time and money one may have to invest for the earlier approach, the DOE approach almost always proves to be a more sensible path. The DOE approach to experimentation was first made widespread by the efforts of Sir. Ronald A. Fischer, in the early 1900s. In its early days, it usually found applications in process industries. However, before long, it set its foot in the academia as well, when

researchers realized its efficiency in their experiments. This is supported by a large volume of published work in this field, from virtually every area of science and engineering.

2.2 Review of standard DOE techniques

From a survey of literature, we learnt about different DOE techniques. In total, three classes of DOE tools were studied; and they are the Fractional factorial design, the Response surface methodology, and the Taguchi method. The most commonly used tool is the Fractional factorial design (FFD); so named because it uses a fraction of the full factorial design table. Being fully complete, the full factorial table provides room to study different orders of interactions between the parameters as well. Usually, the higher the order of the interaction, the lower is its strength in affecting the response. In other words, an interaction between 2 or 3 variables is more powerful in affecting the result than one between 7 or 8 variables. Hence the table can be shortened (or fractioned) by using this redundancy into effect, thereby eliminating these weak interactions. The fractional factorial design uses this philosophy [59].

To clarify the concept of interaction between parameters, we see in fig. 2.1, how two parameters (A and B) set at two levels affect the response, when they are non-interacting and interacting respectively. When the parameters are non-interacting, then the change of level of a parameter (A) causes just an offset in the response of the system, towards change of the other parameter (B). When the parameters start interacting, then the response of the system might be more complex towards changes in the inputs, and accurate prediction becomes difficult.
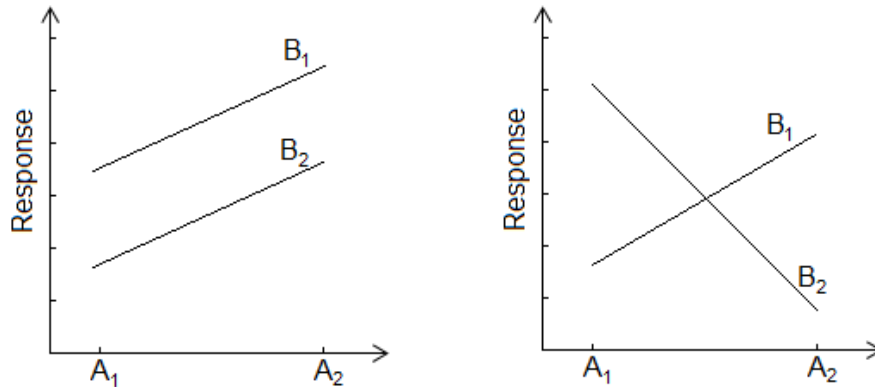
Figure 2.1: Non-interacting and Interacting parameters, and their effect on the response [62].

A FFD with P no. of parameters and L no. of levels, and having a fraction value of F, would mean that the experiment space has been reduced by a factor of L^F, making the number of required experiments to be L^{P-F}. The maximum number of factors, that can be studied by a L^{P-F} experiment is $(L^{P-F}-1)/2$ [60]. In our case, for covering all the 8 parameters at 3 levels, at least a 3^{8-5} design is required, giving rise to 27 experimental runs. However it should also be noted that keeping a fraction as high as 5 would severely limit the power of the FFD to study parameter interactions.

The second type of DOE technique which was studied is known as Response surface methodology (RSM). This is an especially useful tool for modeling and analyzing processes which have highly non-linear relationship between the parameters [61]. The essence of this tool is to find a polynomial from the measured response values, which relates the parameters to the response with a minimum margin of error. Hence this technique is analogous to regression, but extrapolated to a larger number of variables. The calculated

response surface is represented graphically as a function of the different parameters, two at a time. By analyzing the different response curves, the full polynomial equation can be obtained. Once this is done, the maxima and minima of the function may be easily found out. The RSM approach has many advantages for analyzing multivariate functions, like precise estimation of the model coefficients, chance of extrapolation of the response for higher or lower levels of inputs, and robustness against the outlier observations [61]. For these qualities, until now the RSM proved to be an efficient DOE tool for our purpose.

Similar to FFD, the RSM also has different algorithms to design the experimental table. Three common algorithms were studied; they are Central composite design (CCD), Box-Behnken design (BBD) and D-optimal design [61]. The CCD is the most commonly used RSM design for fitting higher order models. However, for the high number of parameters that we have, the default CCD table offers 100 experimental runs[3]. Even after some changes in its algorithm, the least number of runs that could be achieved was 80. This is way too high for our purposes. The next RSM algorithm studied was the Box-Behnken design, which is especially developed for studying processes with three parameter levels. Unfortunately, this again offered a high number of 120 runs, with a modified minimum of 112. For this reason, it was rejected too. The final design was the D-optimal design. This is not a standard design like the previous ones, but is custom-generated by the computer using different algorithms. They are only used in special cases; for instance, when the inputs are constrained by some boundary conditions, or when the experimenter wants to reduce the number of runs for large experiments. We also would have exactly wanted to do the same, but then, the accuracy of the design also reduces considerably on reducing the number of runs. Keeping this in mind, this approach was not tried.

The final class of DOE was the Taguchi method. Named after its discoverer Dr. Genichi Taguchi, this is an elegant optimization tool which is widely used in industrial processes. It allows the experimenter to set the parameters and levels according to standard experimental tables, called orthogonal arrays (OA), which are similar to the tables of FFD or CCD. These arrays are of different sizes, depending on the number of parameters and levels in the experiment. For our requirements, Taguchi had a standard OA with only 18 experimental runs, the lowest figure among the various techniques considered.

There were a few things, which attracted us to this method. Besides offering the minimum number of experiments, this method had the unique advantage of working with the signal-to-noise ratio (SNR) of the output, and not the actual values, as used for the others [62]. This is an especially useful feature for designing experiments where results may vary widely with different trials for the same combination of inputs. As a result of using SNR values, Taguchi ensures robustness of the process from effects of noise [63]. It also has the advantage of simplicity: optimum recipes can be deduced very easily from the experimental data using a standard statistical procedure. However, the main disadvantage is that, it is not well designed to perform when there is a high degree of interaction between the parameters [64, 65]. Also, it gives no chance for interpolating or extrapolating the results any further, as it does not generate a polynomial expression relating the input and output variables.

With all these methods at hand, we had to make a choice of selecting the DOE which would work best for us. The RSM was discarded because of its large experimental size. The FFD and Taguchi were similar in terms of the number of experiments offered (although an excess of nine for FFD would still be costly in cleanroom processes). The initial advantage that FFD had over Taguchi was its ability to model interaction

---

[3] For generating experimental tables for the different RSM methods, we used standard functions available in Matlab. The code may be found in appendix E.1.

effects. However, a fraction of 5 in FFD suggested that it had lost this ability; so Taguchi was the obvious choice. This selection procedure, however, must not be seen as a method of elimination. Taguchi had its own range of advantages to offer; the most important being, the option to work with SNR of the output. As a reconfirmation about the effectiveness of the Taguchi, we looked at several publications in different areas where this had been used with success [66-69]. As a pleasant surprise, we also found that this technique had already been used before in the field of carbon nanotubes, for optimizing several properties [70-72]. To conclude this section, we summarize in table 2.1 the different DOE methods which were discussed. In the next section, we are going to study the Taguchi method in details.

Table 2.1: Some common DOE tools and their features.

DOE method		Number of experiments	Advantages	Disadvantages
Full factorial		3^8 (= 6561)	Highest level of accuracy.	Too many runs.
Fractional factorial		27	Standard and common method.	High degree of fractionation for our experiment.
Response surface methodology	Central composite	80	Good in modeling interactions and extrapolating results.	Too many runs.
	Box-Behnken	112	Designed for 3-level experiments.	
	D-optimal	Adjustable	Customized tables. Possibility for lower number of experiments.	Accuracy is questionable.
Taguchi		18	Uses SNR over real values. Least number of experiments for our design.	Inadequacy in modeling interaction effects.

2.3 The Taguchi DOE method: Working mechanism

The steps for performing a Taguchi DOE analysis are [62]:

- Construction of an orthogonal array
- Performing the experimental runs
- Generating Main effects plot from the SNR values of results
- Performing a verification experiment with the optimized recipe
- Identifying the strength of the parameters in deciding the response (optional)

1. Construction of an orthogonal array: Orthogonal array is the Taguchi equivalent of the experimental table. In other words, it is the name given to a table of parameters set at different levels, which can adequately cover the whole experimental space. In an OA, the columns are designed in such a way that each of them has an equal number of levels for the different parameters. The commonly used OAs can accommodate two, three or four levels. Additionally, some OAs also offer the possibility of working with mixed number of levels (incidentally, this thesis works with such an OA). The orthogonal property of the table means that, the

controlling parameters do not interact among themselves; that is, that they are completely independent of each other, and changes in one will not affect the others. Taguchi also offers the possibility to deal with interacting parameters; however, as discussed, it is generally not suited by nature to study interactions. Since in this thesis, we have dealt with eight parameters, studying interactions between each would cause the OA to increase its size enormously, leading to a large number of experiments. Also, the strength of interaction between the different parameters is difficult to estimate when one does not have prior expertise with the process. For these reasons, interaction effects were not studied during this work.

Orthogonal arrays are indexed by $L_N(L^P)$; where L is the reference to the array, N denotes the number of experimental runs, L is the number of levels of each parameter, and P is the number of parameters. When designing an experiment, once P and L have been decided by the experimenter, she may either use one of the standard OAs as designed by Taguchi, or modify a standard OA to fit her requirements, using linear graphs[4]. The standard OAs are $L_4(2^3)$, $L_8(2^7)$, $L_{12}(2^{11})$, $L_{16}(2^{15})$, $L_{32}(2^{31})$, $L_9(3^4)$, $L_{18}(2^1, 3^7)$, $L_{27}(3^{13})$, $L_{16}(4^5)$, $L_{32}(2^1, 4^9)$ and $L_{64}(4^{21})$.

We will make use of a simple conceptual experiment to understand how a Taguchi DOE analysis is performed. Let us consider an experiment with 4 parameters. The experimenter would like to set each of them to 3 levels. Further she would like to see the response that the different parameters produce, and then determine the most effective combination for optimizing her result. According to Taguchi, optimization can mean either maximizing or minimizing the result, or maintaining it at a desired value. Let us suppose that in this experiment, the result is to be maximized. A look at the standard OAs will tell the experimenter that the L_9 table is best suited for this. In contrast to the 3^4 number of experiments with the brute force approach, only 9 experiments have to be performed this time. The L_9 OA is presented below in table 2.2. We may note that the parameters are always displayed in coded levels in an OA. Thus for three levels, they are set to high (3), medium (2) or low (1) values.

Table 2.2: The L_9 (3^4) experimental table (OA) for the conceptual experiment design. The coded levels of parameters, and notation for results and SNR (as used in the subsequent analysis) are shown.

Experiment number	P_1	P_2	P_3	P_4	Results	SNR
1	1	1	1	1	$R_{1,1} ... R_{1,m}$	SNR_1
2	1	2	2	2	… … … …	…
3	1	3	3	3	… … … …	…
4	2	1	2	3	… … … …	…
5	2	2	3	1	$R_{n,1} ... R_{n,m}$	SNR_n
6	2	3	1	2	… … … …	…
7	3	1	3	2	… … … …	…
8	3	2	1	3	… … … …	…
9	3	3	2	1	$R_{9,1} ... R_{9,m}$	SNR_9

2. Performing the experimental runs: The next step is to perform the experiments using the OA. It is recommended to carry out as many trials as possible for each experiment, as allowed by time and cost. This is

---

[4] Modification of a standard OA using linear graph is beyond the scope of this thesis. The interested reader may refer to [62] for a detailed analysis on this topic.

because the results may differ for successive trials due to noise in the experimental set up. Also, the trials should be performed at random, so as to eliminate any bias accumulated in the machine on repeating the same experiment many times [73].

3. Generating Main effects plot from the SNR values of results: The Main Effects Plot (MEP) is a very powerful feature in any DOE analysis. It is a simple graphical technique which has the ability to show the role of each parameter at all its levels, in determining the value of the output. Subsequently, it shows the combination of the right parameter levels needed to optimize it. Taguchi uses SNR values of the results to construct these plots. Depending on whether the output is intended to be maximized, minimized, or maintained at a nominal level, the following three formulae are used to calculate the SNR.

$$SNR_{larger-the-better}(n) = -10\,log_{10}\left[\frac{1}{M}\sum_{m=1}^{M}\left(1/R_{n,m}\right)^2\right]$$

(2.1a)

$$SNR_{smaller-the-better}(n) = -10\,log_{10}\left[\frac{1}{M}\sum_{m=1}^{M}R_{n,m}^{\;2}\right]$$

(2.1b)

$$SNR_{nominal-the-best}(n) = -10log_{10}\left[\frac{1}{M}\sum_{m=1}^{M}\left(R_{n,m}-R_0\right)^2\right]$$

(2.1c)

where, n is the experiment number; so $n = 1, 2, 3 \ldots. N$.

m is the trial number for each experiment. If M number of trials had been performed, then $m = 1, 2, \ldots., M$.

$R_{n,m}$ is the response for the nth experiment in the mth trial.

R_0 is the value at which the response is desired to be maintained; that is, the nominal value.

Having calculated the SNR values, it is now time to construct the MEP. Before that, however, we need to know the main effect values (MEV) of the SNR for each parameter at their corresponding levels. This is calculated using the formula:

$$SNR_{p,l} = \frac{1}{K}\sum_{k=1}^{K}SNR_{\beta}$$

(2.2a)

where, p is the serial number for each parameter, or $p = 1, 2, \ldots., P$.

l is the serial number for each level, or $l = 1, 2, \ldots., L$.

K is the number of times that l appears in the P_p column of the OA, and β is the corresponding value of n when this event happens.

To understand the concept, we would like to calculate the MEV for the third parameter (P_3) at its medium level ($l = 2$). Looking at the $\mathbf{L}_9$ OA, we see that P_3 appears at $l = 2$, when $n = 2$, 4 and 9; hence K will be equal to 3. Thus, we may write:

$$SNR_{3,2} = \frac{SNR_2 + SNR_4 + SNR_9}{3}$$

<div align="right">(2.2b)</div>

Having calculated all the ($P*L$) number of main effects values, we can now generate the main effects plot[5]. For this hypothetical experiment, it is a collection of 4 plots from the 4 parameters. Fig. 2.2 shows a sketch of the Main effects plot that the experimenter may have generated from the data. The plots clearly show how each parameter influences the outcome. Also, different parameters have difference degrees of strength on optimizing the result. For example, a change in the levels of P_4 would cause a large change in the result, while a change in P_3 will cause only a minor change. Further, increasing the level of P_4 will have a detrimental effect on the result; while performing the experiments with either the low or medium levels of P_3 will cause absolutely no change, but increasing the level further will have a slight incremental effect. The relationship between P_1 and P_2 with the output is more complicated. We can see that there is an optimum level for P_1, where the result is the maximum. On both sides of this level, it decreases. The reverse effect happens for P_2.
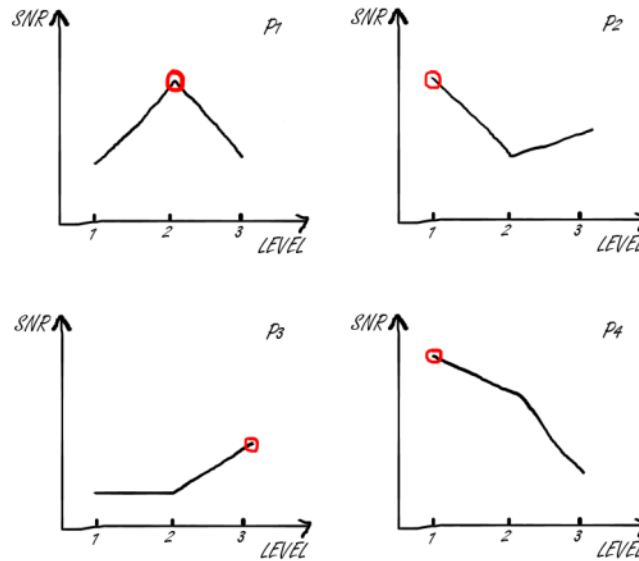
Figure 2.2: Sketch of Main effects plot showing the effect of different parameters and levels on the response.

From the collection of the plots, it now becomes very easy to identify those parameter levels, which will collectively produce the maximum output. These levels had individually resulted in the maximum SNR; as marked in red. We may express this condition by:

$$R_{opt} \equiv \{P1_2, P2_1, P3_3, P4_1\}$$

<div align="right">(2.3)</div>

---

[5] For this thesis, all the main effects plots were generated by Matlab. The code may be found in appendix E.2.

If we take a look at the OA, we see that this is a new recipe which was not present earlier. So, the result can indeed be optimized over the already observed values. In some cases though, the optimum recipe coincides with a recipe in the OA, which means that there is no more scope of optimization. When an experimenter tries to minimize the response, or tries to fix it to a nominal value (which means that the difference between the obtained and the nominal value is to be minimized), those levels which result in the lowest SNR values, would have to be located.

Theoretical prediction of R_{opt}: Taguchi also gives the option of predicting the optimized value of the response theoretically. This may be done by first finding the optimum value of the SNR, according to the following formula:

$$SNR_{opt} = \overline{SNR_n} + \sum_{p=1}^{P} \left[\frac{1}{L} \sum_{l=1}^{L} SNR_{p(l^*)} - \overline{SNR_n} \right]$$

(2.4a)

where, $\overline{SNR_n}$ is the average value of SNR of the n results.

l^* is the optimum level of the parameter in consideration, i.e. P_p.

Thus, for this example, SNR_{opt} can be calculated as:

$$SNR_{opt} = \overline{SNR_n} + \left[\frac{SNR_4 + SNR_5 + SNR_6}{3} - \overline{SNR_n} \right] + \left[\frac{SNR_1 + SNR_4 + SNR_7}{3} - \overline{SNR_n} \right]$$
$$+ \left[\frac{SNR_3 + SNR_5 + SNR_7}{3} - \overline{SNR_n} \right] + \left[\frac{SNR_1 + SNR_5 + SNR_9}{3} - \overline{SNR_n} \right]$$

(2.4b)

Finally, the theoretical prediction for R_{opt} may be simply given as:

$$R_{opt} = 10^{SNR_{opt}/20}$$

(2.5)

In the same way, the theoretical prediction of the response from any other combination of parameters can also be obtained.

4. Performing a verification experiment with the optimized recipe: Now that the analysis is complete, a verification experiment for the optimized condition must be performed to check the accuracy of the DOE. The theoretical and experimental values should exactly be the same if there had been absolutely no interaction between the parameters. However, in reality, there would always be some degree of interaction; and the higher the strength of the interaction, the greater will be the deviation of the two values. At times, the maximized result may even be smaller than the results from the OA itself! In this case, the interaction between the parameters or the noise sources had been so severe, that it heavily altered the system behavior.

5. Identifying the strength of the parameters: It is also possible to get a quantitative idea about the strength of each parameter in determining the final result. This can be done by performing an Analysis of variance (ANOVA). The working mechanism of the procedure has been explained in details in [62]. However, it can also be performed easily with standard commands in software like Matlab or Minitab. The ANOVA generates a metric, known as the Variance ratio (F) for each parameter, which may be linked to its percentage contribution towards the response. This means, higher the F-value, stronger is its role in the optimization process. Closely linked with the variance ratio is another term; the *Prob > F*. Its definition loosely translates to the success of the experiment in achieving the same value of output, when a parameter is eliminated altogether from the design. This means, a strong parameter (with high F) will have a low *Prob > F*, and vice versa. Likewise, ANOVA can also be used in identifying the weakest parameters in the analysis. If the F-value is close to zero, then eliminating it will not affect the result of the experiment at all. ANOVA is also useful in multi-step Taguchi optimization problems, where the strength in each step is determined, and the weaker parameters are eliminated in each step.

2.3.1 Using the Taguchi L_{18} OA for CNT growth experiments

Briefly recalling the material discussed in the last chapter, we had a standard industrial (Nominal) growth recipe as our starting point. It is here, that we recognized that there were six CVD parameters and two substrate parameters one could optimize for. Also, it was intended to keep three levels for each parameter. This choice offered us the possibility of using the Taguchi L_{18} OA, primarily because it offered us the minimum number of experimental runs. The L_{18} OA has a structure of (2^1, 3^7), which means that there are seven parameters with three levels, and one parameter with two levels. We did not want to lose a level from any of the CVD parameters, and neither from the catalyst. So, it was decided to keep the ZrN layer thickness at two levels. Next, the task was to set the levels of these parameters around the values in the Nominal recipe. We will first look at the different parameters and their levels at table 2.3, and then explain the reason behind selecting these values.

Table 2.3: Details of the different growth (substrate and CVD) parameters as used in this work. The (*) denotes their values in the Nominal recipe.

Parameter type	Parameter Name	Level		
		Low	Medium	High
Substrate	Support layer (ZrN) thickness (nm)	10		30
	Catalyst layer (Fe) thickness (nm)	0.5	0.8	1.1
CVD	Catalyst anneal temperature (^{O}C)	400	500*	600
	Catalyst anneal time (min)	1	3*	5
	Growth temperature (^{O}C)	550	650*	750
	Growth pressure (mbar)	20	50	80*
	H_2 flow / C_2H_2 flow	8	14*	20
	C_2H_2 flow (sccm)	30	40	50*

Discussing about the substrate parameters, we had already seen that there exists an optimum Fe catalyst layer thickness for growth with the Nominal recipe. Now we were interested to observe the role of other thickness values in determining the growth height, for different CVD conditions. Since too thick a layer would probably reduce the growth height, as we found before, a narrow selection window had to be kept around the optimum; hence we went for 0.5 nm and 1.1 nm. For the support layer, since we had no prior experience in

working with ZrN, and so far we had seen that a 30 nm layer produces good growth heights, this level was used as the upper level, and the lower being arbitrarily selected as 10 nm.

Discussing about the CVD parameters, the anneal temperature and time were varied equally around the Nominal conditions. We were interested to see what happens for two extreme cases: a short anneal time at low temperatures, and a long anneal time at high temperatures. A similar approach was used for setting the CNT growth temperature. Of course, maintaining a low thermal budget is always appreciated in CMOS processes. However, too low a growth temperature was not attempted since we did not have much idea whether growth would indeed occur at these temperatures. Hence a minimum of 550 ^{O}C and a maximum of 750 ^{O}C were used. The next parameter was pressure. The BM had a maximum rating of 95 mbar pressure, which meant that the Nominal value was operating near to the maximum. Thus it was kept as a high level, and the other two levels were fixed with a wide window, ensuring that we were able to reach even very low growth pressures. The last two parameters were the H_2 and C_2H_2 flow rates. The Nominal recipe had used a flow ratio of 14. In fact, the safe operating regime of BM ensures that a minimum ratio of 5 between H_2 and C_2H_2 be guaranteed in order to prevent deposition of too much amorphous carbon in the chamber. With this knowledge, a minimum ratio of 8 and a maximum ratio of 20 were maintained. Finally, to set the flow rate for C_2H_2, the BM ratings for H_2 (which were 100 sccm and 1000 sccm) and the flow ratio levels were used. The Nominal value of 50 sccm was set as the highest and the other two values fixed accordingly. This completed our design of the experimental table. Table 2.4 shows the complete L_{18} OA, with the parameters and their values.

Table 2.4: The final experimental L_{18} OA showing the different parameters at their various levels. This table has been used for all growth experiments during this work.

Experiment number	Substrate parameters		CVD parameters					
	ZrN thickness (nm)	Fe thickness (nm)	Anneal temperature (^{O}C)	Anneal time (min)	Growth temperature (^{O}C)	Growth pressure (mbar)	H_2flow / C_2H_2 flow	C_2H_2 flow (sccm)
Recipe 1	10	0.5	400	1	550	20	8	30
„ 2	10	0.5	500	3	650	50	14	40
„ 3	10	0.5	600	5	750	80	20	50
„ 4	10	0.8	400	1	650	50	20	30
„ 5	10	0.8	500	3	750	80	8	30
„ 6	10	0.8	600	5	550	20	14	40
„ 7	10	1.1	400	3	550	80	14	50
„ 8	10	1.1	500	5	650	20	20	30
„ 9	10	1.1	600	1	750	50	8	40
„ 10	30	0.5	400	5	750	50	14	30
„ 11	30	0.5	500	1	550	80	20	40
„ 12	30	0.5	600	3	650	20	8	50
„ 13	30	0.8	400	3	750	20	20	40
„ 14	30	0.8	500	5	550	50	8	50
„ 15	30	0.8	600	1	650	80	14	30
„ 16	30	1.1	400	5	650	80	8	40
„ 17	30	1.1	500	1	750	20	14	50
„ 18	30	1.1	600	3	550	50	20	30

With the OA completed, the DOE process could now be started. However, there was a vital step which still needed to be done. For the BM, these growth conditions were all new, so its PID controllers were not tuned to work efficiently for these values. This resulted initially in temperature and pressure fluctuations during the growth operation. In order to repair this, the PID settings for each recipe had to be manually re-tuned. A note on this may be found in appendix B. Here we end our discussion on the theory behind designing the experiment. In the next (and last) section of this chapter, we will take a brief look how multiple variables can be optimized with one single recipe. Although this has not been performed during this thesis, but future experiments can be tried out with this technique.

2.4 Multivariate optimization: Grey relational analysis

So far we had been discussing about optimization techniques where the experiments had only one response. However, it is often the case where two or more responses are needed to be optimized at the same time. It is then desirable to come out with a recipe that can optimize both the responses *simultaneously*. In some (rare) cases, it is indeed possible to generate multiple responses at their exact optimum levels. However, at most times, we have to make a compromise and settle for the recipe that takes the responses as close to their optimum values as possible.

Multivariate optimization is a useful branch in DOE-based statistics, and several techniques have been developed for this purpose. A brief study provided us with methods such as Principal component analysis [74], Regression analysis [75], Neural network and fuzzy logic [76] and Grey analysis [77-79]. A good starting guide which explains these, and even more methods, may be found in [80]. These different methods were briefly studied, and finally the Grey analysis method was explored in details because the technique is simple to use, and it is intricately connected with the Taguchi method.

2.4.1 Working mechanism of Grey relational analysis

Let us design a hypothetical Taguchi DOE that uses the $\mathbf{L}_9$ table. Further let the experiments produce two different outcomes (R^1 and R^2); the first one of which needs to be maximized and the second one minimized. The experimenter would like to generate a recipe which would meet these requirements.

The first step is the **Normalization** of the responses. This means that the R^1 values will have to be coded uniformly, with the maximum value set at 1, and the minimum value at 0. Just the opposite has to be done for R^2.

The normalized values may be mathematically expressed as:

$$\mathbb{N}_n^1 = \frac{R_n^1 - (R_n^1)_{min}}{(R_n^1)_{max} - (R_n^1)_{min}}$$

(2.6a)

$$\mathbb{N}_n^2 = \frac{(R_n^2)_{max} - R_n^2}{(R_n^2)_{max} - (R_n^2)_{min}}$$

(2.6b)

where, $\mathbb{N}^1$ and $\mathbb{N}^2$ are the corresponding normalized values; n is the experiment number, ranging from 1 to 9.

The second step involves the calculation of the **Grey relational coefficients (GRC)** for each of the normalized responses. The GRC is a quantity which expresses the relationship between the ideal and the actual normalized results from the experiment. It may be calculated by the equations:

$$GRC_n^1 = \frac{\Delta_{min}^1 + \zeta\Delta_{max}^1}{\Delta_n^1 + \zeta\Delta_{max}^1}$$

(2.7a)

$$GRC_n^2 = \frac{\Delta_{min}^2 + \zeta\Delta_{max}^2}{\Delta_n^2 + \zeta\Delta_{max}^2}$$

(2.7b)

where, $\Delta_n^1 = |\varphi - N_n^1|$ and $\Delta_n^2 = |\varphi - N_n^2|$,

φ is 1 for R^1 and 0 for R^2,

ζ is a constant which may range from 0 to 1. Frequently, it is maintained at a value of 0.5.

After this step, the **Gray relational grade (GRG)** is calculated. It is basically the average of the GRCs from each observation. It is thus expressed as:

$$GRG_n = {(GRC_n^1 + GRC_n^2)}/{2}$$

(2.8)

The GRG is a figure-of-merit which gives an indication as to which of the experiments in the OA conforms best to Grey analysis. In other words, the experiment which has the highest GRG performs best in the simultaneous optimization process. As a final step, from the GRG values so obtained for each experiment, one can generate a Main effects plot with the larger-the-better methodology. The parameter setting that this MEP generates, would actually be the recipe that would work the best in the multivariate optimization.

2.5 Summary

This chapter introduced us to the concept of using a design of experiments approach for optimizing CNT growth parameters. We studied three classes of DOE tools, and after considering the merits and demerits of each, settled for the Taguchi method. Subsequently, the complete theory behind this method was described.

We then decided to use the L_{18} orthogonal array for our experiments, and motivated the selection of the growth parameters around their Nominal values. Finally, the topic of multivariate optimization was briefly described, and the theory behind the Grey relational analysis was explained. In the next chapter, we are going to look at the results of CNT growth with the Taguchi method.

Chapter 3

# Growth of vertical CNT on unpatterned catalyst layer

In this chapter, we will first report on the growth results of CNT by the different recipes generated by Taguchi DOE analysis. Next, we will try to explain how the different recipes result in different growth heights. We will then use these results to design a new optimized recipe, which is expected to produce ultra-long vertically aligned bundles of CNT. Subsequently, we will check its accuracy by performing a verification experiment. We will also try to understand the role that each parameter plays in maximizing CNT growth.

3.1 Growth height measurement results

Using the Taguchi L_{18} OA, growth experiments were carried out on different batches of wafers. In the first phase, the growth time was maintained at 5 min, and in the second phase, it was 10 min. The AIXTRON BlackMagic Pro CVD reactor was used, and thermal-CVD growth of CNT performed. All the growth experiments were carried out on a continuous layer of catalyst; which meant that the layer was not patterned lithographically.

3.1.1 Results for 5 min growth time

In accordance with Taguchi recommendation of performing multiple numbers of trials per experiments, the entire set of 18 experiments was performed two times, on separate wafer batches. They are referred to as trial 1 and trial 2 respectively. After a growth time of 5 min, the samples were taken out of the reactor, and inspected under a scanning electron microscope (SEM). The film of CNT was scribed with a metallic pen. This way, growth over the entire region could be measured. We will first take a look at the growth results for the different recipes, and then we will explain how the substrate and CVD parameters play a role in CNT growth. Fig. 3.1 shows the results of the two trials.
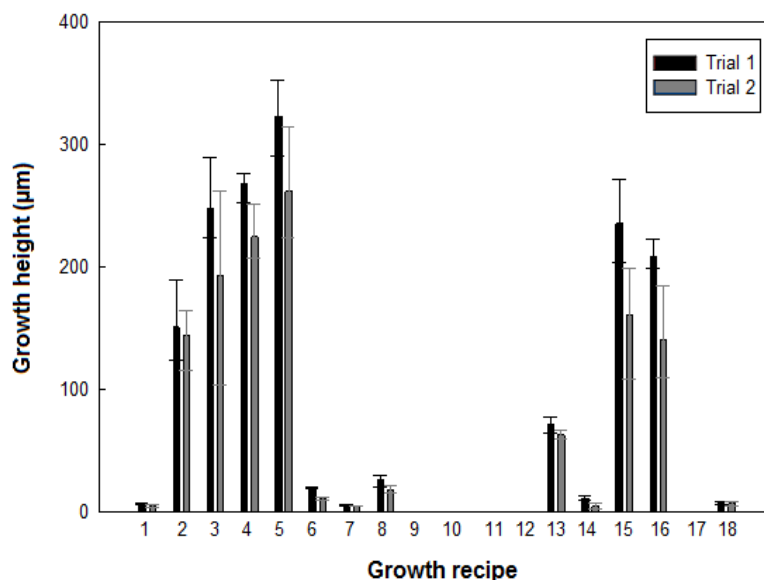
Figure 3.1: CNT growth height for 5 min time for different growth recipes. The bars represent the mean growth height, while the error bars reflect the smallest and the largest measured height. Two trials were done per growth recipe, and three observations were recorded for each trial.

Observation 1: The first observation is that, some of the recipes result in vertical growth of CNT, while some does not. In both the trials, recipe 11 did not produce any growth at all, while recipes 9, 10, 12 and 17 produced only a random, bushy network of tubes which had no vertical alignment. The rest of the recipes gave rise to needle-like, vertically aligned bundles of CNT, growing much like a forest. However, the growth height varied largely from recipe to recipe. Fig. 3.2 shows the two types of growth; random and vertical.

It was not immediately clear to us whether random growth or the total absence of growth for some of the recipes occurred due to some unidentified problem with the CVD reactor. However, since the recipes were well within its safe operating limits, the problem must have lied somewhere else; probably in the recipes themselves. Some recipes might simply not be favorable for CNT growth. Indeed, after a series of growth tests, we could understand why some of the CVD parameters did not support growth. Their explanation will be provided at a later part of this chapter. Among the ones which did produce vertical growth, recipe 5 yielded the highest growth height, with one observation reaching 325 μm. Recipes 2, 3, 4, 13, 15 and 16 also offered good growth, with heights mostly exceeding 150 μm. The remaining recipes (1, 6, 7, 8, 14 and 18) produced shorter growth heights of less than 50 μm.

Observation 2: The growth height of each recipe was not exactly the same for both the trials. Considering that the CVD conditions had more or less been uniform, this might have been caused due to the subtle difference in the actual deposited catalyst layer thickness. We had seen earlier how the thickness of this layer is an extremely important growth parameter. However, the heights obtained from trial 1 is consistently more than trial 2 for all the recipes. This shows that, irrespective of the catalyst film non-uniformity, the CVD parameters are robust enough to support a consistent growth trend.

Observation 3: From the error bars, we have an idea about the variation of growth on different regions of the substrate. For instance, growth heights vary between 100 μm to over 250 μm for CNT grown by recipe 3. The reason for this is probably again the non-uniformity of the catalyst layer.
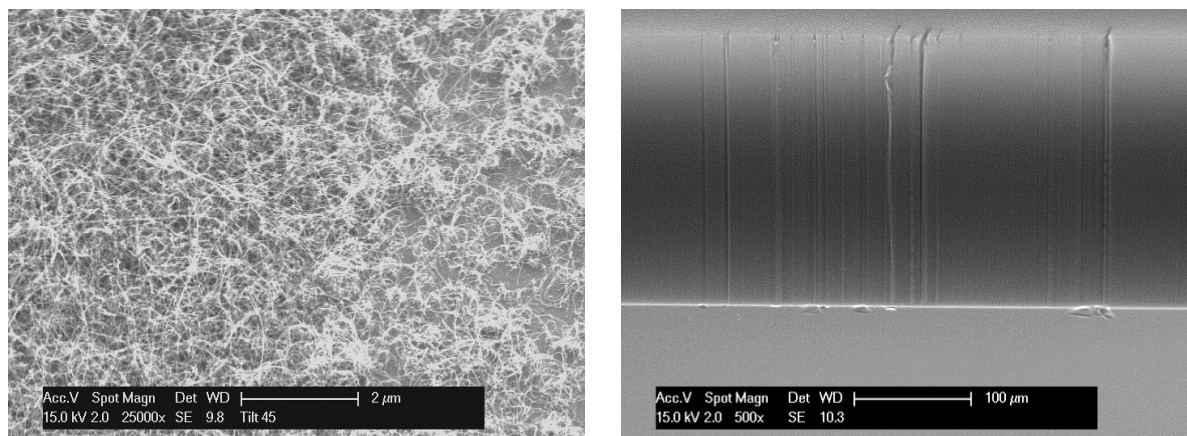
Figure 3.2: Random growth and vertical growth of CNT.

3.1.1.1 Observation of growth patterns

It was fascinating to observe that CNT growth occurred with some very specific patterns, which could be observed with the naked eye. These patterns were exactly the same for both trial runs, and persisted for the different recipes which produced them. Initially the cause of their origin was not given much attention, but it was soon realized that they were giving a strong clue about CNT growth in a CVD process. Fig. 3.3 shows photographs of these patterns.
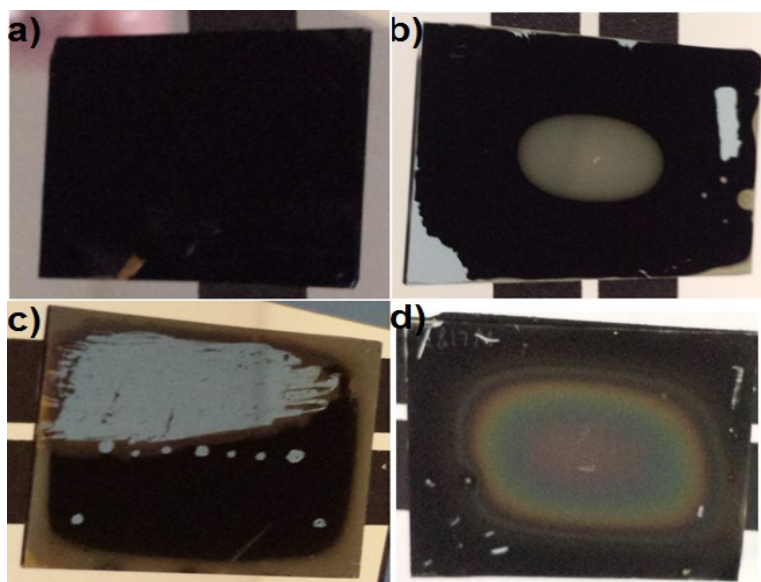
Figure 3.3: Images of fascinating growth patterns, observed for a few growth recipes: (a) Carpet-like growth; (b) Frame-like growth; (c) Reverse frame-like growth; (d) Contour-like growth patterns.

The patterns are classified into five groups, as listed below:

a. Carpet-like growth: Fig. 3.3a shows the picture of a carpet of CNT, with growth at every location on the substrate. This indicates that the substrate supported CNT growth everywhere. This, of course, is what we would like to achieve. Recipes 1, 2, 3, 4, 15 and 16 showed this growth pattern.

b. Frame-like growth: For recipes 5, 8 and 13, CNT grew only at the edges with the center portion showing no growth at all. This can be seen in fig. 3.3b; the pattern resembling a frame. The growth height was maximum at the boundaries of the wafer, and gradually decreased towards the interior.

c. Reverse frame-like growth: This is the third type of pattern, shown in fig. 3.3c. CNT started growing from the center, and the growth gradually tapered towards the boundaries. So this pattern is just the opposite of the frame. Recipes 6 and 18 exhibited growth with this type of pattern.

d. Contour-like growth: The fourth type of growth pattern appears in the shape of contour lines, as can be seen in fig. 3.3d. Further, the lines reflected different colors when viewed under light. The substrate appeared to be covered by a transparent, greasy film, and the variation in color probably meant that the film had different thicknesses at different regions. Recipes 7, 10 and 14 showed this type of growth pattern.

e. Random growth: Finally, some recipes gave random growth as explained, where CNT were only a few microns length, with no vertical alignment.

The fact that some of the recipes did not favor vertical growth demanded a valid explanation. It could be that these growth conditions were unfavorable for vertical CNT growth. However, it could also be that for these recipes, it would take a longer time for vertical growth to initiate. To test this idea, and also to understand the origin of the patterns, growth was performed again for 10 min time. Only one trial was performed and four observations were recorded per experiment. The following section reports the growth results this time.

3.1.2 Results for 10 min growth time

We would first take a look at the growth results, and then proceed with explanations. Fig. 3.4 shows the results of the 10 min growth run.
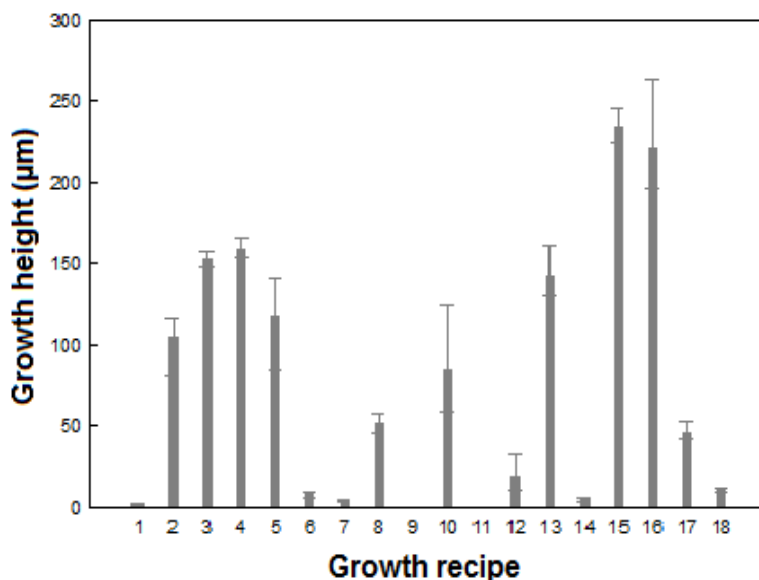
Figure 3.4: CNT growth for 10 min time for different growth recipes. One trial per recipe was performed this time, and four observations were recorded.

Observation 1: The first point to note is, growth has actually reduced this time. This is contrary to our expectations for the longer period of growth. After discarding possibilities like etching of CNT by H_2, it was concluded that this might be again due to the non-uniformity of the catalyst layer. Indeed, the order of the thickness meant that we were working with around 10 atoms of Fe. Clearly, our evaporator was not suited for depositing such ultra-thin layers. There was no alternative in this case, whatsoever, since other deposition machines in the cleanroom were not compatible with Fe.

Observation 2: In addition to the recipes which produced high vertical growth last time (2, 3, 4, 5, 13, 15 and 16), this time recipe 8 showed more growth, and recipes 10, 12 and 17 started to show growth. This had been a strong evidence to confirm our speculation, that for some recipes it indeed takes more time for the vertical alignment to start. Recipes 1, 6, 7, 14 and 18 continued to show less growth as before. Recipe 9 again produced only random growth, while recipe 11 did not produce growth once again.

3.1.2.1 Explanation of the growth patterns

We would like to see how the patterns looked this time. Table 3.1 provides a comparison between the recipes at the two growth times, and their respective growth patterns.

Table 3.1: Different CNT growth patterns and the recipes that produce them, for 5 min and 10 min growth times.

Growth pattern	Illustration	Growth recipe	
		5 min growth	**10 min growth**
Carpet		1, 2, 3, 4, 15, 16	1 ,2, 3, 4, 7, 12, 13, 14, 15, 16, 18,
Frame		5, 8, 13	5, 8
Reverse frame		6, 18	6
Contour		7, 10, 14	10
Random		9, 12, 17	9, 17
None		11	11

Recipes 1, 2, 3, 4, 15 and 16 showed carpet-like growth as before. Of the three frame-like recipes, 5 and 8 continued to show the same pattern; however 13 now showed a uniform carpet-like growth. This probably explains that growth had started from the boundaries for these recipes and gradually proceeded towards the center. For recipe 13, growth on the full wafer surface had already been achieved in the 10 min growth time, while for recipes 5 and 8, it would have probably taken longer to cover the entire substrate with CNT.

Of the reverse frame-like growth pattern, recipe 6 still showed the same; but now, its growth had proceeded almost towards the edge (meaning that, it almost resembled a carpet), while recipe 18 showed full carpet growth. This clearly explains that for these recipes, growth had started from the center and then proceeded towards the boundaries.

These strange phenomena of growth, sometimes progressing from the boundary towards the center, and sometimes in the other direction, can be best explained by a phenomenon called the *catalyst loading effect*, which causes more growth to happen in the center of a catalyst layer than its boundaries. Here we were probably observing the loading effect in one case, and its reverse analogue in the other. A strong point to support this speculation is, the growth height for recipe 6 and 18 were actually higher in the center than in the edges; and just the opposite for recipes 5, 8 and 13. This loading effect phenomenon was encountered several times during the course of this work, for both patterned and non-patterned growth of CNT. A detailed analysis had been done on this subject, and is presented in section 4.2 of the thesis.

Discussing about the contour-like growth; of the three recipes 7, 10 and 14 which were showing this pattern earlier, recipes 7 and 14 showed full carpet-like growth this time, while recipe 10 showed contour lines only in the central parts and a carpet at the boundaries, similar to the frame-like pattern. These results can be explained if we assume that due to higher growth at the boundaries of the 'frame', there had been a local depletion of the feedstock in the central parts. This might have resulted in the formation of an intermediate reaction product, which deposited on the substrate as a thin greasy film. This might well be one of the higher order hydrocarbons which were transiently produced in the reaction process. A similar result is reported in [42]. As a result, the growth had started from the edges and proceeded towards the center, with increasing growth time, gradually filling up the entire substrate. This explains why recipes 7 and 14 had complete carpet growth, while recipe 10 had a mixture of contour and frame-like patterns.

Recipes 9 and 17 produced random growth once again, while recipe 12 formed a carpet. This suggests that unless governed by totally unfavorable CVD conditions, it perhaps would take still more time for 9 and 17 to start the vertical alignment.

Finally, recipe 11 did not support growth this time as well, which indicates that its CVD conditions were just unfavorable for random or vertical growth.

From all these results, it was understood that every recipe which supported some form of growth pattern, gradually drifted towards the formation of a complete-surface vertically aligned CNT carpet. Further, the reverse-frame and frame-like patterns were formed due to catalyst loading effect and its reverse analogue respectively. Further, depletion of the feedstock in the growth regions resulted in an incompleteness of the growth-inducing reaction in the other regions. Finally, some recipes took a longer amount of time to initiate vertical CNT growth.

3.1.3 Analyses of the best-case and worst-case recipes

As a final part of this section, we will try to understand how, physically, different growth recipes contribute to different growth heights. From the earlier chapters, we have seen how each recipe has a specific substrate and CVD condition. From this approach, we will analyze the best case and worst case recipes. Specifically, we'll be answering the following questions:

- *Best-case:* How do recipes 15 and 16 produce the highest growth?
- *Worst-case:* Why does recipe 11 produce no growth at all?

Best-case analysis: Let us first consider recipe 16 first. It annealed the catalyst layer at a low temperature (400 ºC), but for a longer duration of time (5 min). This ensured that the layer got sufficient time to activate itself, without diffusing into the support layer that would occur at higher temperatures [81]. Further, the growth took place at a high temperature (650 ºC), and under moderate levels of C_2H_2 (40 sccm). The high growth temperature was beneficial for high growth lengths. This, coupled with the fact that the feedstock level had not been too high for catalyst poisoning, resulted in recipe 16 to be a high-performing one. Analyzing recipe 15; it had the right catalyst thickness (0.8nm), a high growth temperature (650 ºC) as 16, and a lower C_2H_2 flow rate. These are all positive conditions for high growth. However, an interesting observation lies in the annealing conditions; the catalyst was annealed at a high temperature (600 ºC) for a short time (1 min). Surprisingly, this had not caused its diffusion into the wafer. This was probably because of the short annealing time; 1 min of anneal might have been just enough to activate the layer, without any diffusion. These help us understand why recipes 15 and 16 are considered to be the best-case recipes. As we'll again see in this chapter, a low anneal temperature, but with a high anneal time, together with a high growth temperature and lower levels of feedstock supply, are the ideal conditions for high CNT growth.

Worst-case analysis: We tried to understand why there was a complete absence of growth by recipe 11. We infer that it was the low growth temperature (550 ºC), coupled with brief annealing conditions of the catalyst (500 ºC, 1 min), which were the chief factors. Looking at growth charts, we note that a temperature as low as 550 ºC is not suitable for high growth lengths. For instance, every recipe (1, 6, 7, 14, and 18) which grew at this temperature, resulted in short CNT heights. However, whereas these recipes had at least initiated the vertical growth process, recipe 11 did not produce any form of growth. This led us to consider the catalyst anneal conditions. We infer that the brief annealing condition was insufficient to activate the Fe layer (even when its thickness was as low as 0.5 nm). To support this argument, we look at recipe 17, which also had the same

annealing condition. The fact that recipe 17 grew at a high temperature (750 ^{O}C), suggests that the catalyst got re-annealed at these elevated temperatures before growth started. However, since the C_2H_2 feedstock was already introduced while the catalyst was still in the annealing process, it might have got poisoned early [82], hence terminating the growth reaction, and resulting in a poor growth. This effect of anneal time and temperature also helps to explain why recipe 1 showed at least some growth compared to recipe 11; even when it annealed at poorer conditions (400 ^{O}C, 1 min) and grew at 550 ^{O}C. Perhaps the reason is the lower levels of C_2H_2 in this case, which might have delayed the poisoning of the catalyst, thus allowing the re-anneal to occur for more time. This explains why recipes 1 and 17 at least had short growth, while recipe 11 had none.

So far, these analyses gave us a decent understanding on how the substrate and CVD parameters govern the growth of CNT. Understanding the dynamics of the growth system was valuable, as it helped us in explaining the results of the DOE optimization, which will be covered in the next section.

3.2 Taguchi optimization of growth height

We will now look at the predictions of the Taguchi DOE analysis, to find out the best recipe for maximizing the growth height. The analysis was performed in the manner described in section 2.3. Since we intended to maximize the height, larger-the-better approach was used with the SNR. Further, the analysis was performed on the results of the two trials of 5 min growth, and also from the 10 min growth. The main effect plots so obtained are presented in fig. 3.5a,b, and the results are summarized in table 3.2a. The ANOVA results are also provided in table 3.2b, to show the strength of each parameter in determining the CNT growth height.

$$L_{max5} \equiv \{P1_1, P2_2, P3_1, P4_2, P5_2, P6_3, P7_3, P8_1\}$$
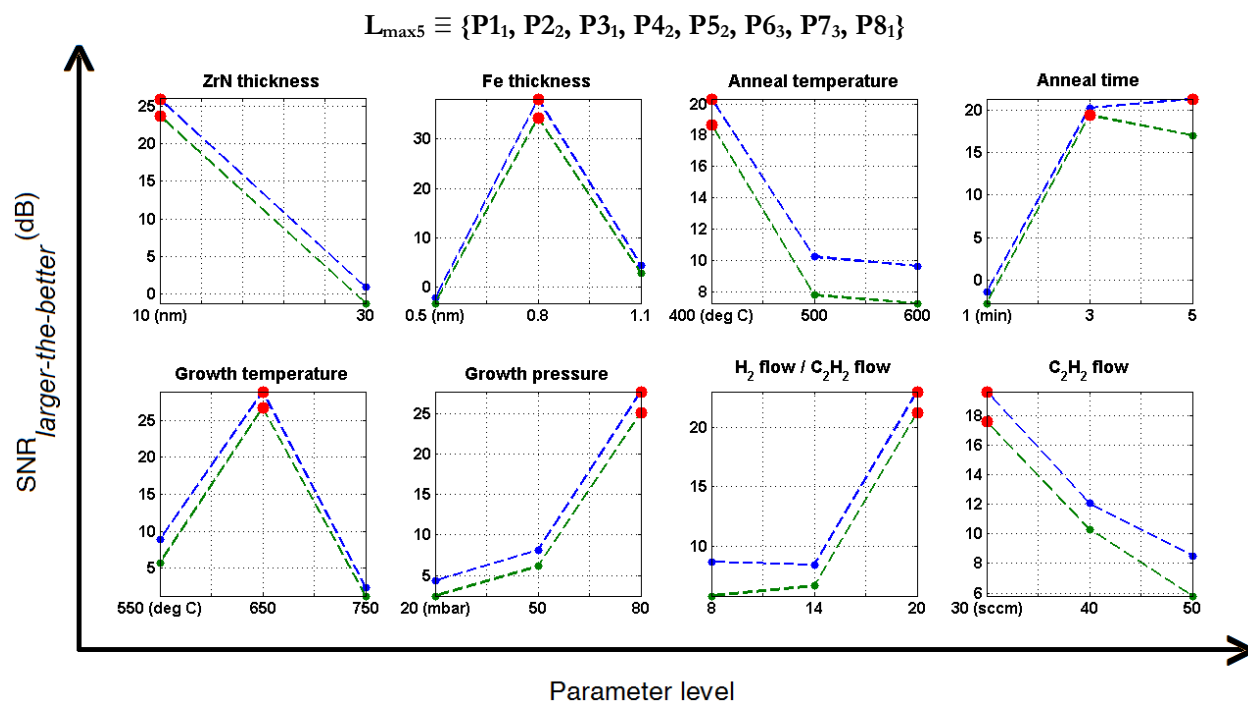
Figure 3.5a: Main effects plot generated from 5 min growth data, for trial 1 (in green) and trial 2 (in blue), showing the effect of the substrate and growth parameters on the growth height. The red points show the optimum levels of the parameters, for maximizing height.
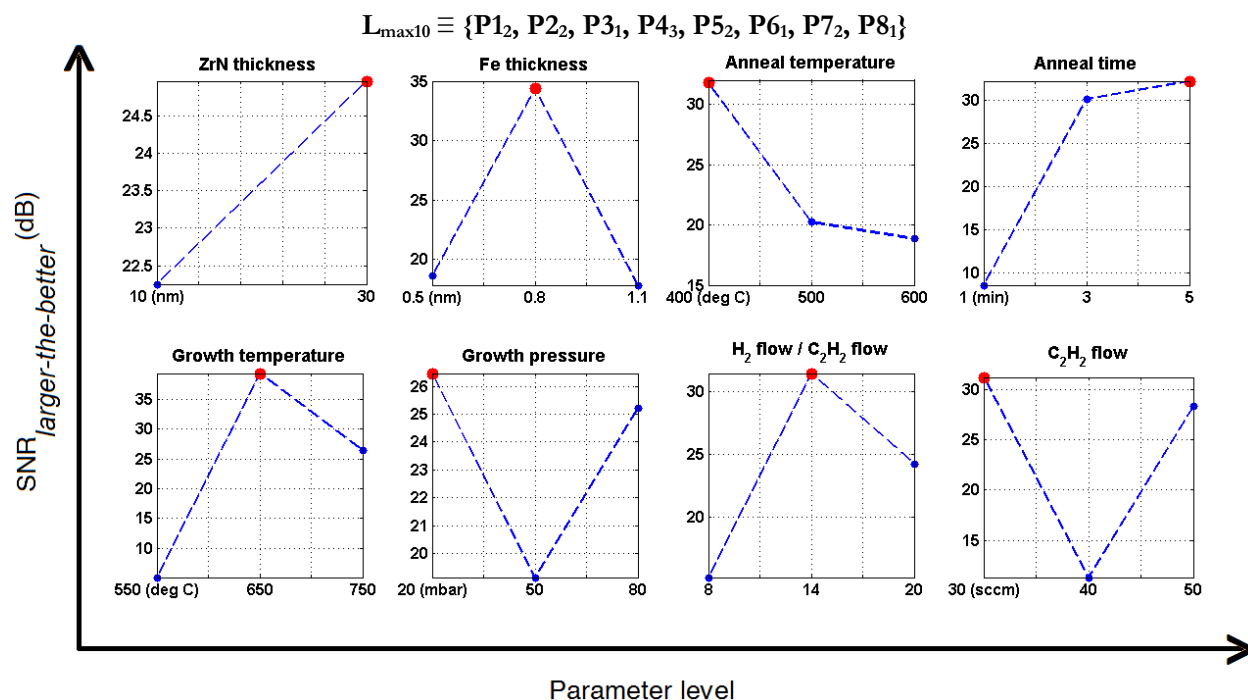
$$L_{max10} \equiv \{P1_2, P2_2, P3_1, P4_3, P5_2, P6_1, P7_2, P8_1\}$$

Figure 3.5b: Main effects plot generated from 10 min growth data.

Table 3.2a: Predicted growth recipes for maximum growth height of CNT, as obtained from Taguchi main effects plot.

Experiment		Name of optimized recipe	ZrN thickness (nm)	Fe thickness (nm)	Anneal temperature (^{O}C)	Anneal time (min)	Growth temperature (^{O}C)	Growth pressure (mbar)	H_2 flow / C_2H_2 flow	C_2H_2 flow (sccm)
5 min growth	Trial 1	L_{max5}	10	0.8	400	3	650	80	20	30
	Trial 2		10	0.8	400	5	650	80	20	30
10 min growth		L_{max10}	30	0.8	400	5	650	20	14	30

Table 3.2b: ANOVA table showing the strength of each parameter in optimizing the CNT growth height.

Experiment	Name of optimized recipe	ANOVA parameters	ZrN thickness	Fe thickness	Anneal temperature	Anneal time	Growth temperature	Growth pressure	H_2 flow / C_2H_2 flow	C_2H_2 flow
5 min growth	L_{max5}	F Prob > F	1.02 0.42	0.92 0.52	0.09 0.92	0.33 0.75	0.40 0.71	0.33 0.75	0.16 0.86	0.08 0.92
10 min growth	L_{max10}	F Prob > F	0.03 0.88	0.47 0.68	0.27 0.79	0.92 0.52	1.61 0.38	0.08 0.92	0.36 0.74	0.62 0.62

Observation1: The main effects plot from 5 min growth data is shown in fig. 3.5a. It reveals similar trends for trials 1 and 2. This is expected, as similar growth trends are observed from both the trial results. The predicted optimum catalyst/support layer thicknesses are 10 nm ZrN/0.8 nm Fe, and the catalyst anneal conditions are 400 °C/3 min. The optimum growth conditions are 650 °C at 80 mbar pressure, under 30 sccm C_2H_2 flow at a gas ratio of 20 (600 sccm H_2). This optimized recipe from 5 min growth results is given the name **L_{max5}**[6].

Observation 2: The main effects plot from 10 min growth data, as shown in fig. 3.5b, is slightly different. The predicted optimum catalyst/support layer thicknesses are 30 nm ZrN/0.8 nm Fe, which should be annealed at 400 °C/5 min. The optimum growth conditions are 650 °C at 20 mbar pressure, under 30 sccm C_2H_2 flow at a gas ratio of 14 (420 sccm H_2). This optimized recipe is given the name **L_{max10}**.

3.2.1 Experimental verification of optimized recipes (L_{max5}, L_{max10})

This is the last but the most important step in any DOE analysis. It shows whether the recipes are predicted accurately enough to work in real life. This is a test for the success of the DOE. It also gives an indication whether there had been a strong interaction between the parameters, or whether there had been some spurious source of noise affecting the experiment, reducing the accuracy of the analysis. As we would find out, one of the recipes is successful in optimization while the other is not. We will try to understand the reason behind this, and also throw some light about the growth conditions which led to the optimized height.

The L_{max5} and L_{max10} recipes were used to grow CNT. The samples were grown for 5 and 10 min respectively; and also for 30 min each for curiosity. Four observations were taken per sample and their average values are presented in table 3.3.

Table 3.3: Theoretical and experimental values of CNT growth height with the optimized recipes.

| Recipe	Growth time (min)	Theoretically predicted growth (mm)	Experimental growth (µm)
L_{max5}	5	288.70	224.75
	30		229.50
L_{max10}	10	4.58	462.50
	30		835.50

We derived some interesting conclusions from the table, which will now be discussed.

Observation 1: We can clearly see that L_{max5} had failed. The growths obtained, even though of high orders, were actually smaller than some of the **L_{18}** recipes themselves. We also note that growth essentially stopped after 5 min, as there was hardly any improvement in the results for 30 min growth. The theoretical growth height for this recipe was calculated to be 28.87 cm, a value much higher as compared to the experimental values.

Observation 2: Recipe L_{max10} gave more interesting results. We got CNT growth of more than 450 µm for a growth time of 10 min. When the growth was continued for 30 min, we achieved an ultra-long mean height of 835.5 µm, with one observation showing a super-growth of CNT of 906 µm (fig. 3.6)! This shows that this recipe had been successful. Also, the theoretical prediction of 4.58 mm is a value that was much closer to the

---

[6] In fact, the two optimum recipes from the two trials vary slightly only with respect to the anneal time. However, the main effects plot indicates that there would not be much difference in growth height for 3 min and 5 min annealing.

actual growth heights. In fact, when subsequent growths were attempted with this recipe, we continuously got heights of more than 600 μm every time. This reduction in length might again be attributed to problems with Fe deposition, but we now we were sure that this recipe was indeed the right one for CNT super growth.
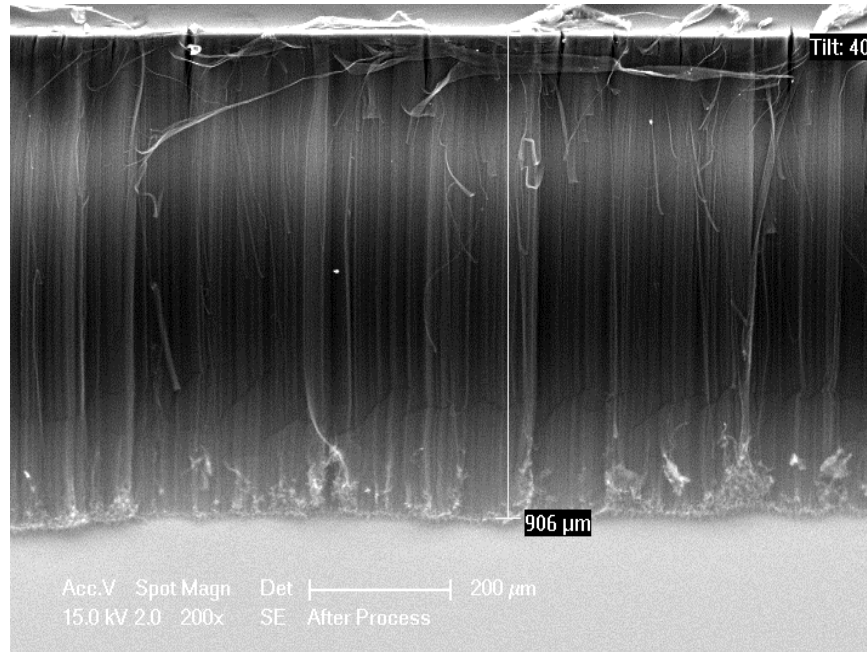
Figure 3.6: SEM image of CNT super-growth of about 1 mm, grown by the optimized recipe L_{max10}.

3.2.2 Reason behind the success of recipe L_{max10}

To find a probable reason why L_{max5} had not been as efficient as L_{max10}, let us reflect on the number of readings considered to generate them. As we know, for 5 min growth, 5 out of the total 18 either showed only random or no growth. So we had used 13 values for the Taguchi calculations, keeping the other values to 0. On the other hand, for 10 min growth, only 2 recipes did not work; so we worked with 16 values. From this, we conclude that for performing Taguchi analysis accurately, every recipe must be working. To avoid the situation of non-functional recipes, one should select the parameter levels with greater care in the design process. However, this requires an intuition, which comes from experience. Unfortunately, in our case, the Fe/ZrN substrate combination had not been tried before, and so we lacked this intuition at the start.

As a closure to this section, we would like to discuss how the different substrate and CVD conditions for L_{max10} played roles in the growth process. A discussion on the effect of parameters is never complete without considering their strength. We will thus be using the main effects and the ANOVA results simultaneously in our explanation.

Analysis of L_{max10}: As a starting point, we refer to the ANOVA results shown in table 3.2b. The parameters are classified as strong, moderate or weak, depending on their F-value. This classification is only qualitative in nature. A parameter is considered to be Strong if it has a F around 1, Weak if its F is less than 0.1, and Moderate for all values in the middle. For convenience, the metrics of L_{max10} are presented again in the table 3.4.

Table 3.4: Parameter levels of recipe L_{max10} and their strengths, as obtained by ANOVA.

Growth parameter	Level	F-value	Strength
ZrN thickness	30 nm	0.03	Weak
Fe thickness	0.8 nm	0.47	Moderate
Anneal temperature	400 ^{O}C	0.27	Moderate
Anneal time	5 min	0.92	Strong
Growth temperature	650 ^{O}C	1.61	Strong
Growth pressure	20 mbar	0.08	Weak
H$_2$ flow / C$_2$H$_2$ flow	14	0.36	Moderate
C$_2$H$_2$ flow	30 sccm	0.62	Moderate

The ZrN support layer thickness is a weak parameter, and does not have much role in the growth process. However the growth has a moderate dependence on the Fe layer thickness, the optimum being 0.8 nm. This incidentally corresponds also to the optimum height for the Nominal recipe, which we had observed in section 1.2.1.

The annealing conditions are 400 ^{O}C, 5 min. This shows that, for ultrathin catalyst layers, annealing at a low temperature, but for a longer duration of time, causes more efficient breakdown of the layer into nanoparticles. A higher anneal temperature would possibly cause diffusion of the Fe atoms into the ZrN. Shorter annealing times would not result in an efficient activation of the layer. In fact, we see that the anneal time is a strong parameter here, indicating its role in determining CNT growth.

Regarding the growth temperature, we had already seen that growth at 550 ^{O}C does not give good results. This shows that the higher the temperature, the better is the growth. This result, coupled with the fact that temperature is a strong parameter, is detrimental to our initial efforts of reducing the growth temperature. Recently a publication from our group reported promising CNT growth at temperatures as low as 350 ^{O}C [49]; however, the substrate conditions were different in the experiments as were the heights of CNT produced.

The next parameter is the reactor pressure. We see that it is a weak parameter, which suggests, growth is not affected by the pressure conditions.

Finally, we consider the gas flow rates, which are 30 sccm of C$_2$H$_2$ and 420 sccm of H$_2$. Both of these are moderate parameters. Lower levels of C$_2$H$_2$, with a high proportion of H$_2$ is favored for high growth, possibly because higher C$_2$H$_2$ levels would be prone to deposit a high amount of amorphous carbon on the catalyst layer, poisoning it prematurely, and preventing further growth. A high level of H$_2$ can convert the amorphous carbon back into volatile hydrocarbons, which can then take part in the growth reaction.

To conclude with our reasoning, it would be interesting to take a look back at the two high-performing recipes (15 and 16) which were analyzed before. We note that recipe L_{max10} is nothing but a combination of the favorable levels from the two recipes! This again helps us conclude the success of this recipe.

3.3 Catalyst deposition profile and the resulting CNT growth

As a final note to this chapter, we would present a brief discussion about the non-uniformity of the catalyst layer, which had been giving rise to variations in growth height. When we suspected that the Fe evaporator might be the cause for this, it was decided to grow CNT on an entire wafer using recipe 15, and probe the height at different locations. The result of this experiment is shown in fig. 3.7.
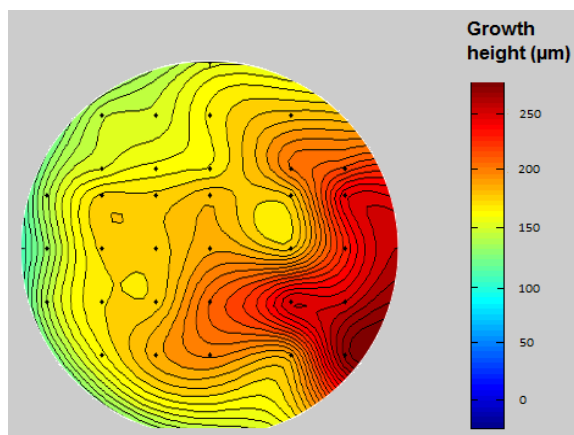
Figure 3.7: Variation in growth height on a wafer surface. The heights were measured at locations shown by the black dots, and the values were interpolated to cover the entire wafer surface. The contour lines are a useful means to represent regions of equal growth.

Clearly it can be seen that there is a significant variation in height over the complete wafer surface, varying from less than 150 μm to more than 250 μm. This much amount of variation could have arisen if there had been a severe non-uniformity in the CVD reactor at different locations on the chuck (in terms of temperature distribution, pressure or gas flow), or non-uniformity in the substrate layer thicknesses. The first speculation seemed unlikely as the BlackMagic was a commercial CVD reactor. Moreover, as we found, ZrN had little role in affecting the growth height; besides, sputtering usually gave good growth uniformity. So, as we discussed several times before, the evaporator might have been the real cause for this. The only way to tackle this problem, and still do meaningful statistics, was to take as much observations as possible and use their SNR values to reduce this 'noise'.

3.4 Summary

This chapter covered the results of CNT growth on an unpatterned catalyst layer. We looked at the 5 min and 10 min growth runs, analyzed their results, and in the process, got a thorough understanding of the growth process. We provided explanations for the origin of the growth patterns, as well as, how different recipes result in high or poor growth. Next we used these results to generate optimum recipes for CNT super-growth. From the verification experiments, we found that one of the recipes was successful in this task; growing almost mm-long CNT bundles. We then analyzed this recipe to understand the growth parameters that were responsible for this. As a final remark, it must be said that DOE analysis was not successful in achieving two of our early aims: the growth temperature could not be reduced below 650 ^{O}C, nor it was possible to reduce the sensitivity of the growth height towards the catalyst thickness. These can be interesting future work. In the next chapter, we will look at growth results on lithographically patterned catalyst islands, and see how the recipes have performed this time.

Chapter 4

Growth of vertical CNT on lithographically patterned catalyst layer

All our discussions so far were based on CNT growing on a continuous catalyst bed. Analyzing the unpatterned CNT growth, provides a good starting point for understanding its growth behavior, but it does not give the complete picture. Ultimately the CNT has to be grown on precise locations on the wafer, for any type of application. In other words, the catalyst layer has to be patterned lithographically, and controlled growth to be attempted on it. CNT growth control on patterned islands is a vast field, and demands dedicated research. This thesis is an attempt to carry out a preliminary research work on the hitherto less traversed path on patterned CNT growth mechanism.

The first step is to find the right chemistry for lithography of the catalyst layer. Since we were working with a novel combination of Fe/ZrN, expertise was limited. The following section will discuss how we standardized the lithography procedure to pattern the Fe layer.

4.1 Lithography procedure for patterning Fe on ZrN [P3256 process]
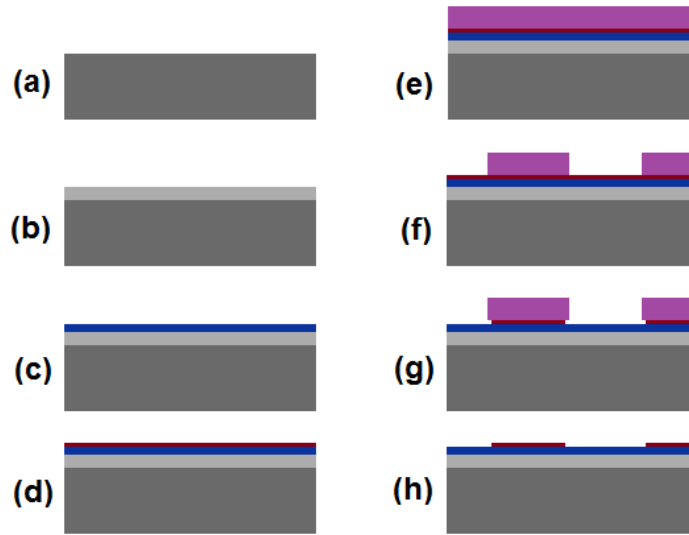
Figure 4.1: Overview of the P3256 process. Dark grey – Si; Light grey – SiO$_2$; Blue – ZrN; Brown – Fe; Purple – Photoresist. The figure is not to scale.

Shown in fig. 4.1 is the flowchart of the P3256 process, which was the lithographic process, standardized during this work. We started with a 100 mm p-type Si (100) wafer, and then thermally oxidized it. Then ZrN was sputtered at 350 $^{\circ}$C, followed by Fe deposition by evaporation. Next, the wafer was coated by SPR 3012 (a positive photoresist), which was then exposed under a mask and developed. After this, the exposed Fe layer was etched by 10% HNO$_3$ solution, and finally the resist stripped off by n-methylpyrrolidone (NMP) at 70 $^{\circ}$C, leaving only the patterned Fe layer. The complete process run is given in appendix D.1. The following section briefly explains how HNO$_3$ and NMP had been finalized for removing the Fe and PR respectively.

4.1.1 Finding the right chemistry for Fe etch

Different acidic solutions were initially tried to see which one best etched the Fe layer, and left the ZrN substrate unaffected. The common options in the cleanroom were H$_2$SO$_4$, HCl and HNO$_3$. Among them, the first two would have reacted with the ZrN layer, while HNO$_3$ was passive to it; hence it was selected. To observe the etching action of this reagent, the first experiments were performed by using a 10% HNO$_3$ soln. at room temperature for 1 minute, on the Fe/ZrN coated wafer. After rinsing and drying, the wafer was introduced in the BlackMagic, and a standard growth recipe used. To our surprise, full growth happened, indicating that Fe had not been etched at all. Assuming that the time of 1 min, or the room temperature operation had been the limiting factors, another wafer was exposed to 10% HNO$_3$ soln. at 50°C for 3 min. This time also, there was full CNT growth.

After brainstorming about the root of the problem [83], it was suspected that Fe was not getting etched because the Si from the backside was probably forming ions in HNO$_3$ more readily than Fe. Thus the wafer was behaving like an electrochemical cell (with the backside as the anode, and the front side the cathode), which prevented the Fe etch. If this was indeed happening, a way to prevent this was to introduce an insulating layer between the frontside and the backside of the wafer, to stop the electrochemical action. It was thus decided to oxidize the wafer to a depth of 100 nm first, and then continue with depositing ZrN and Fe.

This technique worked, and the etching was successful. After solving this problem, three different values of reaction time and temperature were tested. By attempting CNT growth, it was inferred if the Fe had been etched. The results are listed table 4.1. As may be seen, only the last chemistry successfully etched the Fe. So this was used subsequently for lithography.

Table 4.1: Etchant chemistry for Fe and the corresponding CNT growth results and conclusions.

Fe-etch chemistry	CNT growth result	Inference
10% HNO3, Room temperature, 1 min	Full growth	Fe was not etch
10% HNO3, Room temperature, 3 min	Full growth	Fe did not etch
10% HNO3, 50 ^{O}C, 3 min	No growth	Fe etched

4.1.2 Finding the right chemistry for photoresist (SPR 3012) strip

The next step was to identify the chemistry for removing the photoresist. Three common chemicals (Acetone/Isopropanol, Hexane and n-methylpyrrolidone (NMP)), used to strip resist, were tried; then the Fe etched, and CNT growth attempted. Their results are summarized in table 4.2. Looking at the results, we can see that the third option worked best for us. Hence the complete flowchart had been standardized.

Table 4.2: Chemistry for Photoresist removal and the corresponding CNT growth results and conclusions.

PR-strip chemistry	CNT growth result	Inference
Acetone spray + Isopropanol dip, Room temperature, 5min	Non uniform growth Scattered PR residues	PR did not strip completely
Hexane, Room temperature, 5 min	No growth	PR did not strip at all
NMP, 70 ^{O}C, 5 min	Good growth (~120 μm)	PR stripped completely

In addition to the process described here, there was also the option for doing a lift-off process, which would pattern the resist first and then deposit Fe. However, this would have probably caused a shadowing of the Fe layer inside the cavities. Considering the sensitivity of our process to the Fe layer thickness, the lift-off was not tried in the end, and we continued with using the P3256 process for subsequent experiments. Now that we were successful in growing CNT on island patterns, a lot of different masks were used to study the growth behavior. Also, a sure prerogative was to take beautiful pictures of CNT artwork, highly inspired by [84]! Fig. 4.2 shows collage of a few of the growth results.
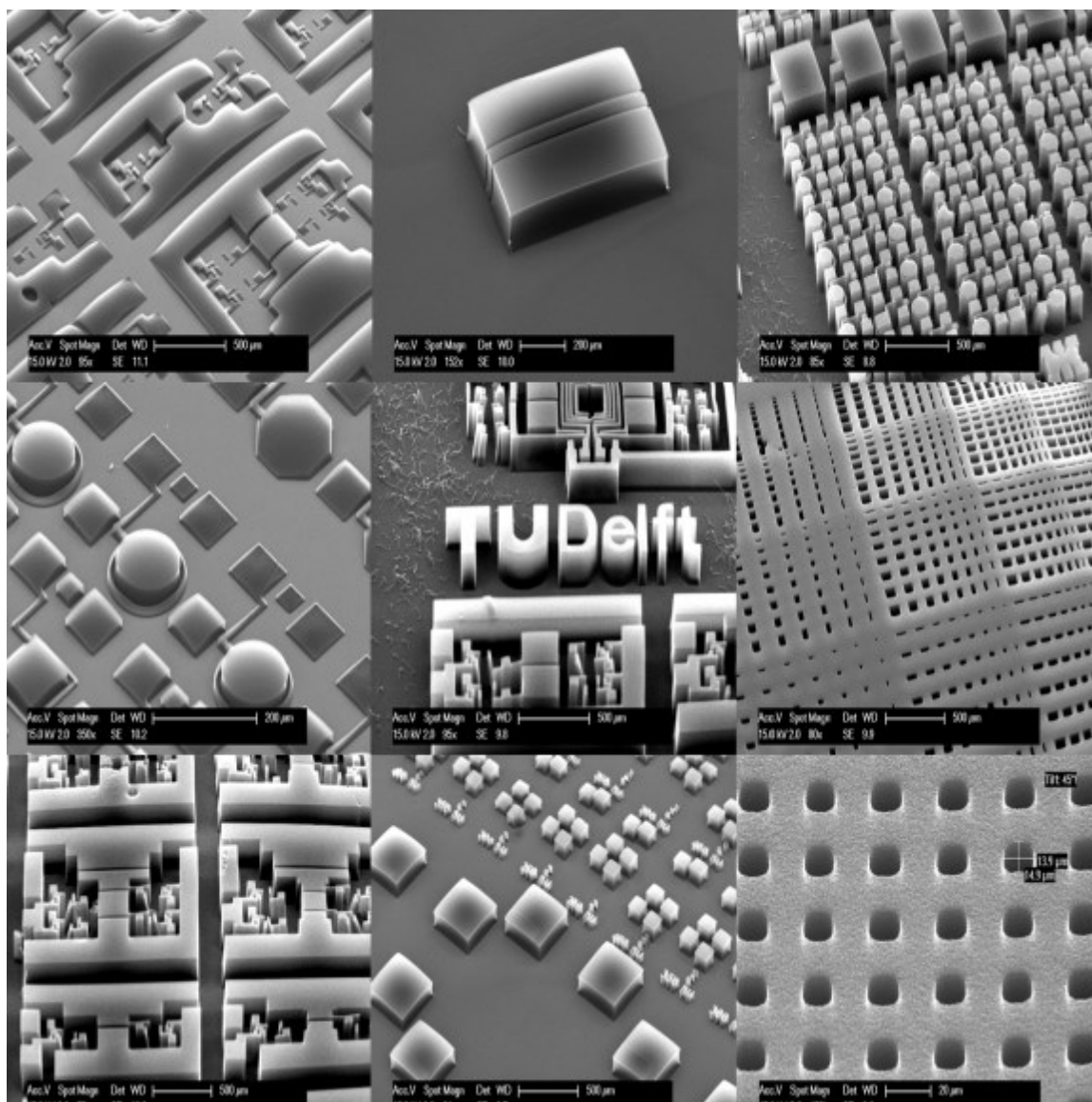
Figure 4.2: A collage of CNT growth on patterned Fe islands with the P3256 process. Different masks were used to observe the growth in different types of island patterns.

4.2 Catalyst loading effect on patterned CNT growth

It was during our growth experiments, that we encountered the catalyst loading effect once again. The growth of CNT was not uniform with some of the masks; it was much higher in the center than near the boundaries of the patterns, just as we had seen in the previous chapter. We soon realized that this would be a major obstacle towards achieving uniform growth on island patterns. Surely, this effect had to be understood and overcome first, before we could proceed further with our idea of CNT integration.

4.2.1 Analysis of loading effect

In order to understand the loading effect better, let us take a look at a few of the growth results shown in fig. 4.4 where this effect is very apparent. Initially, this was speculated to be happening due to some defect in the lithography process, or non-uniformity in the catalyst layer. However, when the results persisted repeatedly over several batches of wafers and growth conditions, we suspected that there must have been a different cause for it. A literature study on patterned CNT growth showed us that this effect had also been observed by a few other researchers. Based on the terminology first used in the work of Hart [85], we called this phenomenon the *catalyst loading effect*. In the last chapter, where we did a preliminary investigation on this effect, we came to the conclusion that this effect is time-dependent, and the wafer gradually attains uniformity in growth when all the regions start taking part in the growth process. However, this might have held true for unpatterned catalyst layers. As we are going to see shortly, many additional effects came into existence when the catalyst was patterned. Hence, the loading effect phenomenon really deserved a thorough understanding.

There was a decent amount of literature available, which had discussed the origin of this phenomenon, and research work done by the groups of Hart and Slocum [86-89], Bronikowski [42, 90, 91] and Campbell [92-94] extensively studied this effect. Based on a collective literature survey of the work of these three groups, it was found that this effect depended on the following three factors:

- Dependency on the catalyst island size and its fill-factor
- Dependency on the catalyst layer thickness
- Dependency on the CVD reactor non-uniformity

We will now be looking at each one of them, and explain how they can affect the CNT growth behavior.

1. Dependency on the catalyst island size and its fill-factor: We will explain how the CNT growth height depends on the size of the patterned island and its fill-factor. The term fill-factor ($\mathbf{F}$) denotes the ratio of the catalyst island area to the total wafer area. This means that some masks have a high $\mathbf{F}$ value, while some have a low value. Likewise, an unpatterned catalyst surface has $\mathbf{F}$ of unity while a surface with no catalyst at all, has a $\mathbf{F}$ of zero. Fig. 4.3 helps to understand the concept.


Figure 4.3: Conceptual pictures of two types of catalyst island distributions. The first one consists of four big islands separated by a small distance, and the second one consists of four small islands separated by a large distance. This results in a higher fill-factor for the first case and a lower fill-factor for the second.

Effect of island size: As Bronikowski in [42] had observed, on islands with larger sizes, the growing CNT bundles tended to adhere together due to van der Waals interaction between them, forming thick fiber-like structures, which grew with a high degree of vertical alignment. On the other hand, for smaller islands, the CNT did not adhere, but grew as individual filaments, often leading to a failure in vertical alignment. In these situations, random growth took place. This meant that for a fixed growth density, larger sized islands could support better growth than smaller islands. So this placed a limit on the minimum island size needed for vertical CNT growth. Further, when the island size was large enough to promote the vertical alignment, a higher CNT growth occurred in those regions where there were more number of CNT fibers growing in the vicinity. This implied that the growth height was more in the center than towards the boundaries of the island. These two effects can be clearly seen in fig. 4.4. This type of loading, which depended only on the island *size*, is termed by us as the *Local loading effect*.
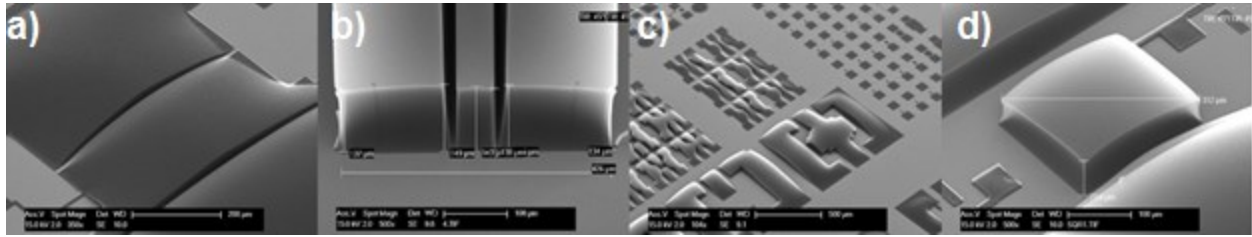
Figure 4.4: Images showing the catalyst loading effect on the CNT growth height. Clearly there is more growth towards the center of the islands than towards the boundaries. Also larger sized islands support better vertical growth than the smaller ones, showing the local loading effect.

Effect of island fill-factor: Now we would consider what happens when there is a higher or lower distribution of islands at a particular region. Research reported by Campbell et al. [92] indicated that high length CNT with lesser number of walls grew on high **F** islands, while CNT with shorter length and more number of walls were produced on low **F** islands. This meant that the amount of carbon formed by decomposition of the feedstock by the catalyst was independent of its area. Thus, low **F** islands were prone to suffer early poisoning by a higher amount of carbon deposition, losing their activity early in the growth period, and leading to shorter CNT growth heights. In the same lines, large **F** islands supported the growth reaction for a longer time, leading to a higher growth. So this placed a limit on the minimum fill-factor required for vertical growth to happen. This type of catalyst loading, which occurred due to the presence of a finite *fill-factor* of the catalyst island, is termed as the *Global loading effect*. Based on data presented by Bronikowski in [42], a graph was plotted between the CNT height and the island fill-factor, shown in fig. 4.5. We can see that there is an approximately logarithmic dependence between the two factors.
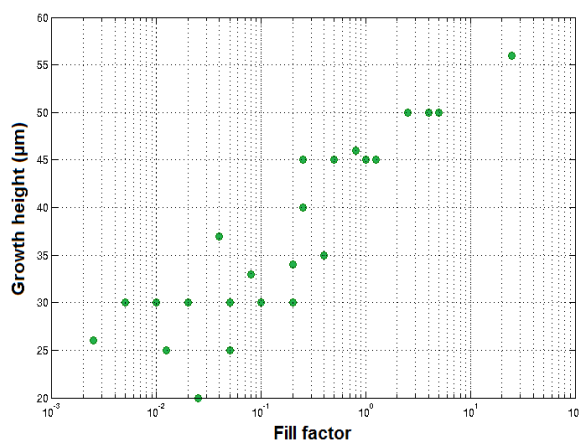
Figure 4.5: Variation of CNT growth height with the island fill-factor[7]; plotted from data presented in the work of Bronikowski [42]. An approximately logarithmic increase in growth height is observed.

To come up with a theory which could explain both the local and global loading effects, we looked at the growth reaction mechanism in more details. When the carbon-containing feedstock came in contact with the catalyst particles, it did not immediately break down into elemental carbon; but higher order hydrocarbons were formed in the reaction process (as seen in chapter 3). These molecular by-products reacted more efficiently with the catalyst particles than the original feedstock itself. Now, for large-sized islands, or with regions of high fill-factor, these intermediates were formed in greater quantities, leading to an increased reaction rate, and causing high density CNT growth. The growing CNT bundles then experienced an increased van der Waal's interaction, leading to better vertical alignment and thus higher growth heights. On the other hand, for the low fill-factor regions or towards the edges of the islands, the quantity of these intermediates started to decrease, and so, the growth height. To summarize, we see that two effects determined the local and global loading effects. One was the early poisoning of the low $\mathbf{F}$ regions, leading to termination of the growth reaction on them. The other was the distribution of the reaction intermediates, which was more in the high $\mathbf{F}$ regions, causing better growth on them.

To prevent (or reduce) the loading effect, increasing the feedstock flow was identified as a solution. It would have yielded a higher concentration of intermediates, which could then distribute to every island, and on every location on an island, thus facilitating more uniform growth. But in this case, chances of catalyst poisoning would also increase for the low $\mathbf{F}$ islands. This could, however, be circumvented by reducing the feedstock supply once vertical alignment set in, thereby prolonging the poisoning effect (although this would result in a lower growth rate). Also, increasing the flow of the carrier gas could sweep these intermediates away, redistributing them evenly to all the growth sites. Experimenting with different feedstock gases (which would produce different intermediate products) would give rise to a   better understanding of this phenomenon.

To conclude this section, we would like to briefly mention a third effect, which is the interaction between the local and global loading effects. This means that, a higher CNT growth would happen in the direction of a neighboring larger island or a high $\mathbf{F}$ region. These interactions are clearly visible in fig. 4.6. Firstly, higher growth took place on the octagonal islands than the squares, which signified the local effect. Secondly, the

---

[7] Here fill-factor has a slightly different definition; it is the ratio between the island diameter (and not the area) to its spacing with a neighboring island.

growth on the squares to the bottom-left of the image, was biased towards the high $\mathbf{F}$ regions of neighboring octagons, which signified the global effect. We can also see that growth on the squares in the central region have almost no such bias, which is because the $\mathbf{F}$ for those regions is below the threshold.
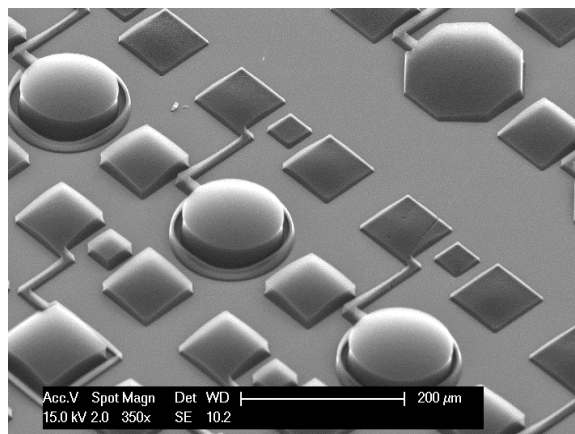
Figure 4.6: Image of a growth region, which clearly exhibits the interaction between the local and global loading effects.

2. Catalyst layer thickness dependency: Earlier we had seen how sensitive the dependence of the CNT height was on the catalyst film thickness, and how there existed an optimum level of thickness for high growth. Now we will take a look at how a film, which had been deposited to its optimum thickness, could also give rise to loading effect; especially if the thickness was large. Using thick layers of catalyst for CNT growth could give rise to two problems. Firstly, they would have to be well-annealed at high enough temperatures and time for efficient activation. Poor and non-uniform annealing would result in non-uniformity in growth height. Secondly, even after annealing them, the size of the as-formed nanoparticles would be quite large. The CNT which would grow from them, would have a lower growth density. Lack of high density could again result in poor vertical alignment. An explanation on the dependence of CNT height and diameter on the catalyst layer, may be found in [95, 96]. In our case, however, this was problem since the catalyst layer thickness was indeed quite low, to cause either of these problems.

3. CVD chamber dependency: For uniform CNT growth, the CVD reactor would also have to be homogeneous in terms of growth conditions. The reactor usually has a chuck on which the wafer is placed. The chuck is heated from the bottom and the top by heaters. Surrounding the chuck are holes, through which jets of gases impinge on the wafer, facilitating the chemical reaction to take place. A standard commercial reactor should guarantee complete uniformity in the temperature and pressure distribution, the gas flow volumes and rates at every position on the chuck. However, poor design of the reactor chamber (or when using a home-built reactor) may violate these, and there may be spatial and temporal non-uniformity of these parameters, which can cause severe non-uniformity in growth. Considering gas flow, not only the rate and volume, but maintaining uniformity of the flow shape is also necessary. For low growth rates, small non-uniformities would not affect much in the growth process; however, for higher growth rates, these factors could be extremely critical [86]. Further, the temperature non-uniformity is linked to the inhomogeneity in the catalyst layer activation as well. A good account of CNT growth behavior depending on the reactor properties is presented in [85]. An introductory discussion on the effect of gas flow and temperature distribution in the reactor may be found in [97]. Besides there are a decent number of publications by several groups [38, 98, 99] which have researched on this topic.

4.2.1.1 Growth results with different masks

Since we were interested in understanding the nature of the loading effect, different masks were used for patterning the catalyst islands, and subsequently they resulted in islands of different sizes and fill factors. Fig. 4.4 showed us how there was a strong presence of (local) loading effect with a low F mask. When a different mask was used (with a very high F), there was highly precise and uniform CNT growth on every island, with almost zero loading effect. Fig. 4.7 shows the result of CNT growth with this mask. The reasoning behind this was intuitive; a collection of very high F islands could be considered as one which was close to an unpatterned layer of catalyst. As a result, loading effect reduced as well. Interestingly, the growth height for this case was around 200 μm (with the Nominal recipe), as compared to the 250 μm of growth obtained for non-patterned catalyst layer.
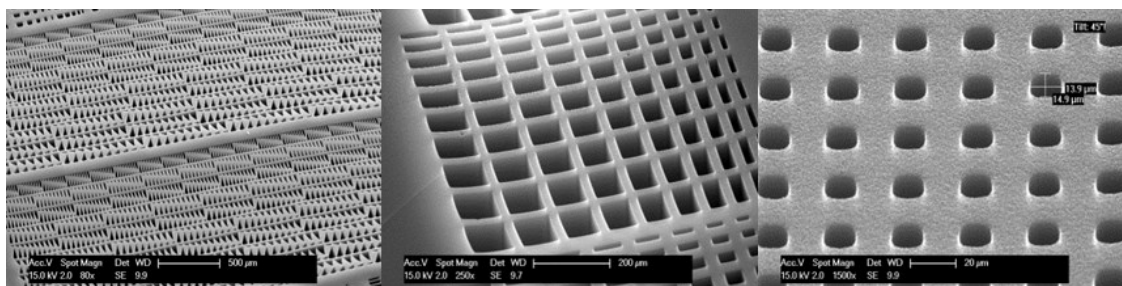
Figure 4.7: CNT growth with a high fill-factor mask showing almost zero loading effect.

It was also decided to use a negative resist for litho-patterning of the Fe layer, and growth was tried with the same high F mask as used just before (this would have given us growth in a low F case). Growth was attempted, and there was only random growth on the catalyst islands, as seen in fig. 4.8. A likely explanation for this was, the F became too low to promote any vertical alignment of CNT at all. So, till now, we had been experimenting with CNT growth using masks with high and low F, and were seeing the loading effect on CNT growth. This was giving us only a qualitative picture. The islands had to be patterned in such a way which would enable us to carry out an orderly and quantitative study. For this reason, it was decided to design a mask specifically dedicated to study this phenomenon.

The following section discusses how we logically used the concepts of the global and loading effects, in coming up with an intelligently designed mask.
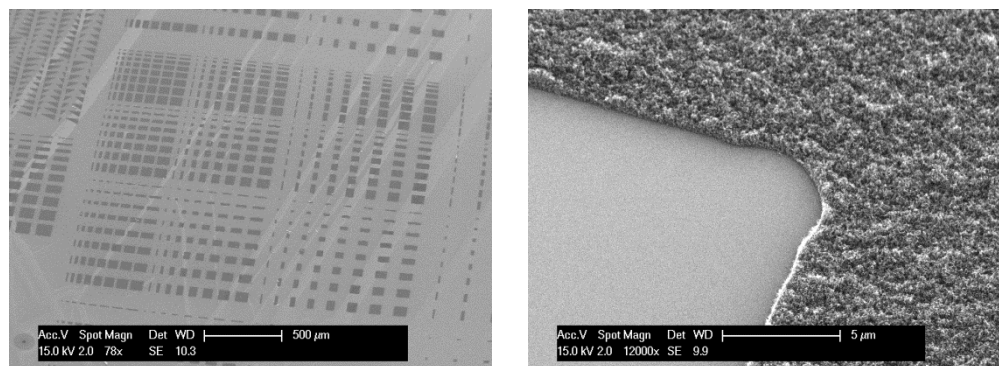

Figure 4.8: CNT growth attempted with a negative PR, which resulted in only random growth. Also a close-up view of an island is shown.

### 4.2.2 Motivation for mask design to quantitatively study the loading effect

4.2.2.1 Philosophy behind implementing the design: Understanding loading effect from simulations

From all the previous growth results, the primary observation was that, the growth height of CNT reduced when the catalyst layer was patterned. Using this as the first principle, we considered an ideal case where the layer which was infinite in extent. Since there were no *boundaries* to this island, the growth conditions were homogeneous everywhere, there would be no local or global loading effects, and growth height would be the same everywhere, solely determined by the process conditions. We assumed that the height for this case to be 1 a.u. (arbitrary unit), as shown in fig. 4.9a.

In the real world, the layer would be patterned on wafer, leading to a boundary. As a result of its finite size, it would suffer from a local loading effect, with the height of the CNT bundles reducing from the center to the boundaries. Looking back at the images where this effect was prominent, we found that the height followed almost a Gaussian distribution (fig. 4.4, 4.10). Likewise, we simulated a Gaussian distribution of heights on a patterned catalyst layer, as shown in fig. 4.9b. The same is represented as a 3-D plot in fig. 4.9c. In these figures, the red region corresponds to the height on the infinitely-spread layer in the ideal case (which was 1 a.u.). The blue regions at the periphery could either be equal to zero (fig. 4.4a) or it might have some finite values (fig. 4.4c). So, this represents the local loading, and the growth shows a variation because there is a boundary to the catalyst layer.
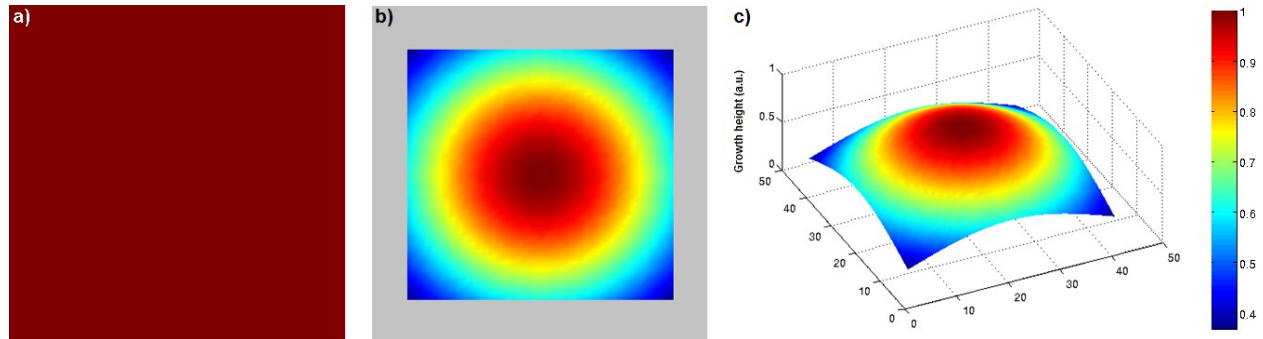
Figure 4.9a: Uniform growth height of 1 a.u. on a catalyst layer, which is of infinite extent; hence no loading effect is present (ideal case). **Figure 4.9b:** Simulation showing the growth height distribution of CNT bundles due to local loading effect, when the layer has been patterned. The grey region shows the bare wafer surface. **Figure 4.9c:** A 3D representation of the same. The scale represents the maximum growth as 1 a.u (in dark red).
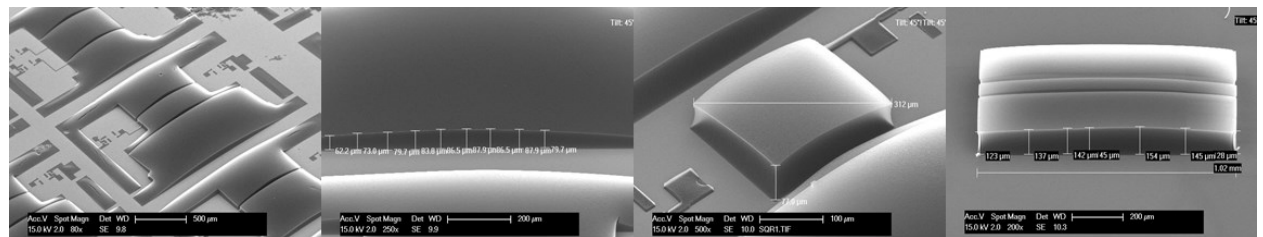

Figure 4.10: Gaussian growth profile of CNT bundles, from local loading effect, similar to fig. 4.4.

Now, let us not consider the local loading for a while, and think that the catalyst island had been patterned into equally spaced islands. In the ideal case, the growth height on each of the islands would be 1 a.u, as shown in fig. 4.11a. However, now the global loading sets in because of the presence of a finite fill-factor, and so the growth height gets reduced. For simulation purposes, we assumed that the growth has dropped to 0.75

a.u (yellow in the scale-bar), as shown in fig. 4.11b. Now introducing local loading to this would mean that on each of the islands, the peak height at the center would be the same (i.e., 0.75 a.u), which would then gradually taper down towards the boundaries, again following a Gaussian profile, similar to the case of the single island. This condition is shown in fig. 4.11c.

So, till now we looked at an infinite catalyst layer and then saw how the local and global loading effects, could cause variation in growth. However, the islands were placed too far apart to allow any interaction of these effects. The black square, shown in fig. 4.11c, conceptually shows the region of interaction of one island. Similar regions exist for all the islands.
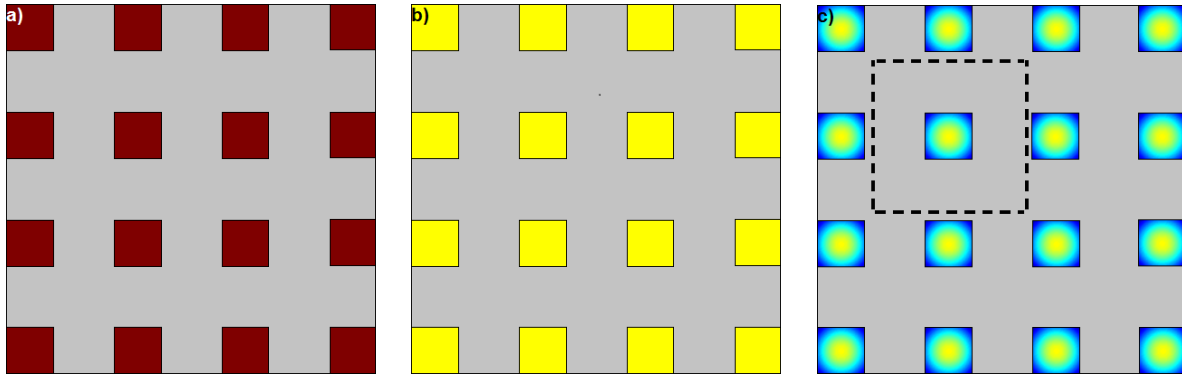
Figure 4.11a: Uniform growth of 1 a.u. on patterned islands, as expected in the ideal case. **Figure 4.11b:** Considering only the global loading effect gives a lesser growth height, which depends on the fill-factor of the islands. The growth is assumed to be 0.75 a.u. in this case. **Figure 4.11c:** When local loading is also included, the growth again follows a Gaussian pattern, which has a peak height of 0.75 a.u. Also shown in the figure is the region of interaction of one island. Similar regions exist for all the islands.

Now we will see how the height gets affected, when the patterns are located within this region of interaction. To start with, let us again neglect the local loading effect and consider only the global effect. Since the fill-factor would be higher now, there would be more growth on the individual patterns. We assumed this to be 0.85 a.u. (orange in the scale bar), as shown in fig. 4.12a. Adding the local loading to this, we would get a profile, as shown in fig. 4.12b; again the growth would start from a peak height 0f 0.8 a.u. in the central parts, and gradually taper towards the boundaries.

At this point, we would consider the effect of interaction between the two effects, which was physically seen in fig. 4.6. As shown in fig. 4.12b, many islands have now come within the region of interaction. Immediately, the two effects would start interacting, which would mean that the CNT growing on the different islands would help each other to grow with a better degree of vertical alignment. Due to this, a fascinating thing would happen: the entire group of islands would start to show a local loading phenomenon, but occurring at a global scale (at every region of the wafer), and the different islands would behave like one big island.

As a result, there would be an increase in the growth height all over the wafer, again following a Gaussian-like distribution. In other words, the central islands would experience a greater increase in height, compared to the peripheral islands. In these simulations, we had assumed that the growth in the central island increased to 0.95 a.u (red in the scale-bar), and the other islands subsequently had a lesser, but finite increase. The result is shown in fig. 4.12c. This completes our analysis on the local and global loading effects.
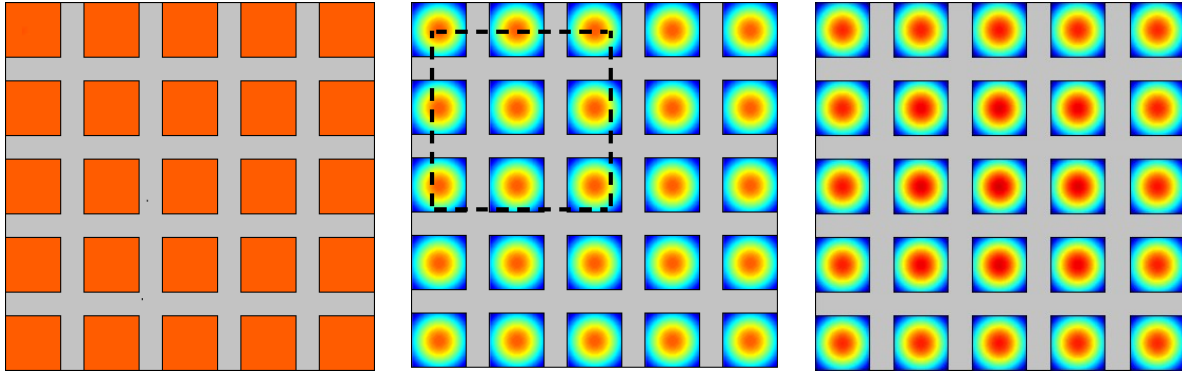
Figure 4.12a: Uniform growth height of 0.85 a.u. obtained on each island, for a higher value of fill-factor. Only the global loading effect is considered here. **Figure 4.12b:** Distribution of height when the local loading effect is also considered. The region of interaction is shown again for reference. It may be noted that now, many islands are situated within its range. **Figure 4.12c:** Simulation of the local loading effect, which again occurs as the islands begin to interact with each other, and start behaving like one whole island. This causes a redistribution of height, causing the central islands to have more growth than the islands at boundaries.

To remind the reader again, this had only been a qualitative analysis based on various growth results from different types of masks, and these conclusions were generalized from observing the different growth patterns. The *quantitative* study of these effects entailed the creation of the mask, which would have patterns of various dimensions and spacing, so that it could give a quantitative idea about the loading effect phenomenon.

4.2.2.2 Brief description of the P3256_V2_CATALYST mask

At the starting point, we were absolutely clueless which kinds of shapes, sizes or separations were needed to include in the mask. Keeping in mind the ultimate goal of this thesis, the dimensions of the patterns would have to be such that, they corresponded to industry standards of TSV-technology. Looking at the ITRS predictions [19], we found that for the year 2014, the diameter of a TSV was predicted to be 1.2 μm. In lines with this prediction, the mask had to be designed with a minimum pattern dimension of 1.2 μm. However, due to the limit of the mask fabrication machine[8], the minimum dimension was kept at 2 μm. Other patterns were made with gradually increasing dimensions. The next consideration was the separation between adjacent patterns. Referring again to the ITRS roadmap the minimum separation was 0.5 μm. But due to the limitation of the fabrication machine, it was maintained at 2 μm. The final consideration was to determine that the separation would be, between the patterns. For this, the work of Bronikowski [42] was used as the reference. In his work, CNT growth was studied for three separation regimes: Dense, Intermediate and Sparse, having fill-factors of 2.5, 0.25 and 0.1 respectively.

For designing the mask, we assumed that Dense would mean a **F** > 1, Intermediate would have a range of **F** from 0.1 to 1, and Sparse would have a **F** of 0.1. Also, in lines of Bronikowski, it was believed that in the Sparse case, the islands would be situated too far away from each other to interact. Accordingly, the patterns were separated by such distances, which resulted in different values of **F**. Table 4.3 indicates the different sizes and **F**-values as used in our design. The dimension is represented as a variable x (where $x = 1$ corresponds to a size of 1 μm), and **F** is represented as a reciprocal of the variable y. Most of the patterns were square in shape with a size of x-by-x; however there were also some other shapes, which were included

---

[8] The mask was fabricated with Heidelberg DWL200 fabrication machine.

to observe how the growth occurred on these islands. The collection of all kinds of shapes which have been used in the mask is represented in fig. 4.13.

Table 4.3: List of the various pattern dimensions (x) and their fill-factors ($F = 1/y$) used in the design.

x (μm)	2	2.5	5	10	25	50	100	500
y		0.2	0.5	0.8	1	2.5	5	10
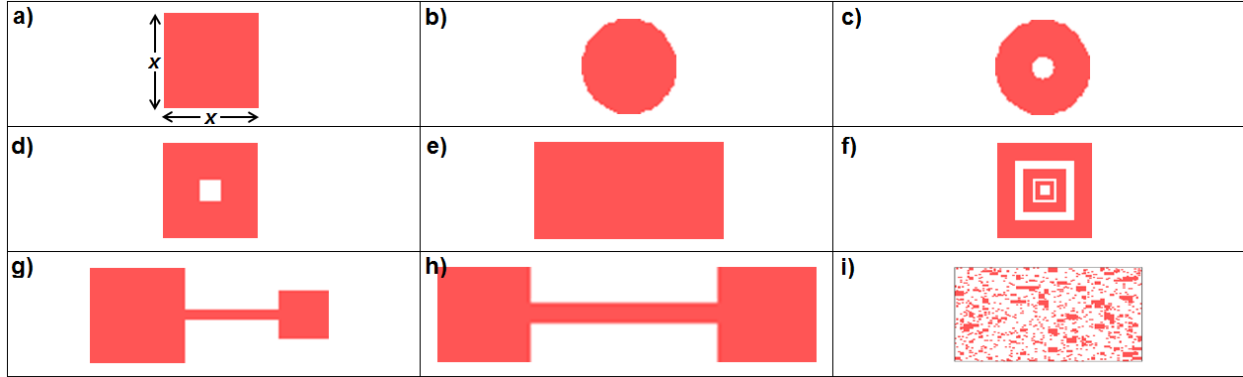
Figure 4.13: Different shapes (and their relative sizes), which had been used for P3256_V2_CATALYST mask: a – Square; b – Circle; c – Donut; d – Square donut; e – Rectangle; f – Spiral; g – Bridge 1; h – Bridge 2; i – Random.

In total, the mask contained 5 layouts, with different combinations of shapes, sizes and separations of the patterns. Detailed description of the layouts is beyond the scope of this chapter, and the interested reader may refer to appendix C. Fig. 4.14 shows the schematic of the P3256_V2_CATALYST mask.
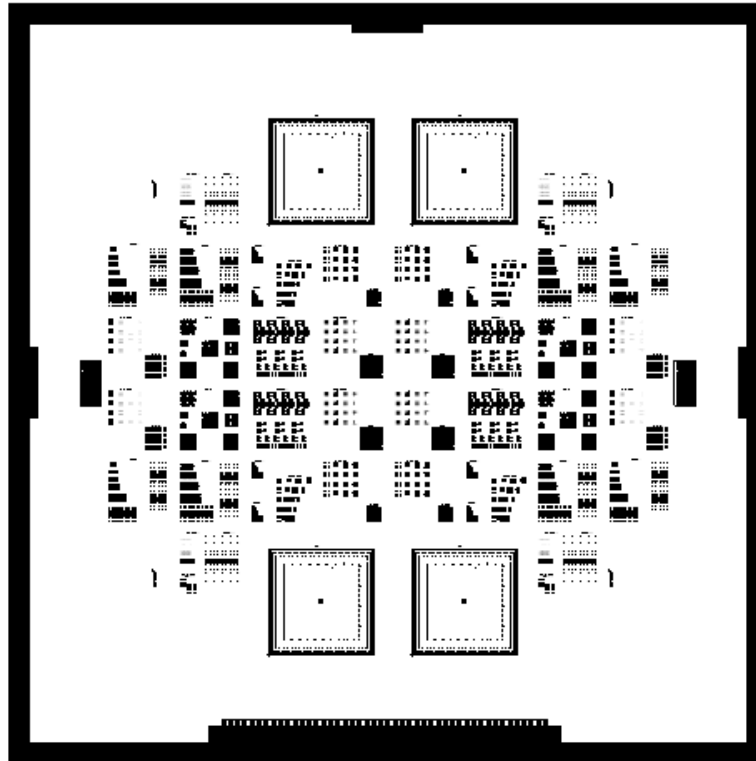
Figure 4.14: Layout of the P3256_V2_CATALYST mask.

4.3 Results of patterned CNT growth with the P3256_V2_CATALYST mask

Using the P3256_V2_CATALYST mask and with the lithography process of P3256, the catalyst layer was patterned and CNT growth was first attempted with the Nominal recipe for 5 min. As we may recall, we had obtained 250 μm growth heights on unpatterned catalyst. We wanted to test the efficiency of this recipe on patterned islands, and the results are shown in fig. 4.15. It can be seen that the Nominal recipe failed to provide growth of more than 10 μm for any pattern.
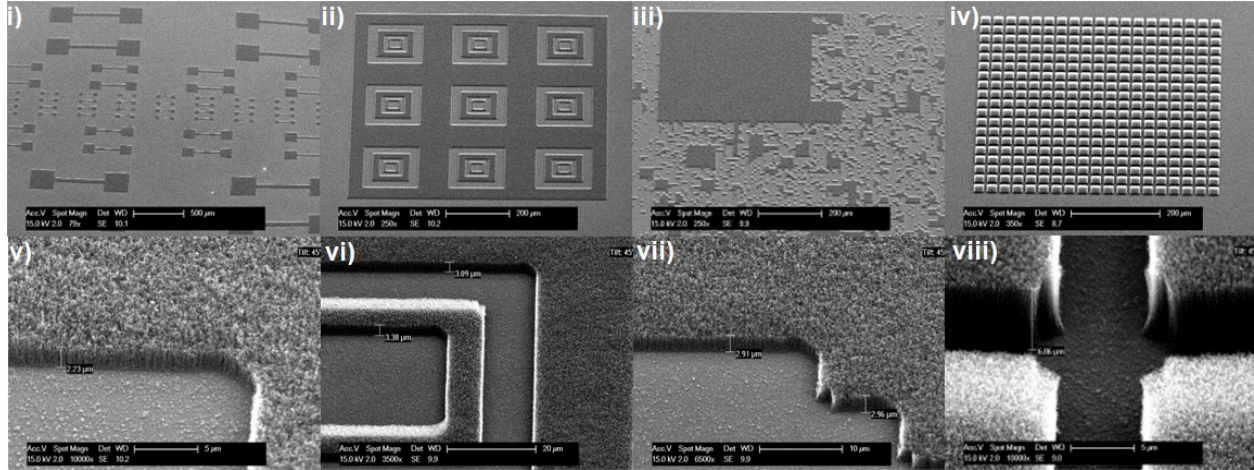
Figure 4.15: Images showing patterned CNT growth with the Nominal recipe: (i,ii,iii,iv) The different growth patterns; (v,vi,vii,viii) Their respective close-up pictures showing growth of only a few microns. Clearly, the Nominal recipe is not efficient in producing high growth on patterned regions.

The next step was to test the Taguchi recipes, and see how they would respond to patterned growth. Some results were as expected, while some had been thought provoking. Table 4.4 lists the growth results for the different recipes, and compares it with growth on unpatterned catalyst layer, as we had seen in the last chapter.

Table 4.4: CNT patterned growth result for the Taguchi recipes with P3256_V2_CATALYST mask. The results of 5 min unpatterned growth are also provided for reference.

Experiment number	Growth on patterned island	Growth on unpatterned island (μm)
Recipe 1	Random	6
,, 2	Random	150
,, 3	Random	248
,, 4	Random	267
,, 5	None	323
,, 6	Random	19
,, 7	Random	5
,, 8	Random	25
,, 9	Random	Random
,, 10	Random	Random
,, 11	None	None
,, 12	Random	Random
,, 13	Random	70
,, 14	Random	10
,, 15	High	235
,, 16	High	208
,, 17	Random	Random
,, 18	Random	7

The following points of observations can be made from these results:

Observation 1: Let us first take a look at the recipes which had produced random growth on unpatterned layer; these were recipes 9, 10, 12 and 17. As expected, this time too they produced only random growth on patterns. Similarly, recipe 11 did not produce any growth this time as well.

Observation 2: The recipes which had produced less growth (< 50 μm) last time, now produced random growth of CNT. These are recipes 1, 6, 7, 8, 14 and 18.

Observation 3: Recipes 2, 3, 4, 5, 15 and 16 had produced high growth on unpatterned layer. But now, only 15 and 16 had produced good growth. Recipes 2, 3 and 4 had surprisingly produced random growth, while recipe 5 resulted in no growth at all.

Explaining observation 1 was easy, as it was expected that these recipes would not favor CNT growth at all, in the given growth time, in either case. From observation 2, we reconfirmed that patterning the island had a detrimental effect on growth height: the recipes producing low CNT growth for the unpatterned layer now produced only random growth on the patterns. This result is consistent with the theory of loading effect discussed earlier. Observation 3 gave us some interesting results. First of all, recipes 15 and 16 had performed well this time also. Growth heights of over 200 μm were observed on almost all the patterns for both recipes, with almost no local or global loading effects. The reason why recipes 2, 3 and 4 produced random growth could not be explained; when they had produced good growth heights the last time. Finally, recipe 5 produced absolutely no growth this time; it had also been one of the better-performing recipes for

unpatterned layers. We reasoned that, because this recipe had already suffered from a reverse loading effect (resulting in frame-like growth patterns) for the unpatterned layer, the effect had got worsened during patterned growth, causing this recipe to fail ultimately.

To summarize, only two of the eighteen growth recipes were successful in supporting good CNT growth heights on the patterned catalyst layer as well. This showed us how sensitive the growth had become to the recipe conditions. Fig. 4.16 shows a collection of growth results from recipes 15 and 16, on the different patterns.
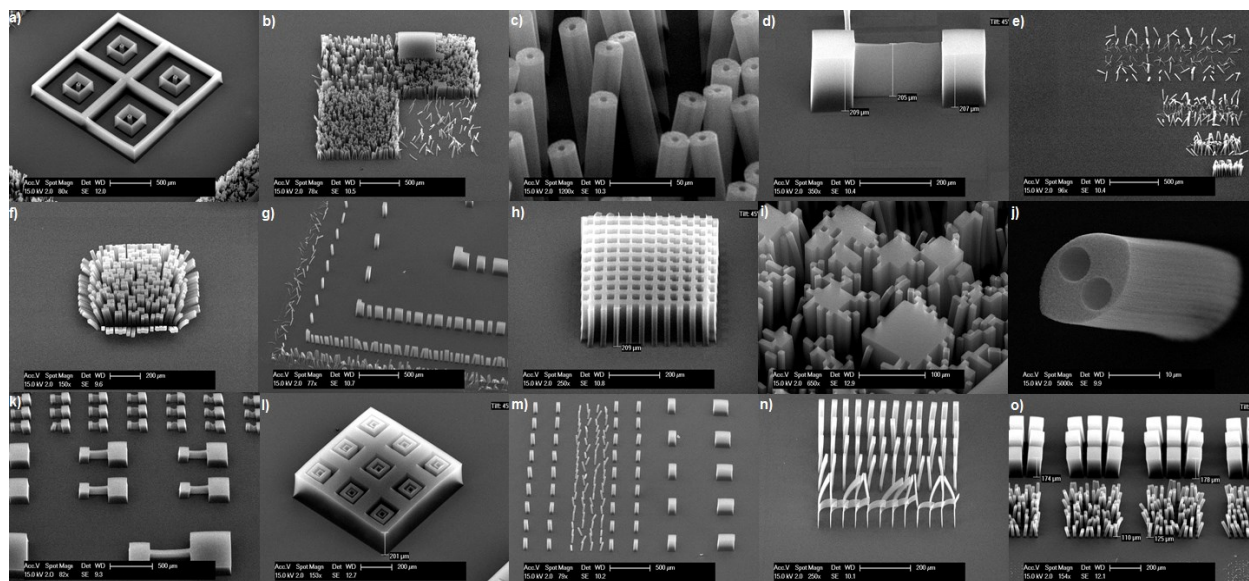
Figure 4.16: Growth results from recipes 15 and 16 showing high growth lengths of over 200 μm on every pattern, with almost no loading effect.

4.3.1 Discussion of growth results

As we have discussed, the main motivation for designing the mask was to quantitatively study the local and global loading effect phenomena. However, looking at the growth results from recipe 15 and 16, we found that the effect was very low for most of the growth patterns. Unfortunately, the other working recipes only produced random growth. This limited the scope of our analysis, and we could not study this phenomenon by observing growth height differences for different fill factor islands, as we had planned during the theoretical discussions. Even though, we could not quantify the loading effect during the scope of this thesis, we did identify these two recipes, which supported growth in excess of 200 μm on patterned catalyst islands, with a very low amount of loading effect. If we recall from the last chapter, recipes 15 and 16 were the best-case ones for growth on unpatterned layers as well. The explanations provided behind their success (lower annealing temperatures, higher annealing times, higher growth temperature, and lower levels of C_2H_2) were probably the same ones for producing excellent results this time as well.

The growth results from these two recipes also gave us an idea about buckling of CNT. Buckling is the deformation of the structure of the CNT bundle, when they cross a threshold of aspect ratio values [100, 101]. This means that the CNT grown by us are prone to this effect, as they are generally of high aspect ratios. From the growth results, we get a preliminary idea how the degree of buckling is related to the fill-factor of the growth region. Buckled CNT bundles can be seen in every image in fig. 4.16, where the fill-factor of the region is low. One of the patterns is repeated again in fig. 4.17, which shows a combination of

different fill-factor islands. The best vertical growth and the least amount of buckling had occurred in the top-right square (with the maximum fill-factor), compared to the other three squares, which have lower fill-factors. We can note that vertical alignment was achieved in the lowest fill-factor square as well (which shows that there had been no loading effect), but the CNT bundles suffer from a high degree of buckling than the other three. Similar results are shown in fig. 4.18.
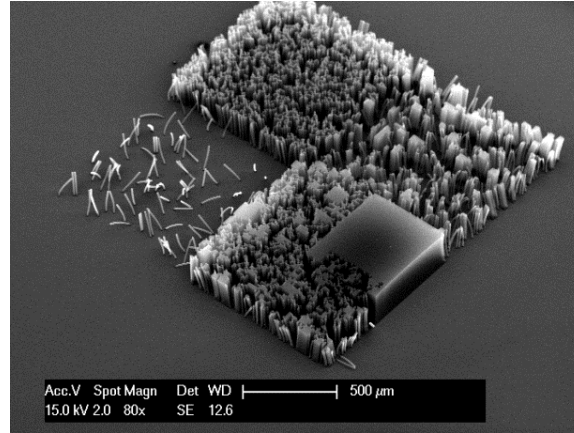
Figure 4.17: The degree of CNT buckling as related to the fill-factor. A high fill-factor region offers les buckling, and vice versa. Vertical growth alignment was achieved for all the islands, however, showing the absence of loading effects.
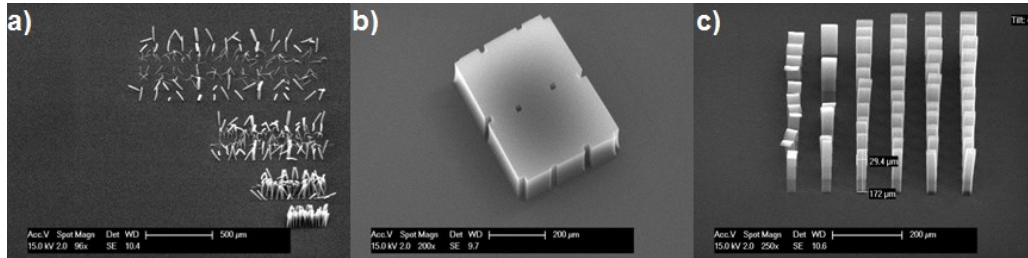
Figure 4.18: Some more pictures of growth samples showing buckling: (a) Low fill-factor regions show a high degree of CNT buckling; (b) Complete absence of buckling due to high fill-factor of the island; (c) Progressive reduction in buckling (from left to right) due to decreasing aspect ratio of CNT bundles.

As a final part to this section, it may also be said that due to the right lithography chemistry developed here, the catalyst have got patterned accurately, and the CNT forests have produced these beautiful shapes. Not only would this help in future development of TSV processes, but these results can also be used for processing MEMS structures that integrate patterned CNT growth.

As we said, this thesis has attempted to just scratch the surface of growth phenomenon of patterned CNT growth, with a carefully designed mask. The first results tell us that only some of the recipes which had been successful in producing growth in a continuous catalyst film, work for patterned CNT growth as well. Unfortunately, we were not able to quantitatively study the loading effect during the course of this thesis work; but we believe that trying a different recipe might be helpful for this purpose. Also, it will be interesting to see what happens when the optimum length recipe is used for patterned growth.

4.4 Summary

In summary, this chapter presented the first results of CNT growth on patterned catalyst islands. We started with the standardization of a cleanroom procedure to pattern the Fe catalyst layer on ZrN substrate. After performing growth with different masks, we found the presence of a strong catalyst loading effect, on the growth height, which depended on the size and distribution (or fill-factor) of the islands. It was observed that an island with a large size or a large fill-factor value, resulted in higher growth heights; and we called these phenomenon local and global loading effects respectively. We explained the origin of these effects, and then, by simulations, showed their behavior. Based on our understanding of the loading effect, we designed a mask with different shapes, sizes and fill-factors of patterns. Our growth results with this mask were promising: we found that recipes 15 and 16 supported uniform patterned growth heights over 200 μm, which proved that they were robust against the loading effect phenomena. Finally, we did a brief analysis on the dependence of CNT buckling on the island fill-factor. This concludes our research on CNT growth. In the next two chapters, we are going to study the electronic properties of the CNT and see how low resistivity vias may be fabricated.

Chapter 5

Electronic modeling of CNT resistivity

In the last two chapters, we studied the growth mechanism of CNT vias, on patterned and unpatterned catalyst layers. In this chapter, we are going to study their electrical properties. Knowledge of both the growth mechanism and the electrical properties is essential to understand how CNT would perform as interconnect materials.

As the goal of this thesis work was to design the best growth recipe to produce ultra-long CNT and with low resistivity values; therefore it was essential to know the resistivity of each of the 18 different growth samples. This, however, would have required the fabrication of test structures for each of the samples; expensive both in regards to time and resources. As we'll find in the next chapter, direct measurement of resistance also gave us extremely noisy results. So, it was decided to *calculate* the resistivity from characterizing the CNT samples. Before that, however, it was required to understand the mechanism of electron transport in a CNT, and how, equivalent circuit models can be constructed from it. In the following sections, we are going to study this topic, and look at two circuit models developed by two leading research groups. Finally, we will look at a simple model, derived during this thesis, which could calculate the resistivity of a CNT vias, from knowledge of individual tube resistances.

5.1 Origin of resistance in a CNT

It is known that the electronic properties of a *single* CNT depends on a host of factors; for instance, whether it is single-walled or multi-walled, the number of walls present if it is multiwalled, whether the wall(s) is metallic or semiconducting (i.e., the chirality), the CNT length and diameter, the quality (which can be related to the amount of defects in the tube) and the temperature. Furthermore, for a CNT *via*, we need to also consider its area, the packing density (i.e. the number of tubes present), and the proportion of MWNT to SWNT in the via. Each of these properties has an incremental or detrimental effect on the resistivity. Table 5.1 shows how the different characteristics of a CNT and a via affect the resistance. Clearly, the overall resistance is a function of all these different parameters. Hence, we would need to build an equation for resistance (and the resistivity), which can accommodate all these physical factors.

Table 5.1: The effect of different CNT and via properties on the overall via resistance.

CNT and via properties		Effect on via resistance
CNT	Diameter	↑
	Quality	↓
	Number of walls	↓
	Chirality (Proportion of metallic tubes)	↓
	Temperature	↓
Via	Height	↑
	Area	↓
	Packing density	↓

This process of deriving electrical properties from the physical properties is called physics-based compact modeling, and has been the goal of many research groups worldwide. A survey of literature from these groups showed that an abundance of techniques had been attempted at building electrical models of CNT interconnects [102-105]. For this thesis, the approaches of two prominent research groups were studied in depth, and their techniques were used to find the resistance of the as-grown CNT structures; these two groups are headed by Prof. A. Naeemi of Georgia Tech, and Prof. K. Banerjee of UCSB. Before studying these two models, and also our resistivity model, we would briefly review the mechanism of electron transport in a CNT.

5.1.1 The three resistance components

A CNT, when transporting electrons though it, poses three types of resistances to the current flow; depending on whether the electrons flow without any scattering (*ballistic transport*) or with scattering (*diffusive transport*), and finally, the resistance encountered at the interface with the external world.

 The resistances arising from these three mechanisms are:

a. The (constant) quantum resistance inherently present in all 1-D conducting channels (ballistic regime)
b. The length-dependent resistance arising from the scattering of electrons (diffusive regime)
c. The contact resistance at the two ends of the tube

Ballistic regime: Every one dimensional electronic conductor has an intrinsic resistance value that is quantized, and depends on the number of conduction channels [106]. The value of a quantum of resistance per channel (R_Q) is $h/2q$. A SWNT, which is essentially a 1-D electronic channel, is no exception. Since it consists of two subbands [107], the value of the resultant quantum resistance is $h/4q^2$. So, this resistance is the smallest resistance that can be encountered in a nanotube. For a very short tube working in the quantum regime only, i.e. whose length is shorter than the mean free path of the electrons (also called the ballistic length), this is the only form of resistance. An interesting physical implication of this may be, one can ideally send in a very high density of current, without destroying the CNT from overheating, which can otherwise happen in a macroscopic conductor.

Diffusive regime: When the tube length exceeds the electron mean free path, the electrons are subjected to a variety of scattering mechanisms during transport. They may be scattered by phonons (which manifest from structural defects in the tube), impurities in the form of ferroelectric materials (which give rise to magnetic fields), or scattering with other valence electrons [108]. All these events obstruct electron flow and cause the

tube to have a finite material resistance, just like the case of a classical current carrying wire, following the Ohm's law. This resistance is linearly dependent on the tube length, because greater the length, greater is the possibility of encountering these scattering mechanisms. In fact, it can be roughly stated that, the resistance increases by one quantum (R_q) for every ballistic-length ($l_{ballistic}$) increase of tube length (L). So, this resistance may be expressed as: $R_L = R_Q (L/l_{ballistic})$.

Contact resistance: Finally, the third component of resistance arises from the interfaces at the ends of the tube, which makes contact with them to measurement structures; which maybe, for instance, a metallic pad. This resistance, known as the contact resistance (R_C), is usually the greatest contributor towards the overall CNT resistance [109], and technologists have been researching aplenty to find ways to minimize this in CNT-based electronic devices [110-112].

5.2 CNT Equivalent circuit models

As an electrical engineer, it is highly interesting to represent the physical effects of a CNT in terms of circuit components, and thereby simulate its electrical behavior under DC or AC excitation. If accurate models can be developed for SWNT and MWNT, then a circuit simulator like Spice can do this task pretty well. Two models were studied during this work, and their results were compared. Since this thesis dealt with only the resistive component of CNT, their inductive and capacitive effects were not included.

5.2.1 Circuit model of A. Naeemi et al.

5.2.1.1 Electronic modeling of a SWNT
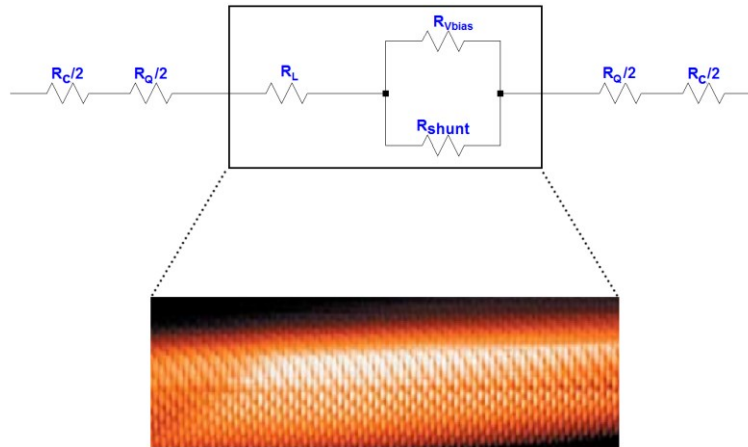
Figure 5.1: Equivalent resistive circuit of a SWNT, as developed by A. Naeemi et al [113]. A high resolution SWNT image is also shown for comparison [107].

Fig. 5.1 shows the equivalent circuit model developed by A. Naeemi et al. to calculate the resistance of one metallic SWNT [113, 114]. The total resistance is split into the three components: fundamental *quantum resistance* (R_Q), the *length dependent resistance* (R_L), the *contact resistance* (R_C); and two additional components: a *bias-voltage dependent resistance* (R_{Vbias}) and a *shunt resistance* (R_{Shunt}). The contact and the quantum resistances are shared equally by the two ends of the tube. The boxed part in the figure represents the bulk of the tube, with the length dependent, bias dependent and the shunt resistances. These last two components had not been encountered in section 5.1.1, and they arise from the dependence of the ballistic length on various types of scattering mechanisms. Their origins will be briefly discussed here.

The mean free path (or, ballistic length) of the conducting electrons is not an independent quantity, but a resultant from various types of scattering mechanisms [115]. Even if we consider only electron-phonon scattering, which is the dominating type for interconnect applications [113], we have to consider two types of phonons; acoustic phonons and optical phonons. We must then consider four types of scattering phenomenon, caused by these phonons. The net ballistic length due to all these scattering events may be expressed as:

$$\frac{1}{l_{ballistic}} = \frac{1}{l_{ac}} + \frac{1}{l_{op,abs}} + \frac{1}{l_{op,ems}^{E}} + \frac{1}{l_{op,ems}^{abs}}$$

(5.1)

where, l_{ac} — Mean free path (MFP) of an electron due to scattering by an acoustic phonon

l_{op} — „ „ „ „ „ scattering by an optical phonon

$l_{op,\,abs}$ — „ „ „ „ „ absorbing an optical phonon

$l_{op,ems}^{E}$ — „ „ „ „ „ emitting an optical phonon due to electric field from the bias voltage

$l_{op,ems}^{abs}$ — „ „ „ „ „ emitting an optical phonon due to absorbing another optical phonon

The MFP due to scattering and absorbing an optical phonon are related by the equation:

$$l_{op,abs} = l_{op}\left(1 + \frac{1}{n}\right)$$

(5.2)

Further, the MFP by emitting an optical phonon on absorbing another optical phonon is the sum of the MFP by scattering and absorbing an optical phonon. Or, $l_{op,ems}^{abs} = l_{op} + l_{op,\,abs}$. Thus, it may be expressed as:

$$l_{op,ems}^{abs} = l_{op}\left(2 + \frac{1}{n}\right)$$

(5.3)

where, n is the number of optical phonons present in the ballistic length of the tube, and which participate in electron scattering [116]. This number follows a Bose-Einstein distribution, following the expression:

$$n = \frac{1}{e^{\hbar\omega/kT} - 1}$$

(5.4)

Finally, MFP by emitting an optical phonon due to the electric field can also be related to the MFP from scattering by an optical phonon; from the relation:

$$l_{op,ems}^{E} = l_{op} + {}^{\hbar\omega}\!/_{(qV_{bias}/L)}$$

(5.5)

where, ω – Angular frequency of the optical phonon

   V_{bias} – DC bias voltage acting on the CNT

   L – Length of the CNT

It is essentially this $l_{op,ems}^{E}$ term, that introduces the bias-voltage dependency (R_{Vbias}) on the overall CNT resistance. Hence, the net ballistic length, from eqn. 5.1, can be written as:

$$\frac{1}{l_{ballistic}} = \frac{1}{l_{ac}} + \frac{1}{l_{op}\left(e^{\hbar\omega/kT}\right)} + \frac{1}{l_{op} + \dfrac{\hbar\omega}{\left(\dfrac{qV_{bias}}{L}\right)}} + \frac{1}{l_{op}\left(1 + e^{\hbar\omega/kT}\right)}$$

(5.6)

Now, optical phonons with angular frequency (ω) have energies ($\hbar\omega$) close to 0.18 eV [117]. Which means, at room temperature, $e^{\hbar\omega/kT}$ is a very large value. So, $e^{\hbar\omega/kT} \approx 1 + e^{\hbar\omega/kT}$. So, the expression for ballistic length then becomes:

$$\frac{1}{l_{ballistic}} = \left[\frac{1}{l_{ac}} + \left(\frac{2}{l_{op}}\right)e^{-\hbar\omega/kT}\right] + \left[\frac{1}{l_{op} + \dfrac{\hbar\omega L}{(qV_{bias})}}\right]$$

(5.7)

It may be observed that eqn. 5.7 has been separated into a bias-free term, and a bias-dependent term. The bias-free term represents the ballistic length of the tube, when there is no applied voltage. Hence, we may finally rewrite eqn. 5.7 as:

$$\frac{1}{l_{ballistic}} = \frac{1}{l_{ballistic|no\ bias}} + \frac{1}{l_{op} + \dfrac{\hbar\omega L}{(qV_{bias})}}$$

(5.8)

Now, as the total resistance of a SWNT can be expressed as a sum of R_C, R_Q and R_L ($= R_Q$ [$L/L_{ballistic}$]), the resistance of a SWNT can be expressed as:

$$R_{SWNT} = R_C + R_Q\left[1 + {}^L\!/_{l_{ballistic}}\right]$$

$$= R_C + R_Q\left[1 + {}^L\!/_{l_{ballistic|no\ bias}} + \frac{L}{l_{op} + \dfrac{\hbar\omega L}{(qV_{bias})}}\right]$$

$$= R_C + R_Q\left[1 + {}^L\!/_{l_{ballistic|no\ bias}}\right] + \frac{1}{\dfrac{l_{op}}{R_Q L} + \dfrac{\hbar\omega}{R_Q(qV_{bias})}}$$

$$= R_C + R_Q + R_{L|no\ bias} + \frac{1}{\dfrac{1}{R_{shunt}} + \dfrac{1}{R_{Vbias}}}$$

(5.9)

Eqn. 5.9 shows us how R_L has been separated into a bias-free part ($R_{L|no\ bias}$), and a parallel network of R_{shunt} and R_{Vbias} resistances; where $R_{shunt} = R_Q L/l_{op}$ and $R_{Vbias} = R_q(qV_{bias})/\hbar\omega$. Now, $l_{op} = kD$, where k is a proportionality constant which varies from 15 to 20 [116] and D, the tube diameter. Hence, for interconnects (where $L >> l_{op}$) R_{shunt} is a very high value; much greater than R_{Vbias}. This means that it can be safely ignored. Thus, the final SWNT resistance model is a simple series combination of four resistances: R_C, R_Q, $R_{L|no\ bias}$ and R_V (plugging in the values of the constants, $R_{Vbias} = V_{bias}/I_0$, where $I_0 = \hbar\omega/R_q q = 27.9$ μA).

Incidentally, the term l_{ac} also depends on the diameter of the nanotube just like l_{op}. Further it also depends on the temperature of the tube, according to the expression: $l_{ac} = 10^3 DT_1/T$; where $T_1 = 400$ K From [115, 116]. So, for room temperature operation, $l_{ac} = (4000D/3)$.

From these expressions, the resistance of a SWNT operating at room temperature may be finally expressed just in terms of the contact resistance, the quantum resistance, tube length, tube diameter and bias voltage, as:

$$R_{SWNT} = R_C + R_Q\left[1 + L\left(\frac{3}{4000D} + \frac{2}{15D}e^{-6.9627}\right)\right] + \frac{V_{bias}}{27.9 * 10^{-6}}$$

(5.10)

If we take a look at the above equation, we would note that the bias-free ballistic length depends only on the tube diameter. If this would have been indeed true, then for a typical tube diameter of 1 nm, the ballistic length would have been in the range of microns. However, the samples used for this thesis have ballistic lengths of just a few tens of nanometers. This huge reduction is probably caused due to various other sources of resistance towards electron flow, which had not been considered in the model; for instance, scattering by other electrons, scattering by various chemical impurities that may be present in the tubes (as they are grown in a CVD process), structural changes caused due to mechanical effects, or even more complex effects such as the heating of the optical phonons by the conducting electrons [118]. A measure of the *real* ballistic length of CNT can be determined from Raman spectroscopy of the as-grown samples. This method has been used in this thesis work, and we will be looking at it in the next chapter (section 6.1.2).

5.2.1.2 Electronic modeling of a MWNT

The resistance of a MWNT may be considered equivalent to the resistance of a SWNT shared by the total number of conduction channels present in the MWNT [113, 119]. It may therefore be expressed as:

$$R_{MWNT} = \frac{R_Q \left(1 + {}^L/_{l_{ballistic}}\right)}{N_{channels}}$$

(5.11)

where, $N_{channels}$ is the total number of channels present in the MWNT.

Since a MWNT is basically a collection of concentric shells of SWNT, the total number of channels may be written as the number of channels per shell summed over the total number of shells.

$$N_{channels} = \sum_{\substack{Number\ of \\ shells}} Number\ of\ channels\ per\ shell$$

$$= \sum_{n=1}^{p} N_{channels/shell} (d_n)$$

(5.12)

where, p is the number of shells present in the MWNT, and n is an integer which denotes the shell number; it ranges from 1 (for the outermost shell) to p (for the innermost shell). If the separation between adjacent shells is δ, the diameter of the outermost shell is d_{out}, and the diameter of the innermost shell d_{in}, then:

$$p = 1 + \frac{d_{out} - d_{in}}{2\delta}$$

(5.13)

Now, since δ is considerably smaller than d_n, the summation in eqn. 5.12 can be approximated by an integral, which gives:

$$N_{channels} = \int_{n=1}^{p} N_{channels/shell} (d_n)$$

(5.14)

It is easier to relate the number of channels per shell with the tube diameter, for the derivation of resistance. In order to accomplish that, $N_{channels/shell}$ is expressed as a function of the valence energy level (E_v) of individual subbands in a shell. It follows a Fermi distribution [120], and may be expressed as:

$$N_{channels/shell} = \sum_{Subbands\ in\ the\ shell} \frac{1}{1 + e^{E_v/K_BT}}$$

(5.15)

where, E_v is a function of the shell diameter. Using this information, a plot can be generated between $N_{channels/shell}$ and d_n, as shown in fig. 5.2 [119]. From the graph, the relation between the two quantities may be obtained.
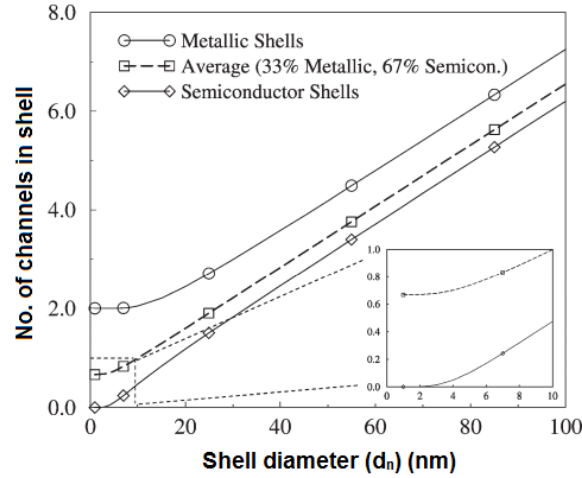
Figure 5.2: Plot showing the variation of the number of channels in a shell with its diameter [113].

Fig. 5.2 shows that, the assumption that a MWNT is composed of only metallic or only semiconducting shells result in different behaviors of the two quantities, especially for the lower diameters (< 6 nm). Consequently, assuming that the shells are only metallic (or only semiconducting) would result in a large difference in the MWNT resistance. This is of significance in this thesis, as our samples had diameters of less than 10 nm. Hence, it is safer to assume a random distribution of chirality for the shells; which would result in $1/3^{rd}$ of them to be metallic and the rest $2/3^{rd}$ semiconducting [108].

Then, $N_{channels/shell}$ can be expressed as a linear function of the diameter of that particular shell (d_n), as:

$$N_{channels/shell}(d_n) = 2/3 \qquad\qquad d_n < 6\ nm$$
$$= \alpha d_n + \beta \qquad\qquad otherwise$$

(5.16)

where, $\alpha = 0.14$ nm^{-1} and $\beta = 0.2$ [113]. The conductivity of a single MWNT can now be written by the traditional equation: $\sigma_{MWNT} = G_{MWNT}(L/A)$, where, G_{MWNT} is the overall conductance of the MWNT, and is the reciprocal of R_{MWNT}. Combining eqn. 5.11, 5.14 and 5.16, we get the expression for G_{MWNT} as:

$$G_{MWNT} = \frac{\int_{n=1}^{p} N_{channels/shell}(d_n)}{R_Q \left(1 + L/l_{ballistic}\right)}$$

(5.17)

Integrating the number of channels in a shell over the entire MWNT for G_{MWNT}, and solving eqn. 5.17, we finally get the expression for the conductivity of one MWNT. This is represented below:

$$\sigma_{MWNT} = \frac{2}{3}\left(\left(\frac{1}{d_{out}} - \frac{d_{in}}{d_{out}^2}\right) - \frac{L}{d_{out}^2 \mathcal{K}} ln\frac{d_{out} + L/\mathcal{K}}{d_{in} + L/\mathcal{K}}\right)\left(\frac{L}{4\delta R_Q}\right) \qquad d_{out} < 6\,nm$$

$$= \left[\left(1 - \frac{d_{in}^2}{d_{out}^2}\right)\frac{\alpha}{2} + \left(\beta - \frac{aL}{\mathcal{K}}\right)\left(\left(\frac{1}{d_{out}} - \frac{d_{in}}{d_{out}^2}\right) - \frac{L}{d_{out}^2 \mathcal{K}} ln\frac{d_{out} + L/\mathcal{K}}{d_{in} + L/\mathcal{K}}\right)\right]\left(\frac{L}{4\delta R_Q}\right) \quad otherwise$$

$$(5.18)$$

where, $\mathcal{K}$ is the ratio between the ballistic length and the outer diameter of the tube.

At this point, it might be useful to note the relationship between conductivity of a MWNT with its diameter, when the diameter is greater than 6 nm (which is the case for most samples used in this work).

When, $L < \mathcal{K}b/a$ -- Conductivity increases as Diameter decreases
$L = \mathcal{K}b/a$ -- Conductivity is independent of Diameter
$L > \mathcal{K}b/a$ -- Conductivity increases as Diameter increases

Thus short and narrow tubes, or long and fat tubes, offer lower values of conductivity, and are useful for the purpose of interconnects. However, when the diameter is lesser than 6 nm, conductivity increases as diameter increases, irrespective of tube length. In most of our samples, however, $\mathcal{K}$ is even less than 10. So, L will always be greater than $\mathcal{K}b/a$; which means that thicker tubes would always give a higher conductivity. This behavior is probably also reflected in eqn. 5.10.

We are, however, interested to know the *resistance* of a single MWNT. In the above model, α and β had been extracted assuming that the shells of a MWNT have random chirality. Since the semiconducting walls do not participate in conduction, so now it was a question of considering only those shells that were indeed metallic. Random assignment of metallic chirality is an easy solution to this problem. But a simple justification can be made which implies that the *peripheral* shells may be metallic. The reason is, larger the diameter, lower is the bandgap of the semiconducting shells [121], and hence closer they are in behaving like a metal. For this reason, the outer third of the shells have been considered metallic, and the rest semiconducting.
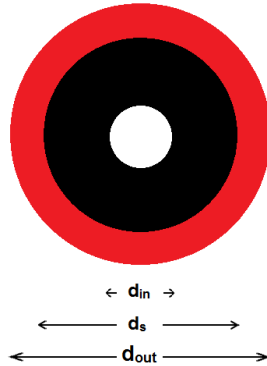
Figure 5.3: Conceptual representation of a MWNT. It has a hollow core, semiconducting shells (in black) and metallic shells (in red).

Fig. 5.3, which represents a MWNT, demonstrates this assumption. The shaded black part constitutes the semiconducting shells and the red part, the metallic shells. The MWNT has an innermost diameter d_{in}, an outermost diameter d_{out}, and a gross diameter of the semiconducting shells d_s. So, the area occupied by the metallic shells (A_M) is given by: $A_M = \frac{\pi}{4}(d_{out}^2 - d_s^2)$, where $d_s = d_{in} + 2\delta\left(\frac{2p}{3} - 1\right)$. Hence, we are basically analyzing the MWNT as a hollow conductive cylinder of metallic shells. Now, the resistance can be simply expressed as $R_{MWNT} = \left(1/\sigma_{MWNT}\right)\left(L/A_M\right)$.

This concludes our analysis on SWNT and MWNT models, developed by the group of A. Naeemi. To summarize, the resistances of both the SWNT and MWNT were derived. To convert the MWNT conductivity into resistance, it was assumed that a MWNT consisted of a random chiral distribution of shells (which would mean 1/3rd metallic tubes and 2/3rd semiconducting), and that, it was similar to a hollow conducting cylinder, with conduction taking place only in the metallic shells at the periphery.

5.2.2 Circuit model of K. Banerjee et al.

5.2.2.1 Electronic modeling of a SWNT

The equation for resistance of one SWNT as developed by K. Banerjee et al. and presented in [122] is given as:

$$R_{SWNT} = R_C + R_{low\ bias} + \frac{V_{bias}}{I_0(L)}$$

(5.19)

Eqn. 5.19 is indeed very similar to eqn. 5.9. However, here it is claimed that I_0 is not a constant, but changes with tube length[122]; however, no equation is derived to relate this. On the other hand, according to [123], I_0 becomes independent of length, when it reaches a value of around 25 μA. This value of I_0 is assumed in majority of literature on CNT modeling, and the value derived in this thesis ($I_0 = 27.9$ μA) is very close to this as well.

5.2.2.2 Electronic modeling of a MWNT

Fig. 5.4 shows the electrical equivalent of a single MWNT, as developed by K. Banerjee et al., and presented in [124, 125]. The MWNT is composed of p number of shells. R_c denotes the contact resistance at the lower and upper end of the tube; R_{qn} is the fundamental quantum resistance of the respective shells ($n = 1$ to p); and R_{Ln} is the length-dependent resistance of the shells.
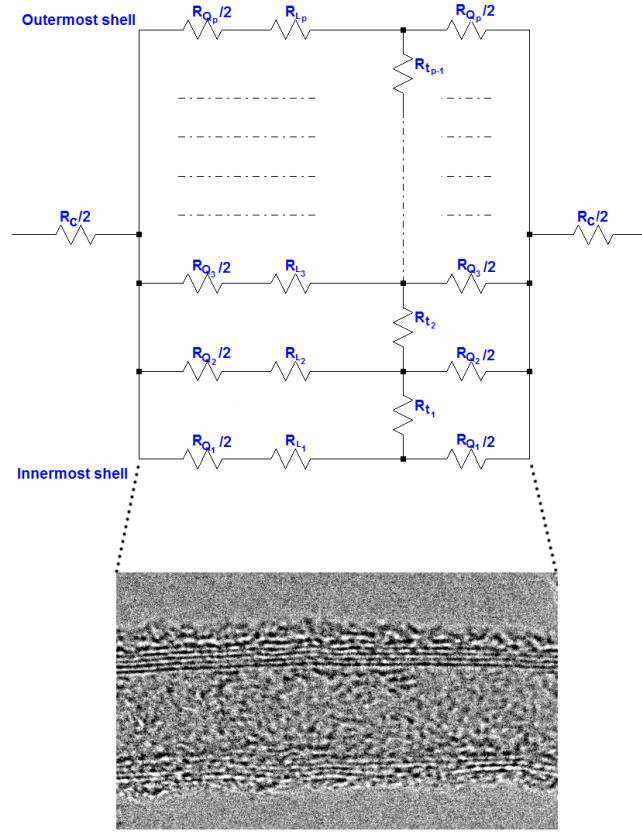
Figure 5.4: Equivalent resistive circuit of a MWNT, as developed by K. Banerjee et al., showing the resistances of different shells [124]. A high resolution MWNT image is also shown for comparison.

As discussed earlier, the quantum resistance offered by each shell is the fundamental resistance ($h/2q^2$) divided by the number of channels present in the shell (N_n). Thus:

$$R_{Q_n} = \left(h/2q^2 \right)\left(1/N_n \right)$$

$$(5.20)$$

and the length-dependent part of the resistance can be expressed as:

$$R_{L_n} = R_{Q_n} \left(L/l_{ballistic}(n) \right)$$

$$(5.21)$$

where, N_n is expressed as a linear function of the shell diameter (D_n) as before, in eqn. 5.16.

In this model though, because of their large diameters, MWNTs are assumed to be always metallic. Hence, the values of α and β are 0.0612 nm^{-1} and 0.425 respectively, which are the coefficients obtained when only metallic shells are considered from fig 5.2. Further, the ballistic length ($l_{ballistic}$) has been represented as a function of n, as if it would have depended on the shell diameter, according to eqn. 5.10. However, for this thesis, since the average $l_{ballistic}$ value was calculated from Raman spectroscopy, it was constant for a particular growth sample.

In this model, there is room to model the tunneling of electrons between adjacent tubes as well, and this effect can be represented by a tunneling resistor (R_{tn}), given by eqn. 5.22.

$$R_{t_n} = {\rho_{t_n}}/{\pi D_n L}$$

(5.22)

Here, ρ_{tn} is a constant; from experiments reported in [126], it has a value of around 5.33 $\mu\Omega$-cm^2.

Now the model of fig. 5.4 can have three levels of sophistication:

a. Every resistance value is considered (*Complete model*)
b. Tunneling effect is neglected (*Intermediate model*)
c. Tunneling is neglected and all the individual shell resistance are assumed equal (*Basic model*)

In this thesis, study of the tunneling effect has been ignored and the Intermediate model has been used. The reason is; for typical values of L, $l_{ballistic}$, and D_n, R_{tn} is quite large compared to R_{Ln} and R_{Qn}. This indicates that tunneling interaction between adjacent tubes can be neglected, which is also confirmed in [127].

So the resistance of a MWNT from fig. 5.4 may be expressed as:

$$R_{MWNT} = R_C + \left(R_{0_1} || R_{0_2} || \ldots + R_{0_n} || \ldots || R_{0_p} \right)$$

(5.23)

where,

$$R_{0_n} = R_{Q_n} + R_{L_n}$$
$$= \left({h}/{2q^2}\right)\left({1}/{N_n}\right)\left(1 + {L}/{l_{ballistic}}\right)$$

(5.24)

which finally gives us the equation for MWNT resistance:

$$R_{MWNT} = \frac{R_Q\left(1 + {L}/{l_{ballistic}}\right)}{p\left[\frac{\alpha}{2}(d_{out} + d_{in}) + \beta\right]}$$

(5.25)

To summarize this model then, the resistance of a SWNT is essentially the same as that of the earlier model. For MWNT, the resistance of each shell is assumed to be conducting and consisting of the usual components R_Q and R_L; each of which depends on the shell diameter and thus varies from the innermost shell to the outermost. And the final resistance is equivalent to the individual shell resistance divided by the number of shells. For more accurate modeling, the coupling between the MWNT shells due to tunneling can be considered.

5.3 A simple model to calculate the CNT via resistivity

This section will analyze the resistivity of a CNT via, from the values of SWNT and MWNT as we derived above. Since we intend to use *bundles* of CNT for vias, as compared to single CNT, working with resistivity is preferred. As we are going to see, a few more physical parameters determine the via resistivity. In the absence of good identification of these parameters, there can be markedly different resistivity values. For instance, an as-grown via would consist of a mixture of SWNT and MWNT. Further, only a fraction of the SWNT would be conducting, depending on the chirality. Finally, the growth density of the CNT would determine the number of CNT present in the via. All these effects would be playing an important role in determining the resistivity.

Let us consider a CNT via, cuboidal in shape, with a base area of (a x a), and a height of L. Fig. 5.5 is a representation of a face of the via, containing n number of SWNT (in green) and m number of MWNT (in red). The density of CNT in the via is D, and the number of CNT in the via-face (a) is D_a (where $D_a = m + n$). The SWNT each has an average diameter d_{sw} and the MWNT each has an average outer diameter d_{out}. The adjacent CNT are separated from each other by a tube spacing of s. For simplicity, s has been considered to be equal for both SWNT and MWNT.
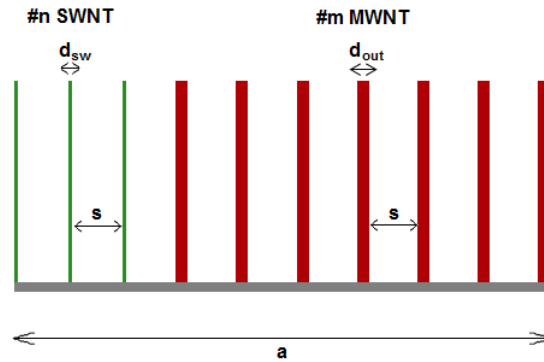
Figure 5.5: Representation of a face of a CNT via, containing a mixture of SWNT and MWNT. The SWNT (in green) has a diameter d_{sw} each, and the MWNT (in red) has an outer diameter d_{out} each. They are separated equally by a distance s. A total of n SWNT and m MWNT are present in a via c/s length a.

The proportion (P) of MWNT to SWNT in the via face needs to be found out first. By calculation, this turns out to be:

$$P = \frac{d_{out} - d_{sw}}{(d_{out} + s) - \frac{1}{\sqrt{D}}} - 1$$

$$(5.26)$$

It is interesting to note that the dimension of the face does not appear in eqn. 5.26, which indicates that P is a constant regardless of the size of the growth surface. The number of SWNT and MWNT present in the via face can then be given as:

$$n = {D_a}/{1 + P}$$
$$m = {D_a}/{1 + P^{-1}}$$

$$(5.27)$$

where, $D_a = a\sqrt{D}$. Now since a random chirality distribution makes approximately a third of the SWNT conducting, $n = D_a/3*(1+P)$. Also, as the MWNT are modeled only as hollow conductors, all of them will conduct; hence, m is the same as before. Thus we have managed to determine the number of SWNT and MWNT present in a via face. The total number of SWNT and MWNT present in the whole via (N and M respectively) can be expressed as:

$$N = n^2$$
$$M = m^2 + 2mn \qquad if\ n < m$$

$$N = 2n^2$$
$$M = 2m^2 \qquad if\ n = m$$

$$N = n^2 + 2mn$$
$$M = m^2 \qquad if\ n > m$$

$$(5.28)$$

If the resistance contribution from all the SWNT be expressed as R_N, and from all the MWNT as R_M, then they can be considered to be the equivalent resistances, contributed by parallel combinations of SWNT and SWNT respectively. Hence, they can be expressed as:

$$R_N = {R_{SWNT}}/{N}$$
$$R_M = {R_{MWNT}}/{M}$$

$$(5.29)$$

The total resistance of the via (R_{via}) is then just a parallel combination of R_N and R_M. Finally, one can find the via resistivity from the conventional equation:

$$\rho_{via} = R_{via}(L)\frac{a^2}{L}$$

$$(5.30)$$

Thus, having started from individual SWNT and MWNT resistances, we have calculated the resistivity of a complete via. As R_{via} depends almost linearly on the tube length L (fig. 5.6) (due to contribution from R_L), it is represented in the form of a function in eqn. 5.30. A linear fitting done on the simulated values of the $R_{via}(L)$ vs. L plot, gives us the slope (κ). Then the via resistivity is simply given as:

$$\rho_{via} = \kappa a^2$$

$$(5.31)$$

This sums up the procedure for finding out the resistivity of a complete CNT via. The resistivity is finally expressed as a function of the individual CNT parameters, in eqn. 5.32.

$$\rho_{via} = f(R_C, T, l_{ballistic}, d_{sw}, d_{in}, d_{out}, D, s, V_{bias})$$

$$(5.32)$$
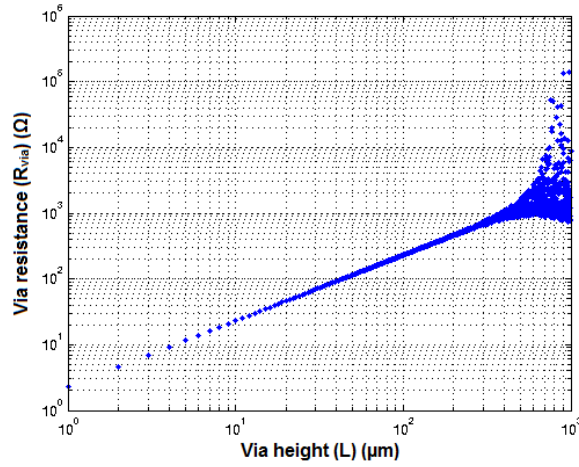
Figure 5.6: The variation of via resistance with height, as simulated by eqn. 5.9 and 5.18 (A. Naeemi et al.), for typical values of CNT parameters. The model breaks down for heights above ~ 300 μm, in most cases. Hence only the linear part should be considered to calculate κ and ρ.

5.4 Summary

In this chapter, we discussed about the three resistance components of a CNT, and how the resistance depends on a number of physical factors. To understand the effect of these factors, we went through compact models developed by two leading research groups, and derived the equations for resistances for single SWNT and MWNT. We then proceeded on to calculate the resistivity of a complete CNT via. We observed how the resistivity depended on a large number of CNT parameters. The next step would be to characterize the CNT samples to obtain these parameters. The next chapter reports the characterization results and the calculated resistivity values.

Chapter 6

Measurement and optimization of CNT resistivity

In chapters 3 and 4, we had been successful in finding the right growth recipe for ultra-long CNT bundles. In the last chapter, we did a complete analysis on the electronic modeling of the CNT, and found an expression for the via resistivity. In this chapter, we will be using this knowledge to calculate the resistivity of our as-grown CNT vias. The target will be to minimize their resistivity. If both high length and low resistivity CNT can be grown, the samples will be ideal for TSV use.

To make TSV with low-resistivity remains a challenge, as the CNT growth density and quality would have to be extremely high. A few research groups have been working to increase these two factors. Robertson et al. have experimented with different catalyst/support layer combinations for high density CNT growth [54] [128] [129], and high quality CNT are being routinely used for experiments in physics [120, 130]. However, incorporating these two properties for TSV applications have not been achieved yet. Another way in which resistivity can be reduced, is to obtain a high degree of chirality control to produce only metallic CNT. This method is still under research phase and the technology for mass producing single-chirality tubes is hitherto unknown. During this thesis, we have approached this problem in an altogether different way. We have tried to minimize the resistivity using the Taguchi DOE method, and aimed at identifying the set of CVD parameters which would help us grow CNT with the lowest ρ value.

To implement this idea, one is required to know the ρ of each of the growth samples. This can be done by measuring the resistance of the CNT, and then calculating ρ from it. This approach was tried in the beginning; but soon proved improbable. Performing accurate measurements directly on the CNT forest by contact probes was not a viable solution, because it was extremely prone to error. Even a slight deformation of the CNT by the probe tip was enough to cause a large variation in resistance values. Shown in fig. 6.1, are two measurements which were done consecutively on the same sample, and we got resistances of 6 Ω and 30 kΩ respectively! Seeing the occurrence of results of these kinds, this method was soon given up.
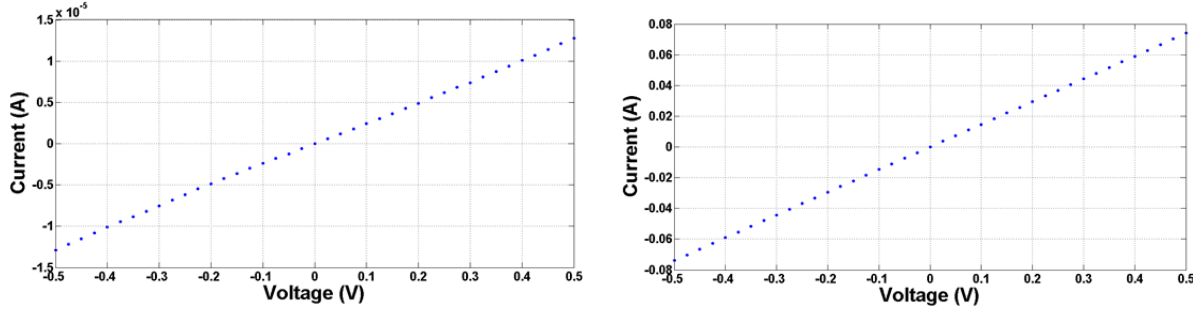
Figure 6.1: Two measurements of resistance done consecutively on a growth sample. The results show variation from 6 Ω to 30 kΩ.

It was here that we came across the idea of *calculating* the resistivity of the CNT samples, from measuring a few of their physical parameters. In the last chapter, we studied two equivalent circuits, and then developed a simple model for the via-resistivity. If this model had been accurate enough, then we would get a fairly right estimate of the resistivity value for the samples, thus eliminating the cumbersome measurement process. The following section will discuss how this approach was undertaken.

6.1 CNT characterization experiments

Electrical modeling studies showed us that the resistivity of a CNT depends on its physical parameters. These various parameters are again presented in eqn. 6.1.

$$\rho_{via} = f(R_C, T, l_{ballistic}, d_{sw}, d_{in}, d_{out}, D, P, V_{bias})$$

$$(6.1)$$

Among all these parameters, the effects of contact resistance (R_c) and temperature (T) had not been studied during this thesis. The reason for omitting R_c was that it could always be added as an offset in the resistance expression; the effect of temperature could not be studied during the course of the thesis. Further, V_{bias} is a constant, determined by technology. As a result, eqn. 6.1 drops out these three parameters, and finally we worked with six parameters as shown below.

$$\rho_{via} = f(l_{ballistic}, d_{sw}, d_{in}, d_{out}, D, P)$$

$$(6.2)$$

Knowing the values of these, the resistivity could be easily calculated by using one of the two circuit models we had studied, coupled with the model we had developed. Fortunately, we had the equipment in our laboratories to perform the measurement of these parameters. Table 6.1 shows the different measurement techniques that were used. For all the measurements, the samples from the 5 min growth run were characterized.

Table 6.1: List of CNT parameters that are required to calculate the via resistivity, along with their measurement techniques.

CNT Parameter	Measurement technique
MWNT inner diameter (d_{in})	TEM[9]
MWNT outer diameter (d_{out})	TEM
Ballistic length ($l_{ballistic}$)	Raman spectroscopy[10]
SWNT diameter (d_{sw})	Raman spectroscopy
Density (D)	SEM[11]
Proportion (MWNT / SWNT) (P)	Simulation

6.1.1 Measurement of MWNT inner and outer diameters --- by TEM

The diameter of nanotubes could be best measured by a transmission electron microscope (TEM). But due to the high cost involved in the process, only 9 samples were sent for TEM measurements. This meant that we finally could get only nine resistivity values in the **L**$_{18}$ table. The samples were selected according to their growth heights; so the samples from recipes 2, 3, 4, 5, 6, 8, 13, 15 and 16 were analyzed. From the TEM images, the inner and outer diameters of the CNT could be measured easily. Fig. 6.2a shows a collage of the TEM results from different samples (in order from recipes 2 to 16), while fig. 6.2b shows a typical image which had been used for measurement.

Due to the lack of experience of characterizing CNT in the past, it was decided to take a good number of observations of d_{in} and d_{out}. Accordingly, 20 measurements were performed on each sample. This decision was, however, justified when we found the variation of the diameters over different observations. This meant that each growth sample had a distribution of different diameters. Fig. 6.2c shows such a distribution for CNT grown using recipe 16. Fig. 6.2d shows the average diameter values for the different recipes.

---

[9] TEM analysis was performed using EI Monochromated Tecnai 200STEM-FEG.

[10] Raman spectroscopy was performed using Renishaw inVia Raman microscope with a 514 nm Ar laser.

[11] Density measurements were performed by Philips XL50 SEM.
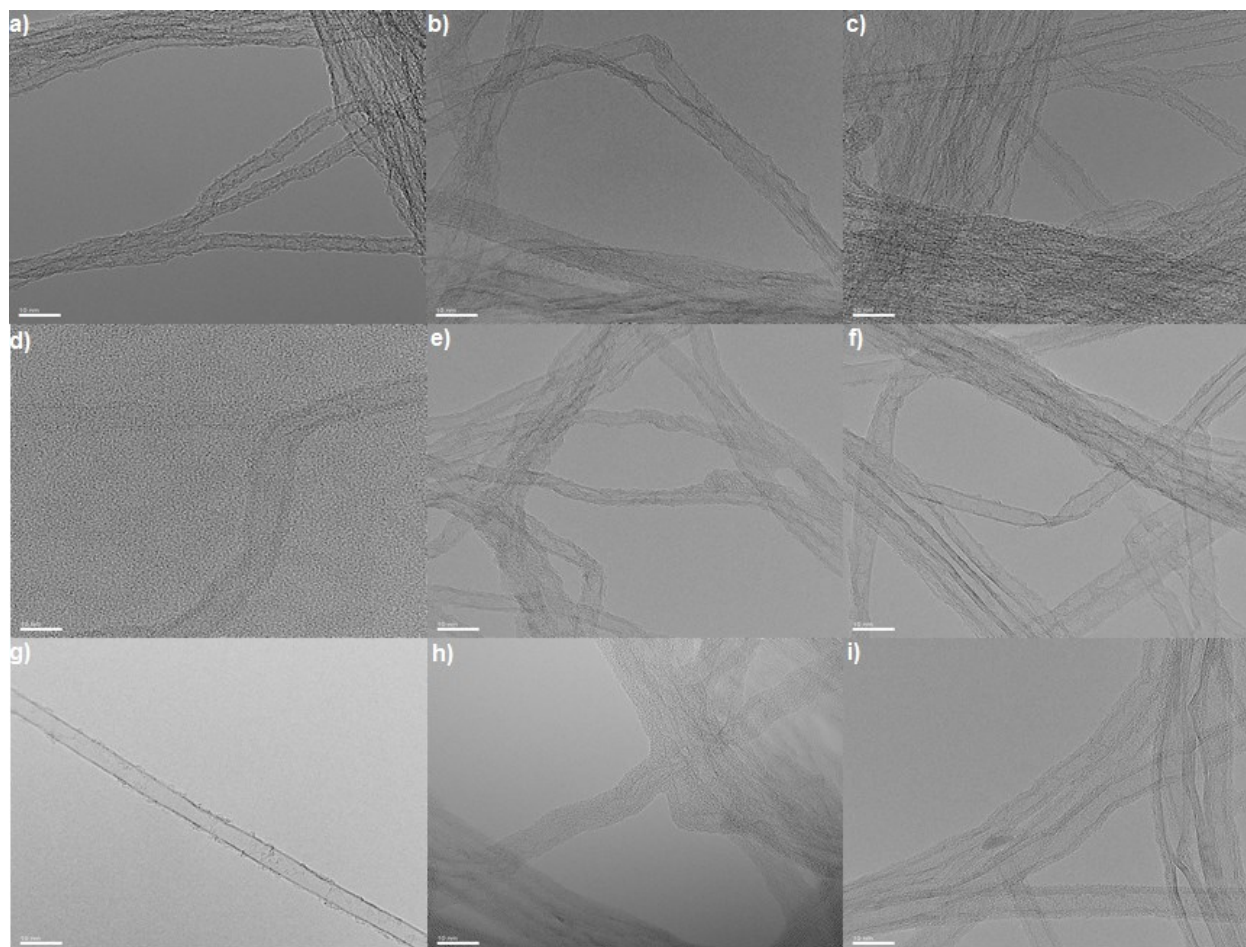
Figure 6.2a: A collection of TEM images, showing individual nanotube (mostly MWNT). The variation of the diameter and the number of walls can be seen on closer inspection. Tubes as narrow as 2 nm and wide as 11 nm were found to be present in the samples.

10 nm
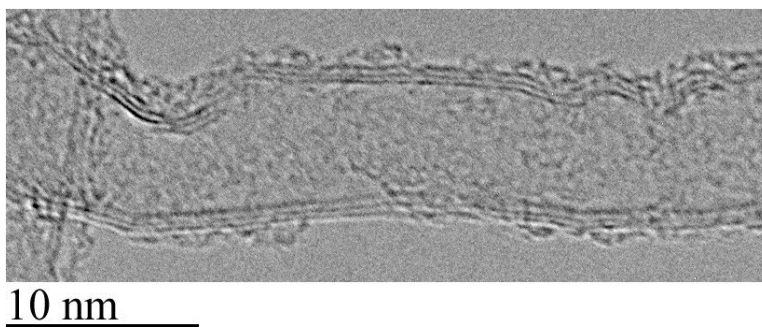
Figure 6.2b: A typical TEM image of a MWNT fiber, used for measurement purposes. The different shells are clearly visible.
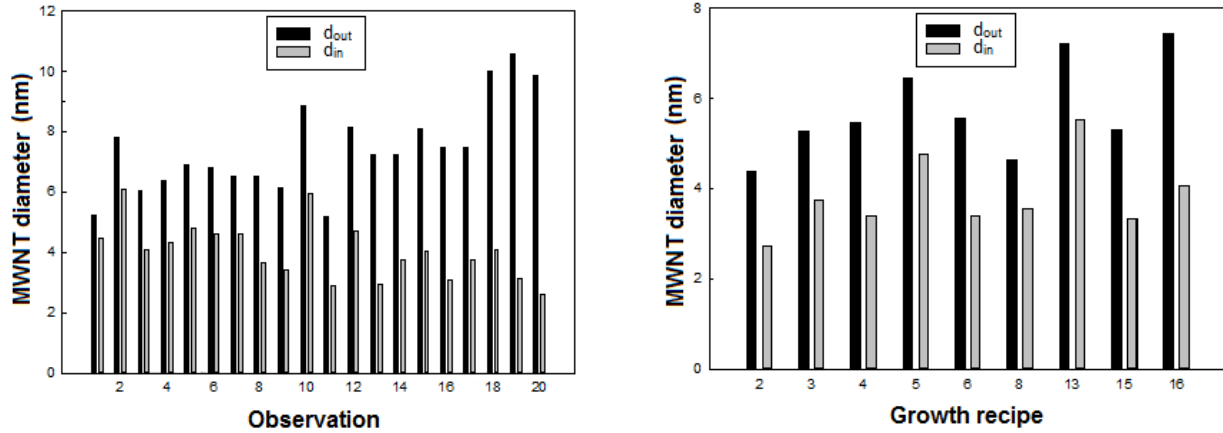
Figure 6.2c: Variation of MWNT inner and outer diameters for 20 observations taken on a growth sample (recipe 16). Other samples also showed similar variation.

Figure 6.2d: Average MWNT inner and outer diameters of the different growth samples.

6.1.2 Measurement of CNT ballistic length --- by Raman spectroscopy

Before we started with the measurement of ballistic length, we speculated how much of an effect should it have in determining the total resistance of a CNT. Especially, since this length generally ranged from a few nanometers to a few microns at the most, neglecting this factor should not have caused too much of an inaccuracy for our CNT samples, which were hundreds of microns long. To answer our question, we simulated the variation of the resistance of a via with the ballistic length. The result is shown in fig. 6.3a. We can see that it had an exponential dependence with the resistance. So, neglecting this factor would have caused an overestimation in the calculated resistivity values.
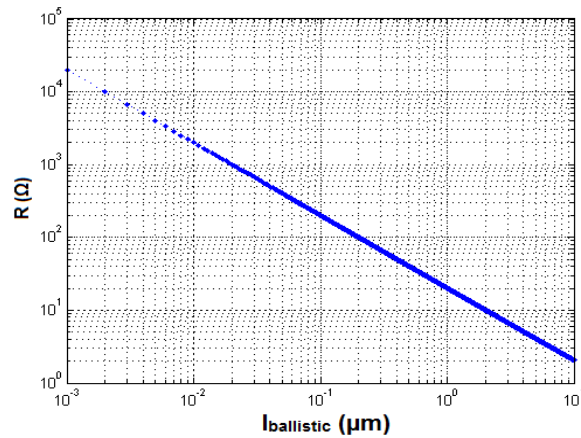
Figure 6.3a: Plot showing the effect of the CNT ballistic length on the via resistance. The variation is logarithmic, which highlights the importance of including the ballistic length term in the modeling equations. The graph is plotted using eqn. 5.9 and 5.11, for a 300 μm via.

A simple and common way to determine the average ballistic length in a mixture of CNT, is from Raman spectroscopy[12]. The quality of the tubes (i.e. ratio of the intensities between G-peak and the D-peak) can be related to its ballistic length [131] . Accordingly, eqn. 6.3 was used to calculate the ballistic length for our CNT samples.

---

[12] The raw data from the Raman spectrum had to be fitted by some standard models. The Matlab codes for the same may be found in appendix E.3.

$$l_{ballistic} = 4.4 * \left(\frac{I_G}{I_D}\right) \, nm$$

<div align="right">(6.3)</div>

Six observations were recorded per sample, and the average value was used for calculation. This time, however, the measurements did not have much variation, indicating that the CNT quality was sufficiently uniform. Fig. 6.3b shows the Raman spectrum of a growth sample (recipe 13), which had a high quality. Fig. 6.3c shows the quality values for the different growth samples.
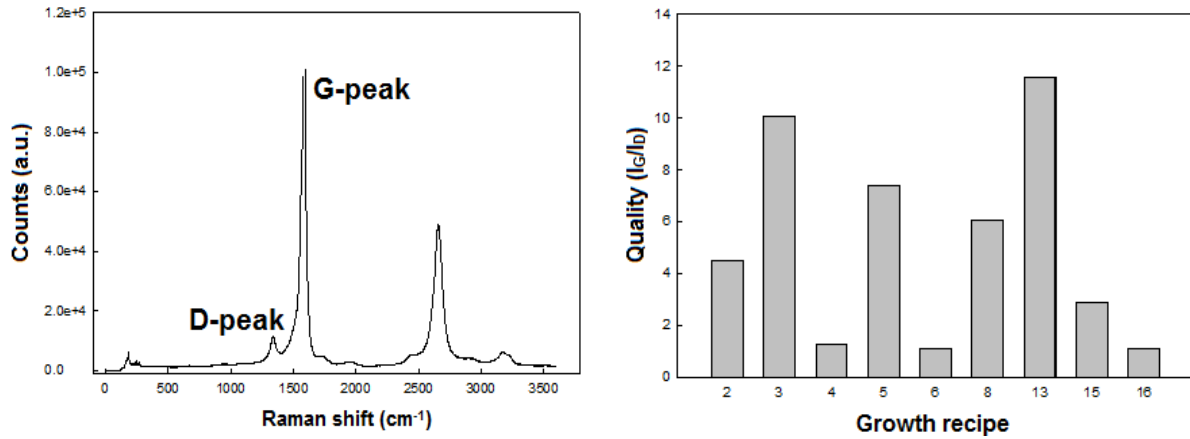
Figure 6.3b: Raman spectrum of a high quality growth sample. The ballistic length is around 50 nm.
Figure 6.3c: Average quality of the different growth samples.

From fig. 6.3c, we may see that the quality varies from less than 2 to nearly 12. Although this itself would mean a small change in the ballistic length, but since the dependence with resistance is logarithmic, we may realize that this small change would also cause a significant difference in the CNT resistance. This is the reason, why high quality CNT vias is so important for interconnect purposes.

6.1.3 Measurement of SWNT diameter --- by Raman spectroscopy

Direct measurement of the SWNT diameter using TEM was difficult, as mostly the presence of MWNT could be seen. An indirect measurement was thus required for our work. Raman spectroscopy was again a possible option. A complete Raman spectrum of CNT reveals some peaks at the lower wave numbers, which are called the radial breathing modes (RBM). The RBM is a signature of the presence of SWNT in the sample [132]; and a pure sample of only MWNT would have no RBM peaks[13]. Further, the locations of the peaks (ω_{RBM}) give information about the diameters of SNWT present (d_{sw}), as expressed in eqn. 6.4 [133].

$$d_{sw} = {248}/{\omega_{RBM}}$$

<div align="right">(6.4)</div>

At first, the 514 nm Ar laser was used to perform the Raman spectroscopy. However, for a few samples, there was absence of these peaks in the spectra. There might have been two possibilities for this; either there had been no SWNT at all in those samples, or the peaks were so weak that were drowned in the noise floor.

---

[13] As a matter of fact, small diameter (d_{out} < 3 nm), double-walled MWNT (DWNT) also generate RBM peaks. In our samples, such small diameter tubes were not observed.

To cross-check this assumption, the samples were now probed by a 633 nm He-Ne laser. This time, there was a clear presence of RBM peaks. Fig. 6.4a shows the Raman spectra of a growth sample (recipe 4) measured by the two lasers. The plots correspond to the color of the light. Clearly, the red laser 'finds' the RBM peaks. For this reason, it was used for every sample.
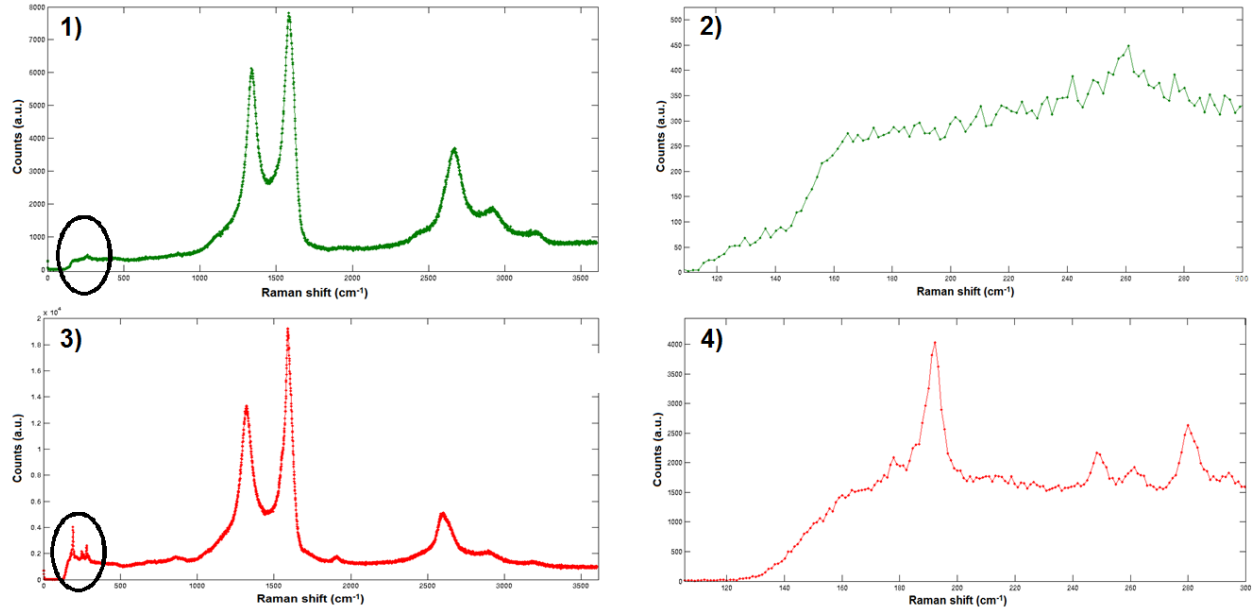
Figure 6.4a: Raman spectra by two lasers; green and red: (1,2) Complete spectra taken by the green laser, and a zoomed version at the low wave numbers, showing that RBM peaks are undetectable; (3,4) Complete spectra taken by the red laser confirming the presence of RBM peaks; and a zoomed version of the RBM region.

For each sample, Raman spectroscopy was carried out three times, and the locations of the RBM peaks were noted, and then d_{sw} calculated. As may be seen from fig. 6.4a.4, there are many peaks spread over different ω values, which tells that the SWNT had a range of diameters. So the average of the d_{sw} value was calculated for our analysis. Fig. 6.4b shows the average d_{sw} values for the different growth samples; the diameter varies between 1 nm and 1.3 nm.
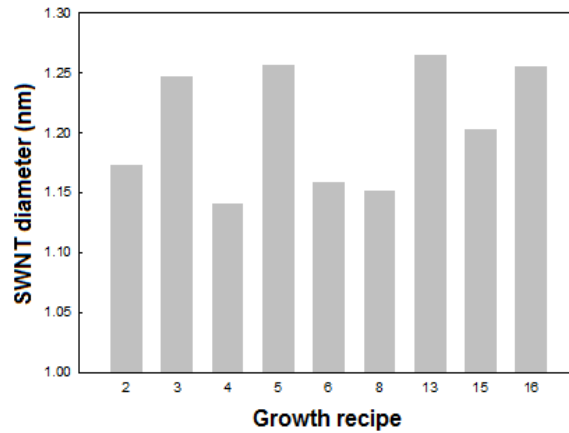
Figure 6.4b: Average SWNT diameter of the different growth samples.

6.1.4: Measurement of growth density --- by SEM

The next parameter to measure was density, and it was done using the SEM. The most common way of measurement is by individually counting the tubes, from high resolution SEM images. This technique may appear quite crude, but it is important to realize that we were only interested to know the *order* of the magnitude, and not the exact value; and this method was fairly accurate for measuring the order. Even so, in order to reduce the margin of error, six observations were taken per sample, and the average was used. Fig. 6.5a shows one of the typical high resolution SEM images from which density had been measured, while fig. 6.5b shows the variation of the measured density values for a recipe. We see that the variation is well within an order of magnitude. Finally fig. 6.5c shows the distribution of the average density for all the nine samples.
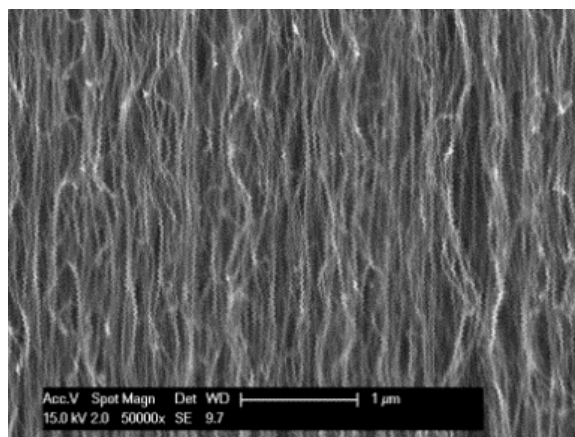
Figure 6.5a: A high resolution SEM image of CNT growth. Images like these can be used to count individual CNT, for estimating the growth density.
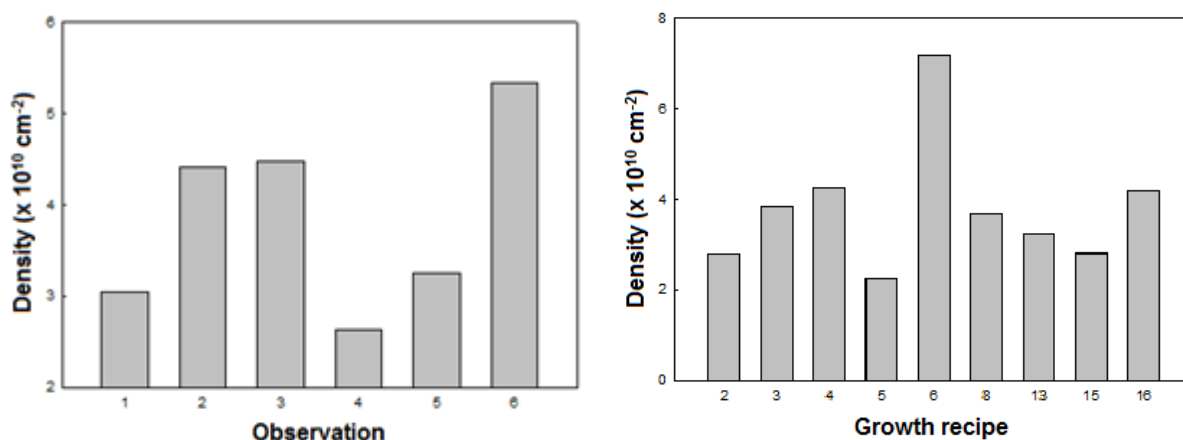
Figure 6.5b: Variation of growth density for 6 observations taken on a sample. Even a crude method like hand-counting results in values within half an order of magnitude.
Figure 6.5c: Average density of the different growth samples.

6.1.5 Measurement of the proportion of MWNT to SWNT --- by Simulation

The amount of MWNT and SWNT in a given sample plays a role in determine its resistivity, because the resistances for the two are different. However, it was tricky to determine this value. Looking back at eqn. 5.26 (given here again as eqn. 6.5) we found that the proportion between the two (P) depended on d_{out}, d_{sw}, D and s. Among these, s (which is the tube spacing) was the unknown parameter. Measuring s from SEM images was not a viable idea as the resolution was limited. Initially, AFM was considered to be used on the CNT bed, in a similar manner reported in [134]. However, this idea could not be tried here due to lack of experience with this method. Hence, an indirect technique had to be developed to have a rough idea for the value of s, and then estimate P.

$$P = \frac{d_{out} - d_{sw}}{(d_{out} + s) - \dfrac{1}{\sqrt{D}}} - 1$$

$$(6.5)$$

The route taken here was to simulate eqn. 6.5. Knowing the values of the other variables, the variation of P with s was observed, when s was varied from 0 to 200 nm. Fig. 6.6a shows such a variation, for one of the growth samples (recipe 16). For every recipe, the curve peaked at a certain s, and from this we obtained P, which was then used for calculation of ρ. The promising thing about this technique was, we got the values of s in some tens of nanometers, which was a quite likely estimate. Fig. 6.6b,c shows the P and s values for the different samples.
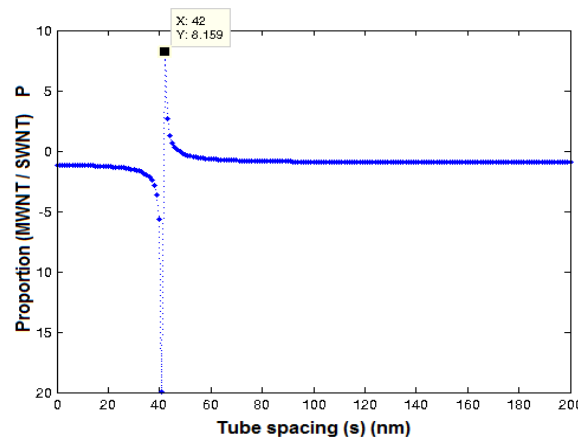
Figure 6.6a: Plot showing the variation of the MWNT proportion (P) with tube spacing (s). The maximum P occurs for a specific s value; such values are used for calculations here. A simulation for growth sample 16 gives P and s as 8.16 and 42 nm respectively.
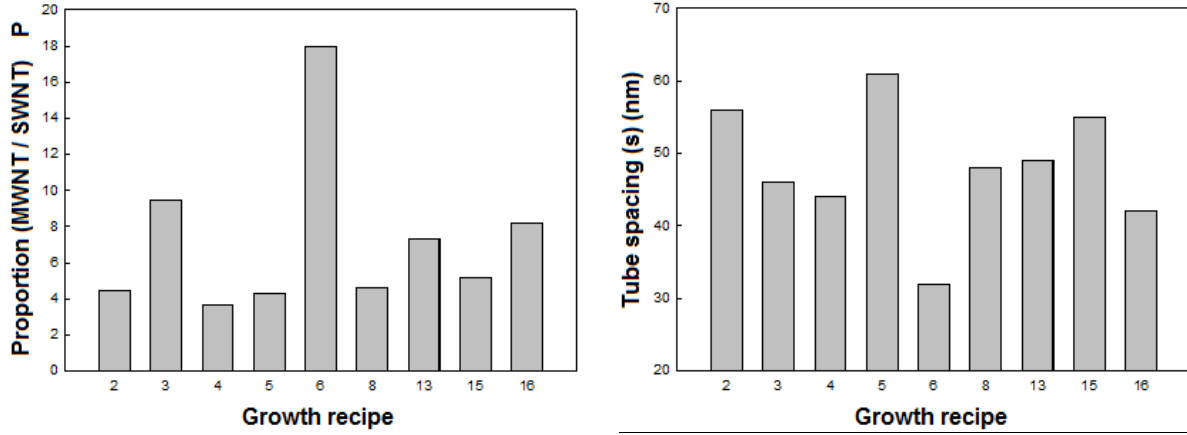
Figure 6.6b: Values of *P* for different growth samples.
Figure 6.6c: Values of *s* for different growth samples.

Thus, having known all the required parameters, the resistivity of the as-grown CNT samples could now be found out. In the following section, we will look at the results obtained from the calculations, and then use the Taguchi method to find a recipe which would result in CNT growth with the minimum resistivity.

6.2 Calculation of resistivity of the as-grown CNT samples

6.2.1 Equivalence of the circuit models of A. Naeemi et al. and K. Banerjee et al.

Before presenting the calculated values for CNT resistivity, we would first comment on the equivalence of the two circuit models (A. Naeemi and K. Banerjee) which we studied in the last chapter. It was realized during this work that both models diverge from the same basic equation.

To briefly recall the material of chapter 5, we first observed that the equation for resistance of a SWNT was the same for both cases. Then while studying the resistance of a MWNT, we saw that the approaches of the two groups were different. Naeemi calculated the *conductivity* of single MWNT directly, instead of the resistance. To convert it to resistance, we assumed that the outer 1/3rd shells of a MWNT would conduct. Next, we focused on the MWNT model of K. Banerjee, and saw that it had three levels of hierarchy. We then studied the intermediate level.

A closer look at the MWNT models of the two groups revealed that, if a few assumptions were made for each model, they reduced to the same equation, which is given below. Simply put, the resistance of a MWNT is equivalent to the resistance of a SWNT divided by the number of conducting channels in the MWNT.

$$R_{MWNT} = {R_{SWNT}}/{No. of\ channels\ in\ MWNT}$$

$$(6.6)$$

From here on, the models diverge. Naeemi takes the integral of the number of conducting channels in each shell ($N_{channels/shell}$) over all the individual shells, and arrives directly at the formula for MWNT conductivity (eqn. 5.18). Banerjee, on the other hand, calculates the number of channels from the product of $N_{channels/shell}$ and the number of shells in his equations. However, he only takes the case of $d_n > 6$ nm (in eqn. 5.16) (d_n

being the average of the outer and inner and inner diameters), and arrives at the MWNT resistance (eqn. 5.25).

This assumption of having the average diameter greater than 6 nm may not be true for certain growth cases. Indeed, in almost all of our samples, d_n < 6 nm. So using the model of Banerjee was not the best idea. In this thesis, we have used a middle-ground between the two models; and assumed that $d_n = (d_{in} + d_{out})/2$ and then calculated the MWNT resistance simply from eqn. 6.6 and 5.16. It is when we were trying to understand the origin of the eqn. 5.18, that we realized the similarity of the two models. Unfortunately, this occurred at a late stage in the thesis, which did not allow the time to study other modelling approaches. As a concluding remark, it may be said that the only point of difference in the two models is the inclusion of tunnel resistance between adjacent CNT in a MWNT, which Banerjee does in the complete model.

6.2.2 Measurement and calculation values

Given below is a list of steps which we used to arrive at the via resistivity. All these steps were discussed in the last chapter, and are listed here for reference. With these steps, not only the resistivity, but resistances of vias of any given length and area can also be easily found out.

1. Calculating the resistance of a single SWNT and a single MWNT
2. Finding out the number of SWNT and MWNT in a given cross-sectional area
3. Estimating total resistance contribution from all SWNT and MWNT in the area
4. Calculating the length coefficient of resistance of the mixed sample
5. Determining the resistivity of the via

We would now look at the table 6.2, which summarizes all the six different measurement values for the nine growth samples, along with resistances of a single SWNT and MWNT, and finally the resistivity of the samples[14]. For all calculations, a via of 1 µm height and 1 µm x 1µm area were assumed.

Table 6.2: List of all the measured, simulated and calculated CNT parameters used for the calculation of via resistivity. For reference: $l_{ballistic}$ – CNT ballistic length; d_{sw} – SWNT diameter; d_{in}, d_{out} – MWNT inner and outer diameters; D – CNT growth density; s – Tube spacing; P – Proportion of MWNT to SWNT in the via; R_{SWNT} – Resistance of a single SWNT; R_{MWNT} – Resistance of a single MWNT; R_{via} – Resistance of the via; ρ – Resistivity of the via

Recipe	Measured parameters					Simulated parameters		Calculated values			
	$l_{ballistic}$ (nm)	d_{sw} (nm)	d_{in} (nm)	d_{out} (nm)	D (x 10^{10} cm^{-2})	s (nm)	P	R_{SWNT} (kΩ)	R_{MWNT} (kΩ)	R_{via} (kΩ)	ρ (x 10^4 µΩ-cm)
2	19.75	1.17	2.73	4.39	2.80	56	4.45	433.0	118.1	0.55	5.39
3	44.23	1.24	3.75	5.28	3.86	46	9.42	252.3	46.8	0.14	1.32
4	5.74	1.14	3.40	5.46	4.25	44	3.68	1231.1	338.3	1.09	10.8
5	32.46	1.25	4.77	6.45	2.26	61	4.32	305.2	40.8	0.24	2.29
6	4.86	1.15	3.41	5.56	7.18	32	17.94	1433.5	393.4	0.59	5.86
8	26.59	1.15	3.56	4.65	3.69	48	4.59	349.0	84.5	0.30	2.89
13	50.99	1.26	5.54	7.22	3.25	49	7.30	232.9	22.0	0.08	0.76
15	12.70	1.20	3.34	5.29	2.81	55	5.15	614.2	157.7	0.71	6.98
16	4.98	1.25	4.06	7.43	4.21	42	8.16	1402.9	205.6	0.57	5.67

---

[14] The Matlab code used for the calculation of these values may be found in appendix E.4.

6.2.3 Discussion on the validity of the resistivity model

It is absolutely important to check the accuracy of any model, by verification experiments. If the opportunity of verification does not exist (like, during this work), then the simulated values must be checked with experimental values reported by other groups. This was done, and the measured values of CNT via-resistivity reported by a few groups, are listed in table 6.3. We may note that majority of the works report values in the order of 10^3 $\mu\Omega$-cm, and in the lower levels of 10^4 $\mu\Omega$-cm, which are slightly lesser than what we have obtained here. It was not, however studied at what temperatures these groups had manufactured the CNT. Higher fabrication temperature leads to better crystallinity of the tubes, leading to lower resistivity. Considering this, and the fact that they had probably only reported the best-case values, we can say that our model was reasonably accurate. Furthermore, the prediction that this model gives, for the growth density of CNT needed to overcome Cu in terms of resistivity (as we'll shortly see in fig. 6.7), matches surprisingly well with the predictions in ITRS 2007 [19]; which states that for a via made up of metallic SWNT, an integration density of 1.38×10^{13} cm^{-2} is required to outperform Cu.

Table 6.3: Experimental values of CNT via-resistivity as reported by different research groups.

Research group	ρ (μm-cm)
Chiodarelli et al. [135]	3.7×10^3
Wu et al. [136]	0.7×10^3
Zhu et al. [137]	1×10^4
Xu et al. [21]	9.7×10^3
Ngo et al. [138]	0.8×10^4
Nihei et al. [31]	0.4×10^3
Marleen et al. [139]	1.3×10^3

6.2.4: Where we stand now: A reality check with Cu

From the table, we see that the resistivity of CNT grown from recipe 13 is the lowest, at 7600 $\mu\Omega$-cm. This value is, however, still orders of magnitude higher than Cu. At the present technology node, Cu has a resistivity of only 5 $\mu\Omega$-cm [9]. Hence, for CNT to beat Cu, its resistivity needs to be reduced by a large margin. Thinking intuitively, this seems to be possible if we can pack more number of tubes in the via. Also greater the quality of the CNT, higher will be the ballistic length, which would reduce the resistance.

Simulations were done to see how the via-resistivity changes with density and quality of the CNT, and the result is presented in fig. 6.7. As we know, the resistivity depends not only on the density and quality, but also on four other parameters. Hence, to plot this graph, the values of the rest were maintained at medium levels (they are: d_{sw} = 1.2 nm, d_{in} = 2.5 nm, d_{out} = 5nm, P = 5). Fig. 6.7 also shows the resistivity of Cu for reference. We may see the two limits of quality and density, which are aimed at. We can also see where we stand now; the position of recipe 13, which is predicted to produce the lowest resistivity CNT. Clearly, qualities in excess of 1000 (i.e. ballistic length of a few microns) or densities exceeding 10^{14} tubes /cm^2 is necessary for CNT vias to have a resistivity lower than Cu.
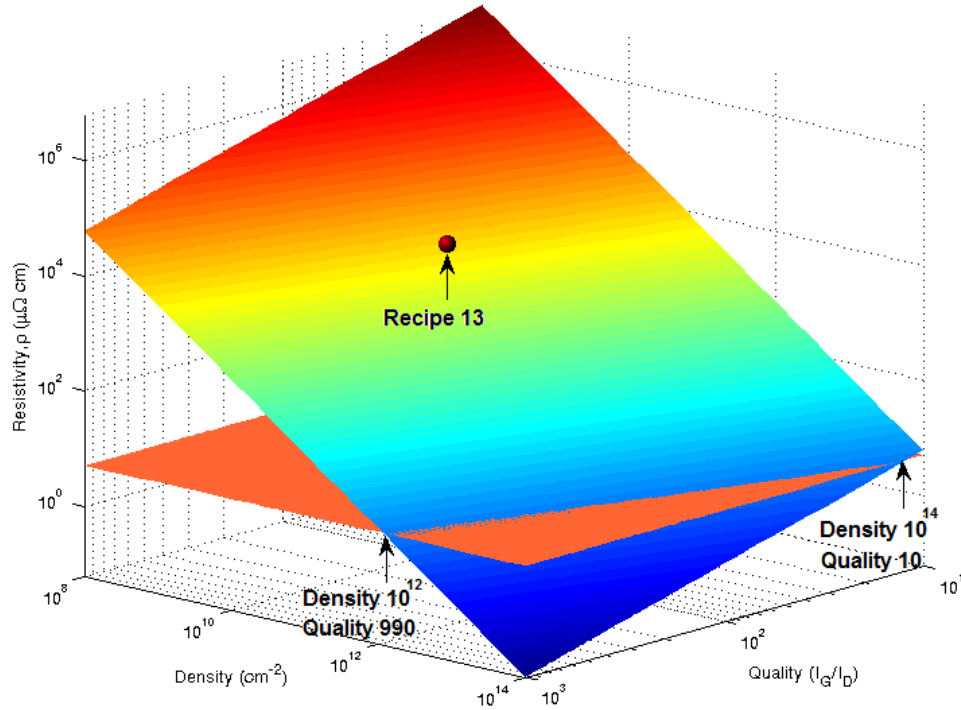
Figure 6.7: Result of simulation showing the variation of Resistivity of a CNT via with its Density and Quality. For comparison, the resistivity of a Cu via is shown. Also marked is the lowest calculated value of resistivity for one of the growth samples (recipe 13). It is clear that a very high density and quality are required for CNT via to overcome Cu in terms of resistivity.

6.3 Using the Taguchi method to minimize CNT resistivity

Having calculated the values of resistivity of the nine growth samples, Taguchi analysis was done keeping the resistivity of the other nine to an arbitrarily high value, this way ignoring them. The main effects plot for resistivity, as shown in fig. 6.8, predict the recipe (ρ_{min}) that should be able to grow CNT with a very low value of resistivity. We do not know whether it is indeed possible to use a DOE approach for generating growth recipes for CNT having the minimum resistivity. Even if the developed model had allowed us to calculate the resistivity of the vias to a fair level of accuracy, it is still a matter of speculation whether every parameter could be individually optimized using a DOE way. Another matter of concern is that, we just used nine results from a pool of eighteen. Unfortunately, the verification experiment for resistivity could not be carried out during the course of this thesis. So, at this point, we cannot be certain whether the recipe predicted in fig. 6.8 is indeed correct. Nevertheless, it had been a rewarding experience to study about the electronic properties of a CNT, and try to come out with an equation which encompasses all the different physical parameters.

$$\rho_{min} \equiv \{P1_2, P2_3, P3_1, P4_1, P5_1, P6_2, P7_1, P8_3\}$$
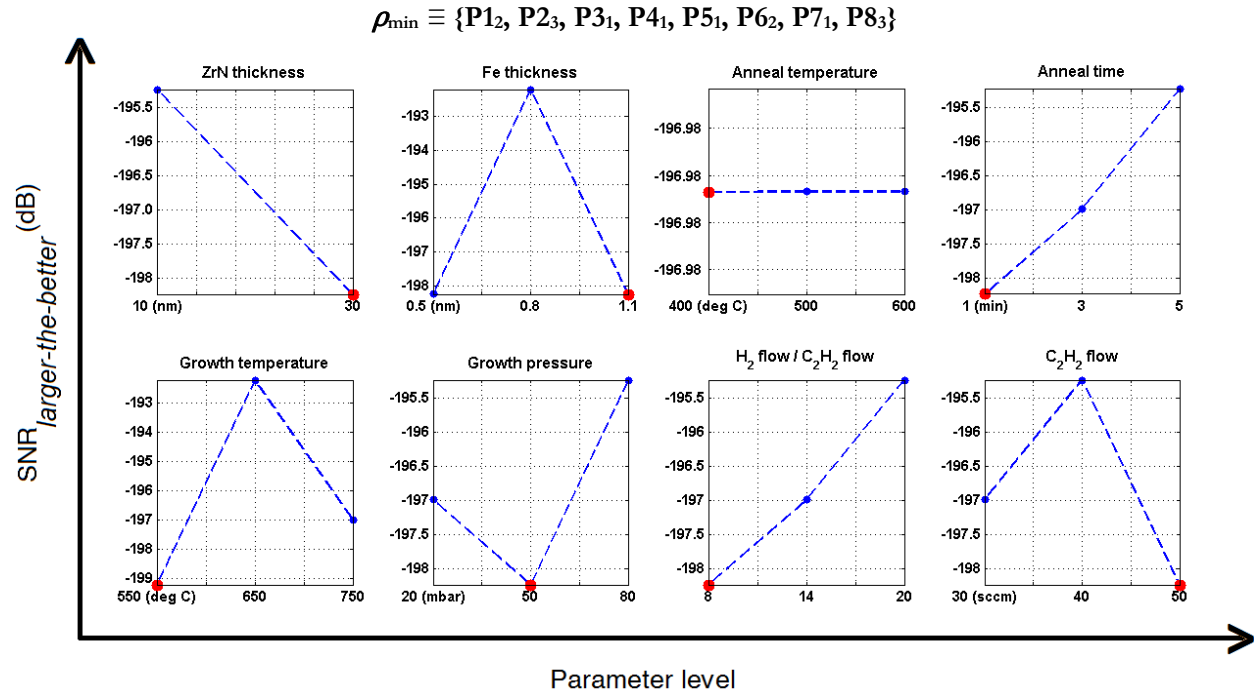
Figure 6.8: Main effects plot showing the optimum levels of substrate and growth parameters required for growing low resistivity CNT vias. The recipe could not be tested during the course of this work.

6.3.1 Optimization of growth density and quality

Fig. 6.7 had shown us why it is necessary to grow CNT with a high value of density and quality. To fulfill this requirement, the Taguchi method was used again as an attempt to maximize these two factors. The following section will briefly describe the way in which the data was collected, the analyses done, and the results obtained.

6.3.1.1 Optimization of CNT growth density

The density of all the growth samples had to be measured for optimization. For recipes with random growth, it was not possible to estimate the density; hence their values were kept arbitrarily low for calculation purposes. Fig. 6.9 shows the main effects plot for density optimization.

$$\mathbf{D_{max5}} \equiv \{\mathbf{P1_1, P2_2, P3_1, P4_3, P5_1, P6_3, P7_3, P8_1}\}$$
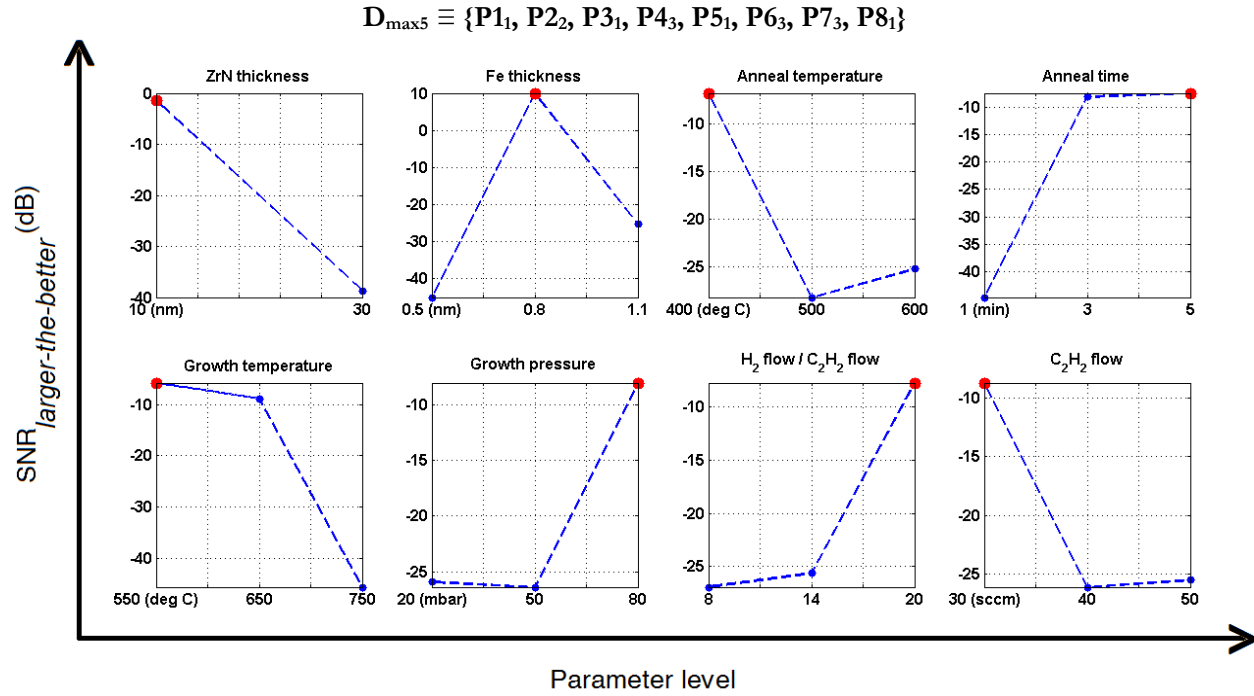
Figure 6.9: Main effects plot showing the optimum levels of substrate and growth parameters required for growing high density CNT vias. The recipe worked with a limited success.

Using the recipe predicted for maximum density (D_{max5}), CNT growth was performed and the density was estimated from a number of observations. The average density came out to be 9.88 x 10^{10} tubes/cm^2, with one observation of 11.77 x 10^{10} cm^{-2}. Even though this was not a huge improvement, the value was greater than the individual densities of the $\mathbf{L_{18}}$ samples. This showed that this recipe had worked, but with limited success. Clearly there was room for better optimization.

The partial success of the recipe was attributed to the fact that the density measurements had been done on 5 min growth samples; hence only 13 readings were used to predict the optimum recipe. As we saw in case of height optimization, the accuracy of the Taguchi method had increased when more number of results were taken into consideration. The solution was to measure the density of the 10 min growth runs and hence work with 16 results. However, taking crisp pictures of the CNT forest and counting the number of tubes was a slow and painstaking task, especially if the heights were low. So this could not be performed during the thesis. However, on the justification that density remained the same for both 5 min and 10 min growth, only the densities of growth samples from recipe 10, 12 and 17 were measured. These were recipes which had produced vertical growth only in the 10 min run. After this, when main effects plot were generated, the optimum predictions (D_{max10}) were found to be changed from the last time.

To estimate which of the recipes was more accurate, we referred to their ANOVA results, presented in table 6.4. For D_{max5}, the strong parameters were ZrN and Fe layer thicknesses, while the weak parameters were the gas flow rates, pressure and anneal temperature. This came as a bit of a surprise, as we would expect that the

CNT growth density should have been affected more strongly by the growth parameters. Consider D_{max10}, we noticed that the anneal time and the flow ratio strongly affected the growth density, which was intuitively justified. Also, when we compared D_{max10} with L_{max10}, it was found that the two recipes were remarkable similar; just the ZrN layer thickness and the C_2H_2 levels were varying (the ZrN layer hardly influenced either length or the density optimization). The similarity of the two recipes could be directly correlated to the fact that, higher growth density aided in better vertical alignment, leading to higher growth heights. From these two points, it was speculated that D_{max10} was a more accurate recipe than D_{max5}. Unfortunately, the verification of D_{max10} could not be performed during the thesis.

Table 6.4: Predicted growth recipes for maximum growth density of CNT, as obtained from Taguchi main effects plot. The parameter levels are represented by (P) and the ANOVA F-values by (F).

Experiment	Name of optimized recipe		ZrN thickness (nm)	Fe thickness (nm)	Anneal temperature (°C)	Anneal time (min)	Growth temperature (°C)	Growth pressure (mbar)	H_2 flow / C_2H_2 flow	C_2H_2 flow (sccm)
5 min growth	D_{max5}	P	10	0.8	400	5	550	80	20	30
		F	1.06	0.79	0.14	0.46	0.50	0.11	0.12	0.10
10 min growth	D_{max10}	P	10	0.8	400	5	650	20	14	50
		F	0.00	0.33	0.46	1.54	0.33	0.37	0.38	1.44

6.3.1.2 Optimization of CNT quality

The final means to decrease the resistivity of CNT vias was to maximize their quality; in other words, to produce tubes with a high degree of crystallinity, as we had seen from fig. 6.7. We made an attempt to do the same, and used the Taguchi for this purpose. Accordingly, Raman spectroscopy of the eighteen growth samples was performed, on the 10 min growth samples, and then the quality determined. Next, the main effects plot was generated to find the optimum recipe (Q_{max10}), which is shown in fig. 6.10.
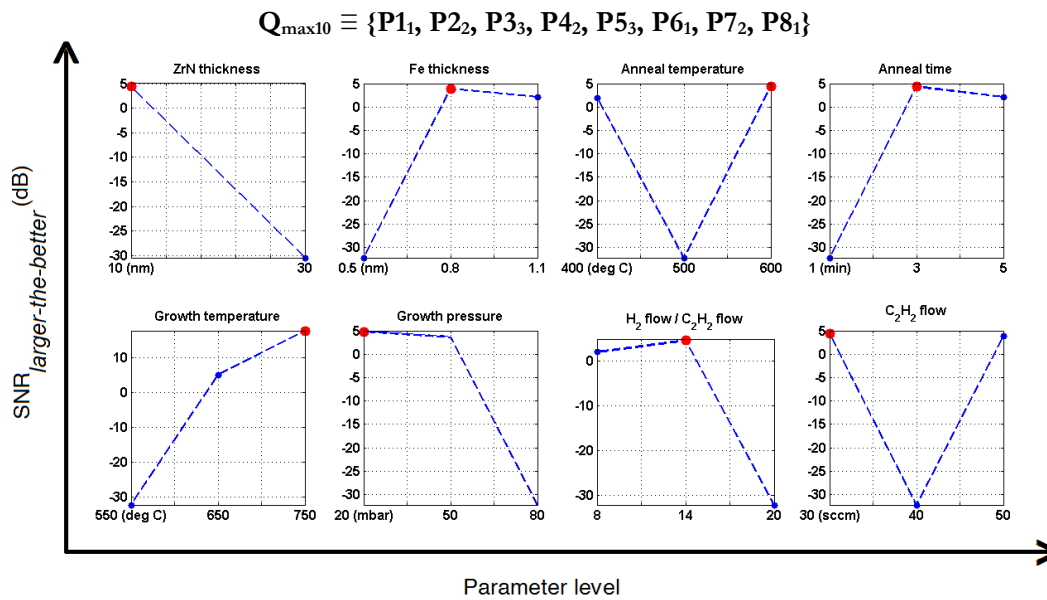
Figure 6.10: Main effects plot showing the optimum levels of substrate and growth parameters required for growing high quality CNT vias. The recipe was not successful in maximizing the quality.

Growth was performed with Q_{max10} recipe, but the results were disappointing. We got an average quality of close to 4, which was lesser than even some of the L_{18} samples.

It is tough to analyze why the DOE failed this time, since we had considered all the 17 growth samples from the 10 min growth experiment. So the argument that the DOE analysis had lost its accuracy due to incompleteness in the table would not hold good. We needed to approach this problem in a different light. After failure of the verification experiment, we wanted to understand how the CVD conditions affected the quality of the CNT, and whether it was really possible to optimize the quality by a DOE approach. Accordingly, Raman spectroscopy of the 5 min growth samples was also carried out. Here we saw an interesting result: the sample qualities for the two growth times were quite similar to each other, as shown in fig. 6.11. This meant that, perhaps the quality of the tubes did have a dependency on the growth parameters, and it was indeed possible to optimize it with a correct recipe. This inference was also verified when we found from the main effects plot, that a higher growth temperature is favorable for growing high quality CNT, as is indeed true. The only reason for failure which we could figure out was that, there had been a fault in the CVD reactor when the verification experiment was carried out; the chuck had been contaminated by a patch of photoresist. This was ignored then, and the chuck was not changed. What might have happened was, the resist evaporated at the high growth temperatures, and then re-deposited on the walls of the CNT, lowering its quality.
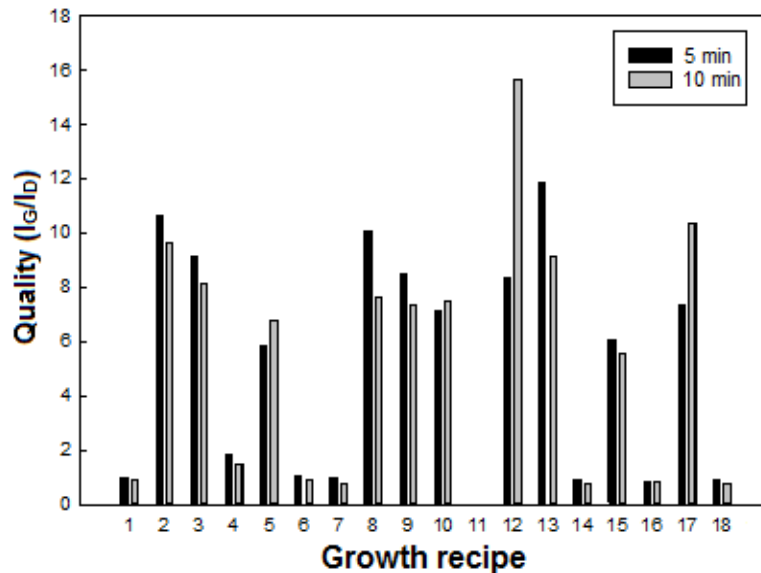
Figure 6.11: Quality values from the 5 min and 10 min growth samples, showing similar results for each growth recipe. Their main effects plot also has the same trend.

6.4 Summary

This chapter serves as the final part of the electronic modeling work done during this thesis. We aimed at measuring and then minimizing the resistivity of the as-grown CNT samples. On finding that direct electrical measurement on a CNT film was erroneous; we decided to physically characterize the samples. Several characterization techniques were used to get information about CNT parameters, like MWNT inner and outer diameters, CNT ballistic length, SWNT diameter, growth density, and the proportion of MWNT to SWNT in a via. We then used our knowledge of CNT electrical modeling to calculate the resistivity of the samples, which were found to be very high compared to Cu. Finally, as an attempt to reduce the resistivity, optimization of the CNT growth density and quality were tried. The density could be increased to around two times from the earlier values, while quality could not be optimized any further. We concluded the chapter by giving explanations on how these two parameters could be maximized. In the next and final chapter, we would be looking at our first results of CNT integration as a TSV, which, if successful, would be the culmination of this thesis work.

Chapter 7

CNT integration as TSV in a 3D stacked IC prototype: Preliminary observations

This chapter serves to be the completion of this thesis work. With the initial aim of fabricating TSV with CNT, we so far studied the different techniques in which the growth process could be optimized for producing ultra-long CNT on patterned and unpatterned catalyst islands. We also came up with an idea to grow CNT with the lowest resistivity. Now, it was time to test our findings in a real 3D-integrated circuit TSV structure.

Research on CNT integration as TSV is still in its nascent phase, and not as widespread as that of CNT vias. The reason is perhaps the difficulty to grow CNT to high lengths. Among the few publications that exist, [22, 23] uses a transfer process to contact the CNT between the top and bottom wafers, [140-142] reports a feasibility study of using CNT as TSV material, growing in only one wafer, and [143] reports CNT integration in monolithic ICs as opposed to TSV. According to our knowledge, this was the first time that CNT growth on a conductive substrate like ZrN was being attempted, for directly integrating the CNT as TSV, in stacked wafers. In this chapter, we would discuss about our growth experiments on CNT integration. Unfortunately, we were not entirely successful in our attempt; but we obtained a few starting results, which promises to guide us in the future. CNT integration has been an on-going work in our research group, and the author contributed on the aspects of CNT growth.

7.1 Brief description of the TSV process design

To build the prototype, a process had to be designed and developed, which would allow us to stack two wafers, and make electrical connection between them with CNT. The concept of making this kind of prototype was developed with recommendations of [144]. Since the process had been only conceptualized by the author, but not explicitly fabricated, only the work performed during this thesis will be explained. The complete flowchart may be found in appendix D.2 for reference.

Before starting with explaining about the process, let us look at how the final completed structure looks like; as depicted in fig. 7.1a,b. Fig. 7.1a shows the cross-sectional schematic, while fig. 7.1b shows the three dimensional structure, which is a 4-probe measurement structure. In a nutshell, the two wafers are bonded together, and the CNT is expected to grow from patterned islands on the bottom wafer, and then inside the though-Si (TS) holes drilled in the top wafer. This way, it is possible to connect electronic circuits fabricated on the two wafers by CNT vias.
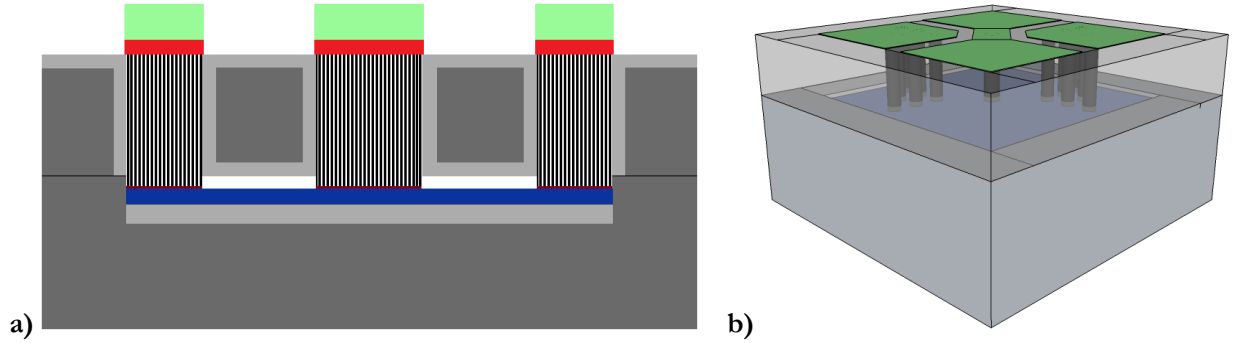
Figure 7.1: Prototype of the conceived 4-point probe 3D stacked-IC structure using CNT as the TSV material:
(a) A cross-sectional view of the schematic. Dark grey – Si; Light grey – SiO$_2$; Blue – ZrN; Brown – Fe; Black – CNT; Red – Ti; Green – Al. The figure is not to scale.
(b) A 3D representation of the prototype, showing the bottom wafer (in grey), top wafer (transparent), ZrN layer (in blue), CNT (in black), and Al metallization layer (in green). The CNT actually grows in vias etched through the top wafer.

Let us start with the bottom wafer, which had a standard thickness of 525 µm. As we note from fig. 7.1a, the wafer was etched to a certain depth (~ 120 nm) in specific regions. In those regions, the Fe and ZrN layers would be deposited. The other places, which were not etched, were used for bonding with the top wafer. To implement this, the wafer was etched in the A dies, and the B dies kept available for bonding, as shown in fig. 7.2. The type of bonding was decided to be Si-Si fusion bonding [145]. The top wafer had a thickness of 300 µm. TS-holes on the top wafer had to be DRIE etched through the bulk of the wafer, in the location of the A dies. A mask, which had been designed during this thesis, was used to set the location for the holes.
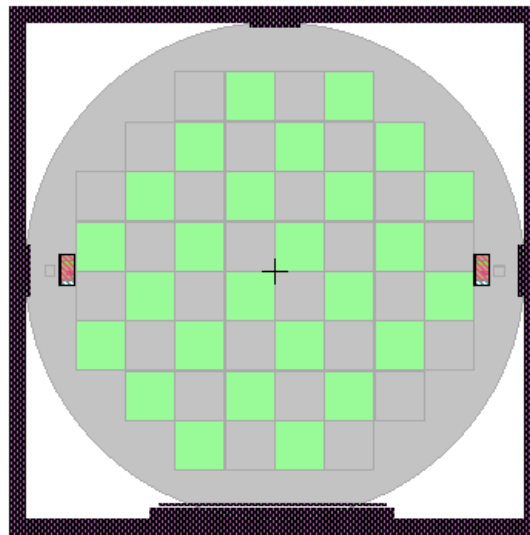
Figure7.2: Picture of the bottom wafer showing locations of A dies (in green) and B dies (in grey). The wafer was etched and subsequent catalyst deposition performed at the A dies. For the top wafer, TS-holes were etched through the bulk of the wafer at the A dies. The locations of the B-dies were used for bonding the wafers.

Brief note on bonding: Wafer bonding for TSV applications had not been used by our group before, so it was decided to use a pair of dummy wafers first, and check the strength of bonding. Bonding was done for 1 hour at 300 °C and 8 kN, and then the wafers were subjected to various stressful conditions, to observe if they could still survive the bond. Fig. 7.3 shows the infrared images of the bonded wafer pair at different stress conditions. If there were any spacing between them, then due to the film of air, interference fringes were produced. This was an easy test to see the quality of the bond. The first figure shows the wafer after it was freshly taken out of the AML. The second figure shows the wafers after they had undergone annealing at 650 °C for 5 min (temperatures they would typically expect during the growth of CNT). The third figure shows after the wafers were immersed in water, and spun dry at 600 rpm. As we can see, in all three cases, fringes appear only in the A dies but not in the B dies. This shows that there had been no disruption in the bonding. Thus these bonding conditions were applicable for the prototype as well.
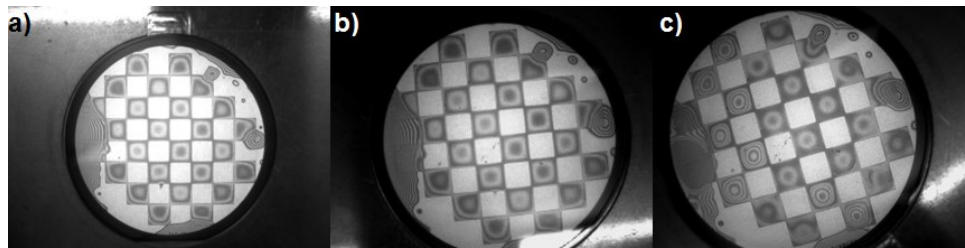
Figure 7.3: Quality of bonding at various levels of stressful conditions. The stress level increases from fig. 7.3a to c. It can be observed that the bonding has remained intact in all conditions.

The ultimate goal behind fabricating the prototype was to measure the electrical resistances of the CNT-TSVs grown through different sized holes. Using a two-point or a four-point probe measurement structure, one could easily measure the resistance from plotting the I-V characteristics. The four-point probe structure is better because it cancels the effect of the various contact resistances that are present in the measurement system [146]. Accordingly, the prototype was so designed in the form of this structure.

Fig. 7.4 shows the 3D conceptual image for the 4-point probe structure, with the CNT growing on Fe islands patterned on the ZrN substrate (blue) on the bottom wafer. Apparently, the CNT would grow in the holes drilled through the top wafer, but for clarifying the concept, the bulk of the top wafer has not been shown here. A stack of metallization was deposited and patterned on the top wafer, to form contact pads for the probe needles. Top view of a contact pad is shown in fig. 7.5a. We can see that the figure is symmetric; there is a TSV at the center through which grows the measurement CNT via, and at each of the two corners is a set of six TSV, through which, the support CNT via. The measurement CNT via is the device-under-test, i.e. the structure whose resistance is being measured; the support CNT via provides the conduction path for the current, as also mechanical support between the wafers.
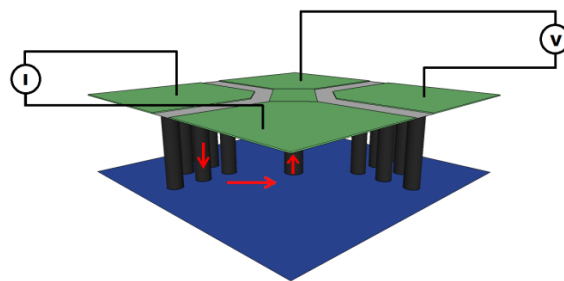
Figure 7.4: Representation of the 4-point probe measurement structure, showing the measurement and support CNT TSVs, and the direction of current

CNT resistance was intended to be measured for vias with different c/s-area; hence a mask had to be designed accordingly. In total, there was a combination of one, two or three measurement vias, with diameters ranging from 5 μm to 150 μm. Fig. 7.5b,c show the naming convention which was be used for the design. For instance, fig. 7.5b suggests that there is 1 measurement CNT-via, whose diameter is 75 μm; while in fig 7.5c there are 2 measurement CNT-vias, each of whose diameter is 75/√2 μm, so that the total area for the two became same as the previous one. The support CNT-vias had a constant diameter of 60 μm each. The complete TSV mask is shown in fig. 7.6. Hence, when each A die was patterned with this mask, it had a complete set of vias with different diameters.
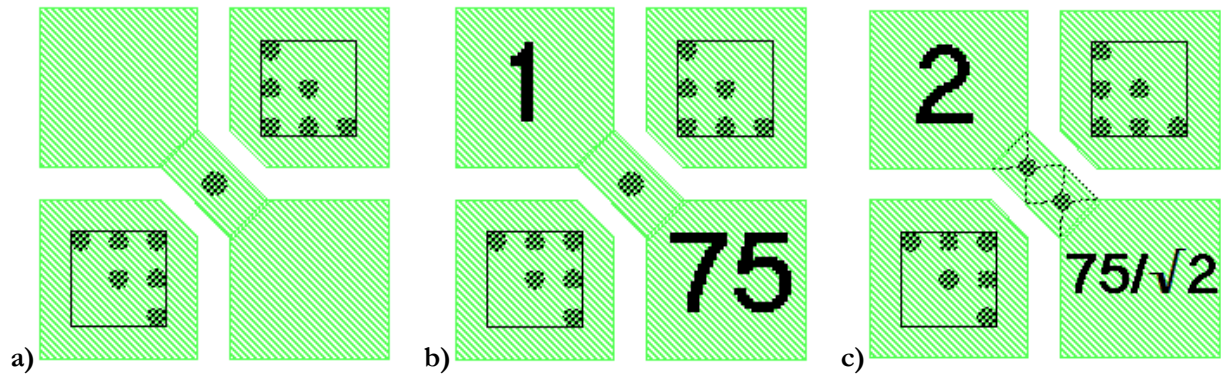
Figure 7.5: Schematic and naming conventions of the contact pad: (a) Top-view of the pad showing the locations of the measurement and support CNT vias; (b, c) Naming convention of the pad; the numbers represent the number and diameter of the measurement CNT vias in microns.
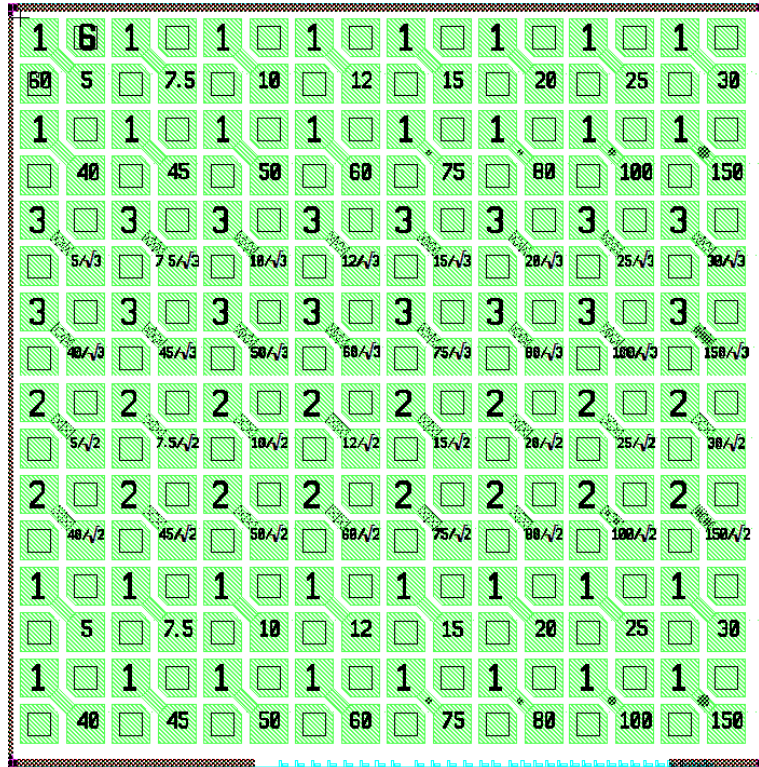
Figure 7.6: Layout of the TSV mask.

7.2 CNT growth results

7.2.1 Growth in design 1 (unpatterned catalyst layer on bottom wafer)

The first pair of wafers had a slightly different design. Contrary to fig. 7.1, where the iron layer was patterned, here the layer was continuous on each A die, as shown in fig. 7.7. Hence CNT growth was expected everywhere from the bottom wafer; and not just in the locations of the vias. It was thought that the growth of CNT under the top wafer would stop when it would hit the wafer, as the feedstock gas would not be able to reach the trench under the vias (because the vias would already be filled already with the growing CNT). With this structure fabricated, CNT growth was attempted using the L_{max10} recipe.
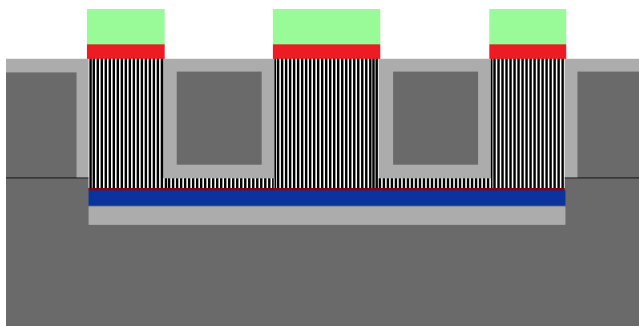
Figure 7.7: Initial concept of the prototype with a continuous catalyst layer (design 1).

After the growth run, when the wafer pair was taken out of the BlackMagic, a crack was noticed on the top wafer, which had progressed from the side towards the interior. For this reason, the subsequent metallization step could not be performed, and measurements were abandoned. However, CNT growth had indeed taken place on the bottom wafer. In fact, that the wafer had cracked, gave us a brilliant opportunity to study how the growth had been. The following section will briefly discuss about them.

We start with looking at fig. 7.8 which shows an image of the bottom wafer. The striking result here is the presence of a reverse loading effect. Growth had consistently been more in the peripheral regions and had reduced towards the center. This behavior is indeed similar to the frame-like growth examples which we discussed before. The CNT growth must then had started in the periphery and gradually progressed towards the center. Notably, the BlackMagic had crashed (due to a power problem) during this growth run in the middle of growth, so full growth did not take place. This once again points to the fact that the loading effect (or its reverse) might be dependent on the growth time; and higher the time, lesser might be the non-uniformity in growth height. Here we used the wafer-cracking as an opportunity to study the different growth stages at different locations on the wafer. Some results are shown in fig. 7.9.

Figure 7.8: Image of the bottom wafer showing a reverse loading effect. The growth has been more towards the periphery compared to the center.
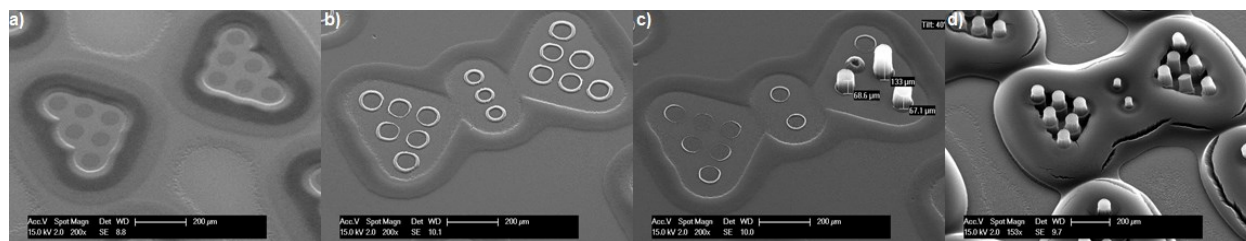
Figure 7.9: Different stages of CNT growth on the bottom wafer: (a) – No growth; (b) – Starting of growth; (c) – Intermediate growth; (d) – Complete growth.

A careful inspection of fig. 7.9d shows that there had been thick undergrowth on regions which were under the top wafer. This led us to speculate whether the wafer had cracked from due to the force of the growing CNT bundles. However improbable this may sound, but considering that millions of CNT were pushing the wafer up, then it might have been possible to crack by the pressure. Fig. 7.10 shows a close-up picture of the high undergrowth. The fact that its height was 140 μm, when the trench height was only 120 nm, suggested that CNT had kept on growing, pushing the wafer upwards, first causing it to crack and then growing further.
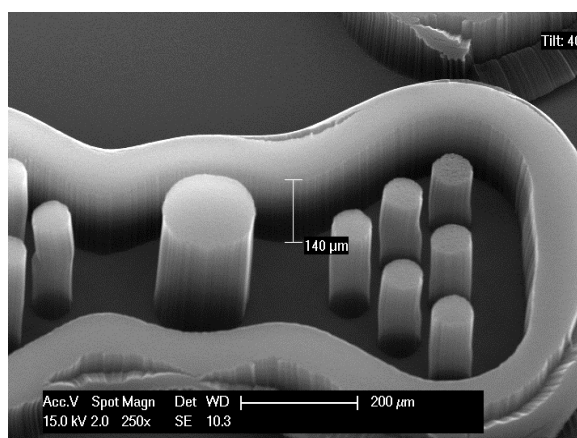
Figure 7.10: Close-up view of a measurement structure showing thick undergrowth of CNT.

7.2.1.1 Discussion on growth patterns: Loading effect revisited

In chapter 4, we had discussed the loading effect in depth, and saw how the local and global effects had caused higher growth at the centers of the islands. Till now, however, no convincing reason could be found to explain the *reverse* loading effect; only its effect was observed from time to time in different growth experiments. Here we see that the global and local effects were present in the reverse loading phenomenon as well. Fig. 7.8 had already shown us the local effect on a large scale throughout the wafer (which was just the opposite of our simulation results in section 4.2.2). Here, fig. 7.11 will show the reverse local effect occurring at each structure.
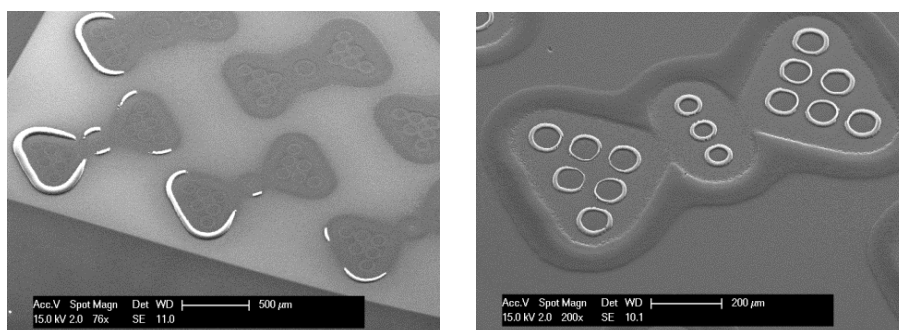
Figure 7.11: Images showing the reverse loading effect, which causes CNT growth to start from the boundaries of the catalyst islands, and then approaching towards the center.

We will present two more findings before ending with this section. In the periphery of the wafer, first the undergrowth started, and then followed by growth in via locations. Just the opposite happened in the central parts; the via-growth occurred earlier. Thinking in terms of the reverse loading effect, we can say that due to the reverse local loading, growth had started from the edges of the structures (which corresponded to undergrowth), and by the time it could progress to the center of the structures, the BlackMagic had already crashed. The result can be seen clearly in fig. 7.12a. On the other hand, in the center of the wafer, there should have been the presence of the conventional local loading effect, causing growth to start from the center of the structures (which correspond to the via locations). This can be seen in fig. 7.12b. An alternative theory may also be put forward, that sees the situation in a different light. It can be speculated that the pressure distribution in the CVD chamber might have been greater at the periphery of the chuck than at the center, causing the feedstock to enter the trenches faster, and thus causing the undergrowth first. However, this explanation cannot be confirmed as we do not have much information about pressure distribution inside the reactor.
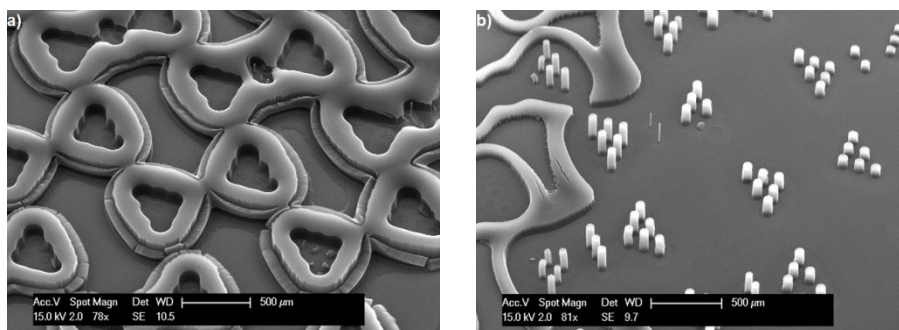
Figure 7.12: Some more images of CNT growth on the bottom wafer: (a) At the periphery of the wafer, undergrowth initiates first; (b) At the central regions, growth at the via locations occurs first.

7.2.2 Growth attempt in design 2 (patterned catalyst layer on bottom wafer)

Due to the problem of wafer breakage, it was decided to pattern the catalyst island just under the TS-holes, as was seen in fig. 7.1a. Accordingly a second structure was created, and growth attempted again with recipe L_{max10}. This time, we got absolutely no CNT growth in any of the vias across the wafer, and there was not even any random growth. Fig. 7.13 shows a typical via which produced no growth.

There may be several reasons why growth did not happen, and we came out with two explanations. Firstly, the growth recipe used here (L_{max10}) was the one optimized for the maximum growth height on an unpatterned layer of catalyst. Since it worked well for the last design, we had assumed that it would work for this design as well. However, now that the catalyst was patterned, it might have had lost its efficiency. We should note that L_{max10} had not been tested for patterned growth during this research. As a matter of fact, we did not expect that loading effect could have happened, as the islands were only exposed locally through jets of feedstock gas flowing through the TS-holes (which would have given the gas an impression that the catalyst was continuous). For this reason, recipe 15 or 16 was not tried. This situation, coupled with the fact that the entire wafer might have been suffering from a loading condition (as before) would probably have further affected the growth mechanism. Unless a strong quantitative analysis of loading effect is carried out in future, it is indeed difficult to design a growth recipe which would be successful in this case.

Our second explanation was that, the Fe catalyst layer might have got damaged during all the processing steps that the wafer had undergone. Since Fe deposition was one of the earliest steps, this ultra-thin layer could have easily got damaged during the subsequent process runs. Even though this did not happen in the previous case, but chances were there, that it may have had during this time.
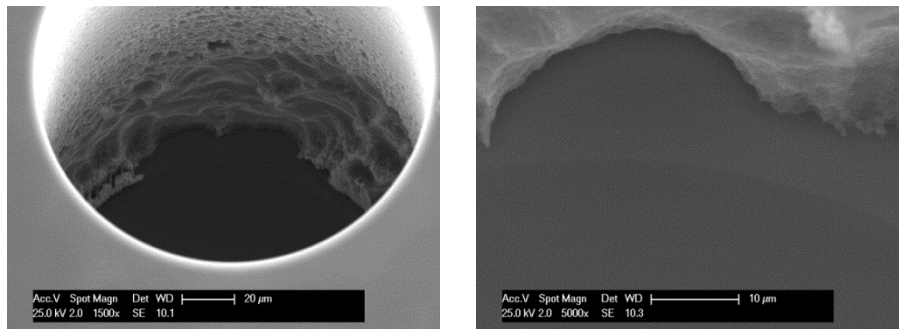
Figure 7.13: Image of a through silicon (TS) hole taken from the top, with its close-up view, showing absolutely no growth. The circular catalyst layer pattern can be clearly observed.

7.3 Summary

This final chapter of the thesis gave the first results of integrating CNT as TSV material, directly on a conductive substrate. The process flow was explained in brief, and the growth results were analyzed. In the first design, with a continuous catalyst layer, the L_{max10} recipe was used for CNT growth. Growth occurred successfully, but the growing CNT bundles forced the top wafer to break. We used this opportunity to study the growth pattern on the bottom wafer, and found that there was a strong reverse loading effect. In the second design, with a patterned catalyst layer, the same recipe was used for CNT growth. This time, however, growth did not happen at all. It was speculated that either the Fe layer had got damaged during the processing steps, or that, the L_{max10} recipe was ineffective in producing patterned CNT growth.

Final words:

With this section, we conclude this chapter, and eventually this thesis. It would have definitely been an achievement to have successfully fabricated a working TSV from CNT as a part of this thesis. However, the volume of results obtained during this work gave us a strong direction of research.

At present, more batches of TSV wafers are being fabricated, and different growth recipes are being designed and tested. Also different catalyst materials are being used, to bring down the growth temperature to CMOS process levels.

With the frantic pace of research work going on, we expect to fabricate a successful working device of a CNT-based TSV structure in the future, and contribute to this novel field of microelectronics.

Conclusion

This thesis served as the first step towards fabricating ultra-long carbon nanotubes, for the purpose of making through-silicon-vias in 3D-integrated circuits. In the process, we learnt about the current problems of the microelectronics industry, from the prospective of interconnects. To reduce the increasing interconnect delay over successive technology nodes, the move to 3D-integration technology, and the problems of using copper vias in this technology, was discussed. Carbon nanotube was hence proposed as a viable alternative for fabricating high aspect-ratio through-silicon vias. CVD growth of CNT was studied, and it was concluded that in order to increase the growth height from present values, a set of right substrate combination was needed, on the basis of their surface energy differences. A Fe catalyst layer with a ZrN support layer was identified as perfect materials for this purpose.

Initial growth experiments with a standard LPCVD (Nominal) recipe, indeed verified our assumption; producing CNT bundles in excess of 200 μm height. However, it was seen that the recipe was extremely sensitive to the thickness of the Fe catalyst layer, and even a difference of a few angstroms resulted in a huge reduction in height. Further, the recipe often produced growth only at random locations on the wafer, and much lesser growth heights were obtained for patterned catalyst islands. Moreover, the growth temperature of 650 °C was too high to be used for CMOS processes, and the density and quality of the samples had to be further maximized. All these factors suggested that we had to redesign the growth recipe.

Studying about CNT CVD growth, we identified that there were six key parameters which played a crucial part in our process, and they were the catalyst annealing temperature and time, growth temperature and pressure, and the C_2H_2 and H_2 gas flow rates. These six, combined with the thicknesses of the two substrates, gave us 8 parameters to optimize for. On realizing that an improbable number of experiments were necessary in order to understand the effects of all these parameters, we decided to follow a design of experiments approach.

Various DOE tools were studied and after comparing the merits and demerits of each, the Taguchi method was selected, and the theory behind the mechanism of this method was explored. Taguchi offered us only 18 number of experiments to be performed. Moreover, it worked with signal-to-noise ratio (SNR) values of the results, which was helpful for our experiments. Further, it generated a main effects plot from the analyzed data, which showed the strength and the right values of parameters needed to optimize the response.

Using the experimental table of Taguchi (the L_{18} orthogonal array), 18 growth recipes were designed and installed in the BlackMagic. The initial growth experiments were first performed on unpatterned catalyst layer, for a time of 5 min. We observed that there was a huge variation in growth height for different recipes (from no growth to > 250 μm), and also the existence of growth patterns. To understand these results, growth was again performed for 10 min. We observed how growth was extremely sensitive to the catalyst layer thickness, and how some recipes took more time to support vertical CNT growth. We then provided an explanation, on how the different substrate and CVD conditions govern the growth height, and understood the origin behind the patterns.

With the data of the 5 min and 10 min growth runs, the Taguchi analysis was done and we got different optimum recipes from each of them (L_{max5} and L_{max10}). Both were experimentally verified, and it was seen that L_{max10} performed better than L_{max5}, producing super-growth of CNT of almost a millimeter. We analyzed the

two recipes and explained why L_{max10} was successful. Finally, the results of a test experiment were reported, which again confirmed the growth sensitivity to the catalyst thickness.

Study of CNT growth is never complete without investigating the growth mechanism on patterned catalyst islands. For this, we started with developing a lithography procedure (P3256) which could selectively etch the Fe, without attacking the ZrN support. Growth experiments were first performed with the Nominal recipe using arbitrary masks. It was here that we observed that growth was severely affected by the catalyst loading effect; which was causing more growth in on large islands, in the center of islands, and in regions where there were a large number of islands (or high fill-factor). We realized that unless the mechanism of this effect was understood, we would not be able to proceed further with the aim of CNT integration.

The first goal was to quantitatively study the loading effect, and the second goal was to find a recipe which would be robust to this effect, and support uniform and high CNT growth. Subsequently, a thorough theoretical analysis was done on the loading effect phenomenon, and we identified the global and the local loading effects. Simulations were done, and explanations were given in our analysis. In order to do the quantitative analysis, a mask (P3256_V2_CATALYST) was designed which had patterns of different shapes, sizes and distributions. Taguchi growth experiments were performed with it, and the results showed that only two recipes (15 and 16) worked, promoting uniform CNT growth of heights more than 200 µm, on any kind of patterns. This meant that they were highly robust to this phenomenon. However, since the other recipes did not produce any growth at all, a quantitative analysis could not be performed. Our analyses ended with a brief discussion on the buckling of CNT structures, and how it was related to the fill-factor.

A CNT TSV should not only be of high length, but it is also expected to have extremely low resistivity; of values lower than copper. With this in mind, the resistivity of the as-grown CNT bundles was intended to be minimized. For this purpose, a detailed study was done to understand the physics behind electronic conduction in a CNT. As a next step, we studied the equivalent circuit models of the groups of Prof. A. Naeemi and Prof. K. Banerjee; and analyzed the equivalent circuits of a single SWNT and a single MWNT. Various CNT parameters like growth length, ballistic length and diameter were found to contribute to the resistance. To find the value of resistivity, a simple model was developed, which accommodated two more factors; the packing density of CNT and the proportion of MWNT of SWNT in the via.

The CNT samples were physically characterized to obtain these parameters. We used the TEM to measure the MWNT inner and outer diameters, Raman spectroscopy for ballistic length and SWNT diameter, and SEM for the packing density. The MWNT proportion was found out from simulation. With all these values, the resistances and resistivities of the growth samples were calculated. Further the validity of the model was checked by reported resistivity values in literature, and it was found that they were within an order of magnitude.

It was found that our CNT samples had a resistivity in the range of 10^4 µΩ cm; whereas the resistivity of Cu in TSV is only 5 µΩ-cm. Two solutions were proposed to bring down this huge difference. First of all, a Taguchi approach could be tried directly on the measured resistivity values, to generate a recipe which could grow CNT with low resistivity. The other approach was to try and increase the density and quality of the CNT samples. From simulations, it was seen that a density of the order of 10^{14} tubes /cm^2 or an ultra-high quality of about 10^3 (ballistic length of more than 4 µm) was needed; whereas, our present best values were 10^{10} tubes / cm^2 and 50 respectively. Taguchi optimization on these two factors was again attempted. The density optimization worked with a limited success, increasing the density to about two times the earlier

values. However, the quality optimization recipe did not work. We gave an explanation on the accuracy of these two optimizations.

As the final closure to the thesis, we fabricated a basic 3D stacked-IC in the form of a 4-point probe measurement structure, with ultra-long CNT to be integrated as the via material. The novelty in our design was that, we were using fabricating TSV directly on a conductive layer of ZrN. We considered two types of design; the initial design having a continuous layer of catalyst island on the bottom wafer, and the final design with patterned islands. Growth was attempted using the L_{max10} recipe, and the force of the growing CNT bundles caused the top wafer to crack. However this allowed us the chance to inspect the growth mechanism on the bottom wafer, where we saw the presence of a strong reverse loading effect. Finally, in the second design, growth was attempted with the L_{max10}, and we got absolutely no growth. We explained that it could be either due to the damage of the catalyst layer due to the complex process runs, or that, this recipe was inefficient in producing growth on patterned islands. At present, a second batch of wafer is being fabricated, and this time the recipe 15 would be used for CNT growth.

This sums up the total volume of work, which had been done during the period of this thesis.

Recommendations for future work

During the course of the thesis, I had the chance to identify a lot of areas of improvement within the scope of this topic. They are listed below, and a brief description about them is presented.

1. Fixing the 'loose ends' of the thesis: If we recall, a few of the things had not seen the light of completion. The D_{max10} recipe needs to be verified to see if we can get a higher growth density. Secondly, the Q_{max10} recipe needs to be performed again on a cleaned reactor chuck. The ρ_{min} recipe needs to be experimentally verified, to see if it is indeed possible to reduce the resistivity using a DOE approach. The quantitative analysis of loading effect can be completed by using a different mask and/or different recipes.

2. Bringing down the growth temperature: The two important recipes, which produced high growth lengths (L_{max10} and recipe 15), both grew CNT at 650 ^{O}C, a temperature too high for CMOS processes. As mentioned earlier, our group had already successfully demonstrated that CNT can be grown at temperatures as low as 350 ^{O}C, using a Co/TiN combination. This is surely a motivation to try Co as a catalyst for future experiments.

3. Using a different DOE technique: From the ANOVA analyses, it was seen that for height optimization, the ZrN thickness and the CVD chamber pressure were not very important. This gives us two less parameters to work with. Thus, a RSM technique like CCD can be used; which would give us a lesser number of experiments this time.

4. Use of Grey analysis: The theory behind the Grey analysis had been explained in this thesis; but it was not used any time. Grey analysis can indeed be used to simultaneously maximize Density and Quality, or maximize Length and minimize Resistivity using a single recipe only.

5. Modeling of capacitance and inductance: This thesis had only modeled the resistance of CNT, and had not considered the capacitance and inductance. These two will be important to understand the behavior of a CNT-TSV under AC excitation. It is thus highly recommended to study the physics-based models for capacitive and inductive behavior. Additionally, the effect of contact resistance for different substrates must also be included in the resistivity analysis, as it is the biggest contributor towards the overall resistance.

6. Study of thermal behavior of CNT: Thermal properties of CNT should also be well-studied if one would like to use them as TSV. The thermal conductivity of short CNT vias was measured using the 3ω voltage method by our group before (where the author participated as a summer intern). We obtained low thermal conductivity values of a few W/mk [147]. To improve this value beyond that of Cu (400 W/mK), research on high quality CNT growth should be carried out. This previous study on short vias can also be extended to measure conductivities of the quality ultra-long CNT grown during this thesis.

7. Research on hybrid TSV: It would indeed be nice if we could incorporate the best properties of Cu and CNT in the TSV. This is a very new field of research, promising exceptional performance of the hybrid vias. So research should be focused in 'mixing' CNT and other novel materials with Cu, to fabricate interconnects.

APPENDICES

Appendix A

'Nominal' growth recipe of the AIXTRON BlackMagic Pro CVD reactor

COMM N2, N2, C2H2, H2	******************************
COMM LPCVD recipe, C2H2 is added after Tgrowth has been reached	*Comment lines*
COMM Now also includes substrate reference for pre-anneal	******************************
VALV 1 OPEN	**PRE-GROWTH CONDITIONING**
TUNE PCON Fully open	
PCON ON 1 1	*Waiting until pressure falls from*
WAIT PRES < 0.10	*ambient to 0.10 mbar*
VALV 1 CLOSE	
FLOW 6 ON 700	*Introducing H_2 at 700 sccm*
FLOW 1 ON 200	*Introducing N_2 at 200 sccm*
FLOW 3 ON 0	
SENS SF 10	
TUNE HTSF 500 SF 700H2 200N2 80mbar	*Ramping up heater before pressure*
HEAT ON 400.0 300.0	*is increased to growth conditions*
WAIT TEMP > 390.0	
TUNE PCON lpcvd 80mbar	******************************
PCON ON 80.0 1.0	**GROWTH PERIOD**
WAIT PRES > 75.00	*Ramping up pressure to growth*
	condition (80 mbar)
HEAT ON 500.0 150.0	
WAIT TEMP > 495.0	*Ramping up heater to anneal*
	temperature (500 ^{O}C)
WAIT TIME > 180	*Annealing of catalyst (3 min)*
TUNE HTSF 650C SF 700H2 200N2 80mbar	
HEAT ON 650.0 300.0	*Ramping up heater to*
	growth temperature (650 ^{O}C)
WAIT TEMP > 645.0	
FLOW 3 ON 50	*Introducing C_2H_2 at 50 sccm*
WAIT TIME > 300	*Growth of CNT*
FLOW 3 OFF	******************************
FLOW 6 OFF	**POST-GROWTH CONDITIONING**
	Turning off heater and C_2H_2
HEAT OFF	*and H_2 supplies*
VALV 1 OPEN	
PCON OFF	
FLOW 1 OFF	
VALV 3 OPEN	

```
WAIT PRES < 0.30                          Waiting until pressure falls to 30 mbar
VALV 3 CLOSE
FLOW 1 ON 1000                                      Introducing N₂ gas to purge
FLOW 2 ON 2000                                             the reactor interior
SENS TC 600
WAIT TEMP < 600.0
FLOW 2 ON 4000
WAIT TIME > 15
FLOW 2 ON 6000                                         Purging and cooling down
                                                                   the reactor

FLOW 1 ON 2500
WAIT TIME > 15
FLOW 2 ON 8000
FLOW 1 ON 5000
WAIT TEMP < 400.0
FLOW 2 OFF
FLOW 1 OFF
WAIT PRES < 0.10                          *****************************
```

Appendix B

Tuning the AIXTRON BlackMagic Pro CVD reactor

The BlackMagic CVD reactor, when installed in the cleanroom, had a set of standard LPCVD CNT growth recipes, developed by its manufacturers. All the CNT growth experiments, performed before the start of this thesis work, had used one of these standard recipes. During this thesis, many new recipes were installed in the reactor, according to the requirements of the Taguchi design. However, before proceeding with growth experiments, the reactor had to be conditioned so as to make it compatible with these new recipes.

1. It was a challenging task, when a recipe had a short anneal time at a low temperature, and the growth was at a high temperature. For these cases, it was crucial that enough power was delivered to the heater so that it could quickly ramp up from the anneal to the growth temperatures, without over-annealing too much. Sometimes, the annealing time was intentionally reduced, so as to compensate for the ramp up time.

2. Changing the gas flow ratio and flow rates would initially result in fluctuation of the temperature and pressure during the growth period. The reactor had default PID loop settings for these controllers, which needed to be retuned for the new growth recipes, which were done manually for each recipe. Only after the temperature, pressure, H_2 and C_2H_2 flow rates showed stable, non-oscillatory behavior during the growth process, the recipes were declared fir to be used.

Fig. B.1 shows the behavior of the BlackMagic, for recipe 6, before and after the tuning process. The catalyst anneal occurs at 600 ^{O}C for 5 min. In the first figure, the default power delivered to the heater was low (35 %), and its PID loop tuning resulted in a much damped response. As a result, it took a long time (12.5 min) before the anneal temperature was even reached (the samples were loaded at ~ 300 ^{O}C). So this resulted in a heavy over-anneal of the catalyst. Adjusting the PID control settings of the heater, and also increasing its power (75 %) significantly reduced the time to reach the anneal temperature (1.5 min). Also the anneal time in the recipe was reduced. These ensured that the annealing conditions stayed the same.
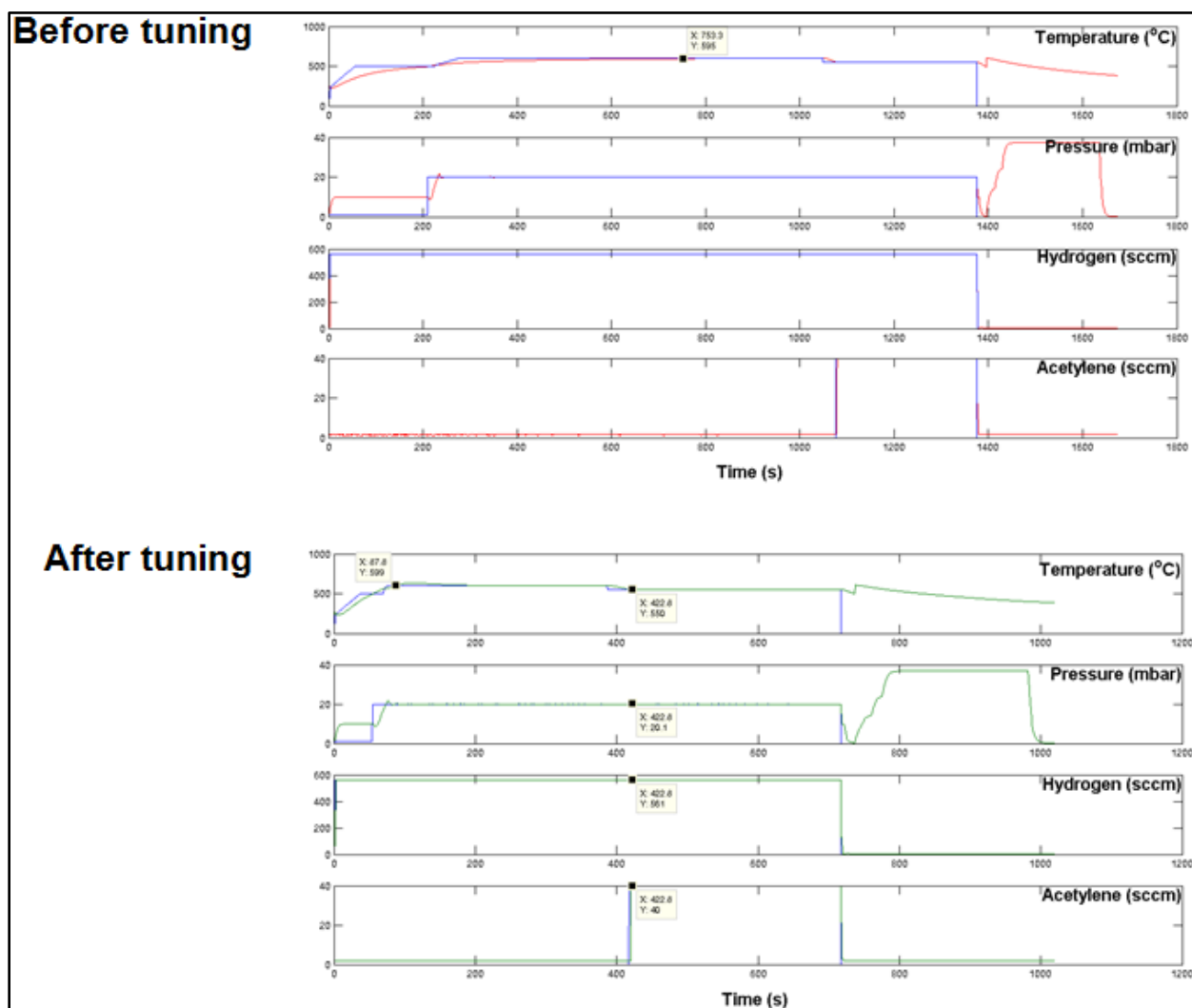
Figure B.1: Response of the BlackMagic CVD reactor for a growth recipe, before and after tuning of the reactor (in blue: ideal response; in green: real response). For this recipe, prevention of over-annealing was the task. By adjusting the heater PID control and delivered power, the ramp-up time to the anneal temperature was reduced from 12.5 min to 1.5 min.

Appendix C

Mask layout: P3256_V2_CATALYST

Layout 1

In lines of the concept of the three-tier interconnect structure (Global, Intermediate, Local), Layout 1 consists of a set of squares and other shapes, that are of different sizes (x) and separations ($x*y$)

Table C.1: Features of the different patterns of Layout 1: shapes, sizes and distributions.

Block	Shape	Local	Intermediate	Global	Fill-factor ($F = 1/y$)
Layout 1.A	Square	$x = 2$	$x = 5$	$x = 10$	$y = 1, 2.5, 5, 10$
Layout 1.B	Square	$x = 10$	$x = 25$	$x = 50$	$y = 0.2, 0.5, 0.8, 1, 2.5, 5, 10$
Layout 1.C	Square	$x = 20$	$x = 50$	$x = 100$	$y = 0.2, 0.5, 0.8, 1, 2.5, 5$
Layout 1.D	Square	$x = 20$	$x = 50$	$x = 100$	$y = 10$
Layout 1.E	Circle	$x = 10$	$x = 25$	$x = 50$	$y = 10$
	Donut	,,	,,	,,	,,
	Square donut	,,	,,	,,	,,
	Rectangle	,,	,,	,,	,,
Layout 1.F	Bridge 1	$x = 10$	$x = 25$	$x = 50$	$y = 1$
Layout 1.G	Bridge 2	$x = 10$	$x = 25$	$x = 50$	$y = 1$
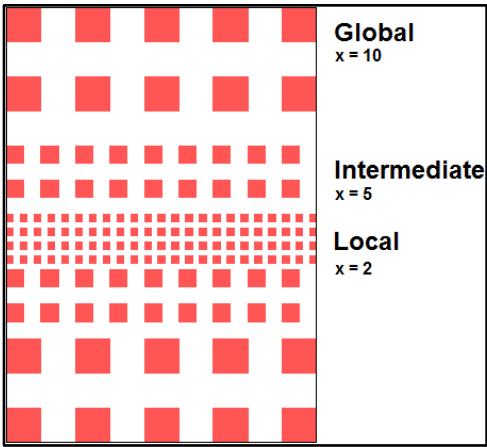
Figure C.1a: Layout 1.A
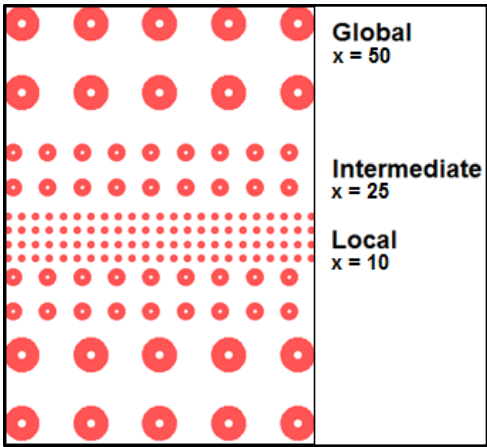
Figure C.1b: Layout 1.E (Donut)

Layout 2

Layout 2.A

Layout 2.A consists of four similar rows of blocks, each containing squares of dimension (x) 25 μm, but a **F** value, corresponding to $y = 10$ (sparse), $y = 5$ (intermediate), $y = 1$ (intermediate) and $y = 0.2$ (dense), from left to right.

Layout 2.B

It is complementary of the previous layout.

Layout 2.C

Equivalent to Layout 2.A, but with Circle, Donut, Square donut and Rectangle shapes instead of Square. Their dimensions (x) are 25 μm, and the **F** corresponds to $y = 1$.

Layout 2.D

Consists of four identical rows of blocks, with dimensions (x) gradually increasing from 2 μm, 4 μm, 20 μm and 100 μm, from the left to the right. The squares in the blocks are separated from each other by a constant distance of 20 μm, which means that, their **F** corresponds to $y = 10$, $y = 5$, $y = 1$ and $y = 0.2$ respectively.

Layout 2.E

Equivalent to Layout 2.D, but the squares are separated by 30 μm. The y values are maintained same as the previous case. Hence the blocks have dimensions (x) of 3 μm, 6 μm, 30 μm and 150 μm respectively.

Layout 2.F

This layout is equivalent to layout 2.1 but the separations between the blocks decrease from the top to the bottom, corresponding to y values of 30, 20, 10, 5 and 1.
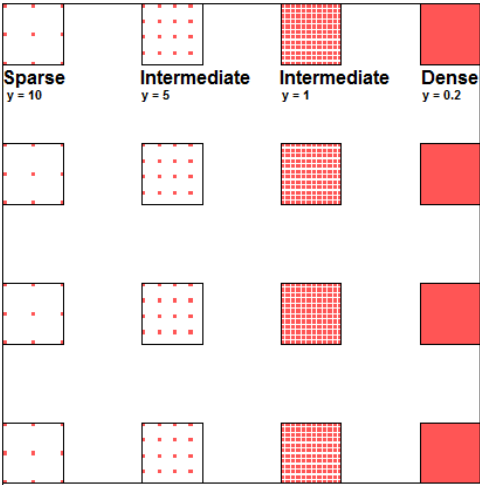
Figure C.2a: Layout 2.A
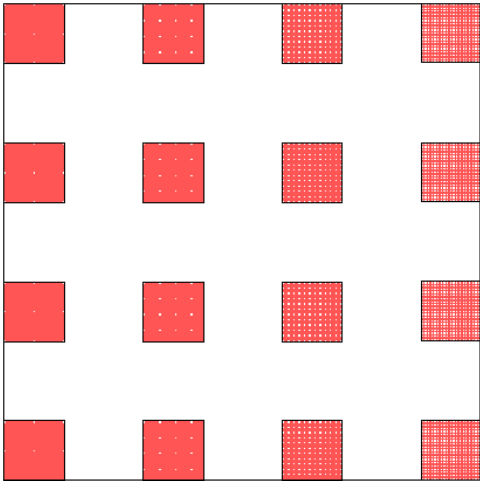
Figure C.2b: Layout 2.B
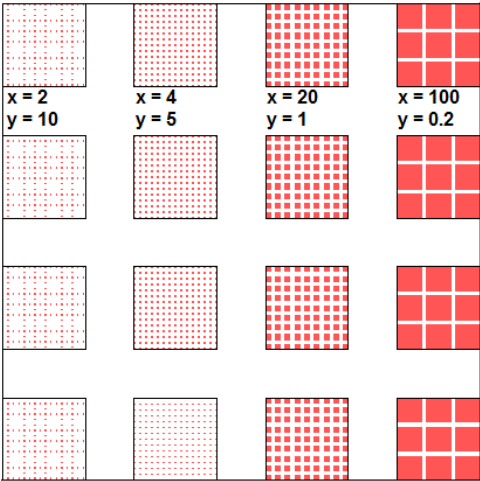
Figure C.2c: Layout 2.D
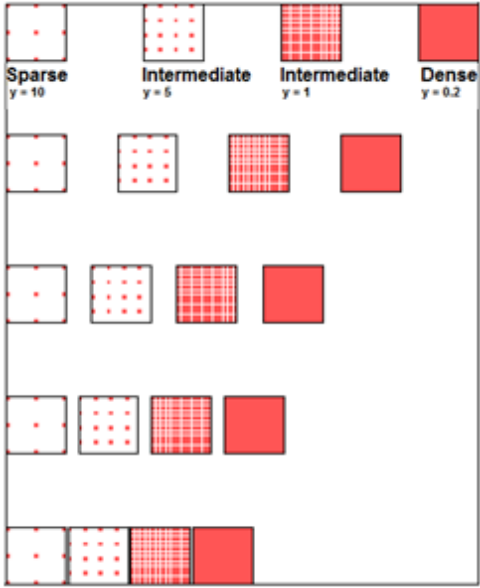
Figure C.2d: Layout 2.F

Layout 3

Layout 3.A

The inner red spiral has a thickness (x) of 10 μm, the middle spiral is 25 μm, and the outer spiral is 50 μm.

They are also separated by a distance of 10 μm and 25 μm respectively, making a **F** corresponding to $y = 1$.

Layout 3.B, Layout 3.C

Equivalent to Layout 3.1 with spiral dimensions (x) of 10 μm, 25 μm and 50 μm; but now with a y value of 10 and 0.2 respectively.
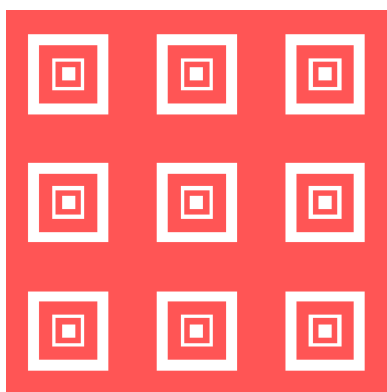
Figure C.3a: Layout 3.A   **Figure C.3b:** Layout 3.B   **Figure C.3c:** Layout 3.C
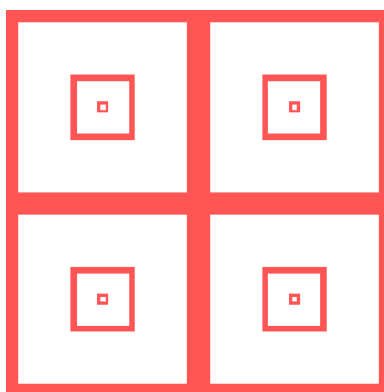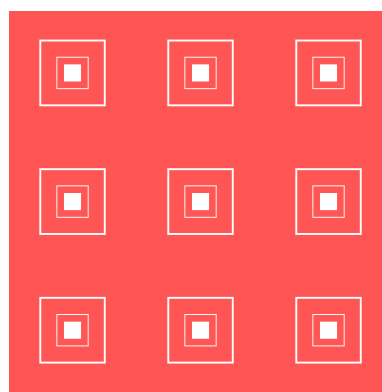
Layout 4

Layout 4.A
This layout is created only with squares of dimension 10 μm, and separated by large distances resulting in a low F value of 0.01.

Layout 4.B
This layout is again created with squares of dimension 10 μm, but separated by small distances, which result in a moderate F value of 0.3.

Layout 4.C
This layout consists of a combination of squares of many dimensions (10, 25, 50, 100 and 500 μm) which gives a high F value of around 0.6.

Layout 4.D
In this layout, there are squares of dimensions 10 μm, 25 μm and 50 μm, and having a moderate F value of around 0.2.
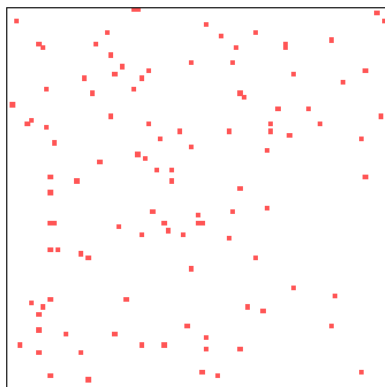
Figure C.4a: Layout 4.A
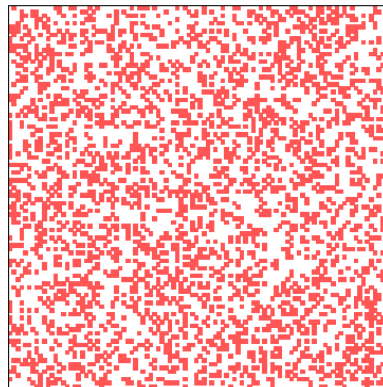
Figure C.4b: Layout 4.B
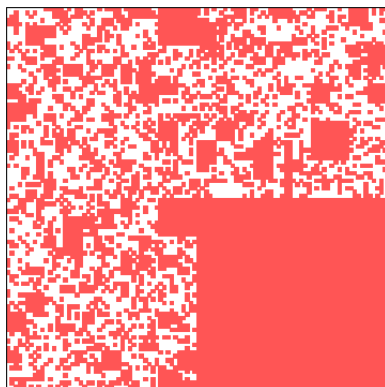
Figure C.4c: Layout 4.C
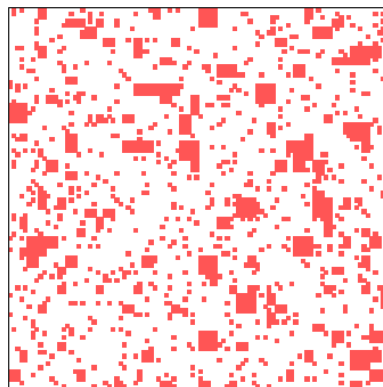
Figure C.4d: Layout 4.D

Layout 5

This is the last type of layout on the mask, and consists of a collection of squares and rectangles, arranged in concentric squares. Two adjacent concentric squares are separated by a distance of $y = 10$. In the entire layout, there are squares from 500 μm a side to 2 μm a side; and separations from 1000 μm to 2 μm. This layout contains the biggest variation in pattern dimension and spacing.
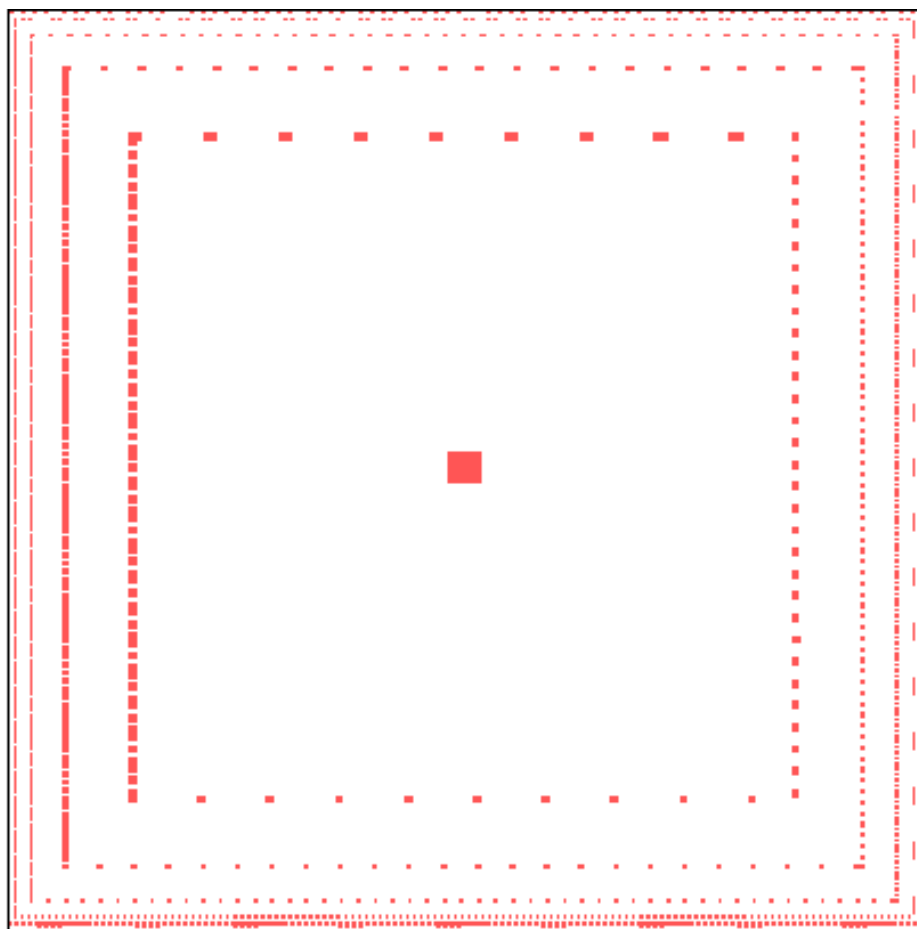
Figure C.5: Layout 5

Appendix D

Process flowcharts

Appendix D.1
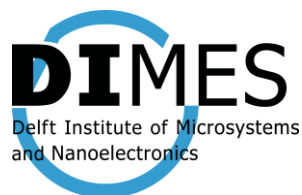
P3256

FLOWCHART

10 test wafers
Optimizing ZrN/Fe growth conditions

Sten Vollebregt & Sourish Banerjee (TFT Group)

VALID FROM: 02/2013

DIMES - DELFT UNIVERSITY OF TECHNOLOGY

Address   :   Feldmannweg 17, 2628 CT Delft, The Netherlands

P.O. Box :   5053, 2600 GB Delft, The Netherlands

Phone   :   +31 - (0)15 - 2786788

Fax   :   +31 - (0)15 - 2622163

Website   :   www.dimes.tudelft.nl

GENERAL REMARKS

1. Always handle wafers with care during processing, and wear cleanroom gloves. Work as clean as possible.

2. Always check equipment and process conditions before starting a process.

   In case of problems with equipment operation or contamination, directly notify the responsible person(s) **and other users**. Do not try to repair or clean unknown equipment yourself, and never try to refresh a contaminated etch or cleaning bath!

3. Always clean wafers after several hours of storage before performing a coating, a furnace or a deposition step. After a furnace step the wafers do not have to be cleaned again if the next process step is carried out immediately.

   Use the correct procedure for cleaning:

- Acetone or Tepla stripper	for photoresist removal
- HNO3 100%	for wafers which are not contaminated with a metal layer
- HNO3 100% metaal	for wafers which are or have been in contact with a metal
- HNO3 100% and HNO3 65%	for all wafers without metal

   Note: The mentioned cleaning procedures may only be applied in the Class 100 cleanroom for uncontaminated silicon wafers. Wafers which are contaminated and wafers made from other materials than silicon are subject to PAC rules, and may have to be cleaned elsewhere!

4. Wafers that are contaminated may never be processed in any of the equipment without permission of the PAC committee. Special precautions may need to be applied, like the use of a special substrate holder.

   Wafers that are covered with a resist or a metal layer may never be processed in a furnace. Only alloying is allowed for wafers with an aluminum layer.

5. Layer thickness measurements may be performed on the process wafers using the Leitz MPV-SP or Woollam equipment. If this is not possible, or when sheet resistance and/or junction depth measurements must be performed, a test wafer must be processed with the process wafers.

6. The use of "non-standard" materials for processing in the class 100 cleanroom and SAL must always be evaluated and approved by the PAC. It is strictly forbidden to use these materials without permission.

   All substrates, layers and chemicals which are not standard being used in the Dimes 01/02/03 or Dimos 01 production processes are considered to be "non-standard" materials, and possibly contaminating. See the PAC rules & Instructions (available on the internet) for more details.

STARTING MATERIAL

Use 10 **single side polished test wafer**, with the following specifications:

Type:	p-type, boron
Orientation:	1-0-0, 0 deg off orientation
Resistivity:	2-5 Ωcm
Thickness:	525 $\pm$ 15 μm
Diameter:	100.0 $\pm$ 0.2 mm

Wafers taken out of an already opened box must be cleaned before processing, according to the standard procedure.
Wafers taken out of an unopened wafer box do not have to be cleaned before processing**.**

P3256

1. Support layer deposition @ Class 100
Use the TRIKON SIGMA sputter coater for the deposition of the different metal support layers on the process wafers.
Follow the operating instructions from the manual when using this machine.

30 nm ZrN @ 350C

Visual inspection: the metal layer must look shiny.

Switch to green box

2. Catalyst deposition @ Class 10000
Use the CHA evaporator to deposit the Fe catalyst layer, optimal thickness to be determined. **Use contaminated shields.**

3. Lithography @ Class 100
- Perform 5 min. HMDS in the manual HMDS station using the **Pt carrier**
- Use the manual coater in the red room with **Cu chuck** to coat the wafers with 1.4 μm SPR3012 resist.
- After coating perform a 60 sec 95 °C soft bake, **put a dummy wafer underneath the wafer**.
- Expose for 5 sec. on EVG 420 using a contact aligner mask, **use Cu chuck**
- Perform a 60 sec 115 °C post exposure bake, **put a dummy wafer underneath the wafer**.
- Manual development using **Cu glassware** and MF322 developer
- Perform a 120 sec 100 °C hard bake, **put a dummy wafer underneath the wafer**.

4. Etching in SAL
Use wet etching to pattern the Fe:
5 min in diluted HNO_3 (99%) (5-10% HNO_3 in water) should do.

Rinse till 5 MΩ, and dry using manual spinner and **Cu chuck.**

After use put the solution in its own dedicated and labeled storage bottle for future use.

5. Photoresist removal in SAL
- Remove the photoresist using some Acetone from a spray bottle
- Put the wafer in a beaker of clean isopropanol for 5 min.
- Rinse till 5 MΩ
- Dry using manual spinner and **Cu chuck.**

6. CNT growth @ Class 10000

Use the AIXTRON BlackMagic Pro to grow CNTs using LPCVD at a temperature of 650°C. Use recipe: lpcvd_subref_waittemp_zrn and change deposition parameters as required.

Use contaminated reactor interior!

7. SEM analysis @ Class 100

Use multiwafer holder.

APPENDIX D.2
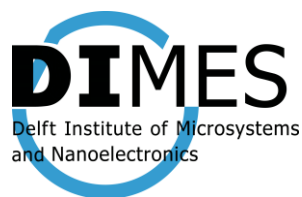
EC1880

FLOWCHART

10 double sided polished wafers
TSV with CNT

Sten Vollebregt (TFT Group)

VALID FROM: 11/2013

DIMES - DELFT UNIVERSITY OF TECHNOLOGY

Address   :   Feldmannweg 17, 2628 CT Delft, The Netherlands

P.O. Box :   5053, 2600 GB Delft, The Netherlands

Phone   :   +31 - (0)15 - 2783868

Fax   :   +31 - (0)15 - 2622163

Website :   www.dimes.tudelft.nl

GENERAL REMARKS

1. Always handle wafers with care during processing, and wear cleanroom gloves. Work as clean as possible.

2. Always check equipment and process conditions before starting a process.

   In case of problems with equipment operation or contamination, directly notify the responsible person(s) **and other users**. Do not try to repair or clean unknown equipment yourself, and never try to refresh a contaminated etch or cleaning bath!

3. Always clean wafers after several hours of storage before performing a coating, a furnace or a deposition step. After a furnace step the wafers do not have to be cleaned again if the next process step is carried out immediately.

   Use the correct procedure for cleaning:

- Acetone or Tepla stripper	for photoresist removal
- HNO3 100%	for wafers which are not contaminated with a metal layer
- HNO3 100% metaal	for wafers which are or have been in contact with a metal
- HNO3 100% and HNO3 65%	for all wafers without metal

   Note: The mentioned cleaning procedures may only be applied in the Class 100 cleanroom for uncontaminated silicon wafers. Wafers which are contaminated and wafers made from other materials than silicon are subject to PAC rules, and may have to be cleaned elsewhere!

4. Wafers that are contaminated may never be processed in any of the equipment without permission of the PAC committee. Special precautions may need to be applied, like the use of a special substrate holder.

   Wafers that are covered with a resist or a metal layer may never be processed in a furnace. Only alloying is allowed for wafers with an aluminum layer.

5. Layer thickness measurements may be performed on the process wafers using the Leitz MPV-SP or Woollam equipment. If this is not possible, or when sheet resistance and/or junction depth measurements must be performed, a test wafer must be processed with the process wafers.

6. The use of "non-standard" materials for processing in the class 100 cleanroom and SAL must always be evaluated and approved by the PAC. It is strictly forbidden to use these materials without permission.

   All substrates, layers and chemicals which are not standard being used in the Dimes 01/02/03 or Dimos 01 production processes are considered to be "non-standard" materials, and possibly contaminating. See the PAC rules & Instructions (available on the internet) for more details.

STARTING MATERIAL

Use **6 double side polished test wafers of 300 μm and 4 double sides polished wafers of 500 μm**

Wafers taken out of an already opened box must be cleaned before processing, according to the standard procedure.
Wafers taken out of an unopened wafer box do not have to be cleaned before processing**.**

Notes:
- **Fe is passivated in pure HNO_3 but etches in diluted HNO_3**
- **Fe will remain on the bottom of the holes during carbon nanotube (CNT) growth (base growth)**
- **After second Ti deposition the Fe and CNT containing measurement structures will be closed off. However, some large area (for Raman and TEM analysis) will NOT be covered. Care should be taken when etching the second Ti layer, as in that case these areas are NOT covered by photoresist. When etching the contact holes they WILL be covered by photoresist.**
- **CNTs can be damaged by oxygen containing plasma, but are resilient against most etching solutions like HNO_3 and HF.**

This flowcharts is divided in three parts:
1. Creation of TS holes in a double sided polished Si wafer
2. Deposition of metal layers and catalyst on second wafer, deposition will be done in trenches to allow oxide-oxide bonding
3. Bonding of two wafers, CNT growth and creation of bonding pads.

PART 0: All wafers alignment markers

8. COATING AND BAKING

Use the EVG 120 wafertrack to coat the wafers with resist, and follow the instructions specified for this equipment.
The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas,
spin coating with Shipley SPR3012 positive photoresist, and a soft bake at 95degC for 90 seconds.
Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

Use coating **Co – Zero Layer** (resist thickness: 1.400 μm).

9. ALIGNMENT AND EXPOSURE

Processing will be performed on the ASM PAS 5500/80 automatic waferstepper.

Follow the operating instructions from the manual when using this machine.

Use **COMURK mask**, the correct litho job:
ZEFWAM: all wafers
And the correct exposure energy (140 mJ/cm^2).

10. DEVELOPMENT

Use the EVG 120 wafertrack to develop the wafers, and follow the instructions specified for this equipment.
The process consists of a post-exposure bake at 115 degC for 90 seconds, followed by a development step using
Shipley MF322 developer (single puddle process), and a hard bake at 100 degC for 90 seconds.
Always check the temperature of the hotplates first.

Use development **program Dev - Single Puddle**.

11. INSPECTION: LINEWIDTH

Visually inspect the wafers through a microscope, and check the linewidth. No resist residues are allowed.

12. PLASMA ETCHING OF ALIGNMENT MARKS

Use the Trikon Ωmega 201 plasma etcher.
Follow the operating instructions from the manual when using this machine.
The process conditions of the etch program may not be changed !

Use sequence **URK_NPD a**nd set the platen temperature to **20 °C** to etch 1200 Å deep ASM URK's into the silicon.

13. CLEANING PROCEDURE: TEPLA + HNO$_3$ 100% and 65%

Plasma strip   Use the Tepla plasma system to remove the photoresist in an oxygen plasma.
 Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
 Use program 1

Cleaning   10 minutes in fuming nitric acid (Merck: HNO$_3$ 100% selectipur) at ambient temperature.
Use wet bench "HNO$_3$ (100%)" and the carrier with the red dot.

QDR   Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Cleaning   10 minutes in concentrated nitric acid (Merck: HNO$_3$ 65% selectipur) at 110 °C.
Use wet bench "HNO$_3$ (65%)" and the carrier with the red dot.

QDR   Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Drying   Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a red dot.

14. COATING AND BAKING

Use the EVG 120 wafertrack to coat the wafers with resist, and follow the instructions specified for this equipment.
The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas,
spin coating with Shipley SPR3012 positive photoresist, and a soft bake at 95degC for 90 seconds.
Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

Use coating **Co – Zero Layer** (resist thickness: 1.400 μm).

Backside for top wafers

15. ALIGNMENT AND EXPOSURE

Processing will be performed on the ASM PAS 5500/80 automatic waferstepper.

Follow the operating instructions from the manual when using this machine.

Use **COMURK mask**, the correct litho job:
Zeaml-up front to back: for top wafers (300 μm)
Zeaml-down: for bottom wafers (500 μm)
And the correct exposure energy (140 mJ/cm^2).

16. DEVELOPMENT

Use the EVG 120 wafertrack to develop the wafers, and follow the instructions specified for this equipment.
The process consists of a post-exposure bake at 115 degC for 90 seconds, followed by a development step using
Shipley MF322 developer (single puddle process), and a hard bake at 100 degC for 90 seconds.
Always check the temperature of the hotplates first.

Use development **program Dev - Single Puddle**.

Backside for top wafers

17. INSPECTION: LINEWIDTH

Visually inspect the wafers through a microscope, and check the linewidth. No resist residues are allowed.

Backside for top wafers

18. PLASMA ETCHING OF ALIGNMENT MARKS

Use the Trikon Ωmega 201 plasma etcher.
Follow the operating instructions from the manual when using this machine.
The process conditions of the etch program may not be changed !

Use sequence **LEON1 3 min** and set the platen temperature to **20 °C** to etch ~6000 Å deep holes into the silicon.

Backside for top wafers

19. CLEANING PROCEDURE: TEPLA + HNO$_3$ 100% and 65%

Plasma strip   Use the Tepla plasma system to remove the photoresist in an oxygen plasma.
                 Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
                 Use program 1

Cleaning	10 minutes in fuming nitric acid (Merck: HNO_3 100% selectipur) at ambient temperature. Use wet bench "HNO_3 (100%)" and the carrier with the red dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Cleaning	10 minutes in concentrated nitric acid (Merck: HNO_3 65% selectipur) at 110 °C. Use wet bench "HNO_3 (65%)" and the carrier with the red dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a red dot.

PART 1: TS etching of double sided wafers

20. BACKSIDE OXIDE DEPOSITION @ Class 100

Use the Novellus to deposit 5 μm of PECVD oxide on the **backside** of the wafer.

21. OXIDE DEPOSITION @ Class 100

Use the Novellus to deposit 6 μm of PECVD oxide on the frontside of the wafer.

22. COATING AND BAKING

Use the EVG 120 wafertrack to coat the wafers with resist, and follow the instructions specified for this equipment.
The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas,
spin coating with Shipley SPR3012 positive photoresist, and a soft bake at 95degC for 90 seconds.
Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

Use coating **Co – SPR3017M – 3000nm** (resist thickness: 3.000 μm).

23. ALIGNMENT AND EXPOSURE

Processing will be performed on the PAS5500/80
Follow the operating instructions from the manual when using this machine.

Mask: TSV, job g10ab-1 id=2, energy = 650 mJ/cm^2 (only A-dies)

24. DEVELOPMENT

Use the EVG 120 wafertrack to develop the wafers, and follow the instructions specified for this equipment.
The process consists of a post-exposure bake at 115 degC for 90 seconds, followed by a development step using
Shipley MF322 developer (double puddle process), and a hard bake at 100 degC for 90 seconds.
Always check the temperature of the hotplates first.

Use development **program Dev – SP**.

25. INSPECTION

Visually inspect the wafers through a microscope, and check openings and overlay.

26. PLASMA ETCHING OF 6000 nm OXIDE

Use the Drytek 384T plasma etcher.
Follow the operating instructions from the manual when using this machine.
The process conditions of the etch program may not be changed!

Use program StdOxide (8-10 nm/s) and change time to t=700 s.

27. DRIE ETCHING OF 300 μm Si (TS)

Use the Adixen DRIE plasma etcher.
Follow the operating instructions from the manual when using this machine.
The process conditions of the etch program may not be changed!

Use program INNOVIA8, for 2h30 or 3h (to open 30 μm holes)

28. CLEANING PROCEDURE: HNO$_3$ 100% and 65%

Plasma strip   Use the Tepla plasma system to remove the photoresist in an oxygen plasma.
                 Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
                 Use program 3

Cleaning	10 minutes in fuming nitric acid (Merck: HNO_3 100% selectipur) at ambient temperature. Use wet bench "HNO_3 (100%)" and the carrier with the red dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Cleaning	10 minutes in concentrated nitric acid (Merck: HNO_3 65% selectipur) at 110 °C. Use wet bench "HNO_3 (65%)" and the carrier with the red dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a red dot.

29. WET ETCHING OF OXIDE

Use BHF (1:7) to remove the oxide masks. Etch till front and backside are hydrophobic

30. WET OXIDATION: 700 NM @ Class 100

Use furnace D1 to grow 700 nm of wet thermal oxide. Use recipe WTOX1000 with an oxidation time of 2h30 minutes.

The oxide will passivate the TS holes.

31. BACKSIDE THIN DOWN OF OXIDE @ Class 100

Use the Alcatel GIR300 to thin the oxide at the backside of the wafer down to about 100 nm (600 nm should be etched)

PART 2: preparation of catalyst wafers

32. COATING AND BAKING

Use the EVG 120 wafertrack to coat the wafers with resist, and follow the instructions specified for this equipment.
The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas,
spin coating with Shipley SPR3012 positive photoresist, and a soft bake at 95degC for 90 seconds.
Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

Use coating **Co – SPR3012 – 1400nm – no EBR** (resist thickness: 1.400 μm).

33. ALIGNMENT AND EXPOSURE

Processing will be performed on the ASM PAS 5500/80 automatic waferstepper.

Follow the operating instructions from the manual when using this machine.

Use **Open10x10 mask**, the correct litho job g10ab id = 2 and the correct exposure energy (140 mJ/cm^2).

34. DEVELOPMENT

Use the EVG 120 wafertrack to develop the wafers, and follow the instructions specified for this equipment.
The process consists of a post-exposure bake at 115 degC for 90 seconds, followed by a development step using
Shipley MF322 developer (double puddle process), and a hard bake at 100 degC for 90 seconds.
Always check the temperature of the hotplates first.

Use development **program Dev – Single Puddle**.

35. INSPECTION

Visually inspect the wafers through a microscope, and check openings and overlay.

36. PLASMA ETCHING OF TRENCHES

Use the Trikon Ωmega 201 plasma etcher.
Follow the operating instructions from the manual when using this machine.
The process conditions of the etch program may not be changed !

Use sequence **URK_NPD** and set the platen temperature to **20 °C** to etch minimum 120 nm deep trench into the silicon.

37. ZrN METALLIZATION @ Class 100

Use the TRIKON SIGMA sputter coater for the deposition of the ZrN metal layer on the process wafers.
Follow the operating instructions from the manual when using this machine.

Use recipe ZrN_30nm_350 to reactively sputter a 0.030 μm thick layer of ZrN (to prevent oxidation of Ti). Add dummy
wafers inbetween as required. Temperature = 350 °C

Visual inspection: the metal layer must look shiny.

38. COATING AND BAKING @ Class 100

Use the **EVG-120** automatic wafertrack to coat the wafers with 1.4 μm resist.
The process includes a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating for 30s
with Shipley SPR 3012 and prebaking for 90 seconds at 95 °C.
Follow the instructions specified for this equipment, and always check the temperature of the hotplate first.

Use program: **Co – SPR3012 -1400 nm** (resist thickness: 1.400 μm at 48% RV).

39. ALIGNMENT AND EXPOSURE @ Class 100

Processing will be performed on the ASM PAS 5500/80 automatic waferstepper.

Follow the operating instructions from the manual when using this machine.

Use **Open10x10 mask**, the correct litho job g10ab id = 3,and g10a-edge(full) id = 2 the correct exposure energy (140 mJ/cm^2). Perform a 10 micron shift and do 4 exposures (10,10; 10,-10; -10,-10; -10,10)

40. DEVELOPMENT @ Class 100

Development step on the EVG-120 using Shipley MF322 developer (double puddle process), and a hard bake at 100 °C for 90 seconds. Follow the instructions specified for this equipment, and always check the temperature of the hotplates first.

Use program: Dev – Single Puddle

41. INSPECTION

Visually inspect the wafers through a microscope, and check openings and overlay.

42. WET ETCH ZrN from B dies and edge

Remove the ZrN by etching for 1 minute in 0.55% HF (METAL).

43. NMP RESIST STRIPPING @ SAL
Remove the resist by submerging the wafers in NMP at 70 °C for several minutes. Use Class 100 glassware. No plasma stripping can be used as it might damage the ZrN layer. Rinse and dry using single wafer dryer.

44. COATING AND BAKING @ Class 100

Use the **EVG-120** automatic wafertrack to coat the wafers with 1.4 μm resist.
The process includes a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating for 30s with Shipley SPR 3012 and prebaking for 90 seconds at 95 °C.
Follow the instructions specified for this equipment, and always check the temperature of the hotplate first.

Use program: **Co – SPR3012 -1400 nm – no EBR** (resist thickness: 1.400 μm at 48% RV).

45. ALIGNMENT AND EXPOSURE @ Class 100

Processing will be performed on the ASM PAS 5500/80 automatic waferstepper.

Follow the operating instructions from the manual when using this machine.

Use **TSV mask**, the correct litho job g10ab id = 2, the correct exposure energy (140 mJ/cm^2). Oversize the masks by performing shifted depositions or using the oversize option.

46. DEVELOPMENT @ Class 100

Development step on the EVG-120 using Shipley MF322 developer (double puddle process), and a hard bake at 100 °C for 90 seconds. Follow the instructions specified for this equipment, and always check the temperature of the hotplates first.

Use program: Dev – Single Puddle

<u>**Use white box with Fe written on it**</u>

47. Fe CATALYST DEPOSITION @ Class 10000

Use the CHA Solution e-beam evaporator to deposit 0.8 nm Fe directly on the ZrN surface.

48. Lift-off @ SALAB

Perform lift-off procedure with NMP solvent in beaker on hotplate with stirrer at 70 °C and 250 rpm. **Use dedicated beaker from Cu corner**

49. RINSE & DRY @ SALAB

Rinse the wafers in DI and dry using manual dryer **with special Cu chuck**

50. INSPECTION @ SALAB

Visually inspect the wafers through a microscope, check if catalyst layer remained on surface. Put paper under wafer and throw away paper after use.

PART 3: Bonding, CNT growth and pad formation

51. WET ETCHING OF OXIDE of 300 μm wafer

Use BHF (1:7) for Si bath to remove the oxide from the backside of the double sided wafers. Etch till back side is hydrophobic.

52. RCA CLEAN of 300 μm wafer

Clean   Rinse the quartz RCA1 beaker with DI water and place it on a hot plate.
Rinse the thermocouple connected to the temperature controller with DI water and place it in the RCA1 beaker.
Slowly pour the measured amount of chemicals into the beaker:
-      2500 ml DI water
-      500 ml NH_4OH
-      Use the 1000ml and 500ml graduated cylinders

Make sure that the mouth of the bottle doesn't make contact with the graduated cylinder in order to prevent contamination. Never pour back chemicals into the bottle!!!
Clean the graduated cylinder with water.
Turn the temperature controller on the hot plate and set the temperature to 75 C.
When the temperature reaches 65 C, add 500ml of H_2O_2.
In the meantime put the wafers in the proper carrier (green/blue dots).
When the temperature reaches 72 C, dip the carrier with the wafers into the beaker, but don't start the timer yet.
Once it reaches 75 C, start the 10 minutes countdown. When the 10 minutes are done, turn off the hot plate and transfer the wafers to the DI water container and start rinsing.

Rinse   Rinse in the water bath for 5 minutes and in the meantime start the demi water for the Maragoni dryer. After 3 minutes, turn on the IPA in the Maragoni bath.

Dry   Carefully place the wafers in the maragoni wafer holders and then dip them into the solution for 40 seconds. After that, start taking them out of the bath and because of the IPA they'll come out dry.

53. WAFER BONDING @ Class 100

Bond the wafers using the ALM wafer bonding tool in the yellow room. Bonding conditions: Si-Si bonding 300 °C
Use contaminated wafer chuck

54. INSPECTION @ Class 100

After the process is finished, take out the bonded wafers and inspect the alignment. Make sure the patterns are properly aligned and **make sure there are no voids inside** the bonded pair.

Make sacrificial dummy wafer for inspection setup to prevent contamination.

55. CNT growth @ Class 10000

Use the AIXTRON BlackMagic Pro to grow CNTs using LPCVD at 650°C for Fe catalyst layers. Use recipe: lpcvd_subref_waittemp_zrn
Sacrifice one wafer to determine growth rate for measurement wafers.

56. Ti and Al METALLIZATION @ Class 100

Use the TRIKON SIGMA sputter coater for the deposition of the Ti metal layer on the process wafers.
The target must exist of 100% Ti.
Follow the operating instructions from the manual when using this machine. **Use a dedicated Fe transport wafer to prevent contamination! Use cassette from Novellus with wide slots.**

Use recipe 'Ti100 + 3um Al LP RT' to sputter 100 nm Ti, followed by 3 μm Al at 25 °C.

Visual inspection: the metal layer must look shiny.

57. MANUAL COATING @ Class 100

Manually coat the wafers with 1.4 μm SPR3012. First perform a 10 min HMDS treatment (using the Pt holder), followed by spinning using appropriate program on the Cu chuck. Perform a soft bake at 95 °C on a dedicated dummy wafer.

58. ALIGNMENT AND EXPOSURE @ Class 100

Processing will be performed on the EVG 420 contact aligner **using the Cu chuck!**
Follow the operating instructions from the manual when using this machine.

Mask Metal1, exposure time 8 sec.

59. WET ETCH Al and Ti @ MEMS Lab

Remove the Al layer using PES 77-19-04 (20-25 min.), rinse the wafers and remove the Ti layer using 0,55 % HF (1 min.). Rinse wafers for 5 min., and dry using single wafer dryer.

60. PHOTORESIST REMOVAL @ MEMS Lab

Acetone   Dissolve the photoresist in acetone and let them dry in the air.

61. CLEANING PROCEDURE: HNO3 100% metal @ MEMS Lab
Cleaning   10 minutes in fuming nitric acid (Merck: HNO3 100% selectipur) at ambient temperature.
<u>Make sure to take fresh solution in your own small container with single wafer holder.</u>
Rinse   Manually for a few minutes until 5 MΩ
Drying   Use single wafer dryer

Appendix E

Matlab codes

Appendix E.1

%%% GENERATION OF DOE-RSM EXPERIMENTAL TABLES %%%

```matlab
clc; close all; clear all
n = 8;                              % Number of parameters in the experiment

% Central composite design
name  = 'Type';                     % Type of CCD used
value = 'Circumscribed';            % Location of center points
d_CC  = ccdesign(n,name,value);     % CCD table
size(d_CC)

% Box-Behnken design
name  = 'Center';                   % Type of BBD used
value = 8;                          % Number of center points
d_BB  = bbdesign(n,name,value)      % BBD table
size(d_BB)

% D-optimal design
nruns = 3;                          % Number of desired runs
Model = 'Interaction';             % linear regression model
d_D =   rowexch(n,nruns,Model)      % D-optimal table
```

Appendix E.2

```matlab
%%% MAIN EFFECTS PLOT GENERATOR %%%

clc; clear all; close all

% The SNR values of results
SNR = [];

% Calculating the Main effects SNR values
% A, B, ... H are the 8 parameters. 1, 2, 3 are the parameter levels.
A1 = (SNR(1)+SNR(2)+SNR(3)+SNR(4)+SNR(5)+SNR(6)+SNR(7)+SNR(8)+SNR(9))/9;
A2 = (SNR(10)+SNR(11)+SNR(12)+SNR(13)+SNR(14)+SNR(15)+SNR(16)+
      SNR(17)+SNR(18))/9;

B1 = (SNR(1)+SNR(2)+SNR(3)+SNR(10)+SNR(11)+SNR(12))/6;
B2 = (SNR(4)+SNR(5)+SNR(6)+SNR(13)+SNR(14)+SNR(15))/6;
B3 = (SNR(7)+SNR(8)+SNR(9)+SNR(16)+SNR(17)+SNR(18))/6;

C1 = (SNR(1)+SNR(4)+SNR(7)+SNR(10)+SNR(13)+SNR(16))/6;
C2 = (SNR(2)+SNR(5)+SNR(8)+SNR(11)+SNR(14)+SNR(17))/6;
```

```
C3 = (SNR(3)+SNR(6)+SNR(9)+SNR(12)+SNR(15)+SNR(18))/6;

D1 = (SNR(1)+SNR(4)+SNR(9)+SNR(11)+SNR(15)+SNR(17))/6;
D2 = (SNR(2)+SNR(5)+SNR(7)+SNR(12)+SNR(13)+SNR(18))/6;
D3 = (SNR(3)+SNR(6)+SNR(10)+SNR(8)+SNR(14)+SNR(16))/6;

E1 = (SNR(1)+SNR(6)+SNR(7)+SNR(11)+SNR(14)+SNR(18))/6;
E2 = (SNR(2)+SNR(4)+SNR(8)+SNR(12)+SNR(15)+SNR(16))/6;
E3 = (SNR(3)+SNR(5)+SNR(9)+SNR(10)+SNR(13)+SNR(17))/6;

F1 = (SNR(1)+SNR(6)+SNR(8)+SNR(12)+SNR(13)+SNR(17))/6;
F2 = (SNR(2)+SNR(4)+SNR(9)+SNR(10)+SNR(14)+SNR(18))/6;
F3 = (SNR(3)+SNR(5)+SNR(7)+SNR(11)+SNR(15)+SNR(16))/6;

G1 = (SNR(1)+SNR(5)+SNR(9)+SNR(12)+SNR(14)+SNR(16))/6;
G2 = (SNR(2)+SNR(6)+SNR(7)+SNR(10)+SNR(15)+SNR(17))/6;
G3 = (SNR(3)+SNR(4)+SNR(8)+SNR(11)+SNR(13)+SNR(18))/6;

H1 = (SNR(1)+SNR(5)+SNR(8)+SNR(10)+SNR(15)+SNR(18))/6;
H2 = (SNR(2)+SNR(6)+SNR(9)+SNR(11)+SNR(13)+SNR(16))/6;
H3 = (SNR(3)+SNR(4)+SNR(7)+SNR(12)+SNR(14)+SNR(17))/6;

% Plotting of Main effects graphs
Ax = [1 2];        Ay = [A1 A2];      [Amax,AImax] = max(Ay');
subplot (2,4,1);  plot(Ax,(Ay)',':.',AImax,Amax,'r*');
title('ZrN thickness');

Bx = [1 2 3];      By = [B1 B2 B3];  [Bmax,BImax] = max(By');
subplot (2,4,2);  plot(Bx,(By)',':.',BImax,Bmax,'r*');
title('Fe thickness');

Cx = [1 2 3];      Cy = [C1 C2 C3];  [Cmax,CImax] = max(Cy');
subplot (2,4,3);  plot(Cx,(Cy)',':.',CImax,Cmax,'r*');
title('Anneal temperature');

Dx = [1 2 3];      Dy = [D1 D2 D3];  [Dmax,DImax] = max(Dy');
subplot (2,4,4);  plot(Dx,(Dy)',':.',DImax,Dmax,'r*');
title('Anneal time');

Ex = [1 2 3];      Ey = [E1 E2 E3]   [Emax,EImax] = max(Ey');
subplot (2,4,5);  plot(Ex,(Ey)',':.',EImax,Emax,'r*');
title('Growth temperature');

Fx = [1 2 3];      Fy = [F1 F2 F3];  [Fmax,FImax] = max(Fy');
subplot (2,4,6);  plot(Fx,(Fy)',':.',FImax,Fmax,'r*');
title('Growth pressure');

Gx = [1 2 3];      Gy = [G1 G2 G3];  [Gmax,GImax] = max(Gy');
subplot (2,4,7);  plot(Gx,(Gy)',':.',GImax,Gmax,'r*');
title('H_2 flow / C_2H_2 flow');

Hx = [1 2 3];      Hy = [H1 H2 H3];  [Hmax,HImax] = max(Hy');
subplot (2,4,8);  plot(Hx,(Hy)',':.',HImax,Hmax,'r*');
title('C_2H_2 flow');
```

Appendix E.3

```
%%% CURVE FITTING OF RAMAN SPECTRUM %%%
%Uses a 8 Lorentzian fit combined with a Gaussian for D'

clear all

%[filename, filedirectory]  = uigetfile ('*.txt', 'Select Raman data:');
%file = strcat(filedirectory,filename);
files = dir('*.txt');

mkdir results;

storename = input('In which file do you want to store the fitting parameters?
[fitresults.txt]: ', 's');
if isempty(storename)
    storename = 'fitresults.txt';
end

cd results;
message = 'Fit of Raman spectrum with poly-4 baseline removal using 8
Lorentzians and 1 Gaussian curves for Dprime';
dlmwrite(storename, message, 'delimiter', '', 'newline', 'pc');
cd ..;

skipall = input('Do you want to automatically accept all fitting results? y/n
[n]: ', 's');
if isempty(skipall)
    skipall = 'n';
end

for i = 1:length(files)
    %Retreive data
    filename = files(i).name;
    DATA = dlmread(filename, '\t');
    freq = DATA(:,1);
    spec = DATA(:,2);

    % --- Create fit "baseline"

    % Apply exclusion rule "spectrum si and notch v2"
    if length(freq)~=4258
        error('Exclusion rule ''%s'' is incompatible with ''%s''.','spectrum
si and notch v2','freq');
    end
    ex2_ = true(length(freq),1);
    ex2_([(1:487) (1906:2577) (3468:3850) (3885:4212)]) = 0;
    fo2_ =
fitoptions('method','LinearLeastSquares','Normalize','on','Robust','On');
    ok2_ = isfinite(freq) & isfinite(spec);
    if ~all( ok2_ )
        warning( 'GenerateMFile:IgnoringNansAndInfs', ...
            'Ignoring NaNs and Infs in data' );
    end
    set(fo2_,'Exclude',ex2_(ok2_));
```

```matlab
    ft2_ = fittype('poly4');

    % Fit this model using new data
    if sum(~ex2_(ok2_))<2  %% too many points excluded
        error('Not enough data left to fit ''%s'' after applying exclusion
rule ''%s''.','fit 1','spectrum si and notch v2')
    else
        cf2_ = fit(freq(ok2_),spec(ok2_),ft2_,fo2_);
    end

    %Now generate and substract the obtained linear baseline
    baseline = feval(cf2_,freq);
    rm_spec = spec - baseline;

    %Normalize spectrum to G-peak
    f_1500 = find(freq > 1499 & freq < 1501);
    f_1800 = find(freq > 1799 & freq < 1801);
    [g_mag,g_index] = max(rm_spec(f_1800:f_1500));

    clean_spec = rm_spec./g_mag;

    %Start generated fit script
    f_ = clf;
    figure(f_);
    %set(f_,'Units','Pixels','Position',[467 144 688 483]);
    legh_ = []; legt_ = {};   % handles and text for legend
    xlim_ = [Inf -Inf];       % limits of x axis
    ax_ = axes;
    set(ax_,'Units','normalized','OuterPosition',[0 0 1 1]);
    set(ax_,'Box','on');
    grid(ax_,'on');
    axes(ax_); hold on;

    % --- Plot data originally in dataset "norm_spec vs. freq"
    freq = freq(:);
    clean_spec = clean_spec(:);
    h_ = line(freq,clean_spec,'Parent',ax_,'Color',[0.333333 0 0.666667],...
        'LineStyle','none', 'LineWidth',1,...
        'Marker','.', 'MarkerSize',12);
    xlim_(1) = min(xlim_(1),min(freq));
    xlim_(2) = max(xlim_(2),max(freq));
    legh_(end+1) = h_;
    legt_{end+1} = 'clean_spec vs. freq';

    % Nudge axis limits beyond data limits
    if all(isfinite(xlim_))
        xlim_ = xlim_ + [-1 1] * 0.01 * diff(xlim_);
        set(ax_,'XLim',xlim_)
    else
        set(ax_, 'XLim',[66.338840000000005, 3635.8451599999999]);
    end

    % Fit spectrum"
    fo_ =
      fitoptions('method','NonlinearLeastSquares','MaxFunEvals',1000,'Lower',
```

```
   [0     0     0     0     0     0     0     0     0    0 1100 1300 1400 1579
   1610 2400 2600 2900 3100 3200    0.1    0.1    0.1    0.1    0.1    0.1
   0.1    0.1    0.1    0.1],'Upper',[Inf  Inf  Inf  Inf  Inf  Inf  Inf
   Inf   Inf   Inf 1200 1400 1550 1585 1630 2500 2750 3000 3200 3300  Inf
   Inf  Inf  Inf  Inf  Inf  Inf  Inf  Inf  Inf]);
 ok_ = isfinite(freq) & isfinite(clean_spec);
if ~all( ok_ )
    warning( 'GenerateMFile:IgnoringNansAndInfs', ...
        'Ignoring NaNs and Infs in data' );
end
st_ = [0.1 1 0.1 1 0.1 0.1 1 0.1 0.1 0.1 1150 1335 1450 1582 1618 2450
        2650 2930 3170 3230 10 10 10 10 10 10 10 10 10 10];
set(fo_,'Startpoint',st_);
ft_ = fittype('a1/(1+((x-b1)/(c1/2))^2) + a2/(1+((x-b2)/(c2/2))^2) +
              a3/(1+((x-b3)/(c3/2))^2) + a4/(1+((x-b4)/(c4/2))^2) +
              a5*exp(-(x-b5)^2/(2*(c5/(2*sqrt(2*log(2))))^2)) +
              a6/(1+((x-b6)/(c6/2))^2) + a7/(1+((x-b7)/(c7/2))^2) +
              a8/(1+((x-b8)/(c8/2))^2)  + a9/(1+((x-b9)/(c9/2))^2) +
              a10*exp(-(x-b10)^2/(2*(c10/(2*sqrt(2*log(2))))^2))',...
              'dependent',{'y'},'independent',{'x'},...
              'coefficients',{'a1', 'a2', 'a3', 'a4', 'a5', 'a6', 'a7',
              'a8', 'a9', 'a10', 'b1', 'b2', 'b3', 'b4', 'b5', 'b6',
              'b7', 'b8', 'b9', 'b10', 'c1', 'c2', 'c3', 'c4', 'c5',
              'c6', 'c7', 'c8', 'c9', 'c10'});

% Fit this model using new data
[cf_, quality] = fit(freq(ok_),clean_spec(ok_),ft_,fo_);

% Plot this fit
h_ = plot(cf_,'fit',0.95);
legend off;  % turn off legend from plot method call
set(h_(1),'Color',[1 0 0],...
    'LineStyle','-', 'LineWidth',2,...
    'Marker','none', 'MarkerSize',6);
legh_(end+1) = h_(1);
legt_{end+1} = 'fit 1';

% Plot fits
coeff = coeffvalues(cf_);

f_1200  = coeff(1)./(1+((freq-coeff(11))./(coeff(21)/2)).^2);
f_dlor  = coeff(2)./(1+((freq-coeff(12))./(coeff(22)/2)).^2);
f_1500  = coeff(3)./(1+((freq-coeff(13))./(coeff(23)/2)).^2);
f_g     = coeff(4)./(1+((freq-coeff(14))./(coeff(24)/2)).^2);
f_dpgauss = coeff(5)*exp(-(freq-
        coeff(15)).^2./(2*(coeff(25)./(2*sqrt(2*log(2)))).^2));
f_2450  = coeff(6)./(1+((freq-coeff(16))./(coeff(26)/2)).^2);
f_gp    = coeff(7)./(1+((freq-coeff(17))./(coeff(27)/2)).^2);
f_2950  = coeff(8)./(1+((freq-coeff(18))./(coeff(28)/2)).^2);
f_3200  = coeff(9)./(1+((freq-coeff(19))./(coeff(29)/2)).^2);
f_3240  = coeff(10)*exp(-(freq-
        coeff(20)).^2./(2*(coeff(30)./(2*sqrt(2*log(2)))).^2));

plot(freq, f_1200, 'g', freq, f_dlor, 'g', freq, f_1500, 'g', freq, f_g,
    'g', freq, f_dpgauss, 'g', freq, f_2450, 'g', freq, f_gp, 'g', freq,
    f_2950, 'g', freq, f_3200, 'g', freq, f_3240, 'g');
```

```matlab
    % Done plotting data and fits.  Now finish up loose ends.
    hold off;
    leginfo_ = {'Orientation', 'vertical', 'Location', 'NorthEast'};
    h_ = legend(ax_,legh_,legt_,leginfo_{:});  % create legend
    set(h_,'Interpreter','none');
    xlabel(ax_,'');                    % remove x label
    ylabel(ax_,'');                    % remove y label


    %Display quality of fit
    disp(quality);


    %If desired ask user to accept fit
    if skipall == 'n'
        reply = input('Do you accept the fit? y/n [y]: ', 's');
        if isempty(reply)
            reply = 'y';
        end
    else
        reply = 'y';
    end


    if reply == 'y'
        %Retreive the fitting parameters and write out data
        coefficients = coeffvalues(cf_);
        fit_par = [coefficients(1,1:10)' coefficients(1,11:20)'
coefficients(1,21:30)'];

        cd results;
        samplename = strrep(filename, '.txt', '');
        dlmwrite(storename, samplename, '-append', 'roffset', 1, 'delimiter',
'', 'newline', 'pc');
        dlmwrite(storename, fit_par, '-append', 'delimiter', '\t',
'precision', 6, 'newline', 'pc');

        writename = strrep(filename, '.txt', '-fit.txt');
        dlmwrite(writename, fit_par, 'delimiter', '\t', 'precision', 6,
'newline', 'pc');

        writename2 = strrep(filename, '.txt', '-norm.txt');
        dlmwrite(writename2, [freq clean_spec], 'delimiter', '\t',
'precision', 6, 'newline', 'pc');
        cd ..;
    end
end
```

Appendix E.4

```
%%% CALCULATION OF R_SWNT, R_MWNT, R_VIA AND RHO %%%

clc; close all; clear all

% CNT physical parameters
l_ballistic = [];        % Ballistic length (um)
d_sw        = [];        % SWNT diameter (um)
d_in        = [];        % MWNT inner diameter (um)
d_out       = [];        % MWNT outer diameter (um)
D           = [];        % Growth density (cm^-2)
s           = [];        % Tube spacing (um)
P           = [];        % Proportion of MWNT to SWNT


% CNT electrical constants
Rc          = 0;                 % Contact resistance (ohm)
Rq          = 6.45*1000;         % Quantum resistance (ohm)
I0          = 25*(10^-6);        % Constant (ampere)
V           = 2.5;               % Applied bias (volt)
delta       = 0.34*(10^-3);      % Separation between adjacent walls (um)
A           = 1;                 % Side of square via (um)
a1          = 140;               % Fitting constant1 (/um)
b1          = 0.2;               % Fitting constant2 (dim less)


% The analysis below is carried out for each of the nine growth samples
for expt = 1:9;

    % Calculating the total number of channels in MWNT
    if d_out < 6*(10^-3)
      N_chan = (2/3)*(1+(d_out - d_in)/(2*delta));
    else
      N_chan = (1+(d_out - d_in)/(2*delta))*((a1/2)*(d_out+d_in)+b1);
    end

    % Calculating the resistance of a SWNT and a MWNT, of 100 um length
    for L  = 1:100;                              % Length of CNT (um)

      R_SWNT = Rc + Rq*(1+(L/l_ballistic)) + (V/I0);  % Resistance of a SWNT
      R_MWNT = Rq*(1 + L/l_ballistic)/N_chan;         % Resistance of a MWNT

      % Calculating the number of SWNT and MWNT in a face of the via
      Da = A*(10^-4)*(D^0.5); % #tubes in a um length
      n  = Da/(1+P);          % No. of SWNT in the via
      n  = n/3;               % 1/3 of SWNT will be metallic
      m  = Da/(1+(1/P));      % No. of MWNT in the via

      % Calculating the number of SWNT and MWNT in the complete via
      if    n < m
            N = (n^2);
            M = (m^2)+(2*m*n);
      elseif n = m
            N = 2*(n^2);
            M = 2*(m^2);
      else
```

```
            N = (n^2)+(2*m*n);
            M = (m^2);
     % Calculating the bulk resistance of the via
     RN          = R_SWNT/N;        % Resistance of all SWNT
     RM          = R_MWNT/M;        % Resistance of all MWNT
     R_via(L)    = (RN*RM)/(RM+RN);  % Total resistance of SWNT and MWNT
    end
    % Calculating the value of k and rho by linear fitting of the R_via(L)
      function
    Lx                  = 1:100;
    R_via_fit           = polyfit(Lx,R_via,1);
    R_via_fit1(expt,:)  = R_via_fit;
end
k   = R_via_fit1(:,1);         % Resistance per unit length of as-grown CNT via
Rho = R_via_fit1(:,1)*(A^2);   % Resistivity of as-grown CNT via
```

References

[1]   M. T. Bohr, "Interconnect scaling-the real limiter to high performance ULSI," in *International Electron Devices Meeting*, 1995, pp. 241-244.

[2]   J. D. Meindl, "Beyond Moore's Law: the interconnect era," *Computing in Science & Engineering,* vol. 5, pp. 20-24, 2003.

[3]   K. Banerjee and A. Mehrotra, "A power-optimal repeater insertion methodology for global interconnects in nanometer designs," *Electron Devices, IEEE Transactions on,* vol. 49, pp. 2001-2007, 2002.

[4]   I. T. R. f. Semiconductors. (2012). *ITRS 2012 Update.* Available: http://www.itrs.net/Links/2012ITRS/Home2012.htm

[5]   G. Yeap, "Qualcomm Technologies Inc. 5775 Morehouse Drive, R-226G, San Diego, CA 92121," in *Electron Devices Meeting (IEDM), 2013 IEEE International*, 2013, pp. 1.3. 1-1.3. 8.

[6]   IBM. (2014). *Copper Interconnects: The Evolution of Microprocessors*. Available: http://www-03.ibm.com/ibm/history/ibm100/us/en/icons/copperchip/

[7]   S. Sun, "Process technologies for advanced metallization and interconnect systems," in *Electron Devices Meeting, 1997. IEDM'97. Technical Digest., International*, 1997, pp. 765-768.

[8]   S. Rossnagel, R. Wisnieff, D. Edelstein, and T. Kuan, "Interconnect issues post 45nm," in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, 2005, pp. 89-91.

[9]   K.-H. Koo, H. Cho, P. Kapur, and K. C. Saraswat, "Performance comparisons between carbon nanotubes, optical, and Cu for future high-performance on-chip interconnect applications," *Electron Devices, IEEE Transactions on,* vol. 54, pp. 3206-3215, 2007.

[10]   C.-K. Hu, B. Luther, F. Kaufman, J. Hummel, C. Uzoh, and D. Pearson, "Copper interconnection integration and reliability," *Thin Solid Films,* vol. 262, pp. 84-92, 1995.

[11]   J. M. S. Swan, AZ, US), Natarajan, Bala (Phoenix, AZ, US), Chiang, Chien (Fremont, CA, US), Atwood, Greg (San Jose, CA, US), Rao, Valluri R. (Saratoga, CA, US), "Integrated circuit die and an electronic assembly having a three-dimensional interconnection scheme," United States Patent, 2005.

[12]   S.-m. I. M. Kim, KR), Yun, Eun-jung (Seoul, KR), Kim, Dong-won (Gyeonggi-do, KR), Yoon, Jae-man (Seoul, KR), "3-Dimensional flash memory device and method of fabricating the same," United States Patent, 2010.

[13]   S. M. C. Alam, MA, US), Elfadel, Ibrahim M. (Ossining, NY, US), Guarini, Kathryn W. (Yorktown Heights, NY, US), Ieong, Meikei (Wappingers Falls, NY, US), Kudva, Prabhakar N. (New York, NY, US), Kung, David S. (Chappaqua, NY, US), Lavin, Mark A. (Katonah, NY, US), Rahman, Arifur (Freemont, CA, US), "Three dimensional integrated circuit and method of design," United States Patent, 2010.

[14]   M. Koyanagi, H. Kurino, K. W. Lee, K. Sakuma, N. Miyakawa, and H. Itani, "Future system-on-silicon LSI chips," *Micro, IEEE,* vol. 18, pp. 17-22, 1998.

[15]   A. W. Topol, D. La Tulipe, L. Shi, D. J. Frank, K. Bernstein, S. E. Steen*, et al.*, "Three-dimensional integrated circuits," *IBM Journal of Research and Development,* vol. 50, pp. 491-506, 2006.

[16]   R. Beica, C. Sharbono, and T. Ritzdorf, "Through silicon via copper electrodeposition for 3D integration," in *Electronic Components and Technology Conference, 2008. ECTC 2008. 58th*, 2008, pp. 577-583.

[17]   J. Bea, K. Lee, T. Fukushima, T. Tanaka, and M. Koyanagi, "Evaluation of Cu contamination at backside surface of thinned wafer in 3-D integration by transient-capacitance measurement," *Electron Device Letters, IEEE,* vol. 32, pp. 66-68, 2011.

[18]   I. T. R. f. Semiconductors. (2009). *ITRS 2009 Update.* Available: http://www.itrs.net/Links/2009ITRS/Home2009.htm

[19]   I. T. R. f. Semiconductors. (2007). *ITRS 2007 Update.* Available: http://www.itrs.net/Links/2007ITRS/home2007.htm

[20]   A. Gupta, S. Kannan, B. C. Kim, F. Mohammed, and B. Ahn, "Development of novel carbon nanotube TSV technology," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 1699-1702.

[21]   T. Xu, Z. Wang, J. Miao, X. Chen, and C. M. Tan, "Aligned carbon nanotubes for through-wafer interconnects," *Applied Physics Letters,* vol. 91, p. 042108, 2007.

[22]   T. Wang, S. Chen, D. Jiang, Y. Fu, K. Jeppson, L. Ye*, et al.*, "Through-silicon vias filled with densified and transferred carbon nanotube forests," *Electron Device Letters, IEEE,* vol. 33, pp. 420-422, 2012.

[23]   T. Wang, K. Jeppson, L. Ye, and J. Liu, "Carbon‐nanotube through‐silicon via interconnects for three‐dimensional integration," *Small,* vol. 7, pp. 2313-2317, 2011.

[24]   B. Wei, R. Vajtai, and P. Ajayan, "Reliability and current carrying capacity of carbon nanotubes," *Applied Physics Letters,* vol. 79, pp. 1172-1174, 2001.

[25]   E. Pop, D. Mann, Q. Wang, K. Goodson, and H. Dai, "Thermal conductance of an individual single-wall carbon nanotube above room temperature," *Nano Letters,* vol. 6, pp. 96-100, 2006.

[26]   S. Iijima, "Helical microtubules of graphitic carbon," *nature,* vol. 354, pp. 56-58, 1991.

[27]   T. Guo, P. Nikolaev, A. G. Rinzler, D. Tomanek, D. T. Colbert, and R. E. Smalley, "Self-assembly of tubular fullerenes," *The Journal of Physical Chemistry,* vol. 99, pp. 10694-10697, 1995.

[28]   M. Jose-Yacaman, M. Miki-Yoshida, L. Rendon, and J. Santiesteban, "Catalytic growth of carbon microtubules with fullerene structure," *Applied Physics Letters,* vol. 62, pp. 202-204, 1993.

[29]   M. Meyyappan, L. Delzeit, A. Cassell, and D. Hash, "Carbon nanotube growth by PECVD: a review," *Plasma Sources Science and Technology,* vol. 12, p. 205, 2003.

[30]   T. De Los Arcos, F. Vonau, M. Garnier, V. Thommen, H.-G. Boyen, P. Oelhafen*, et al.*, "Influence of iron–silicon interaction on the growth of carbon nanotubes produced by chemical vapor deposition," *Applied physics letters,* vol. 80, pp. 2383-2385, 2002.

[31]   M. Nihei, A. Kawabata, D. Kondo, M. Horibe, S. Sato, and Y. Awano, "Electrical properties of carbon nanotube bundles for future via interconnects," *Japanese journal of applied physics,* vol. 44, p. 1626, 2005.

[32]   T. Dikonimos Makris, L. Giorgi, R. Giorgi, N. Lisi, and E. Salernitano, "CNT growth on alumina supported nickel catalyst by thermal CVD," *Diamond and related materials,* vol. 14, pp. 815-819, 2005.

[33]   W. Zhou, Z. Han, J. Wang, Y. Zhang, Z. Jin, X. Sun*, et al.*, "Copper catalyzing growth of single-walled carbon nanotubes on substrates," *Nano letters,* vol. 6, pp. 2987-2990, 2006.

[34]   S. Bhaviripudi, E. Mile, S. A. Steiner, A. T. Zare, M. S. Dresselhaus, A. M. Belcher*, et al.*, "CVD synthesis of single-walled carbon nanotubes from gold nanoparticle catalysts," *Journal of the American Chemical Society,* vol. 129, pp. 1516-1517, 2007.

[35]   Y. Homma, T. Yamashita, P. Finnie, M. Tomita, and T. Ogino, "Single-walled carbon nanotube growth on silicon substrates using nanoparticle catalysts," *Japanese journal of applied physics,* vol. 41, p. L89, 2002.

[36]   L. Zhu, Y. Xiu, D. W. Hess, and C.-P. Wong, "Aligned carbon nanotube stacks by water-assisted selective etching," *Nano letters,* vol. 5, pp. 2641-2645, 2005.

[37]   S. Vollebregt, R. Ishihara, J. Derakhshandeh, J. van der Cingel, H. Schellevis, and C. Beenakker, "Integrating low temperature aligned carbon nanotubes as vertical interconnects in si technology," in *Nanotechnology (IEEE-NANO), 2011 11th IEEE Conference on*, 2011, pp. 985-990.

[38]   A.-Y. Lo, S.-B. Liu, and C.-T. Kuo, "Effect of temperature gradient direction in the catalyst nanoparticle on CNTs growth mode," *Nanoscale research letters,* vol. 5, pp. 1393-1402, 2010.

[39]   C. J. Lee, J. Park, Y. Huh, and J. Yong Lee, "Temperature effect on the growth of carbon nanotubes using thermal chemical vapor deposition," *Chemical physics letters,* vol. 343, pp. 33-38, 2001.

[40]   S. Wei, W. Kang, J. Davidson, and J. Huang, "Aligned carbon nanotubes fabricated by thermal CVD at atmospheric pressure using Co as catalyst with NH< sub> 3</sub> as reactive gas," *Diamond and related materials,* vol. 15, pp. 1828-1833, 2006.

[41]   M. Chhowalla, K. Teo, C. Ducati, N. Rupesinghe, G. Amaratunga, A. Ferrari*, et al.*, "Growth process conditions of vertically aligned carbon nanotubes using plasma enhanced chemical vapor deposition," *Journal of Applied Physics,* vol. 90, pp. 5308-5317, 2001.

[42]   M. J. Bronikowski, "CVD growth of carbon nanotube bundle arrays," *Carbon,* vol. 44, pp. 2822-2832, 2006.

[43]   H. Cui, G. Eres, J. Y. Howe, A. Puretkzy, M. Varela, D. B. Geohegan*, et al.*, "Growth behavior of carbon nanotubes on multilayered metal catalyst film in chemical vapor deposition," *Chemical Physics Letters,* vol. 374, pp. 222-228, 2003.

[44]   S. Pisana, M. Cantoro, A. Parvez, S. Hofmann, A. Ferrari, and J. Robertson, "The role of precursor gases on the surface restructuring of catalyst films during carbon nanotube growth," *Physica E: Low-dimensional Systems and Nanostructures,* vol. 37, pp. 1-5, 2007.

[45]   Y. T. Lee, J. Park, Y. S. Choi, H. Ryu, and H. J. Lee, "Temperature-dependent growth of vertically aligned carbon nanotubes in the range 800-1100 C," *The Journal of Physical Chemistry B,* vol. 106, pp. 7614-7618, 2002.

[46]   T. Xu, Z. Wang, and J. Miao, "Through-wafer interconnects using carbon nanotubes synthesized by chemical vapor deposition," in *Nano/Micro Engineered and Molecular Systems, 2008. NEMS 2008. 3rd IEEE International Conference on*, 2008, pp. 471-475.

[47]   S. Vollebregt, J. Derakhshandeh, R. Ishihara, M. Wu, and C. Beenakker, "Growth of High-Density Self-Aligned Carbon Nanotubes and Nanofibers Using Palladium Catalyst," *Journal of electronic materials,* vol. 39, pp. 371-375, 2010.

[48]   S. Vollebregt, R. Ishihara, F. Tichelaar, Y. Hou, and C. Beenakker, "Influence of the growth temperature on the first and second-order Raman band ratios and widths of carbon nanotubes and fibers," *Carbon,* vol. 50, pp. 3542-3554, 2012.

[49]   S. Vollebregt, F. Tichelaar, H. Schellevis, C. Beenakker, and R. Ishihara, "Carbon nanotube vertical interconnects fabricated at temperatures as low as 350° C," *Carbon,* 2014.

[50]   C. Zhang, F. Yan, C. Allen, B. Bayer, S. Hofmann, B. Hickey*, et al.*, "Growth of vertically-aligned carbon nanotube forests on conductive cobalt disilicide support," *Journal of Applied Physics,* vol. 108, p. 024311, 2010.

[51]   R. Seidel, G. S. Duesberg, E. Unger, A. P. Graham, M. Liebau, and F. Kreupl, "Chemical vapor deposition growth of single-walled carbon nanotubes at 600 C and a simple growth model," *The Journal of Physical Chemistry B,* vol. 108, pp. 1888-1893, 2004.

[52]   S. Vollebregt, "Carbon Nanotubes as Vertical Interconnects in 3D Integrated Circuits," Doctorate of Philosophy, Department of Microelectronics, Delft University of Technology, Delft, 2014.

[53]   L. Vitos, A. Ruban, H. L. Skriver, and J. Kollar, "The surface energy of metals," *Surface Science,* vol. 411, pp. 186-202, 1998.

[54]   S. Esconjauregui, M. Fouquet, B. C. Bayer, C. Ducati, R. Smajda, S. Hofmann*, et al.*, "Growth of ultrahigh density vertically aligned carbon nanotube forests for interconnects," *ACS nano,* vol. 4, pp. 7431-7436, 2010.

[55]   G.-Y. Xiong, D. Wang, and Z. Ren, "Aligned millimeter-long carbon nanotube arrays grown on single crystal magnesia," *Carbon,* vol. 44, pp. 969-973, 2006.

[56]   S. Hofmann, M. Cantoro, B. Kleinsorge, C. Casiraghi, A. Parvez, J. Robertson*, et al.*, "Effects of catalyst film thickness on plasma-enhanced carbon nanotube growth," *Journal of applied physics,* vol. 98, p. 034308, 2005.

[57]   M. Nihei, A. Kawabata, and Y. Awano, "Direct diameter-controlled growth of multiwall carbon nanotubes on nickel-silicide layer," *Japanese journal of applied physics,* vol. 42, p. L721, 2003.

[58]   Y. Wang, Z. Luo, B. Li, P. S. Ho, Z. Yao, L. Shi*, et al.*, "Comparison study of catalyst nanoparticle formation and carbon nanotube growth: support effect," *Journal of applied physics,* vol. 101, p. 124310, 2007.

[59]   G. Box, W. Hunter, and J. Hunter, "Statistics for experimenters An introduction to design, data analysis and model building John Wiley and Sons," *New York,* 1978.

[60]   J. Wu. (2008). *Design and Analysis of Experiments.* Available: http://www2.isye.gatech.edu/~jeffwu/courses/isye6413/

[61]   D. C. Montgomery, D. C. Montgomery, and D. C. Montgomery, *Design and analysis of experiments* vol. 7: Wiley New York, 1997.

[62]   R. K. Roy, *A primer on the Taguchi method*: Sme, 2010.

[63]   G. Taguchi and D. Clausing, "Robust quality," *Harvard Business Review,* vol. 68, pp. 65-75, 1990.

[64]   J. J. PIGNATIELLO JR and J. S. RAMBERG, "Top ten triumphs and tragedies of Genichi Taguchi," *Quality Engineering,* vol. 4, pp. 211-225, 1991.

[65]   K.-L. Tsui, "An overview of Taguchi method and newly developed statistical methods for robust design," *Iie Transactions,* vol. 24, pp. 44-57, 1992.

[66]   V. Gaitonde, S. Karnik, B. Achyutha, and B. Siddeswarappa, "Methodology of Taguchi optimization for multi-objective drilling problem to minimize burr size," *The International Journal of Advanced Manufacturing Technology,* vol. 34, pp. 1-8, 2007.

[67]   N. Daneshvar, A. Khataee, M. Rasoulifard, and M. Pourhassan, "Biodegradation of dye solution containing Malachite Green: Optimization of effective parameters using Taguchi method," *Journal of Hazardous Materials,* vol. 143, pp. 214-219, 2007.

[68]   J. F. Khaw, B. Lim, and L. E. Lim, "Optimal design of neural networks using the Taguchi method," *Neurocomputing,* vol. 7, pp. 225-245, 1995.

[69]   D. Yu, C. Wang, X. Cheng, and F. Zhang, "Optimization of hybrid PVD process of TiAlN coatings by Taguchi method," *Applied Surface Science,* vol. 255, pp. 1865-1869, 2008.

[70]   S. Santangelo, M. Lanza, E. Piperopoulos, S. Galvagno, and C. Milone, "Optimization of CVD growth of CNT-based hybrids using the Taguchi method," *Materials Research Bulletin,* vol. 47, pp. 595-601, 2012.

[71]   S. Porro, S. Musso, M. Giorcelli, A. Chiodoni, and A. Tagliaferro, "Optimization of a thermal-CVD system for carbon nanotube growth," *Physica E: Low-dimensional Systems and Nanostructures,* vol. 37, pp. 16-20, 2007.

[72]   K. Dasgupta, D. Sen, S. Mazumder, C. Basak, J. Joshi, and S. Banerjee, "Optimization of parameters by Taguchi method for controlling purity of carbon nanotubes in chemical vapour deposition technique," *Journal of nanoscience and nanotechnology,* vol. 10, pp. 4030-4037, 2010.

[73]   P. R. Apte. (2013). *TAGUCHI Methods / Robust Design / Design of Experiments.* Available: http://www.ee.iitb.ac.in/~apte/CV_PRA_TAGUCHI.htm

[74]   C.-P. Fung and P.-C. Kang, "Multi-response optimization in friction properties of PBT composites using Taguchi method and principle component analysis," *Journal of Materials Processing Technology,* vol. 170, pp. 602-610, 2005.

[75]   J. J. Pignatiello Jr, "Strategies for robust multiresponse quality engineering," *IIE transactions,* vol. 25, pp. 5-15, 1993.

[76]   J. Antony, R. B. Anand, M. Kumar, and M. Tiwari, "Multiple response optimization using Taguchi methodology and neuro-fuzzy based model," *Journal of Manufacturing Technology Management,* vol. 17, pp. 908-925, 2006.

[77]   C. Lin, "Use of the Taguchi method and grey relational analysis to optimize turning operations with multiple performance characteristics," *Materials and manufacturing processes,* vol. 19, pp. 209-220, 2004.

[78]   E. Kuram and B. Ozcelik, "Multi-objective optimization using Taguchi based grey relational analysis for micro-milling of Al 7075 material with ball nose end mill," *Measurement,* vol. 46, pp. 1849-1864, 2013.

[79]   J. Lin and C. Lin, "The use of the orthogonal array with grey relational analysis to optimize the electrical discharge machining process with multiple performance characteristics," *International Journal of Machine Tools and Manufacture,* vol. 42, pp. 237-244, 2002.

[80]   R. Jeyapaul, P. Shahabudeen, and K. Krishnaiah, "Quality management research by considering multi-response problems in the Taguchi method–a review," *The International Journal of Advanced Manufacturing Technology,* vol. 26, pp. 1331-1337, 2005.

[81]   K. Graff and H. Pieper, "The properties of iron in silicon," *Journal of the Electrochemical Society,* vol. 128, pp. 669-674, 1981.

[82]   R. Xiang, Z. Yang, Q. Zhang, G. Luo, W. Qian, F. Wei*, et al.*, "Growth deceleration of vertically aligned carbon nanotube arrays: Catalyst deactivation or feedstock diffusion controlled?," *The Journal of Physical Chemistry C,* vol. 112, pp. 4892-4896, 2008.

[83]   Discussions with dr. H. Schellevis, DIMES, TU Delft, 2013.

[84]   J. Hart. (2014). *Nanotube architectures*. Available: www.nanobliss.com

[85]   A. J. Hart, "Chemical, Mechanical and Thermal Control of Substrate-Bound Carbon Nanotube Growth," Doctorate of Philosophy, Department of Mechanical Engineering, Massachusetts Institute of Technology, Cambridge, MA, 2006.

[86]   A. J. Hart and A. H. Slocum, "Rapid growth and flow-mediated nucleation of millimeter-scale aligned carbon nanotube structures from a thin-film catalyst," *The Journal of Physical Chemistry B,* vol. 110, pp. 8250-8257, 2006.

[87]   A. Hart, B. Boskovic, A. Chuang, V. Golovko, J. Robertson, B. Johnson*, et al.*, "Uniform and selective CVD growth of carbon nanotubes and nanofibres on arbitrarily microstructured silicon surfaces," *Nanotechnology,* vol. 17, p. 1397, 2006.

[88]   A. J. Hart, H. K. Taylor, and A. H. Slocum, "2D and 3D growth of carbon nanotubes on substrates, from nanometre to millimetre scales," *International Journal of Nanomanufacturing,* vol. 1, pp. 701-709, 2007.

[89]   A. J. Hart, A. H. Slocum, and L. Royer, "Growth of conformal single-walled carbon nanotube films from Mo/Fe/Al2O3 deposited by electron beam evaporation," *Carbon,* vol. 44, pp. 348-359, 2006.

[90]   M. J. Bronikowski, H. M. Manohara, and B. D. Hunt, "Growth of carbon nanotube bundle arrays on silicon surfaces," *Journal of Vacuum Science & Technology A,* vol. 24, pp. 1318-1322, 2006.

[91]   M. J. Bronikowski, "Longer nanotubes at lower temperatures: the influence of effective activation energies on carbon nanotube growth by thermal chemical vapor deposition," *The Journal of Physical Chemistry C,* vol. 111, pp. 17705-17712, 2007.

[92]   G.-H. Jeong, N. Olofsson, L. K. Falk, and E. E. Campbell, "Effect of catalyst pattern geometry on the growth of vertically aligned carbon nanotube arrays," *Carbon,* vol. 47, pp. 696-704, 2009.

[93]   M. Kabir, R. E. Morjan, O. Nerushev, P. Lundgren, S. Bengtsson, P. Enoksson*, et al.*, "Fabrication of individual vertically aligned carbon nanofibres on metal substrates from prefabricated catalyst dots," *Nanotechnology,* vol. 17, p. 790, 2006.

[94]   M. Jönsson, O. Nerushev, and E. E. Campbell, "Dc plasma-enhanced chemical vapour deposition growth of carbon nanotubes and nanofibres: in situ spectroscopy and plasma current dependence," *Applied Physics A,* vol. 88, pp. 261-267, 2007.

[95]   S. Sinnott, R. Andrews, D. Qian, A. Rao, Z. Mao, E. Dickey*, et al.*, "Model of carbon nanotube growth through chemical vapor deposition," *Chemical Physics Letters,* vol. 315, pp. 25-30, 1999.

[96]   W. Hu, D. Gong, Z. Chen, L. Yuan, K. Saito, C. A. Grimes*, et al.*, "Growth of well-aligned carbon nanotube arrays on silicon substrates using porous alumina film as a nanotemplate," *Applied Physics Letters,* vol. 79, pp. 3083-3085, 2001.

[97]   J. McFarland, "Investigation of Carbon Nanotube Growth Using a Nozzle CVD Method," Bachelors of Science, Department of Physics, Pomona College, 2006.

[98]   G. Li, S. Chakrabarti, M. Schulz, and V. Shanov, "The effect of substrate positions in chemical vapor deposition reactor on the growth of carbon nanotube arrays," *Carbon,* vol. 48, pp. 2111-2115, 2010.

[99]   S. Yasuda, D. N. Futaba, T. Yamada, J. Satou, A. Shibuya, H. Takai*, et al.*, "Improved and large area single-walled carbon nanotube forest growth by controlling the gas flow direction," *ACS nano,* vol. 3, pp. 4164-4170, 2009.

[100] M. Falvo, G. Clary, R. Taylor, V. Chi, F. Brooks, S. Washburn, *et al.*, "Bending and buckling of carbon nanotubes under large strain," *Nature,* vol. 389, pp. 582-584, 1997.

[101] H. Shima, "Buckling of Carbon Nanotubes: A State of the Art Review," *Materials (1996-1944),* vol. 5, 2012.

[102] Y. Xu and A. Srivastava, "A model for carbon nanotube interconnects," *International Journal of Circuit Theory and Applications,* vol. 38, pp. 559-575, 2010.

[103] A. Maffucci, G. Miano, and F. Villone, "A new circuit model for carbon nanotube interconnects with diameter-dependent parameters," *Nanotechnology, IEEE Transactions on,* vol. 8, pp. 345-354, 2009.

[104] Y. Massoud and A. Nieuwoudt, "Modeling and design challenges and solutions for carbon nanotube-based interconnect in future high performance integrated circuits," *ACM Journal on Emerging Technologies in Computing Systems (JETC),* vol. 2, pp. 155-196, 2006.

[105] A. Raychowdhury and K. Roy, "Modeling of metallic carbon-nanotube interconnects for circuit simulations and a comparison with Cu interconnects for scaled technologies," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on,* vol. 25, pp. 58-65, 2006.

[106] J. Nygard. (2012). *Tutorial on Electronic Transport*. Available: http://nanotube.msu.edu/

[107] C. Dekker, "Carbon nanotubes as molecular quantum wires," *Physics today,* vol. 52, pp. 22-30, 1999.

[108] R. Saito, G. Dresselhaus, and M. S. Dresselhaus, *Physical properties of carbon nanotubes* vol. 4: World Scientific, 1998.

[109] S. J. Tans, A. R. Verschueren, and C. Dekker, "Room-temperature transistor based on a single carbon nanotube," *Nature,* vol. 393, pp. 49-52, 1998.

[110] J.-O. Lee, C. Park, J.-J. Kim, J. Kim, J. W. Park, and K.-H. Yoo, "Formation of low-resistance ohmic contacts between carbon nanotube and metal electrodes by a rapid thermal annealing method," *Journal of Physics D: Applied Physics,* vol. 33, p. 1953, 2000.

[111] J. Tersoff, "Contact resistance of carbon nanotubes," *Applied Physics Letters,* vol. 74, pp. 2122-2124, 1999.

[112] A. Javey, J. Guo, D. B. Farmer, Q. Wang, D. Wang, R. G. Gordon, *et al.*, "Carbon nanotube field-effect transistors with integrated ohmic contacts and high-$\varkappa$ gate dielectrics," *Nano Letters,* vol. 4, pp. 447-450, 2004.

[113] A. Naeemi and J. D. Meindl, "Performance Modeling for Carbon Nanotube Interconnects," in *Carbon Nanotube Electronics*, ed: Springer, 2009, pp. 163-190.

[114] A. Naeemi and J. D. Meindl, "Design and performance modeling for single-walled carbon nanotubes as local, semiglobal, and global interconnects in gigascale integrated systems," *Electron Devices, IEEE Transactions on,* vol. 54, pp. 26-37, 2007.

[115] A. Naeemi and J. D. Meindl, "Carbon nanotube interconnects," in *Proceedings of the 2007 international symposium on Physical design*, 2007, pp. 77-84.

[116] J. Jiang, R. Saito, A. Grüneis, S. Chou, G. G. Samsonidze, A. Jorio, *et al.*, "Photoexcited electron relaxation processes in single-wall carbon nanotubes," *Physical Review B,* vol. 71, p. 045417, 2005.

[117] E. Pop, D. Mann, J. Reifenberg, K. Goodson, and H. Dai, "Electro-thermal transport in metallic single-wall carbon nanotubes for interconnect applications," in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, 2005, pp. 4 pp.-256.

[118] M. Lazzeri, S. Piscanec, F. Mauri, A. Ferrari, and J. Robertson, "Electron transport and hot phonons in carbon nanotubes," *Physical review letters,* vol. 95, p. 236802, 2005.

[119] A. Naeemi and J. D. Meindl, "Compact physical models for multiwall carbon-nanotube interconnects," *Electron Device Letters, IEEE,* vol. 27, pp. 338-340, 2006.

[120] H. J. Li, W. Lu, J. Li, X. Bai, and C. Gu, "Multichannel ballistic transport in multiwall carbon nanotubes," *Physical review letters,* vol. 95, p. 086601, 2005.

[121] T. W. Odom, J.-L. Huang, P. Kim, and C. M. Lieber, "Atomic structure and electronic properties of single-walled carbon nanotubes," *Nature,* vol. 391, pp. 62-64, 1998.

[122] N. Srivastava, H. Li, F. Kreupl, and K. Banerjee, "On the applicability of single-walled carbon nanotubes as VLSI interconnects," *Nanotechnology, IEEE Transactions on,* vol. 8, pp. 542-559, 2009.

[123] Z. Yao, C. L. Kane, and C. Dekker, "High-field electrical transport in single-wall carbon nanotubes," *Physical Review Letters,* vol. 84, p. 2941, 2000.

[124] H. Li, W.-Y. Yin, K. Banerjee, and J.-F. Mao, "Circuit modeling and performance analysis of multi-walled carbon nanotube interconnects," *Electron Devices, IEEE Transactions on,* vol. 55, pp. 1328-1337, 2008.

[125] H. Li, W.-Y. Yin, J.-F. Mao, and K. Banerjee, "Performance analysis of multi-walled carbon nanotube based interconnects," in *Semiconductor Device Research Symposium, 2007 International*, 2007, pp. 1-2.

[126] B. Bourlon, C. Miko, L. Forro, D. Glattli, and A. Bachtold, "Determination of the intershell conductance in multiwalled carbon nanotubes," *Physical review letters,* vol. 93, p. 176806, 2004.

[127] P. Collins and P. Avouris, "Multishell conduction in multiwalled carbon nanotubes," *Applied Physics A,* vol. 74, pp. 329-332, 2002.

[128]   S. Esconjauregui, B. Bayer, M. Fouquet, C. Wirth, C. Ducati, S. Hofmann*, et al.*, "Growth of high-density vertically aligned arrays of carbon nanotubes by plasma-assisted catalyst pretreatment," *Applied Physics Letters,* vol. 95, p. 173115, 2009.

[129]   M. Cantoro, S. Hofmann, S. Pisana, V. Scardaci, A. Parvez, C. Ducati*, et al.*, "Catalytic chemical vapor deposition of single-wall carbon nanotubes at low temperatures," *Nano Letters,* vol. 6, pp. 1107-1112, 2006.

[130]   A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, "Ballistic carbon nanotube field-effect transistors," *Nature,* vol. 424, pp. 654-657, 2003.

[131]   L. Cancado, K. Takai, T. Enoki, M. Endo, Y. Kim, H. Mizusaki*, et al.*, "General equation for the determination of the crystallite size L a of nanographite by Raman spectroscopy," *Applied Physics Letters,* vol. 88, pp. 163106-163106-3, 2006.

[132]   M. S. Dresselhaus, G. Dresselhaus, R. Saito, and A. Jorio, "Raman spectroscopy of carbon nanotubes," *Physics Reports,* vol. 409, pp. 47-99, 2005.

[133]   A. Jorio, R. Saito, J. Hafner, C. Lieber, M. Hunter, T. McClure*, et al.*, "Structural (n, m) determination of isolated single-wall carbon nanotubes by resonant Raman scattering," *Physical Review Letters,* vol. 86, p. 1118, 2001.

[134]   J. Li, Q. Ye, A. Cassell, H. T. Ng, R. Stevens, J. Han*, et al.*, "Bottom-up approach for carbon nanotube interconnects," *Applied Physics Letters,* vol. 82, pp. 2491-2493, 2003.

[135]   S. Masahito, Y. Kashiwagi, Y. Li, K. Arstila, O. Richard, D. J. Cott*, et al.*, "Measuring the electrical resistivity and contact resistance of vertical carbon nanotube bundles for application as interconnects," *Nanotechnology,* vol. 22, p. 085302, 2011.

[136]   W. Wu, S. Krishnan, T. Yamada, X. Sun, P. Wilhite, R. Wu*, et al.*, "Contact resistance in carbon nanostructure via interconnects," *Applied Physics Letters,* vol. 94, pp. 163113-163113-3, 2009.

[137]   L. Zhu, J. Xu, Y. Xiu, Y. Sun, D. W. Hess, and C. Wong, "Growth and electrical characterization of high-aspect-ratio carbon nanotube arrays," *Carbon,* vol. 44, pp. 253-258, 2006.

[138]   Q. Ngo, A. M. Cassell, A. J. Austin, J. Li, S. Krishnan, M. Meyyappan*, et al.*, "Characteristics of aligned carbon nanofibers for interconnect via applications," *Electron Device Letters, IEEE,* vol. 27, pp. 221-224, 2006.

[139]   M. H. van der Veen, Y. Barbarin, B. Vereecke, M. Sugiura, Y. Kashiwagi, D. J. Cott*, et al.*, "Electrical improvement of CNT contacts with Cu damascene top metallization," in *Interconnect Technology Conference (IITC), 2013 IEEE International,* 2013, pp. 1-3.

[140]   T. Wang, K. Jeppson, N. Olofsson, E. E. Campbell, and J. Liu, "Through silicon vias filled with planarized carbon nanotube bundles," *Nanotechnology,* vol. 20, p. 485203, 2009.

[141]   R. Xie, C. Zhang, M. van der Veen, K. Arstila, T. Hantschel, B. Chen*, et al.*, "Carbon nanotube growth for through silicon via application," *Nanotechnology,* vol. 24, p. 125603, 2013.

[142]   N. Chiodarelli, K. Kellens, D. J. Cott, N. Peys, K. Arstila, M. Heyns*, et al.*, "Integration of vertical carbon nanotube bundles for interconnects," *Journal of The Electrochemical Society,* vol. 157, pp. K211-K217, 2010.

[143]   H. Wei, N. Patil, A. Lin, H.-S. Wong, and S. Mitra, "Monolithic three-dimensional integrated circuits using carbon nanotube FETs and interconnects," in *Electron Devices Meeting (IEDM), 2009 IEEE International,* 2009, pp. 1-4.

[144]   Discussions with dr. G. Pandraud, DIMES, TU Delft, 2013.

[145]   Discussions with ir. A. Damian, NXP Semiconductors, 2013.

[146]   D. K. Schroder, *Semiconductor material and device characterization*: John Wiley & Sons, 2006.

[147]   S. Vollebregt, S. Banerjee, K. Beenakker, and R. Ishihara, "Thermal conductivity of low temperature grown vertical carbon nanotube bundles measured using the three-ω method," *Applied Physics Letters,* vol. 102, p. 191909, 2013.

List of Figures

List of Tables