A Low-Noise Fractional-N Digital Frequency Synthesizer With Implicit Frequency Tripling for mm-Wave Applications

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A Low-Noise Fractional-*N* Digital Frequency Synthesizer With Implicit Frequency Tripling for mm-Wave Applications

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***Abstract*— In this paper, we propose a 60-GHz fractional-*N* digital frequency synthesizer aimed at reducing its phase noise (PN) at both the flicker ($1/f^3$) and thermal ($1/f^2$) regions while minimizing its power consumption. The digitally controlled oscillator (DCO) fundamentally resonates at 20 GHz and co-generates a strong third harmonic at 60 GHz which is extracted to the output while canceling the 20-GHz fundamental. The latter component is fed back to the frequency dividers in an all-digital phase-locked loop for phase detection, which comprises a pair of digital-to-time and time-to-digital converters with $\Sigma\Delta$ dithering to attenuate fractional spurs. The mechanism of flicker noise upconversion to $1/f^3$ PN in the DCO is investigated, and a reduction technique is proposed. The 28-nm CMOS prototype achieves 213–277-fs rms jitter in the 57.5–67.2-GHz tuning range while consuming only 40 mW. The DCO flicker PN corner is record low at 300–400 kHz.**

***Index Terms*— 60 GHz, all-digital phase-locked loop (ADPLL), digitally controlled oscillator (DCO), digital-to-time converter (DTC), flicker noise, flicker noise upconversion, fractional-*N* PLL, fractional spur suppression, harmonic boosting, harmonic extraction, implicit multiplier, mm-wave (mmW), phase noise (PN), time-to-digital converter (TDC).**

I. Introduction

RECENT years have witnessed the blooming of mm-wave (mmW) applications, such as 5G communications, automotive radars, and wireless backhaul [1]–[3]. Phase-locked loops (PLLs) are the key sub-systems, which determine the performance of mmW transceivers. They require low phase noise (PN) and wide tuning range (TR) at low power consumption. In practice, however, physical, circuit- and architecture-level limitations set performance and power efficiency barriers. Passive devices at mmW frequencies feature low quality (Q)-factor, which limits the oscillator's PN performance. In the feedback frequency divider path, the frequency division ratio between the mmW output and the input reference clock is large. Design complexity of mmW frequency prescalers is significant [4]. These facts pose challenges in designing mmW PLLs that are power efficient and of low PN.

Several approaches have been reported to improve the integrated PN (IPN) or rms jitter of mmW PLLs. In [5] and [6], a sub-sampling technique was applied to a 60-GHz integer-*N* analog PLL. Wide loop bandwidth (BW) of >1 MHz was used to suppress the voltage controlled oscillator (VCO) PN and achieve good IPN. In [7], low IPN was reported in a 60-GHz integer-*N* charge-pump (CP) PLL by means of a high-frequency reference (FREF) clock of 135 MHz and wide BW. However, those techniques cannot be easily migrated to fractional-*N* PLLs, where the loop components contribute significant noise. A 60-GHz fractional-*N* all-digital PLL (ADPLL) with a fine-resolution (450 fs) time-to-digital converter (TDC) was introduced in [8] to achieve low IPN. Again, with a high FREF of 100 MHz and power-hungry fine-resolution TDC, the PLL BW was set to >2 MHz to suppress the oscillator PN. However, complicated off-line calibration procedures and stringent timing conditions are required. Wide loop BW is not optimal for spur suppression, either. Similar approaches (i.e., 125-MHz FREF, wide BW, and fine-resolution TDC) are adopted in the *W*-band ADPLL in [9]. In [10], low IPN was achieved in a fractional-*N* ADPLL with a fine-resolution (310 fs) digital-to-time converter (DTC) and 20-GHz digitally controlled oscillator (DCO). However, complicated digital predistortion algorithms were necessary to improve the DTC linearity. An extra *LC* tank was employed for tail filtering in the DCO for better PN. All the aforementioned solutions demand low-noise loop components to suppress the oscillator PN.

In this paper, we propose an alternative approach to realize the fractional-*N* 60-GHz generation at low PN. Instead of pursuing the minimum noise from the reference and feedback loop, the oscillator PN is significantly improved by the proposed $1/f^3$ noise suppression technique and third-harmonic (H3) boosted 20-GHz DCO. Meanwhile, implicit frequency tripling is achieved inside the DCO. Since the DCO PN is improved, the constraints on the loop components are simplified. It gives a margin for narrower BW to suppress the TDC quantization noise and spurious tones while maintaining the low IPN. A TDC sub-system with medium resolution is

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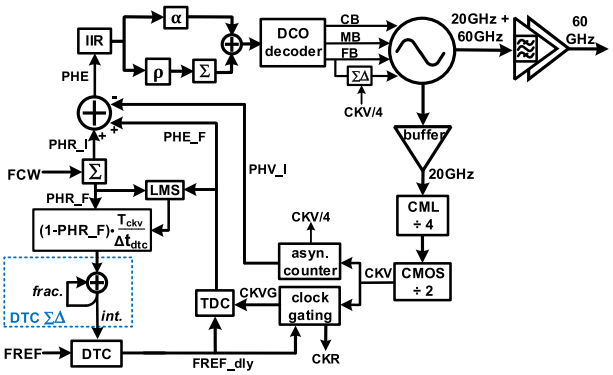


Fig. 1. Architecture of the proposed ADPLL generating 60 GHz.

adopted for a better power efficiency and linearity. Furthermore, the implicit tripling in the DCO eliminates frequency dividers or multipliers that operate directly at mmW frequencies. The power efficiency is further enhanced with the reduced design complexity.

The rest of this paper is organized as follows. Section II introduces the proposed ADPLL architecture. Circuit-level flicker noise upconversion mechanisms and the proposed suppression technique are described in Section III. Section IV proposes the 20-GHz cancellation technique. The implementation of phase detection is detailed in Section V. Experimental results are given in Section VI.

II. ADPLL Architecture

The system diagram of the ADPLL-based 60-GHz digital frequency synthesizer is shown in Fig. 1. At its center lies a harmonic-boosting 20-GHz DCO featuring improved PN in both the $1/f^3$ and $1/f^2$ regions. Strong H3 at 60 GHz is generated alongside the 20-GHz fundamental in the DCO. The co-generated H3 is extracted and fed forward to the 60-GHz output buffer, which simultaneously suppresses the 20-GHz component. In the feedback path, the 20-GHz signal is prescaled by ÷4 current-mode logic (CML) and ÷2 CMOS dividers to generate a variable clock (CKV) for phase detection in the ADPLL. The directly available 60-GHz signal from the DCO exempts the demands for further frequency multiplication in the feedforward path. In this way, the conventional 60-GHz frequency dividers or doublers/triplers to 60 GHz, which typically suffer from the limited locking range and large power consumption, are avoided. This simplifies the design and enhances its robustness. Compared with the PLLs employing 60-GHz fundamental oscillators, the relatively smaller 60-GHz swing from the 20-GHz DCO may require more power consumption in the buffer to amplify it and drive the loads. A similar scenario also happens at the output of the conventional frequency triplers [11]. In this design, the H3 swing is boosted in the DCO. This relaxes the requirements on the gain of the buffer and reduces the power overhead in it. Overall, these approaches help to improve the power efficiency of the 60-GHz frequency synthesizer.

An 8-bit counter digitizes the integer part of the CKV phase. The resulting PHV_I[k] is compared with the integer part of the reference phase PHR_I[k] to generate the integer part of the phase error, PHE_I[k]. The FREF clock is delayed by a DTC, whose delay is determined by the fractional part of the reference phase (PHR_F[k]). The DTC is controlled by a $\Sigma\Delta$ modulator ($\Sigma\Delta$M) and covers a range that is a bit larger than one CKV period. A least-mean-square (LMS) algorithm [12] runs in the background to calibrate the DTC gain. The DTC output, FREF_dly, is used to clock-gate the CKV to generate CKVG, as well as the retimed clock, CKR, for the digital logic [13]. The TDC digitizes the phase difference between CKVG and FREF_dly and provides, after the normalization, the fractional phase error PHE_F[k]. A small TDC detection range can slow down the transient settling or locking time of the ADPLL in some cases. For a more robust operation, it covers a detection range that is 40% of the CKV period. Furthermore, during the settling process, once TDC overflow or underflow is detected, the TDC output is overwritten by a maximum or minimum value. It facilitates the settling speed [13]. After the PLL is locked, only a few cells in the middle of the TDC chain are active. The composite phase error, PHE[k]=PHE_I[k]+PHE_F[k], is fed to the digital loop filter (LF), which comprises a proportional–integral (PI) controller and a fourth-order IIR filter. The LF output is fed to the DCO as its tuning word through a decoder.

In this paper, the PLL BW is optimized for low IPN. The DCO PN is high-pass filtered by the loop. However, unless otherwise wide loop BW is used, the high close-in PN (typically the $1/f^3$ noise) of the oscillators could even dominate the PLLs' in-band PN in many cases. It will be further analyzed in Section III-B. To have more freedom in optimizing the loop BW, the $1/f^3$ noise of the DCO is targeted to be low in this design. Wideband carrier recovery loops in the transceiver baseband can filter out the close-in PN [14]. However, in some applications (such as radars), they may not be available. This paper targets low IPN from the PLL itself. To achieve this goal, the noise contribution from FREF, DTC, TDC, and frequency dividers, which are low-pass filtered by the loop, should also be minimized. FREF noise floor is predefined by the crystal oscillator and tends to be conservatively around −150 dBc/Hz for a 40-MHz FREF used in this design. The noise floor of the frequency dividers and DTC is designed to be significantly (about 7 dB) below the FREF noise floor so that they have a negligible contribution to the ADPLL output PN. TDC quantization (Q)-noise can be reduced by improving its resolution, typically at the cost of a larger power consumption and degraded INL linearity that will create fractional spurs [15]. However, significant lowering of the TDC Q-noise below that of FREF or DCO's contribution cannot further improve the in-band PN. With the targeting low $1/f^3$ DCO, its in-band contribution should be less than or comparable to that of FREF. For the optimal power efficiency and linearity, the TDC Q-noise is designed at the same level as the FREF noise floor. This corresponds to the TDC resolution of 3 ps with 40-MHz FREF.

The DTC $\Sigma\Delta$M quantization noise-induced PN is given by

$$L_{\mathrm{dtc}}(\Delta f) = \frac{1}{12}\cdot\frac{(\Delta t_{\mathrm{dtc}})^2}{f_{\mathrm{ref}}}\cdot(2\pi f_o)^2\cdot\left[2\sin\left(\frac{\pi\,\Delta f}{f_{\mathrm{ref}}}\right)\right]^2\cdot|H_{\mathrm{cl}}(\Delta f)|^2 \quad (1)$$

where $\Delta t_{\rm dtc}$ is the DTC resolution, $f_{\rm ref}$ is the FREF clock frequency, f_o is the PLL output frequency, and $H_{\rm cl}(\Delta f)$ is the close-loop transfer function of the DTC noise to the output. Besides the PI controller, the IIR filter in $H_{\rm cl}(\Delta f)$ provides extra attenuation to the high-frequency $\Sigma\Delta$M quantization noise. The DTC resolution is optimized so that $L_{\rm dtc}(\Delta f)$ has marginal contribution to the IPN. In this design, the DTC resolution should be below 16 ps so that its degradation on the IPN is less than 0.5 dB. To reduce the TDC dynamic range, fine DTC resolution is desired as well. On the other hand, with better resolution, more delay unit cells are required in the DTC to cover one CKV period. The long DTC delay chain is typically more prone to linearity degradation. As a tradeoff, the DTC resolution is chosen as 12 ps in this design.

III. Low $1/f^3$ Third-Harmonic Boosted DCO

A. DCO Topology

In order to co-generate the 60-GHz carrier within the 20-GHz oscillator, an H3-tuned DCO is chosen, as shown in Fig. 2. To achieve a sufficiently strong level of the H3 component, the resonant LC tank should exhibit a relatively large impedance at 60 GHz. A transformer-based dual-resonance LC tank with $k_m = 0.6$ is used to boost the H3 component [16], as shown in Fig. 2(a). Its operating principle is shown in Fig. 2(b). The simulated H3-to-fundamental voltage swing ratio in the DCO [i.e., $V_{\rm DH3}/V_{\rm DH1}$ in Fig. 2(b)] is 40%.

The DCO is segmented into four switched-capacitor banks: 4-bit binary coarse tuning (CB), 31-bit unary mid-coarse tuning (MB), 60-bit unary fine tuning (FB), and 3-bit unary FB for a high-speed $\Sigma\Delta$M. The CB is replicated at the primary and secondary windings, both of which are tuned simultaneously to ensure that the second resonance tracks the fundamental resonant frequency (H1). The MB and FB are only placed at the secondary winding for a simple and compact layout. Since the TR of MB and FB is small, they will not introduce any significant misalignment between the second resonance and H3 frequencies. The three tuning banks are sized for 260-, 35-, and 3-MHz/bit unit steps (i.e., DCO resolution, $K_{\rm DCO}$) at the 60-GHz carrier, respectively. The high-speed $\Sigma\Delta$M clocked at CKV/4 (600 MHz) reduces the DCO Q-noise. It can be programed as a first or second order.

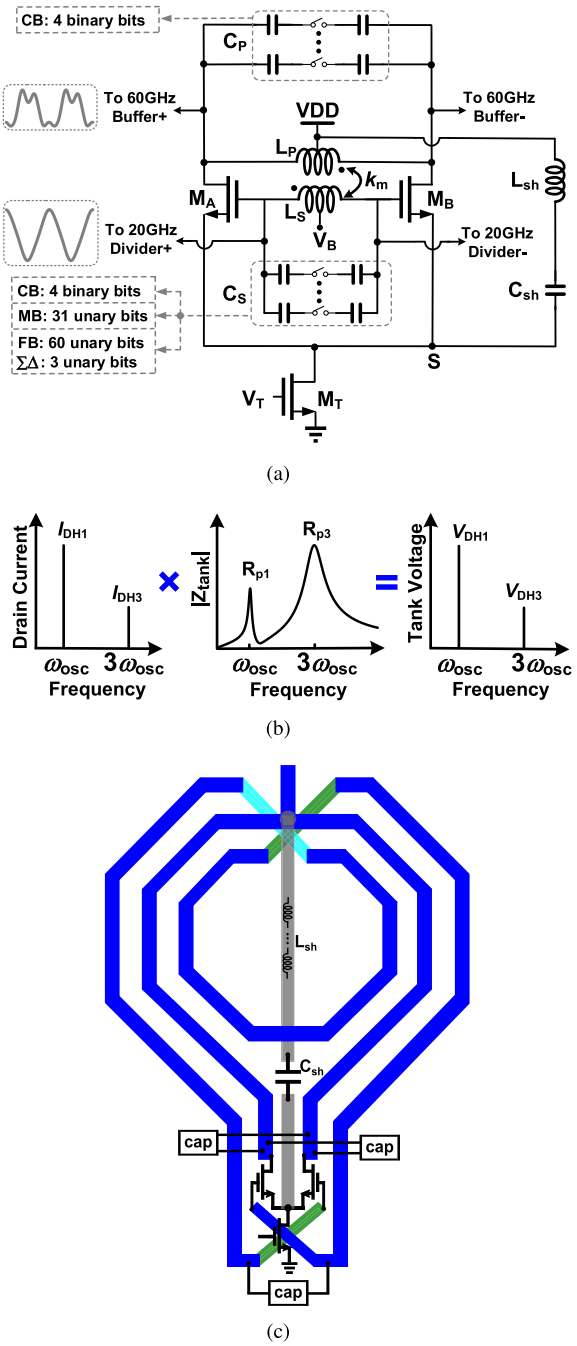
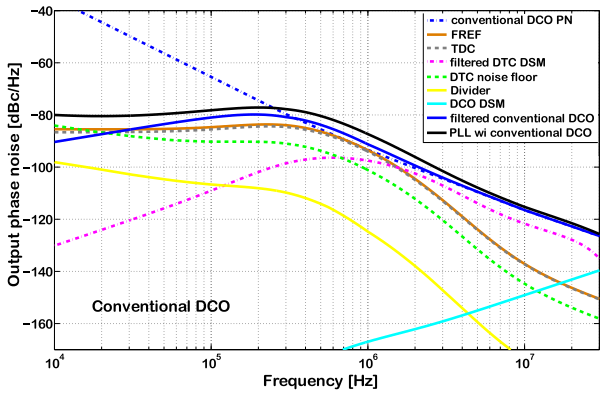


Fig. 2. (a) Schematic, (b) operating principle, and (c) concept layout of the DCO.

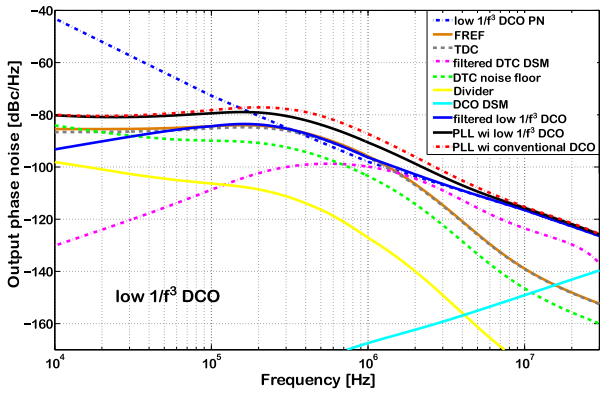
B. $1/f$ Noise Upconversion and Its Suppression

To achieve low IPN at the ADPLL output without excessively increasing its loop BW, the DCO PN should be minimized. The 20-GHz LC tank can have a much better Q-factor compared with the 60-GHz counterparts. Also, boosting the generated H3 sharpens the waveform transitions and results in a lower impulse sensitivity function (ISF). These two advantages ensure lower PN induced by the thermal noise in the DCO circuitry. However, the upconverted $1/f$ noise can deteriorate the overall jitter, especially when the loop BW is narrower than the $1/f^3$ corner (>1 MHz in the conventional 60-GHz oscillators [17], [18]). Keeping the other loop components and noise sources identical, two ADPLLs with different DCO $1/f^3$ corners, one at 1 MHz (i.e., conventional) and the other at 300 kHz (i.e., improved target), are investigated based on an s-domain linear model. As shown in Fig. 3, for the typical $1/f^3$ case, the DCO's contribution to the in-band PN is much higher than that caused by the TDC and FREF noise floor. IPN of the PLL with conventional $1/f^3$ DCO is 2.3 dB higher than that with the low $1/f^3$ DCO. Therefore, the currently achievable $1/f^3$ noise corner should be substantially reduced to achieve lower in-band PN.

Techniques to lower the flicker noise upconversion have been proposed for single-GHz voltage-biased oscillators [19], [20]. However, they are sensitive to parasitic



(a)



(b)

Fig. 3. 60-GHz ADPLL output PN with two different corners of DCO $1/f^3$ noise (a) 1 MHz and (b) 300 kHz.

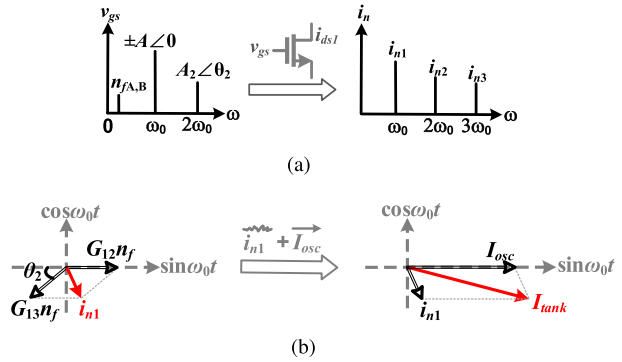


Fig. 4. (a) Flicker noise upconversion to high-frequency current noise in i_{ds1}. (b) Flicker noise direct conversion to PN.

inductances and capacitances between VDD and VSS supply rails. This effect becomes, especially, important when the VDD routing is physically away from VSS, and effects of which are greatly magnified at mmW frequencies. Therefore, those techniques have tight constraints in practical mmW designs. Moreover, they are not applicable to current-biased oscillators, i.e., those employing a tail current source (e.g., M_T in Fig. 2), which is helpful for power supply rejection and oscillation amplitude control. In the presence of tail current, its parasitic capacitance provides an extra medium for the flicker noise of the $M_{A,B}$ transistors to be upconverted to PN [21]. Furthermore, the $1/f$ upconversion mechanism has not been yet comprehensively explained.

Flicker noise in the tail current source can be upconverted to $1/f^3$ PN. However, with a large transistor size or its outright replacement by digitally controlled resistors, its contribution can be made marginal. In this paper, we specifically focus on the $1/f$ noise upconversion mechanism by the cross-coupling transistors ($M_{A,B}$) that sustain the oscillation. Flicker noise in $M_{A,B}$ is upconverted to the respective drain current i_{ds} at oscillation frequency ω_0 and its harmonics through higher-order nonlinearities. Within the physical circuit constraints, assume $v_{\mathrm{gs}} = \pm A \sin\omega_0 t + \sum_{n=2k} A_n \cos(n\omega_0 t + \theta_n) \pm \sum_{n=2k+1} A_n \sin(n\omega_0 t + \theta_n) + n_{fA,B}$, where $n_{fA,B}$ is the input-referred flicker noise of M_A or M_B and $k = 1, 2, 3 \ldots$. In a steady-state oscillation, $M_{A,B}$ traverses through sub-threshold, saturation, and triode regions. The total i_{ds} value can be segmented into three parts: i_{ds1} that only depends on v_{gs}, i_{ds2} that depends on both v_{gs} and v_{ds}, and i_{ds3} that only depends on v_{ds}. Detailed analysis can be found in the Appendix. i_{ds1} induced by v_{gs} can be expressed as

$$i_{\mathrm{ds1}} = a_1 v_{\mathrm{gs}} + a_2 v_{\mathrm{gs}}^2 + a_3 v_{\mathrm{gs}}^3 + \cdots \tag{2}$$

where $a_1, a_2, a_3, \ldots$ represent the fundamental and higher-order large-signal nonlinearity coefficients. It directly upconverts the $1/f$ noise in v_{gs} to high frequencies. i_{ds2} is induced by v_{ds} on the periodically varying g_{ds} of $M_{A,B}$. Upconverted $1/f$ noise at high-order harmonic frequencies in v_{ds} is mixed with g_{ds}. The $1/f$ noise can be indirectly upconverted to fundamental frequency in this way. i_{ds3} typically plays a little role and is neglected here.

In practical LC oscillators, higher order harmonics in v_{gs} are small and so at most only the second harmonic (H2) and H3 need to be considered. For easy illustration, we take H2 as the only such harmonic. The procedure for H3 would be similar. The H2 component is common mode (CM). Such a component is propagated from i_{ds} to v_{gs} of the g_m-pair. Its phase is determined by the CM (trans-)impedance termination at H2 (Z_{trans2}) in this path. If it is resistive, the H2 would be anti-phase with $\cos 2\omega_0 t$. Assuming that a realistic phase misalignment with $\cos 2\omega_0 t$ is θ_2

$$v_{\mathrm{gs}} = \pm A \sin\omega_0 t + A_2 \cos(2\omega_0 t + \theta_2) + n_{fA,B}. \tag{3}$$

The upconversion of $n_{fA,B}$ to high-frequency current noise in i_{ds1} is shown in Fig. 4(a).

1) Direct Upconversion: Plugging (3) into (2), the upconverted $1/f$ noise component in i_{ds1} around ω_0 (i.e., H1) is differential (as gathered by the $\pm$ sign)

$$i_{n1} = \pm G_{12} \sin\omega_0 t \cdot n_{fA,B} \mp G_{13} \sin(\omega_0 t + \theta_2) \cdot n_{fA,B} \tag{4}$$

where upconversion transconductances $G_{12} = 2a_2 A$ and $G_{13} = 3a_3 A A_2/2$. The first term in (4) is induced by the second-order nonlinearity. It is in-phase with the fundamental oscillation current signal and can only create amplitude noise. The second term in (4) is induced by the third-order nonlinearity. Decomposing $n_{fA,B}$ into CM and differential-mode (DM) components, its DM part clearly cannot introduce PN. For the

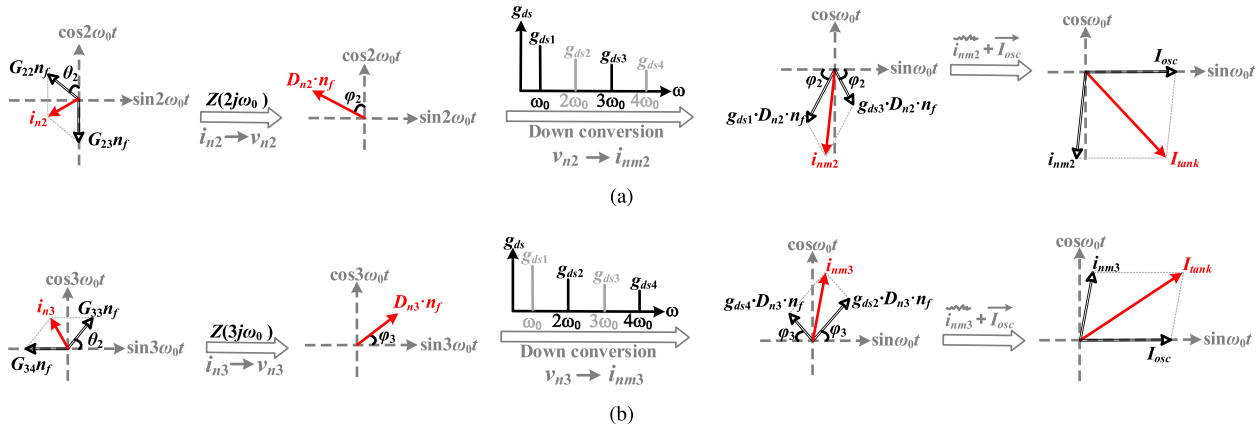


Fig. 5. Indirect conversion to PN from the upconverted flicker noise around (a) second harmonic frequency and (b) third harmonic frequency.

CM component, if $\theta_2 \neq 0$ or π, it directly induces PN [22], as shown in Fig. 4(b).

A large impedance at dc (e.g., an ideal current source) that is in series with the differential g_m-pair can suppress the $1/f$ noise in CM to some extent. Therefore, this DCO employs the tail current source, M_T. However, in 28-nm CMOS, the dynamic output impedance of transistors, $r_{\rm ds}$, is rather small. Also, the limited voltage headroom and large-signal operation push M_T close to, and momentarily into, the triode region, which further limits its $r_{\rm ds}$. Therefore, the $1/f$ upconversion to PN from $M_{A,B}$ is still significant.

With the relatively small tail-current impedance at dc, there are two possible ways to suppress the direct $1/f$ upconversion in $M_{A,B}$: 1) reducing G_{13} by minimizing the H2 voltage [i.e., A_2 in (3)] in $v_{\rm gs}$ of $M_{A,B}$, which essentially requires minimizing $Z_{\rm trans2}$ and 2) forcing $\theta_2 = 0$ or π by tuning the CM $Z_{\rm trans2}$ to resistive at H2.

2) Indirect Upconversion: The upconverted $1/f$ noise current around H2 (through second- and third-order nonlinearities) is CM

$$i_{n2} = -G_{23}\cos 2\omega_0 t \cdot n_{fA,B} + G_{22}\cos(2\omega_0 t + \theta_2)\cdot n_{fA,B} \quad (5)$$

where $G_{23} = a_3 A^2/2$ and $G_{22} = 2a_2 A_2$. This current flows into the CM impedance (annotated as Z_2) that connects the drain with source of cross-coupling transistors via the path from the LC tank through VDD–VSS supply rails to M_T, and induces a voltage swing at H2

$$v_{n2} = D_{n2} \cdot n_{fA,B} \cdot \cos(2\omega_0 t + \varphi_2) \quad (6)$$

where $D_{n2} = |Z_2 \cdot i_{n2}/n_{fA,B}|$ is the upconversion gain and φ_2 is the extra phase shift introduced by the reactive tank impedance at H2 in addition to the phase of i_{n2}. v_{n2} mixes with the fundamental and H3 components (differential) in $g_{\rm ds}(t)$ of $M_{A,B}$ and induces a channel noise current i_{nm2}

$$\pm n_{fA,B} \cdot [G_{x23} \cdot \sin(\omega_0 t - \varphi_2) - G_{x21} \cdot \sin(\omega_0 t + \varphi_2)] \quad (7)$$

where $G_{x21} = D_{n2} \cdot g_{\rm ds1}/2$, $G_{x23} = D_{n2} \cdot g_{\rm ds3}/2$, and $g_{\rm ds1}$ and $g_{\rm ds3}$ are the fundamental and H3 components in $g_{\rm ds}(t)$. Also, only the CM component in $n_{fA,B}$ will modulate the phase to create PN. This procedure is shown in Fig. 5(a).

The upconverted $1/f$ noise current around H3 (through the fourth- and third-order nonlinearities, respectively) is differential

$$i_{n3} = \mp G_{34}\sin 3\omega_0 t \cdot n_{fA,B} \pm G_{33}\sin(3\omega_0 t + \theta_2)\cdot n_{fA,B} \quad (8)$$

where $G_{34} = a_4 A^3/2$ and $G_{33} = 3a_3 A A_2/2$. It flows into the LC tank and induces differential voltage swing at H3

$$v_{n3} = \pm D_{n3} \cdot n_{fA,B} \cdot \sin(3\omega_0 t + \varphi_3) \quad (9)$$

where $D_{n3} = |Z_3 \cdot i_{n3}/n_{fA,B}|$, Z_3 is the tank impedance at H3, and φ_3 is the extra phase shift introduced by the reactive tank impedance at H3 in addition to the phase of i_{n3}. v_{n3} is mixed with the H2 and H4 components (CM) in $g_{\rm ds}(t)$ of $M_{A,B}$ and induces a channel noise current i_{nm3}

$$\pm n_{fA,B} \cdot [G_{x32} \cdot \sin(\omega_0 t + \varphi_3) - G_{x34} \cdot \sin(\omega_0 t - \varphi_3)] \quad (10)$$

where $G_{x32} = D_{n3} \cdot g_{\rm ds2}/2$, $G_{x34} = D_{n3} \cdot g_{\rm ds4}/2$, and $g_{\rm ds2}$ and $g_{\rm ds4}$ are the H2 and H4 components in $g_{\rm ds}(t)$. Again, only the CM component in $n_{fA,B}$ will modulate the phase to create PN. This procedure is also shown in Fig. 5(b). i_{nm2} and i_{nm3} are the current noises in $i_{\rm ds2}$.

In CMOS transistors, the higher order nonlinearities are much weaker than the lower order ones. Therefore, $a_4 < a_3 < a_2$ and $G_{33} < G_{22}$. Moreover, $g_{\rm ds2} < g_{\rm ds1}$ and $g_{\rm ds4} < g_{\rm ds3}$. Depending on the magnitude of reactive part in Z_2 and Z_3, contributions of the upconverted flicker noise i_{n2} and i_{n3} to the oscillator PN vary.

In order to reduce the indirect $1/f$ upconversion through self-mixing, there are two possible solutions: 1) the H2 and H3 noise voltage components in $v_{\rm ds}$ of $M_{A,B}$ (i.e., v_{n2} and v_{n3}) are minimized by suppressing the harmonic noise current in $i_{\rm ds}$ (i.e., i_{n2} and i_{n3}) or minimizing Z_2 and Z_3, and 2) φ_2 in v_{n2} and φ_3 in v_{n3} are forced to 0 by tuning the CM Z_2 and DM Z_3 to resistive. These requirements align with those in the direct upconversion mechanisms. Adding a tail filter LC tank resonating at H2 would suppress the H2 current [21]. However, the extra LC tank occupies a larger area. To avoid that, two other possible approaches can be applicable: 1) tuning Z_2 and Z_3 to be resistive by creating

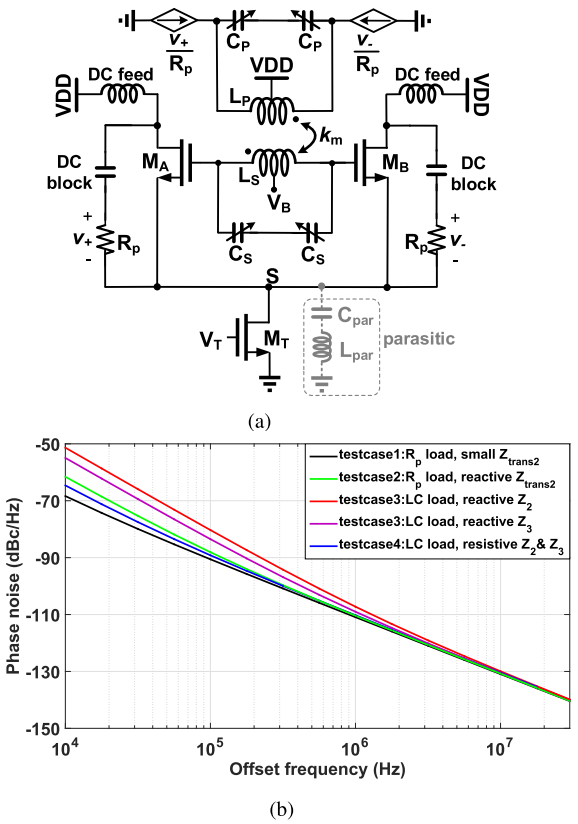


Fig. 6. (a) Testbench to avoid PN indirect upconversion from $1/f$ noise and (b) simulated PN with this and Fig. 2 testbenches.

resonances at H2 and H3 and 2) tuning the reactive Z_2 and Z_3 to be very small (e.g., very large capacitive or small inductive loading). Table I summarizes the direct and indirect $1/f$ noise upconversion mechanisms, as well as the corresponding suppressing solutions.

A circuit simulation testbench is introduced in Fig. 6(a) to validate the proposed theory. It is designed to oscillate at 20 GHz. The drain nodes of $M_{A,B}$ are electrically isolated from the LC tank's primary winding by means of a unidirectional signal flow. They are terminated with R_p, i.e., the tank impedance at ω_0. R_p is maintained much lower than the reactive impedance of $C_{\rm ds}$ in $M_{A,B}$. It ensures that the drain current ($i_{\rm ds}$) of $M_{A,B}$ only flows through resistive loads. The oscillation current is injected into the tank through an ideal voltage-controlled current source, whose transconductance is $1/R_p$. Z_2 and Z_3 are designed to be strongly reactive. Since the weak CM magnetic coupling in the 1:2 transformer greatly attenuates the H2 signal transferring from the primary (drain) to the secondary (gate) winding, $Z_{\rm trans2}$ is small when no parasitic appears in M_T or the VDD–VSS supply rails. In this case (test case 1), simulated PN shows that its $1/f^3$ corner is not visible (i.e., <10 kHz), as indicated by the black curve in Fig. 6(b). Varying the reactive impedance value of Z_2 or Z_3 (e.g., by means of single-ended and differential tank capacitors) has little effect on the $1/f^3$ corner. However, by adding a reactive impedance at H2 between node S and VSS ($L_{\rm par}$ and $C_{\rm par}$ to account for the parasitics in tail current and VDD/VSS supply rails) (test case 2), the reactive part in $Z_{\rm trans2}$ increases. It forces $\theta_2 \neq 0$ or π in (3) and so the simulated $1/f^3$ corner raises to 80 kHz. This validates the above-described direct upconversion mechanism.

A practical testbench is then configured as in Fig. 2 with the same 20-GHz LC tank and transistors as in Fig. 6(a) testbench. Parasitics in VDD–VSS supply rails are not included to keep $Z_{\rm trans2}$ small. When Z_2 or Z_3 is reactive (test case 3), its $1/f^3$ corner is 1 MHz or 450 kHz, respectively. Test cases 1 and 3 suggest that indirect upconversion through self-mixing is a major mechanism for the $1/f$ noise upconversion to PN. After tuning Z_2 and Z_3 to be resistive (test case 4), the $1/f^3$ corner drops to 30 kHz. Fig. 6(b) shows the simulated PN with different test cases. It confirms the proposed direct and indirect mechanisms.

In this design, the LC tank is tuned for the ancillary resonance at H3, and the H3 component is filtered out at $v_{\rm gs}$. This coincides with the criteria associated with H3. In the traditional single-resonance LC oscillators with reasonably high Q-factors, since H3 is far away from the resonance, the tank impedance at H3 is low. Therefore, the criterion for H3 can be easily satisfied. At H2, the direct and indirect upconversion mechanisms set up a criterion for the CM impedance in two paths: $Z_{\rm trans2}$ and Z_2. However, both the paths include the VDD–VSS routing path, which is vulnerable to parasitic inductance and capacitance in layout and difficult to estimate. This is especially true for inductors/transformers with an odd number of turns since the center-tap is on the opposite side of the terminals. In order to robustly define the CM H2 impedance, the VDD–VSS routing path should be bypassed.

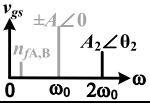
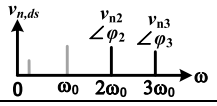
A generic technique to suppress the $1/f$ noise upconversion is proposed here and applied to this DCO. The schematic and layout implementation are revealed in Fig. 2. An extra series LC branch ($L_{\rm sh}$ and $C_{\rm sh}$) is introduced between VDD (transformer's center-tap) and a common-source node of $M_{A,B}$ (node S). Two conditions should be satisfied: 1) the impedance of this series LC feed resonates at H2 and 2) the LC network between the drain of $M_{A,B}$ and node S (i.e., Z_2) resonates at H2 in CM. Condition #1 bypasses the practically ill-defined path between VDD and node S with a short-circuit path at H2. Since the H2 current path is explicitly defined by this auxiliary LC branch, it is not subjected to any normal parasitic effects in the VDD/VSS routing. In this way, $Z_{\rm trans2}$ and H2 component in $v_{\rm gs}$ are ensured to be small due to the short path between node S and center-tap at H2. Therefore, condition #1 also prevents the $1/f$ noise upconversion through the direct conversion mechanism. Condition #2 ensures that H2 in $v_{\rm ds}$ is in-phase. It reduces the $1/f$ noise indirect upconversion through self-mixing. The respective solutions to suppress the direct and indirect upconversion in the proposed technique are also summarized in Table I. This idea provides an extra design freedom for the $1/f$ noise upconversion reduction at no cost of area or power.

IV. 20-GHz Component Suppression

The proposed PLL is intended for a wireless transceiver. In such a case as in many others, the undesired 20-GHz tone should be sufficiently attenuated to lie well

TABLE I

SUMMARY OF DIRECT AND INDIRECT $1/f$ NOISE UPCONVERSION MECHANISMS AND THE SOLUTIONS

Mechanism	Root cause	Possible solutions	Design choices	Implementation in this work
Direct conversion	out-of-phase harmonics in v_{gs} 	minimize A_2	minimize Z_{trans2}	extra series LC resonance at H2 for explicitly defined CM path; weak CM magnetic coupling at H2 in transformer
		tune θ_2=0	tune Z_{trans2} resistive	N/A
Indirect conversion	out-of-phase upconverted $1/f$ noise at H2 and H3 in v_{ds} 	minimize v_{n2} and v_{n3}	minimize noise current at H2 and H3	N/A
			minimize Z_2 and Z_3	N/A
		tune φ_2=0 and φ_3=0	tune Z_2 and Z_3 resistive	extra series LC resonance at H2 for explicitly defined CM path; Z_2 and Z_3 resonate at H2 and H3

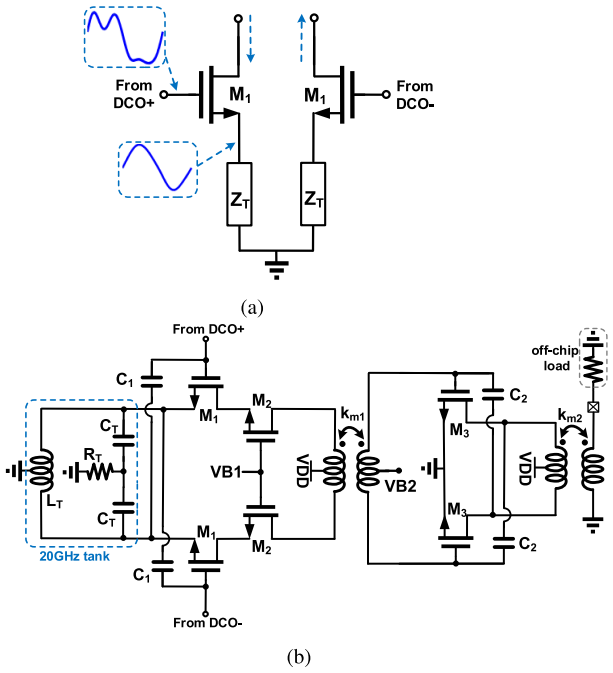


Fig. 7. (a) Working principle and (b) schematic of 60-GHz buffer with 20-GHz suppression.

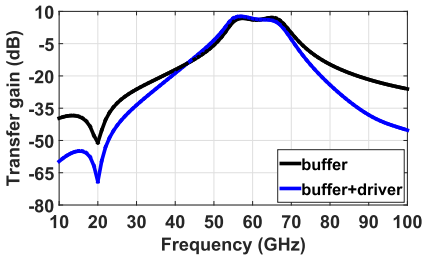


Fig. 8. Simulated transfer gain of the 60-GHz buffer stage and combined buffer and driver stage.

below the spectrum mask of a transmitter or to meet the blocker tolerance of a receiver. To get a "pure" spectrum at the 60-GHz carrier output, the 20-GHz fundamental DCO tone should be suppressed in the 60-GHz buffer path. To achieve this effect, we propose a cancellation scheme of this 20-GHz component. Fig. 7(a) reveals the core idea in which the source of the buffer's input transistor (M_1) follows the DCO's 20-GHz component, but sees the ground at 60 GHz. This requires a large impedance at 20 GHz, but a very low impedance (ideally zero) at 60 GHz. A parallel LC tank that resonates at 20 GHz is therefore placed between the source of M_1 and ground, as shown in Fig. 7(b). At 20 GHz, M_1 is source-degenerated by a large impedance provided by the 20-GHz tail tank. There should be no 20-GHz current flowing in M_1, and there is no g_m gain. The LC tank has a very low impedance ($<10\ \Omega$) at 60 GHz, and hence, the desired 60-GHz input signal experiences large g_m.

Compared with the conventional notch filter solutions [23], the proposed suppression technique offers several advantages. It achieves a better 20-GHz component rejection ratio. The 20-GHz signal gain is

$$\frac{G_m \cdot Z_{\text{load}}(j\omega_0)}{1 + G_m \cdot Z_{\text{tail}}(j\omega_0)} \tag{11}$$

where G_m is the transconductance of M_1/M_2. For typical circuit parameters that are used in this design, the tail tank suppresses the transconductance gain by 17 dB at 20 GHz. Together with the passive matching network loading the M_1/M_2 stage, this 60-GHz buffer provides a 50-dB suppression at 20 GHz. With the same LC elements as in the tail tank for constructing a conventional notch filter, this solution would suppress the 20-GHz signal by 40 dB. Across the frequency range, the proposed technique offers 7–11 dB of better suppression at 20 GHz than the notch filter, while the 60-GHz gain is almost the same.

Since the capacitive source degeneration at high frequencies in M_1 may cause stability concerns, neutralization capacitor C_1 is added differentially between the gate and source to ensure DM stability. A dampening resistor $R_T = 10\ \Omega$ is inserted between the common node of the tail tank capacitors C_T and ground to ensure a CM stability. A simulated stability factor shows that this buffer is unconditionally stable. The buffer is followed by an output driver to deliver >0 dBm for measurements. Loosely coupled transformer ($k_{m1} = 0.25$) is used for wideband interstage matching. As shown in Fig. 8, across the frequency range, the buffer stage alone provides -43- to -51-dB suppression of the 20-GHz component and 6$\sim$7-dB gain of the 60-GHz input while achieving 13-GHz

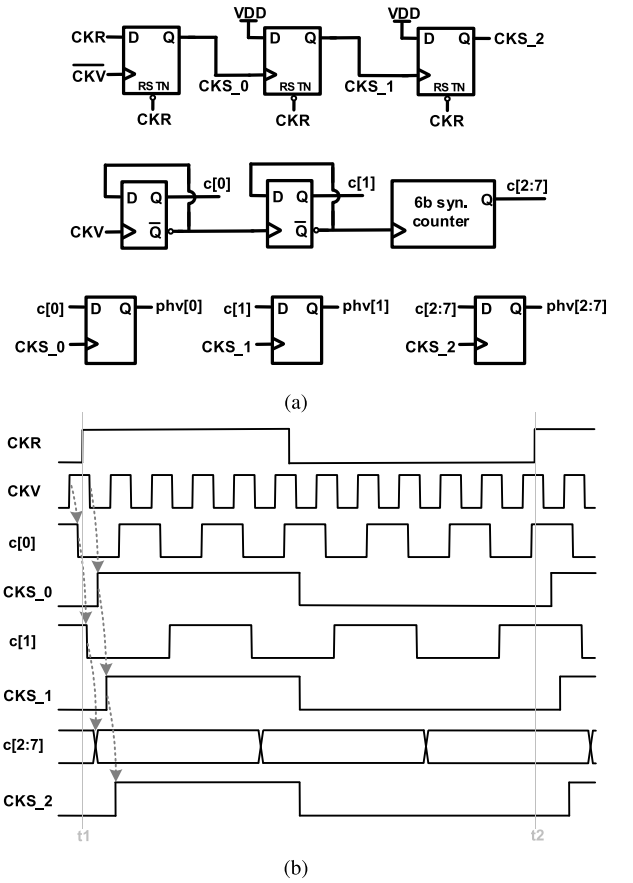


Fig. 9. (a) Block diagram and (b) timing sequence of the asynchronous high-speed counter.

(22%) BW. Including the output driver, the two stages provide −70-dB suppression at 20 GHz, as also shown in Fig. 8.

V. Phase Detection

In this design, an 8-bit variable-phase high-speed counter, PHV_I, and a noise-shaping DTC-assisted TDC act as the phase detector. As a tradeoff between power consumption and design complexity, the 2-LSB integer bits are handled by an asynchronous counter to support the high speed at low power, the remaining 6-MSB bits are handled by a synchronous counter. Timing for reading out the combined counter output is critical due to its asynchronous and high-speed nature. Due to the staggered settling of the counter's LSB bits, extreme care must be taken to guarantee the proper sampling of PHV_I by the CKR clock edge, especially over process, voltage and temperature variations (PVT). Any misalignment between various bits or metastability will result in catastrophic phase jumps and thus a failure in locking.

To ensure robust operation, an asynchronous sampling scheme is used in the high-speed counter readout. Fig. 9 shows the circuit diagram and timing sequence. A specific case is also demonstrated in Fig. 9(b), in which the counter output bits c[1:7] are not yet settled at the CKR rising edge t_1. In the proposed solution, the CKV-to-Q delay for each asynchronous bit is added on to the respective sampling clock. The falling edge of CKV samples CKR and generates the sampling clock CKS_0 for bit $c[0]$. The delay between the rising edge of

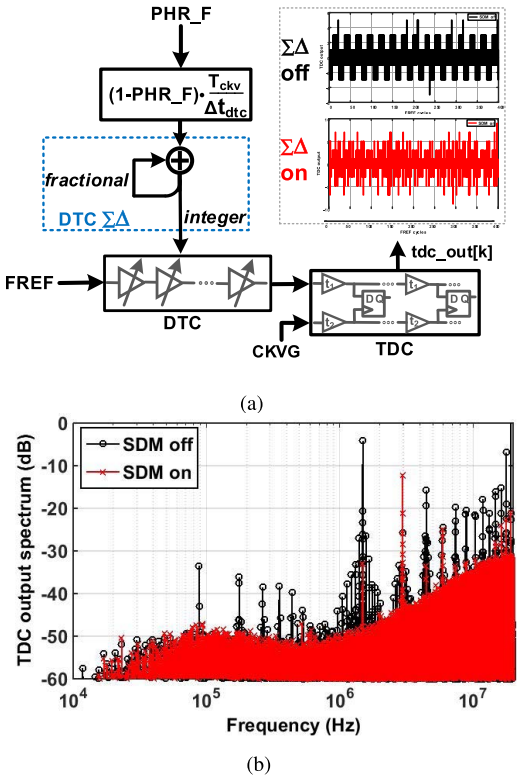


Fig. 10. (a) Circuit diagram and output pattern of the DTC–TDC and (b) simulated TDC output spectrum with ΣΔM ON/OFF.

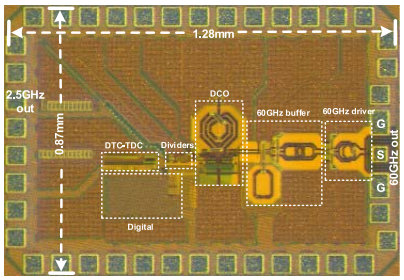


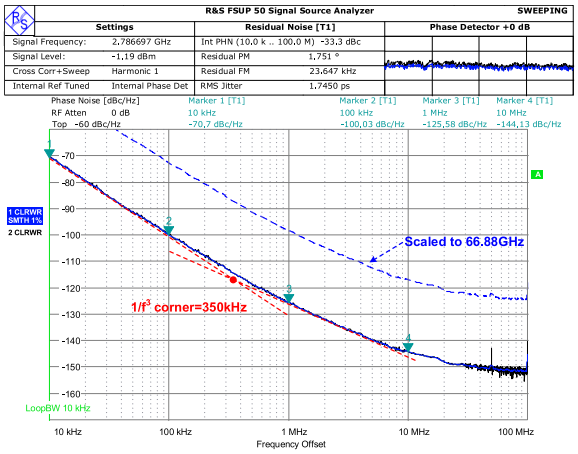
Fig. 11. Chip micrograph of the proposed 60-GHz ADPLL.

CKS_0 and $c[0]$ is exactly half the CKV period if the D flip-flops have the same delay. The rising edge of CKS_0 samples VDD and generates CKS_1, the sampling clock for bit $c[1]$. The sampling clocks for all the other asynchronous bits are generated in this manner. In this way, the delay in asynchronous bits also propagates in the respective sampling clocks. It ensures that each sampling clock always appears half CKV period after the counter bit is settled. The counter output can be robustly read out in each cycle with this asynchronous sampling technique.

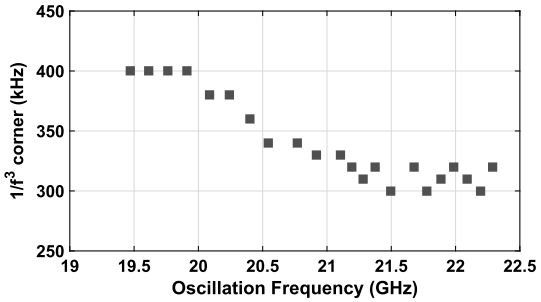
A 64-stage DTC with 12-ps resolution is based on current-starved delay-cells. This helps to reduce the required detection range of the TDC. A 64-stage 2.7-ps fine-resolution TDC uses a Vernier line and ensures that its quantization (Q)-noise level is comparable to the FREF noise floor. It is well known that the DTC/TDC Q-error and nonlinearity can introduce spurious tones. An error-feedback ΣΔ modulation (ΣΔM) is introduced to the DTC, as highlighted in Fig. 10(a). It eliminates the spur induced by the Q-error from DTC–TDC

TABLE II
COMPARISON OF THE DCO WITH RELEVANT STATE-OF-THE-ART

		Shi ASSCC15	Vigilante JSSC18	Zong JSSC16	Guo SSCL18	Cherniak ISSCC18	Szortyka JSSC16	This work
Osc. Freq. (GHz)		23.5-27.3 (15%)	16.1-19.8 (20.6%)	16.1-20.8 (25%)	25.3-29.5 (15.7%)	20.4-24.6 (18.7%)	53.8-63.3 (16%)	19.1-22.4 (15.6%)
$1/f^3$ Corner (kHz)		3000	2000	1000	550	NA	1000-4000	300-400
PN (dBc/Hz)	100kHz	-74.6	NA	-81.5	-80.5	NA	-63~-67	-82.1
	1MHz	-101.5	-108	-109.5	-108.7	-102	-91~-94.5	-107.5
P_{DC} (mW)		7.2	75-87.6	13.5	6.6	10	14	17
FoM (dBc/Hz)	100kHz	174	NA	175.9	181.4	NA	-167.6~-170	177.2
	1MHz	180	174	183.9	189.6	178.8	-175~-177.7	182.2
CMOS (nm)		28	28	40	65	65	40	28
No. of inductors		2 (tail filtering)	2	1	3	2 (tail filtering)	2 (tail filtering)	1
Type		VCO	VCO	VCO	VCO	VCO	VCO	DCO



(a)



(b)

Fig. 12. (a) Measured DCO PN at dividers output and scaled up to 66.9 GHz. (b) Measured DCO $1/f^3$ noise corner over TR.

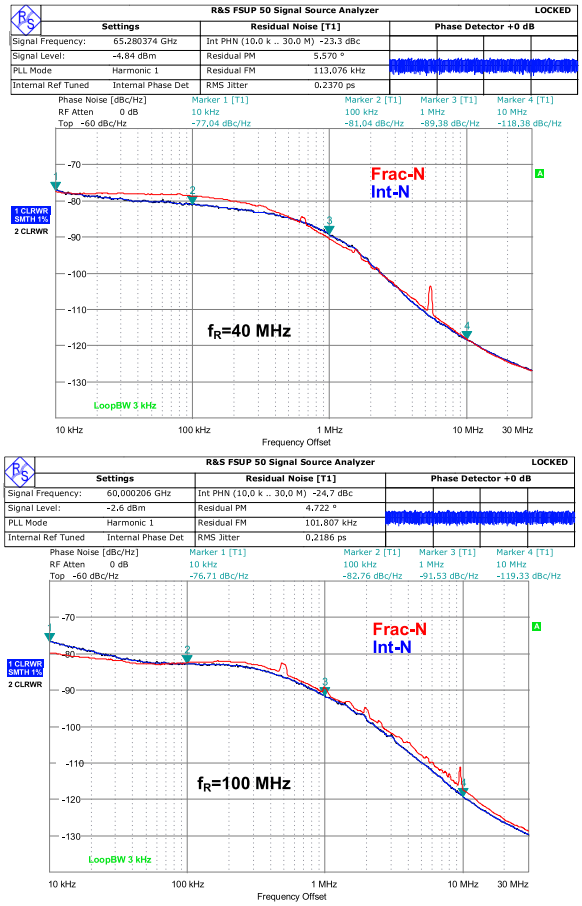


Fig. 13. Measured ADPLL PN with $f_R = 40$ and 100 MHz at integer-*N* and fractional-*N*.

and by the nonlinearity of the TDC. $\Sigma\Delta$M shapes the DTC Q-noise to high frequencies, which is then filtered by the LF. Moreover, the TDC input is scrambled by the preceding $\Sigma\Delta$M-DTC, such that the TDC Q-error and nonlinearity will not induce spurious tones. With the DTC $\Sigma\Delta$M ON/OFF, the respective TDC outputs are read out in the PLL close-loop simulations. Fig. 10(b) shows the corresponding frequency spectrum. As we can see, the low-frequency tones at the TDC output disappear or are suppressed below the noise in the system when the $\Sigma\Delta$M is ON. The remaining spurs are caused by the nonlinearity in the DTC and limited cycle output of the $\Sigma\Delta$ modulator. They are attenuated by the following LF.

VI. EXPERIMENTAL RESULTS

The proposed 60-GHz digital fractional-*N* frequency synthesizer is prototyped in a 28-nm 1P9M LP CMOS. Fig. 11 shows the chip micrograph. The design occupies a core area of 0.38 mm^2, while the total chip area (including pads) is 1.1 mm^2. The PN and spectra of the generated 60-GHz carrier are measured via on-wafer probing. Outputs of the 2.5-GHz frequency dividers could also be conveniently monitored.

TABLE III
COMPARISON OF THE 60-GHz FRACTIONAL-*N* ADPLL WITH RELEVANT STATE-OF-THE-ART

		ISSCC'09 Scheir	JSSC'11 Musa	JSSC'16 Siriburanon	ISSCC'13 Yi	JSSC'14 Wu	JSSC'15 Szortyka	ISSCC'18 Huang	JSSC'17 Hussein	**This Work**	
Architecture		Analog PLL	20G PLL + 60G QILO	20G SSPLL + 60G QILO	Analog PLL	ADPLL	SSPLL	ADPLL	ADPLL	**ADPLL**	
Type		INT-N	INT-N	INT-N	INT-N	FRAC-N	INT-N	FRAC-N	FRAC-N	**FRAC-N**	
Output frequency (GHz)		57-66 (14.6%)	58-63 (8.3%)	58.3-64.8 (10.5%)	58-68.5 (8.3%)	56.5-63.5 (11.6%)	53.8-63.3 (16.2%)	82-107.6 (27%)	50.2-66.5 (28%)	57.5-67.2 (15.6%)	
Ref. frequency (MHz)		100	36	40	135	100	40	125	100	40	100
PN (dBc/Hz)	In-band	-70	-60	-75	NA	-75	-88~ -92	-84~ -87	-79~ -83	-77~ -81	-81~ -84
	1MHz	-75	-95	-92	-89.8~ -91.5	-90	-88~ -92	-81	-88~ -94.5	-89~ -92	
RMS jitter (fs)	Integer channel	NA	NA	290	238	590.2	200	276~328	223~302.5	**236~266**	**213~241**
	Fractional channel								962~1540	**236~316**	**213~277**
V_{DD} (V)		1.1	1.2	1	1.2	1.2	1	1.2/0.8	1	1.05	
P_{DC} (mW)		78	80	32	24.6	48	42	35.5	46	**28.6 + 10.5 ***	**31 + 10.5 ***
FoM # (dB)	Integer channel	NA	NA	-235.7	-238.5	-227.8	-237.7	-234~ -235.7	-233.8~ -236.4	-235.6~ -236.6 *	-236.2~ -237.2 *
	Fractional channel								-219.6~ -223.7	**-234~ -236.6 ***	**-235~ -237.2 ***
Reference spur (dBc)		-42	<-47	-38	-54.5	-74	<-40	-34~ -52	NA	-62	-65
Area (mm^2)		0.82	1.68	1.09	0.19 **	0.48 **	0.16 **	0.36 **	0.45 **	1.1 (core area is 0.38)	
CMOS technology (nm)		65	65	65	65	65	40	65	65	28	

*: include the power consumption of the 60GHz output buffer stage (10.5mW)
**: only include the core chip area
#: $\text{FoM} = 10 \cdot \log_{10}\left[\left(\frac{\text{Jitter}_{\text{rms}}}{1\text{s}}\right)^2 \cdot \frac{P_{DC}}{1\text{mW}}\right]$

The ADPLL is first set to an open-loop mode for the DCO performance measurements using an R&S FSUP50 Signal Source Analyzer. The TR of the DCO is 57.5–67.2 GHz, covering all four 802.11ad channels (58.32, 60.48, 62.64, and 64.8 GHz) with sufficient margin. The DCO draws 19 mA from a 0.9-V supply. PN of the free-running DCO is measured after the frequency dividers (CKV point in Fig. 1), as shown in Fig. 12(a). The PN referred to the 66.88-GHz carrier is -98 dBc/Hz at 1-MHz offset. Across the TR, the $1/f^3$ noise corner varies between 300 and 400 kHz, as shown in Fig. 12(b). The slightly higher $1/f^3$ corner at lower oscillation frequencies is expected to be caused by the possible misalignment between the auxiliary resonances at H2/H3 and the fundamental frequencies. With more accurate EM modeling, it can be further improved. The DCO performance is compared with the state-of-the-art oscillators at 20 and 60 GHz, as shown in Table II. The $1/f^3$ corner is the lowest. A better figure-of-merit (FoM) is reported in [30], at the cost of two extra inductors in the resonator.

The ADPLL is separately measured with different external crystal reference clocks of $f_R = 40$ and 100 MHz, at which it respectively consumes 28.6 and 31 mW (17 mW for DCO and 9.5 mW for frequency dividers). The 60-GHz buffer and 50-Ω-load driver stage consume 10.5 and 11.5 mW, respectively. All the circuit blocks (except for DCO) are supplied at 1.05 V (i.e., the nominal voltage for this technology). The ADPLL PN is measured with R&S FSUP50 with an extension V-band harmonic mixer for downconversion. The loop BW is programmed to 200–300 kHz for the lowest rms jitter. PN at an integer-N channel and a fractional-N channel is shown in Fig. 13. With 40-MHz FREF, the rms jitter integrated from 10 kHz to 30 MHz is 237 fs at 65.28 GHz (integer-N) and 268 fs at 65.411 GHz (fractional-N). With the 100-MHz reference, the in-band PN and rms jitter are substantially improved. Fig. 14(a) shows the spectrum at 65.411 GHz with DTC $\Sigma\Delta$M ON (in red line) and OFF (in blue line). When $\Sigma\Delta$M is engaged, the fractional spurs are significantly attenuated, and the highest spur level observed at this carrier frequency is -51 dBc. The effect of DTC $\Sigma\Delta$M on the ADPLL PN is examined in Fig. 14(b). As we can see, the PN between 1–10 MHz has been slightly increased by <1.5 dB. The degradation on IPN is only 0.3 dB. It is even smaller with 100-MHz FREF.

The measured rms jitter across the fractional frequency command word (FCW) offsets away from the 60-GHz integer-N channel and with the 40- and 100-MHz references is summarized in Fig. 15(a). With $f_R = 40$ MHz, the measured rms jitter is 236∼266 and 236∼316 fs, respectively, across the integer-N (all swept) and fractional-N settings. With $f_R = 100$ MHz, the rms jitter is improved to 213∼241 and 213∼277 fs across the respective channels. Fig. 15(a) reveals that the rms jitter improves at some special fractional FCWs (such as 0.125, 0.25, and 0.5) with $f_R = 40$ MHz, while this reduction becomes smaller with $f_R = 100$ MHz. With these fractional FCWs, the TDC quantization error is not uniformly distributed, and its contribution to the ADPLL PN decreases.

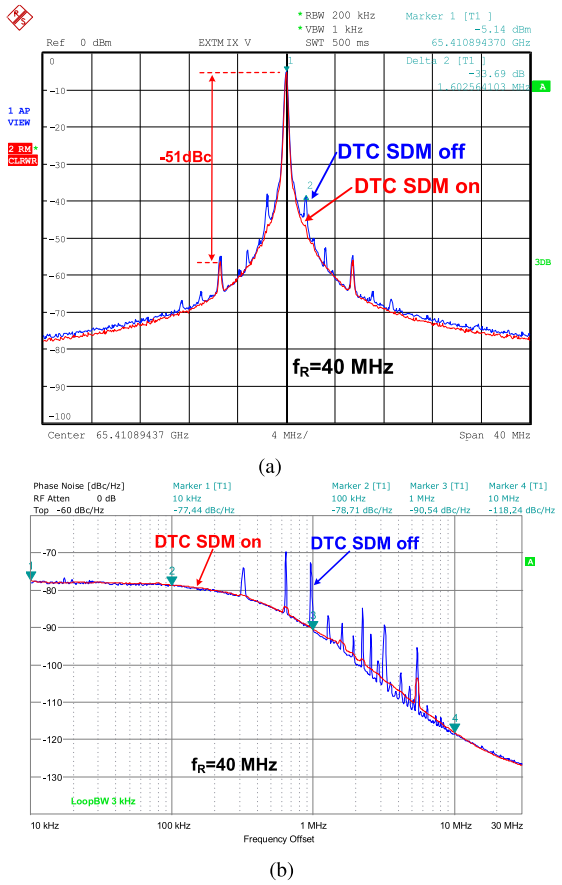


Fig. 14. Measured ADPLL output (a) spectrum and (b) PN with DTC $\Sigma\Delta$M ON/OFF.

This causes the drop in the rms jitter in case of $f_R = 40$ MHz. Since the uniformly distributed TDC quantization noise with $f_R = 100$ MHz is already a marginal contributor (4 dB below the FREF noise) to the ADPLL PN, the aforementioned effect exhibits less impact on the rms jitter. Fractional spurs are measured at the 2.5-GHz divider output with DTC $\Sigma\Delta$M enabled, and scaled to the corresponding 60-GHz frequencies. The fractional spurs across different fractional settings are summarized in Fig. 15(b). At 2.5-GHz divider output, the fractional spurs are measured <-57 dBc. When referring to the 60-GHz carrier frequencies, they are below -30 dBc. It should be noted that only a few papers report fractional spur levels at mmW frequencies. In [8], the spur levels appear to have been incorrectly taken from PN plots without accounting for the resolution BW. In [10], with the sophisticated DTC nonlinearity calibration, a lower fractional spur of -38 dBc (normalized to 60 GHz) was achieved. There is no DTC/TDC nonlinearity calibration done in our design, but it can be applied if the spurs need further suppression in some applications. Random dithering in $\Sigma\Delta$M [31] can also reduce part of the spurs.

The output power level at the 60-GHz carrier and the leaked 20-GHz tone are measured to validate the effectiveness of the 20-GHz tone suppression technique. After de-embedding cable losses, the driver delivers 1 dBm at 60 GHz to the external 50-Ω load, with $\pm$1-dB variation across the TR (see Fig. 16). The 20-GHz residual level is within $-51 \sim -57$ dBm across the TR. The achieved harmonic rejection ratio is 20 dB better compared with the notch filter solution in [23]. The 40-GHz

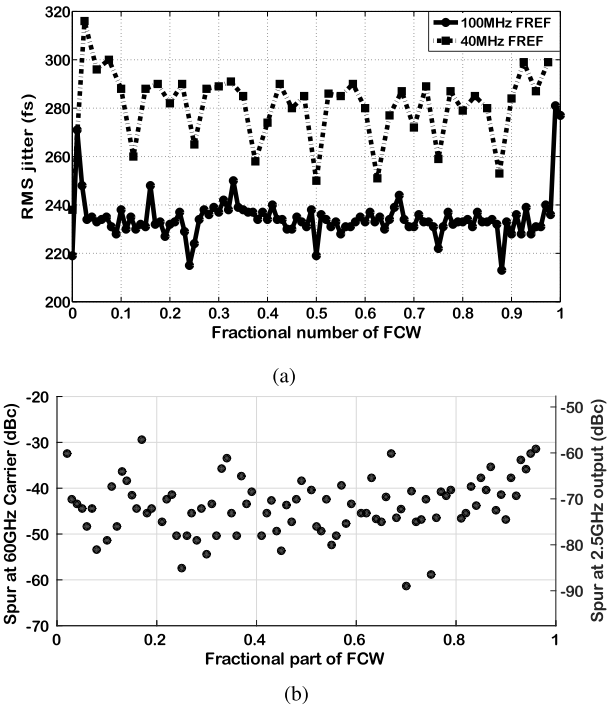


Fig. 15. Measured ADPLL (a) rms jitter and (b) worst case fractional spurs, across fractional offsets from 60.0-GHz integer-*N*.

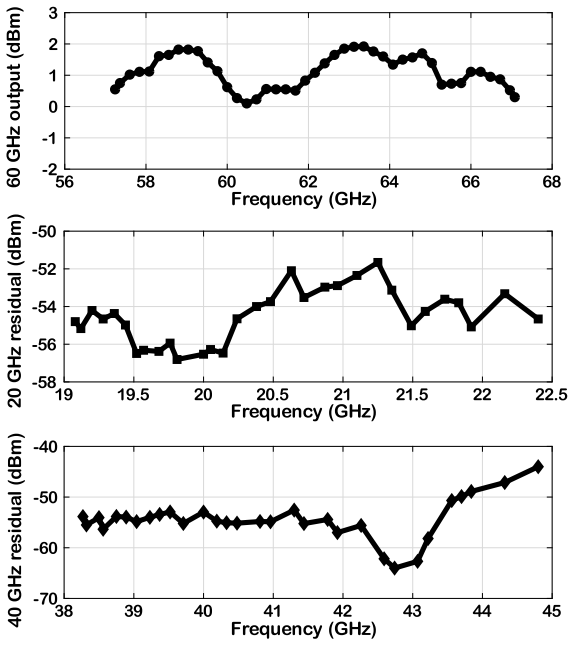


Fig. 16. Measured power across the TR at 60-GHz carrier and 20- and 40-GHz residual.

tone, which is caused by the nonlinear effects in the buffer stage, is measured at $-44 \sim -64$ dBm across the TR.

Table III summarizes the performance of the proposed 60-GHz ADPLL and compares it with the relevant state-of-the-art PLLs at 60 GHz or above. Only three fractional-*N* PLLs at 60 GHz or above are found in the literature. The rms jitter of our ADPLL is the best compared with the other fractional-*N* counterparts while consuming the lowest power. The FoM

improves the state-of-the-art by 1.5 dB at the fractional-N operation, even with including the power consumption of the 60-GHz buffer stage.

VII. Conclusion

A low-noise 60-GHz digital fractional-N frequency synthesizer is demonstrated. A low PN DCO and moderate loop BW are adopted to relieve the demand on fine-resolution TDC. Owing to the co-generation of 20- and 60-GHz signals, power-hungry mmW frequency dividers or multipliers are avoided. $1/f$ noise upconversion mechanisms are comprehensively investigated, and a $1/f^3$ suppression technique is proposed. It leads to a $1/f^3$ corner of 300–400 kHz, which is the best reported at mmW. The TDC–DTC pair with 2.7-ps resolution achieves optimal power efficiency, while $\Sigma\Delta$M in DTC helps to reduce fractional spurs. The undesired 20-GHz tone is suppressed by 50 dB in the 60-GHz buffer with a tail tank. Prototyped in 28-nm CMOS, the ADPLL exhibits 213-fs rms jitter and achieves the best power efficiency (FoM) among the fractional-N PLLs at 60 GHz.

Appendix

In large-signal operation, the total drain current ($i_{\rm ds}$) of the g_m-devices can be separated into three parts: $i_{\rm ds1}$, $i_{\rm ds2}$, and $i_{\rm ds3}$. They are given by

$$i_{\rm ds1} = \begin{cases} I_0 \cdot \exp(v_{\rm gs}/V_T), & \text{subthr.} \\ \dfrac{K}{2} \cdot (v_{\rm gs} - V_{\rm TH})^2, & \text{satur.} \\ K \cdot \left[(v_{\rm gs} - V_{\rm TH}) V_{\rm DS0} - \dfrac{1}{2} V_{\rm DS0}^2 \right], & \text{triode} \end{cases}$$

$$i_{\rm ds2} = \begin{cases} 0, & \text{subthr.} \\ \dfrac{K}{2} \cdot (v_{\rm gs} - V_{\rm TH})^2 \cdot \lambda \cdot v_{\rm ds}, & \text{satur.} \\ K \cdot (v_{\rm gs} - V_{\rm TH})(v_{\rm ds} - V_{\rm DS0}), & \text{triode} \end{cases}$$

$$i_{\rm ds3} = \begin{cases} 0, & \text{subthr.} \\ 0, & \text{satur.} \\ -\dfrac{K}{2} \cdot (v_{\rm ds} - V_{\rm DS0})^2, & \text{triode} \end{cases}$$

where $V_{\rm DS0}$ is the instantaneous drain–source voltage when the g_m-devices transition from saturation to triode region, $K = \mu C_{ox}(W/L)$, and $i_{\rm ds} = i_{\rm ds1} + i_{\rm ds2} + i_{\rm ds3}$. $V_{\rm DS0}$ is a fixed dc voltage in a steady-state oscillation. $i_{\rm ds1}$ is a nonlinear continuous function of $v_{\rm gs}$. Strong nonlinear behaviors in MOSFETs can be captured by the modified Volterra series [32]. In this case, the nonlinearity is static in the $i_{\rm ds1}$ equation and can be represented by (2).

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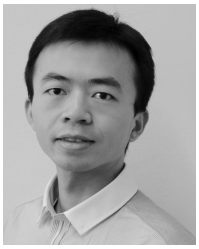

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