170-GHz Power Amplifier in 0.13-µm SiGe BiCMOS

By

X.Tong

4788370

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Supervisor:	dr. Marco Spirito
Thesis committee:	dr. Morteza Alavi,
	Prof. dr. Nuria Llombart,
	ir. E.S. Malotaux

Abstract

In recent years, the demand for the wireless connectivity is increasing and leads to the research into the above 100GHz design. Developments have been made with the circuit and technologies to make the circuit operate at 100GHz. The current availability of silicon-based technologies providing devices with *ft*/*f*max frequencies exceeding 300-GHz allows targeting above 100GHz for commercial telecom links.

The project presents an automated design approach that utilizes “Ocean” and “Skill” code to automate parts of the design flow of the mm-wave power amplifier. The Ocean script, the scripting language used by the cadence environment to control the simulations, together with Matlab is applied for data handling and to automate lots of the recurring simulations. The Skill-code, which under the cadence’s environment is applied to automatically generate the tunable layouts to realize a DRC conform circuit design.

The design of a 170-GHz Power Amplifier in 0.13-µm SiGe BiCMOS applied the automation design flow is presented in this thesis. The gain-stage characteristics such as gain, stability, power-added-efficiency, saturated output power or 1dB-Compression are automatically generated and plotted. Specifically, this 170-GHz PA achieves a 15dB power gain and 11.7dBm output 1dB compression point.

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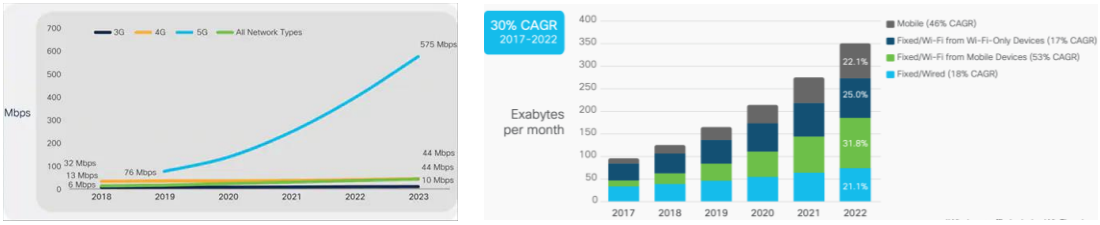
Chapter 1.
Introduction

1.1. The data throughput challenge

The upcoming generation of telecom systems (i.e., 5G) is being conceived to provide faster data down- and up-load speeds (Figure 1.1a) and an overall increase in mobile system data capacity (Figure 1.1b).



a) b)

Figure 1.1: The upcoming generation of telecom systems a) Global mobile average speeds by network type [1], b) Wireless data growth forecast [2].

Nevertheless, when looking at the data requirement forecasts for the coming decade also the high performance of the up-coming generation seems to be completely inadequate to face the challenges set by the future traffic communication mostly when machine to machine (M2M) data are included.

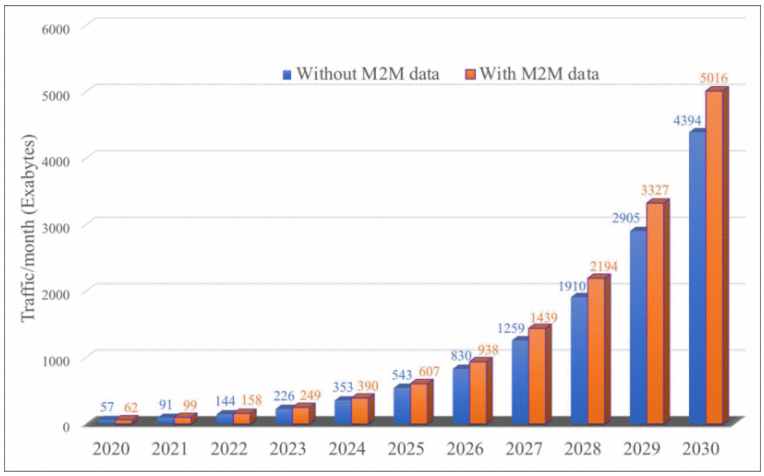


Figure 1.2: Global mobile data traffic forecast by ITU [3]

For this reason research centres worldwide and the developers of standards related to the future communication systems (i.e., 6G) are looking beyond the 100GHz frequency frontier to enable the usage of the widely available mm-wave spectrum, to support the data rates required by the next future. The wireless links in these higher frequency band can provide a wide bandwidth and thus can achieve high-data rate wireless communication, and high rate in both front haul and back haul [4] applications. Compared to wireless links below 100GHz, i.e., E-band (71GHz to 86GHz) backhaul systems [5], the links operating above 100GHz, i.e. W-band (92GHz to 114.25GHz) and D-band (130GHz to 174.8GHz) system, are challenged by the transmit (Tx) power requirements realize these future communication links, which is bounded by the maximum oscillation frequency of state of the art RF technologies.

To make circuits operating at a frequency above 100GHz possible, some developments have been made on device level (i.e., technology performance) and circuit standpoint (i.e., architectures and design methodologies). From the point of view of the device, some techniques are developed to maximize the performance of the device. Opposite to low-frequency design, parasitic components, such as parasitic inductors, resistors and capacitors, are not negligible for above 100GHz design. Thus, several techniques at every interconnect level also at the device levels are required to improve the maximum oscillation frequency of the device to meet the requirement of above 100GHz design.

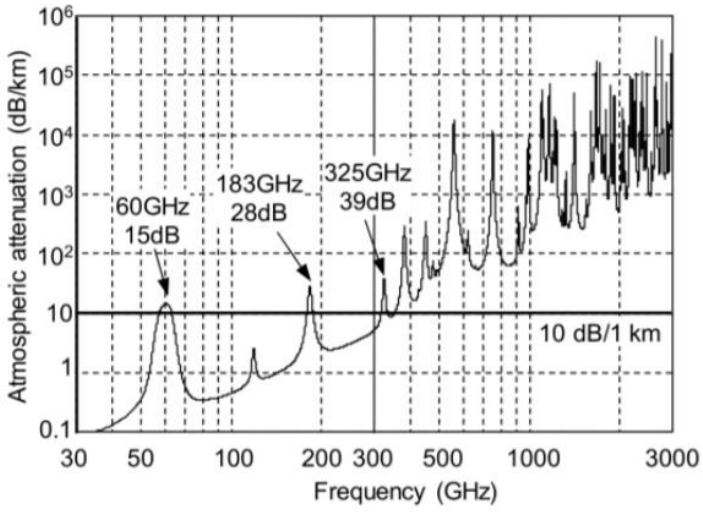


Figure 1.3: Attenuation in dB/km [6]

There are several frequency bands whose allocation for wireless communications is envisioned between 100 GHz to 275 GHz. These are selected based on the transmission loss due to atmospheric absorption when those are lower than 10dB/km [7] in these frequency band and example of these are the W-band and the D-band which are respectively located between 95 GHz – 114GHz and 130 GHz–174 GHz. it is important to keep the transmission loss lower than 10dB/km to guarantee the outdoor communication quality. In this project, the frequency band will be targeted from 167GHz to 175GHz [8].

1.2. Application and design goals

Considering the simplified block scheme of an IQ based TX module this project focuses on the design methodology to design, optimize and layout the power amplifier (PA) based on accurate targeting component specifications from the system level analysis.

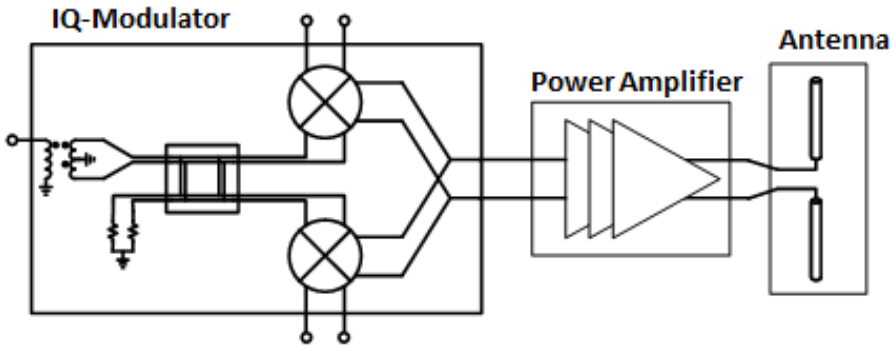


Figure 1.4: Simplified scheme block of a generic TX module based on an IQ up-converter, power amplifier and radiating antenna

In order to derive a specific user case and employ pre-defined system level specifications the targeted power amplifier is chosen to be part of an envisioned sub-

mm-wave wireless link spanning part of the campus of the Delft University of Technology as shown in Figure 1.5.

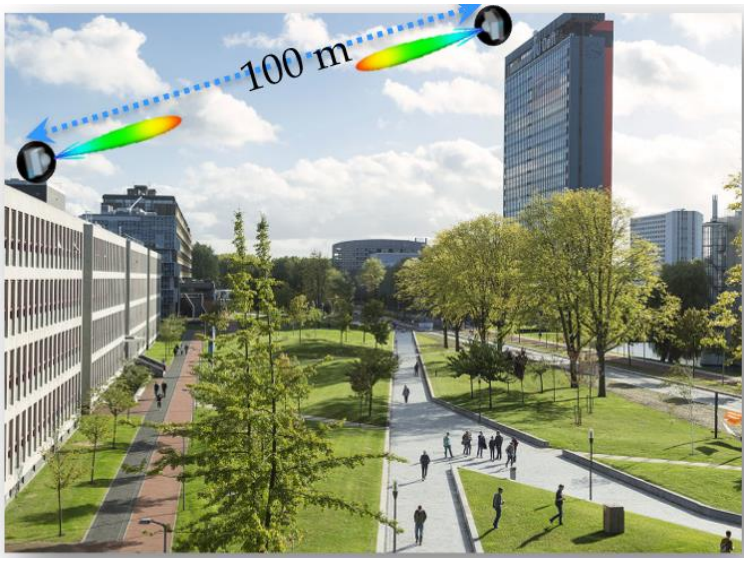


Figure 1.5: TU Delft envisioned 170 GHz point to point link based on the Fly's Eye concept, providing the test case for the specifications of this project

This work presented in this thesis targets a PA design, providing a -3dB operation frequency band from 167GHz to 175GHz to reach a 100 Gbit/s capacity requirement [8] as shown in Figure 1.6, using IHP's 130-nm SiGe BiCMOS technology. This technology was chosen as it provides a sufficiently high unity gain frequency and maximum oscillation frequency to allow performance beyond 100 GHz. The specification received for this project are given in Table 1.

Table 1 Design specification

Specification	Symbol	Unit	Value
Frequency	fc	[GHZ]	170
Bandwidth	BW	[GHz]	7
Gain[dB]	G	[dB]	15
1dB Compression Point	P_{1dB}	[dBm]	12
Saturated Output Power	P_{sat}	[dBm]	14
Peak Power added efficiency	PAE	[%]	10

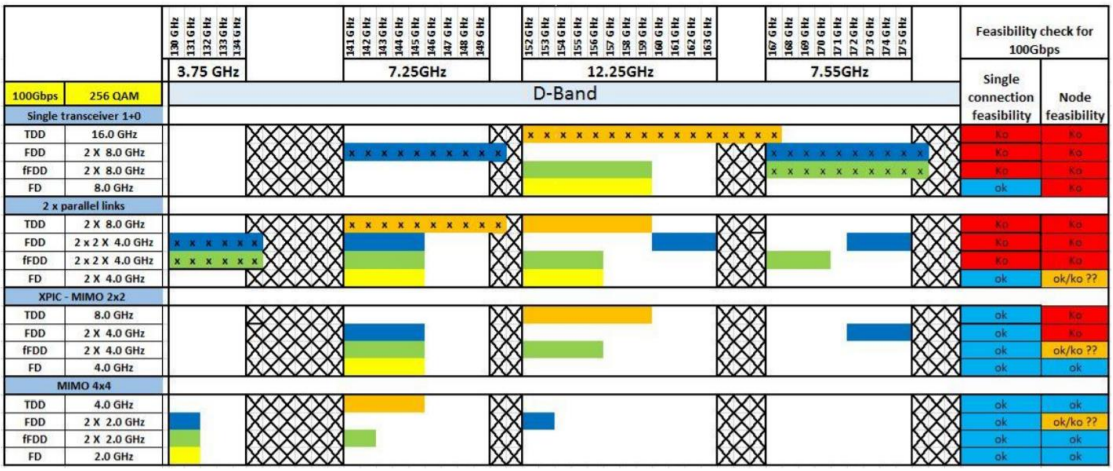


Figure 1.6: Analysis for 100 Gbit/s & 256-QAM solutions in D-band [8]

1.3. Outline of the thesis

The research question that lies at the base of this thesis project can be formulated as:

> *Define an analysis and design methodology for power amplifier operating in the deep mm-wave band (i.e., 170 GHz) providing a structured automated flow capable of being simply mapped to various technology nodes and including all the steps from circuit performance implementation up to, and including, design rules checking (DRC) compliant layout generation.*

As a by-product the goal of this work is also to provide a in depth documentation of the design steps, which is embedded in the usage of a coded approach, to potentially reduce start-up and design time for future designs.

The outline of this work is as follows:

Chapter 2 starts with identifying and describing the common performance metrics of a power amplifier. After this it provides a brief literature survey which is used to identify the design that can serve as both design examples and benchmark circuit to which the design presented in this work can be compared. Then

Chapter 3 describes the design flow of power amplifiers and the current CAD tools which help with the power amplifier design.

Chapter 4 attempts to identify steps that have to be performed multiple times during the design, because one needs to compare multiple topologies or devices against

each other or because they are used to benchmark performance degradation as the design moves staring from an ideal schematic representation toward a full layout were each at each step more and more interconnect parasitic are incorporated until the full design is achieved.

Chapter 5 purposed the design detail and the post-layout simulation result of the 170GHz power amplifier in 0.13-µm SiGe BiCMOS.

Chapter 6 provides a summary of the work and after this recommendation for future work are made and possible improvements are discussed.

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Chapter 2. Literature Review

To benchmark the design presented in this thesis, the circuit should be compared with competing state-of-the-art power amplifier designs. This chapter therefore starts with listing and defining power amplifier figures-of-merit after which it will attempt to answer the following questions. What performance is currently achieved by state-of-the power amplifiers? Which are the relevant designs in literature which to be used as benchmarks? What topologies and design techniques are used in these publications to achieve their state-of-the-art results?

2.1 Power amplifier performance metrics

The power amplifier (PA) is the stage in a transmitter that, within a given bandwidth defined around a carrier frequency, generates the output power required to compensate the losses the transmitted signal incurs as it travels from transmitter to receiver. When doing this, it should provide sufficient gain to amplify the signal available at its input to the power level required at its output, while simultaneously operating in an efficient manner and guaranteeing a certain level of signal integrity, i.e. the signal should be amplified in a linear manner as to not distort the signal. This behavior of a power amplifier is commonly specified using a number of performance metrics. The definition of these performance metrics will now be repeated as they will be used in the remainder of this work to discuss design choices in de presented power amplifier design and to facilitate comparison with other power amplifier implementations.

The gain of a PA states the amplification factor of the amplifier or in other words, the ratio between the power at it input P_{in} and the power at its output P_{out} in Watts both in unit Watts, and the equation is given in eq. 2.

$$Gain = \frac{P_{out}}{P_{in}} \qquad \text{(eq. 2)}$$

This gain tends to be constant at low input powers but when the input power increases beyond a certain power level after which an amplifier is no longer increases with the gain and it starts to saturate. An example of this is given in Figure

2.1. In this graph, the input power level is given on the x-axis and the output power on the y-axis. With a lower power the output power increases linearly with the input power, but as the output increases the curve starts to deviate from its ideal theoretical repose and start to converge to a content power level. This power level is referred to as the saturated output power of the amplifier. The P1dB (output 1dB compression point) seen in Figure 2.1 is defined as the output power point where the large-signal power gain is compressed by 1 dB from the linear power gain line. In other words, the P1dB is defined as the output power point where the large-signal power gain is 1 dB less than the small-signal power gain.

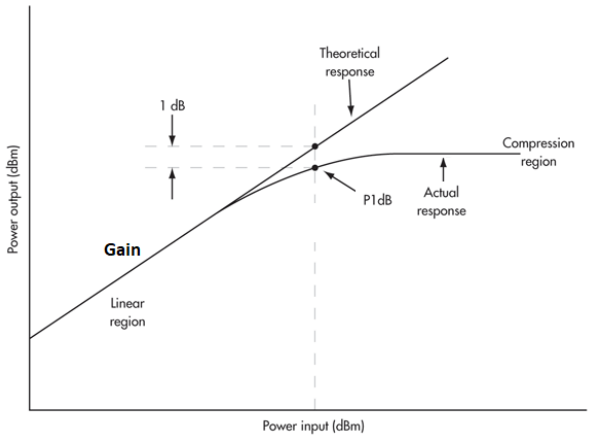

Figure 2.1: Output power vs input power [1]

In addition, a common metric to describe the efficiency with which a design provides the desired gain and linearity is the power-added-efficiency (PAE), which as the name suggests the efficiency with which the PA is able to add additional power to the signal and is can be defined as

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \quad \text{(eq. 3)}$$

Where the DC power is defined as the sum of the dc-current flowing through the circuit multiplied with the voltages provided at the supplies.

$$P_{DC} = V_{DC} \cdot I_{DC} \quad \text{(eq. 4)}$$

Besides having these before mentioned characteristics, the amplifier should also under no condition become unstable. To ensure if a particular design is not prone

to instability the following stability factor is monitored throughout the design. The power amplifier is assumed to be unconditional stable, i.e. will not start to oscillate when, the stability factor(K) and the related parameter Δ, which are defined as

$$K = \frac{2G_{11}G_{22} - \Re(Y_{12}Y_{21})}{|Y_{12}Y_{21}|} \quad \text{(eq. 6)}$$

and

$$|\Delta| = |S_{11} \cdot S_{22} - S_{12} \cdot S_{21}| \quad \text{(eq. 7)}$$

should always be higher than one (K > 1) and the absolute value of delta should be smaller than one (|Δ| < 1). (G11 and G_{22} are the real part of Y_{12} and Y_{21}) to make the PA unconditional stable. If K<1, which means the system is conditional stable, the feedback path could be added to cancel the internal feedback path and convert the system to unconditional stable.

2.2 Sate-of the-art power amplifier above 100 GHz

After listing the figure-of-merit for the power amplifier design, one can then begin to answer the questions which purposed at the beginning of this chapter, by examining the graph presented in, which is the is generated from over 1500 data point compiled in a power amplifier survey which encompasses publications found in relevant journals and conferences, and also including severable commercially available power amplifiers.

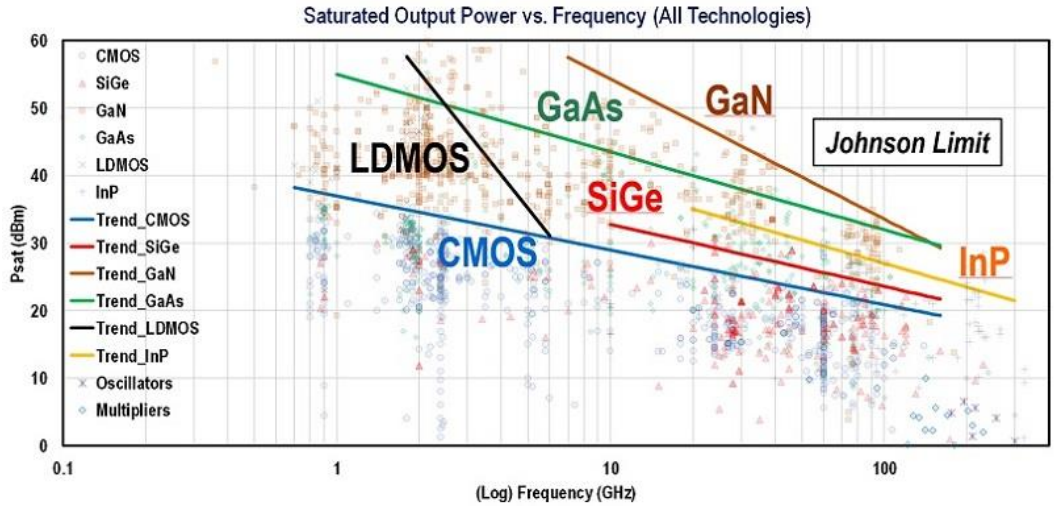

Figure 2.2: Saturated output power vs. frequency (all technologies) [2]

The graph presented the saturated power versus operating frequency of power amplifiers that are collected in a survey active since 2000. In the figure one can see that the data points consist of amplifiers demonstrated in six different technologies, namely LDMOS, CMOS, SiGe, GaAs, GaN and InP together with the trend lines of their saturated output power, Psat as the frequency increases. At frequencies below 2 GHz LDMOS seems to be the technology of choice, the performance however seems to decline with 15 dBm per decade. At frequencies above 10 GHz, GaN shows the best performance but the trend line indicates a decline in Psat approximately 7 dBm per octave with the trendline of this technology losing out against the remaining technologies somewhere between 150 GHz and 350 GHz as the slope of the trendline of GaAs, SiGe and CMOS technologies reduces by with a slope of 2 dBm to 3 dBm per octave. It therefore, seems that for frequencies between 100 GHz and 200 GHz the order of technologies in providing high output power is GaN, GaAs, InP, SiGe and lastly CMOS.

This however does not mean that the silicon-based technologies should be disregarded in favor of the named III-V technologies as potential candidate technologies for power amplifier implementation. Silicon-based technologies benefit from the large available production volume which allows a design in these technologies to serve larger markets and lower prices while also providing a higher-level functional integration as they allow the combination of both analog and digital functionality to be integrated on the same die. Therefore III-V technologies tend to only serve high performance low volumes markets.

2.3 Comparison of CMOS and SiGe for high frequency design

As mentioned in the introduction of this work the topic of this thesis is the design of a power amplifier in a SiGe technology and thus the remainder of this the literature review focuses on SiGe and CMOS implementations. If one then excludes the more exotic III-V examples from the previous analysis, one obtains the graph shown in Figure 2.3 which showing the power gain of silicon-based power amplifiers versus frequency and Figure 2.4 shows the 1dB-compression point of these same amplifiers. These figures then allow one to isolate potential candidate power amplifiers which can be used for both analysis, evaluation, and later on for comparison. The candidates chosen for these purposes are the data triangular data points. Of the chosen power amplifiers two are CMOS implementation to also have a comparison across technology and five are in SiGe.

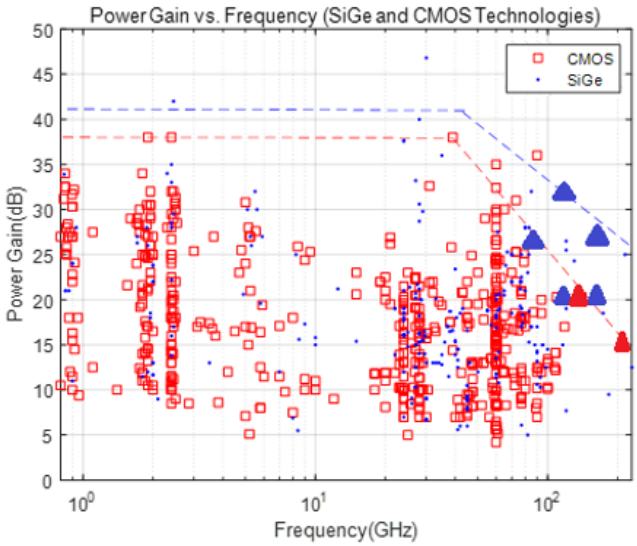

Figure 2.3: Power gain vs frequency (SiGe and CMOS technologies).

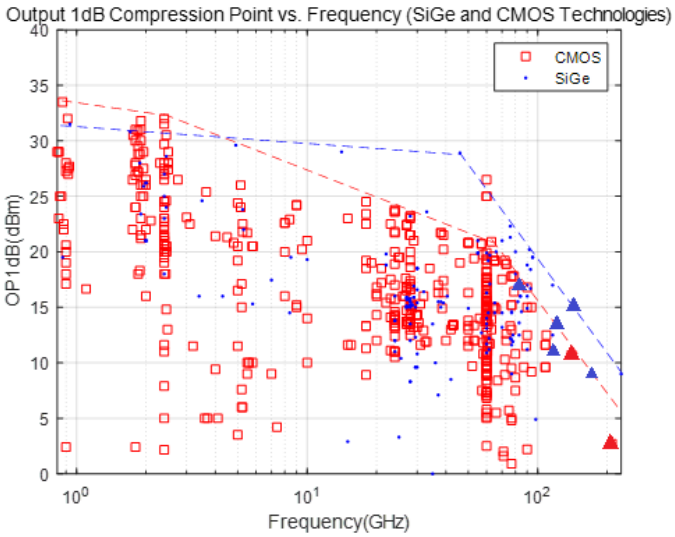

Figure 2.4: OP1dB vs frequency (SiGe and CMOS technologies)

Since the abilities of the power generation and power amplification for the power amplifier degrade when the operating frequency approach f_{max} (the operating frequency is normally designed as 1/3 of the f_{max}), designers are finding the solutions to overcome the limitation of f_{max}. Especially for the mm-wave and THz power amplifier design, except for careful marching network and power amplifier design, designers should select the technology with high f_t/f_{max}.

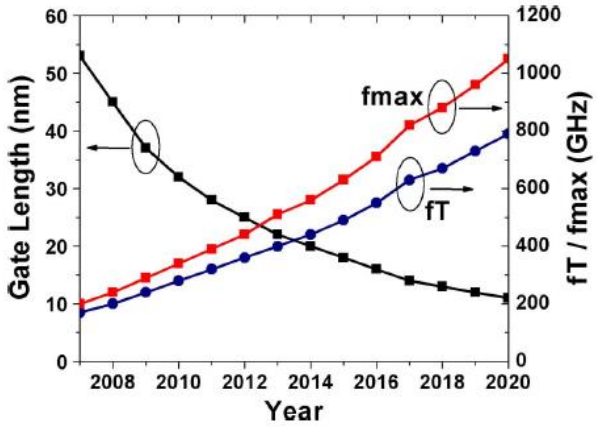

Figure 2.5: Development of ft, fmax with gate length of CMOS technologies [3]

Currently, CMOS and SiGe are two commonly used technologies in mm-wave power amplifier design. In order to improve the operating frequency of the power amplifier, SiGe technology, which has a smaller bandgap compared to the Si technology [4], is used in the mm-wave design. It can be seen in Figure 2.3 and Figure 2.4, above 100GHz, SiGe technologies can produce higher output power as CMOS technologies. With the same base current, the SiGe technology can have more collector current than previous Si technology and the breakdown voltage of SiGe is higher than CMOS technologies, which leads to higher power gain and output power compared to CMOS technologies. SiGe Technologies are more suitable than CMOS for the high frequency and high-power PA design.

Even though, there are some limitations with SiGe technologies. With the well-known $f_t \times BV_{CEO}$ product, which means that the breakdown voltage of the SiGe technology is well related to the peak f_t [5]. With better high-frequency performance which means higher f_t, the SiGe technology allows the lower breakdown voltage, which causes the less available collector current and the constraint of the output power at higher frequencies[6], which can also be seen in Figure 2.4. With a lower base thickness, the base transit time

$$\tau_B = \frac{w_B^2}{2D_{nB}} \qquad \text{(eq. 8)}$$

reduces and

$$f_t \approx \sqrt{\frac{1}{2\pi(\tau_B + \tau_C + \tau_E + \tau_{CSCL}}} \quad \text{(eq. 9)}$$

improves but the f_{max}, which is defined as

$$f_{max} \approx \sqrt{\frac{f_t}{8\pi R_B C_{CB}}} \quad \text{(eq. 10)}$$

degrades due to the larger base resistance R_B [7]. Thus, for the design of the SiGe HBT, the tradeoff between the improvement of the f_t and the degradation of the f_{max} is always considered by choosing the optimized gate width, collector width and collector doping.

The advantages of SiGe HBT in the power amplifier design is obvious, such as allowed higher breakdown voltage which means higher output power, higher peak f_t and f_{max} compared to CMOS technology. Several previous power amplifier designs based on the SiGe BiCMOS will be discussed below.

As shown in Figure 2.6, A 60GHz 3-stage CB 4-way combining power amplifier uses the 130nm SiGe BiCMOS technology which has the f_t/f_{max} of 240/270GHz.

There are three ways to increase the output power: utilizing cascode differential topology, scaling the output stage transistor and power combining.

In order to get enough output power and power gain, the 3-stage differential CB topology is used here and the three transistors from the first CB stage to the last stage are scaled as 1 - 2 - 8. The power combiner at the output terminal sums up the output power from 4 paths and could provide more output power, compared to one path topology. Instead of using lumped components as impedance matching network, the input impedance matching (which matches the input impedance to 50Ohm) is realized by the on-chip balun which also does the single-end to differential conversion [8], and the inner-stage impedance matching is realized by the balanced transformer. There are several advantages of using the transformer as an impedance matching network instead of lumped components and transmission-line, such as remove the external biasing or the DC supply from the input and output ports [9], which will be discussed more in the following chapters.

In the end, this 4-way combining power amplifier could achieve 5.2 dB power gain, 6.4dBm output 1dB compression point (OP1dB), 9.3dBm saturation output power and a peak PAE of 9%.

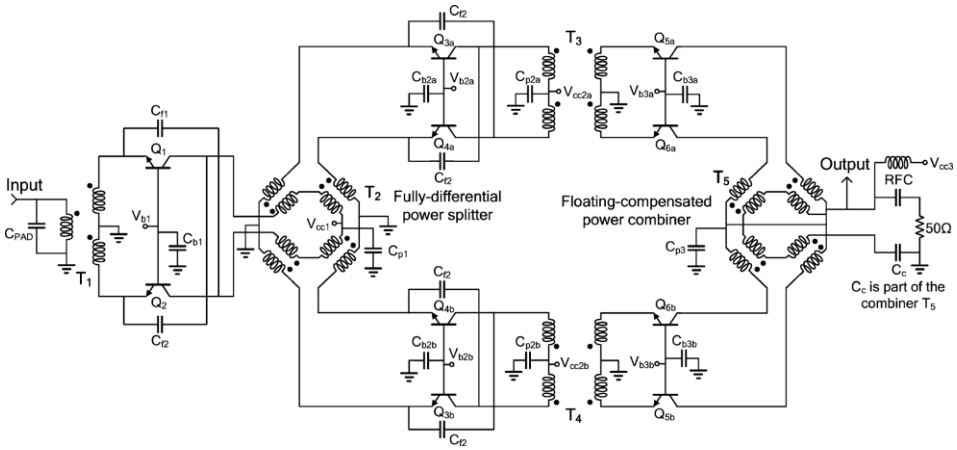

Figure 2.6: A 60GHz 4-way combining power amplifier [10]

A 160GHz power amplifier, which has a three-stage cascode topology, is shown in Figure 2.7. The 130nm SiGe technology which has the f_t/f_{max} of 240/270GHz is used in the PA design.

In this PA, the differential 3 stage cascode topology is used to get enough output power and power gain. Moreover, with the differential topology, the virtual ground is generated at the base of the CB stage the cascode topology. Thus, the number of the decoupling capacitors, which provides AC ground, could be reduced which makes the design of the layout easier.

Instead of conjugate matching, the load line matching is realized in this PA design to maximize the output voltage swing and the output current swing [11], which leads to more output power compared to the conjugate matching. The load line matching will be discussed more in the following chapters.

By the end, this 160GHz power amplifier could achieve 20dB power gain, 8.5dBm OP1dB and 10dBm output saturation power.

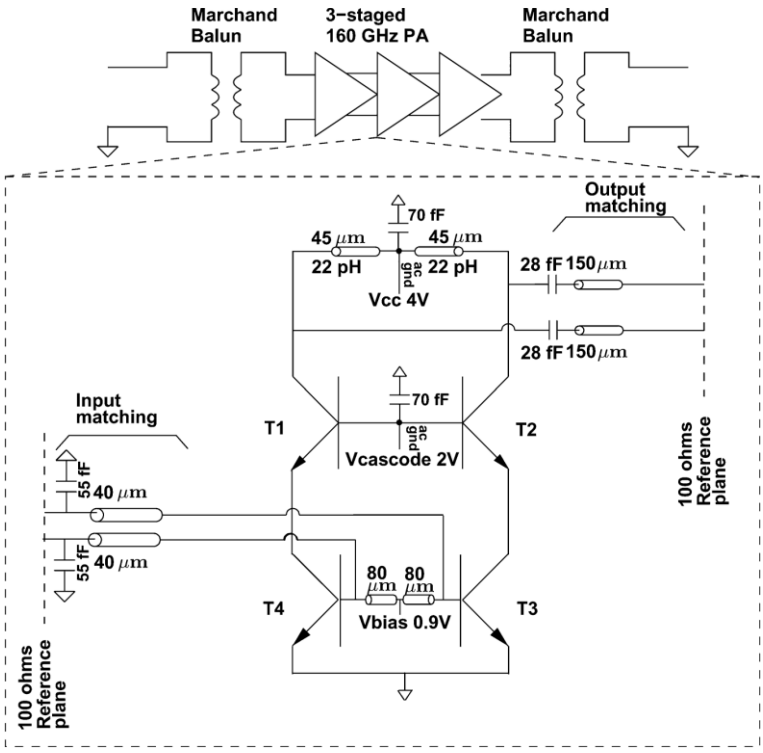

Figure 2.7: A 160GHz power amplifier [11]

A 120GHz power amplifier, which has a single-end four-stage CE topology shown in Figure 2.8. The power amplifier design gets use of the 90nm SiGe technology with f_t/f_{max} of 310/350 GHz. This power amplifier design provides 20 dB gain, 13.8dBm output saturation power and 11.6% peak PAE. The metal-oxide-metal (MOM) capacitor is applied in this power amplifier design to achieve the impedance with high quality factor (Q). With the 8-way combining structure which is shown in Figure 2.9, the output saturation power and OP1dB of this 120GHz power amplifier can be improved to 17 dBm and 20.8 dBm.

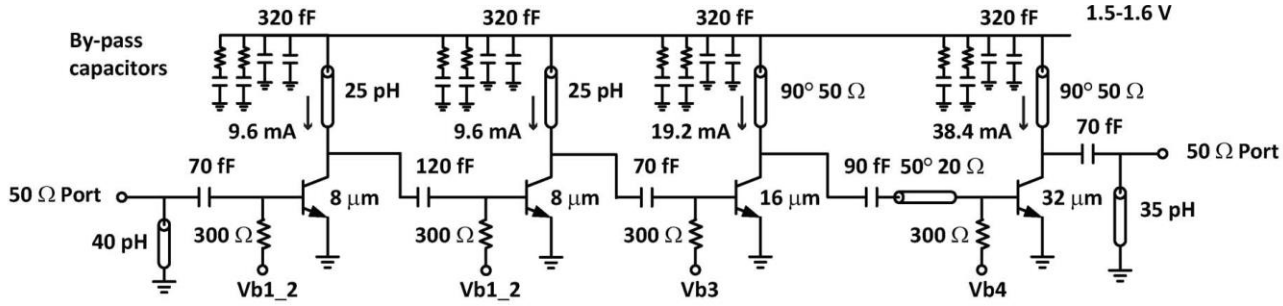

Figure 2.8: A 120GHz power amplifier [12]

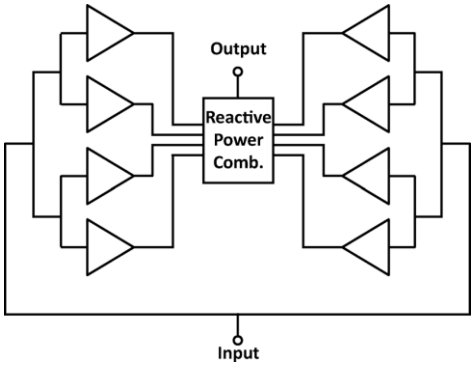

Figure 2.9: The 8-way combining structure [12]

As shown in Figure 2.10, A D-band power amplifier which uses the 120nm SiGe technology with the $f_t/f_{max}$of 330/250 GHz. The three-stage differential cascode topology is applied for the sufficient 17.8 dBm saturation output power and 32dB power gain. The MOM capacitor which has high quality factor works as the decoupling capacitor at the base of the CB stage in the cascode topology. At the end, the D-band power amplifier provides a 4.3% PAE.

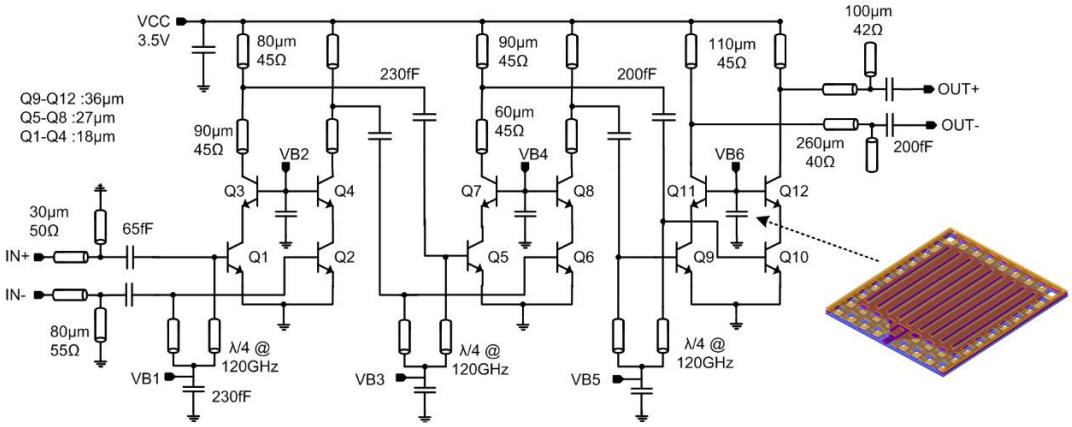

Figure 2.10: A D band power amplifier [13]

As shown in Figure 2.11, The 160GHz power amplifier uses the 130nm SiGe technology which has an f_t/f_{max} of 500/300 GHz. The transistors are biased for the peak f_t and the transistors are scaled as 1, 2, 4, 8 from stage one to stage four to get the adequate output power and the power gain. The MIM capacitor is used as the decoupling capacitor. Conjugate matching is achieved by the L matching network for the input, output impedance matching and the inner stage impedance matching. The transmission line which has Metal 2 as the top and Metal 1 as the ground which has the lowest power loss is used in the L matching network.

By the end, this 160GHz power amplifier could achieve a power gain of 25.7 dB, OP1dB of 16dBm, the output saturation power of 16 dBm and a peak PAE of 19%

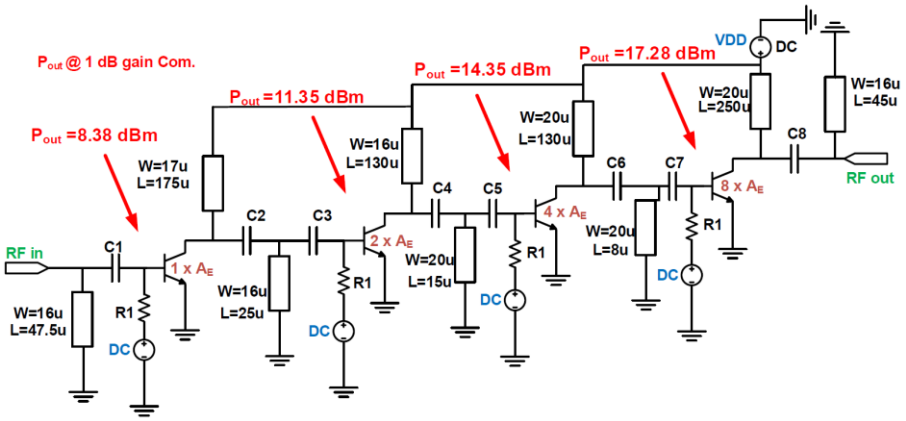

Figure 2.11: A 160 GHz power amplifier [14]

Even though, compared to SiGe technologies, the CMOS technologies still have advantage such as low cost. Several previous power amplifier designs based on the CMOS technologies will be discussed below.

A 140GHz power amplifier in 40nm CMOS technology is shown in Figure 2.12.

In order to increase the output power, this 140GHz power amplifier has 3 cascoded stages. As we have discussed before, except for utilizing cascode topology, there are other two ways to increase the output power of the power amplifier. One is increasing the finger number of the output transistor. Another one is utilizing power combining. Although increasing the size of the output transistor can improve the ability of the output power generating of the power amplifier, the stability of the cascode topology is mainly affected by the parasitic at the gate node and the parasitic will also increase with the increasing size of the output transistor. To avoid big size of the output transistor, the power combiner is utilized in this power amplifier. The input and the driving stage of the transistors are sized to avoid reaching the 1dB compression point of the stage itself.

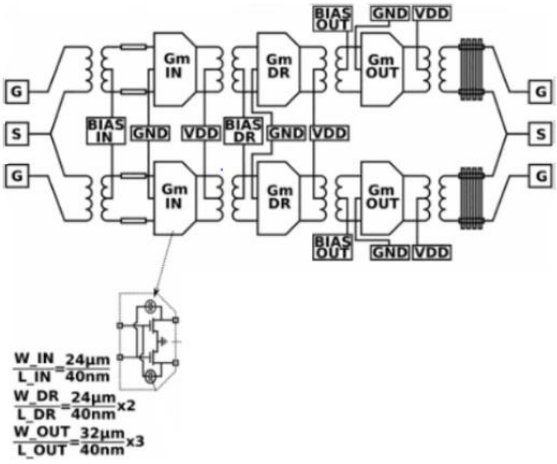

Figure 2.12: A 140GHz power amplifier [15]

This 140GHz power amplifier can reach a power gain of 20.3 dB and an output saturation power of 14.8 dBm.

One another 210GHz power amplifeir can be seen in Figure 2.13, since the Gmax of the transistor is only 4.5 dB, after adding losses in between stages, the avaliable power gain of each stage reduces to 2 dB, by applying the over-neutralization technique, the avaliable power gain could increase to 4 dB with a margin of stability (K = 1.2)

This three stage 210GHz power amplifier can reach a power gain of 15 dB and OP1dB of 2.7 dBm.

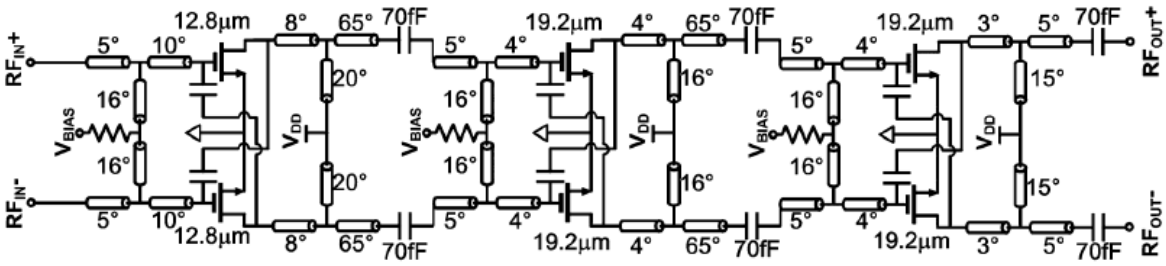

Figure 2.13: 210GHz power amplifier [3]

‘

Table 2 Comparison of the previous SiGe BiCMOS power amplifiers

Ref	Tech (nm)	Freq (GHz)	Gain (dB)	P1dB (dBm)	Psat (dBm)	Pdc (mW)	Peak PAE	Topology
[10]	130 SiGe	84	27	16	18	395	9%	3-stage 4-way differential CB
[11]	130 SiGe	160	20	8.5	10	-	-	3-stage differential cascode
[12]	90 SiGe	114-134	20	11	13.8	200	11.6%	4-stage Single-Ended CE
[13]	130 SiGe	110-130	32	13.5	17.8	560	4.3%	3-stage differential cascode
[14]	130 SiGe	138-175	25.7	16	18	-	19%	4-stage Single Ended CE

Table 3 Comparison of the previous CMOS power amplifiers

Ref	Tech (nm)	Freq (GHz)	Gain (dB)	P1dB (dBm)	Psat (dBm)	Pdc (mW)	Peak PAE	Topology
[15]	40 CMOS	140	20.3	10.7	14.8	306	8.9%	3-stage 2-way differential cascode
[3]	40 CMOS	210	15	2.7	4.6	40	6%	3-stage differential CE

Conclusion

In this chapter, we first focus on the advantages and disadvantages of SiGe and CMOS technologies in high frequency design and described in details the reported works implementing state-of-the-art power amplifier designs, in the above

mentioned technologies. To provide a broader picture of the achieved capabilities in sub-THz Pas also references employing GaAs and InP have been discussed in the comparison.

The reported literature allows to provide a good understanding of where the targeted performance of the PA targeted by this thesis work are located in the international research community.

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Chapter 3.

MM-wave PA Design Flow

In the previous chapter we reviewed the key figure-of-merits for power amplifiers and described various topologies presented in literature which can be used as benchmarks for the power amplifier concept that will be developed in this work (described in Chapter 5). In this chapter we will analyse the design flow and present the proposed approach to approach the design of high-performance integrated Pas in the specific case of deep mm-wave designs.

This chapter will describe, based on the proposed approach, the required steps needed to move from the basic analysis of a technology performance to the implementation of a circuit design that meets the intended specifications while operating within the constraints set by the technology.

3.1 Conventional power amplifier design flow

In order to present the challenges posed by design operating in the deep mm-wave frequency range (i.e., above 100GHz) let us first review a classical design flow process to achieve a circuit level design capable of achieving targeted performance metrics. In order to discuss the conventional PA design flow, we can refer to the simplified flow graph shown in Figure 3.1.

The performance centric design flow, starts from the indication of the parameter which are the target of the design, see box 1 in Figure 3.1.

From the frequency requirement and overall gain of the TX chain the designer can easily identify the key DC parameters and the required number of stages need to reach the set performance parameters, as shown in box 2 of Fig. 3.1.

Following the approach presented in [1]:

1) determine the maximum allowed drain-source/collector-emitter voltage swing, defined as eq. 11.

$$V_{swing} = V_{Max} - V_{DS,Sat} \quad \text{(eq.11)}$$

centred around the supply voltage V_{DD}, where $V_{DS,Sat}$ is the drain-source/collector-emitter saturation voltage and V_{MAX} is defined as

$$V_{MAX} = 2V_{DD} - V_{DS,Sat} \quad \text{(eq. 12)}$$

2) S-parameter simulation, set the biasing point (drain/collector current density at the biasing point I_{DC}, gate-source/collector-emitter voltage V_{GS}/V_{CE}) and V_{DD}/V_{CC} to maximize the power gain.

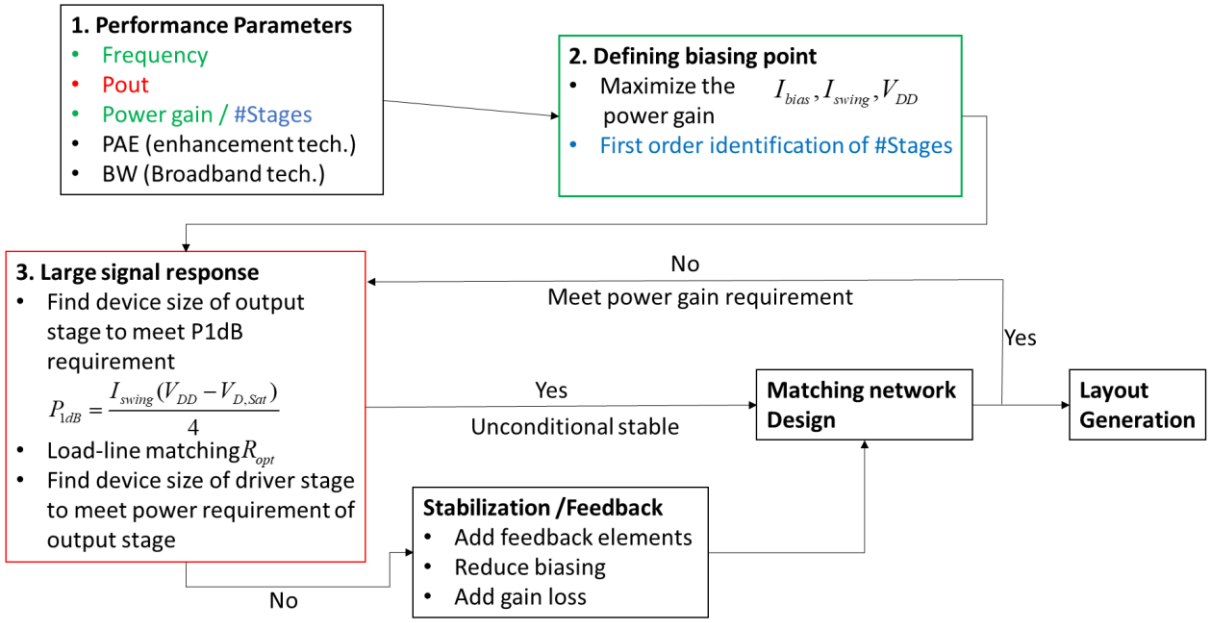

Figure 3.1: Simplified flow diagram representing the design steps to achieve an RF PA achieving set user metrics

3) is to find the device size of the output stage to obtain the required output power. We can get the maximum collector current swing I_{swing} before 1dB compression point, from the expression of P_{1dB} shown in eq. 13.

$$P_{1dB} = \frac{I_{swing} \times (V_{DD} - V_{DS,Sat})}{2} \quad \text{(eq. 13)}$$

Finally, we can compute the W which is the width of the output stage device from

$$I_{swing} = current\ density \times W \quad \text{(eq. 14)}$$

In a small signal amplifier this would provide directly the input output termination (i.e., source and load conditions) required to maximize the power transfer, i.e., power match conditions. Nevertheless, in a large signal (i.e., allowing input/output transfer distortion) amplifier these source and load condition do not guarantee the optimization of the maximum amount of power that device can deliver up to its 1dB compression point ($\mathrm{P_{1dB}}$) .

As it was shown in [2], and is reported in Figure 3.2, in order to increase the power driving capability of a power cell a different load resistor (neglecting the compensation of the reactive components) need to be chosen compared to the small signal power match case (i.e., $\mathrm{R_{opt}}$ for output power will be lower compared to the power match case). This implied a trade-off between gain and output power driving capability, as can be seen in Figure 3.2

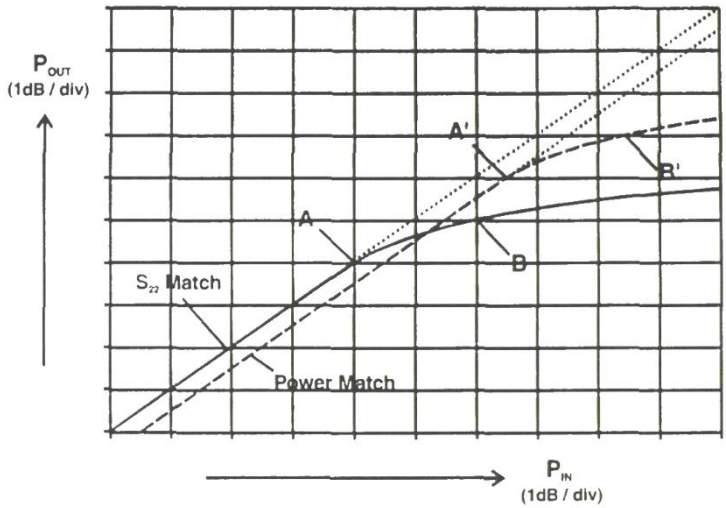

Figure 3.2: Compression characteristics for conjugate (S22) match and power match, reprinted from [2]

This load resistance can be defined as “loadline” matching load

$$R_{opt} = V_{max}/I_{max} \qquad \text{(eq. 15)}$$

After defining the $\mathrm{R_{opt}}$, the next step is to add matching network for the output stage. But before that, we first need to check whether the PA is unconditional stable. If not, we need to first add the feedback element (i.e., neutralization capacitor, negative feedback element, etc.), reduce the biasing voltage or add some gain loss in between the stages to stabilize the circuit. After stabilization, the output matching

network is required to transform R_{opt} impedance at the device plane to the proper interface impedance of the circuit, i.e., often 50 Ohm.

After adding the matching network for the output stage, if more stages are needed for the power gain requirement (the proceeding stage should provide adequate output power for its next stage), adding the intermediate stage matching, the matching network topologies are needed to be carefully selected to minimize the insertion loss in between the stages. And repeat previous steps for the proceeding stages.

Until the input stage, conjugate match the first stage to the 50 Ohm characteristic impedance to minimize the power reflection and maximize the power gain.

After concluding the schematic optimization phase, the designer begins to construct the circuitry in the layout environment and annotates the including parasitic introduced and the real responses of the passive components in order, when needed, to retune the device. It is important to note that the headroom of the device technologies (i.e., available gain per stage) allows this process to be linear and requiring few iteration cycles.

3.2 Differentiators in deep mm-wave PA design

When considering the case of a PA operating in the deep mm-wave band it is important to analyse the impact of the reduced design headroom on the design flow.

Power cells from state-of-the-art silicon-based technologies optimized for mm-wave operation will all present maximum oscillation frequency below 500GHz. This translated in a design frequency in the order of factor 3 to 4 to the maximum frequency where the device presents gain. The strong impact of the maximum gain available from a single power cell can be easily observed plotting maximum available gain (i.e., gain obtained in source and load conjugate match condition) versus frequency for the chosen technology, as can be seen in Figure 3.3.

When we consider that the parasitic inductance and capacitances added by the transistor level interconnections are comparable to the impedance level provided by the device and that the insertion losses of the matching networks often accounts up to few dBs (i.e., 2-3) it becomes clear that the design head room present at lower frequencies is not available in deep mm-wave designs.

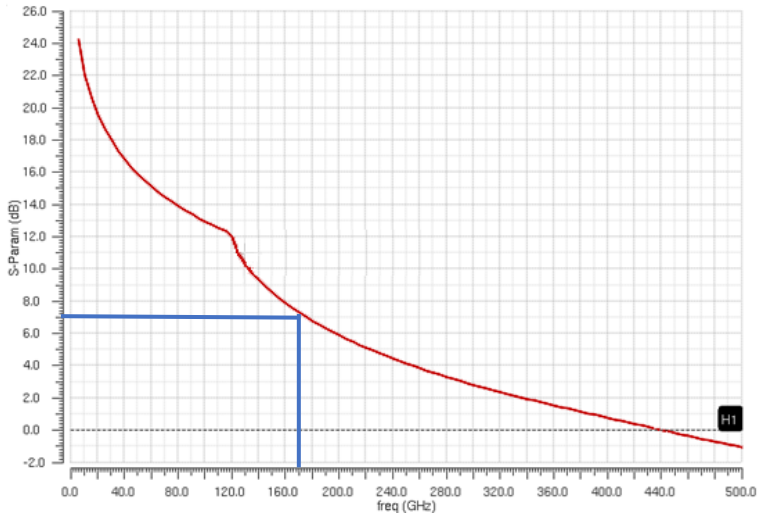

Figure 3.3: Maximum available gain of IHP G2 intrinsic transistor versus frequency

This basic set of constraints makes a conventional design flow very inefficient since accounting for the parasitic impact in a later stage of the design process and leaving to the designer the task of incorporating and tuning the layout geometries leads to a large amount of redesign and optimization loops.

In order to overcome this main bottleneck the work of this thesis is centred around the enhanced usage and interface of the design tools (i.e., circuit non-linear editor and simulation, layout design tool, parasitic extraction tool, and data analysis tool) available to the HF designer.

3.3 Proposed CAD tools eco-system interfacing for mm-wave design

This thesis work proposes and optimizes the following CAD tool eco-system.

1) Cadence design system is employed for the circuit level linear and nonlinear simulation.

2) Usage of Open Command Environment for Analysis (OCEAN) scripting language to create generic or deign specific automated test benches.

3) Usage of the Locator/Identifier Separation Protocol (LISP) coding language proprietary of cadence named SKILL for automated 2D layout generation.

4) Usage of MATLAB environment to access iterate and store the results of the OCEAN script-based simulation for advanced elaboration or analysis of the simulation results.

Conclusion

This chapter described the conventional RF PA design flow and touched upon the challenges when attempting to simply replicate these approaches for deep mm-wave designs. In addition to this, the mm-wave CAD tools and eco-systems proposed for this thesis work were introduced.

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Chapter 4.

Automation using Ocean & Skill

In the previous chapter, the conventional tools and analysis for the mm-wave PA design have been discussed. In addition to this, some of the current mm-wave CAD design tools and eco-systems were introduced. The available tools leave some functionality still to be desired. One of these is the automation of certain tasks that in mm-waves can requires some iterations to get right. This because the higher frequencies make the devices and circuits less unilateral giving these a certain transparency thus resulting in the fact that the output and input of these devices circuits cannot be considered decoupled. Changes on one side results in modified behaviour on the other one. Another aspect that can use improvement is the data handling capability of the available CAD tools. When handling data or data sets obtained from simulations become large one would be better served by programs such as MATLAB or Python. That allow efficient handling and manipulation of large data sets with ease. Besides these drawbacks in CAD tools there is also the aspect that mm-wave design relies more heavily EM-simulations to accurately predict the behaviour of a circuit. The outcome of such simulations usually requires more than one iteration get right. Thus, automating several of these recurring tasks would save up time that could then be used on more critical part of the design. This chapter will therefore focus on isolating some of the obvious recurring task and attempt to automate them partially or completely in order to minimize their impact on the project's timeline. The code/scripts discussed in this project are written in "Skill" [1] and "Ocean" [2], which are scripting languages used in many of the software tools produced by "Cadence Design Systems", as there is prior experience within with these languages. Moreover, the data saved under the Cadence circumstance is shared with MATLAB platform, which has big data handling ability.

4.1 Recurring tasks in a power amplifier design flow

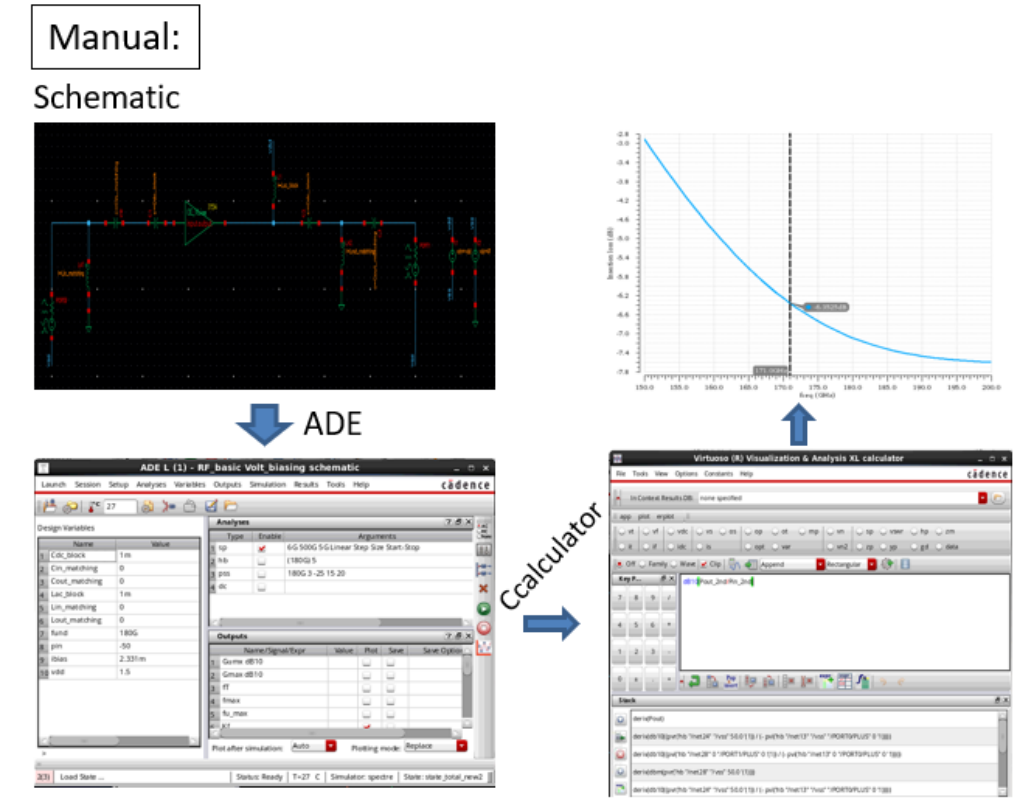
In the design flow stated before, one can observe several steps that will need at least once per technology, or once per device, or multiple times in a design flow. An

example of such a step would be the acquisition of a device's f_t/f_{max} versus current density. This would be a necessary step to select the bias point of the fastest device in a technology or in the case of multiple device candidates for a multiple of devices within the same technology. This procedure could therefore be said to be a candidate for automation through the implementation of a standardized template with a corresponding ocean script which would allow one to simply insert a device in the schematic or netlist and run the script to quickly obtains the desired information. Automation of this step would be even more worthwhile if this ft/fmax plot would be used in for instance monitoring the performance degradation of a transistor after layout which introduces parasitic components related to metals lines and features that from the interconnect to surrounding circuitry.

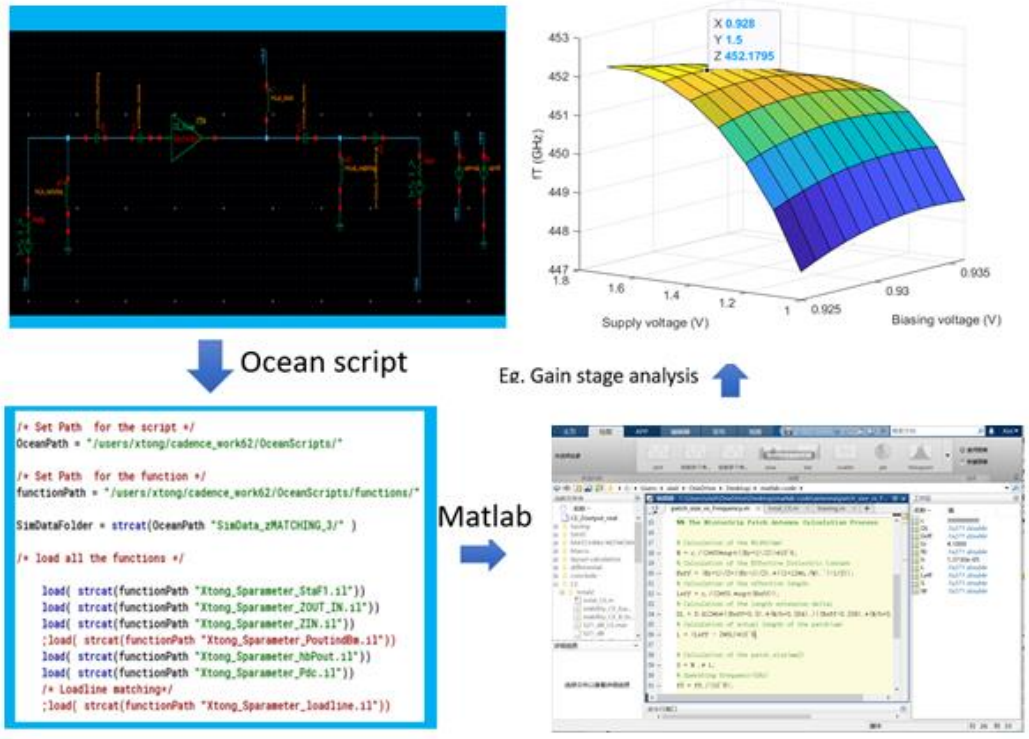
Another candidate task for automation is the gain stage analysis, similar as the procedure of the automated biasing point selection. There is no need for the designer to manually change the number of the device in the schematic for many times, with the automation design flow, designers only need to modify and run the script to obtain the desired information and then the analysis can be done with the help of the MATLAB code.

4.2 Benefit of scripted mm-wave design flows

In this section, the benefit of the scripted mm-wave design flow would be discussed. The partial code of the scripted design flow can be found in Appendix A, B and C.



(a)



(b)

Figure 4.1: Comparison of (a) conventional, (b) ocean scripted design flow

One of the advantages of the scripted design flow is the improvement of the big data handling ability. As shown in Figure 4.1(a), in a conventional design flow using cadence platform, one needs to build up the schematic and use Virtuoso ADE to analyze the circuit manually step by step (applying calculator if a complicated equation is needed for the analysis) and plot data under the circumstance of cadence platform. As shown in Figure 4.1(b), in the ocean scripted design flow, the design steps are coded in one script. The data is shared between cadence and MATLAB platform and is plotted under the circumstance of MATLAB platform. With the characteristics of the MATLAB platform, such as complex data calculation ability and large data handling ability, one can do the 3-D plot as shown in Figure 4.1(b), which is unfeasible under the cadence circumstance.

Another advantage of the scripted design flow is the formalization of the design flow and the ability to be transferable to future project and technologies. The design flow of the system is formalized and coded in one ocean script. As we have discussed in previous chapter, parameters and analysis needed to evaluate the performance of the PA are consistent. The design flow is formalized in one scripted and the parameters such as gain, OP1dB, PAE and so on, are saved and then transfer to the MATLAB environment, as shown in Figure 4.2,one can simply compare the standard performance of different technologies by only changing the netlist of the arbitrary gain stage in the ocean scripted without “repetitive clicks” in Virtuoso ADE.

Not like low-frequency design, for the mm-wave PA design, the parasitic inductance and capacitance have influence on the performance of the PA. The scripted design flow could save the time for the designers to do the layout optimization.

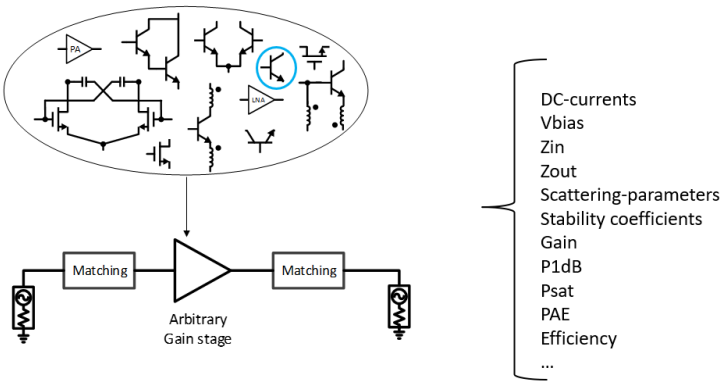


Figure 4.2: Gain stage example

4.3 Ocean script design flow

The automation design flow applied for this 170GHz power amplifier design is shown in Figure 4.3.

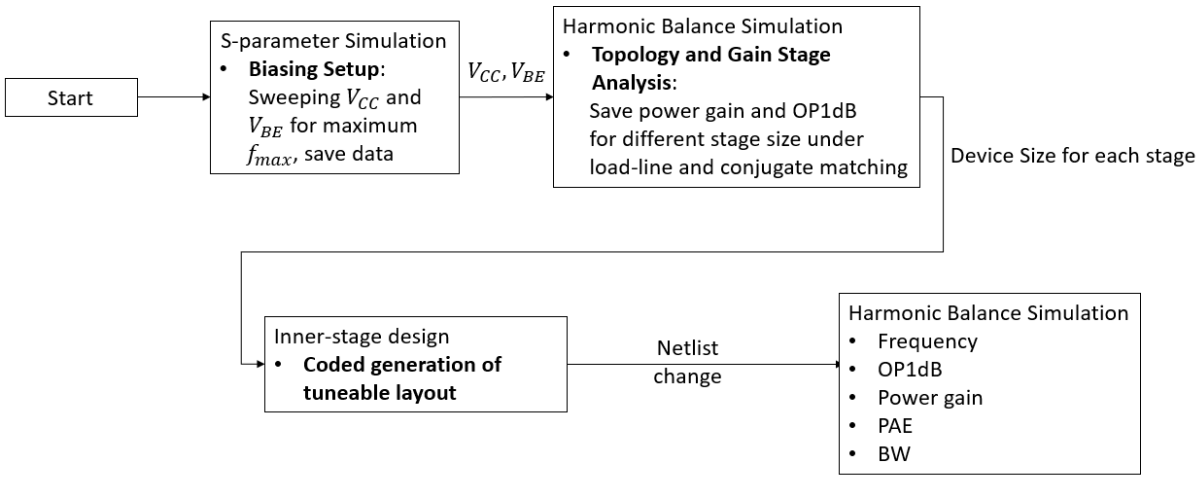


Figure 4.3: Automation design flow

Before going through the scripted design flow, the first step is to quickly converge to an initial gain stage line-up as one example shown in Figure 4.4 under the requirement of Gain, $\mathrm{P_{1dB}}$, operating frequency of the power amplifier.

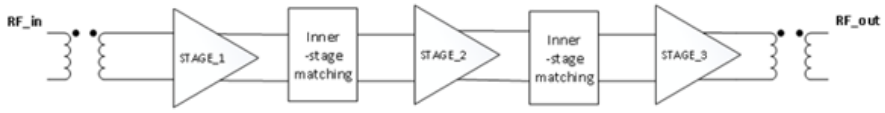


Figure 4.4: Example of an initial gain stage line-up

As shown in Figure 4.3, the first step of this automation design flow is the Biasing Setup. The schematic of one CE (Common Emitter) stage is shown in Figure 4.5. The transistor Q1 is biased with an ideal voltage source $\mathrm{V_{be}}$, C1 and C2 are selected to be 1mF which is large enough to be the DC block. The collector of Q1 is connected with the supply $\mathrm{V_{CC}}$ with L1 (1 mH) which is large enough to be the AC block.

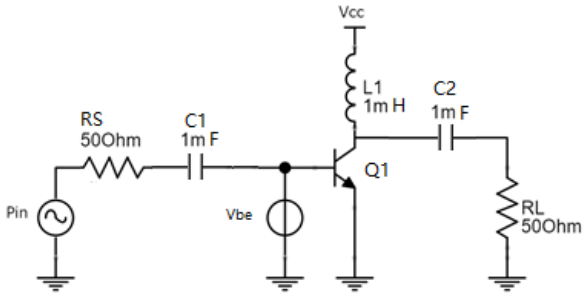
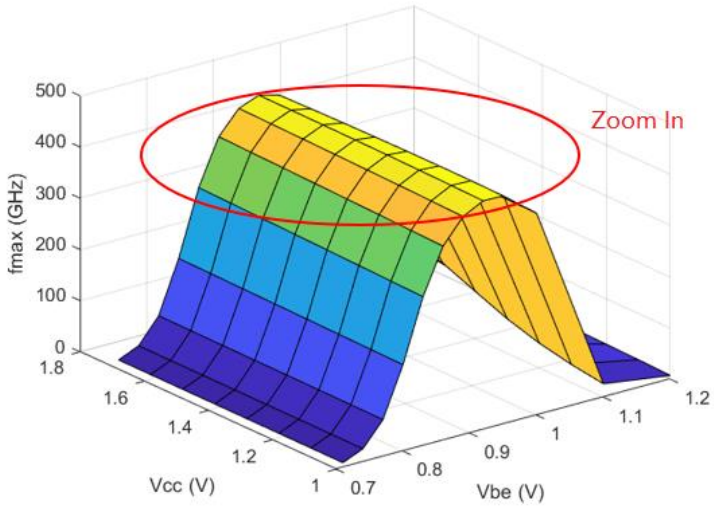


Figure 4.5: Schematic of one CE stage

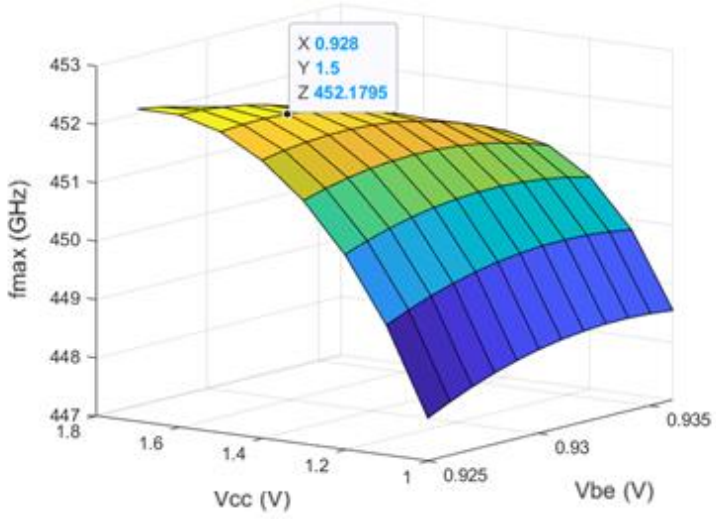
The script part of biasing setup is running under the cadence circumstance and using the S-parameter method. The data of f_{max}, V_{CC} and V_{be} are transferred and plotted Under MATLAB circumstance.

For the power amplifier, since the power gain capability of one PA is related to the f_{max}. We would like to find one biasing point for this CE stage to achieve f_{max} in order to achieve maximum power gain. Figure 4.6 (a) and (b) show that,

If we want to achieve a maximum f_{max}, V_{CC} should be 1.5 (but to reach higher reliability maybe this value should be lower). We can achieve a maximum f_{max} with V_{ce} 1.5V with V_{be} 0.93V, while biasing collector current density is $40\ \mathrm{mA/um^2}$ and the size for the single transistor is 0.07*0.9 $\mathrm{um^2}$.



a)



b)

Figure 4.6: Biasing setup a) f_{max} with V_{be} and V_{CC} b) zoom-in part

At the meantime, with the advantage of the scripted design flow which is data-handling ability improvement, one can easier do further complex analysis to select the biasing point.

There is one example of this kind of analysis. From Figure 4.7 and Figure 4.8, one can see that, when the biasing voltage reduces from 0,928 V to 0.915 V, the PAE can be improved by 3.4% and OP1dB can be improved by 0.03 dBm, with only 0.09 dB power gain sacrifice.

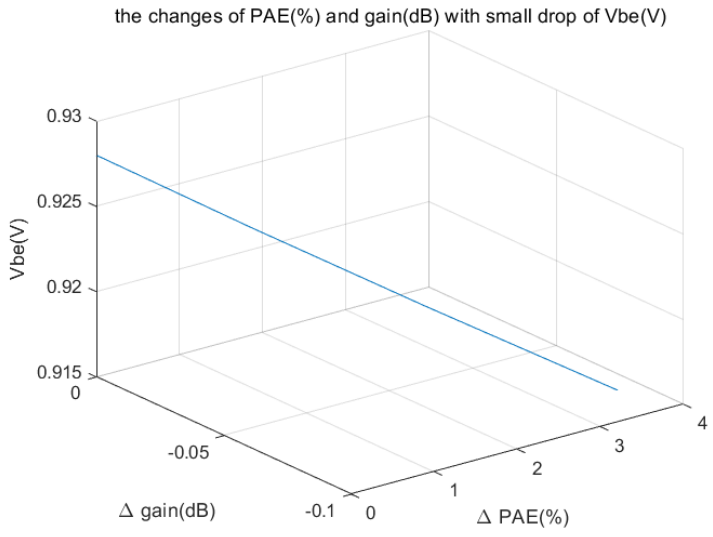


Figure 4.7: The changes of PAE and gain with a small drop of V_{be}

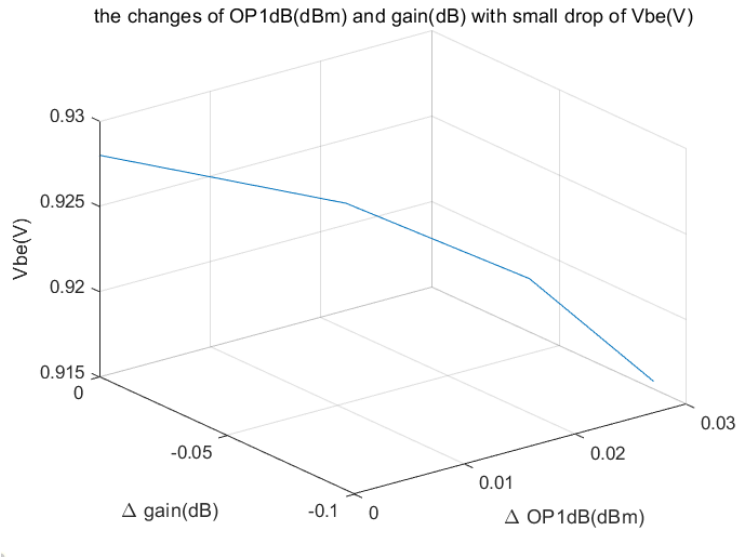


Figure 4.8: The changes of OP1dB with a small drop of V_{be}

From above analysis, one can get, with the sacrifice of the biasing voltage, the PAE and output 1dB compression point (which could indicate the linearity performance) can be improved but meanwhile the gain will also be sacrificed. Since the last stage of the power amplifier should be designed for the sufficient output power and efficiency where a bit of the gain sacrifice can be allowed while the preceding stages are designer for enough power gain. Tuning the biasing point of the last stage could be a good way to improve the PAE and the OP1dB of the power amplifier.

4.4 Gain stage and topology analysis

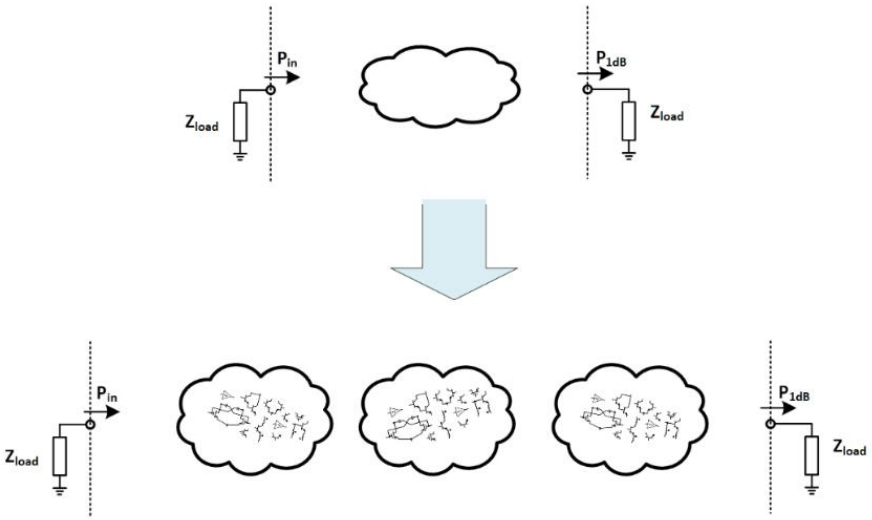


Figure 4.9: Selection of the stage topology

After the biasing setup, the next step is select the topology for each stage of the PA, which we called topology analysis. Since the scripted design flow has the advantage that it is transferable between different technologies and topologies, as shown in Appendix A, one can simply change the simulated topology by changing the netlist name in the script and do the same analysis for different topologies to compare their performance, which saves time for the designers since there is no need to click the button in the ADE again and again.

Figure 4.10 shows the schematic of three common use topologies for a power amplifier: CE, CB and cascode. As discussed in the previous section, from the Biasing Setup step, V_{be} would be 928 mV and the supply voltage V_{CC} would be 1.5V to maximize the f_{max} for the CE and CB stage as shown in Figure 4.10(a) and (b). For the cascode topology, which can be seen as one CE stage series with one CB stage, as shown in Figure 4.10(c), the supply voltage is 3 V and V_{bias} at the base of the CB stage is 2.43 V to provide the voltage headroom for the CE stage.

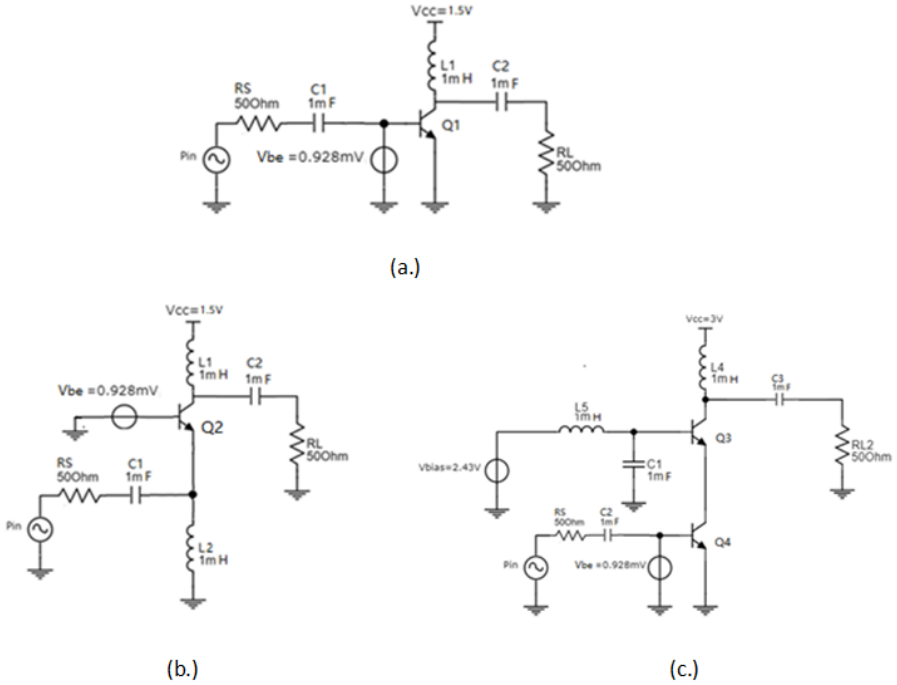


Figure 4.10: Schematic of the single-stage topologies a) CE, b) CB, c) cascode

Figure 4.11 shows the reverse isolation (S12) of CE, CB and cascode topologies as shown in Figure 4.10. Among three topologies, cascode is able to achieve lowest reverse isolation with is because there is less direct input-output coupling appears in cascode topology compared to CE and CB topologies. Furthermore, with higher reverse isolation, the input stage can be well decoupled with the output matching network [1], for the design of PA, it means that more impedance mismatching between antenna and PA can be tolerated [2]. Moreover, as shown in Figure 4.12, the cascode topology is also able to achieve higher power gain compare to CE and CB topology, which is due to the higher output impedance that the cascode topology has compared to CE and CB topology.

Thus, the cascode topology is selected to be the gain stage due to the achievable power gain and output power and the lowest reverse isolation among three topologies. But as we mentioned before, this analysis is not limited to those three topologies, the designers can choose different topologies and technologies by changing the netlist in the script to compare their performance, which we will leave for the further research.

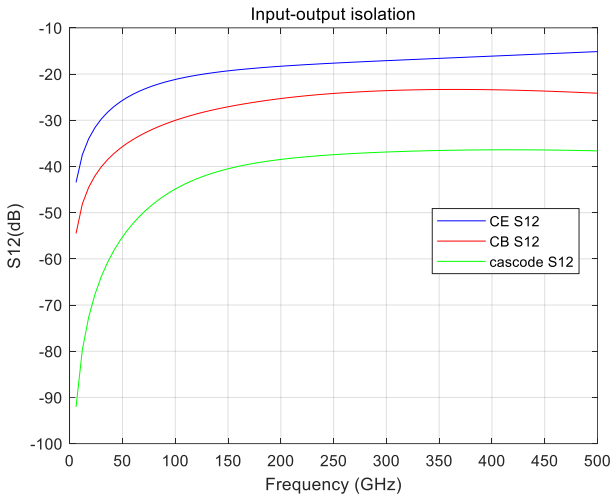


Figure 4.11: Reverse(input-output) isolation of CE, CB and cascode topologies

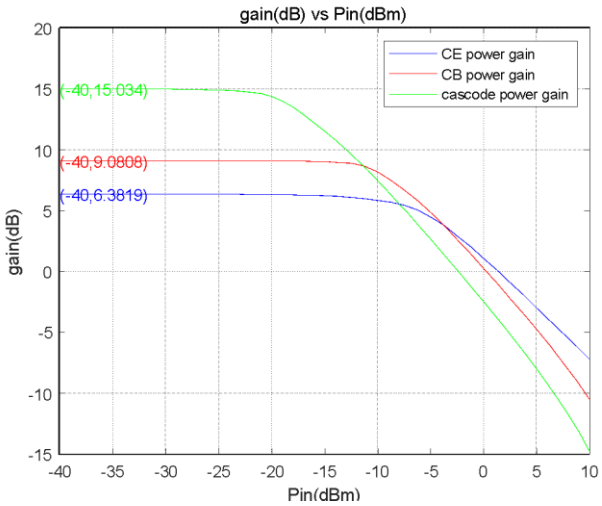


Figure 4.12: Power gain of the CE, CB and cascode topologies

After the topology analysis, the next step is to do the gain stage analysis. The main purpose of the gain stage analysis is to select the device size for each stage in order to achieve the output power and power gain requirement of the PA.

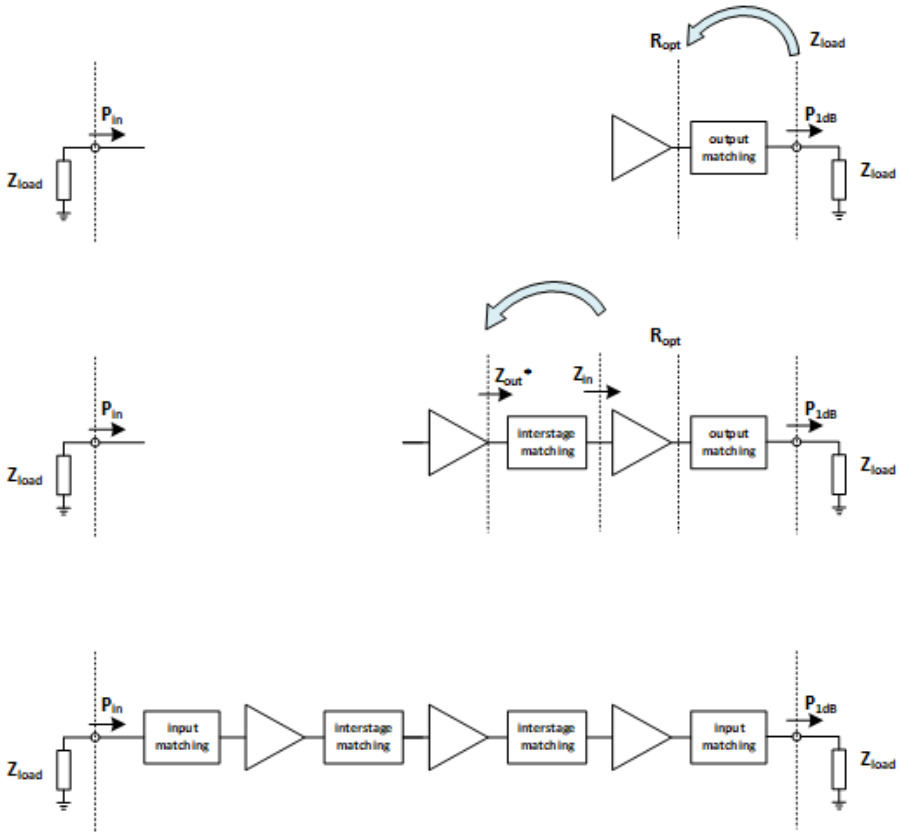


Figure 4.13: Automated generating matching network

The script part of gain stage analysis is running under the cadence circumstance and using the harmonic balance method. The data of power, gain and stage size are transferred and plotted Under MATLAB circumstance. As one can see in Appendix A, the script of the stage analysis includes two parts: one is to automate the generation of gain stage characteristics (Gain and Op1dB) versus number of parallel devices under optimum load condition(automated matching Z_{load} to R_{opt} as shown in (Figure 4.13) to obtain maximum output power , and another one is to automate the generation of gain stage characteristics (Gain and Op1dB) versus number of parallel devices by partially automating ideal single frequency Matching network generation for input and output impedance which allows the simulation as shown in Figure 4.13. With the result from the gain stage analysis, we can then line up the stages with the ideal matching as shown in Figure 4.14.

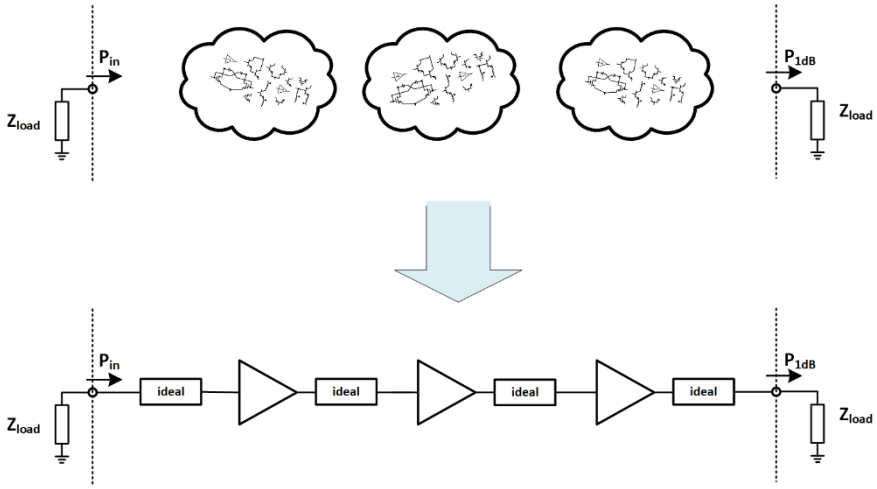


Figure 4.14: Line-up of the gain stages with the ideal matching

As an example, Figure 4.15 illustrates the line-up of a three stages differential CE structure. the output stage of the PA is selected to be a differential CE with 8 parallel devices with OP1dB of +10 dBm and a power gain of 6.5 dB. The input stage and second stage of the PA are selected to be differential CE with 6 parallel devices with OP1dB of +8.5 dBm and a power gain of 6.7 dB.

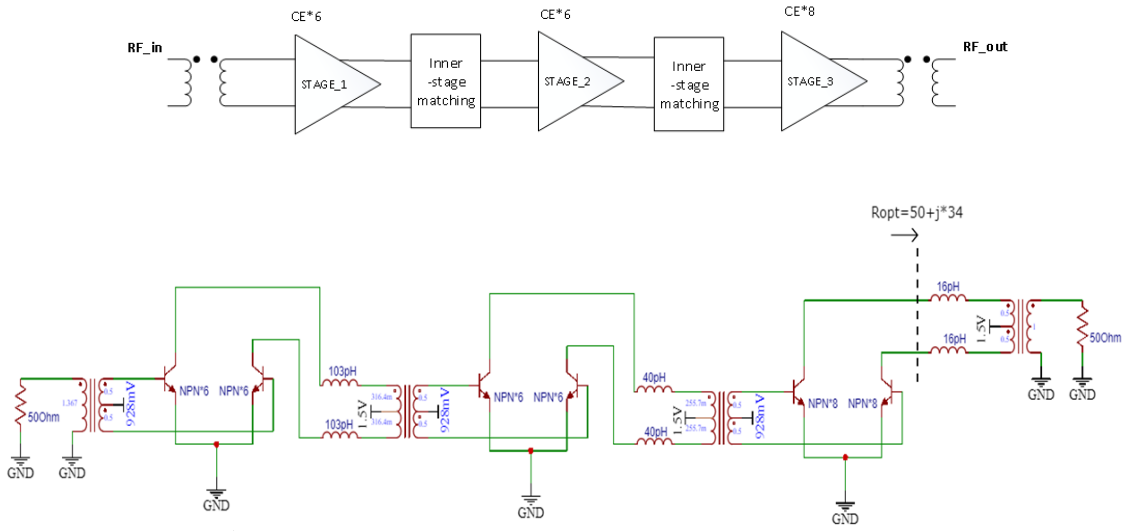


Figure 4.15: Line-up of a three stages differential CE structure

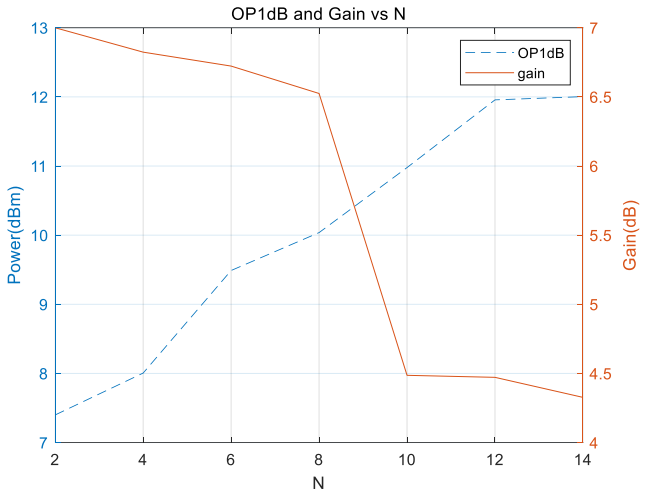


Figure 4.16: Gain stage analysis under optimum load condition

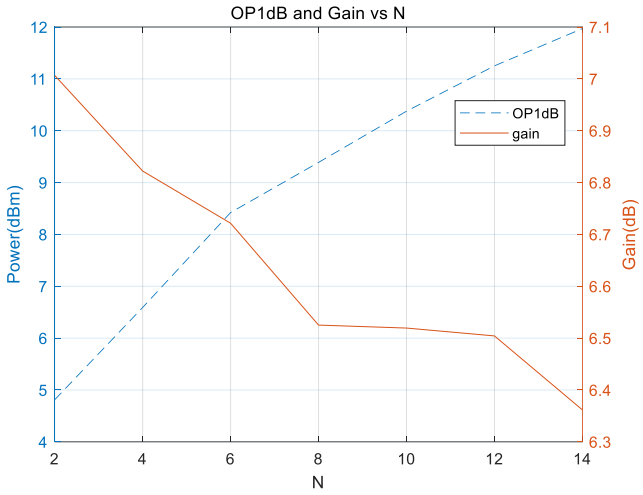


Figure 4.17: Gain stage analysis under conjugate matching condition

The simulated OP1dB and power gain of this gain stage line-up are shown in Figure 4.18 and Figure 4.19.

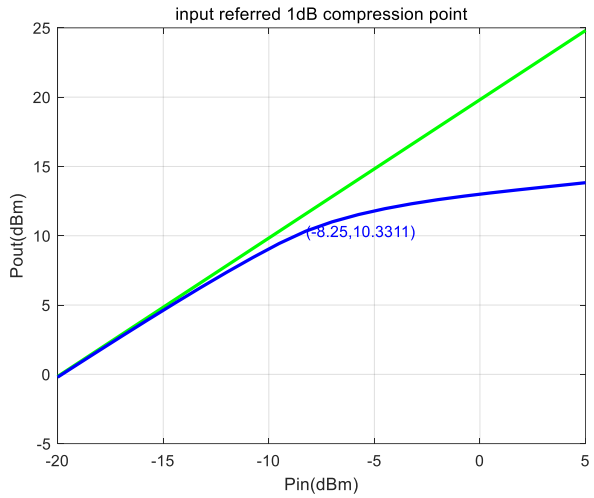


Figure 4.18: Simulated OP1dB of the three stages CE gain stage line-up

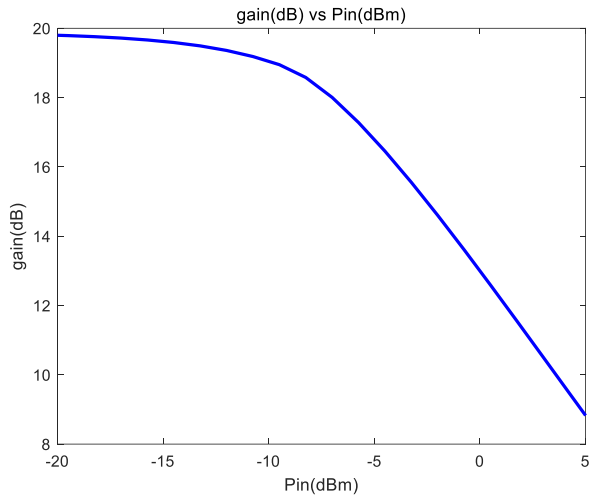


Figure 4.19: Simulated power gain of the three stages CE gain stage line-up

In Figure 4.20, the derivative of the power gain is compared between the designed gain stage line-up and the traditional gain stage line-up (size of each stage: 2, 4, 8 and 4, 4, 8). One can see that, with the help of the automated gain stage line-up, the linearity of the designed gain stages is improved compared to the traditional line-up.

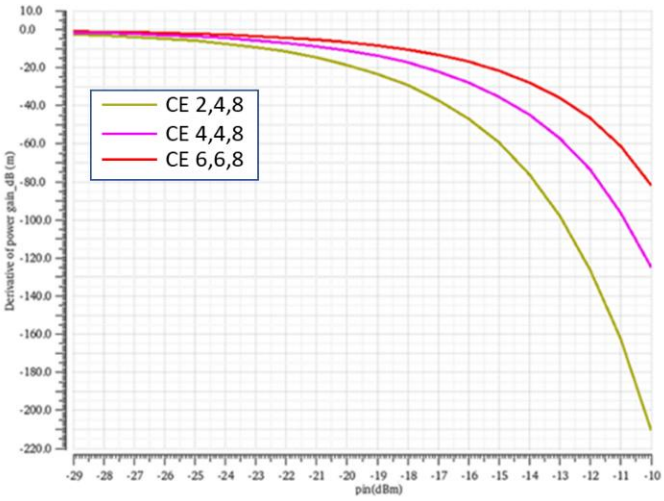


Figure 4.20: Derivative of the power gain

As we discussed in the previous section, the ocean scripted can be easily transferred through different technologies and topologies. By simply change the netlist in the ocean scripted, we can also get the result of the gain stage analysis of the cascode topology shown in Figure 4.21 and Figure 4.22, one can see that the cascode topology can achieve higher power gain and output power, which proves cascode is favourable to be the gain stage.

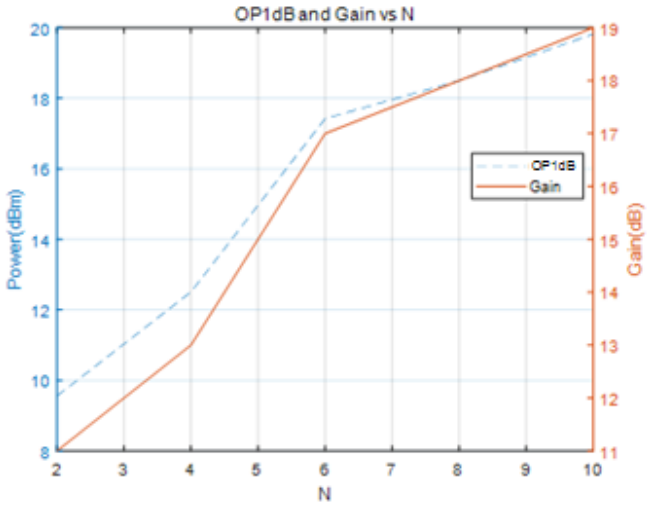


Figure 4.21: Gain stage analysis of the cascode under optimum load condition

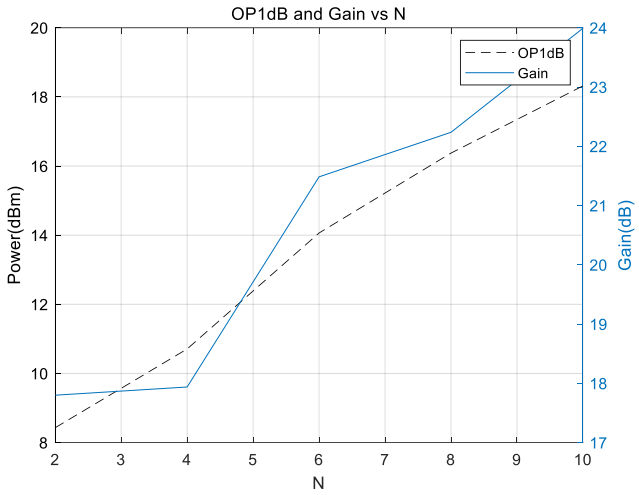


Figure 4.22: Gain stage analysis of the cascode under conjugate matching

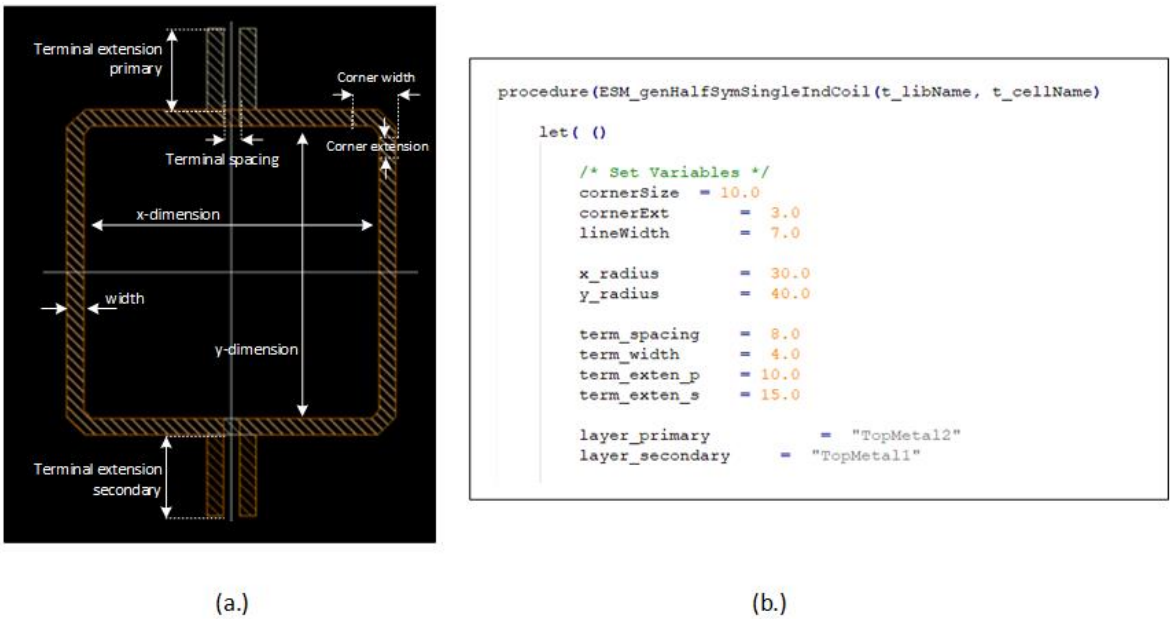
4.5 Skill code generated semi-parametrized layout

An integrated circuit design consists of two parts. The first is the schematic which describes the electrical behaviour of the circuit and which, if it is to accurately portray the behaviour of the final circuit, incorporates both the components available in the technology used, and the dominant parasitic components from the interconnections and environment. The second deliverable is a layout which represents the physical implementation of the circuit and describes the device and interconnect geometries within each layers of a process used. In essence the layout is thus a collection of coordinates representing the shapes in the layers.

As the shape of the components tends to correspond to the desire to elevate. i.e. make dominant, one particular facet of the electrical behaviour, each component, it being an inductor, capacitor or resistor, will many times end up having a similar shape. If such a geometry is then parametrized piece of code, it becomes possible to quickly generate modified version this shape as needed. During this work therefore several components and structures of which versions are present in the layout of a final design have been hard coded for the technology used. The available structures are a dual single coil stacked transformer, a ground-signal-ground-pad, a dc-pad and a ground pad and cells that implement ground planes. Using these sections of code, a significant part of the labour needed in realise a layout can be saved again allowing more time to use a critical design tasks.

4.5.1 Skill code for parametrized transformer

A transformer is commonly used component in mm-wave circuits where it is, amongst other things, used for impedance translation or for single-ended to differential conversion. The geometry of this component can be easily captured, provided a simple topology, with only a few parameters. An example of a dual single coil stacked transformer layout generated by skill code is given in Figure.4.23. This structure can be divided into two coils with a certain inner dimension of the coils and generated in a specified layer. These coils can in turn be sub-divided into corner and rectangular sections with a given width. The parameters of the skill code, which allows a bit more flexibility than just diameter and width, is given in Figure.4.23(b). For more of the code the reader is referred to appendix C.



(a.) (b.)

Figure.4.23: Partial code of the transformer layout generation

The benefit of having a parametrized function that generates the layout of such a transformer is that the electrical behaviour of this components is commonly using s-parameters generated by an EM-simulation. To fine tune it to its eventual configuration usually several iterations are required with small deviation in the geometry. Doing this several times by hand can be time consuming task which can now be diverted to other things thanks to the script. Figure 4.24 shows the final implementation of a transformer used in design that is presented in chapter 5 generated using the same script, thus showing the flexibility it provides.

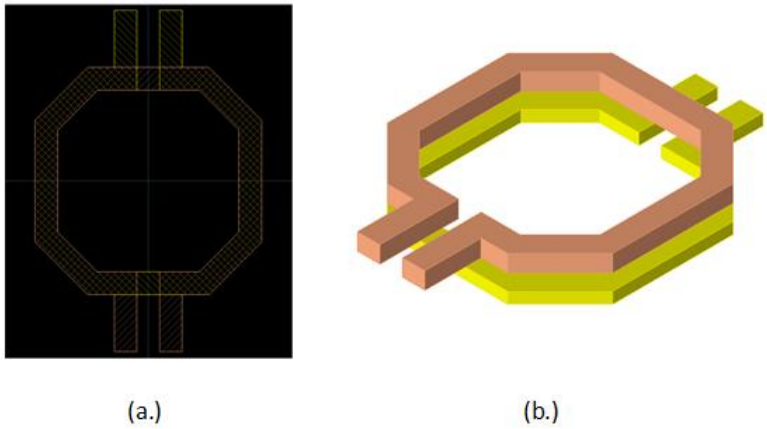


Figure 4.24: The final implementation of a transformer used in design

4.5.2 Skill generated pad ring structures

Another structure that lends itself for automated generation is the pads in the pad ring used to interface the chip to the outside world. The dimensions of these structures are set to accommodate the mechanical needs of the equipment used to interface with the chip during assembly or measurement. These dimensions tend to be relatively fixed and repetitive and can thus be captured in a parametrized piece of code. The example layout given in Figure 4.25 is generated using the pitch of the probes to be used in characterization and other trade-off corresponding to the measurement methodology used in the TU-Delft mm-wave laboratory. Partial code available in the appendix C.

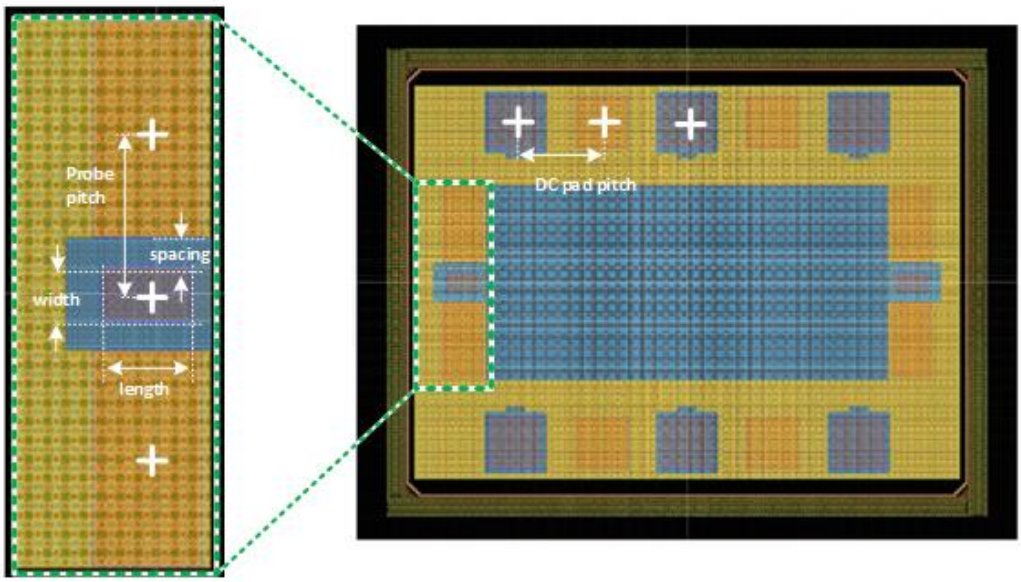


Figure 4.25: The example layout of Skill generated pad ring structures

4.5.3 Density tuneable sub-cells for ground plane implementation

Figure 4.26 presents the implementation of small xy-symmetric sub-cells with a tuneable metal density which can be used to implement ground planes throughout the chip design. The cell is implemented with very simple geometries such as cross and a donut shapes which have an area equal to the specified density in de code. Then connected together the from deign rule check (DRC) clean metal grid of the metals they are composed of. The thin metal cells are 2 µm x 2 µm in size and these are combined in a 5-by-5 matrix below donut and combined with cross shapes in thick metal shapes to from ground cells of 10 µm x 10 µm. If the remainder of the design and the RF-core of the circuit conform with a 2 µm and 10 µm grid a significant part the time that gets dedicated placing the functional part of the circuitry with the periphery around it , while potential modification can be made by modifying parts of the script.

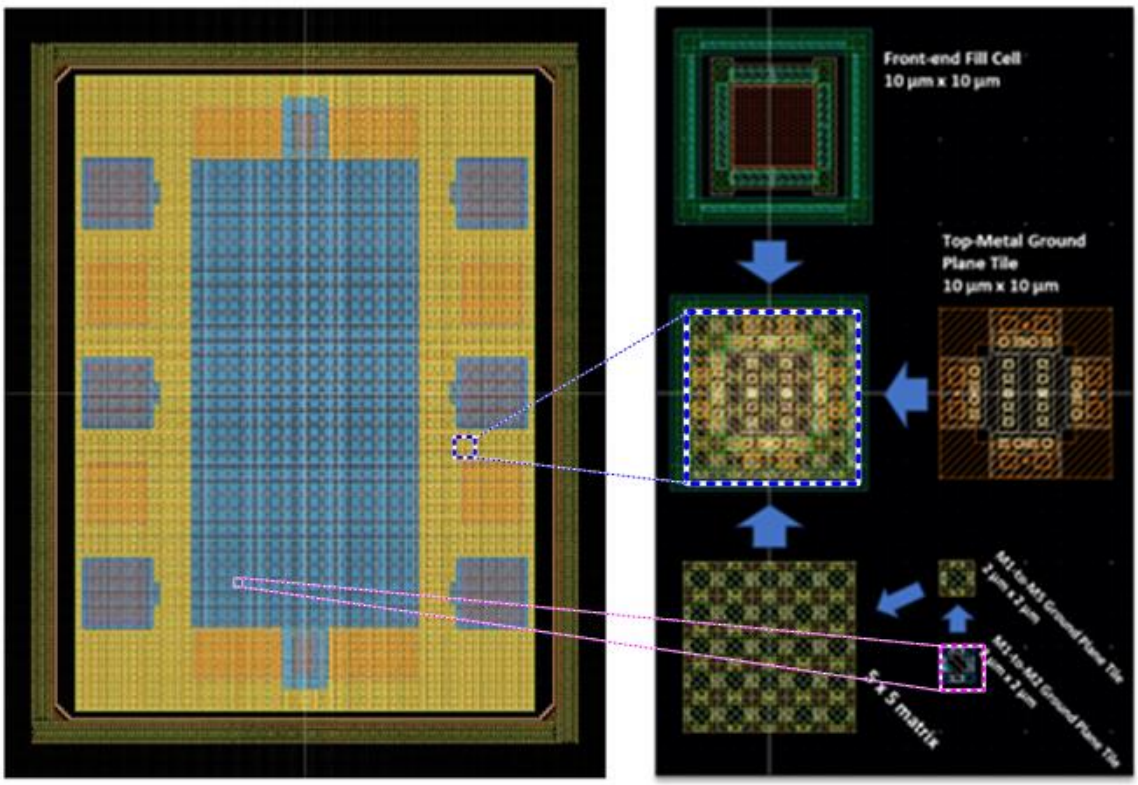


Figure 4.26: Skillcode layout generation in basic lego block

4.6 Conclusion

Before any continuous improvement in the design flow can be made, the consolidation through standardization should be first achieved. In this PA design automation flow, the standard sets of PA design techniques are first formalized and templated in order to be able to be accessed by the ocean scripting and skill coding. The ocean scripting and the skill coding tools can change the repetitive manual design work to a one-time-effort work, which can make the design flow easier and improve the design efficiency.

In this chapter, we first focus on the benefit of the scripted mm-wave design flows, such as one-time-effort, formalization of the standard design flow and the ability of transformation through different technologies.

Moreover, focusing on the high-level explanation of ocean script design flow for this 170GHz power amplifier. Finally, the Coded Generation of Tuneable Layout is proposed.

Even though, the complexity of mm-wave PA design is increasing. Expect for attaining the optimum performance with robust design models, faster time to market and higher design efficiency are also critical point and need to be considered by the PA designer.

With the help of the Skillcode, one can generate hundred ground cells, thousand ground cells and so on just by changing one number in the Skillcode with one-time effort. The Skillcode saves a lot of time for the repetitive structure layout such as transformer (purposed in Appendix B), In addition, the Skillcode can be transferable to the future project and other technologies by only changing the path of the basic geometries (Lego Blocks).

“Ocean” together with “Skill” compose the automation design flow.

As significant parts of the workload are shifted to writing code also the licencing time needed to finalize a design can be significantly reduced, which in a commercial environment and the licencing prices can potentially

References

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[2] Cadence, "OCEAN Reference" Product Cersion 5.1.41, June 2004.

[3] A. M. Niknejad and H. Hashemi, *mm-Wave silicon technology: 60 GHz and beyond*. Springer Science & Business Media, 2008.

[4] Y. Zhao, "High-Performance mm-Wave and Wideband Large-Signal Amplifiers," 2013.

Chapter 5.

Design of a 170 GHz Power Amplifier

The previous two chapters present both a possible design flow for mm-wave PAs and several ocean scripts to automate the recurring tasks within this flow to potentially reduce design time while simultaneously documenting the design for future reference. This chapter follows-up on these descriptions by presenting the use of this flow and the scripts in the design of a 170 GHz power amplifier in IHPs 130-nm SiGe BiCMOS process. At the end of this chapter expected performance of this design will then be compared to the performance of the power amplifiers selected for benchmarking in chapter 2.

5.1 Technology

The technology available for this design is IHP's SG13G2 technology. This is a 130-nm SiGe:C BiCMOS technology which features a silicon germanium hetero-junction bipolar transistor with a f_t and f_{max} of 300 GHz and 500 GHz respectively and has a collector-emitter breakdown voltage of 1.7 V. The active area of the HBT devices are fixed, so are not available as a design parameter, however layouts of multiple parallel devices are available in the pdk. The back-end-of-line (BEOL) of this technology is composed seven aluminium metal layers. The first five of these layers are thin metals and the top two being thick metals with a height of 2 µm and 3 µm. The highest of these layers is separated from the substrate by approximately 10 µm which together with the thickness makes this BEOL quite suitable for the implementation of high-quality passives. The technology comes with a further complement of MIM capacitor, varactors and a p-type poly and high resistance poly resistors.

5.2 Schematic design

The simplified schematic of the power amplifier resulting from the design flow and scripts is presented in Figure 5.1. The figure shows the power amplifier to be implemented using two cascode gain stages. The first gain stage is matched to a preceding 50-Ω source impedance using a balun. The two stages themselves are matched using a transformer while the output of the second stage interfaces to an envisioned antenna using a transmission line-based matching scheme. The remainder of this subsection used to describe the design in detail from the output to the input as this work covers the design of a power amplifier where delivering the desired power at the output with a prescribed level of linearity is of prime concern.

Firstly, the load. The power amplifier is envisioned to operate with a on-chip antenna as load. The expected impedance of this load is expected to be similar to that impedance of the antenna realized in [1]. The operating frequency of 170 GHz, results in an effective wavelength and a quarter-wavelength, i.e. the size deemed necessary for the theoretical dipole antenna approximately 861 µm and 215 µm respectively, within the stratification of the integrated technology. This therefore allows the realisation of the on-chip antenna within dimensions similar to that of an inductor or transformer and can thus be said to have dimensions that could be deemed economically acceptable. Integrating the antenna together with the transmitter on the same die has several benefits. The losses usually incurred when providing a transition from the chip to stratification, be it, a PCB , or a can be avoided [ref] [ref]. Similarly, when using a transformer, the symmetry of an antenna geometry can be used to implement a RF cold point, i.e. a point in the rf current chancel out, which can be used to provide a confinement bias point thereby avoiding the need for additional components otherwise needed for this purpose as done. Lastly, the antenna design can take advantage of both the fine feature size, order of nanometres instead of micrometres, allowed by the lithography process used to for monolithic circuits to realise more complex structures while simultaneously also obtaining the higher repeatability in the vertical dimensions of the stratification these technologies also provide.

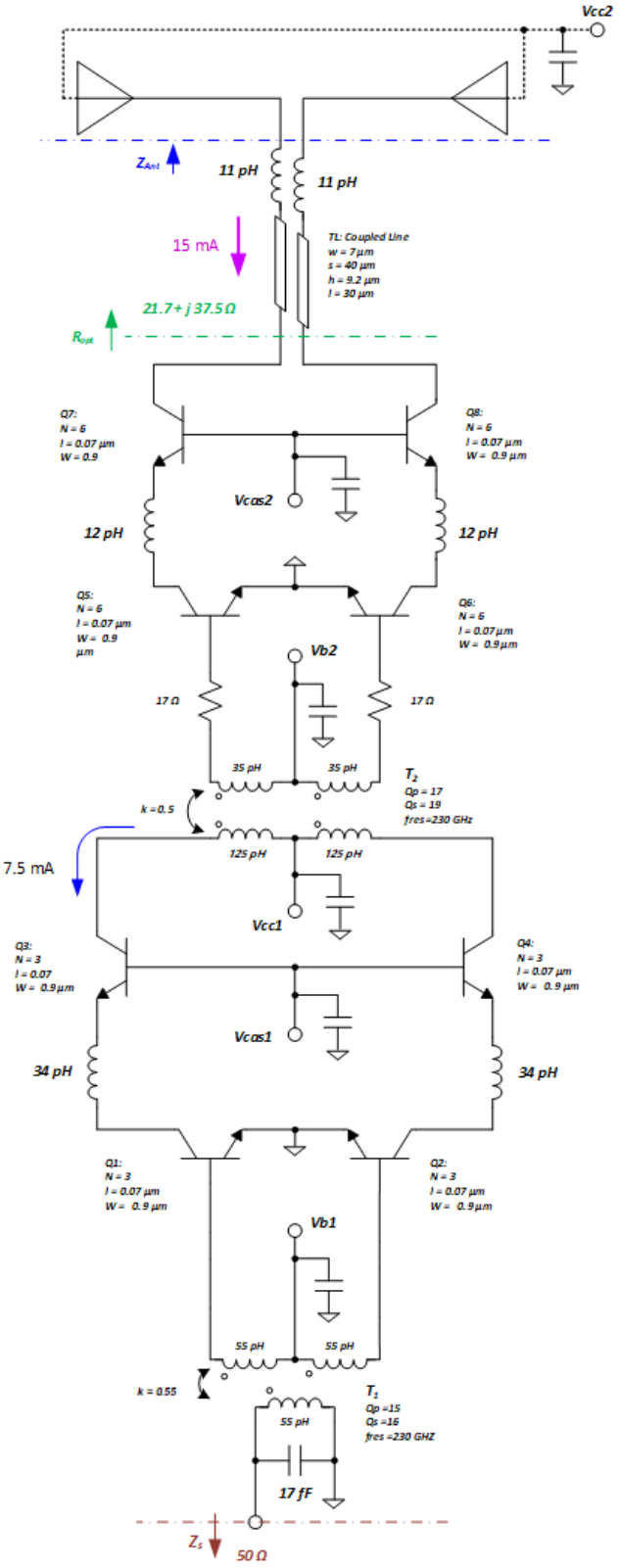

Figure 5.1: Simplified schematic of power amplifier with antenna as load

The output stage of the power amplifier consists of a differential cascode. This gain stage topology was selected from other alternatives such as the common-emitter, common-base evaluated in the gain stage analysis as it is able to provide. Figure 4.21 illustrate the result of the gain stage analysis of the differential cascode topology with loadline matching for the output stage of the PA. In order to achieve the requirement of +12dBm OP1dB, considering an around -5dB insertion loss which will be added into the PA system with the output transmission line matching network, the output stage of the PA is selected to be a differential cascode with 6 multipliers with OP1dB of +17 dBm. The input stage of the PA is then selected to be a differential 3 parallel cascode with OP1dB of +9 dBm and a power gain of 18dB. During the analyses also the required number of parallel devices to reach the desired linearity and output power was set to also the number of parallel devices is selected.

Chapter four presented several ocean scripts which are applied to the design of the 170 GHz power amplifier in this chapter. Automated task is bias point analysis, gain stage topology evaluation, large signal load-line matching analysis, gain stage analysis. From the topology analysis, it is found that cascode topology is the most favourable topology in order to obtain the desired 1dB-compression ($\mathrm{P_{1dB}}$).

Combine with the biasing analysis and gain stage analysis, we decided to have the output stage with a 6-parallel cascode configuration biased at 15 mA to achieve a +16 dBm output signal at 1dB compression point, and an input stage with a 3-parallel cascode configuration biased at 7.5 mA to achieve a +8 dBm Op1dB. The size of all the transistors in the input and output stage are summarized in Table 4.

Table 4 Transistor size summary

Transistor Number	Size (μm^2)
Q1 – Q4	$3 \times 0.07 \times 0.9$
Q5 – Q8	$6 \times 0.07 \times 0.9$

To guarantee unconditional stability of the output stage, a 10 Ohm resistor is in series with the base of CE transistor to improve the stability factor K from 920m to

1.5, as shown in Figure 5.2. Instead of Gatepoly resistor, the 10 Ohm resistor is realized by adding vias connection.

From loadline matching analysis, we found out the optimal resistance R_{opt} for the output cascode stage should be (21.7+j37.5) Ohm. 12 pH inductors and A coupled transmission line with a impedance of 75 Ohm are used to match the input impedance (20-j12) Ohm of the antenna [3], shown in Figure 5.3, to R_{opt}.

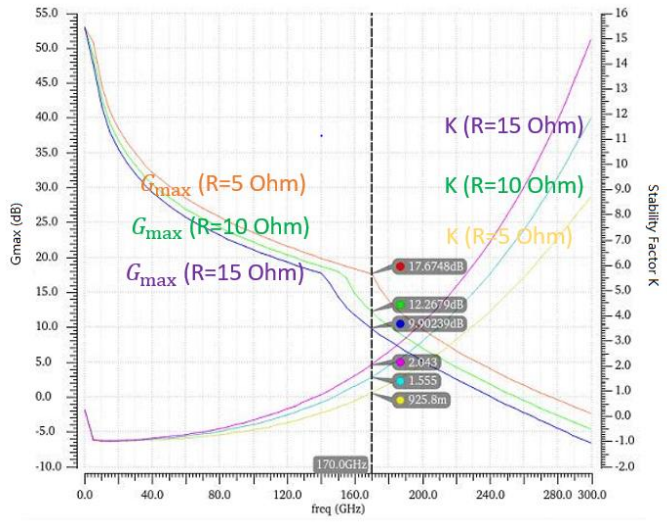

Figure 5.2: Improved stability using resistor at base of CE transistor

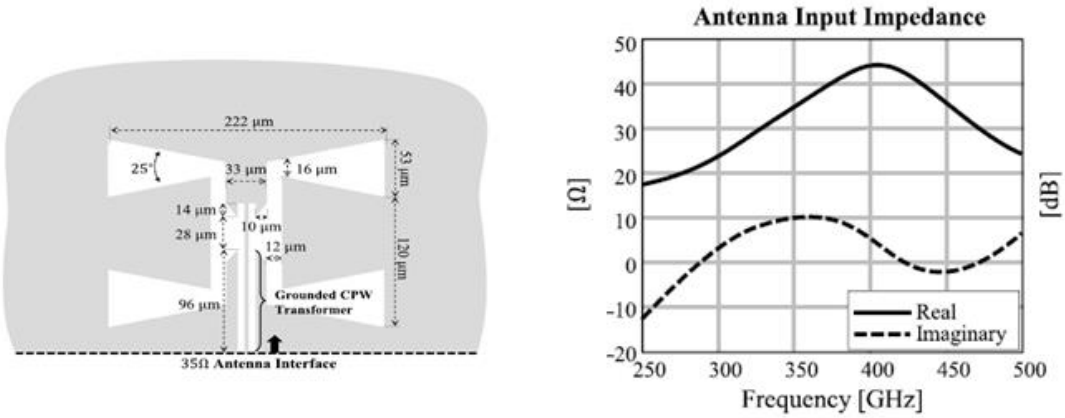

Figure 5.3: A CPW-fed antenna [3]

The intermediate matching network is realized with a center-tapped transformer with a winding diameter of 40 um and a winding diameter of 2 um, while the input matching network is realized with one center-tapped balun with a winding diameter

of 45 um and a winding width of 6 um. The selection of the transformer and the balun are discussed in the following sections.

5.2.1 Intermediate Matching Network Design

The main aim of the transformer is to minimize the power loss in between two stages. There are two basic transformer structures we can choose from to do the intermediate matching network design, stacked transformer and interleaved transformer, which are shown in Figure 5.4. According to [4], compared to an interleaved transformer, a stacked transformer is favourable due to higher coupling factor between the primary winding and the secondary winding, which can reduce the power loss.

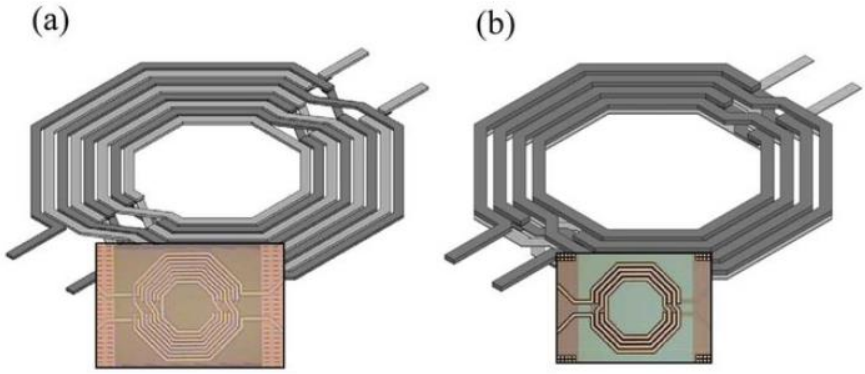

Figure 5.4: 3D view of (a) interleave transformer, (b) stacked transformer [5]

As shown in Figure 5.1, a center-tapped stacked transformer with a coupling factor of 0.5 is used to match the output impedance of the input stage to the input impedance of the output stage the impedance of which are shown in Table 5.

Table 5 Small signal impedance level of the input and output stage at 170GHz

	Small Signal Impedance
Z_{out} **of the input stage**	4 - j148
Z_{in} **of the output stage**	71 - j21

Since then, from the calculation,

$$n = \sqrt{\frac{Re[Z_{out}]}{Re[Z_{in}]}} = \sqrt{\frac{71}{4}} \approx 4 \quad \text{(eq. 16)}$$

the transformer should have a transformation ratio of 1-to-4.

To indicate the primary inductance L_P, the secondary inductance L_S, the primary resistance and the secondary resistance, the transformer can be modeled as shown in Figure 5.5.

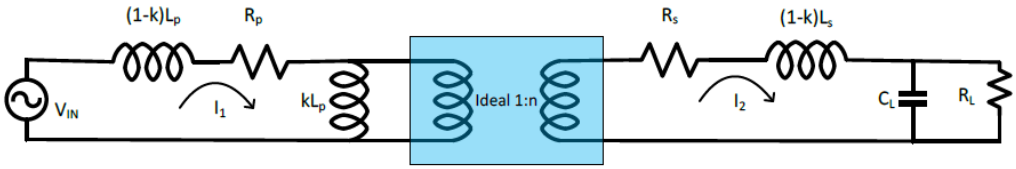

Figure 5.5: Transformer model [6]

From the equation of the resonant frequency f_{SR}

$$f_{SR} = \frac{1}{2\pi\sqrt{(1-k)L_S C_{eq}}} \quad \text{(eq. 17)}$$

Where the C_{eq} is the series load capacitance and can be calculated as

$$C_{eq} = \frac{1 + (wR_L C_L)^2}{w^2 R_L^2 C_L} \quad \text{(eq. 18)}$$

$$w = 2\pi f_{SR}$$

With k of 0.45, from the calculation, we can get L_S should be 40 pH.

To reach a transformation ratio 1-to-4 and the maximum power efficiency. From the equation below

$$L_P = \frac{1-k}{k}\frac{L_S}{n^2}2\pi f_{SR} \quad \text{(eq. 19)}$$

We can get L_P should be 2.6 pH, which means the transformer would be unfeasibly small.

To get a compromise, we will design the transformer based on the resonant frequency f_{SR} with an L_P of 250 pH.

5.2.2 Input Matching network design

To match the input impedance (53 – j20) of the PA to the characteristic impedance of 50 Ohm and convert the single-ended signal to the differential signal, one centre-tapped balun resonant with the parasitic capacitance of the Ground-Signal-Ground (GSG) pad shown in Figure 5.6 is designed. The dimension of the GSG pad and pad capacitance is given in Table 6.

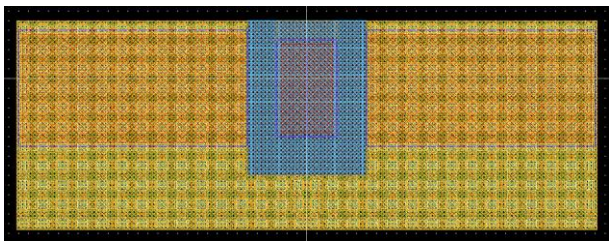

Figure 5.6: GSG pad structure

Table 6 Dimension of the GSG pad

GSG Pad parameters	Value
Ground Pad Dimension	115 x 60 $\mu\mathbf{m}^2$
Centre to Centre Pitch	90 $\mu\mathbf{m}^2$
Pad Capacitance	16.23 fF

Like the calculation discussed in 5.1.1, the transformation of this balun is chosen to be 1-to-1 and L_P, L_S should be 54 pH and 108 pH.

Not like the transformer designed for intermediate matching, the phase and amplitude imbalance which is caused by the inter-winding capacitance are also important to measure the performance of the balun.

For an ideal balun, the signal amplitude difference of two differential ports should be 0 and the phase difference should be 180 degrees. With the consequence of the imbalance, the amplitude and phase difference of two differential ports are no longer 0 and 180 degree.

Assuming port 1 is the single-ended port, port 2 and port 3 are the differential ports, the amplitude imbalance (AI), phase imbalance (PI) and insertion loss (IL) can be computed as in

$$AI = \left|\frac{S_{31}}{S_{21}}\right| \quad \text{(eq. 20)}$$

$$PI = \angle\left(-\frac{S_{31}}{S_{21}}\right) \quad \text{(eq. 21)}$$

And insertion loss

$$IL = \frac{S_{31}}{2} \quad \text{(eq. 22)}$$

To reach the L_P and L_S calculated before, three cases are studied: winding width/winding diameter are respectively 2 µm/30 µm, 4 µm/40 µm, 6 µm/45 µm.

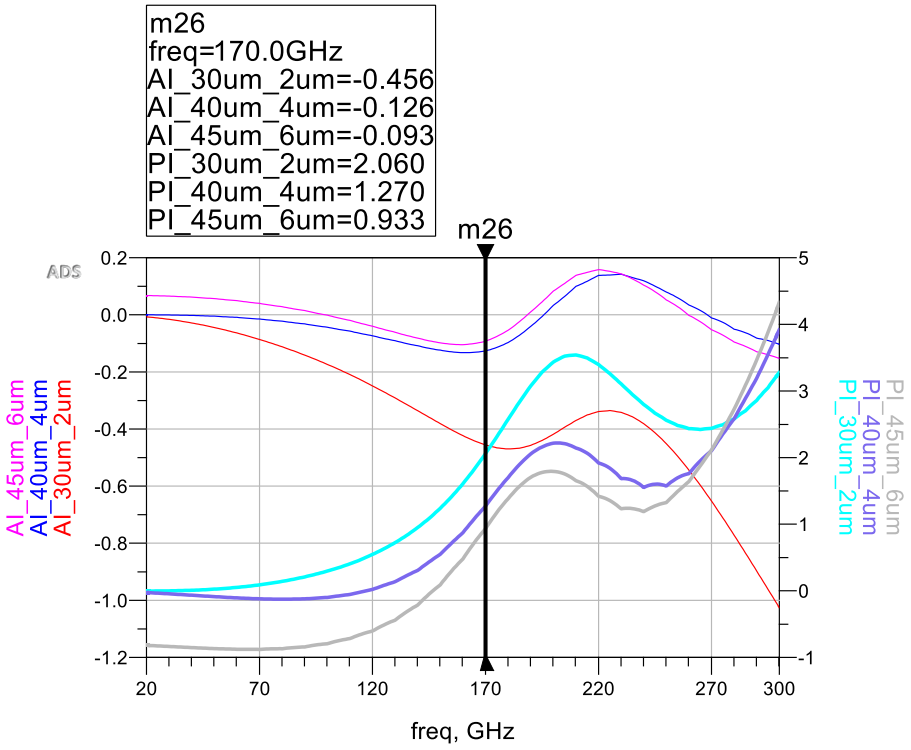

Figure 5.7: Simulated imbalance using different winding dimensions

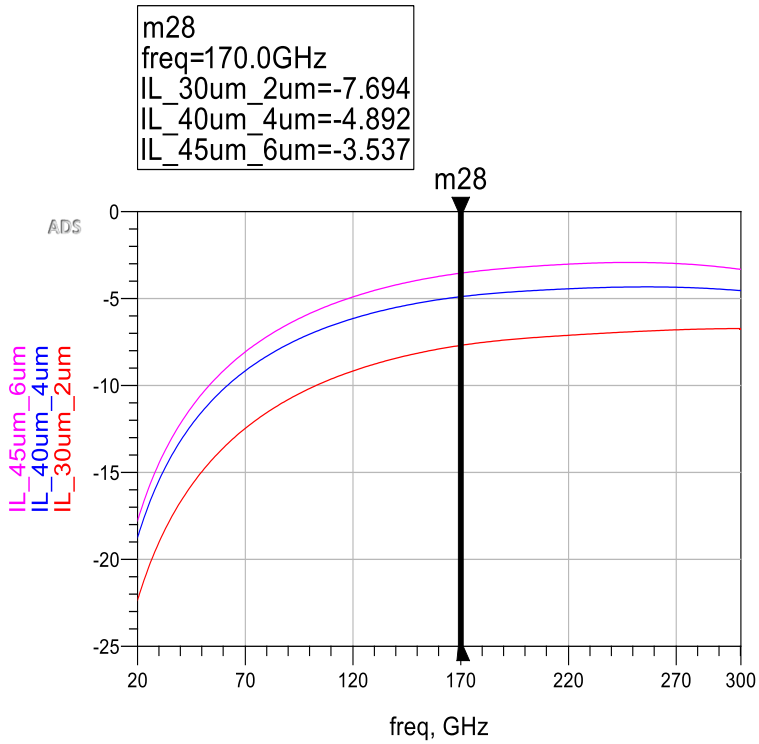

Figure 5.8: Simulated insertion loss for different possible winding dimension

The EM-Simulation results of those three cases are illustrated in Figure 5.7 and Figure 5.8.

One can observe that, with the same L_P value, at 170GHz the winding with a width/diameter of 6 µm/45 µm shows lowest amplitude imbalance, lowest phase imbalance and lowest insertion loss among those three configurations. But it can also be observed that the winding size only has little influence on the amplitude imbalance and phase imbalance, though it has a clear effect on the insertion loss.

Thus, the balun design with a winding width of 6 µm and a winding diameter of 45 µm is chosen.

5.3 Layout design

As discussed in the previous chapter, unlike low-frequency design, in the mm-wave design the layout parasitic has a deep influence on the performance of the device.

In this section, the device performance metrics for the cascode topology is discussed. Then, the layout techniques of the important sub-blocks of the PA are illustrated.

5.3.1 Layout of the cascode topology

As we have discussed in the previous chapter, f_t *and* f_{max} are two important metrics which define the power gain performance of the device. f_T and f_{max} are defined in

$$f_t = \frac{1}{2\pi \cdot \tau_{BC}(J_C A_E) + \frac{kT}{qJ_C A_E}(C_{BE} + C_{BC}) + (R_E + R_C)C_{BC}} \quad \text{(eq. 23)}$$

and

$$f_{max} \approx \sqrt{\frac{f_T}{8\pi R_B C_{BC}}} \quad \text{(eq. 24)}$$

τ_{BC}: the base-collector transient time,

J_C: the collector current density,

A_E: the emitter area,

C_{BE}, C_{BC}: total base-emitter, total base-collector capacitor

R_B, R_C and R_E: base, collector and emitter resistor

From the equations, one can see that C_{BC} shows the main effect on the value of f_T and f_{max}, moreover R_B also shows the effect on the value of f_{max}. In the layout design, R_B and C_{BC} need to be minimized to reduce the gain loss. Moreover, as shown in Figure 5.9, by ignoring other parasitic component expect for C_{m1} and C_{m2} which are the emitter to ground parasitic capacitance of the CB stage and the collector to ground parasitic capacitance of the CE stage. Since RF current will bypass through C_{m1} and C_{m2} to the ground, C_{m1} and C_{m2} cause the power loss in between CE and CB stages. Adding inductance L_m in between CB and CE stage can cut the direct connection between CB and CE stage where C_{m1} and C_{m2} are neutralized. Thus, high-frequency gain attenuation can be compensated. From the equation

$$\frac{u_{out}}{u_{in}} = \frac{g_{m1} Z_{e2} \frac{1}{jwC_{m2}}}{Z_{e2}\left(1 + \frac{C_{m1}}{C_{m2}} - w^2 L_m C_{m2}\right) + j(wL_m \frac{C_{m1}}{C_{m2}} - \frac{1}{wC_{m2}})} \quad \text{(eq. 25)}$$

One can get the value of L_m, as shown in equation

$$L_m = \frac{C_{m1} + C_{m2}}{w^2 C_{m1} C_{m2}} \quad \text{(eq. 26)}$$

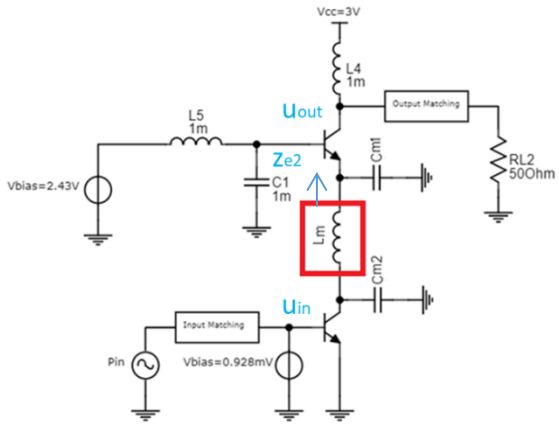

Figure 5.9: Collector to ground parasitic capacitance in cascode Topology

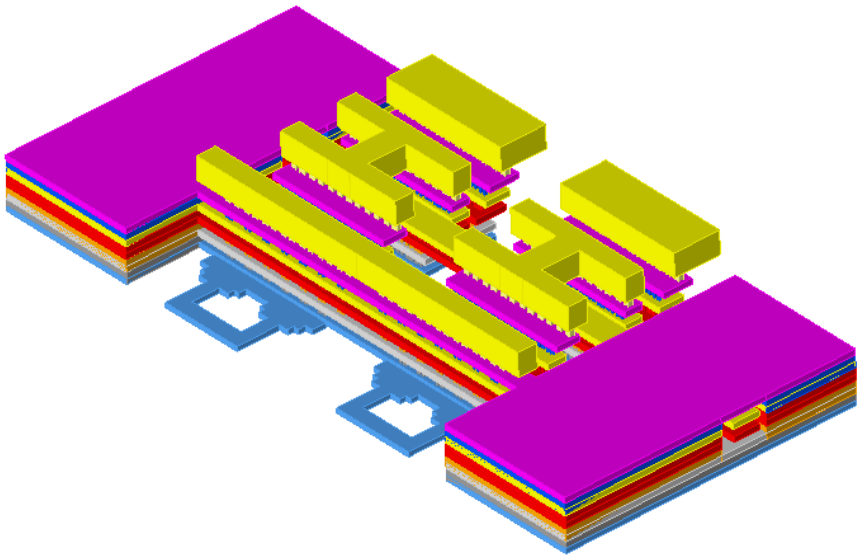

Figure 5.10: Layout of the cascode

Figure 5.10 illustrates the layout of the cascode configuration. The connection between the collector of the CE stage and the emitter of the CB stage is implemented on top metal 1, which introduces the L_m in between CE and CB stages. The Manhattan structure shown in Figure 5.11 implemented for the base connection of the CE stage, for the parasitic capacitance and inductance minimization. As illustrated in [6], the “sandwich” structure shown in Figure 5.12 could introduce decoupling capacitor closed to the base of the CB stage and reduce

the base parasitic inductance by minimizing the current loop, which contributes to the stability performance of the cascode stage.

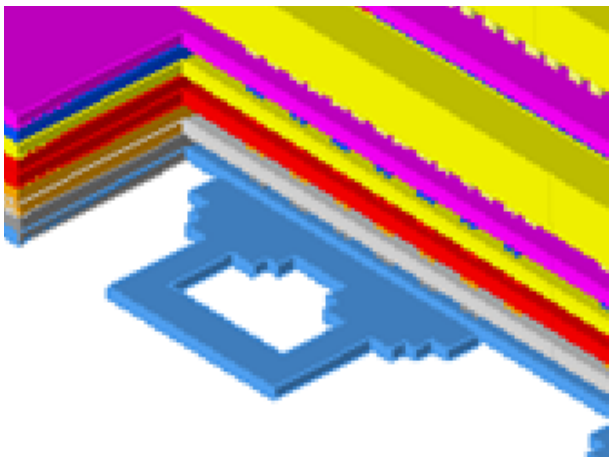

Figure 5.11: Manhattan structure

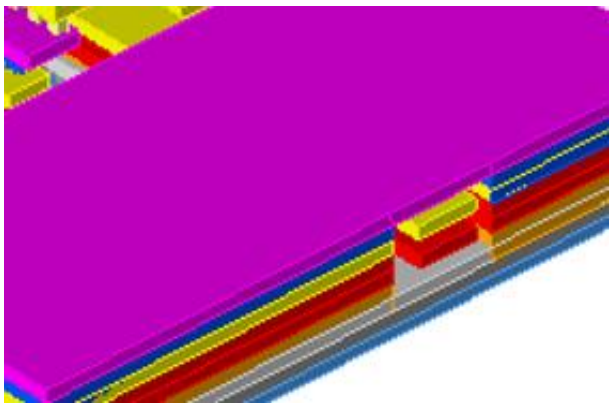

Figure 5.12: "Sandwich" layout technique

Figure 5.13 shows the layout of the inner-stage matching network. The layout of the transformer is generated automatically with the SkillCode presented in Appendix B. To meet the requirement of the performance discussed in the previous section, the transformer is selected to have a winding diameter of 40 um and a winding width of 2 um. In case of the input balun shown in Figure 5.15, the winding diameter is selected to be 45 um and the winding width is selected to be 6um. As shown in Figure 5.14, the transformer in the inner-stage matching network presents an insertion loss of 5.6 dB. And as shown in Figure 5.16 and Figure 5.17, the input balun presents an insertion loss of 3.28 dB, an amplitude imbalance of 0.5 dB and a phase imbalance of 11.8 degrees.

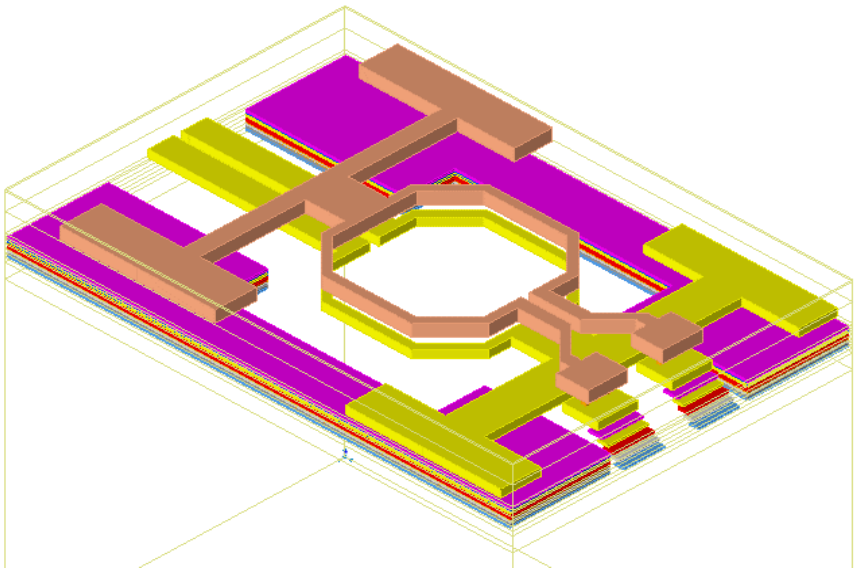

Figure 5.13: Layout of the inner-stage matching network

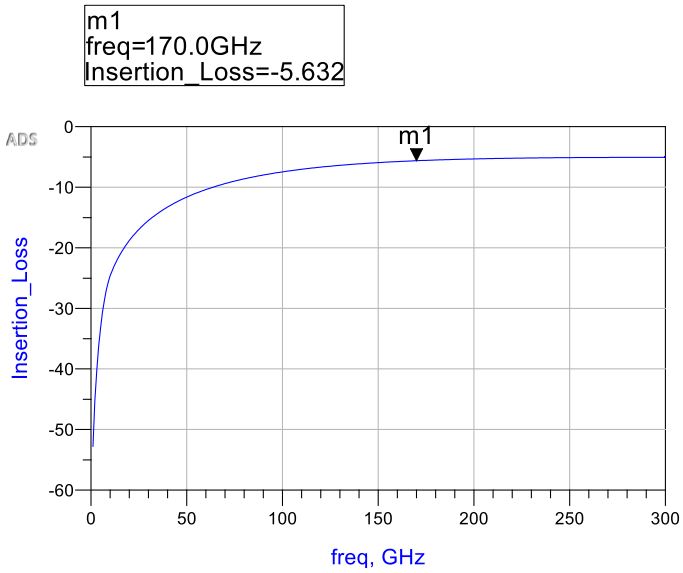

Figure 5.14: Simulated insertion loss of the inner-stage matching network

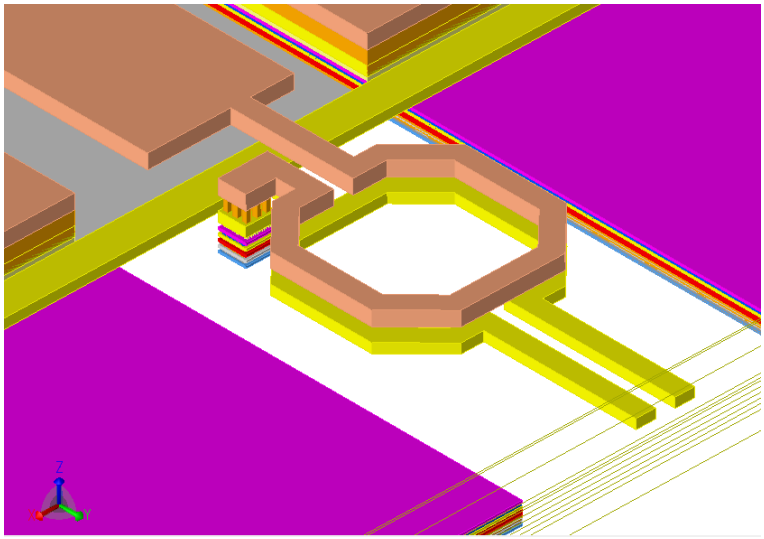

Figure 5.15: Input matching network

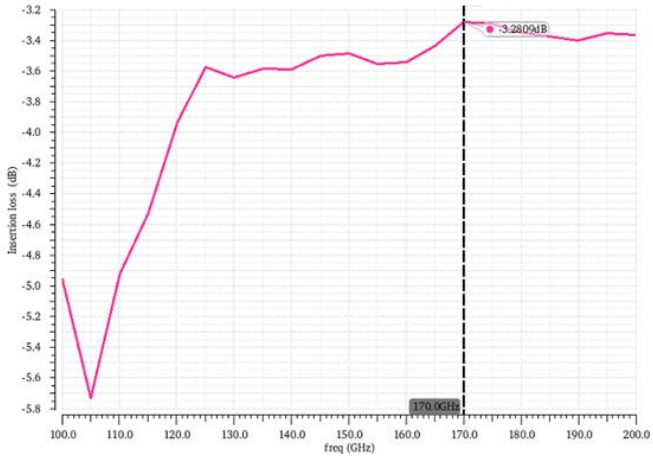

Figure 5.16: Simulated insertion loss of the input matching network

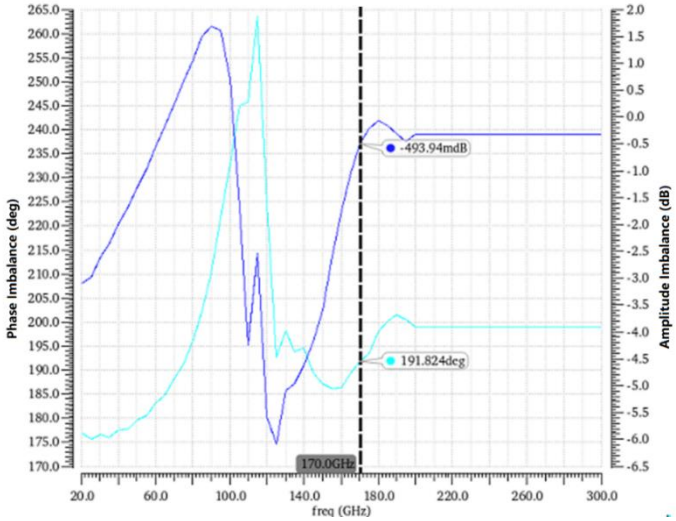

Figure 5.17: Simulated imbalance of the input matching network

Figure 5.18 shows the layout of the output TL matching, the coupled line matching the input impedance of the antenna to R_{opt} has a characteristic impedance of 75 Ohm and an insertion loss of 6 dB

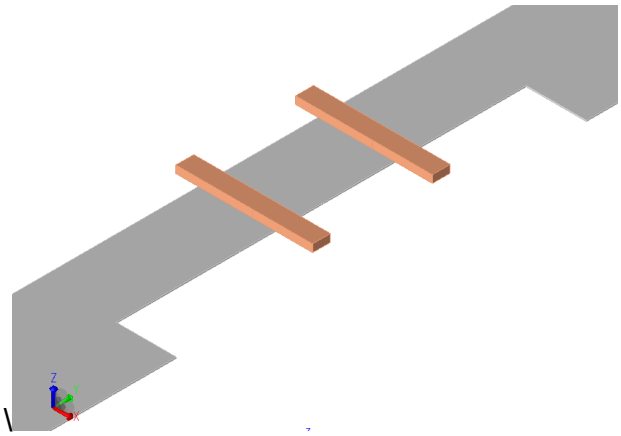

Figure 5.18: Layout of the output TL matching

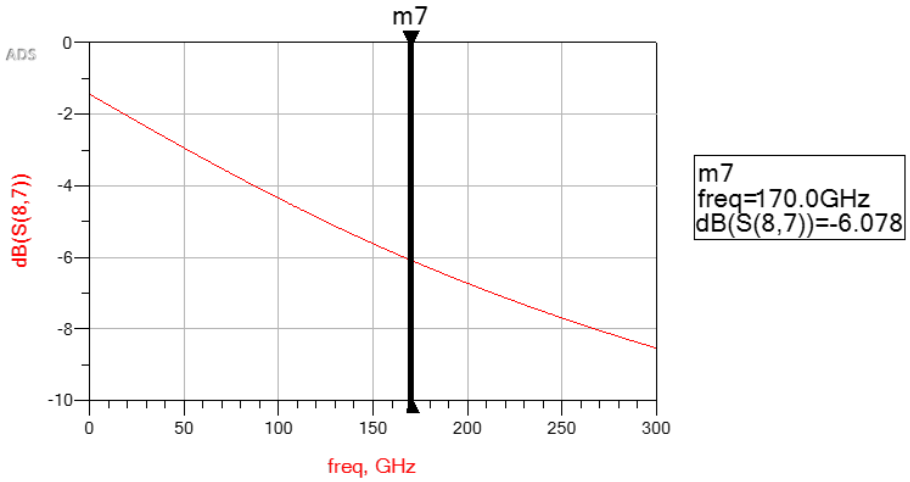

Figure 5.19: Simulated insertion loss of the output TL matching

With the help of the Ocean script presented in Appendix A, the small-signal performance and the large-signal performance of the power amplifier are simulated and shown below.

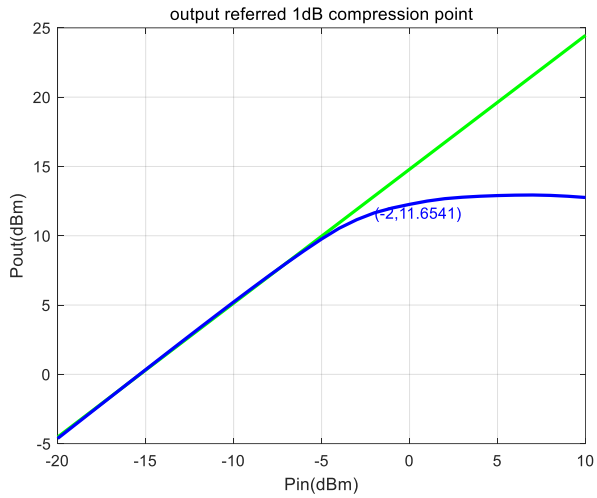

Figure 5.20: Simulated output power vs input power

Figure 5.20 purposed that the power amplifier could achieve an output referred 1dB compression point of 11.7 dBm with a Psat of 13 dBm. Figure 5.21 shows the value of the large-signal power gain at 170 GHz which is 13.7 dB.

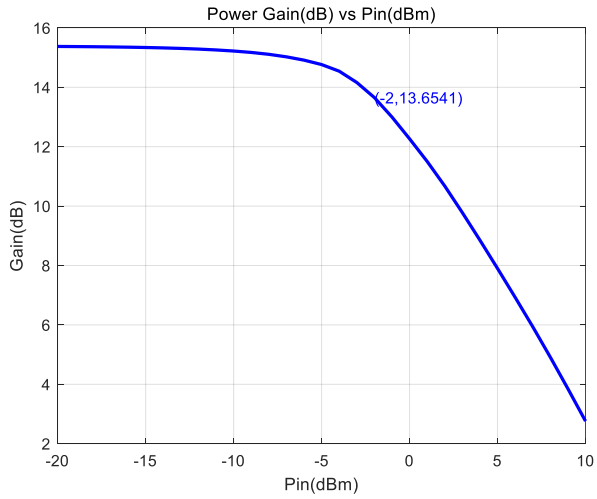

Figure 5.21: Simulated power gain vs input power

Figure 5.22 shows the value of the small-signal gain (S21) versus frequency. The peak S21 is around 15 dB at 166GHz and the PA has a -3dB bandwidth (from 146GHz to 182GHz) of 36 GHz. As shown in Figure 5.23, the reverse isolation (S12) of the power amplifier is small than -68 dB.

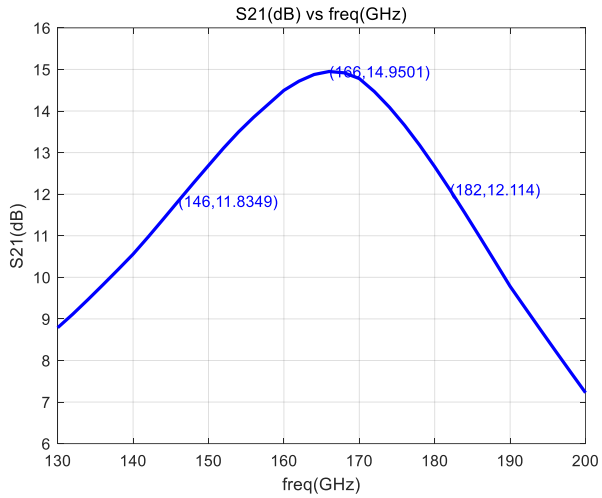

Figure 5.22: Simulated small signal gain (S21)

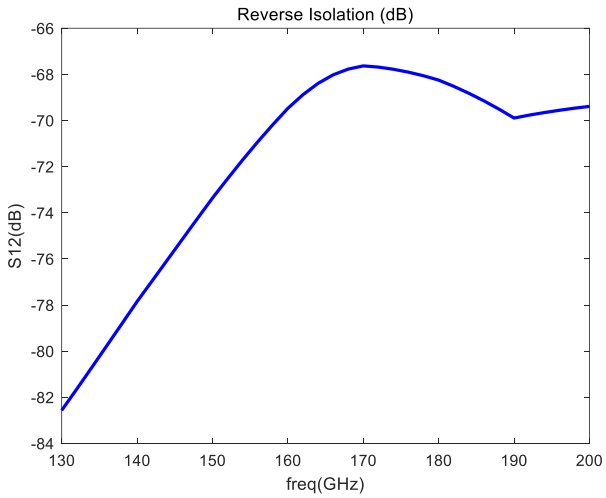

Figure 5.23: Simulated reverse isolation (S12)

As mentioned before, to ensure the system could be unconditional stable, the stability factor K>1 and $|\Delta| < 1$. Thus, from Figure 5.24 and Figure 5.25, one can see that the power amplifier is unconditional stable.

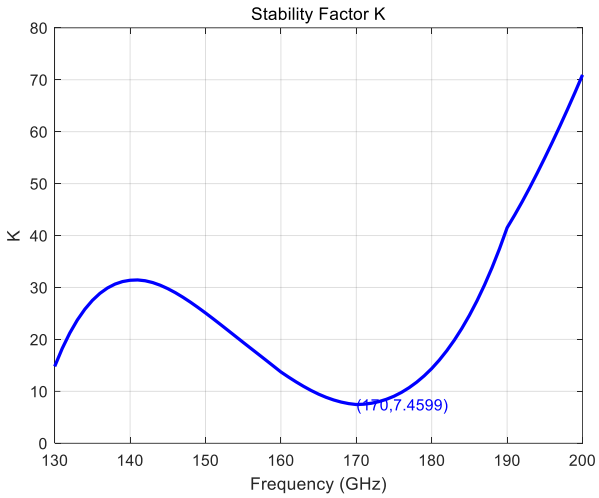

Figure 5.24: Simulated stability factor K

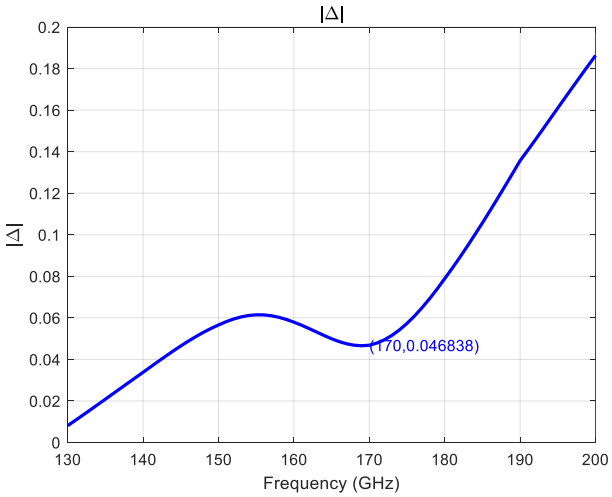

Figure 5.25: Simulated |Δ|

Figure 5.26 presents the peak power added efficiency of the PA is 12.8%, while at the 1dB compression point, the value of power added efficiency reduces to 11%.

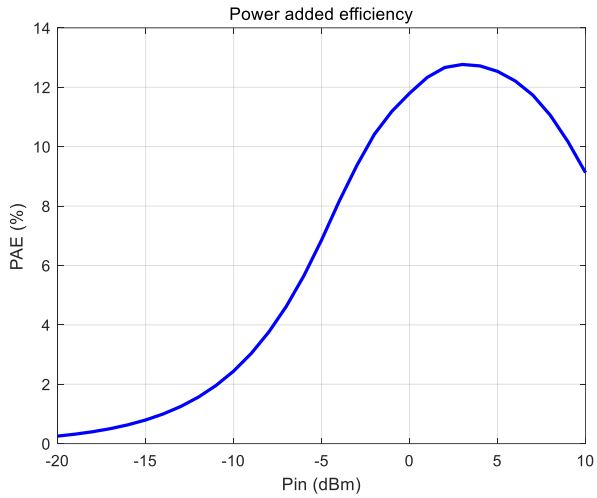

Figure 5.26: Simulated power added efficiency (PAE) vs input power

The performance of the 170GHz power amplifier designed in this work is then compared with the state-of-art is shown in the below table.

Table 7 Table of comparison

Ref	Tech (nm)	Freq (GHz)	Gain (dB)	P_{-1dB} (dBm)	P_{sat} (dBm)	Peak PAE	Topology
[7]	130 SiGe	160	20	8.5	10	-	3-stage Differential cascode
[8]	130 SiGe	138-175	25.7	16	18	19%	4-stage single-ended CE
[9]	40 CMOS	140	20.3	10.7	14.8	8.9%	3-stage 2-way differential cascode
This Work	130 SiGe	170	15	11.7	13	12.8%	2-stage differential cascode

Conclusion

In this chapter, we will present a 170-GHz Power Amplifier design in 0.13-μm SiGe BiCMOS with 15 dB power gain and 11.7 dBm output 1dB compression power. This design applies automation design flow which we have described in chapter 4.

This PA includes two cascode stages to achieve a power gain of 15dB. one transmission line with 5dB insertion loss is designed, to match the input impedance of one differential antenna described in [3] to R_{opt}. The input and intermediate matching network are generated by the Skillcode which saves a large amount of time. The intermediate matching network is realized by a centre-tapped stacked transformer with an insertion loss around 7 dB [10]. To convert an unbalanced single-ended signal to a balanced differential signal at the input of PA, we designed one centre-tapped balun.

It can be seen in the design process that, the automation design flow saves a lot of initial analysis time and layout generating time.

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Chapter 6.

Conclusion

This chapter briefly summarizes the work proposed in this project. The contributions of this work along with the future improvement opportunities are also briefly presented in this chapter.

6.1 Contributions & Conclusions

This paper presents a 170GHz two-stage differential cascode PA in IHP's SG13G2 technology using automation scripts, which include ocean script and skill code.

The proposed two-stage power amplifier achieved 15 dB gain at 170GHz with a-3dB bandwidth of 36 GHz. The output 1dB compression point is 11.7 dBm and the achieved saturation power is 14.8 dBm with a peak PAE of 12.8% at 170GHz.

In this work, the ocean scripting and the skill coding tools help to reduce the amount of repetitive manual design work to a one-time-effort work. By isolating and automating some repetitive task such as gain stage evaluation and coded generating the tuneable layout such as transformer, the design efficiency is much improved with the automation design flow proposed in this work.

Moreover, this approach has more benefits such as hard-coded settings and being transferable through different technologies and topologies, easing inter-team communication and significantly less button pushing.

6.2 Future work

The automation design flow can be improved in several ways as below.

The automation design flow proposed in this work could be transferred to other topologies and technologies. For future work, we would like to improve the capability of this automation design flow by transferring it to other technologies.

One problem we found in the automation design flow is that the format of the Output data from Ocean does not match the MATLAB code available plotting Smith Chart. For the future work, we would like to automate loadpull step to find gain stage optimum load.

Appendix A - Ocean Script for the PA design

Partial code for Stage Analysis

```
/*
Run Command:

load("/users/xtong/cadence_work62/OceanScripts/old_versions/Xtong_main_loop_outin_loadline.ocn")

remove the dictionary

;csh(strcat("rm -r path/filename"))

csh(strcat("rm -r /users/xtong/cadence_work62/OceanScripts/SimData_Cascode"))
================================================================================
*/


/* Set Path  for the script */
OceanPath = "/users/xtong/cadence_work62/OceanScripts/"

/* Set Path  for the function */
functionPath = "/users/xtong/cadence_work62/OceanScripts/functions/"

SimDataFolder = strcat(OceanPath "SimData_tries/" )

/* load all the functions */

    load( strcat(functionPath "Xtong_Sparameter_StaF1.il"))
    load( strcat(functionPath "Xtong_Sparameter_Y.il"))
    load( strcat(functionPath "Xtong_Sparameter_S.il"))
    load( strcat(functionPath "Xtong_Sparameter_S21.il"))
    load( strcat(functionPath "Xtong_Sparameter_ZOUT_IN.il"))
    load( strcat(functionPath "Xtong_Sparameter_ZIN.il"))
    ;load( strcat(functionPath "Xtong_Sparameter_PoutindBm.il"))
    load( strcat(functionPath "Xtong_Sparameter_hbPout.il"))
    load( strcat(functionPath "Xtong_Sparameter_Pdc.il"))
    load( strcat(functionPath "Xtong_Sparameter_Ropt.il"))


Vdd = 3

freq = 180G

/*
simulator( 'spectre )
design(  "/users/xtong/cadence_work62/sim/Volt_biasing/spectre/schematic/netlist/netlist")
resultsDir( "/users/xtong/cadence_work62/sim/Volt_biasing/spectre/schematic" )
path( "/data/cad/DesignKits/IHP/v0.6/SG13G2_617_rev0.9.0_a/lib/TL_SG13/RLCG/spectre/" )
modelFile(
    '("$IHP_TECH/tech/SG13_MOS/library/spectre/cornerMOSlv_psp.scs" "tt")
    '("$IHP_TECH/tech/SG13_MOS/library/spectre/cornerMOShv_psp.scs" "tt")
    '("$IHP_TECH/tech/SG13G2_PASSIVES/spectre/SG13_cornerRES.scs" "typ")
    '("$IHP_TECH/tech/SG13G2_PASSIVES/spectre/SG13_cornerCAP.scs" "typ")
    '("$IHP_TECH/tech/SG13G2_PASSIVES/spectre/SG13_dschottky_nbl1.lib" "")
    '("$IHP_TECH/tech/SG13G2_PASSIVES/spectre/SG13_diodes.lib" "")
    '("$IHP_TECH/tech/SG13G2_HBT/VBIC/spectre/SG13G2_cornerBIP_vbic.scs" "typ")
    '("$IHP_TECH/tech/SG13_ESD/spectre/SG13_esd.lib" "")
)
analysis('sp ?ports list("/PORT2" "/PORT3")  ?start "6G"  ?stop "500G"
        ?step "6G"  )
desVar(   "Cdc_block" 1m    )
desVar(   "Cin_matching" 0  )
desVar(   "Cout_matching" 0 )
desVar(   "Lac_block" 1m    )
desVar(   "Lin_matching" 0  )
desVar(   "Lout_matching" 0 )
desVar(   "fund" 180G   )
desVar(   "pin" -50 )
desVar(   "ibias" 2.331034m )
desVar(   "vdd" Vdd )
envOption(
    'enableNoiseRefactor  nil
    'analysisOrder  list("sp" "hb" "pss" "dc")
)
temp( 27 )
run()
Gmax\ dB10 = db10(gmax(sp(1 1 ?result "sp") sp(1 2 ?result "sp") sp(2 1 ?result "sp") sp(2 2 ?result "sp")))
plot( Gmax\ dB10 ?expr '( "Gmax dB10" ) )
================================================================================
*/
```

```
79
80  csh(strcat("rm /users/xtong/cadence_work62/OceanScripts/SimData_tries/IDC"))
81  csh(strcat("rm /users/xtong/cadence_work62/OceanScripts/SimData_tries/VDC"))
82
83  Xtong_Sparameter_Ropt(SimDataFolder Vdd freq ropt)
84
85
86  csh(strcat("rm /users/xtong/cadence_work62/OceanScripts/SimData_tries/CE_Kf"))
87  csh(strcat("rm /users/xtong/cadence_work62/OceanScripts/SimData_tries/CE_Delta_abs"))
88
89  Xtong_Sparameter_StaF1(SimDataFolder Vdd freq ropt)
90
91  csh(strcat("rm /users/xtong/cadence_work62/OceanScripts/SimData_tries/S12_dB"))
92  Xtong_Sparameter_S(SimDataFolder Vdd freq ropt)
93
94  ;csh(strcat("rm /users/xtong/cadence_work62/OceanScripts/SimData_tries/Y22_imag"))
95  ;csh(strcat("rm /users/xtong/cadence_work62/OceanScripts/SimData_tries/Y11_imag"))
96  ;csh(strcat("rm /users/xtong/cadence_work62/OceanScripts/SimData_tries/Y21_imag"))
97  ;csh(strcat("rm /users/xtong/cadence_work62/OceanScripts/SimData_tries/Y12_imag"))
98  ;csh(strcat("rm /users/xtong/cadence_work62/OceanScripts/SimData_tries/Y22_real"))
99  ;csh(strcat("rm /users/xtong/cadence_work62/OceanScripts/SimData_tries/Y11_real"))
100 ;csh(strcat("rm /users/xtong/cadence_work62/OceanScripts/SimData_tries/Y21_real"))
101 ;csh(strcat("rm /users/xtong/cadence_work62/OceanScripts/SimData_tries/Y12_real"))
102
103 Xtong_Sparameter_Y(SimDataFolder Vdd freq ropt)
104
105
106
107 csh(strcat("rm /users/xtong/cadence_work62/OceanScripts/SimData_tries/CE_Zoutput_real"))
108 csh(strcat("rm /users/xtong/cadence_work62/OceanScripts/SimData_tries/CE_Zoutput_imag"))
109
110 Xtong_Sparameter_ZOUT_IN(SimDataFolder Vdd freq ropt)
111
112
113
114
115
116 output_matching_c    = 7.0214f
117 output_matching_l = 86.831p
118
119
120 csh(strcat("rm /users/xtong/cadence_work62/OceanScripts/SimData_tries/CE_Zinput_real"))
121 csh(strcat("rm /users/xtong/cadence_work62/OceanScripts/SimData_tries/CE_Zinput_imag"))
122
123 ;Xtong_Sparameter_ZIN(SimDataFolder output_matching_c output_matching_l Vdd freq ropt)
124
125
126 input_matching_c    = 24.147f
127 input_matching_l = 48.466p
128
129
130
131
132
133 csh(strcat("rm /users/xtong/cadence_work62/OceanScripts/SimData_tries/CE_POUTvsPIN"))
134 csh(strcat("rm /users/xtong/cadence_work62/OceanScripts/SimData_tries/CE_Pdc_mag"))
135
136 Xtong_Sparameter_PoutindBm(SimDataFolder input_matching_c input_matching_l output_matching_c output_matching_l Vdd freq ropt)
137
138
139 csh(strcat("rm /users/xtong/cadence_work62/OceanScripts/SimData_tries/CE_Pdc_mag"))
140
141 ;Xtong_Sparameter_Pdc(SimDataFolder Vdd freq ropt)
142
143 output_matching_c    = 7.0214f
144 output_matching_l = 86.831p
145 input_matching_c    = 24.147f
146 input_matching_l = 48.466p
147
148 csh(strcat("rm /users/xtong/cadence_work62/OceanScripts/SimData_tries/S21_dB"))
149
150 Xtong_Sparameter_S21(SimDataFolder Vdd freq ropt input_matching_c input_matching_l output_matching_c output_matching_l)
151
152
```

Partial code for biasing setup

```
/*
Run Command:

load("/users/xtong/cadence_work62/OceanScripts/old_versions/biasing/sweepVb_power.ocn")

remove the dictionary

;csh(strcat("rm -r path/filename"))

csh(strcat("rm -r /users/xtong/cadence_work62/OceanScripts/SimData_Cascode"))
================================================================================

*/


/* Set Path  for the script */
OceanPath = "/users/xtong/cadence_work62/OceanScripts/"

/* Set Path  for the function */
functionPath = "/users/xtong/cadence_work62/OceanScripts/functions/"

SimDataFolder = strcat(OceanPath "SimData_biasing/" )

csh(strcat("mkdir -p " SimDataFolder))




csh(strcat("rm /users/xtong/cadence_work62/OceanScripts/SimData_biasing/CE_Pdc_mag"))
simulator( 'spectre )
design(  "/users/xtong/cadence_work62/sim/Volt_biasing_CE/spectre/schematic/netlist/netlist")
resultsDir( "/users/xtong/cadence_work62/sim/Volt_biasing_CE/spectre/schematic" )
path( "/data/cad/DesignKits/IHP/v0.6/SG13G2_617_rev0.9.0_a/lib/TL_SG13/RLCG/spectre/" )
modelFile(
    '("$IHP_TECH/tech/SG13_MOS/library/spectre/cornerMOSlv_psp.scs" "tt")
    '("$IHP_TECH/tech/SG13_MOS/library/spectre/cornerMOShv_psp.scs" "tt")
    '("$IHP_TECH/tech/SG13G2_PASSIVES/spectre/SG13_cornerRES.scs" "typ")
    '("$IHP_TECH/tech/SG13G2_PASSIVES/spectre/SG13_cornerCAP.scs" "typ")
    '("$IHP_TECH/tech/SG13G2_PASSIVES/spectre/SG13_dschottky_nbl1.lib" "")
    '("$IHP_TECH/tech/SG13G2_PASSIVES/spectre/SG13_diodes.lib" "")
    '("$IHP_TECH/tech/SG13G2_HBT/VBIC/spectre/SG13G2_cornerBIP_vbic.scs" "typ")
    '("$IHP_TECH/tech/SG13_ESD/spectre/SG13_esd.lib" "")
)
analysis('hb ?autoharms "yes"  ?autotstab "yes"  ?oversample list("5")
        ?fundfreqs list("(180G)")  ?maxharms list("5")  ?param "V_B"  ?start "828m"
        ?stop "1028m"  ?lin "18"  )
desVar(   "Cdc_block" 1m    )
desVar(   "Cin_matching" 14.524f    )
desVar(   "Cout_matching" 12.417f   )
desVar(   "Lac_block" 1m    )
desVar(   "Lin_matching" 44.669p    )
desVar(   "Lout_matching" 51.544p   )
desVar(   "V_B" 928m    )
desVar(   "fund" 180G   )
desVar(   "pin" -50 )
desVar(   "ibias" 2.331034m )
desVar(   "vdd" 1.5 )
envOption(
    'enableNoiseRefactor  nil
    'analysisOrder  list("sp" "hb" "pss" "dc")
)
temp( 27 )
run()
gain_dB = db10((pvi('hb "/net013" 0 "/PORT3/PLUS" 0 '(1)) / (- pvi('hb "/net09" 0 "/PORT2/PLUS" 0 '1))))
plot( gain_dB ?expr '( "gain_dB" ) )
pout_dBm = dbm(pvi('hb "/net013" 0 "/PORT3/PLUS" 0 '(1)))
plot( pout_dB ?expr '( "pout_dB" ) )




csh(strcat("rm /users/xtong/cadence_work62/OceanScripts/SimData_biasing_casc/CE_POUTvsPIN"))
csh(strcat("rm /users/xtong/cadence_work62/OceanScripts/SimData_biasing_casc/gain_dB"))

/* Construct the file name for the output impedance(real part) data */
filename = strcat("CE_POUTvsPIN")
/* Add the file name to the simulation data folder */
SimData_destination = strcat(SimDataFolder filename)
file_pointer = outfile(SimData_destination "a")
ocnPrint(?output file_pointer pout_dBm ?numberNotation 'scientific ?precision 16)
close(file_pointer)



/* unbound all the pointer*/
filename                = 'unbound
SimData_destination     = 'unbound
file_pointer                = 'unbound
```

```
89
90
91
92  /* Construct the file name for the output impedance(real part) data */
93  filename = strcat("gain_dB")
94  /* Add the file name to the simulation data folder */
95  SimData_destination = strcat(SimDataFolder filename)
96  file_pointer = outfile(SimData_destination "a")
97  ocnPrint(?output file_pointer gain_dB ?numberNotation 'scientific ?precision 16)
98  close(file_pointer)
99
100
101
102 /* unbound all the pointer*/
103 filename                = 'unbound
104 SimData_destination     = 'unbound
105 file_pointer                = 'unbound
106
107
108
109
110
111
112
113
114
115
116
117
118 simulator( 'spectre )
119 design(  "/users/xtong/cadence_work62/sim/Volt_biasing_CE/spectre/schematic/netlist/netlist")
120 resultsDir( "/users/xtong/cadence_work62/sim/Volt_biasing_CE/spectre/schematic" )
121 path( "/data/cad/DesignKits/IHP/v0.6/SG13G2_617_rev0.9.0_a/lib/TL_SG13/RLCG/spectre/" )
122 modelFile(
123     '("$IHP_TECH/tech/SG13_MOS/library/spectre/cornerMOSlv_psp.scs" "tt")
124     '("$IHP_TECH/tech/SG13_MOS/library/spectre/cornerMOShv_psp.scs" "tt")
125     '("$IHP_TECH/tech/SG13G2_PASSIVES/spectre/SG13_cornerRES.scs" "typ")
126     '("$IHP_TECH/tech/SG13G2_PASSIVES/spectre/SG13_cornerCAP.scs" "typ")
127     '("$IHP_TECH/tech/SG13G2_PASSIVES/spectre/SG13_dschottky_nbl1.lib" "")
128     '("$IHP_TECH/tech/SG13G2_PASSIVES/spectre/SG13_diodes.lib" "")
129     '("$IHP_TECH/tech/SG13G2_HBT/VBIC/spectre/SG13G2_cornerBIP_vbic.scs" "typ")
130     '("$IHP_TECH/tech/SG13_ESD/spectre/SG13_esd.lib" "")
131 )
132 analysis('dc ?param "V_B"  ?start "928m"  ?stop "1028m"
133         ?lin "20"  )
134 desVar(   "Cdc_block" 1m    )
135 desVar(   "Cin_matching" 14.524f    )
136 desVar(   "Cout_matching" 12.417f   )
137 desVar(   "Lac_block" 1m    )
138 desVar(   "Lin_matching" 44.669p    )
139 desVar(   "Lout_matching" 51.544p   )
140 desVar(   "V_B" 928m    )
141 desVar(   "fund" 180G   )
142 desVar(   "pin" -50 )
143 desVar(   "ibias" 2.331034m )
144 desVar(   "vdd" 1.5 )
145 envOption(
146     'enableNoiseRefactor  nil
147     'analysisOrder  list("sp" "hb" "pss" "dc")
148 )
149 temp( 27 )
150 run()
151 PDC = (i("/L14/PLUS" ?result "dc") * v("/vdd" ?result "dc"))
152 plot( Pdc ?expr '( "Pdc" ) )
153
154
155 /* Construct the file name for the Pout_mag vs Pin data */
156 filename = strcat("CE_Pdc_mag")
157 /* Add the file name to the simulation data folder */
158 SimData_destination = strcat(SimDataFolder filename)
159 file_pointer = outfile(SimData_destination "a")
160 ocnPrint(?output file_pointer PDC ?numberNotation 'scientific ?precision 16)
161 close(file_pointer)
162
163 /* unbound all the pointer*/
164 filename                = 'unbound
165 SimData_destination     = 'unbound
166 file_pointer                = 'unbound
167
168
```

Appendix B – MATLAB code for data handling

Partial code for matching network automation

```
%************************************************************************%
% lumped component impedance matching                                    %
%************************************************************************%

clear all;


% Define the working frequency
f = 170e9;

%% output matching network(LC Highpass)
% output_matching_c: Capacitpr of the LC Highpass matching network
% output_matching_l: Inductor of the LC Highpass matching network

% Define lumped component
RS = importdata('CE_Zoutput_real');       % import the real part of the output impedance from the file
rs = RS.data(2);                          % real part of the output impedance
Zout_real = rs;                           % save the real part of the output impedance
XS = importdata('CE_Zoutput_imag');       % import the imag part of the output impedance from the file
xs = XS.data(2);                          % imag part of the output impedance
Zout_imag = xs;                           % save the imag part of the output impedance
rl = 50;                                  % 500hm load
xl = 0;

w  = 2*pi*f;
ql = -xl/rl;
qs = xs/rs;
cl = -1/w/xl;
ll = (1+qs*qs)*xs/w/qs/qs;
rp = (1+qs*qs)*rs;
rs = rl;
% Calculation of the value of the iumped components of the LC Highpass output matching network
                Q = sqrt(rp/rs-1);
                lp = rp/w/Q;
                cs = 1/Q/w/rs;
                if (xl==0)
                    output_matching_c = cs;
                 else
                    if (cl==cs)
                        output_matching_c = Inf;
                    else
                        output_matching_c = cl*cs/(cl-cs);
                    end
                end
                if (xs==0)
                    output_matching_l = lp;
                 else
                    if (ll==lp)
                        output_matching_l = Inf;
                    else
                        output_matching_l = lp*ll/(ll-lp);
                    end
                end

% %% input matching network(CL highpass)
% % input_matching_c: Capacitpr of the CL Highpass matching network
```

```
% % input_matching_1: Inductor of the CL Highpass matching network
%
% % Define lumped component
% clear all
%
% f = 180e9;
%
% RS = importdata('CE_Zinput_real');       % import the real part of the input impedance from the file
% rs = RS.data(2);                          % real part of the input impedance
% Zin_real = rs;                           % save the real part of the input impedance
% XS = importdata('CE_Zinput_imag');       % import the imag part of the input impedance from the file
% xs = XS.data(2);                          % imag part of the input impedance
% Zin_imag = xs;                           % save the imag part of the input impedance
% r1 = 50;                                  % 500hm source
% x1 = 0;
%
% w  = 2*pi*f;
% q1 = -x1/r1;
% qs = xs/rs;
% c1 = -1/w/x1;
% l1 = (1+qs*qs)*xs/w/qs/qs;
% rp = (1+qs*qs)*rs;
% rs = r1;
% % Calculation of the value of the iumped components of the LC Highpass output matching network
%               Q = sqrt(rp/rs-1);
%               lp = rp/w/Q;
%               cs = 1/Q/w/rs;
%               if (x1==0)
%                   input_matching_c = cs;
%                else
%                   if (c1==cs)
%                         input_matching_c = Inf;
%                     else
%                         input_matching_c = c1*cs/(c1-cs);
%                     end
%                 end
%               if (xs==0)
%                   input_matching_1 = lp;
%                else
%                   if (l1==lp)
%                         input_matching_1 = Inf;
%                     else
%                         input_matching_1 = lp*l1/(l1-lp);
%                     end
%                end

%% input matching network(LC highpass) (WHEN IMAG_ZIN>0)
% input_matching_c: Capacitpr of the CL Highpass matching network
% input_matching_1: Inductor of the CL Highpass matching network

% Define lumped component

f = 180e9;

RS = importdata('CE_Zinput_real');       % import the real part of the input impedance from the file
rs = RS.data(2);                          % real part of the input impedance
```

```
    Zin_real = rs;                          % save the real part of the input impedance
    XS = importdata('CE_Zinput_imag');      % import the imag part of the input impedance from the file
    xs = XS.data(2);                         % imag part of the input impedance
    Zin_imag = xs;                          % save the imag part of the input impedance
    rl = 50;                                 % 50Ohm source
    xl = 0;

    w  = 2*pi*f;
    ql = -xl/rl;
    qs = xs/rs;
    cl = -1/w/xl;
    ll = (1+qs*qs)*xs/w/qs/qs;
    rp = (1+qs*qs)*rs;
    rs = rl;
    % Calculation of the value of the iumped components of the LC Highpass output matching network
                    Q = sqrt(rp/rs-1);
                    lp = rp/w/Q;
                    cs = 1/Q/w/rs;
                    if (xl==0)
                        input_matching_c = cs;
                     else
                        if (cl==cs)
                            input_matching_c = Inf;
                        else
                            input_matching_c = cl*cs/(cl-cs);
                        end
                    end
                    if (xs==0)
                        input_matching_l = lp;
                     else
                        if (ll==lp)
                            input_matching_l = Inf;
                        else
                            input_matching_l = lp*ll/(ll-lp);
                        end
                    end
```

Partial code for biasing setup

```
clear all
close all

% Define the working frequency
f = 170e9;

%% sweeping fmax with Vbe(biasing voltage) and Vce(Vdd supply voltage)

% extract data
Fmax_SWEEP = importdata('CE_fmax_sweep_3');
VDD = Fmax_SWEEP.data(1,:);                          % sweeping of VDD
V_BIASING = Fmax_SWEEP.textdata(3:14,:);              % sweeping of VDD
V_BIASING = cell2mat(V_BIASING);
V_BIASING = str2num(V_BIASING);
Fmax = Fmax_SWEEP.data(2:13 , 1:8);
Fmax = Fmax/(10^9);

% plot fmax vs VB/Vdd
Y = Fmax';
[X,Z] = meshgrid(V_BIASING,VDD);
figure(1)
contour(X,Y,Z);
title('fmax versus Vbe and Vcc')
xlabel('Vbe (V)')
ylabel('fmax (GHz)')
grid on;

%% 3D plot
figure(4)
surf(X,Z,Y)
xlabel('Vbe (V)')
ylabel('Vcc (V)')
zlabel('fmax (GHz)')
grid on;
```

Partial code for PA performance display

```
%************************************************************************%
%  Stability factor                                                      %
%************************************************************************%

% Define the working frequency
f = 170e9;

%% Plot of stability factor

STAB = importdata('CE_Kf');             % extract the stability factor data
freq = (STAB.data(: , 1)/1e9)';
stab = STAB.data(: , 2)';
p = find(freq==170);

% Plot the stability factor K
plot(freq, stab, 'b', 'LineWidth', 2)
% Add title and axis labels
title('Stability Factor')
xlabel('Frequency (GHz)')
ylabel('Stability Factor K')
% Turn on the grid
grid on
% add point on the 180GHz
text(freq(p),stab(p),['(',num2str(freq(p)),',',num2str(stab(p)),')'],'color','b')



%% Plot of the absolute value of Delta

DELTA = importdata('CE_Delta_abs');             % extract the stability factor data
freq2 = (DELTA.data(: , 1)/1e9)';
delta = DELTA.data(: , 2)';
p = find(freq2==180);


figure(2)
% Plot the stability factor K
plot(freq2, delta, 'b', 'LineWidth', 2)
% Add title and axis labels
title('|\Delta|')
xlabel('Frequency (GHz)')
ylabel('|\Delta|')
% Turn on the grid
grid on
% add point on the 180GHz
text(freq2(p),delta(p),['(',num2str(freq2(p)),',',num2str(delta(p)),')'],'color','b')
```

Appendix C – Skill code for layout generation

Partial code for transformer generation

```
procedure(ESM_genHalfSymSingleIndCoil(t_libName, t_cellName)

    let( ()

        /* Set Variables */
        cornerSize  = 10.0
        cornerExt       =  3.0
        lineWidth       =  7.0

        x_radius        =  30.0
        y_radius        =  40.0

        term_spacing    =  8.0
        term_width      =  4.0
        term_exten_p    = 10.0
        term_exten_s    = 15.0

        layer_primary           =  "TopMetal2"
        layer_secondary     =  "TopMetal1"

        ;coil_offset = 10.0 Variable not implemented tooffset the two coil and tune the coupling factor


        /* Create and and open new cellview  */
        ESM_openCellView( t_libName, t_cellName)
        cvId = geGetWindowCellView()


        ESM_genSymSingleIndCoil("primary",          ; primary or secondary coil
                                "left",                 ; left or right side of the symetric coil
                                 x_radius,              ; radiuos of uter edge of coil in x-direction
                                 y_radius,              ; radiuos of uter edge of coil in y-direction
                                 cornerSize,        ; size in x - and y-direction of the corner
                                 cornerExt,             ; dimension additional line section after 45-degree corner
                                 lineWidth,             ; line width of the coil
                                 term_spacing,          ; spacing between terminals
                                 term_width,        ; with of the terminals
                                 term_exten_p,          ; terminal extension distance primary coil
                                 term_exten_s,          ; terminal extension distance secondary coil
                                 layer_primary,     ; Layer of the primary coil
                                 layer_secondary    ; layer of the secondary coil

                                ) ; genSymSingleIndCoil


        ESM_genSymSingleIndCoil("primary",          ; primary or secondary coil
                                "right",                ; left or right side of the symetric coil
                                 x_radius,              ; radiuos of uter edge of coil in x-direction
                                 y_radius,              ; radiuos of uter edge of coil in y-direction
                                 cornerSize,        ; size in x - and y-direction of the corner
                                 cornerExt,             ; dimension additional line section after 45-degree corner
                                 lineWidth,             ; line width of the coil
                                 term_spacing,          ; spacing between terminals
                                 term_width,        ; with of the terminals
                                 term_exten_p,          ; terminal extension distance primary coil
                                 term_exten_s,          ; terminal extension distance secondary coil
                                 layer_primary,     ; Layer of the primary coil
                                 layer_secondary    ; layer of the secondary coil

                                ) ; genSymSingleIndCoil


        ESM_genSymSingleIndCoil("secondary",            ; primary or secondary coil
                                "left",                 ; left or right side of the symetric coil
                                 x_radius,              ; radiuos of uter edge of coil in x-direction
                                 y_radius,              ; radiuos of uter edge of coil in y-direction
                                 cornerSize,        ; size in x - and y-direction of the corner
                                 cornerExt,             ; dimension additional line section after 45-degree corner
                                 lineWidth,             ; line width of the coil
                                 term_spacing,          ; spacing between terminals
                                 term_width,        ; with of the terminals
                                 term_exten_p,          ; terminal extension distance primary coil
                                 term_exten_s,          ; terminal extension distance secondary coil
                                 layer_primary,     ; Layer of the primary coil
                                 layer_secondary    ; layer of the secondary coil

                                ) ; genSymSingleIndCoil

        ESM_genSymSingleIndCoil("secondary",            ; primary or secondary coil
                                "right",                ; left or right side of the symetric coil
                                 x_radius,              ; radiuos of uter edge of coil in x-direction
                                 y_radius,              ; radiuos of uter edge of coil in y-direction
                                 cornerSize,        ; size in x - and y-direction of the corner
                                 cornerExt,             ; dimension additional line section after 45-degree corner
                                 lineWidth,             ; line width of the coil
                                 term_spacing,          ; spacing between terminals
                                 term_width,        ; with of the terminals
                                 term_exten_p,          ; terminal extension distance primary coil
                                 term_exten_s,          ; terminal extension distance secondary coil
                                 layer_primary,     ; Layer of the primary coil
                                 layer_secondary    ; layer of the secondary coil

                                ) ; genSymSingleIndCoil

        /* Merge the polygons */
        leMergeShapes(cvId~>shapes)

```

Function list used in transformer generation

```
C:\Users\xixit\OneDrive\Desktop\graduation\SkillCode_SG13G2\Skill_procedure_lib\Functions_basicgeo
/*

*/

procedure(ESM_initFuncTransformer(functionPath)

    load( strcat(functionPath "ESM_genTransformerStraightSection.il"))
    load( strcat(functionPath "ESM_gen45LineCorner.il"))

    load( strcat(functionPath "ESM_genHalfSymSingleIndCoil.il"))
    load( strcat(functionPath "ESM_genSymSingleIndCoil.il"))

    load( strcat(functionPath "ESM_genTransformerDualSingleCoil.il"))

    load( strcat(functionPath "ESM_genTransformerDualSingleCoil.il"))

)

```

Partial code for GSG-pad generation

```
procedure(ESM_genGSGConfig()

    let( ()

    println("Generate a GSG-pad configuration ")

        /* Select Probe Pad Layers */
        probePadLayers = list("TopMetal2" "dfpad" "Passiv")


        /* Build up the signal pad */
        /*=========================*/
        let( (signalPadLength signalPadWidth signalPadPoly)

            signalPadLength = 30.0;
            signalPadWidth  = 50.0;

            signalPadPoly = list(       /* 1. */ -signalPadLength/2 :  signalPadWidth/2
                                  /* 2. */               0.0 :  signalPadWidth/2
                                  /* 3. */               0.0 : -signalPadWidth/2
                                  /* 4. */ -signalPadLength/2 : -signalPadWidth/2

                                ) /* list */

            foreach( layer probePadLayers

                println(layer)

                if( layer == "Passiv" then

                    signalPadPoly = list(       /* 1. */ -signalPadLength/2+2.1 :  signalPadWidth/2-2.1
                                          /* 2. */                   0.0 :  signalPadWidth/2-2.1
                                          /* 3. */                   0.0 : -signalPadWidth/2+2.1
                                          /* 4. */ -signalPadLength/2+2.1 : -signalPadWidth/2+2.1

                                        ) /* list */


                    layerPoly   = dbCreatePolygon(cvId list( layer  "drawing" ) signalPadPoly)

                    dbMoveShape(layerPoly cvId list(0:0 "R0" SCALEFACTOR_ROUNDED))

                else


                    layerPoly   = dbCreatePolygon(cvId list( layer  "drawing" ) signalPadPoly)

                    dbMoveShape(layerPoly cvId list(0:0 "R0" SCALEFACTOR_ROUNDED))

                ) /* if else */

            ) /* foreach */

        ) /* let signal pad variables */

        /* Build Ground Pads  */
        /*====================*/
        let( (probe_pitch_minimum probe_pitch_maximum probepin_offset length width Xcoord_offset Ycoord_offset)
```

```
60
61
62              probe_pitch_min =  50.0 /* WR- 2.2  325-525 GHz */
63              probe_pitch_max = 125.0 /* WR-10.0   75-110 GHz */
64
65              probepin_offset_inner = 20.0
66              probepin_offset_outer = 20.0
67
68              width  = 60.0
69
70              foreach( layer probePadLayers
71
72                  if( layer == "Passiv"
73
74                      then
75
76                          lowerleftCorner = (-probe_pitch_min + probepin_offset_inner - 2.1): -width/2 + 2.1
77                          upperightCorner = (-probe_pitch_max - probepin_offset_outer + 2.1):  width/2 - 2.1
78
79                          dbCreateRect(cvId list(layer "drawing") list(lowerleftCorner upperightCorner))
80                                  .
81                      else
82
83                          lowerleftCorner = (-probe_pitch_min + probepin_offset_inner): -width/2
84                          upperightCorner = (-probe_pitch_max - probepin_offset_outer):  width/2
85
86                          dbCreateRect(cvId list(layer "drawing") list(lowerleftCorner upperightCorner))
87
88                  ) /* if else */
89
90              ) /* for each */
91
92          ) /* let - ground pad parameters*/
93
94      ) /*let*/
95
96  )/*procedure*/
97
98
```