Electrothermal Filters for No-Trim Temperature Sensors

[Daguang Liu]

Thesis submitted in partial fulfillment of

the requirements for the requirements for the degree of

MASTER OF SCIENCE

IN

ELECTRICAL ENGINEERING

Author: BSc.D.Liu

Student ID: 4739760

Supervisor: Prof. Kofi A.A. Makinwa

Ir. Sining Pan

[2019 Oct 12th]

Abstract

This thesis describes the design and characterization of thermistor-based electrothermal filters (ETFs) intended for use in high-accuracy CMOS temperature sensors. ETFs have been previously realized by placing an on-chip heater in close proximity to an on-chip thermopile, which then picks up the thermally-delayed signals generated by the heater. This delay is a well-defined function of absolute temperature and can be used as the basis for highly accurate temperature sensors. In this work, the thermopiles are replaced by a thermistor, resulting in greater sensitivity and higher resolution. Measurements show that the new ETFs can achieve 3.6m℃ resolution in a conversion time of 1s and 0.2℃(3σ) untrimmed inaccuracy from 30℃ to 60℃.

Contents

1 – Introduction

1 1 – Motivation and objective

Temperature is an important environmental quantity. It plays a significant role in most physical, chemical and biomedical processes [1]. This makes temperature measurement critical for the monitoring and control of such processes. Thanks to the development of integrated circuit technology, extremely small temperature sensors can be realized based on BJTs [2] [3], MOSFETs [4], resistors [5] [6] and electro-thermal filters [7] [8].

Accuracy is one of the most important specifications of a temperature sensor. Since the inherent accuracy of integrated temperature sensors is limited by process spread, their accuracy is typically improved by trimming on the basis of information acquired by calibration [9] [10]. Traditionally, this requires a temperature-controlled environment, an external reference sensor and a certain amount of time, during which the device-under-test (DUT) reaches thermal equilibrium with the reference sensor. However, this is time-consuming and thus costly. Recently, voltage-based calibration [12] and heater-assisted calibration [11] have been proposed to address this problem. However, these techniques have been developed specifically for BJT-based temperature sensors.

Temperature calibration could be improved if the reference sensor could be realized on the same piece of silicon. Since silicon is a good conductor, the thermal equilibrium between the DUT and the reference sensor can be reached in a very short time (<<1s), enabling a significant reduction in calibration speed and cost. The design of such a reference sensor is the goal of this thesis.

Fig.1.1 shows an application of this idea for the thermal monitoring of a large silicon chip. In modern system-on-chips (SoCs), a large number of small but fast temperature sensors are needed to monitor hot-spots whose intensity and location rapidly changes. Given a highly accurate reference sensor, all the other sensors can be rapidly trimmed without the need for a temperature-controlled environment.

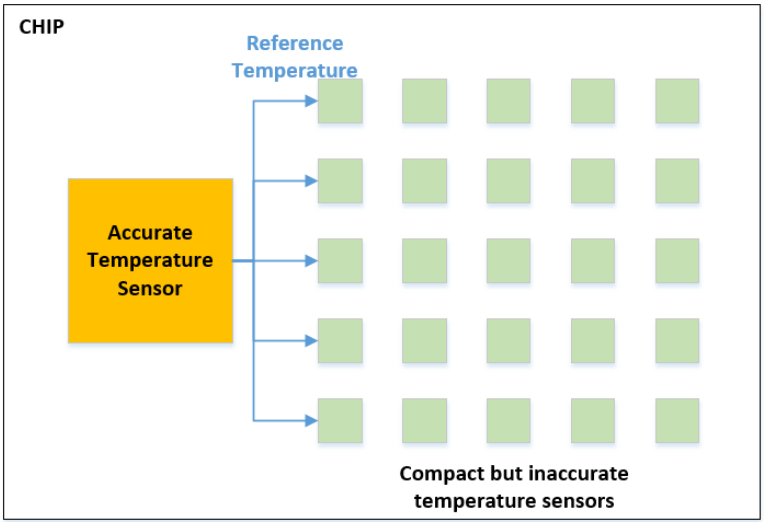


Figure 1.1 Temperature sensor as an on-chip calibration reference

It should be noted that although the reference sensor should be more accurate than the DUT (error < 0.05℃), it does not need to cover a wide temperature range. This is because trimming is usually done in a fairly stable environment (less than 10℃ variation) To leave some margin, a temperature range of 30℃ is set as one of the targets. Also, the reference sensor's conversion time needs to be short (<1s) to avoid increasing the time-related cost.

The target specifications of a reference sensor are summarized in Table 1.1.

Table 1 Specifications of a reference sensor

Specification	Target
Temperature accuracy	<0.05℃
Conversion time	<1s
Temperature range	30℃ to 60℃

1 2 – Literature review

1.2.1 – BJT based temperature sensor

In CMOS technology, both PNPs and NPNs can be used to sense temperature. Vertical PNPs are usually preferred due to their lower sensitivity to packaging stress. NPNs typically have more current gain, but typically require extra process options (twin wells or deep n-wells). Regardless of what type of BJT is used, their use as temperature sensors relies on the temperature-dependency of a BJT's base-to-emitter voltage V_{BE}, which can be expressed as:

$$V_{BE} = \frac{kT}{q} \ln(\frac{I_C}{I_S}) \quad (1.1)$$

In this equation, I_C is the collector current, I_S is the saturation current, k is the Boltzmann constant, q is the electron charge, and T is the temperature. Because of the temperature dependence of I_S, V_{BE} decreases over temperature with a 2 mV/K slope, which is complementary to absolute temperature (CTAT) [12].

For a pair of BJTs biased at different current densities, the difference of their base-emitter voltages exhibits another characteristic, which is given by:

$$\Delta V_{BE} = \frac{kT}{q} \ln(p) \quad (1.2)$$

where p is the ratio between their current densities This equation shows that ΔV_{BE} is proportional to absolute temperature (PTAT), which is inherently independent of process and supply voltage.

The CTAT V_{BE} and PTAT ΔV_{BE} can be linearly combined to get the well-known temperature-independent band-gap voltage V_{REF}, given by[13]:

$$V_{REF} = \alpha \Delta V_{BE} + V_{BE} \quad (1.3)$$

Where ΔV_{BE} is scaled by a factor of α. This principle is shown in Figure 1.2.

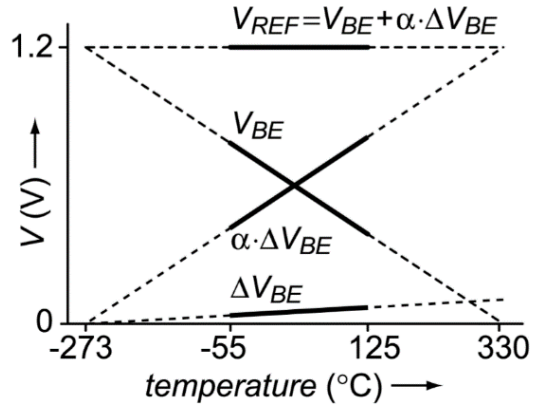


Figure 1.2 Bandgap voltage of BJT based temperature sensor [10]

The reference voltage can then be used to digitize the PTAT ΔV_{BE} and to sense temperature since the ratio of them is a function of absolute temperature:

$$\mu = \frac{V_{PTAT}}{V_{REF}} = \frac{\alpha \Delta V_{BE}}{\alpha \Delta V_{BE} + V_{BE}} \tag{1.4}$$

Figure 1.3 shows how the combination is realized in real circuits.

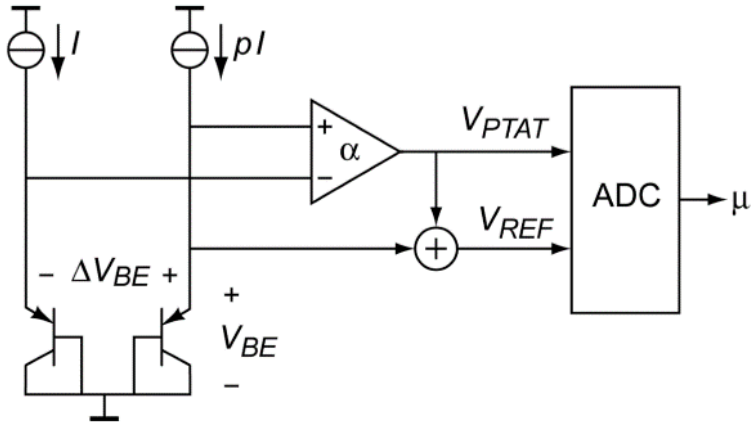


Figure 1.3 Block diagram of a BJT-based temperature sensor [10]

After a single-point trim, BJT-based sensors can achieve 0.1°C inaccuracy over the military temperature range (-55°C to 125°C) [3]. However, due to process spread, the saturation current changes from batch to batch, resulting in an untrimmed inaccuracy of a few °C [14]. Also, the fact that V_{BE} is approximately 0.7V sets a lower limit on the supply voltage, restricting the use of such sensors in advanced technologies in which supply voltages are typically less than 1V.

1.2.2 – MOSFET based temperature sensor

There are also various types of MOSFET-based temperature sensors, since many MOS device parameters (Trans-conductance, threshold voltage, etc.) are heavily temperature-dependent.

For a MOSFET, there is an exponential relationship between the drain current I_{DS} in the weak inversion region and the overdrive voltage V_{GS} - V_{TH} given by:

$$V_{GS} - V_{TH} = \left(\frac{\eta kT}{q}\right) \ln\left(\frac{I_{DS}}{I_0}\right) \tag{1.5}$$

where η is the sub-threshold slope factor and I_0 is a process-dependent parameter. Dynamic-Threshold based temperature sensor, in which the BJTs in a bipolar core are replaced with DTMOST(Dynamic-Threshold MOSFET) [15]. Basically, it is a MOSFET

whose body, drain and gate terminals are tied together, a diode-connected DTMOST exhibits a near-ideal exponential replationship between I_D and V_{GS} [28]. As the V_{TH} of DTMOST sensors is well-defined, they can be used in the same way as BJTs to achieve decent accuracy.

Compared to BJT sensors, however, DTMOST sensors have one more variable that can spread over process: the sub-threshold slope factor η. With a single-point trim, the state-of-the-art accuracy is 0.4 ℃(3σ) over the military temperature range [4].

There are also other types of MOSFET-based temperature sensors. E.g., [3] is built by comparing the difference in the propagation delay of differently types of inverters. This type of sensor can be quite compact (< 0.01mm^2) and is compatible with a sub-1V supply. However, since the delay is a complicated function of the transconductance and threshold voltage of many transistors, many error sources contribute to the final spread, making these kinds of sensors rather inaccurate, even after 2-point trimming.

1.2.3 – Resistor based temperature sensor

On-chip resistors can have stable temperature coefficients as large as 0.3%/°C, which provides another temperature sensing mechanism. The basic idea is to compare the resistance change of a temperature-dependent resistor with a fixed reference resistor that is temperature insensitive.

The front end of a resistor-based sensor could either be a Wheatstone bridge [6] or a Wien-bridge filter [16]. For a Wheatstone bridge, the reference is another on-chip resistor. For a Wien bridge, the resistors are combined with capacitors, to create a temperature-dependent time constant (phase shift). Temperature information can then be extracted by measuring the phase shift output of the Wien bridge.

The biggest advantage of these types of sensors is that they can be designed for low noise and extremely high resolution (sub-mK) [6]. In addition, resistor-based temperature sensors do not have a fundamental limit on voltage headroom.

Unfortunately, the untrimmed inaccuracy of resistor based sensors is quite poor, since variations in geometry and doping concentration cause large resistance spread. This spread can be ±20%, which corresponds to temperature errors of tens of °C.

1.2.4 – Thermal diffusivity based temperature sensor

In addition to the three aforementioned types of temperature sensors, thermal diffusivity based sensors are another option [7]. The thermal diffusivity of silicon, D_{si} describes the time it takes for heat signals to diffuse through a volume of silicon. Its temperature sensitivity comes from the temperature-dependent phonon scattering of crystalline semiconductors. Since silicon is a highly homogeneous and pure material, the temperature sensitivity of D_{si} is a well-defined function of absolute temperature, and can be approximated by [17]:

$$D_{si} \propto T^{-1.8} \tag{1.6}$$

As shown in Fig.1.4, heat signals diffuse from a heater to the surrounding silicon substrate, and a sensor is placed at a distance 'S' to pick up the delayed heat signal. Since thermal diffusivity defines the speed of the diffusion process, the thermal delay between heater and sensor will also be temperature-dependent. Such a structure is known as an Electro-thermal Filter, or ETF [18].

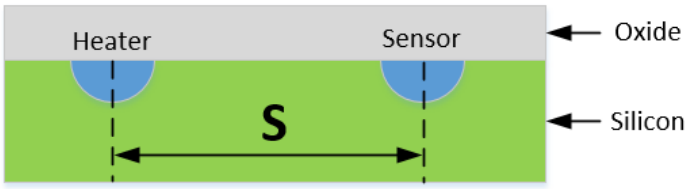


Figure.1.4 A basic electro-thermal filter (ETF)

As the distance 'S' is defined by lithography, it is also a well-defined variable: so in principle, the sensor can be quite accurate even without trimming.

Table 1.2 provides an overview of the best accuracy (untrimmed or 1 point trimmed) achieved by different types of temperature sensors so far. Compared to the other types, thermal diffusivity based temperature sensors achieve the best untrimmed inaccuracy of 0.2 ℃(3σ) [8], making them the most promising candidate for the targeted application.

Table 1.2-Overview of the most accurate temperature sensors

State of the art	Accuracy ℃(3σ)	Temperature Range	Reference
BJT-based	0.3 (untrimmed)	-55℃ to 125℃	[3]
MOSFET-based	0.4 (1 point trim)	-55℃to 125℃	[19]
Resistor-based	0.3 (1 point trim)	-40℃ to 85℃	[20]
Thermal diffusivity-	0.2 (untrimmed)	-55℃ to 125℃	[8]
Targeted specification	0.05 (untrimmed)	30℃ to 60℃	

1 3 – Organization of the thesis

The rest of this thesis is organized as follows. First, the principles, prior art and major accuracy limitations of TD sensors are analyzed in Chapter 2. In Chapter 3, a new type of ETF is proposed, and its advantages and disadvantages compared with traditional ETFs is discussed. In order to characterize the performance of this new type of ETF, two batches of test chips have been taped out. They are presented in Chapter 4 and Chapter 5, including the chip details, measurement setups and characterization results. The thesis concludes in Chapter 6. Possible future work is presented in the same chapter.

2 – TD Temperature Sensor

This chapter discusses how the thermal diffusivity of silicon D_{si} can be measured by using an electro-thermal filter (ETF). First, the thermal properties of Si and SiO_2 are discussed. Second, an electro-thermal model is developed and used to estimate ETF performance. Then the performance of previous TD sensors based on ETFs realized in CMOS technology is presented. Last but not least, the accuracy and resolution of traditional ETFs are discussed and compared to the targeted specification, which suggests the need for a new type of ETF.

2.1 – Principles of TD sensor

Thermal diffusivity D defines the speed at which heat diffuses through a material. It is the ratio of k and C_v, given by [21]:

$$D = \frac{k}{C_v} = \frac{1}{3} v_s \lambda_{ph} \tag{2.1}$$

in which *k* is the thermal conductivity in W/m/K, C_v is the volumetric heat capacity in J/cm^3/K, v_s is the mean photon velocity and λ_{ph} is the mean free path. As shown in Fig. 2.1, D_{si} and D_{SiO_2} can be obtained from the previous equation and from literature [17]. Note that D_{SiO_2} is multiplied by a factor of 100 to fit on the same scale as D_{si} .

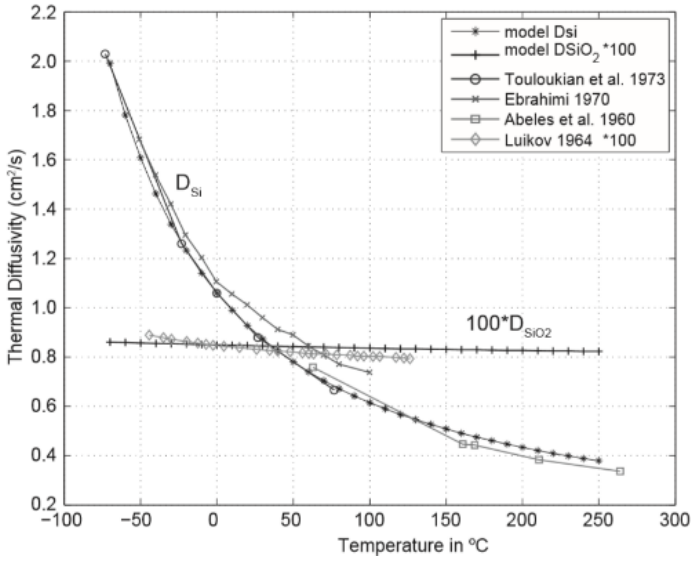


Figure.2.1 Historical data and simulated values of D_{si} and D_{SiO_2} [21]

Two observations can be made from the equation and plot above:

1. D_{si} is strongly temperature-dependent, while D_{SiO_2} is much less sensitive to temperature variations. For D_{si}, a $1/T^{1.8}$ power-law proportionality holds well over a wide temperature range (-55℃ to 125℃) [14].

2. As v_s is fairly constant and λ_{ph} is only weakly sensitive to doping variations, D_{si} is only technology-dependent and the thermal constants are very well-defined.

Since D_{si} is a thermal characteristic rather than an electrical one, a thermal detection system, in this case, an Electro-thermal filter (ETF) [14] is needed to sense it. An ETF consists of a heater, a thermal medium (silicon in this case) and a relative temperature sensor.

Fig 2.2 shows the cross-section of a conceptual ETF which consists of a point heater and a point temperature sensor on the surface of silicon bulk. In general, the value of their spacing 'S' is much smaller than the thickness of the silicon substrate (~300μm). Furthermore, the SiO_2 layer can be considered to be a thermal insulator due to its much lower thermal diffusivity.

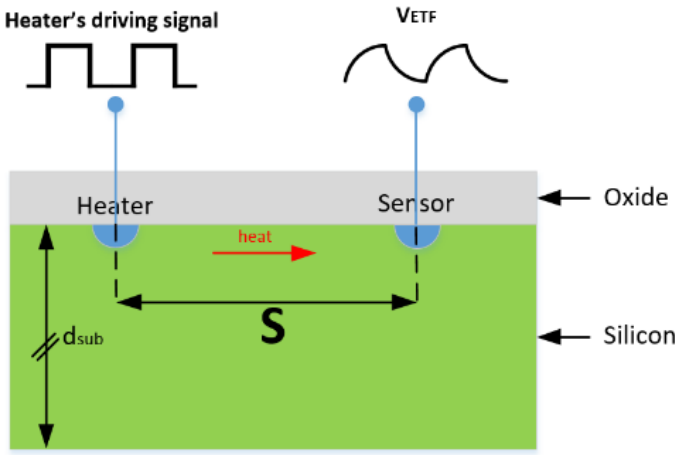


Figure 2.2 The cross-section of a basic ETF that measures D_{si}

When the heater is driven by a harmonic signal at a fixed frequency, heat diffuses into silicon in a semi-spherical manner. The associated temperature profile is given by solving [22]:

$$\frac{d^2(rT(r))}{dr^2} - q^2 rT(r) = 0 \tag{2.2}$$

in which r s the distance to the point heater, $T(r)$ is the temperature profile along the diffusion path, and $q^2 = j\omega / D$. The solution of Eq.(2.2) defines the thermal impedance[22], which is related to the temperature profile $T(\omega, r)$ and heater's power $P_{heater}(\omega)$:

$$Z_{th}(\omega, r) = \frac{T(\omega, r)}{P_{heater}(\omega)} = \frac{1}{2\pi k_{si} r} \exp(-r\sqrt{\frac{\omega}{2D_{si}}}) \exp(-jr\sqrt{\frac{\omega}{2D_{si}}}) \tag{2.3}$$

The magnitude and phase components can be computed as follows:

$$\left|Z_{th}(\omega, r)\right| = \frac{1}{2\pi k_{si} r} \exp(-r\sqrt{\frac{\omega}{2D_{si}}}) \tag{2.4}$$

$$\phi(\omega, r) = -r\sqrt{\frac{\omega}{2D_{si}}} \tag{2.5}$$

These equations indicate that the thermal impedance $\left|Z_{th}(\omega, r)\right|$ is a function of k_{si} and D_{si} . As the drive frequency goes up, the magnitude of the phase shift will increase, just as in an electrical low-pass filter. Assuming this ETF has a sensitivity S_t , then the amplitude of ETF's output is given by:

$$V_{ETF}(\omega, r) = \frac{P_{heater} S_t}{2\pi k_{si} r} \exp(-r\sqrt{\frac{\omega}{2D_{si}}}) \tag{2.6}$$

And the phase output can be rewritten as:

$$\phi_{ETF} = -s\sqrt{\pi f_{drive} / D_{si}} \propto -s\sqrt{\pi f_{drive} T^{1.8}} \tag{2.7}$$

This shows that the ETF phase ϕ_{ETF} has a near-linear $T^{0.9}$ dependency, which is only dependent on heater distance 'S', driving frequency f_{drive} and D_{si}. Fig. 2.3 shows the simulated $|\phi_{ETF}|$ for S=24μm and f_{drive}=42kHZ.

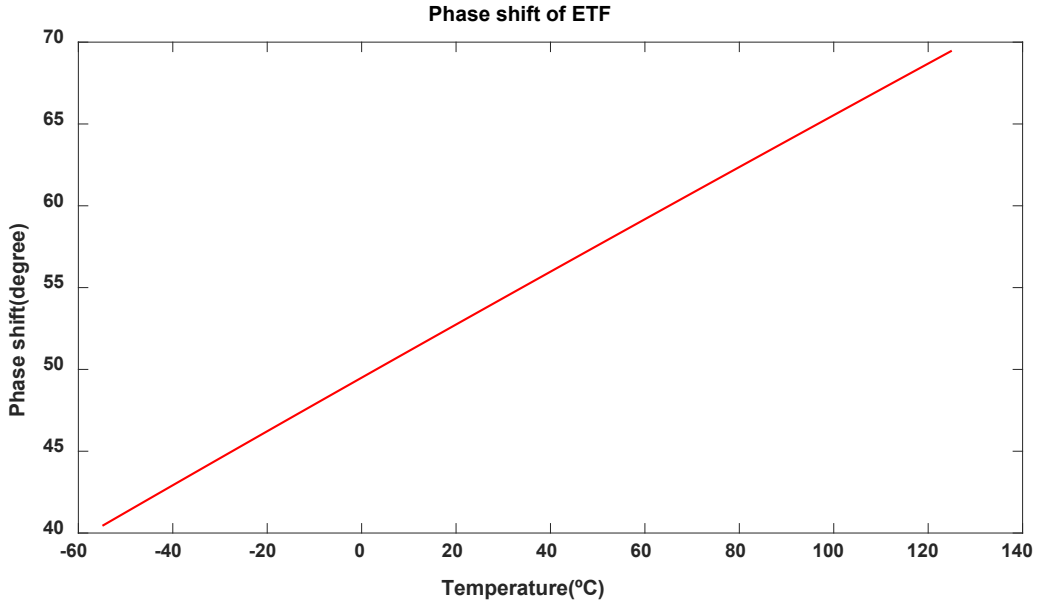


Figure.2.3 Simulated ϕ_{ETF} as a function of temperature

Compared to the ETF phase ϕ_{ETF}, V_{ETF} has more degrees of freedom. For instance, the heater power P_{heater}, will depend both on its resistance and on the supply voltage, which can easily vary by over 10%. On the contrary, ϕ_{ETF} is a well-defined function over temperature, and can serve as an accurate temperature reference.

2.2 – ETF Design in CMOS

As shown in the Fig.2.2, there are 2 necessary elements for an ETF: a heater and a temperature sensor. In prior art, the heaters were simply realized as small on-chip resistors, while the temperature sensors were realized as thermopiles [23] [8].

A typical thermopile is shown in Fig.2.4; it consists of series-connected p+ diffusion resistors and aluminum strips. Due to the Seebeck effect, a voltage that is proportional to the temperature difference between the hot/cold junctions (~0.5mV/K) is created. Being passive sensors, thermopiles are intrinsically offset-free. However, thermopile ETFs suffer from significant thermal noise, due to the finite resistance (140 Ω/square) of diffusion resistors.

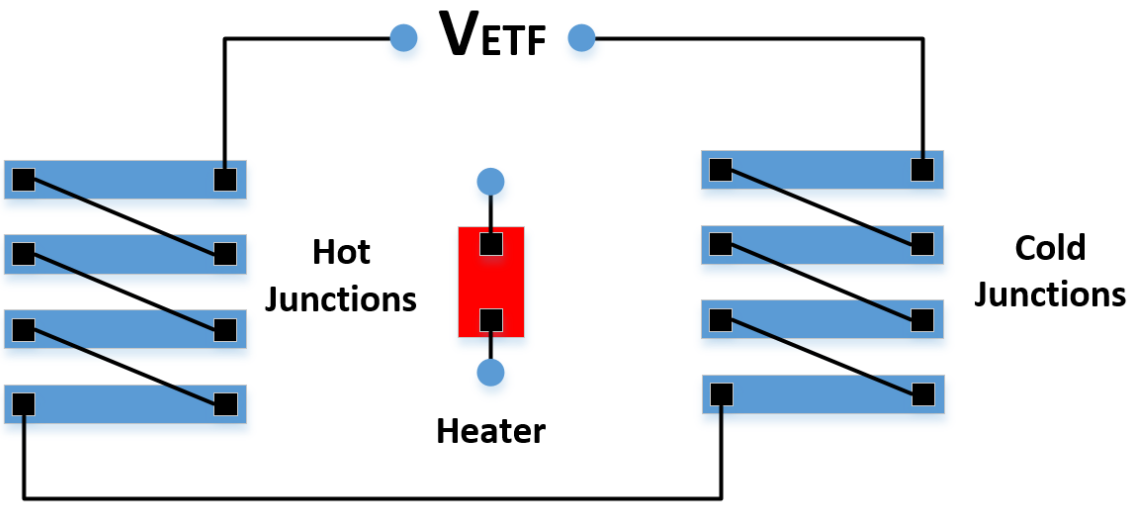


Figure.2.4 A thermopile based ETF

As mentioned earlier, there are two metallurgical junctions in thermopile ETFs, called the hot junction and the cold junction, respectively. The hot junction is closest to the heater and can detect the phase information from the delayed heating signal, while the cold junction is placed far away from the heater so that it is ideally at ambient temperature. In reality, however, it will still pick up a weak signal and reduce the voltage output of the ETF. For this reason, the cold junction should be placed as far away as possible in order to get a strong ETF signal. However, long thermopiles will exhibit significant thermal noise. From [14], the optimum SNR is achieved when the length of the thermopile is roughly equal to ‘S’.

The distance between the heater and hot junctions is critical for accuracy. In a CMOS process, the distance 'S' is defined by the mask dimensions and lithography. Lithography misalignment will result in a variation in the effective 'S', and this variation will lead to a temperature (phase) error, which is given by [14]:

$$\frac{\partial s}{s} = \frac{\partial \phi_{ETF}}{\phi_{ETF}} = 0.9\frac{\partial T}{T} \tag{2.8}$$

Therefore, an ETF's accuracy can be improved by increasing 'S'. But this will be at the expense of resolution, since the signal amplitude drops as ‘S’ increases (Eq. 2.6).

The parasitic junction capacitance of thermocouples is another source of error, since this will add extra phase-shift to the ETF signal and degrade phase accuracy. The junction

capacitance is caused by the P+ diffusion resistors and the substrate and is proportional to the thermocouple area.

Various ETF geometries have been proposed and implemented in the literature in order to achieve optimal performance.

2.2.1 – Bar ETF

The simplest ETF geometry is the bar ETF, whose layout is shown in Figure 2.4. In this type of ETF, a bar-shaped heater is surrounded by a number of thin, long thermocouples that are perpendicular to the heater. The bar ETF is simple, but is not optimal for SNR [24], since the phase of the heatwave is not the same for each hot junction and the temperature information picked up by each thermocouple does not sum up coherently. Therefore, heat generated at the edges of the heater is wasted.

2.2.2 – Phase contour ETF

X. Sha et al. proposed a new type of ETF [24], in which the hot junctions are placed on a constant phase shift contour around the heater, shown in Fig. 2.5. The resulting SNR was 50% better than a Bar ETF with approximately the same delay. In this ETF, the heater was miniaturized, so that it approximates a point-source. All of the heat generated by the heater can then be detected by the hot junctions in a coherent fashion. Both hot and cold junctions are placed on a circular pattern around the heater and the radial distance 'S' defines a specific phase shift.

Phase contour ETFs have been used in integrated temperature sensors, which have achieved excellent accuracy ($0.2℃(3\sigma)$) [8]. However, since the hot junctions did not completely surround the heater, some of its thermal output is lost, resulting in a sub-optimal SNR.

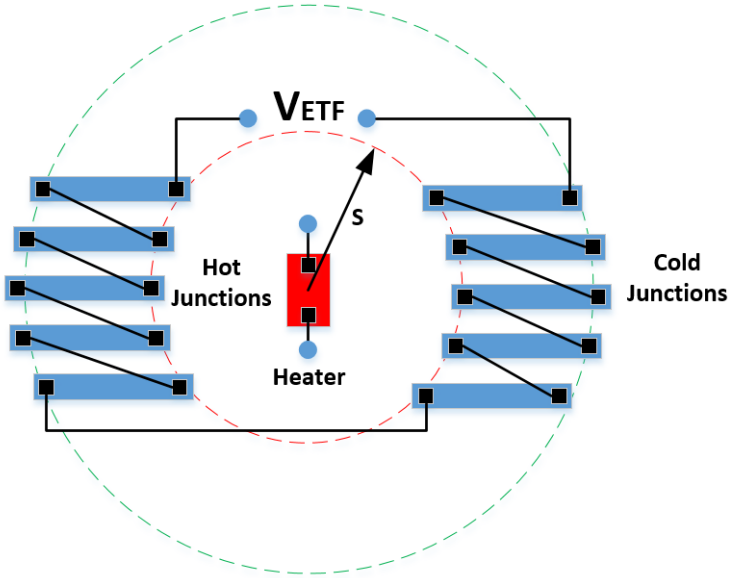


Figure.2.5 A phase contour ETF

2.2.3 – Polygon ETF

In order to improve the SNR of phase contour ETF, U. Sönmez et al. proposed a polygon ETF [15], as shown in Figure 2.6, in which the thermocouples have been expanded to fully cover the area between hot and cold phase contours. In this way, the resistance (or thermal noise) of thermocouples is reduced, which boosts the ETF's SNR. One drawback of this ETF is a somewhat larger parasitic junction capacitance since it covers a much larger silicon area. This, in turn, means that (the spread) in its RC phase shift will contribute more error.

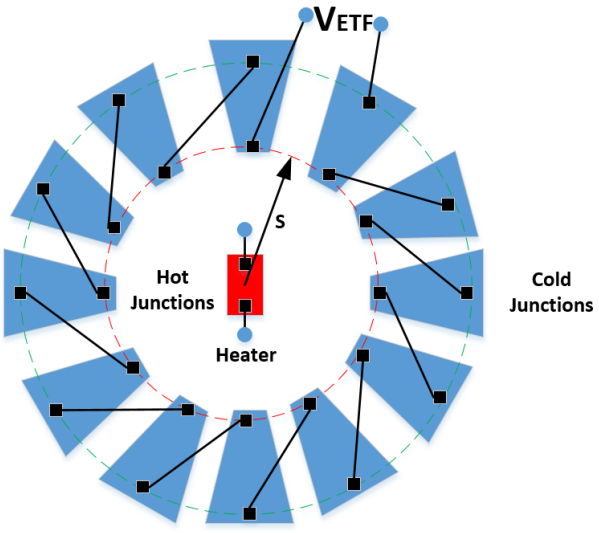


Figure.2.6 A polygon ETF

2.3 – ETF Accuracy

As mentioned earlier, accuracy is one of the most important specifications of a temperature sensor. Two dominant limitations on the accuracy of ETFs will be discussed in this section.

2.3.1 – Lithography

From equation 2.8, lithographic misalignment will cause 'S' of ETF to spread, which will result in a phase shift spread and temperature error. The spread of 'S' can be estimated from the accuracy of the process masks used to build the ETF.

As shown in Fig.2.7, in the case of a thermopile ETF implemented in a modern CMOS process, two masks define 'S': the active (p+) and the silicide protection masks. The distance S0 and S1 in the figure indicate the closest and farthest end of the hot junction from the mid-point of the heater. Then the effective 'S' can be approximated as (S0+S1)/2. The distance S0 is determined only by the p+ active mask, while S1 is defined by both P+ active and silicide protection masks. Therefore, the misalignment of these masks defines the spread in ‘S’ [23].

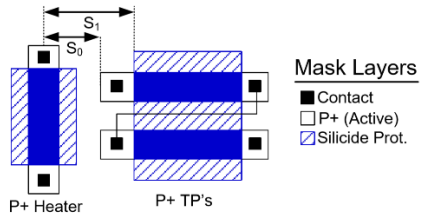


Figure.2.7 The layout of a simple bar ETF, showing the three masks involved [23]

As shown in Fig. 2.8, the accuracy can be improved by extending the silicide protection mask of the heater resistor so that S0 and S1 are only determined by the silicide protection mask [23].

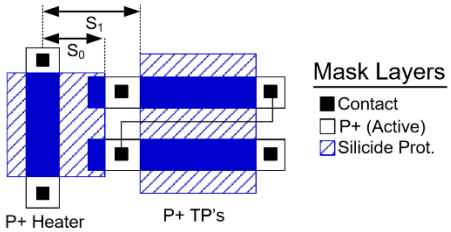


Figure.2.8 The improved layout of a BAR ETF, in which only the silicide protection mask defines the critical distance 'S' [23]

2.3.2 – Self-heating effect

Apart from a dynamic heat signal, the DC component of P_{heater} will result in a static temperature gradient across the thermopile [14]. For heat diffusing from a point heater to a point sensor in a semi-sphere of silicon, the static temperature increase at a radius 'S' is given by:

$$T_{DC}(s) = \frac{P_{heater}}{2\pi k_{si} s} \tag{2.9}$$

From Eq.2.2, variations of the heater resistance or the supply voltage will both result in temperature errors. Apart from this static temperature offset, the finite thermal impedance of the package also leads to temperature spread. For example, a typical ceramic package has a thermal impedance of 50℃/W [25], which will also spread depending on how the package is mounted on a PCB. Hence, the total error due to the self-heating effect can be approximated as:

$$T_{selft-heating}(s) = \frac{P_{heater}}{2\pi k_{si} s} + P_{heater} \times Z_{package} \tag{2.10}$$

Assuming a thermopile with S = 24μm, $Z_{package}$ = 50℃/W, and a 5% spread in P_{heater} = 10mW, the total error due to the self-heating effect would be 0.05℃. This error can be reduced by precisely controlling the ETF's heating power, at the cost of more complex readout circuits.

2.4 – ETF resolution

As shown in Figure 2.11, the performance of previous TD sensors shows that accuracy improves with a larger 'S' and with better process technology. In a 180nm process, 'S' should be increased to 96μm to achieve a 0.05℃ (3σ) accuracy. Then in order not to add significant error after a single measurement, the resolution of the ETF should be below 0.01℃(3σ).

Self-heating effect is another limiting factor. As shown above, for an S24 thermopile ETF, the maximum allowed P_{heater} under the 0.05 ℃ accuracy constraint is 10mW.

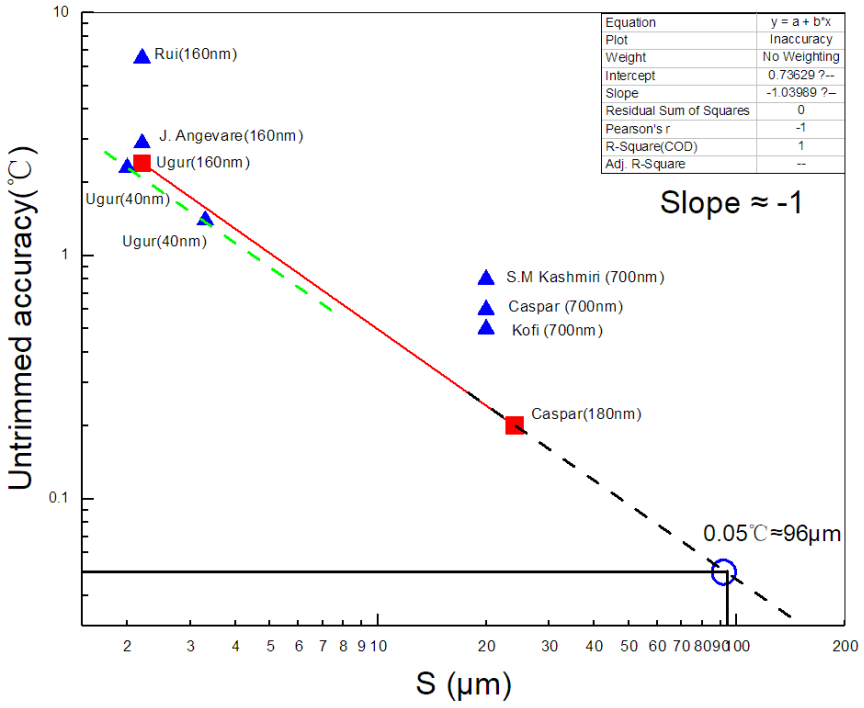


Figure 2.11 ETF accuracy as a function of 'S'

Table 2.1 shows how the resolution is estimated for a phase contour ETF with S=96 μm. Comparing to [8], 'S' is quadrupled, which means that the ETF's output signal becomes 4x weaker, while a thermopile with optimal length (96μm) would exhibit 4x more thermal noise power. The number of thermopiles can be enlarged to 96 to improve the signal amplitude by 2x. Taking these factors into account, the estimated resolution is 150m℃rms.

If a polygon ETF is used, the resistance of the ETF will drop by 2.9x so its resolution will be improved by 70% [23] compared to the optimized phase contour ETF. Thus the best resolution possible with an S96 thermopile based ETF is 30m℃rms, which is still 3x worse than the targeted value. Hence, a new type of ETF with much better resolution is required.

Figure 2 Resolution estimation of Phase contour ETF (S96)

	'S'	Pheater	Conversion rate (Sample/s)	Number of TP	Length of TP	Resolution
Caspar's Work	**24 μm**	**2.5mW**	**0.16**	**24**	**24 μm**	**20m ℃rms**
Phase contour ETF(S96)	**96 μm**	**10mW**	**1**	**96**	**96 μm**	**50m ℃rms**
Scaled factor for resolution	**4 x**	**0.25 x**	**2.5 x**	**0.5 x**	**2x**	**2.5 x**

2.5 – Summary

Design considerations and accuracy limitations of thermopile ETFs have been described in this chapter. Based on a point-heater point-sensor ETF, a thermal-electrical model has been built which offers useful insights into the thermal diffusivity based temperature sensors. Different limiting factors (lithography, self-heating and resolution) of the ETFs have been analyzed, which show that in a 180nm CMOS process, the traditional thermopile ETF cannot meet the targeted requirements. Hence, a new type of ETF with better accuracy/resolution needs to be designed.

3 – Ring ETF

In this chapter, a new type of resistor-based ETF, known as a ring ETF, is presented, which has a much higher resolution than previous thermopile-based ETFs. Its pros and cons, working principle, design considerations will be discussed in detail.

3.1 – Principles

In a ring ETF, the signals generated by the heater are detected by a ring-shaped thermistor rather than by a thermopile. As shown in Fig. 3.1, four heaters are placed in the center of four ring-shaped thermistors, which are configured as a Wheatstone bridge. The heaters are driven in anti-phase so that two of them are heating up while the other two are cooling down. The distance 'S' can be defined as the average radius of the rings.

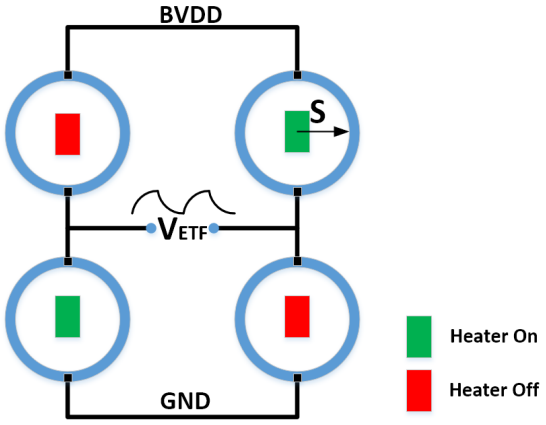


Figure.3.1 A basic Ring ETF in one phase

During operation, the heaters are switched on or off alternately at a fixed driving frequency. In one phase, the bottom left and top right heaters are turned on, while the other heaters are off. The resistance R_{ring} of the corresponding thermistors will increase to $R_{ring} \times (1 + \Delta T * T_C)$, where Tc is its temperature coefficient, and ΔT is the raised temperature. In the meantime, the other two thermistors will be cooling down, and their resistance will be decreasing. In the next phase, their resistance will start increasing as the bottom right and top left heaters are turned on. Given a fixed supply voltage and driving frequency, the bridge will output an AC signal whose phase is proportional to the ETF's thermal delay.

Using Eq. 2.6, the amplitude of the output of a ring ETF is given by:

$$V_{Ring\_ETF}(\omega,r)=\frac{BVDD}{2}\times\frac{P_{heater}T_c}{2\pi k_{si}r}\exp(-r\sqrt{\frac{\omega}{2D_{si}}}) \quad (3.1)$$

where BV_{DD} is the Wheatstone bridge's supply voltage.

Using Eq. 2.7, the phase of the output of a Ring ETF is given by:

$$\phi_{Ring\_ETF}=-s\sqrt{\pi f_{drive}/D_{si}}\propto -s\sqrt{\pi f_{drive}T^{1.8}} \quad (3.2)$$

Like that of a thermopile ETF, ϕ_{Ring_ETF} is a well-defined function of temperature.

3.2 – Different structures

Apart from the basic Ring ETF shown in Fig 3.1, other Ring ETF configurations are possible, as shown in Fig. 3.2. The main differences are in the shape of the thermistors (full-ring, half-ring, concentric-ring or open-ring) and the number of heaters (two or four).

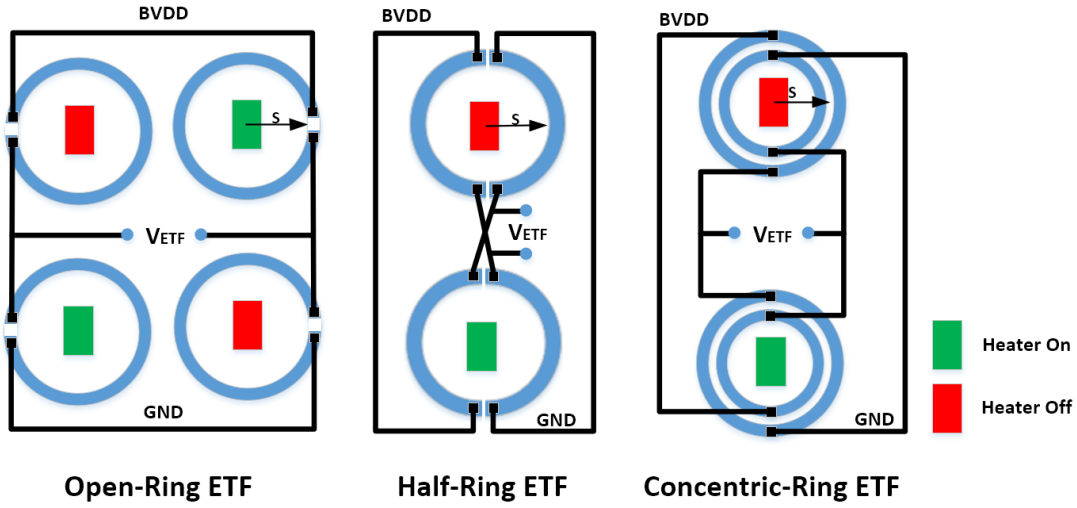


Figure.3.2 Other three types of Ring ETFs: Open-Ring ETF / Half-Ring ETF / Concentric-Ring ETF

The resistance of the thermistors of an open-ring ETF is 4x higher than the resistance of those in a basic ring ETF, which means that it dissipates less power, and can be interfaced more easily with current-based readout circuits. The half-ring and concentric ring ETFs only employ two heaters, so that their heater power is reduced by half. This improves their power-efficiency and reduces errors due to self-heating. To experimentally compare their resolution, accuracy and power efficiency, various ring ETFs with different values of "s" and different configurations have been implemented in two test chips.

3.3 – Choice of thermistor

In order to achieve a good resolution, the temperature coefficient (T_C) of the Ring resistor should be high, while its resistance (R_{ring}) should be low to minimize its thermal noise. Also, it should not be a poly resistor, since the oxide layer beneath such resistors is a good thermal insulator.

According to Cadence models of the chosen 180nm process, n-well resistors have the largest TC (0.356%/°C), but they also have a large sheet resistance (440 Ω/square). Compared to N+ diffusion resistors without silicide (0.1383%/°C, 61.6 Ω/square), the N+ diffusion resistor with silicide has ~2x larger TC (0.335%/°C), and ~10x smaller sheet resistance (6.82 Ω/square). Therefore, N+ diffusion resistors with silicide are preferred for us in ring ETFs.

Resistor width is another critical parameter because it affects the resistance and area. A wider resistor will lead to lower thermal noise and better SNR, but also to more parasitic capacitance, which can degrade accuracy. It also leads to more power dissipation, and thus self-heating.

3.4 – Resolution analysis

In the case of a Ring ETF, its phase-shifted output can be demodulated with the help of a fixed phase reference ϕ_{demod}. Assuming a square-wave reference signal as in [14], the DC component of the demodulator output V_{DC} can be expressed as:

$$V_{DC} = \frac{8}{\pi^2} \times V_{Ring\_ETF} \times \cos(\phi_{Ring\_ETF} - \phi_{demod}) \tag{3.3}$$

The sensitivity of V_{DC} to temperature is given by its derivative to T, which can be estimated by substituting the temperature dependencies of k_{si} ($k_{si} \propto T^{-1.3}$) and D_{si} ($D_{si} \propto T^{-1.8}$) in Eq. 3.3. To eliminate the supply sensitivity, V_{DC} is usually not read out directly. Instead, ϕ_{demod} is adjusted such that V_{DC} can be made zero. Thus, the cosine term in Eq.3.3 becomes $\cos(\pi/2)$ [14].

The sensitivity of V_{DC} to temperature variations can be investigated by taking the derivative of Eq.3.3, which can be simplified as:

$$\frac{\partial V_{DC}}{\partial T} \propto \frac{8}{\pi^2} \times \frac{BVDD}{2} \times \frac{P_{heater} T_c}{2\pi r} \exp(-r\sqrt{\pi f_{drive} T^{1.8}}) \times (1.3T^{0.3} - 0.9r\sqrt{\pi f_{drive}} \times T^{1.2}) \quad (3.4)$$

For Ring ETFs, the thermal noise from the bridge is the main noise source. Fig.3.3 illustrates a single ring-shaped thermistor whose resistance is given by:

$$R_{ring} = \frac{R_{sq}\pi}{2}(\frac{1}{2} + \frac{S}{W}) \quad (3.5)$$

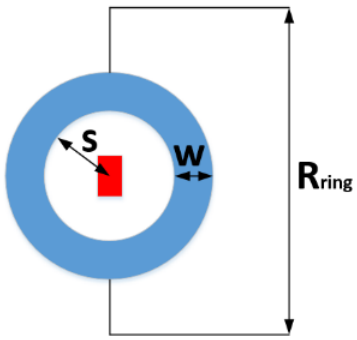


Figure 3.3 A single ring-shaped thermistor

Assuming that the input-referred noise of the phase detector is dominated by Johnson noise (white noise) with a PSD of $4KTR_{ring}$ and the bandwidth is limited to B by the low-pass filter at the output, the ETF's temperature sensing resolution can be calculated as:

$$res \approx \frac{\sqrt{4kTR_{ring}B}}{\frac{8}{\pi^2} \times \frac{BVDD}{2} \times \frac{P_{heater} T_c}{2\pi r} \exp(-r\sqrt{\pi f_{drive} T^{1.8}}) \times (1.3T^{0.3} - 0.9r\sqrt{\pi f_{drive}} \times T^{1.2})} \quad (3.6)$$

Assuming S=24μm, P_{heater} = 4mW, B=0.5Hz, T=27℃ and Fdrive=42kHz, the resolution of a Ring ETF with a minimum width (0.42 μm) resistor can be derived from Eq.3.6, which is commensurate with the target accuracy (0.05℃(3σ)), as shown in Fig.3.4. Hence, the minimum width was selected for constructing the Ring ETFs.

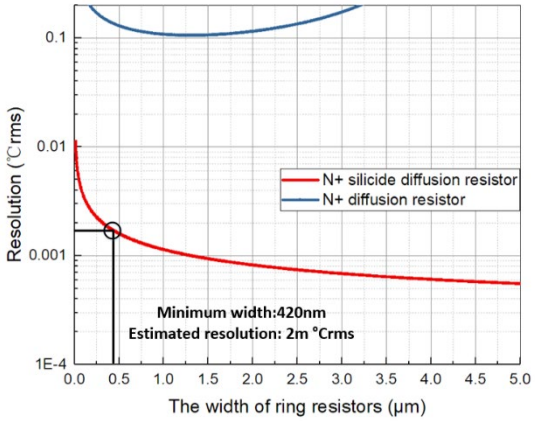


Figure3.4 Resolution versus with thermistor width: N+ diffusion resistor with or without silicide

3.5 – Ring ETF design in CMOS

3.5.1 – Layout

Due to the design rule constraints in Cadence, implementing ring-shaped thermistors is quite difficult. As shown in Fig.3.5, they have been replaced by octagonal thermistors, which are much easier to draw. The only consequence of this is that it will change the effective value of “S” to something between half the width of the octagon and half the width of its diagonal. Since they are driven in anti-phase, there will be no temperature variations at points equidistant to the two heaters. So to maximize their output signal, the octagons should not be too close together. In the test chips the distance between them is set to 100μm in the test chips, which is much larger than the largest implemented value of “S,” which was 24μm.

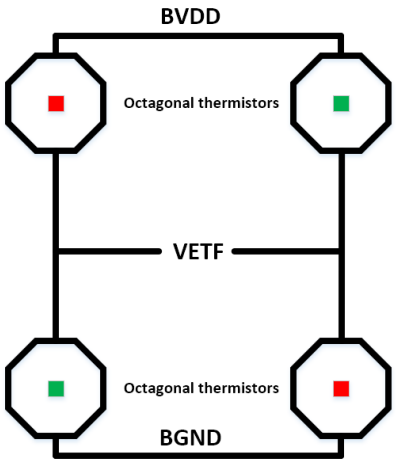


Figure.3.5 Octagonal thermistors-based Ring ETF

3.5.2 – Pros and Cons

Theoretically, Ring ETFs have several advantages compared to thermopile ETFs:

1. The structure of a Ring ETF is quite simple. Both layout and readout circuits can be implemented and scaled easily in the CMOS design.
2. The thermistors surround the heaters, which maximizes their output.
3. The effective ‘S’ is determined by a complete ring, rather than by a finite number of junction contacts as in a thermopile ETF. Thus, for the same ‘S’, the lithography-related error should be smaller.
4. For thermopile ETFs, the residual signal at cold junctions will result in a weaker output signal and a worse resolution [14]. Ring ETFs do not have cold junctions, so this issue does not arise.

However, the main drawback of Ring ETFs is larger power consumption. Apart from the heater, the bridge itself also dissipates power. The resulting self-heating may be a significant error source. Bridge offset is another disadvantage, since thermopile ETFs are intrinsically offset-free. However, this is not a major problem, since the signal of interest is an AC phase shift.

3.6 – Readout System

Since the ring ETF is a new type of ETF, it was decided to evaluate its performance by realizing a test chip with the bare minimum of readout circuitry.

The phase of an ETF can be read out by a standard lock-in amplifier (LIA). Fig.3.6 presents the corresponding block diagram. The LIA provides a reference signal that drives the on-chip heaters, and the output phase signal of one of the Ring ETF is selected by multiplexers and sent to the LIA. The phase difference between this signal and the LIA’s reference signal is a representation of temperature.

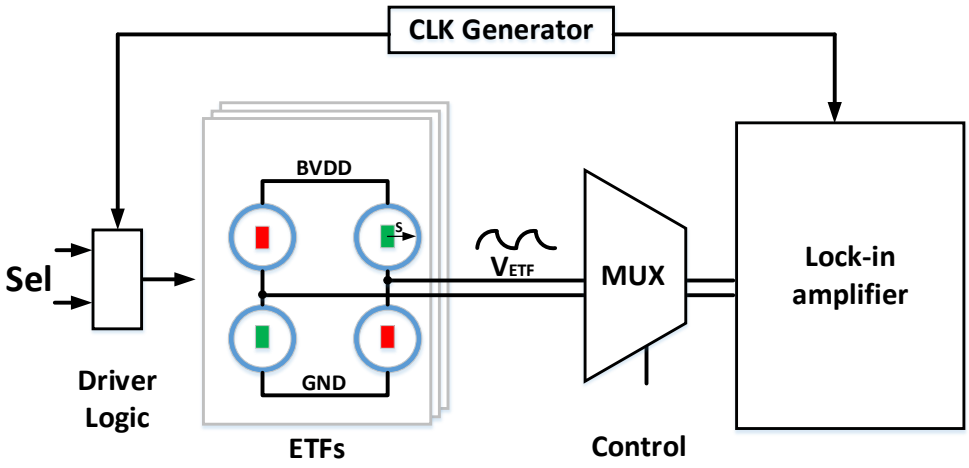


Figure.3.6 Readout system for Ring ETFs

3.7 – Error source analysis

3.7.1 – Lithography

Similar to the thermopile ETF, lithography misalignment will cause 'S' of ring ETF to spread, resulting in a phase shift spread and then a temperature error. In previous work [8] [15] [26], lithography error is suspected to be the dominant error source. It is hard to estimate this with standard simulation tools. Thus, a practical way of investigating the lithography error is by building several Ring ETFs with different ‘S’ and then analyzing the correlation between ‘S’ and temperature error.

3.7.2 – Self-heating effect

As mentioned in section 2.3.2, the variations of heater resistance, supply voltage or thermal resistance of the package all result in different levels of self-heating and thus temperature errors. In order to achieve 0.05℃ accuracy, the power consumption of a single chip should not exceed 10mW.

In addition, as temperature sensors, other heat sources on the die or PCB may potentially interfere with the temperature variations detected by ETF. When multiple ETFs are built in the same die, they should be placed far away (100μm) from each other to eliminate the interference. In addition, the heat generated by other components on the PCB (buffers and digital isolators) will affect the temperature distribution around the chips, thus resulting in significant errors as well, especially when many test chips are to be measured simultaneously on the same PCB.

3.7.3 – RC error

Any extra phase-shift that occurs in the signal path between the ETFs and the LIA will be a source of error. For example, there will be an RC error associated with the finite delay between the Ring ETF and the LIA. At the chip's output, the bridge resistance and the parasitic capacitance (pad and PCB) forms an RC low-pass filter. This adds a nominal phase offset as well as potential phase spread to ϕ_{Ring_ETF}. Assuming the phase spread is 10% and the ETFs have a phase sensitivity of 5℃/º, the temperature error could be estimated as follows:

$$T_{error\_RC} = \arctan(\frac{f_{drive}}{f_{-3dB}}) \times 10\% \times 5°C / ° \tag{3.7}$$

To guarantee 0.05℃ accuracy, this error should be at a 0.01℃ level. Hence, the phase offset should be below 20mº at a typical F_{drive}=42kHz (this choice will be discussed later), which corresponds to a -3dB-bandwidth of 120MHz.

3.7.4 – Delay of on-chip logic

Apart from the phase shift due to the thermal filtering of ETF, the delay (phase shift) of on-chip also will be measured by the LIA. Obviously, the spread of this delay will result in error as well. Assuming the delay spread is 10% and the ETFs have a phase sensitivity of 5℃/º, this temperature error is given by:

$$T_{error\_Delay} = Delay \times 10\% \times f_{drive} \times 360 \times 5°C / ° \tag{3.8}$$

From Eq.3.8, the delay of on-chip logic should be below1.3ns to ensure this error lower than 0.01℃ at F_{drive}=42kHz.

3.7.5 – Frequency reference

Another error source would be the accuracy of the frequency reference. From Eq.3.2, the phase shift of ETF is a linear function of $\sqrt{f_{drive}}$, the spread of f_{drive} will result in phase and temperature as well. This temperature error can be estimated as follows:

$$T_{error\_fdrive} = 0.5 \times S \times \sqrt{\frac{1}{D_{si}}} \times f_{drive}^{-0.5} \times \frac{180}{\pi} \times \Delta f_{drive} \times 5°C / ° \tag{3.9}$$

Assuming S=24μm, F_{drive}=42kHz, and the typical value of Dsi at room temperature is 0.7cm^2/s, the frequency accuracy should better than 120 ppm to make this error lower than 0.01℃.

3.7 –Summary

In this chapter, the Ring ETF has been presented. Its principles, resolution, structures, design considerations, advantages or disadvantages and error sources have been discussed. To characterize this new type of ETFs quickly, a simple readout system based on a lock-in-amplifier has been proposed.

4 – Test chip 1

A first prototype with Ring ETFs was fabricated in a TSMC180nm CMOS process. In this chapter, design details, measurement set-up and characterization results of this test chip will be discussed.

4.1 –Chip details

4.1.1 – ETF details

The top-level layout of this test chip is shown in Fig.4.1. It contains 8 ETFs, including 7 Ring ETFs and 1 Polygon ETF (as a reference). Table 4.1 summarizes their parameters, like their names, ETF type, 'S' and bridge resistance.

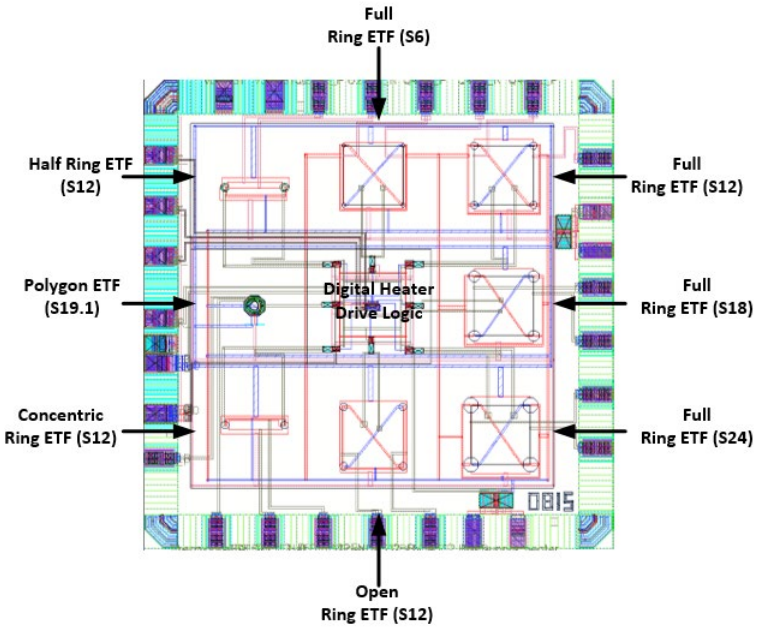


Figure.4.1 The top-level layout of this test chip 1

For the heaters, bar-shaped n+ diffusion resistors without silicide (Length: 7.2μm, Width:2.5μm, Resistance:194Ω) are used. The width of the heaters is limited by the maximum current density (800μA/μm) specified in Cadence models. This low resistance allows for a maximum heater power of 8mW which provides a large enough signal to characterize the ring ETFs.

Table-4.1 ETF details of test chip 1

No.	Name	ETF Type	Distance 'S'(μm)	Rbridge(Ω)
1	Q4S6	Full Ring	6	136
2	Q4S12	Full Ring	12	320
3	Q4S18	Full Ring	18	432
4	Q4S24	Full Ring	24	580
5	HalfS12	Half Ring	12	458
6	OpenS12	Open Ring	12	1005
7	Q2S12	Concentric Ring	12	319
8	TP	Polygon	19.1	494

4.1.2 – Circuit diagrams

As shown in Fig.4.2, the circuit diagram of a single ETF includes a heater drive circuit and a ETF core. The heater drive circuit is used to switch on/off the heater periodically after selecting by a 3-to-8 decoder. In the ETF core, the outputs are taken directly to the pads.

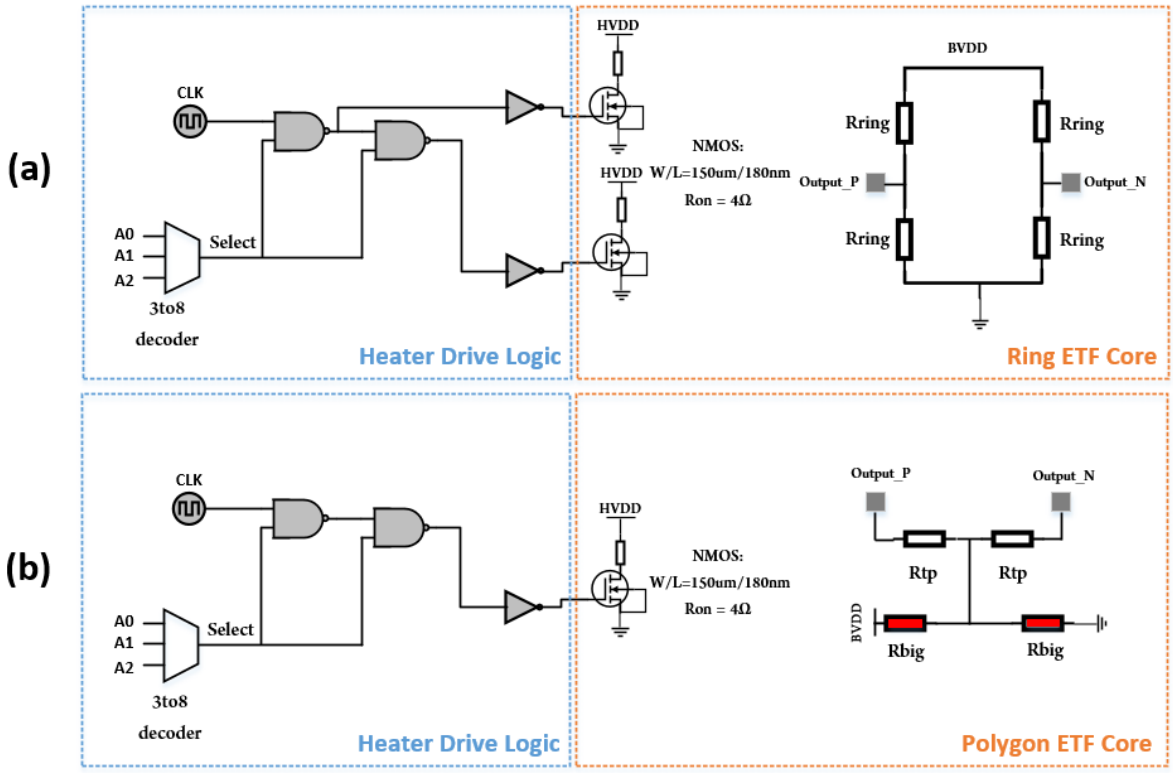


Figure 4.2 The circuit diagram of the ring ETFs (a) and the polygon ETF (b) in test chip 1

As shown in Fig.4.2, a square wave heat signal is achieved by driving an NMOS switch placed in series with the heater. For the size of driving NMOS, there is a design trade-off:

1. The on-resistance should be small enough to ensure less spread and less power wasted in the switch. In this sense, a wide NMOS switch is preferred.
2. The error due to CLK delay spread over corners should be minimized. A narrow NMOS switch is favorable because of its small gate capacitance.

Take these considerations into account, the optimal width of NMOS is around 150μm with the minimum length (0.18μm). The simulated CLK delay is 300ps. Given F_{drive}=42kHz, 20% spread of this CLK delay would result in a 5m℃ error, which is sufficiently low for the targeted accuracy. Given a 1.8V supply, the heater's power spreads by 0.4mW over corners in the simulation. Assuming S=24μm, $Z_{package}$=50℃/W, the error due to the power variation would be 0.04℃. However, in this design, the fatal flaw is the huge power consumption of bridges (81mW), since they are not multiplexed properly. As will be shown later, it introduces more than 0.5℃ error, which degrades the accuracy of the various ETFs significantly.

4.1.3 – Layout

Fig.4.3 illustrates the layout of the Q4S24 ETF in this test chip, including the bar-shaped heaters and 4 octagonal thermistors.

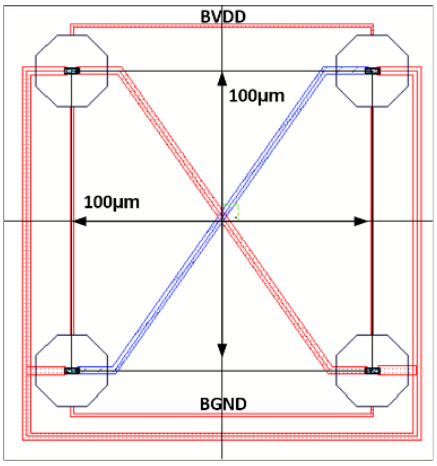


Figure 4.3 The layout of Q4S24 ETF in test chip 1

4.2 –Measurement set-up

4.2.1 – System diagrams

In all the measurements, samples were characterized in a Votsch VT 7004 oven in which temperature can be well controlled. A Pt-100 temperature sensor was used as the temperature reference, which had been calibrated to better than 10mK (from -75℃ to 145℃). Its resistance was measured by a Keithley 2002 multimeter. The resolution of the multimeter is 26 bits with a measured period of 1 power line cycle, which corresponds to 3μΩ in a 200Ω range and a temperature resolution of 7.7μK. The Pt-100 sensor was placed inside a large aluminium block, and chips were mounted on the block [27].

The diagram of measurement setup is shown in Fig.4.4. A PC was used to send all the control commands and record the data. The lock-in amplifier (LIA) was used to demodulate the outputs of ETFs and read out the phase information directly. The type of the Lock-in amplifier is SR865A. The phase noise of this amplifier (<1m° with 100ms time constant and 12dB/oct slope) can be translated to less than 5mK temperature resolution, which is sufficiently low for the target accuracy. The frequency accuracy of the LIA is 25ppm, which will result in less than 2mK temperature error (from Eq.3.9). The PCBs' design will be discussed in the next section.

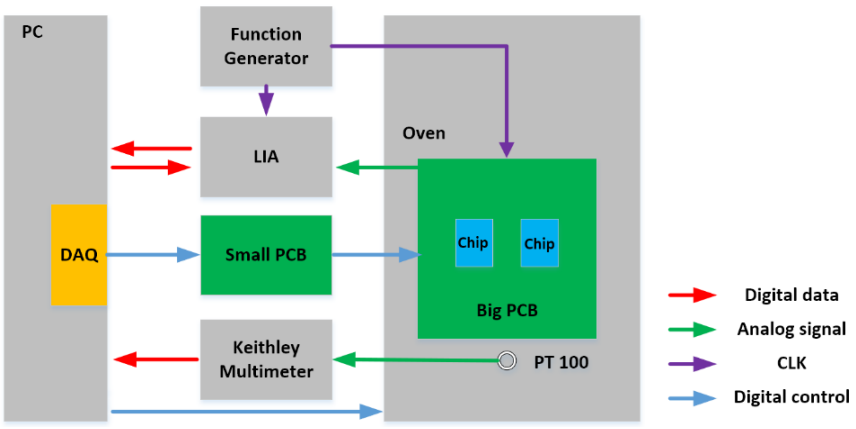


Figure.4.4 Measurement system diagram

4.2.2 – PCB design

As shown in Fig.4.5, there are 2 PCBs in the whole measurement setup. All the digital control signals are controlled by a PC and transmitted to the chips via a small PCB. the small PCB is an adaptor between a VHDCI header (PC) and a flat cable header (big PCB). In the big PCB, digital isolators are used in conjunction with isolated power supplies

to prevent noise currents on the data buses. The primary purpose of the big PCB is selecting the ETF outputs from different sensors and sending it to the lock-in amplifier.

The spread of delay (phase shift) on the readout chain can introduce significant temperature error during measurements. In order to minimize this error, the output signal is firstly buffered by a high-speed buffer (500MHz -3dB-bandwidth), and then multiplexed using reed relays (<1Ω on-resistance) before it was sent to the lock-in amplifier via coaxial cables. For the Q4S24 ETF, the large bridge resistance (580Ω) together with the total parasitic capacitance (8pF) of the pad and the PCB, limits the bandwidth of the entire readout chain to 34MHz. According to Eq.3.7, the estimated RC error is 35mK then about given F_{drive}=42kHz. Therefore, a resistor (500 Ω) and a dummy buffer in a reference CLK path are used to mimic the RC delay to provide a first order compensation.

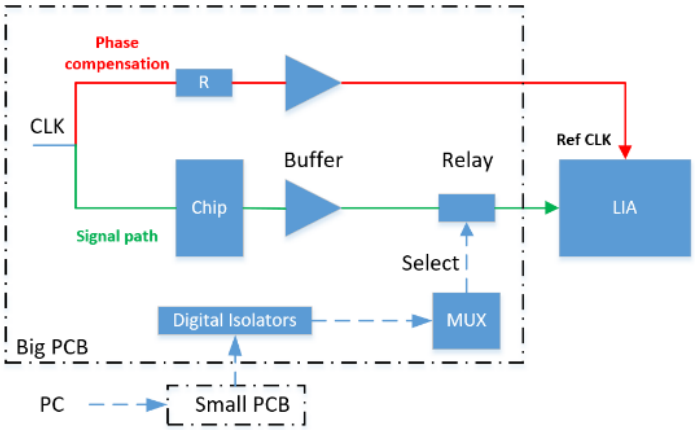


Figure 4.5 PCB diagram of this test chip 1

4.2.3 – Temperature stability control

The key accurate temperature measurements is creating a thermal equilibrium between the Pt-100 reference and the sensors so that the measurement error can be minimized. As shown in Fig.4.6, in order to achieve this, the lead of chips was touched with a thermal pad of excellent thermal conductivity (5W/mK) and screws were used to press the chips against a large block tightly. The metal block acted as a low-pass thermal filter with an extremely low corner frequency (<1mHz), keeping the sensor's temperature stable during the measurements. A metal lid was used to avoid temperature fluctuations due to airflow inside the oven. The Pt-100 temperature sensor was inserted into a hole on the block near the chips.

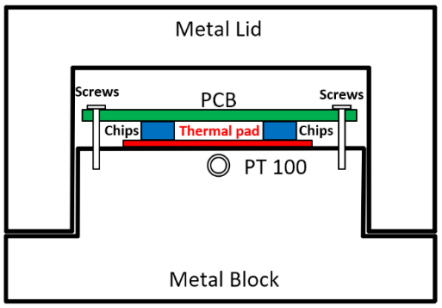


Figure.4.6 Measurement set-up for test chip 1, cross-sectional view

By recording the resistance of the PT-100 sensor with a Keithley multimeter at 30℃, the temperature stability with the metal block was measured to be 1.5mK (3σ) with a 0.1Hz sampling rate. In the accuracy measurements, the difference between two successive readouts of the Pt-100 temperature reference (about 30s per readout) was measured to be less than 1mK, this results held for 300 successive readouts without any exception. Therefore, the Pt-100 and the chips could then be considered to be in thermal equilibrium, and thus the LIA could start to capture the signals. For a single temperature point, the oven takes about 4 hours to settle.

4.2.4 – Set-up evolvements

To speed up the measurements, initially, two sockets were placed on the big PCB so that two chips could be measured in the same oven run. However, the phase spread between two sockets was measured to be 15m°, leading to around 1℃ temperature error. In order to eliminate the socket dependency, we finally decided to use only one socket to measure the chips, at a cost of 2x more measurement time.

4.3 –Measurement results

4.3.1 – Phase characteristics

The initial measurements (Fig.4.7) show that ϕ_{Ring_ETF} is a near-linear function of temperature as expected from Eq.3.2. This validates the Ring ETF's temperature sensing potential.

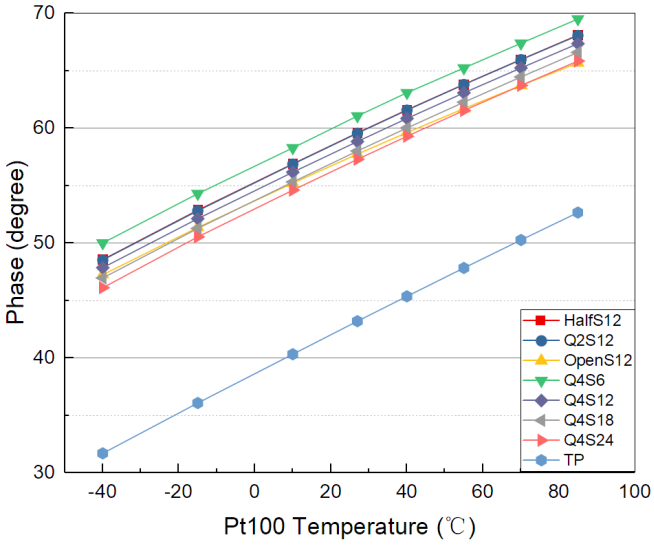


Figure.4.7 Phase versus temperature at a constant driving frequency

To investigate whether the phase shifts are as expected, we can define a normalization factor 'X' given by: $X=\mathrm{S}\times\sqrt{f_{drive}}$. As suggested by Eq.3.2, at a certain temperature, this 'X' should be proportional to the ETF's output phase with a slope of $\sqrt{\frac{\pi}{D_{si}}}$. As shown in Fig.4.8, at a fixed temperature (27℃), all Ring ETFs exhibited this feature, which is similar to the thermopile ETF.

However, the bar heater was not an ideal point source in our design, so the effective 'S' is layout dependent. Assuming D_{si} is constant, we can use the results from a reference ETF (S24) to compute the effective 'S' and the thermal diffusivity D_{si} of the substrate from the measured slopes:

$$S_{\text{effective}} = \frac{Slope_{\text{ref}}}{Slope_{measured}} \times S_{\text{nominal}} \qquad (4.1)$$

The effective 'S' of 8 ETFs and estimated D_{si} are summarized in Table 4.2 as well. The effective value of thermal diffusivity 'Dsi' (0.7cm^2/s) matches well with the results in [26]. By replacing the nominal 'S' with the effective 'S' and adjusting normalization factor 'X', all the curves we found to overlap as shown in Fig.4.9.

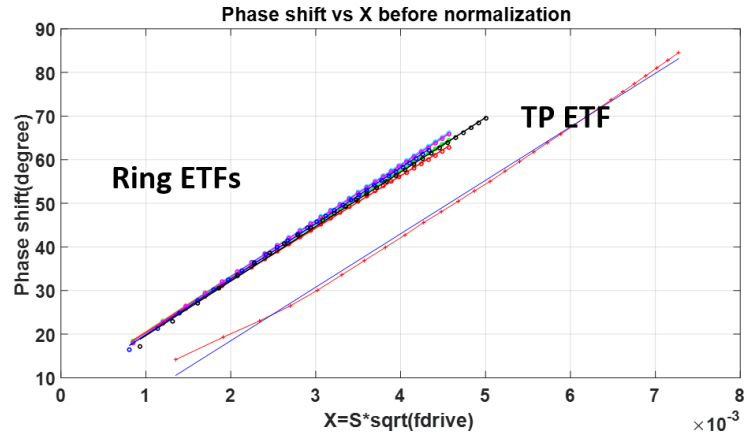


Figure.4.8 Phase vs. 'X', before normalization

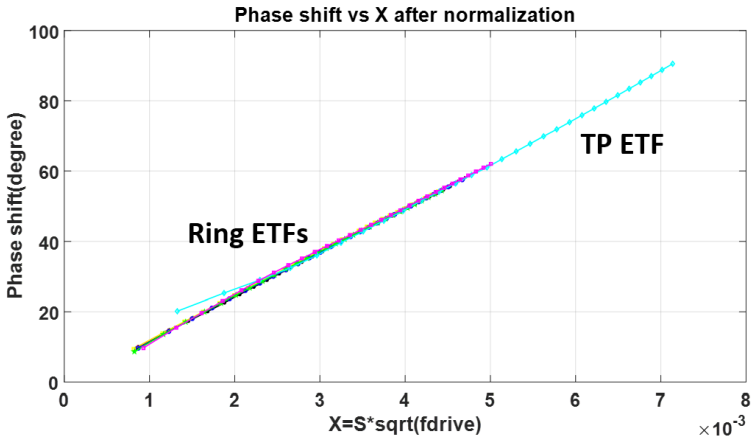


Figure 4.9 Phase vs. 'X', after normalization

4.3.2 – Resolution optimization

Maximizing the temperature-sensing resolution of ETFs is an important way of preventing noise from degrading the measurement accuracy. Hence, it is important to find the optimal driving frequency for ETFs and maximize the resolution. From Eq.3.6, theoretical analysis of the resolution is too complex obviously, so an experimental approach is used.

Considering a point heater ETF driven by a sine wave, whose phase shift ϕ_{ETF} is read out by a phase detector in the lock-in amplifier. The filtered output will be a DC component given by:

$$V_{DC} = A_{ETF} \times \mathrm{Sin}(\phi_{ETF} - \phi_{demo}) \qquad (4.2)$$

where A_{ETF} is the amplitude of the ETF output and ϕ_{demo} is the reference phase for demodulation. After using a lock-in amplifier to measure A_{ETF} and ϕ_{ETF} at two close temperatures, e.g. T1 (27℃) and T2 (30℃), the sensitivity $\frac{\partial V_{DC}}{\partial T}$ of ETF could be calculated as follows:

$$\frac{\partial V_{DC}}{\partial T} = \frac{A_{ETF,T_2} \times \mathrm{Sin}(\phi_{ETF,T_2} - \phi_{demo}) - A_{ETF,T_1} \times \mathrm{Sin}(\phi_{ETF,T_1} - \phi_{demo})}{T_2 - T_1} \tag{4.3}$$

Since A_{ETF} changes much slowly with temperature, A_{ETF,T_2} is approximately equal to A_{ETF,T_1}, then the sensitivity $\frac{\partial V_{DC}}{\partial T}$ of ETF is approximately:

$$\begin{aligned} \frac{\partial V_{DC}}{\partial T} &\approx \frac{A_{ETF,T_2} \times \left[\mathrm{Sin}(\phi_{ETF,T_2} - \phi_{demo}) - \mathrm{Sin}(\phi_{ETF,T_1} - \phi_{demo}) \right]}{T_2 - T_1} \\ &\approx 2 \times A_{ETF,T_2} \times \frac{\mathrm{Sin}(\frac{\phi_{ETF,T_2} - \phi_{ETF,T_1}}{2})}{(T_2 - T_1)} \times \mathrm{Cos}(\frac{\phi_{ETF,T_2} + \phi_{ETF,T_1}}{2} - \phi_{demo}) \end{aligned} \tag{4.4}$$

ϕ_{demod} is adjusted such that V_{DC} can be made zero. Thus, the cosine term in Eq.4.4 becomes cos(π/2) [14]. And the phase difference $\left(\phi_{ETF,T_2} - \phi_{ETF,T_1}\right)$ is close to zero. Then the sensitivity of V_{DC} to temperature variations can be simplified further as follows:

$$\frac{\partial V_{DC}}{\partial T} \approx A_{ETF,T_2} \times \frac{\mathrm{Sin}(\phi_{ETF,T_2} - \phi_{ETF,T_1})}{(T_2 - T_1)} \tag{4.5}$$

After sweeping the driving frequency, we would be able to find out the optimal F_{drive} to maximize the sensitivity $\frac{\partial V_{DC}}{\partial T}$. The measured $\frac{\partial V_{DC}}{\partial T}$ is shown in Fig.4.10, which increases at first and then decreases with the driving frequency.

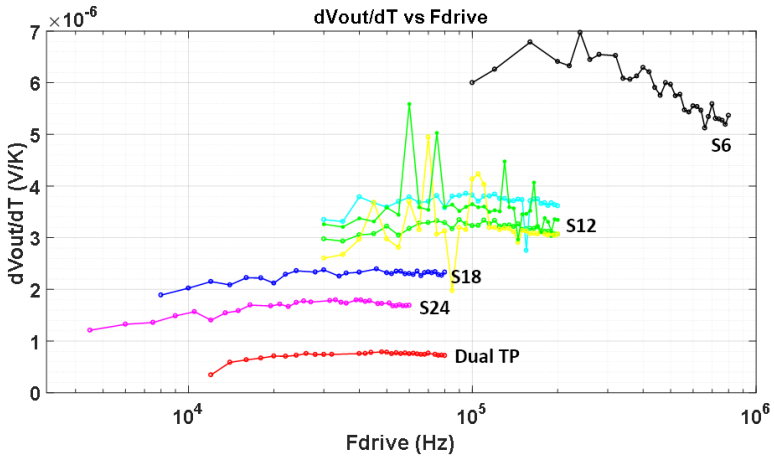


Figure 4.10 Fdrive optimization for 8 ETFs

Given the optimal driving frequency, the temperature sensing resolution of a ETF can be calculated as follows:

$$res = \frac{\sqrt{4kTR_{bridge}B}}{\left(\partial V_{DC} / \partial T\right)} \tag{4.6}$$

The optimal frequencies and calculated resolutions are listed in Table 4.2. The resolutions of all ring ETFs are lower than 2m ℃rms in a bandwidth of 0.5Hz.

4.3.3 – Untrimmed accuracy

To reduce the significant error due to the huge power of bridges and evaluate the real spread of ETF, two approaches are proposed: power regulation & extrapolation , and FIB circuit edit.

4.3.3.1 – Power regulation and extrapolation

The first approach is to regulate the total power dissipation P_{total} of chips at two power modes by first adjusting the power supplies of bridges and heaters, then plotting the phase versus P_{total}, and finally doing the extrapolation to find the expected phase output when P_{total} =0. After the extrapolation, the Q4S18 ETF has the best accuracy among all the ETFs. As shown in Fig.4.11, its 3σ spread (16 samples) of phase at 0 power dissipation is about ±0.04° at room temperature. With the measured phase-sensitivity of 7°C/°p, the untrimmed inaccuracy is ±0.3 ℃ (3σ). By implementing this approach, the measured temperature spread of various ETFs is summarized in Table 4.2.

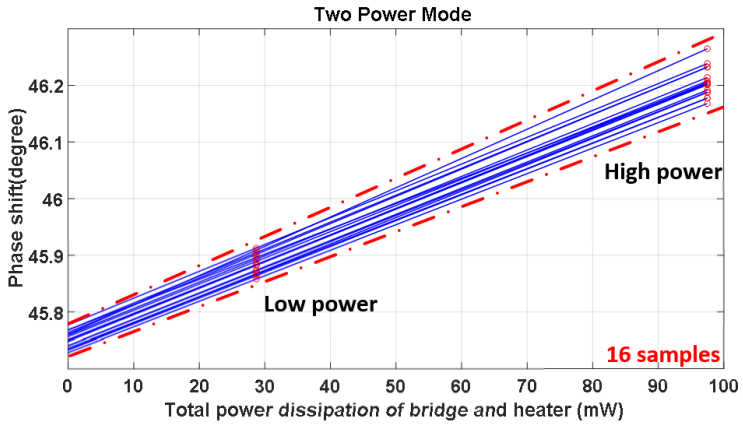


Figure 4.11 Power regulation and extrapolation to reduce the self-heating effect

4.3.3.2 – FIB circuit edit

A costly way is to use FIB to modify the on-chip circuits. Thanks to the help of ADI, 7 out of 8 bridges were disabled by disconnecting them from the bridge's power supply, and only the Q4S18 ETF remained operational. As a result, the total power consumption of the entire chip dropped by 7x roughly. 5 devices were measured at 27℃, the phase spread was 400m°, which corresponds to 0.28℃ (3σ) temperature error.

4.4 –Summary table

Table-4.2 Measurement result summary for test chip 1

No.	ETF Type	'S' (μm)	Effective 'S' (μm)	Estimated 'Dsi' (cm^2/s)	Optimal 'Fdrive' (kHz)	Resolution (m℃rms)	Untrimmed accuracy at 27℃ (℃(3σ))
1	Full Ring	6	6.2	0.76	300	0.15	1.05
2	Full Ring	12	11.9	0.70	100	0.50	0.47
3	Full Ring	18	17.8	0.69	46	0.79	0.30 (*1) 0.28 (*2)
4	Full Ring	24	24 (ref)	0.7	35	1.22	0.51
5	Half Ring	12	11.9	0.69	100	0.51	0.41
6	Open Ring	12	12.3	0.75	100	0.91	0.54
7	Concentric Ring	12	11.8	0.68	100	0.44	0.64
8	Polygon	19.1	19.7	0.75	46	2.58	0.44

*1: The estimated untrimmed accuracy with power regulation and extrapolation (16 samples)
*2: The estimated untrimmed accuracy with FIB circuit edit (5 samples)

4.5 –Summary

In this chapter, the design details, measurement set-up and characterization results of test chip 1 have been discussed. Similar to thermopile ETFs, the phase shift of ring ETF has a near-linear $T^{0.9}$ temperature dependency. Given the same measurement set-up, ring ETFs exhibit high enough resolution (<2m ℃rms) and good untrimmed inaccuracy (Q4S18: 0.3℃(3σ)). In conclusion, they have the potential to be used as electrothermal filters for no-trim temperature sensors.

However, both the self-heating effect and RC error degraded the performance of ring ETFs too much. To investigate them further, an improved version of test chip will be discussed in the next chapter.

5 – Test chip 2

The second prototype chip of ring ETFs was fabricated in the ADI180nm CMOS process. The first prototype chip was transferred to ADI, where it was modified and improved mainly by a small team, including Jed Hurwitz, Declan McDonagh, Chris Brown, Caspar Van Vroonhoven and Jeo Spalding. In this chapter, the chip details, measurement set-up and characterization results will be discussed.

5.1 –Chip details and improvements

5.1.1 – ETF details

The top-level layout of this test chip 2 is shown in the figure below. This test chip also contains 8 ETFs, including 7 Ring ETFs and 1 Dual-Polygon ETF (as a reference). Table 5.1 shows their parameters.

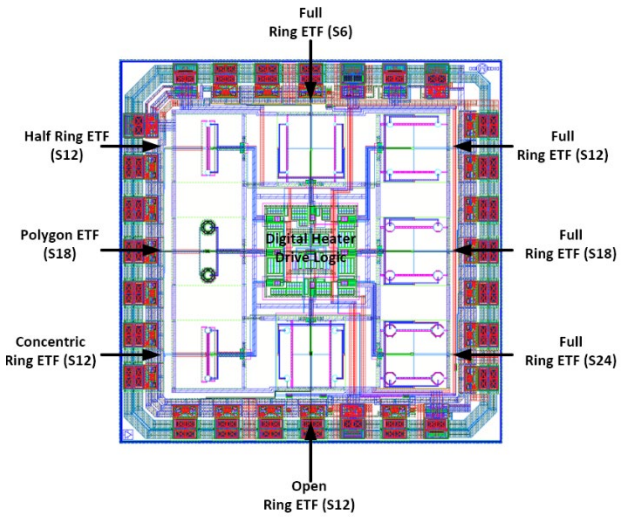


Figure.5.1 The top-level layout of test chip 2

Table-5.1 ETF details of test chip 2

No.	Name	ETF Type	Distance 'S'(μm)	Rbridge(Ω)
1	Q4S6	Full Ring	6	175
2	Q4S12	Full Ring	12	236
3	Q4S18	Full Ring	18	349
4	Q4S24	Full Ring	24	464
5	HalfS12	Half Ring	12	456
6	OpenS12	Open Ring	12	918
7	Q2S12	Concentric Ring	12	243
8	Dual-TP	Polygon	18	630

5.1.2 – Chip improvements

Five main changes were made in the new chip to improve its performance:

1. The bridges were multiplexed so that the chip dissipated ~5x less power, leading to much less temperature error due to self-heating effects.

2. The phase shift due to the RC filtering and the delay of the on-chip logic circuits, can be measured and compensated. This will be discussed in section 5.1.3.

3. Instead of using the bar heater, a compact octagonal heater was implemented. As shown in Fig 5.2, the contact vias were placed inside the ring, making the radius of the whole heater smaller than 2μm. Thus, it behaves more like an ideal point source compared to the bar heater (7.2μm x 2.5μm). The resistance of new heater is about 560Ω, so each heater would consume 3mW power when driven by a square wave with a 1.8Vpp amplitude.

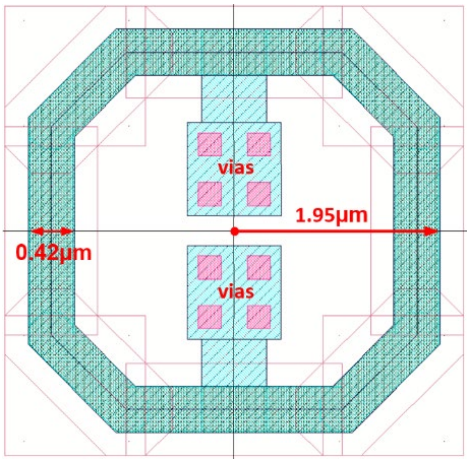


Figure.5.2 The octagonal heater in test chip 2

4. To minimize the crosstalk between heater/clock lines and signal lines, shielding layers were used. As Fig 5.3 shows, the heaters were shielded by a wall of M1 and M2, then capped by M3, while the connections to heaters were brought up to M4 and M5. The thermistors were shielded as well. For the S24 ETF, the extra parasitic capacitance associated with the shields was estimated to be in the magnitude of fF, which is negligible.

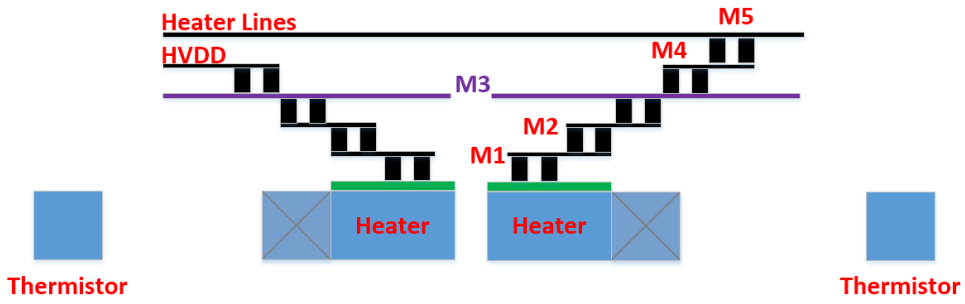


Figure 5.3 Shielding layers are used to avoid crosstalk

5. The single thermopile ETF was replaced by a dual thermopile ETF to provide a balanced output and improve the signal level by 2x thus $\sqrt{2}$x better resolution. However, this comes at the expense of doubling the heater power. Figure 5.4 shows the structure of the dual-thermopile ETF.

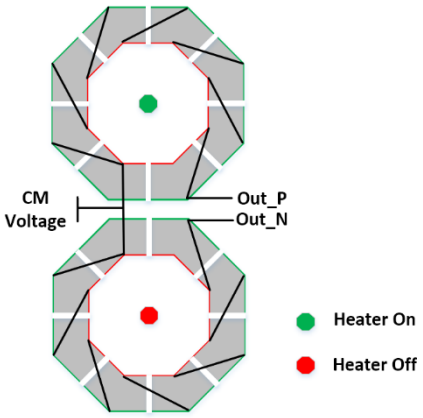


Figure 5.4 The structure of the dual-thermopile ETF

5.1.3 – Circuit diagrams

5.1.3.1 – Phase autozeroing

The ETFs can be operated in two different modes: the normal mode and the test mode. In the normal mode, the heaters are driven by a square-wave and the ETFs behave as typical TD sensors. The phase shift is ϕ_{normal}. In the test mode, all heaters are switched off and two long modulating NMOS beside the bridge are turned on/off at the same driving frequency as shown in Fig.5.5 (b). Thus, a small differential square-wave voltage is generated at the ETF outputs. The phase shift of this voltage ϕ_{test} should be identical to the additional phase shift due to RC filtering and on-chip logic in the normal mode. Hence,

the exact phase shift due to the thermal diffusion process of ETF can be computed as follows:

$$\phi_{ETF} = \phi_{\text{normal}} - \phi_{\text{test}} \tag{5.1}$$

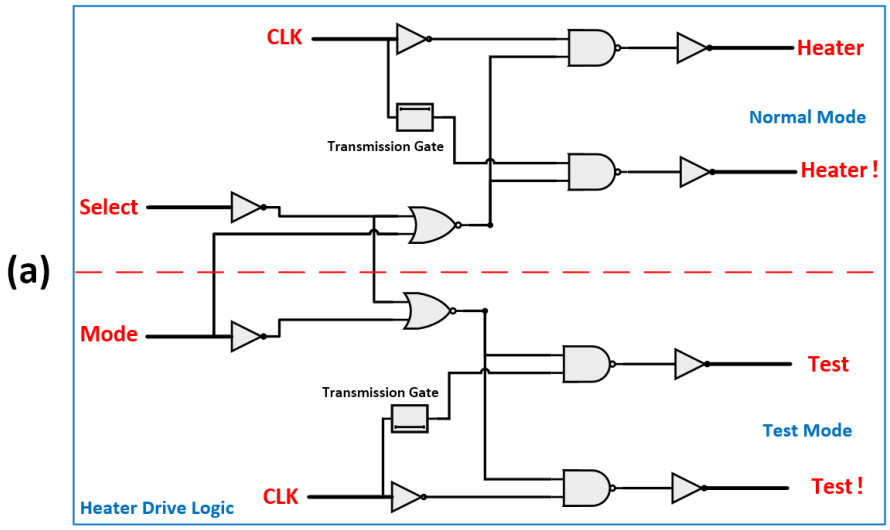
With this approach, the spread of on-chip logic delay and RC delay is expected to be reduced dramatically.

5.1.3.2 – Circuit implementation

Like test chip 1, the heater is driven by a single NMOS switch. Apart from the CLK and 3-bit address, another pair of control signals (Test/Test!) are added to switch between two modes. As shown in Fig 5.5, a transmission gate is used to compensate for the delay of the first inverter. This ensures that the edges of Heater and Heater! are well synchronized. An NMOS is placed in series with the bridge to disable it when select ='0'.

For phase autozeroing, the on-resistance of the modulating NMOS is about 10kΩ. To obtain similar amplitude outputs for the different ETFs, the associated NMOS switches are designed to have different on-resistances.

In addition, the gates of the modulating NMOS are loaded with MOS caps of the same size as the heater drive NMOS, which makes the delay difference between two modes negligible (<10ps).



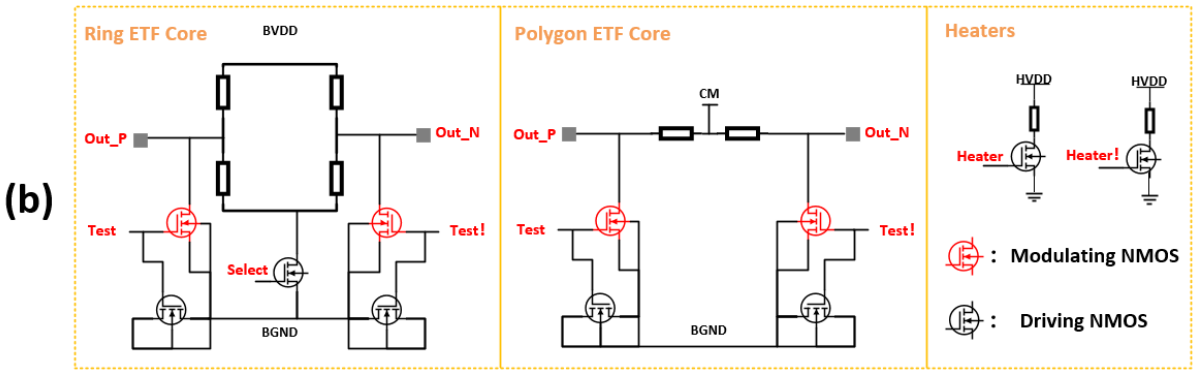


Figure 5.5 The circuit diagram of ring ETF and polygon ETF in test chip 2, including heater drive circuits (a) and ETF cores (b)

5.1.4 – Layout

Fig.5.6 illustrates the layout of Q4S24 ETF in this test chip, including the octagonal heaters and 4 octagonal thermistors.

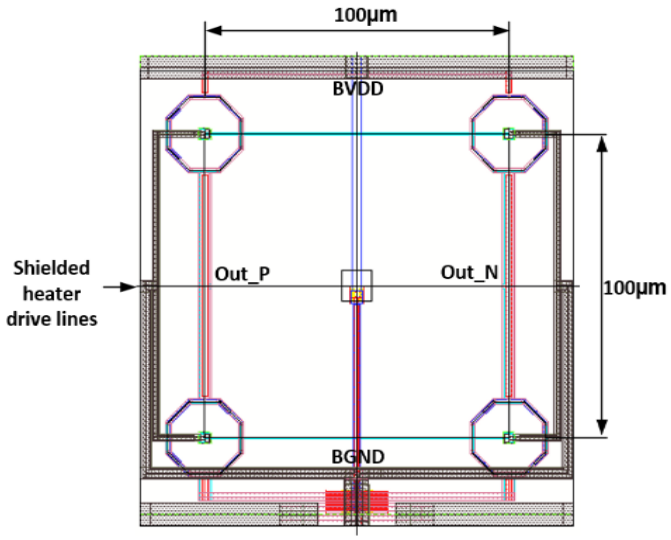


Figure 5.6 The layout of Q4S24 ETF in test chip 2

5.2 –Measurement set-up

Since the measurement system of test chip 2 is quite similar to that of test chip 1, this section will only focus on the PCB design and set-up evolvements.

5.2.1 – PCB design

To speed up the measurements, a larger PCB was designed so that 8 chips (64ETFs) can be characterized in a single oven run. As mentioned early, the introduction of test mode should make the RC errors insignificant, which relaxes the PCB design. However, we expect that the phase compensation would perform better when the bandwidth of the entire readout chain is higher.

Fig.5.7 presents the system diagram of PCBs. The outputs are multiplexed by 2 levels of 8-to-1 MUX's together with 3 levels of high-speed buffer (500MHz -3dB bandwidth). The RC delay is dominated by the bridge and the parasitic capacitors of pad, traces, and buffers (~8pF). Assuming S =24μm, optimal F_{drive}= 35kHz, Rbridge=464Ω, phase sensitivity= 7℃/°p, the -3dB bandwidth is around 43MHz. The phase shift is 47m°,10% spread of it would causea temperature error of about 0.03°C before compensation.

For each chip, 16 1st-level buffers are placed close to the pins to reduce the parasitic capacitance of traces. To save power, only one group of buffers are turned on when the chip is selected. Totally, the big PCB employees 146 buffers (1st-level: 128 , 2nd-level: 16,3rd-level: 2) and 18 8-to-1 MUXes (1st-level: 16, 2nd-level: 2).

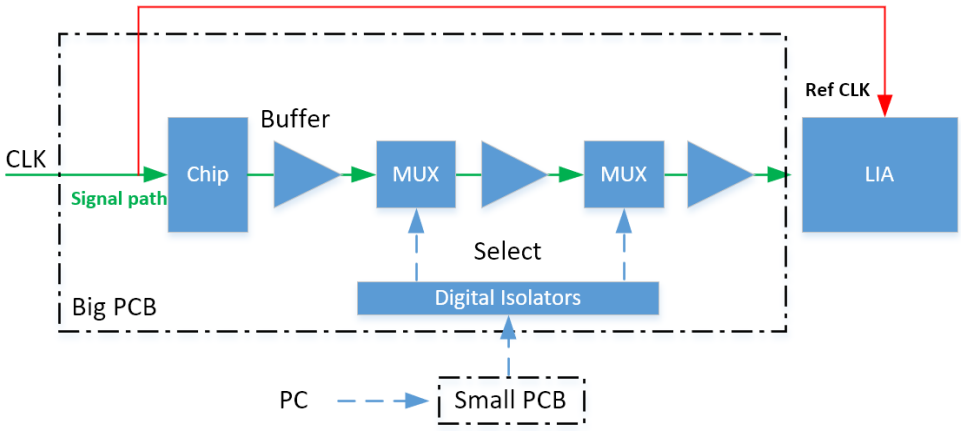


Figure 5.7 PCB system diagram of test chip 2

5.2.2 – Set-up evolvements

5.2.2.1 – New set-up

Since this PCB cannot fit with the previous aluminum block, a new set-up is needed. Fig.5.8 shows the new set-up, in which a steel plate was used to press the chips against the block for better thermal contact. A metal box was used to avoid temperature

fluctuations due to the airflow in the oven. Instead of using the thermal pad, chips were covered by the thermal paste and attached to the block directly, which is helpful to achieve better thermal equilibrium between chips and the block.

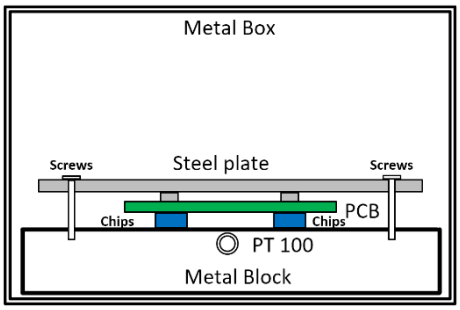


Figure 5.8 New set-up for test chip 2, cross-sectional view

5.2.2.2 – PCB modification

As discussed in section 3.6.2, any heat generated by the components on the PCB will destroy the temperature equilibrium between the chips and block, therefore resulting in a significant error. During the measurements, 34 buffers (1^{st}-level: 16, 2^{nd}-level:16, 3^{rd}-level: 2) are switched on concurrently and consume 680mW power. This resulted in ~0.5℃ temperature offsets between sockets, makeing it impossible to measure the real spread of the ETFs. Thus, in the latest version of PCB, the 1^{st} and 2^{nd} level buffers were removed and replaced by direct connections. However, the -3dB bandwidth of the entire readout chain is reduced to 8.6MHz because of the large value of the total on-capacitance of the 1^{st} and 2^{nd} level MUX (40 pF). For Q4S24 ETF, the phase shift is 230m° given Fdrive=35kHz, 10% spread of it will introduce temperature error of about 0.2°C before compensation.

In addition, to avoid picking up interference from outside, the lids of ceramic package chips are shorted to ground with wires. Without this, it was observed that the dual thermopile ETF suffers from significant heater/output crosstalk.

5.3 –Measurement results

5.3.1 – Phase characteristics

5.3.1.1 – Phase normalization

Phase normalization also was performed for 8 ETFs in test chip2 as shown in Fig 5.9. The phase shift of Ring ETF follows the Eq.3.2 very well over a wide frequency range.

The dual thermopile ETF has much less phase shift and exhibits non-linearity at low frequencies, this will be explained in the next section.

The effective 'S' and estimated 'Dsi' are listed in Table 5.2. Since the octagonal heater behaves more like an ideal point source as 'S' increases, the ratio between '$S_{effective}$' and 'S' is approaching unity as expected.

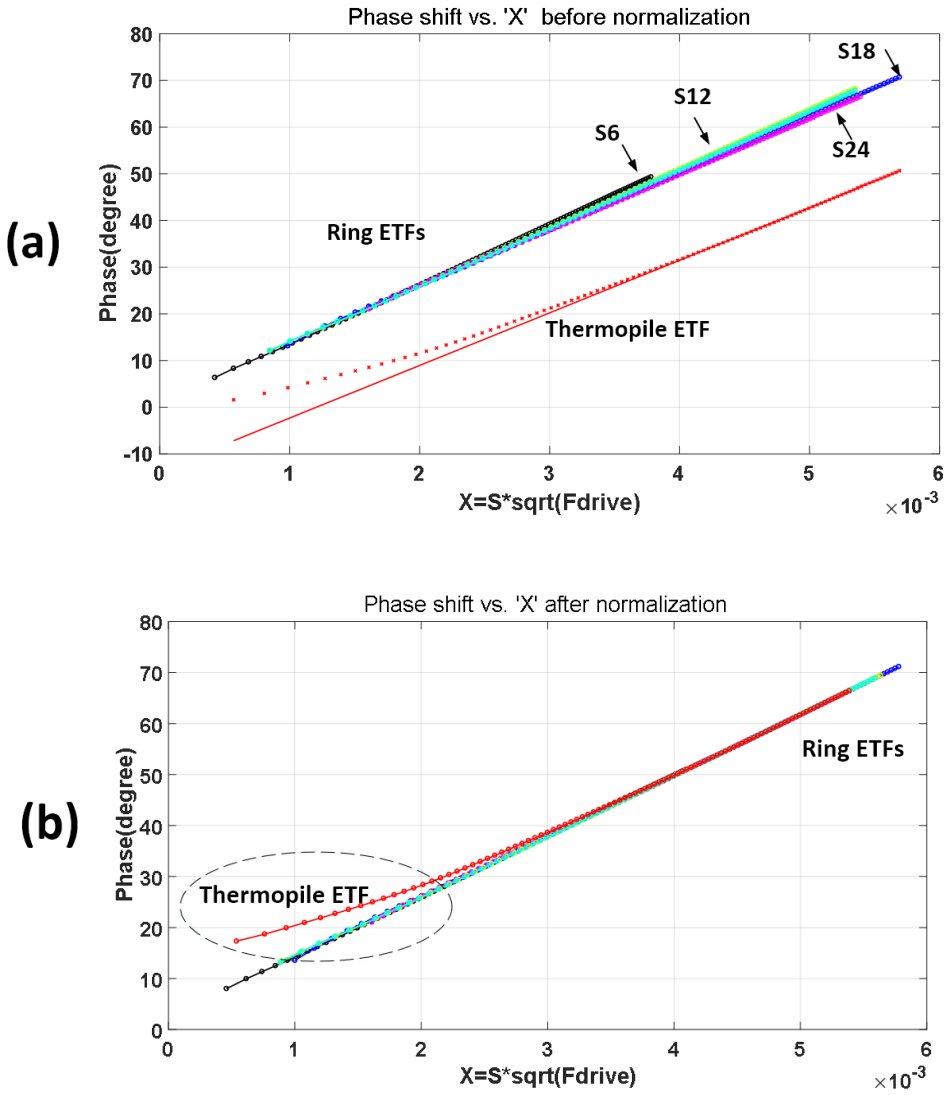


Figure 5.9 Phase normalization for test chip 2, before (a) and after (b) normalization

5.3.1.2 – Thermopile ETF model

In Fig.5.9, the normalized phase of the dual thermopile ETF exhibits some non-linearity at low frequencies, i.e. it no longer like a simple point source /point sensor ETF. This is because of the finite distance between the hot junctions and the cold junctions. To

understand this better, the phase response of each of the two junctions (S_{hot}=18μm , S_{cold}=26μm) was be modeled with ring ETF.

For example, the behaviour of cold junction is imitated by a S24 ring ETF, while the hot one is imitated by S18/S12/S6 ring ETFs. The thermal impedance of different junctions (hot/cold) in a thermopile ETF can be writtenas:

$$Zth_{hj} = \frac{Vsig_{hj} \times \exp(-i * phase_{hj})}{(BVDD/2) \times Tc \times P_{heater\_ring}} \tag{5.2}$$

$$Zth_{cj} = \frac{Vsig_{cj} \times \exp(-i * phase_{cj})}{(BVDD/2) \times Tc \times P_{heater\_ring}} \tag{5.3}$$

where $Vsig_{cj}$ ($Vsig_{hj}$) and $phase_{cj}$ ($phase_{hj}$) are the measured signal amplitude and the phase shift of S24 (S18/S12/S6) ring ETFs, respectively, Tc is the temperature coefficient of N+ diffusion resistor with silicide, P_{heater_ring} is the heater power of Q4S24 or Q4S18 ETF. The thermal impedance of the artificial thermopile ETF can be computed as follows:

$$Zth_{Tp\_module} = Zth_{hj} - Zth_{cj} \tag{5.4}$$

Thus, the phase of the thermopile ETF can be calculated and plotted as shown in Fig.5.10. The S18/S24 combination matches well with the measurement results.

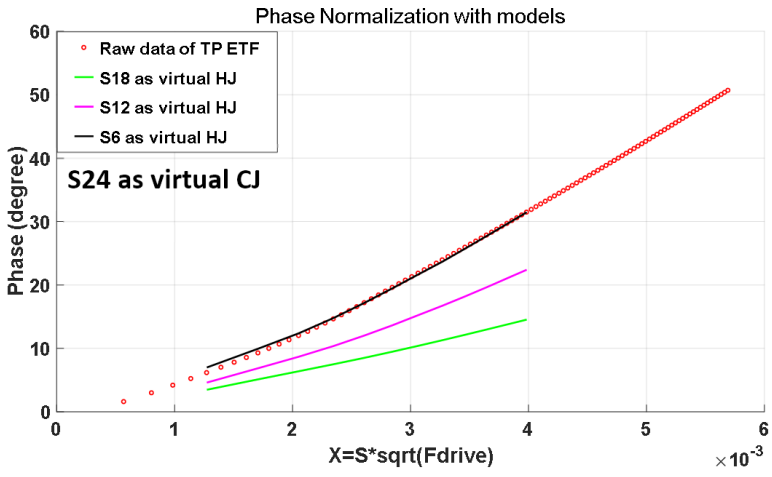


Figure 5.10 Use the output response of ring ETFs to model TP ETF

From Eq.2.6, combining with Zth_{Tp_module}, the Seebeck coefficient of the thermopile can also be estimated as follows:

$$S_{tc} = \frac{V_{sig\_TP}}{\left|Zth_{TP\_module}\right| \times P_{heater\_TP} \times N} \tag{5.5}$$

where V_{sig_TP} is the measured signal amplitude of dual thermopile ETF, P_{heater_TP} is the heater power, N is the number of thermocouples (16 in this case). The calculated Seebeck coefficient of the thermopile is 0.42mV/K, which matched well with the reported value (0.5mV/K) in [14].

5.3.2 – Resolution optimization

The resolution optimization was done for 8 ETFs in test chip2. Experiments were conducted at two temperature points: T1 (27℃) and T2 (35℃). The sensitivities are plotted in Fig. 5.11. Comparing to Fig. 4.13, a bigger temperature gap provides a more clear estimation of the optimal F_{drive}. An overview of the optimal driving frequencies and estimated resolutions in a bandwidth of 0.5Hz of 8 ETFs are provided in Table 5.2.

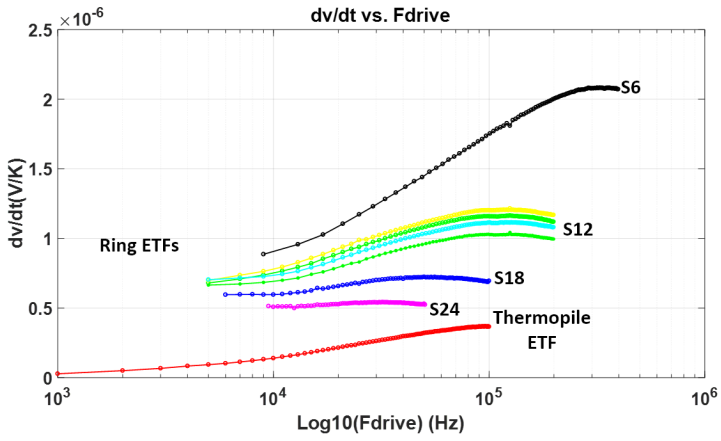


Figure.5.11 Fdrive optimization for 8 ETFs for test chip 2

5.3.3 – Untrimmed Accuracy

5.3.3.1 – Polynomial fit experiments

In this project, a phase output is provided by the LIA, and a polynomial curve fitting is needed to transfer this phase into temperature. In order to limit the impact of the fitting error on the system accuracy (targeted at 0.05℃), the fitting error should be sufficiently

low (~10mK). Higher-order fitting would lead to less error, but longer measurement time and complicated digital circuits are required. Therefore, a minimum polynomial order that meets the accuracy limit is preferred.

To investigate the minimum polynomial order, 5 devices were measured from 5℃ to 85 ℃ with a step of 5℃. Fig.5.12 shows that a 6th order polynomial fitting can guarantee a fitting error of 10mK. As a consequence, for the following accuracy measurements, all the ETFs were characterized at 7 temperature points.

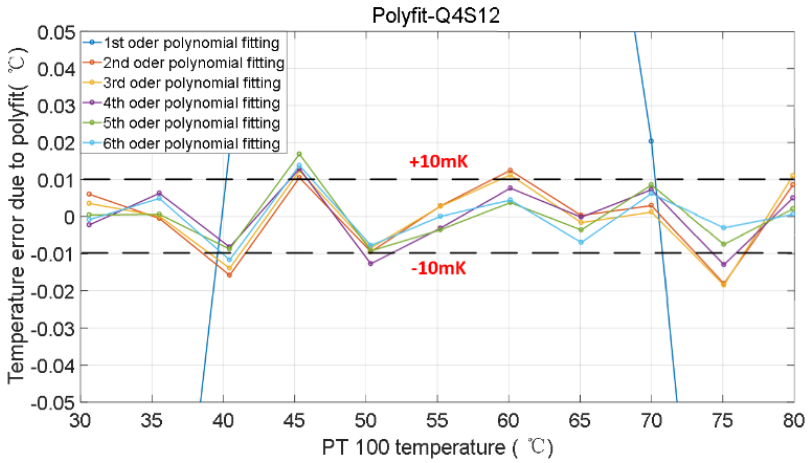
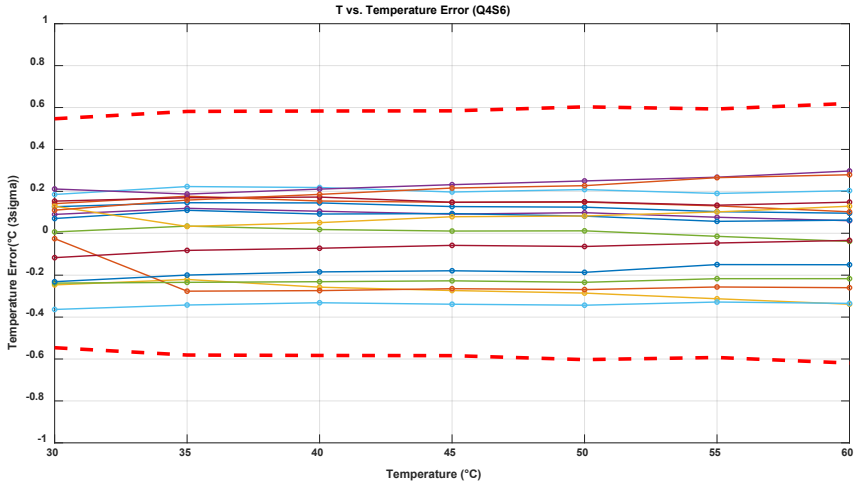


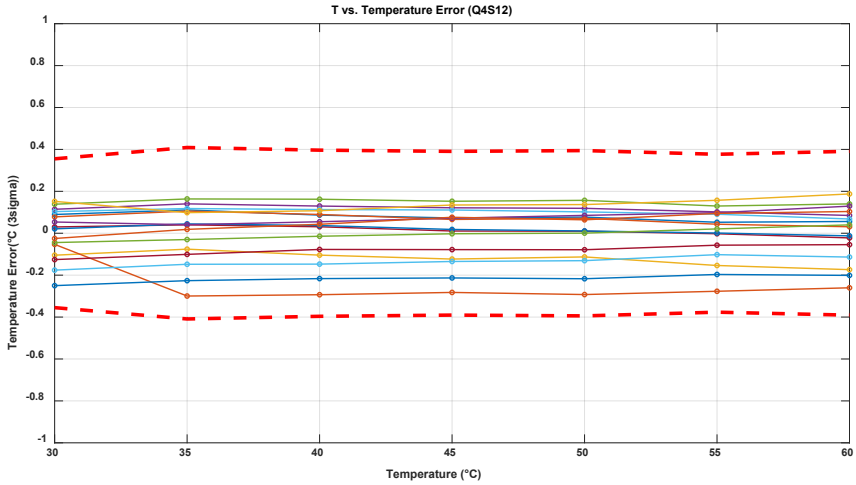
Figure 5.12 Polynomial curve fitting for Q4S12

5.3.3.2 – ETFs accuracy

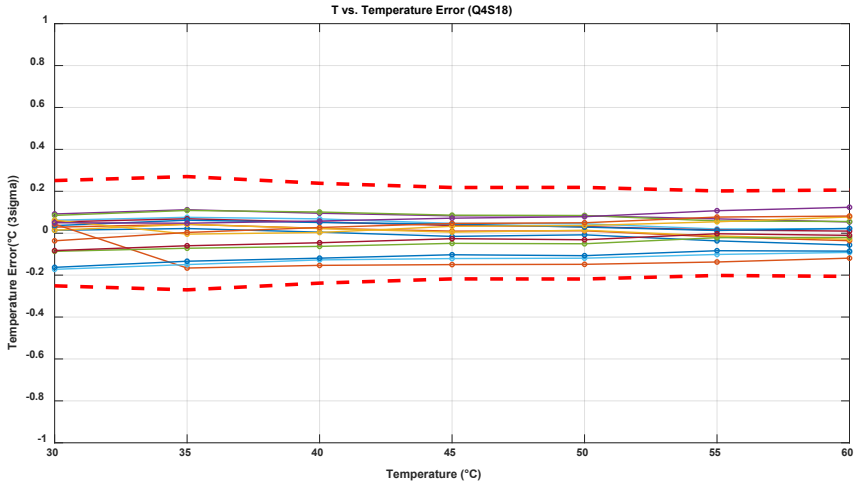
An essential step of these experiments is measuring the untrimmed device-to-device spread of 8 ETFs from 30℃ to 60℃ with a temperature step of 5°C. For all the ETFs, 16 devices with ceramic packages were measured in the same set-up. After polynomial fitting in MATLAB, the spread plots of 8 types of ETFs from a single batch are shown below, with red dash lines indicating the estimated ±3σ limits.



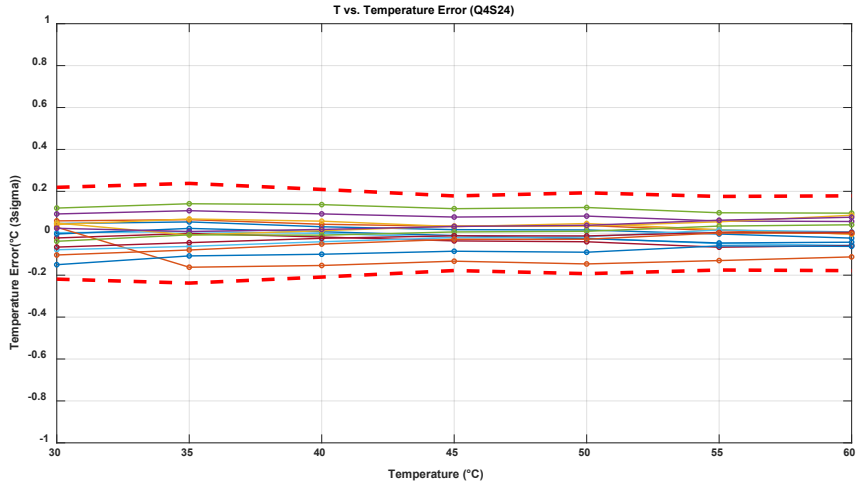
(a) Q4S6 ETF



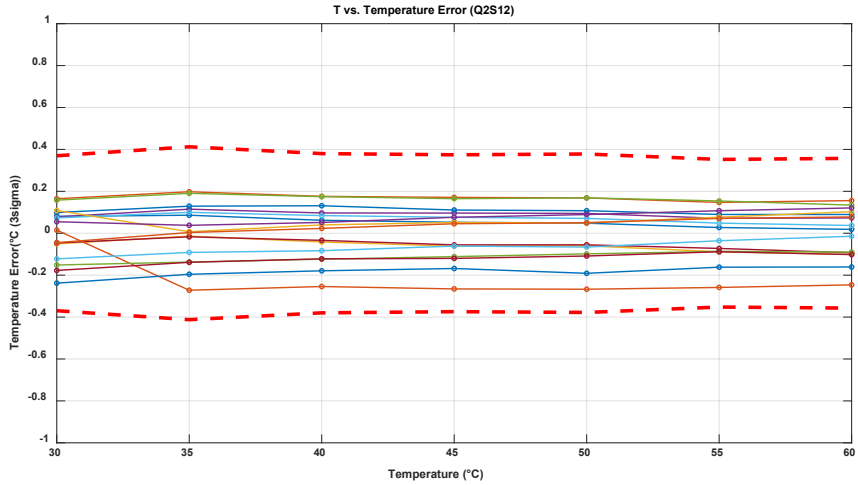
(b) Q4S12 ETF



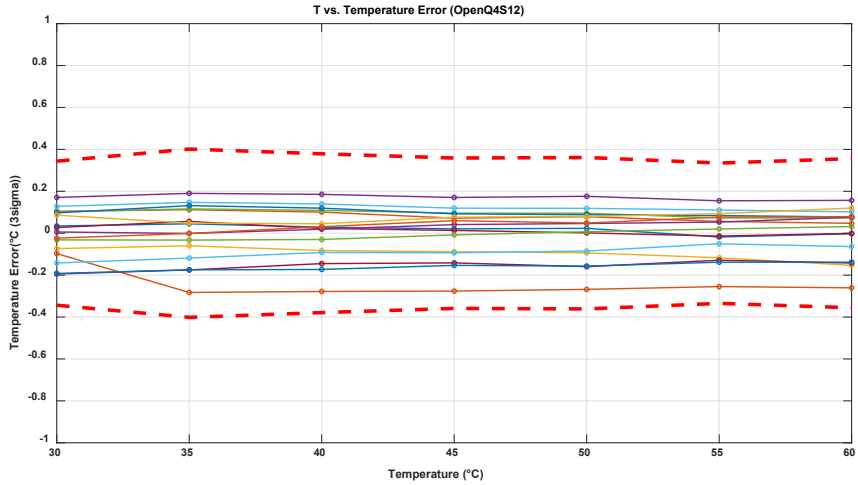
(c) Q4S18 ETF



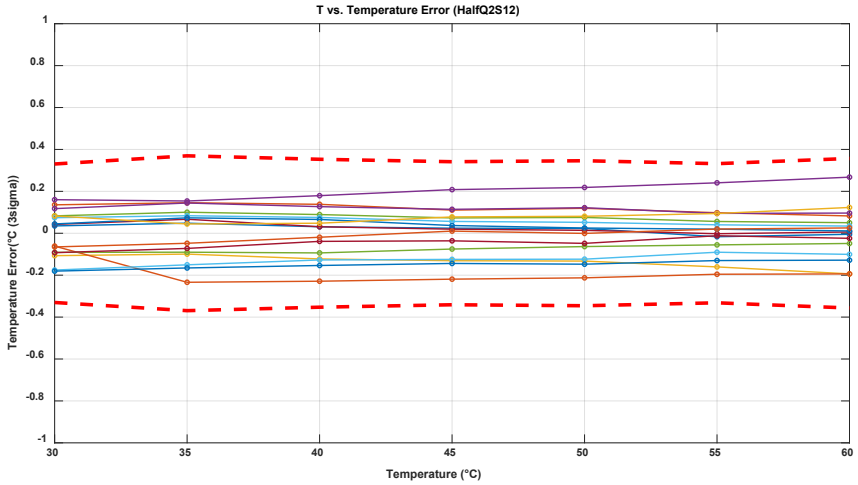
(d) Q4S24 ETF



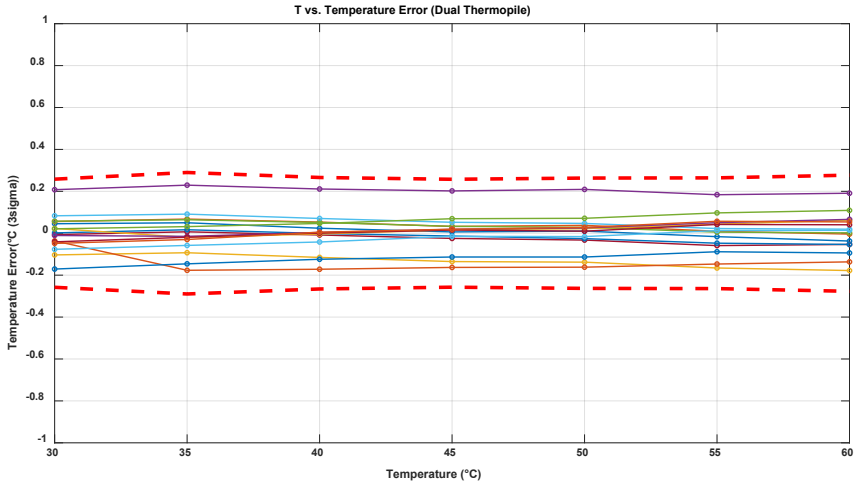
(e) Q2S12 ETF



(f) OpenS12 ETF



(h) HalfS12 ETF



(i) Dual thermopile S18 ETF

The results show that lithography is indeed the main error source of temperature in ring ETFs. The accuracy can be improved if 'S' increases. The Q4S24 ETF has the best accuracy of ±0.2℃(3σ) over 30℃ to 60℃ range, and the dual thermopile S18 ETF exhibits the same accuracy (±0.3℃(3σ)) as Q4S18 ETF.

S12 ETFs have almost the same untrimmed accuracies, indicating that the structures have no effect on the accuracy. However, for the sake of power efficiency, half-ring ETF and concentric-ring ETF are favorable in the future design.

5.3.3.3 – Wafer-to-wafer spread

In order to investigate the effects of wafer-to-wafer spread, two separate wafers were fabricated in a 180nm CMOS process from 2 wafer suppliers. 16 devices are from one wafer and the other 8 devices are from another one. For all the devices, the readout

circuitries are identical and they have the same nominal doping concentration and thickness. In total, 24 devices (Q4S24 ETF) were measured over a temperature range of 30℃ from 30℃ to 60℃. Fig 5.13 shows that the difference between the average errors of the two wafers is no more than ±0.1℃.

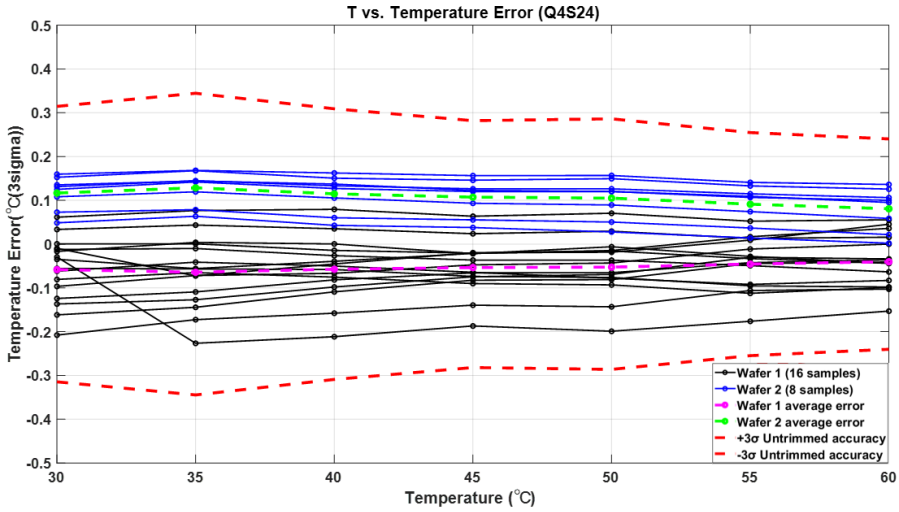
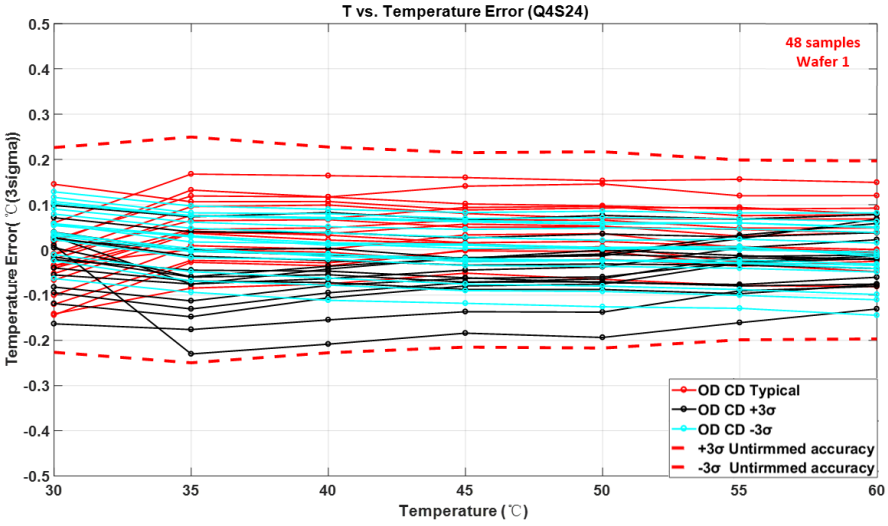


Figure 5.13 Wafer-to-wafer spread for the Q4S24 ring ETF in 180nm CMOS

5.3.3.4 – Batch-to-batch spread

To evaluate the effect of batch-to-batch spread, 72 devices were fabricated from 3 process slots with different critical dimensions (CD) of the active layer (OD). 48 devices are from wafer 1 and the other 24 devices are from wafer 2. The splits modify the width of active layer slightly, this alters the center position of heater and thermistors. The spread experiment was done for Q4S24 ETFs. As shown in Figure 5.14, it is good to see that the batch-to-batch spread is insignificant (offset < 0.2℃) and the intra-batch spread remained at ±0.2℃(3σ).

(a)



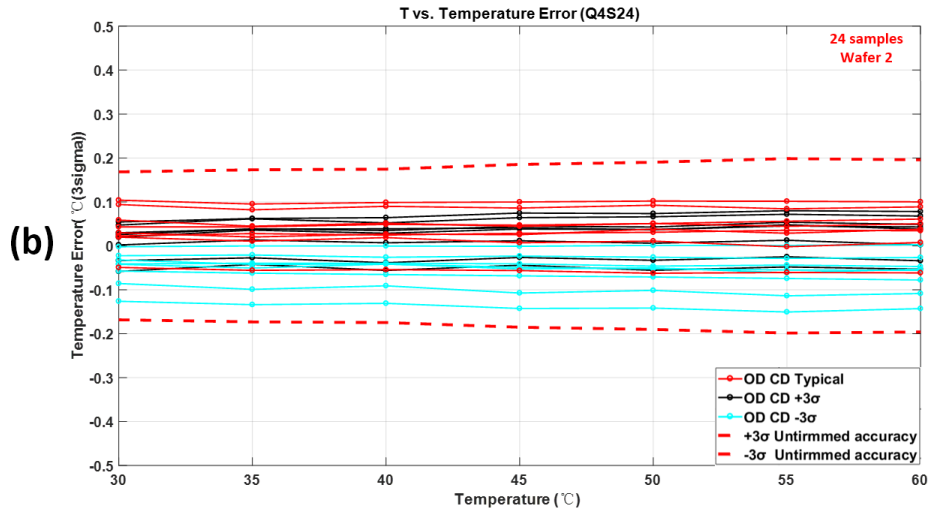


Figure 5.14 Measured batch-to-batch spread for Q4S24 ETFs (3 batches), 48 samples from wafer 1 (a) and 24 samples from wafer 2 (b)

5.3.3.5 – Mechanical stress

To study the effects of mechanical stress, 32 devices from a single wafer were packaged in both ceramic DIL and plastic packages. The plastic packages were fabricated using mold compound to seal, which will contract and exerts compressive stress onto the die as it cools down[14]. The below figures presents the temperature spread of 16 devices in plastic packages and the other 16 devices in ceramic packages, indicating that the ring ETFs are sensitive to mechanical stress.

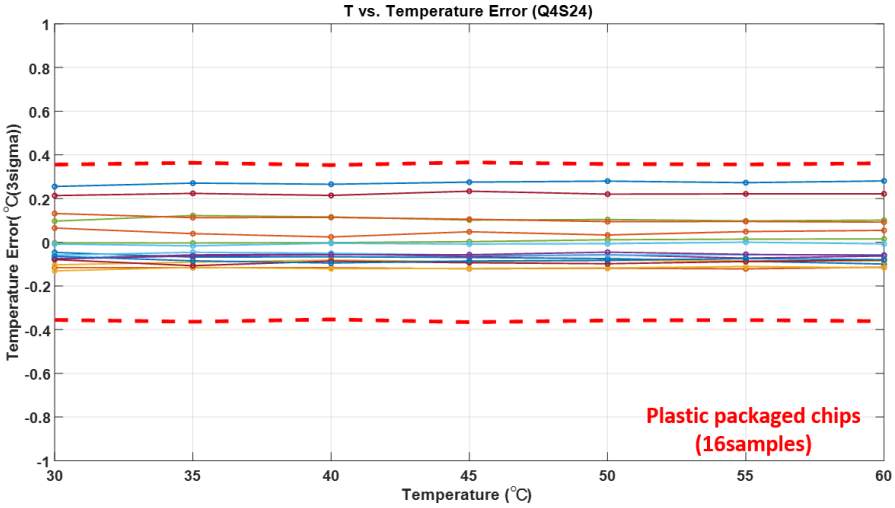


Figure 5.16 Device-to-device spread for Q4S24 ETF in plastic packaged chips

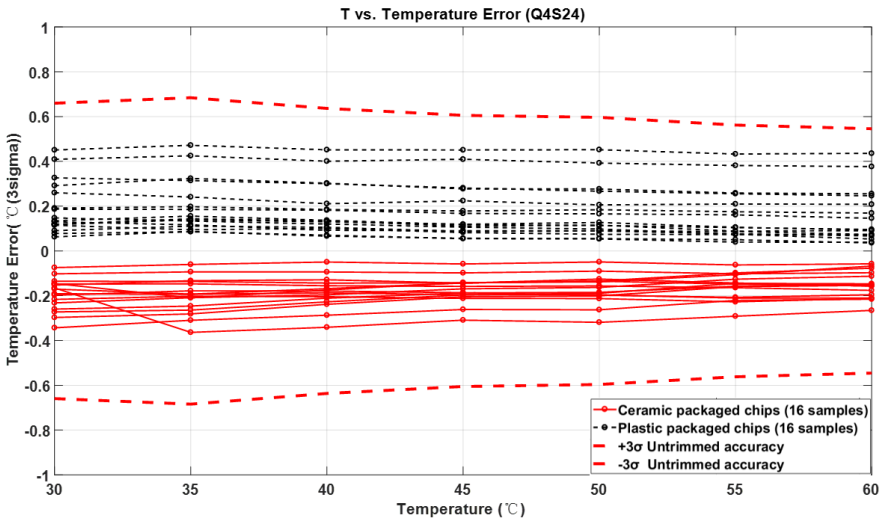


Figure 5.17 Measured device-to-device errors for devices in plastic and ceramic packages

Compared to the same ETF in ceramic packages, the 3σ limits based on the devices in plastic packages shows an increased spread of ±0.35℃(3σ). The systematic difference of temperature error between two packaged chips is ~0.4℃, and the plastic packaged chips have a mean positive error, indicating that they always overestimate the ambient temperature. The self-heating effect might be the reason for the slight increase in spread and the systematic difference since the nominal thermal resistance Zth of the plastic packages is about 100K/W, which is 2x higher than that of ceramic packages. The spread in Zth is higher thus increasing the device-to-device spread slightly.

5.4 –Summary table and analysis

5.4.1 –Summary table

Table-5.2 Summary of Ring ETFs in test chip 2

No.	ETF Type	'S' (μm)	Effective 'S' (μm)	Estimated 'Dsi' (cm^2/s)	Optimal 'Fdrive' (kHz)	Resolution (m℃rms)	Untrimmed accuracy (℃(3σ)) Ceramic Package	Untrimmed accuracy (℃(3σ)) Plastic Package
1	Full Ring	6	5.54	0.62	317	0.6	0.62	1.0
2	Full Ring	12	11.57	0.68	125	1.3	0.41	0.65
3	Full Ring	18	17.72	0.71	50	2.4	0.27	0.50
4	Full Ring	24	24 (ref)	0.73	32	3.6	0.20	0.35
5	Half Ring	12	11.45	0.66	125	1.6	0.37	0.45
6	Open Ring	12	11.54	0.67	125	2.5	0.40	0.60
7	Concentric Ring	12	11.38	0.66	125	1.2	0.41	0.64
8	Polygon	18	18.8	0.79	99	6.2	0.29	0.31

5.4.2 –Other error sources analysis

Apart from the lithography error, it is necessary to evaluate the effect of other error sources, like RC error and self-heating effect.

5.4.2.1 – RC error

Since the spread of R_{bridge}/ parasitic capacitance or on-chip delay will result in a phase-shift change in the test mode eventually, the phase spread in the test mode can be used to evaluate the RC error before compensation directly.

As shown in Figure 5.18, the phase spread in the test mode for Q4S24 ETF is 0.025°(3σ), indicating that the RC error is at ±0.2℃(3σ) level without auto-zeroing. Imperfect phase autozeroing will make the RC error be a dominant limitation in our measurements.

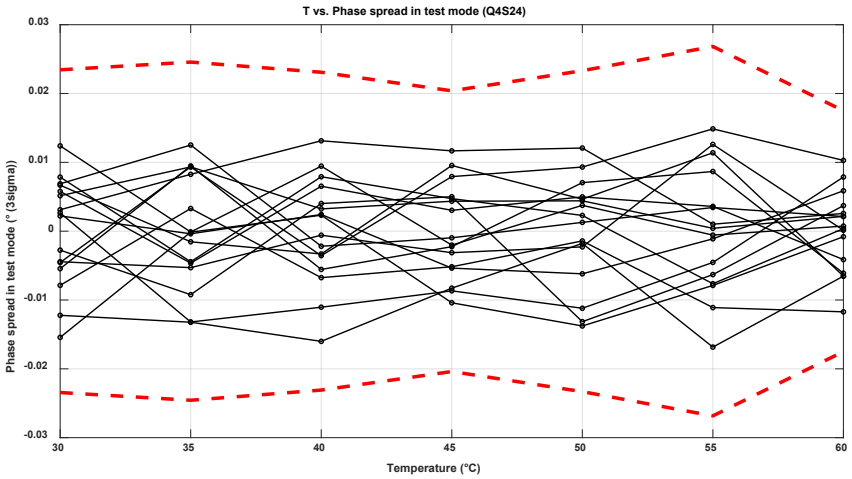


Figure 5.18 Phase spread in the test mode for Q4S24 ETF

5.4.2.2 – Self-heating effect

The spread of heater and bridge resistance will cause power variation thus self-heating spread. Experiments were done to measure the heater and bridge resistance of 16 samples. Figure 5.19 shows that the spread of R_{bridge} and R_{heater} are both less than 15Ω. For Q4S24 ETF, the averaged R_{bridge}=464Ω and the averaged R_{heater}=566Ω. Given 1.8V supplies, the calculated power variation is about 0.15mW. From Eq 2.10, the error due to power variation is 15m℃, which is negligible comparing to the measured error.

However, if the spread of $Z_{package}$ is also taken into consideration, the conclusion would be different. The total power consumption of Q4S24 ETF is 18mW, 10% spread of $Z_{package}$ would result in 0.1℃ temperature error.

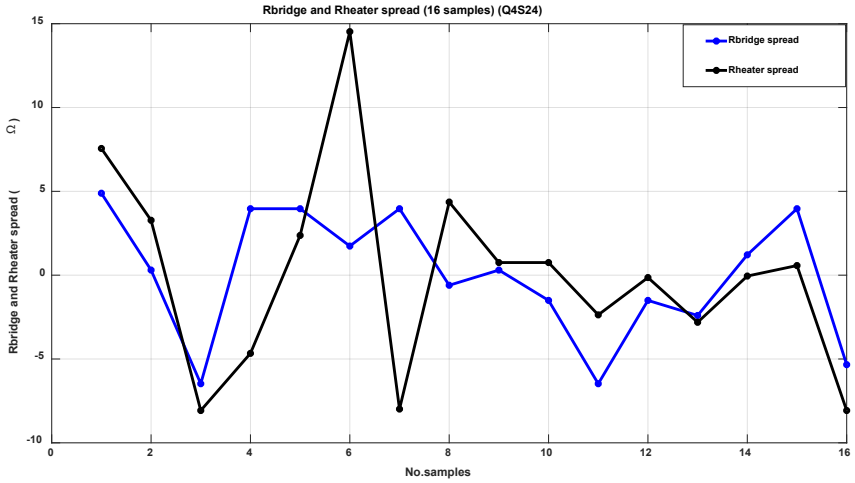


Figure 5.19 Rbridge and Rheater spread for Q4S24 ETF

5.5 –Summary

In this chapter, the chip details, measurement set-up and results of test chip 2 have been discussed. Comparing to test chip1, a newly introduced test mode compensates the RC delay of the readout chain and helps to reveal the real characters of ring ETFs. The measurement results show that ring ETFs have an untrimmed accuracy as good as thermopile ETFs but with 5x better resolution.

6 –Conclusion and Future work

6.1 –Conclusion

In this thesis, a new type of electrothermal filter (ETF) has been proposed and designed for no-trim temperature sensors. The electrothermal filter employs ring-shaped thermistors (N+ diffusion resistor with silicide) instead of thermopiles serves as the heat sensing elements, named ring ETF. Various structures of ring ETFs, including full-ring, half-ring, open-ring and concentric-ring have been proposed. To investigate their performance quickly, 8 ETFs with different 'S' and structures were implemented in two test chips.

For the ring ETF with 'S' =24μm, a temperature-sensing resolution of 3.6mK in a 1s conversion time can be achieved. To quantify the temperature sensing spread and accuracy, 16 samples have been measured over a small temperature range from 30℃ to 60℃. Without trimming, Q4S24 ring ETF achieved a 0.2℃ inaccuracy (3σ) while lithography error is still the dominant error source.

Comparing to traditional thermopile ETF, ring ETFs based TD sensors with the same 'S' have similar untrimmed accuracy but 5x better resolution. These results imply that if 'S' keeps increasing, this new type of ETF can be used in no-trim CMOS-compatible temperature sensors and achieve higher accuracy in the future.

6.2 –Future work

To suppress the delay-oriented error from interconnections (mainly off-chip RC constants), a phase auto-zeroing technique is used when characterizing the test chip 2. Despite the added complexity, however, the performance is not guaranteed.

This problem can be solved by using on-chip readout circuits, like a phase-domain sigma-delta modulator [13]. Since all interconnections would be on-chip, delay-oriented errors can be suppressed dramatically.

Fig.6.1 shows the block diagram of an ETF readout circuit. According to [13], a -3dB-bandwidth of 800MHz is achievable for the gm stage. The resulting phase error is less than 3m° at f_{drive}=42KHz, and the temperature error is less than 0.02°C.

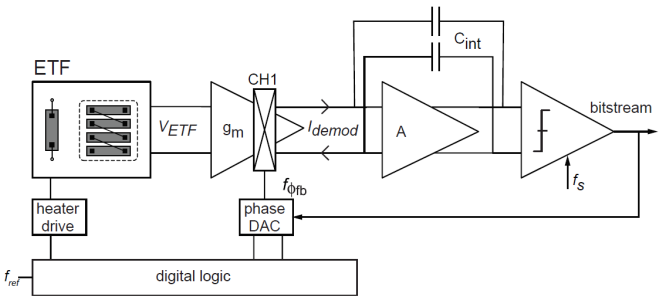


Figure 6.1 Block diagram of an ETF readout by a PD$\Sigma\Delta$M [13]

Acknowledgements

There are many people without whom this thesis would not have come into existence. I would like to dedicate my sincere gratitude to all of those who helped and supported me during the past academic year.

My first thanks go to my supervisor, Professor Kofi Makinwa, for offering me the opportunity to take responsibility for this 'golden' project. His unfaltering guidance and insightful ideas helped me a lot when I was lost and suffering during measurements. In this group, I taped out the first chip in my life. Despite some silly mistakes I made, he kept encouraging me and gave me a second chance to continue my project, so that I could continue learning from him.

I am also very grateful to Sining Pan, who offered me many valuable suggestions on doing circuit design, presenting ideas and writing essays. His guidance and experience helped me a lot and I wish him great success in his academic career.

I would like to thank people in ADI for offering me so much help. Both the FIBed chips and the test chip2 from ADI are extermely important to study this new type of ETF.

I would also like to thank people in the EI lab. Thanks go to Miao, Matheus, Jan, Cagri, Efraïm, Xianglong, Shardul, for their friendship and kindly answering all types of questions. I would like to thank Zu-yao, Lukasz, Ron, for chip-bonding, PCB designing, and instrument maintaining; and our secretary Joyce for all her support.

Finally, I would like to thank my parents, who always stand by my side and support me in the last 24 years.

Reference

[1] A. Bakker, "CMOS smart temperature sensors-an overview." pp. 1423-1427.

[2] A. Heidary *et al.*, "12.8 A BJT-based CMOS temperature sensor with a 3.6 pJ· K 2-resolution FoM." pp. 224-225.

[3] A. L. Aita *et al.*, "A CMOS smart temperature sensor with a batch-calibrated inaccuracy of±0.25 C (3σ) from− 70 C to 130 C." pp. 342-343,343 a.

[4] K. Souri *et al.*, "A precision DTMOST-based temperature sensor." pp. 279-282.

[5] S. Pan *et al.*, “A Resistor-Based Temperature Sensor With a 0.13 pJ $\cdot $ K2 Resolution FoM,” vol. 53, no. 1, pp. 164-173, 2017.

[6] S. Pan, and K. A. Makinwa, "A Wheatstone Bridge Temperature Sensor with a Resolution FoM of 20fJ. K2." pp. 186-188.

[7] C. van Vroonhoven, and K. Makinwa, "Thermal diffusivity sensors for wide-range temperature sensing." pp. 764-767.

[8] C. P. van Vroonhoven, D. d'Aquino, and K. A. Makinwa, "A thermal-diffusivity-based temperature sensor with an untrimmed inaccuracy of±0.2° c (3s) from− 55° c to 125° c." pp. 314-315.

[9] A. L. Aita, “Low-power high-accuracy smart temperature sensors in CMOS technology,” 2011.

[10] M. A. Pertijs, and J. Huijsing, *Precision temperature sensors in CMOS technology*: Springer Science & Business Media, 2006.

[11] B. Yousefzadeh, and K. A. Makinwa, "9.3 A BJT-based temperature sensor with a packaging-robust inaccuracy of±0.3° C (3σ) from− 55° C to+ 125° C after heater-assisted voltage calibration." pp. 162-163.

[12] M. A. Pertijs, K. A. Makinwa, and J. H. J. I. J. S.-S. C. Huijsing, “A CMOS smart temperature sensor with a 3 inaccuracy of±0.1 C from− 55 C to 125 C,” vol. 40, no. 12, pp. 2805-2815, 2005.

[13] K. Souri, Y. Chae, and K. A. J. I. J. o. S.-S. C. Makinwa, “A CMOS Temperature Sensor With a Voltage-Calibrated Inaccuracy of $\pm 0.15^{\circ} $ C (3$\sigma $) From $-$55$^{\circ} $ C to 125$^{\circ} $ C,” vol. 48, no. 1, pp. 292-301, 2012.

[14] C. Van Vroonhoven, “Integrated Temperature Sensors based on Heat Diffusion,” 2015.

[15] U. Sönmez, F. Sebastiano, and K. A. Makinwa, “Compact thermal-diffusivity-based temperature sensors in 40-nm CMOS for SoC thermal monitoring,” *IEEE Journal of Solid-State Circuits,* vol. 52, no. 3, pp. 834-843, 2017.

[16] S. Pan *et al.*, "10.3 A 0.12mm2 Wien-Bridge Temperature Sensor with 0.1°C (3σ) Inaccuracy from -40°C to 180°C." pp. 184-186.

[17] Y. S. Touloukian *et al.*, *Thermophysical Properties of Matter-The TPRC Data Series. Volume 10. Thermal Diffusivity*, Thermophysical and Electronic Properties Information Analysis Center …, 1974.

[18] A. W. van Herwaarden, “Thermal vacuum sensors based on integrated silicon thermopiles,” 1989.

[19] K. Souri *et al.*, "A 0.85 V 600nW all-CMOS temperature sensor with an inaccuracy of $+/-0.4 mathrm {C}(3mathrm {s}) $ from-40 to 125 C." pp. 222-223.

[20] S. Pan *et al.*, “A Resistor-Based Temperature Sensor With a 0.13 pJ $\cdot $ K2 Resolution FoM,” *IEEE Journal of Solid-State Circuits,* vol. 53, no. 1, pp. 164-173, 2017.

[21] M. Holland, “Analysis of lattice thermal conductivity,” *Physical Review,* vol. 132, no. 6, pp. 2461, 1963.

[22] J. Barber, “The conduction of heat from sliding solids,” *International Journal of Heat and Mass Transfer,* vol. 13, no. 5, pp. 857-869, 1970.
[23] Ü. Sönmez, “Compact thermal-diffusivity-based temperature sensors for SoC thermal monitoring,” *Unpublished Ph.D. Thesis, Department of Political Science and Public Administration, Delft University of Technology*, 2019.
[24] S. M. Kashmiri, S. Xia, and K. A. Makinwa, “A temperature-to-digital converter based on an optimized electrothermal filter,” *IEEE Journal of Solid-State Circuits,* vol. 44, no. 7, pp. 2026-2035, 2009.
[25] "Package information," Sept.18th, 2019; http://www.bitsonchips.com/wp-content/uploads/2017/07/ref42.pdf.
[26] R. Quan *et al.*, "27.8 A 4600μm 2 1.5° C (3σ) 0.9 kS/s thermal-diffusivity temperature sensor with VCO-based readout." pp. 1-3.
[27] S. Pan, “A High-Resolution Energy-Efficient Resistor-Based Temperature Sensor,” 2016.