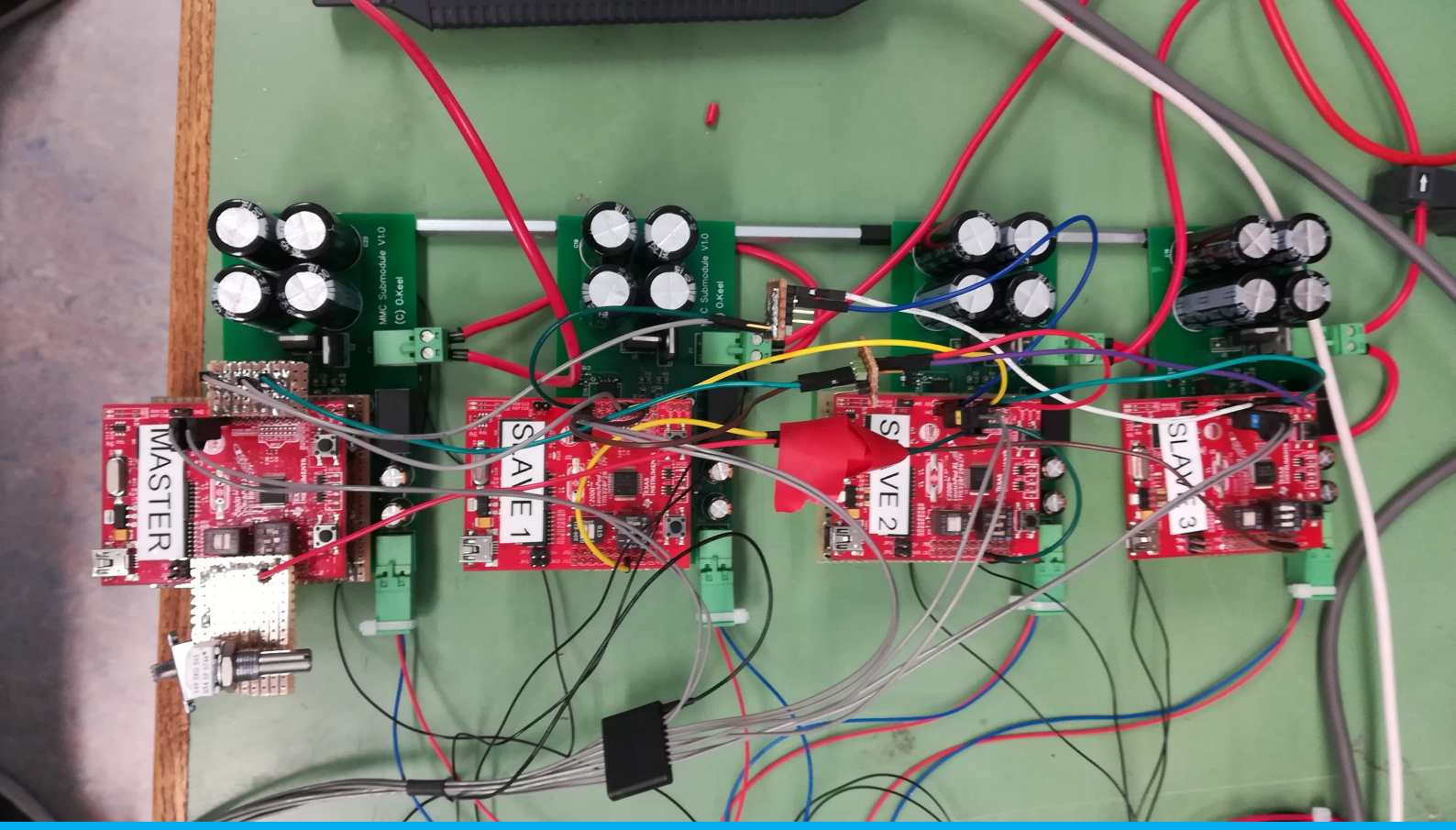


# Modular Multilevel Converter

## Introduction of a low level communication bus for distributed control

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TU Delft

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## Introduction of a low level communication bus for distributed control

by

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TU Delft

# Preface

The last 8 month were invested into this thesis with the goal of achieving my master degree in sustainable energy technology. This would have not been possible with the support of many. First of all I want to thank my father which introduced me into engineer from my early childhood. He always supported my projects with constructive inputs and financially funding. As well I want to thank my mother even though it still difficult for her to understand what I am actually doing with electricity. I also want to thank my girlfriend which supported me every second during my two years studying abroad. Even though it was not an easy time for our relationship she was always willing to help were she could.
My Interests in propulsion technology started with my electric motorcycle built and introduced me to good people which helped me along the way. Two of the persons which made this thesis possible are Martin Stöck and Katja Stengert from Thyssen Krupp. Their constructive inputs leaded me to the actual research topic. As this thesis topic was proposed by myself it required someone who trusted in my capabilities. Therefore I want to thank Professor Ferreira which made this possible for me. He gave me the freedom to design this thesis which made it possible to learn a lot. Moreover I want to thank to Mladen Gagic, my weekly supervisor. He gave me good concrete input and feedback to my problems. He also introduced me to Ilija which helped me with setting up the embedded control correctly. Additionally I want to thank Professor Teodorescu from Aalborg University for his time he took off for me. I want to thank for the interesting conversation about the MMC technology and his willingness to help me. Lastly I want to thank to the magnificent lab assistants of the DCES group, especially Joris and Bart. Without your daily support and investment of your own time I would not have been able to finish this thesis in time. You were always up for a good talk and helped me with the frustration of programming with Simulink.

*O.Keel*
*Delft, June 2018*

# Abstract

The transportation industry is causing 14% of the worldwide greenhouse gas emission. Therefore, the United Nation concluded with the Paris climate agreement to reduce and limit their emissions to keep the global average temperature increase below 2 degrees Celsius. Based on the agreement the European union introduced new regulations to limit the average fleet emission of car companies. In this push towards lowering emission the companies introduced their first generations of electric cars. To further improve the efficiency of the electric drive train new multilevel topologies were introduced. One of the topologies is called modular multilevel converter (MMC) introduced by R. Marquardt and A. Llesnicar in 2003. This new topology main advantage are its modularity and the option to use low voltage component. However, no company industrialized the MMC for drive train application. The reason therefore are the extensive control architecture, hardware and software wise. This thesis investigated possible ways to reduce the wiring and complexity by introducing a low level communication bus together with distributing the control to remove the centralized architecture. Therefore, the different possible low level communication bus were analysed and compared. The different bus protocols were compared based on speed and time to send the same amount of information to control a MMC. It was concluded that the serial peripheral interface bus (SPI) shows the highest capability for the proposed single phase 5 level converter set-up. Therefore, an experimental system was built to validate the performance. The system itself was designed with the goal to use low cost and low voltage component. The validation of the experimental set-up showed the stable operation of the system with an open loop control. Thereby it proofs the possibility to integrate and control the MMC with a low level communication bus. The results can be used as a baseline to further research on integrating the MMC and make it viable for drive train applications.

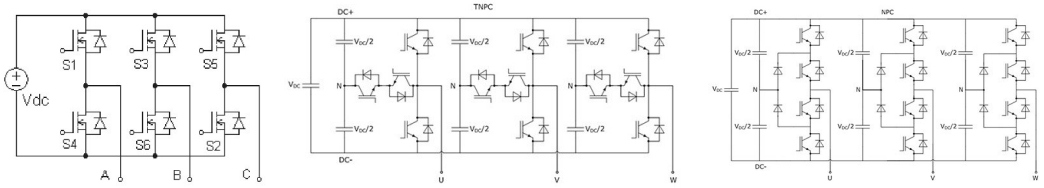
# List of notations

| | |
|---|---|
| MMC | Modular multilevel converter |
| PWM | Pulse width modulation |
| HVDC | High voltage direct current |
| NPC | Neutral point clamped |
| TNPC | T-type neutral point clamped |
| FLC | Flying capacitor |
| IEEE | Institute of electrical and electronics engineers |
| PD | Phase disposition |
| PSC | Phase shifted |
| NLC | Nearest level control |
| ATB | Average tolerance band |
| CTB | Cell tolerance band |
| $\mu C$ | Microcontroller |
| FPGA | Field programmable gate array |
| I/O | Inputs and Outputs |
| DSP | Digital signal processor |
| CAN | Control area network |
| I2C | Inter-integrated circuit |
| SPI | Serial peripheral interface |
| UART | Universal asynchronous receiver transmitter |
| MOSFET | Metal-oxide-semiconductor field-effect transistor |
| $I_{up}$ | Upper arm current |
| $I_{low}$ | Lower arm current |
| $I_{ac}$ | AC output current |
| $I_{circ}$ | Circulating current |
| $U_{up}$ | Upper arm voltage |
| $U_{low}$ | Lower arm voltage |
| $U_{dc}$ | DC bus voltage |
| $U_{ac}$ | AC output voltage |
| $U_{Rua}$ | Voltage drop over upper arm resistance |
| $U_{Rla}$ | Voltage drop over lower arm resistance |
| $U_{Lua}$ | Voltage drop over upper arm inductor |
| $U_{Lua}$ | Voltage drop over lower arm inductor |
| $L$ | Inductance |
| $R$ | Resistance |
| $P_{up}$ | Power upper arm |
| $P_{low}$ | Power lower arm |
| $P_{\Sigma}$ | Sum upper and lower power |
| $P_{\Delta}$ | Difference of upper and lower power |
| $EMI$ | Electromagnetic interference |
| HV | High voltage |
| LV | Low voltage |
| PCB | Printed circuit board |

# Contents

# 1 Introduction

The united nations decided in the Paris climate accord to reduce their green house gas emission to limit the increase of the global average temperature below 2°C [5]. Based on the agreement the European union has implemented regulations for the CO2 per kilometre for all kind of transportation. In case of cars the regulation limits the car company's fleet average to 95 grams of CO2 per kilometre [7]. This means a fuel consumption of around 4.1 litres per 100 kilometres for petrol and 3.6 litres per 100 kilometres for diesel cars. This goal can be achieved by electrifying the power train. The electric drive train consist of the inverter, which inverts the DC current into AC current and an electric motor. The first generation of electric car drives use two level converter together with electric motors which are designed in a speed range up to 15'000 revolutions per minute and a relative high pole pair number between 3-6. This results in a high electrical frequency at the inverter outlet. The inverter therefore needs to maintain a high PWM frequency (>8kHz) for low harmonics and good current signal quality. The result is high switching losses and additional losses in the motor from the harmonics in the current[45]. Not only does the high PWM frequency lead to losses at the same time the motor insulation is stressed because of the high dV/dt value. Depending on the application and the DC bus voltage, a higher insulation rating is required or a dV/dt filter which contributes to further losses and cost [45].




(a) 2 level (b) 3 level TNPC (c) 3 level NPC

Figure 1.1: 2 and 3 level topologies by Semikron

The alternative is to implement higher level power electronic topologies. Already adopted topologies are with 3 and 5 level. The 3 level topologies are used for drives [1] and grid inverter in the low voltage range, whereas the 5 level topologies are used in medium voltage application [4].

In 2003 A. Lesnicar and R. Marquardt introduced the idea of a modular multilevel converter (MMC) for a wide power range [33]. The electric power generation and transmission industry as well as various research institutions have investigated and developed working prototypes mainly for the high-power application alike high voltage DC (HVDC) transmission. Siemens [3] and ABB [2] sell commercialized versions of their MMC prototypes. The newly introduced MMC topology opens further improvement with the additional levels and the opportunity to use low voltage power components. The disadvantage is the control complexity which increases with rising numbers of levels. Therefore the MMC has not been developed to a commercially available inverter for drive system.

## 1.1. Structure

The introduction gave a short problem statement of the MMC topology and their application in motor drive application. The second chapter first gives an overview on the MMC topology in comparison to existing multilevel topologies. Specifically it shows that the number of components are similar. Based on that result it was decided to conduct a literature study on the state of research of MMC control system. The literature study in chapter 3 shows an overview on the control related topics and their implementation. Together the second and third chapter built the basis for the construction of the research question. Even though the research question was defined later in the timeline of this thesis it was put into the introduction. This should avoid confusion resulting from the deviation of the typical research report structure. Chapter 6 and 7 show the design, implementation and validation of the system. The last chapter number 8 gives a the answer to the research question and concludes this report with further research recommendation.

## 1.2. Research question

This section contains the main and sub research questions. Those questions result from the the state of technology analysis in chapter two together with the literature study presented in chapter three. Chapter two compared the MMC on a quantitative base and came to the conclusion that the number of required power electronic components at the same level number is equal or higher for non MMC topologies. Therefore the higher cost and complexity of the MMC results from the control architecture and auxiliary supplies. This thesis focuses on reducing the complexity of the control architecture. Chapter three therefore presents a literature study on the field of control architecture. In conclusion that the research conducted to reduce the complexity can be divided into two domains. First domain contains the control software implementation to reduce the amount of sensors or unfavourable operation mode whereas the second domain involves the physical implementation of the control architecture. The literature study shows that little research was conducted to integrate functions and by that reduce the volume. Therefore it proposes to look into low level communication bus protocols to distribute the control messages. Present MMC implementation mostly use a central controller with a communication link in form a of an optic fibre to every submodule. The advantage of using an an communication bus is to reduce the amount and length of the connection, moreover economical copper connection could be used. Further could the bus be used to distribute the processing power between the different master and slave controller. Therefore the following questions resulted:

- Which low level communication bus qualifies for the application in a MMC?

Low level communication buses have limitation depending on what application their are used for. Therefore it gives also a limitation to the MMC system size.

- What are the limitations of those low level communication bus?

The diversity of communication buses were implemented with different objectives. Therefore they have limitations in speed, hardware configuration or robustness. In case of an MMC those limitation have to be found to select the right communication bus for the application.

- What are the advantage of using a low level communication protocol?

Many DSP and $\mu C$ have integrated low level communication bus hardware. Low level communication buses are standardized and well studied platforms for serial communication with a low number of I/O. If they can be used instead of optic fibre or Ethercat, it results in a reduction of cost and complexity of the system.

- Can distributed control be implemented with a low level communication bus ?

Distributed control in MMC application shifts part of the control processing to the submodule. The advantage of distributed control is the reduction of I/O and processing power of the master and slave hardware. Existing distributed control implementation use higher level communication bus like Ethercat or optic fibres which make them more expensive than with low level communication buses.

- Do low level protocol contribute to a higher integration of an MMC?

Industrial MMC are built mainly for HVDC application for which the size and weight of the system is not a concern. For automotive application the MMC hardware needs to be integrated into small compartments and requires to be light weight to be viable for the industry.

As the structure of the report is explained in the former section the following will give an detailed overview of the time line for better understanding.

## 1.3. Plan of action

A timetable was set up with a rough planning for the time span of 8 months. The table 1.1 shows the operational step for every four weeks. The detailed planning was done weekly based on milestones decision during the implementation. The first six week of the thesis was used for the literature study. For this thesis it was decided to take a simulation, design and validation approach. This method consists of the three named parts. The first "simulation" part replicates the solution to the research question in a simulation model. This keeps the risks and investment of time low and can uncover flaws in the solution. Thereafter in the "design" step a system is built to test the solution in hardware. The designed hardware should be as simple as possible to answer mainly the research question and not open up other questions or problems. During the last "validation" step the simulated solution in step one are reproduced and compared. This step validates if the simulations are correct.

| Weeks | Month | Operation step |
|---|---|---|
| 1 | November | Literatur study & Simunlink model implementation |
| 2 | | Literatur study & Simunlink model implementation |
| 3 | | Literatur study & Simunlink model implementation |
| 4 | December | Literatur study & Simunlink model implementation |
| 5 | | Literatur study & Simunlink model implementation |
| 6 | | Literatur study & Simunlink model implementation |
| 7 | | Design submodule, component selection |
| 8 | January | Design submodule, component selection |
| 9 | | Manufacturing submodule |
| 10 | | Manufacturing submodule |
| 11 | | Comissioning Submodule |
| 12 | February | Comissioning Submodule |
| 13 | | Comissioning Submodule |
| 14 | | Comissioning Submodule |
| 15 | | Implementation of control architecture |
| 16 | March | Implementation of control architecture |
| 17 | | Implementation of control architecture |
| 18 | | Comissioning of single phase MMC open loop |
| 19 | | Comissioning of single phase MMC open loop |
| 20 | April | Design of experiment |
| 21 | | Design of experiment |
| 22 | | Execution of experiment |
| 23 | | Execution of experiment |
| 24 | Mai | Execution of experiment |
| 25 | | Validation of experiment |
| 26 | | Validation of experiment |
| 27 | | Report writing |
| 28 | June | Report writing |
| 29 | | Report writing |
| 30 | | Report writing |
| 31 | | Preperation for defense |
| 32 | July | Defense of thesis |

Table 1.1: Research plan

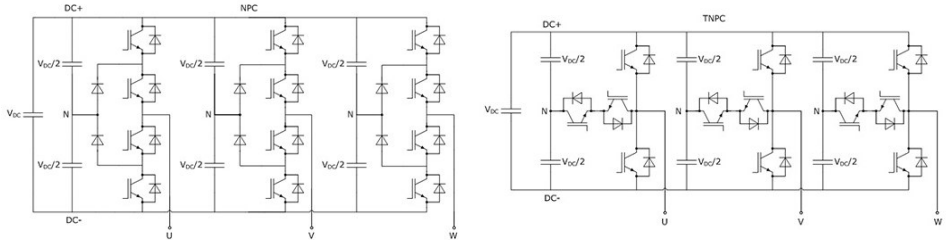
# 2

# Multilevel power electronic converter topologies and the modular multilevel converter

This chapter introduces common multilevel topologies and compares them to the modular multilevel topology (MMC). The working principles for each topology will be shortly introduced. The comparison is based on the quantity of components required to design the topologies as well as the specification of the implemented components. Those are countable quantities and make a comparison simpler. Hence, the results of the comparison are independent of manufacturer and component design. The independence of manufacturer and component design has the advantage that no cost comparison had to be made. A cost analysis is difficult as price varies with supply, demand and quantity. Generally it can be said that with higher market quantity of a component the lower the per unit prices is. Moreover it will not be looked into the control strategy as there are many ways to solve similar control problems. At the end of the comparison is a conclusion which will introduce the next step towards the research question.

## 2.1. Description and working principles of common multilevel topologies

Well known multilevel topologies are neutral point clamped (NPC), T-type neutral point clamped (TNPC) and flying capacitor (FLC). All of them can be set up in a 3 or 5 level topology. The introduction into these topologies will only be done for three level topologies, the five level and higher topology works with the same principle. In a first step the TNPC and NPC will be described and the working principle will be explained.




(a) three level NPC topology

(b) three level TNPC topology

Figure 2.1: Topologies which use capacitors clamped to the DC bus to generated levels in between

The TNPC and NPC work similar, both have a neutral point between DC+ and DC-. The neutral point is generated by two series capacitors. The difference is that the NPC uses two upper and lower switches which are connected with passive diodes to the neutral point. The TNPC implement anti parallel switches to the neutral point and only one two switches to connect to the DC bus. The three levels are generated by connecting the

output either to DC+, neutral or DC-. The difference between the two topologies are the possible commutation paths between switching stages and amount of semiconductors. Apart of that they both have similar working principle.

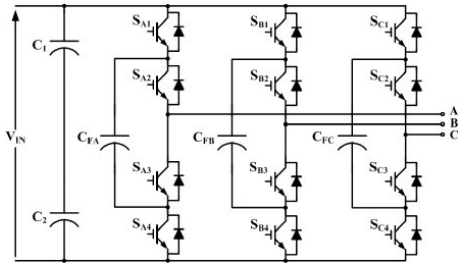
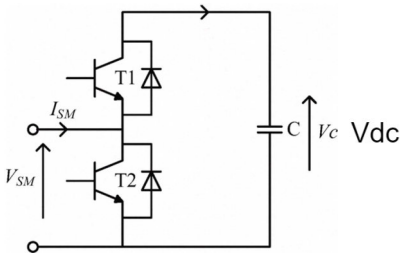



Figure 2.2: 3 level FLC inverter

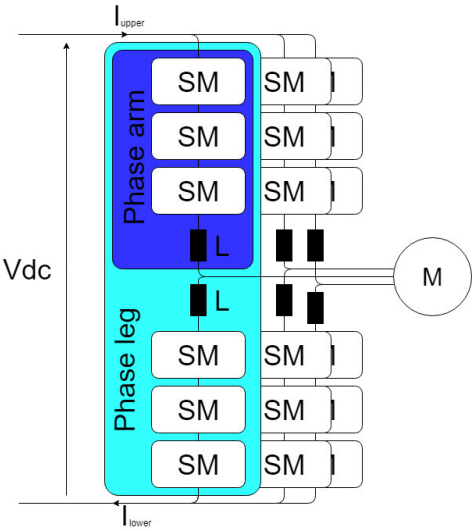
The FLC has a different approach to generate the third level. Instead of implementing a neutral point with two capacitors in series it uses a "flying" capacitor. The arrangement of the semiconductor is similar to the NPC but instead of clamping trough diodes to the neutral points it uses a capacitor connected to the same point. The capacitor needs to be precharged before operation of the inverter. During the operation the capacitor is used in series with the DC+ or DC- to create a neutral point. Crucial for operation of this topology is the voltage control of the flying capacitor.

## 2.2. Description and working principles of the MMC

The modular multilevel converter (MMC) uses a different approach to generate the multilevel output voltage. The smallest unit of a MMC is called a submodule and most often consist of a half bridge which is connected to a capacitor. The submodule represents the origin of the name modular multilevel converter. Figure 2.3a shows the schematic of the subdmodule. The voltage Vc represents the voltage of the capacitor. The voltage Vsm depends on the switching state and current flow direction. For the in figure 2.3a shown implementation of the submodule four different states are possible. The different states are shown in table 2.1.




(a) Single submodule




(b) Three phase MMC connected to a motor

Figure 2.3: Submodule and MMC

| Current direction | S1 state | S2 state | Vsm value | Capacitor status | Conducting device |
|---|---|---|---|---|---|
| Ism>0 | ON | OFF | Vc | Charging | D1 |
| | OFF | ON | 0 | By passed | S2 |
| Ism<0 | ON | OFF | Vc | Discharged | S1 |
| | OFF | ON | 0 | By passed | D2 |

Table 2.1: Voltage Vsm depending on switching state and current direction

The submodules are connected into series to build a phase arm. The phase arm contains an own inductor or part of a coupled inductor. Two phase arm in series compose a single phase leg. The phase arm connected to DC+ is called upper phase arm whereas the other is called lower phase arm. The AC output is tapped between the phase arms. Hence, three phase legs in parallel generate a three phase system. The AC ouput voltage is generated by actively inserting lower and upper submodules. Therefore the number of inserted submodules is called insertion index. The difference in number of inserted modules controls the outlet voltage. The insertion index results from the modulation. There are multiple possibilities to generate the insertion index and modulate the PWM signal, which will be explained later. Which method to use depends on requirement and application.

## 2.3. Comparison between common multilevel topologies and the MMC

The former subsections present the different topologies and how their working principles are. This chapter compares the topologies based on amount of semiconductor, capacitor and inductor required depending on number of levels. Additionally it will compare what voltage requirement the components depend upon. The table 2.2 shows the number of semiconductors, capacitor and inductor the different topologies need from left to right. The comparison is only conducted for 3 and 5 level topologies as they represent the available direct competitor to the MMC for drives. In the following subsection a discussion and conclusion follows for each kind of component.

| | 2L | 3L TNPC | 3L NPC | 3L FLC | 5L NPC | 5L FLC | 5L MMC |
|---|---|---|---|---|---|---|---|
| Switches | 6 | 6&6 | 12 | 12 | 24 | 24 | 24 |
| Diodes | 6 | 6&6 | 18 | 12 | 24&3*2 | 24 | 24 |
| Capacitors | 1 | 6 | 6 | 3&3 | 12 | 3&3&3&3 | 12 |
| Inductor | - | - | - | - | - | - | 3 |

Table 2.2: Number of components of each topology

### 2.3.1. Switches

The number of switches for 3 and 5 level are the same for all the mentioned topologies. This results in similar increase of conduction losses of all the topologies. The differences in switching losses are depending on control and modulation method. If a sort and select algorithm is used only one submodule is switching and rest are either on or of. In the other hand when a phase shifted modulation is applied all the switches are constantly operating. Apart of increasing the conduction losses the TNPC topology requires switches with different break down voltages. Generally it applies that for an increase in levels, the conduction losses increase because the current has to flow trough multiple semiconductor.

### 2.3.2. Diodes

The minimum number of diodes are the same for FLC, TNPC and MMC topologies. For the NPC topology the neutral point is clamped with two extra diodes in the case of 3L and six more in the case of 5L. Here the same conclusion is drawn as for the switches. The higher the number of diodes in series the higher the conduction losses are.

### 2.3.3. Capacitors

All the topologies apart of the MMC require a DC bus capacitor to compensate for reactive power. Moreover is the DC bus capacitor required to filter the PWM switching towards the battery or power supply. For the TNPC and NPC the originally single bus capacitor is split up into multiple in series connected capacitors. This could result into lower voltage rated components which have usually a bigger market volume and are therefore cheaper. In the case of FLC multiple extra capacitor are needed. In the case of 3L one extra and in the case for 5L three extra capacitors in comparison to NPC/TNPC are needed. Those three capacitor need also a different voltage rating.

For the MMC the situation is different. It does not require a DC bus capacitor but one for each submodule. The capacitor of every module will have the same voltage rating and value of capacitance. To conclude this chapter it shows that TNPC/NPC and MMC have an equal increase of capacitor. The loser in the capacitor comparison is the FLC topology.

### 2.3.4. Inductors

Only the MMC requires an arm inductor and therefore has for this point its biggest disadvantage in comparison to the other topology. Inductors have multiple disadvantage as they are generally expensive components and heavy. This would be a disadvantage in case of a drive inverter where the comparison takes place in the unit of power per weight and volume.

## 2.4. Conclusion of comparison

From the previous comparison and conclusion for each component it was shown that generally the higher the level number the more components are needed which results in higher conduction losses and possible higher costs. For a high level analysis the components of an converter system can be divided into three parts. The power hardware which was compared before is one of the three. The two other main parts of an inverter are the control hardware and the low voltage power supplies for the gate drive and the control hardware. The following list shows the three allocated main parts of an inverter.

- Power components
- Control hardware
- Power supplies

The comparison showed that the quantity of power components between the topologies at the same level number are equal or higher for non MMC topologies. Therefore the MMC topology can only compete with market strategical advantages like lower component prices or special MMC power modules. This would lead to an economical market analysis and is not scope of this thesis. The other two possible components are the control hardware and the auxiliary power supply. The control hardware contains the micro controllers, FPGA, sensors and software needed to run the inverter. Subsequently, the auxiliary power supplies are all the power supplies for the gate drives and the control hardware. Both can offer possibilities to reduce the amount of hardware required. The decision was taken to continue investigating the field of control. Therefore a state of research was conducted in form of a literature study. The literature study analysed papers related to control of MMC. The outcome together with this technical comparison will construct the basis for the research question.

# 3

# Literature study - MMC control architecture

This chapter contains the literature study which was used as a basis for the decision what this thesis should investigate on. The chapter groups different control fields related to the software and hardware implementation for the MMC.

## 3.1. Literature study on control system for MMC

The literature study started from the book "Modular Multi-Level Converter: Modeling, Simulation and Control in Steady State and Dynamic Conditions" from Giacomo Caseidi et al [16]. The book was written mainly with the focus for HVDC transmission technology. Therefore only the basic bullet points were taken out and further research on IEEE Xplore and researchgate with the scope on drive was undertaken. The following figure 3.1 shows a mind map with the bullet points star out of the center topic. Some of the subtopics are framed in blue as those can interact strongly with other blue subtopics.

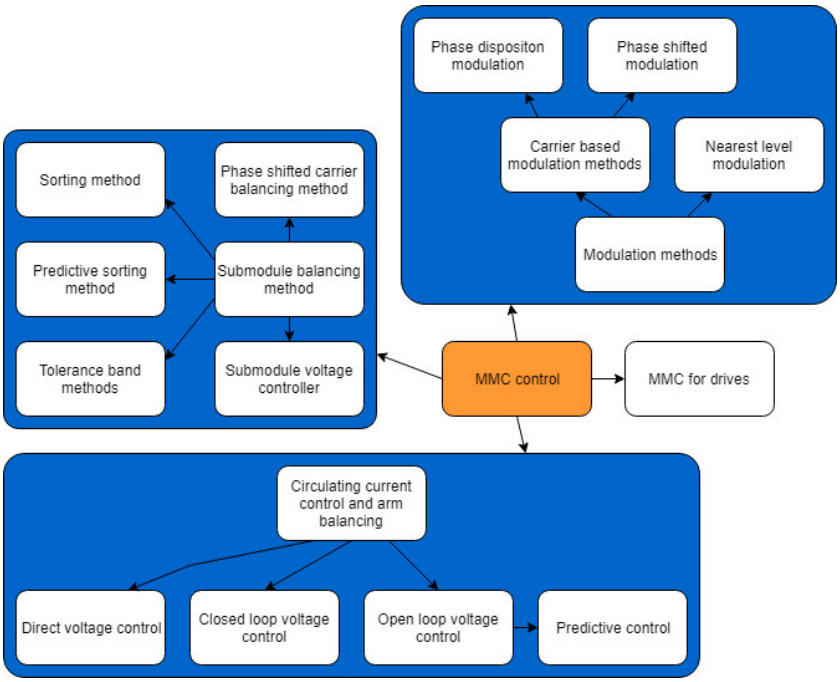



Figure 3.1: Mind map with the overview of control related topic to MMC

### 3.1.1. Modulation methods

This subsection treads the modulation methods of the submodules in a string. The modulation method should not be mixed up with the submodule balancing method where the goal is to control the submodule capacitor voltage. The modulation methods define how many submodules at what time point have to be inserted to create an output voltage respectively to a reference signal. In the book of Casadei et al [16] three different methods are presented of which two are part of the carrier based modulation. Carrier based modulation work with a carrier signal which are mostly in a saw tooth or triangle waveform. On top of the carrier signal the reference signal is laid. The pulse width modulated (PWM) signal is generated by setting the output to high and low at the crossing points of carrier and reference signal. Figure 3.2 shows an example of that method with the carrier and reference signal on top and the PWM signal at the bottom. Important for this modulation method is that the carrier signal has a frequency which is in order of magnitudes higher than the reference signal.

The quality of the output signal can be measured by the harmonics and the total harmonic distortion. For grid application the strength of the harmonic signal is limited by regulation and norms. In contrast to drive application were the harmonics are normally not regulated. Important to mention is that its generally the goal for drive as well to keep them low as they are causing additional losses and as the case may be undesired torque ripple and vibration [25].

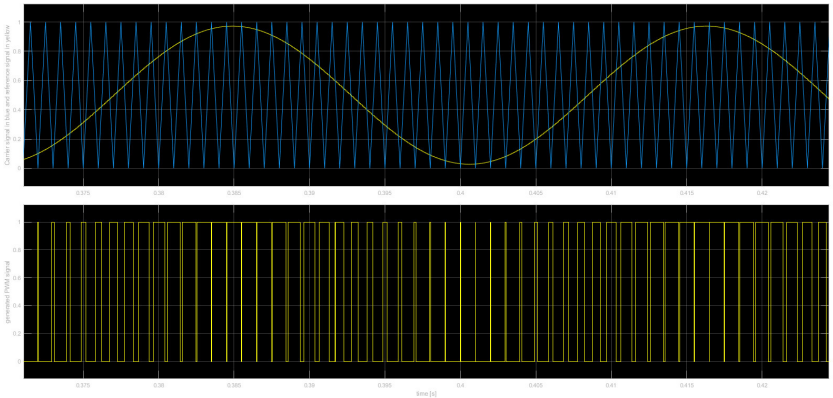
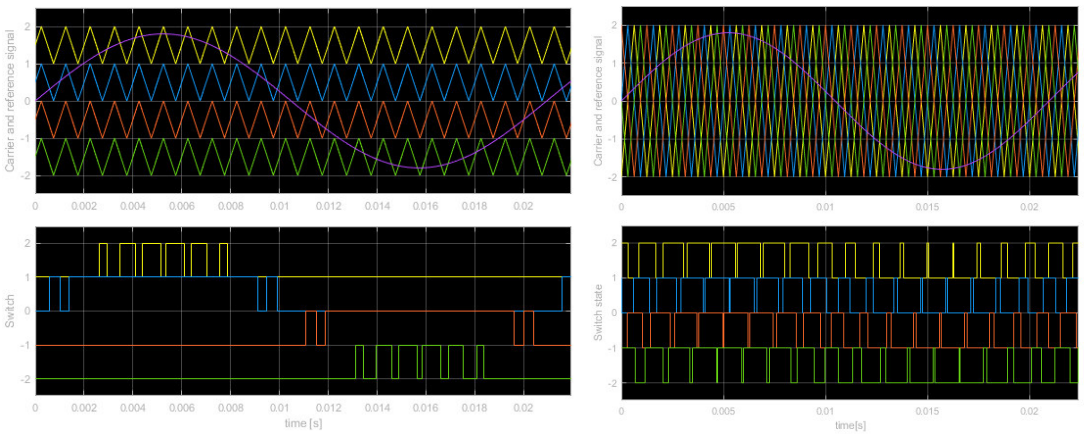


Figure 3.2: Example of carrier based modulation - Top: Reference on top of the carrier; Bottom: Generated PWM signal

In case of a two level inverter or in the case of MMC with only a half bridge topology a submodule the output voltage have 2 levels. The output is either DC+/Vc or Dc-/0. For the modulation of a reference signal between those two levels, one single carrier signal is required. To add multiple levels additional carriers are needed. The result of multiple carrier is that the reference signal can be arranged differently in reference to the carrier. Basically there are two main option of which the first one is the so called phase shifted carrier (PSC) and the second one the phase disposition carrier (PD)[31]. In case of PSC the carrier for the different levels have a phase shift between another. That leads to an equal amount of switching action per period of all the levels. For phase disposition the carrier are level shifted and have a smaller amplitude than the reference signal. This leads to lower switching action per period of reference signal. The comparison between the two methods is shown in figure 3.3.




(a) PD multilevel modulation

(b) PSC multilevel modulation

Figure 3.3: Two carrier based modulation methods - Top: Carrier and reference signal; Bottom: PWM signal for each level

The comparison in figure 3.3 between the two methods shows the effect of switching action on the submodule voltage behaviour. Both methods need voltage control of the submodule to keep the average voltage of the module constant. In case of the PD modulation extra controller is needed to distributed the switching action over all the submodules equally whereas for the PSC method only small adaption of the duty cycle are required. A comparison between the methods in [31] showed that PD is not suitable with out extra control. Other research papers tried to improve the disadvantage of PD with introduction of a state machine which distributes the switching evenly so that now sorting algorithm is needed [36]. The named sorting algorithm is a method to maintain voltage control of the submodules with PD modulation. More to this topic will follow in the subsection submodule balancing methods.

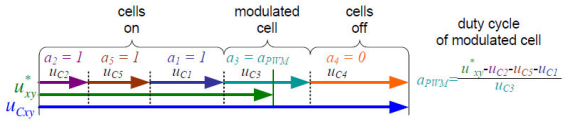
Similar methods are shown in [38] where the authors introduce a selective loop bias mapping to distribute the switching evenly. The authors in [13] introduce a method to improve the PSC modulation by a fundamental frequency sorting algorithm. In this paper the author uses methods from the PD modulation sorting algorithm to improve the performance of the PSC modulation. The advantage is that the sorting can run on much lower speed and lowers thereby the computational cost. Moreover it also makes the arm current sensor unnecessary. In [15] the authors used a similar approach. In their research the authors used a fast sorting algorithm and select the modules to insert depending on their on time during a cycle of the reference signal angle. They realized that biggest swing in energy of the capacitor is happening at pi/2 of the reference signal angle. Apart of optimizing the PD and PSC modulation research also discovered inherent advantage of the frequency factor of reference signal and carrier signal. In [23] the authors show that switching frequencies which are multiples of the fundamental frequency should be avoided. This is a problem for constant frequency operation of grid tied inverters.

Apart of the two PWM based modulation methods there is a third one which can further decrease switching action in case large number or submodule are used. The described method is called nearest-level control (NLC) or staircase modulation [16]. The method does not use a carrier signal but therefore uses the sum of available level to create the nearest available level. This method requires as well a sorting algorithm as some submodules are inserted longer than others and would result in unbalance of the submodule voltages. As the method is similar to the PD modulation, research was done in comparing both methods. In paper [14] the author introduces a new balancing algorithm and test them on NFC and PD modulation. The author shows that his method can reduce the voltage ripple in the submodule capacitor but remarks that the NLC method can only reach similar result to PD with higher submodule number.

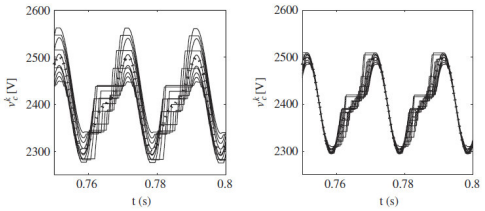
### 3.1.2. Submodule balancing methods

After introducing the modulation method it is crucial for a stable operation to have submodule balancing method. Those control methods are required to balance out voltage difference between the modules. The difference in voltage result basically because of two reasons. First of all the modulation method. If not phase shifted modulation is used it can be seen from 3.3a that phase disposition results in different numbers of average switching events. Therefore those submodules get charged and discharged unequally. Secondly be-

cause of hardware tolerances. Power electronic components come with tolerances which lead to unequal specification for the capacitor in series. The effect is that some submodule charge or discharge more than others. To tackle those problems there are three main methods for non phase shifted modulation. The first on is called the sorting method. It was introduced by the founder of the MMC R. Marquardt and A. Lesnicar [33]. When using PD modulation only one submodule is switching whereas the others are either inserted or bypassed. The modules which are inserted are either charged when the current is positive or discharged when negative. That results in an automatic unbalance of the submodule voltages. The sorting algorithm sorts the submodule according to their voltage and puts them into a list. If the current is positive the modules with the lowest voltage are inserted. The number of submodules inserted depends on the reference voltage. Figure 3.4a shows an example for five submodule. Each submodule has an arrow representing its voltage. The longer the arrow the higher the voltage. The blue arrow on the bottom represent the total voltage of all submodule. Consequently the green arrow for the generated reference needs to be lower then the blue one. As result from the list the submodule number two, five and one are inserted first because of their lowest voltage. Submodule number three is modulating the voltage and submodule number four is bypassed. The list is inverted for the case the current is negative. Additionally the rate of refreshing the list depends on the the submodule design and how much the voltage can deviate from the average value. An example of the effects on the refresh rate is shown in figure 3.4b. The left graph shows a refresh rate three times faster and on the right side 6 times faster than the fundamental frequency. The disadvantage of PD modulation and the sort algorithm is that they require measurement of each submodule voltage and current direction of upper and lower arm. For this reason the system is also prone to fail as the PD requires all the the named information to operate stable.




(a) Sorting scheme for positive current [29]




(b) Submodule voltage with difference refresh rate of the list [43]

Figure 3.4: Two carrier based modulation methods - Top: Carrier and reference signal; Bottom: PWM signal for each level

In the case of nearest level modulation the same control method is applied as for PD modulation. The difference is only that the submodule can only be bypassed or inserted and do not have the modulation operation mode.

Research tried to to reduce the requiered amount of sensor or make it more robust to failing sensors. Additionally it was tried to reduce the refresh rate of the list and reduce in the same time the deviation of the submodule capacitor from the average voltage. Therefore the predictive sorting and tolerance band methods were introduced. Predictive sorting estimates the switching pattern in advance and distributes according to the voltage level [24]. The authors show that the advantage has a two sided advantage. First the switching is only 2.8 times the fundamental frequency which results in low switching losses. Secondly the capacitor ripple could be reduced by 24%. By reducing the current ripple the size and cost of the capacitor can be lowered.

Tolerance band methods can be divided in two main methods, namely the average submodule voltage tolerance band (ATB) or cell tolerance band (CTB) [19]. Both work with a tolerance band in which the submodule voltage is limited. In case a submodule capacitor voltage is crossing the maximum tolerance it will be selected to be bypassed or inserted depending on current direction. In case of the ATB the sum of all capacitor voltage divided by the number of submodules is calculated. The tolerance band is around that value and therefore varying over time. In the case of CTB the tolerance band is based on the specification of the capacitor rating and fixed. The results from Hassanpoor et al. show that the ATB method has an excellent voltage balancing but requires a high updating rate of the list. CTB in the other hand, demands less computational power but cannot handle fault cases. Both methods have the advantage that the voltage measurement could be implemented simpler than in a pure list and sort implementation by using analogue comparators. CTB additionally has the advantage that it does not requiring a sorting algorithm and refreshes the list as soon a submodule crosses the tolerance band.

The last submodule balancing methods are based phase shifted carrier. Because the PSC has an advantage of naturally balancing the submodule without any additional control [39]. However the disadvantage of that method is the increased switching frequency and therefore its losses. Studies in [13] and [42] designed hybrid system based on the PSC and sorting algorithm. Chen et al. are proposing a fundemantel sorting algotrithm to balance the submodule capacitor in combination with low frequency phase shifted carrier modulation. The results reduced switching losses in comparison with normal phase shifted modulation. As well does it lower the computational requirement for the sorting algorithm as it is executed at fundamental frequency. By using phase shifted modulation no arm current sensors are required because of its natural balancing. This makes the system cheaper too. In the second study, Qingrui et al. present a reduced switching algorithm for voltage balancing with phase shifted carrier. They introduce the circulating current suppressing controller to minimize it. The results show that the controller can reduce the circulating and at the same time reduce the losses of the system with the voltage balancing method.

The last method is a direct voltage controller on the submodule. This controller is required because the paper of Kalle et al. [23] has shown that if the switching frequency is a integer multiple it can cause the capacitor voltage to unbalance. Therefore it can often be seen in distributed implementation that a local controller is used for example in [49] or [35]. The controller is usually a proportional feedback controller which adapts the reference signal.

### 3.1.3. Circulating current control and arm energy balancing

The next higher level after the submodule balancing is the arm energy controller. The goal is to evenly distribute the charge between upper/lower arm and between the phase legs. This is done by controlling the circulating current. The circulating current describes the internal current between the DC bus terminals which is not leaving to the phase outlet. Therefore the circulating current is controls the charging and discharging behaviour of the inserted submodule. However, the insertion indices also controls the current itself. Therefore arm balancing and circulating current is controlled with the insertion number of lower and upper arm. Thus, the control of the circulating current is complex task.

The methods can be divided in three basic methods which are direct, closed loop and open loop voltage control. Direct voltage control generates directly without any capacitor sum reference the indices. It was shown in [18] that the direct voltage control proves to be a asymptotically stable but parasitics appear in the output and internal voltages. The authors solved that with an cascaded circulating current control. Closed loop voltage control describes all method which are using measurement feedback from submodule voltages or arm currents to generate the insertion indices. The authors in [8] showed that using the capacitor voltage sum as reference for the insertion indices generation in combination of a upper and lower arm energy controller shows the best result without any parasitic voltage components on the phase voltage. She et al. show in their paper [44] that with a proportional controller for the circulating current can further reduce the AC component of it. To the same results came the authors in [11]. An other alternative to reduce the harmonics of the circulating current is presented in [20] in which they introduce repetitive control scheme. In the work of Tu et al. [48] show that with a transforming the circulating into a two axis axis frame they can be controlled by a pair of PI controller. Their focus was to optimize operation for a three phase system. The disadvantage of all the closed loop approaches is the requirement of many sensors. Additionally the system was relying on those sensors for stable operation. Therefore the open loop voltage controlled was developed. Most of them take similar approach by estimating the sum capacitor voltage to generate the insertion indices and for the arm balancing. Resulting in less sensors and therefore a more economical MMC. In [9] the authors show that the proposed method is asymptotically stable. Thereafter in [41] show in a comparison with closed loop similar performance and verify it on experimental set-up. A possible application for the MMC with open loop voltage control the authors show in [6] in which they present a three phase 50 Hz to single phase 16.7 Hz converter for railway networks. To improve the open loop approach regarding the reduction of the circulation current harmonics the authors present in [22]. The authors present a method for the numerical estimation of the amplitude and phase of the induced harmonics for circulating current control. Another approach to reduce the numbers of sensor needed is to use model predictive control. The authors in [26] therefore introduce a discrete- time mathematical model of the system and a predictive model corresponding to it. The predictive is used to generate the best switching patterns based on cost function associated with control goals of the MMC system. The system was evaluated on a time domain simulation study in which it showed satisfactory operation. Similar work was done in [34] inwhich the authors developed a state space model of the MMC. Together with a state observer it is possible to estimate the capacitor voltage based on the output cur-

rents. The study [40] proposes a control structure consisting of periodic linear quadratic regulator with and extended least square estimator to determine the current and energies. The proposed strategy was verified with simulations.

### 3.1.4. Control architecture

In the book of Casadei et al. they differentiate between centralized control and decentralized control. Centralized control represents a MMC in which all the control and modulation is executed in one central unit and then distributed over optical fiber or similar to the submodule. That results in large number of fibre optic connection and a central controller which requires a high computational power and many I/O. Moreover every sensor, either on the submodule or on the arms, needs to be connected as well to the central controller.

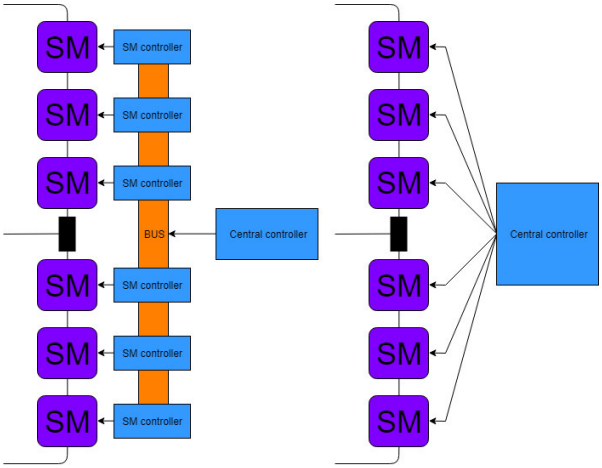



Figure 3.5: Comparison of distributed control on the left and centralized control on right side

On the other hand distributed control refers to the system where part of the control is distributed over different level. This results in either in a leg, arm or submodule controller which is then conected to a central controller again. Figure 3.5 shows the two extremes of which on the left side every submodule has an own controller and on the other side a single centralized controller. The advantage of distributed control is that the computational power can be distributed and offers a higher redundancy in case one of the controller fails to operate. Moreover, distributed control does open the possibility to use a bus based communication. An example for distributed control on phase leg level is the implementation of Johannes Kolb in [28]. The author used a single FPGA per phase leg which is connected to a bus. All the measurements and the main controller are conected to the bus as well. The FPGA is in charge of sorting, selecting and modulation which needs to be fast whereas the central DSP is in charge of the high level control.

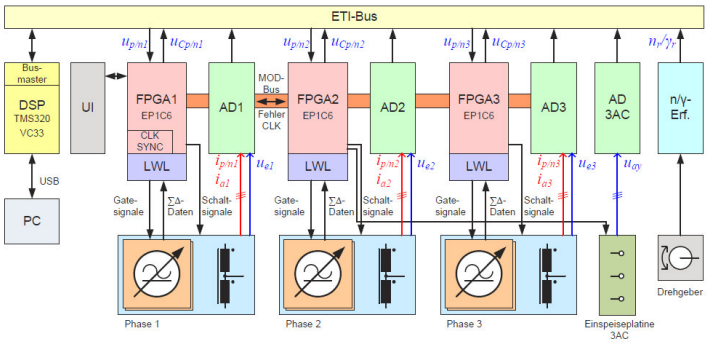



Figure 3.6: Implementation of distributed control by Kolb in [28]

To further reduce the workload on the bus, Mathe et al. investigated to distribute the modulation and balancing to every module [35]. The modules are therefore connected to an EtherCAT bus and receive only the

reference from a central controller. The advantage is that they are lowering the data volume between the central controller and submodule to only 4 bytes instead of 16 bytes. Moreover the cable length was reduced by at least one third in their test setup. This results in a reduction of overall cost of the designed converter. The difficulty in the authors implementation is the synchronization between the submodules for the modulation and the time to send the reference to all the submodule. In his implementation he reached a speed of 90-100 $\mu C$ with a cable length of 0.3m between 6 modules and a data length of 10 bytes. This results in a maximum update frequency of 10 kHz.

Instead of using Ethercat, The et al. used the CAN protocol as a bus [47]. They are reasoning that for low number of submodule the CAN protocol is fast enough and therefore they decided to experimentally test it. The setup is a single phase MMC similiar to the EtherCAT implementation. The difference comes in the implementation of the bus. The CAN bus set-up uses only two slaves which controls four submodules for upper and lower arm whereas the EtherCAT implementation uses one controller per submodule. The CAN bus implementation used a sort and select balancing method instead of the phase shifted carrier method of the EtherCAT set-up. The problem of The et al. came across was the CAN bus architecture is a multi-master communication protocol and therefore makes the access to the bus of each node unequal. The result is then that some nodes were prioritized of using the bus which is unfavourable for the master control. The authors say that it can be solved with a request answer methodology instead of multi-master communication.

Both authors came to the same conclusion that it would be possible to use lower level communication like SPI or I2C to make the hardware simpler and cheaper for low submodule number converters. This conclusion could lead to a simpler and cheaper implementation.

### 3.1.5. MMC for drives

The introduction explained why multilevel converter are attractive for drive applications. For that reason the industry started to look into the field in cooperation with research institution. Therefore Hiller et al. make a comparison with established topolgies in [21]. The analysis shows that the MMC requires comparable Si-area and DC link capacitance. In the conclusion the authors state that the MMC can "lead to compact and attractive solution for a wide range of application in the medium voltage converter market". The problem of using an MMC as a drive inverter is the start up and low output frequency operation. When deriving the maximum power pulsation per submodule the following equation will result.

$$\Delta W_{max} = \frac{\hat{i}_o}{\omega_o}\left(\frac{U_{dc}}{2} - \frac{2}{3}\cdot\frac{\hat{u}_o^2}{U_{dc}}\Big(1 + cos(\phi)\Big)\right) \tag{3.1}$$

The subscript 'o' stands for output. Hence it can be seen that the work pulsation is inverse proportional to the frequency. The result would be an non-operational MMC in lower frequency range as the capacitor would limit the pulsation. To solve that problem different papers introduced a common mode voltage with a much higher frequency as the output frequency. The outlet current is not affected by the voltage as it only would introduce circulating current which is needed to reduce the work pulsation. This concept is presented and verified in [27], [32] and [30]. The author in [32] is concerned about the proposed method and recommends to investigate the effect of bearing discharge resulting from the induced common mode voltage. The authors in [17] compare sinusoidal, third order harmonic and square wave induced common voltages with each other. They come to the conclusion that using square wave common mode voltage injection leads to the smallest increase in circulating current while reaching a stable operation of the MMC in low frequency. Moreover it was possible to verify a start up from standstill in a experimental set-up. The reason why researchers try to keep the resulting circulating low is because of the increase in switch current rating. The authors in [10] show that under constant torque from zero to nominal speed the arm current is up to 3.5 times higher in the low frequency operation. In conclusion the inverter needs to be designed with higher current capability to operate with constant torque up to the nominal speed. For the correct sizing the author in [29] did a very extensive guideline how to size the power electronic components.

## 3.2. Conclusion literature study

The literature study gave a brief overview on the state of research for MMC control since the first introduction of it in 2004. The focus of this thesis is to find a possible option to reduce the complexity of a MMC system. The possible ways to reduce components or software complexity can be divided into two categories. First

category is modification of the control system to get rid of sensors or lowering certain unwanted operation modes. The second category is to maintain the control system but changing the physical hardware implementation. The former literature study shows that more research paper are related to control improvement like reducing circulating current or using an energy estimator instead of capacitor voltage measurement. In the second category are topics like distributed control and bus communication. The two papers found on the topic of bus communication date back to 2015 and 2017 (see subsection 3.1.4). Both paper recommend that further investigation in lower level bus protocols could lead to a less hardware and software intense implementation of a MMC. For the long term goal of implementing a drive inverter into a small housing it makes sense to directly couple the $\mu C$ with a low level communication protocol like I2C, SPI or UART. Those protocol require short distances between the $\mu C$ which is the case for a integrated drive unit. The argument of integration leads to the question why not directly use a central controller. Therefore a list of argument for and against the proposed distributed control was established. The following arguments speak for a distributed control based on a low level communication protocol. The arguments are based on results from research papers in the literature study.

- High redundancy
- No need of hardware implemented centralized controller
- $\mu C$ requires low numbers of I/O
- Less connections between $\mu C$

After listing the argument which are speaking for it, the following arguments are against.

- High number of $\mu C$ required - one per submodule
- Resulting limitations by the communication bus

The listed arguments are oppositional to the arguments which speak for a centralized controller. For example the high redundancy of a distributed controller results in lower redundancy for a centralized controller. Therefore more argument speak for a distributed control which is based on a bus communication. This thesis therefore set the goal to implement a system to validate the distributed control with a low level communication protocol. The simplification of the system is the resulting full modularity of the submodules and scalability. To limit the boundaries of the thesis, following decision were taken for the test set-up hardware design procedure.

- Well-known components with good reference designs
- Low voltage components
- No power specification for the design procedure

Those simplification respectively limitations keep the cost of the system low and result in a fast implementation of validation platform. The reason therefore is that the hardware design does not add anything new to the state of research moreover it gives the opportunity for the designer to improve his design skills.

# 4

# Framework design and communication bus selection for a single phase system

This chapter contains the process how the Simulink model was implemented. In a first step minimum requirements to answer the research questions were defined. The first decision was to build a single phase system to minimize the time to build the hardware. In a next step the numbers of levels had to be decided. The decision was taken based on two arguments. First argument is that a comparison between multilevel topologies is only coherent if they possess the same number of levels. Therefore only 3 or 5 level were viable option. The second fact is that according to IEC 60034-12 the value for dV/dt at the phase connector of the electric motor is limited to specified values. The MMC is designed with high speed MOSFET switches and therefore will reach high dV/dt values. Subsequently the higher level option is preferred to lower the dV/dt value of a single level step. The final decision was therefore to design for 5 levels implemented by four submodules. Before going into detail of the Simulink model the mathematical description will be presented. Thereafter the bus for the implementation was selected. Based on the selected bus the system was first designed in Simulink to be later on replicated into hardware.

## 4.1. Mathematical description of a single phase MMC

The mathematical description is based on a single phase system with simplified units of the MMC. This section is based on the work of Johannes Kolb in [28]. In Kolb's Phd thesis Johannes Kolb built a back to back MMC converter to drive an electrical machine. Kolb's derivation are focused on drive application and are therefore used here. The following figure 4.1 shows the model in which the system is represented. Moreover, each block represents a main part of the single phase arm. The two blue circles in series represent the constant voltage source which make up the DC bus. The violet output block is the phase outlet of the MMC phase leg. Uac represent its voltage and Iac the current trough the outlet. Rua and Rla represent the the sum of lower and upper resistance resulting from the inductor, wiring and semiconductors. The arm inductor is represented as a coupled inductor with upper inductance Lua and lower inductance Lla. The yellow block with blue circles represent the submodules. Thus it is a variable voltage source depending on insertion index. In a next step the Kirchhoff's law is applied to the current at the knot next to the coupled inductor in the following equation 4.1.

$$I_{up} = I_{circ} + \frac{I_{ac}}{2} \quad I_{low} = I_{circ} - \frac{I_{ac}}{2} \tag{4.1}$$

The circulating current follows with the sum of both and equals to the following equation 4.2.

$$I_{circ} = \frac{1}{2} \cdot (I_{up} + I_{low}) \tag{4.2}$$

The load current follows from the subtraction of the currents from 4.1 and results in equation 4.3.

$$I_{ac} = I_{up} - I_{low} \tag{4.3}$$

Applying the second Kirchhoff's law the voltage sum for the upper and lower mesh is calculated, the result are the following two equations (4.5 and 4.4).

$$\frac{U_{dc}}{2} = U_{up} + U_{Rua} + U_{Lua} + U_{ac} \tag{4.4}$$

$$\frac{U_{dc}}{2} = U_{low} + U_{Rla} + U_{Lla} - U_{ac} \tag{4.5}$$

The voltage on the inductor (4.7) and the resistance (4.6) the following equation applies. The indices x stands for either upper or lower arm.

$$U_{Rx} = R_x \cdot I_x \tag{4.6}$$

$$U_{Lx} = L_x \cdot \dot{I}_x \tag{4.7}$$

After adding the equation for the inductor and resistor to the main equation 4.4 and 4.5 a solution for the circulating current and the AC current can be found. The result shows that the circulating current is not coupled to the AC current. For the circulating current following equation can be derived.

$$\frac{L}{R}\dot{I}_{circ} = \frac{1}{2R} \cdot (U_{dc} - U_{up} - U_{low}) - I_{circ} \tag{4.8}$$

The equation 4.8 shows that the circulating current has a behaviour of a first order element with a time constant of L/R and a gain factor of 1/2R. The equation for the AC current can be simplified if a coupled inductor is used by cancelling out the inductor term. Then the equation can be derived for the current as well and the following equation 4.11 results.

$$I_{ac} = \frac{1}{2} \cdot (U_{low} - U_{up} - 2U_{ac}) \tag{4.9}$$

The equation shows that the AC current can be directly control by the difference of upper and lower insertion index. The derivation gave an insight on how the output current is controlled and how the circulating current can be minimized. However it does not show how the energy flows trough the arm and how the capacitor are affected.

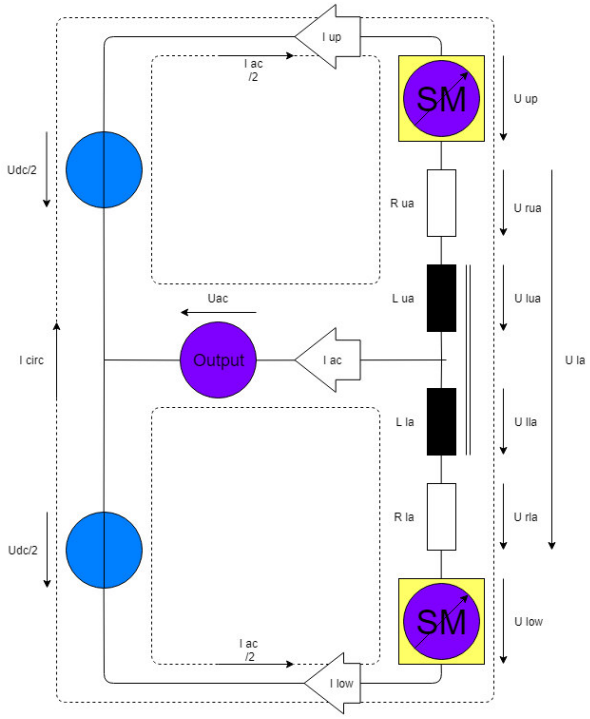



Figure 4.1: Single phase MMC model

Therefore the power equations for the upper and lower arm are derived. The equation 4.4 and 4.5 can be rearranged to the voltage of the strings.

$$U_{up} = \frac{1}{2}U_{dc} - U_{ac} - R_{ua} \cdot I_{circ} - L_{ua}\dot{I_{circ}} - \frac{1}{2} \cdot (R_{ua} \cdot I_{ac} - L_{ua}\dot{I_{ac}}) \tag{4.10}$$

$$U_{low} = \frac{1}{2}U_{dc} - U_{ac} - R_{la} \cdot I_{circ} - L_{la}\dot{I_{circ}} - \frac{1}{2} \cdot (R_{la} \cdot I_{ac} - L_{la}\dot{I_{ac}}) \tag{4.11}$$

The ohmic and inductive voltage drop can be neglected for this analysis as their contribution is small in comparison to the voltages from the submodule capacitors and DC bus voltage. The power of upper and lower arm results from the product with the simplified arm voltage times the arm current $I_{up}$ and $I_{low}$.

$$P_{up} = \frac{1}{2}U_{dc} \cdot I_{circ} - \frac{1}{2}U_{ac} \cdot I_{ac} + \frac{1}{4}U_{dc} \cdot I_{ac} - U_{ac} \cdot I_{circ} \tag{4.12}$$

$$P_{low} = \frac{1}{2}U_{dc} \cdot I_{circ} - \frac{1}{2}U_{ac} \cdot I_{ac} - \frac{1}{4}U_{dc} \cdot I_{ac} + U_{ac} \cdot I_{circ} \tag{4.13}$$

Both equations have the same first two terms which is the difference between DC power and AC power. As the submodules are not consuming or generating active power in average the the difference needs to be zero. This reflects the power flow from the AC to the DC side of the converter. The third term represent the pulsating power generated by the output current. This is a pure pulsating power with an average of zero and needs to be compensated by the capacitors. The last term is similar to the third term whereas here the output voltage is pulsating with the output frequency. The circulating current can be controlled to contain a AC component in phase with the output voltage $U_{ac}$ and therefore lets shift energy between the arms. Following to the analisys of the power the sum and difference between the upper and lower arm can be calculated based on equation 4.13 and 4.12.

$$P_{\Sigma} = P_{up} + P_{low} = U_{dc} \cdot I_{circ} - U_{ac} \cdot I_{ac} \tag{4.14}$$

$$P_{\Delta} = P_{up} - P_{low} = \frac{1}{2}U_{dc} \cdot I_{ac} - 2U_{ac} \cdot I_{circ} \tag{4.15}$$

As mentioned before the equation 4.14 is the power flowing into and out of the arm. It is controlled by the constant current component of $I_{circ}$ and the active power component of the output current $I_{ac}$. The second equation 4.15 contains the pulsating power components of upper and lower arm. They can be controlled with the AC current component of $I_{circ}$. Both equations need to equal to zero in steady state operation. To conclude the derivation it was shown that following variable need to be controlled for a stable operation of the MMC phase leg.

- $I_{circ}$ AC component
- $I_{circ}$ DC component
- Phase angle and amplitude of $I_{ac}$

To control the two presented current the controller has to act on $U_{up}$ and $U_{low}$. In case of the the circulating current $I_{circ}$ with difference of $U_{dc}$ and the sum of $U_{up}$ and $U_{low}$. Whereas for the $I_{ac}$ the difference between both $U_{up}$ and $U_{low}$ is the variable which has to be acted on.

## 4.2. Communication bus selection

The mainly used communication ports of a $\mu C$ or a DSP are I2C, SPI and UART. Those communication standards can be used to communicate directly with the processor without the need of an intermediate processing unit. For the proposed application a bus with multiple slaves is required, therefore UART falls out of the selection. The two bus protocol left over are I2C and SPI. Before selecting the bus an overview of the performance of each bus type is showed in table. The performance of the bus depends of the used hardware.

The hardware used to develop power electronic control in the research group is LAUNCHXL-F28027 from Texas instruments. This is a developer board which can be programmed with Simulink with no need of C-programming skills. The table 4.1 shows the performance of the two buses with the F28027 board. The most obvious difference comes in baudrate and word length. SPI is faster and can send words with a higher resolution than I2C. On the other hand SPI requires more connection than I2C does. Its even worse in case SPI is used with multiple slaves and not in a daisy chain configuration. For that the master would require a slave select pin for every additional slave. On the other hand I2C has and hardware implemented address assignation for every slave on a single two wire bus.

| | SPI | I2C |
|---|---|---|
| Baudrate | 15 Mbits | 400 kBits |
| Word length | 16 bits | 8 bits |
| Number of connection | 4 at least | 2 |
| Multimaster ability | No | Yes |
| Architecture | Daisy chain or multislave | Multinode bus |

Table 4.1: Comparison of SPI and I2C

In a next step the limitation of the bus on the planned application had to be found. Therefore some assumption were made for the message sent between the master and the slave. First of all the master sends the sinus reference to the slaves. The sinus is defined by its angle, amplitude and shift. Secondly the master needs the voltage information of each submodule back for control purpose. That results in a total of 6 words which have to be exchanged. In case of the SPI communication the bus is designed in a daisy chain configuration. Every F28027 has a shift register with 16 bits. The master module pulls down the slave select and starts the clock to initiate the transmission of the messages. Word by word will be pushed forward controlled by the master. The slaves are reading out as many words as they are programmed to do and hand them to a receive register. As the SPI protocol does not have a start or stop information in the word sent the slaves do not know what information they get. Therefore a additional start indication word is added. As a result the master needs to push 10 words to get the 6 important words trough the chain. After getting the information back he can check if the received words are in the right order and not corrupted as a sanity check. Figure 4.2 shows the set-up of the implemented SPI bus. The clock and slave select connection are connected in parallel from the master to all the slaves and are not shown. As the slave select is connected in parallel all the slaves are sending and receiving at the same time.

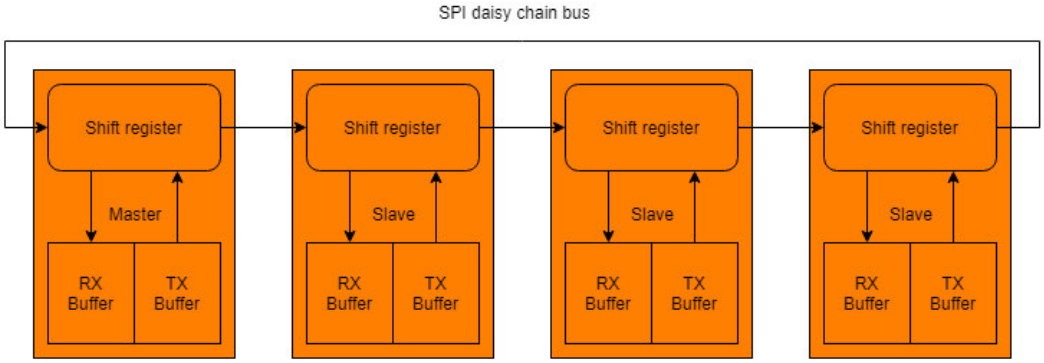



Figure 4.2: SPI bus daisy chain implementation

The I2C has less connection from master to slave and moreover are the slaves not connected in series. Therefore the master is in control of the bus and hands over the control to the slave with a command. In addition the master needs to address to which slave he wants to talk. The I2C protocol has an acknowledge bit as a sanity check of the received word. This altogether creates an overhead of 12 bits to send or receive 8 bits of data. Figure 4.3 shows the two communication lines and what signals they are transmitting. It has to be taken into account that the ratio of data to overhead gets better if 16 bits wants to be sent as with the SPI implementation. After understanding how the two communication methods work the requirement for the MMC were

defined. For stable operation of the MMC it is assumed that the reference sine wave is update for modulation with every PWM cycle. Therefore the operation of the MMC is limited by the maximum rate of refreshing the required information which is 6 words with 16 bit resolution. The maximum rate can be calculated with number of bits of the message divided by the maximum bitrate of the communication bus. The shown results in table 4.2 are based on a 4 submodule phase leg. It can be seen that the message length for the I2C bus is already longer than the SPI bus, together with the lower bitrate the maximum refresh rate reached for the assumption taken is 2299 Hz.

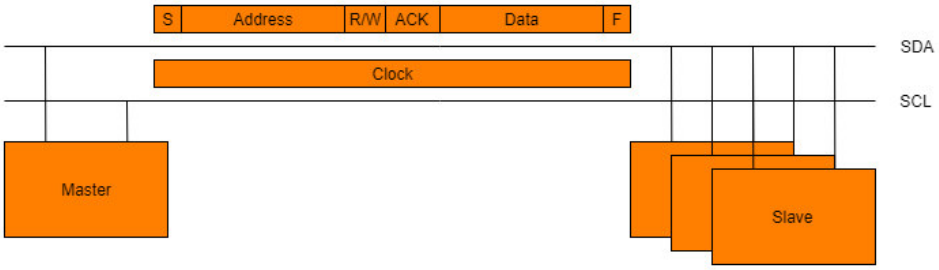



Figure 4.3: I2C bus

Therefore it is about 40 times slower than the SPI bus with 93750 Hz. As the modules are operating phase shifted the switching frequency respectively the refresh rate has to be multiplied with the number of submodule. This results in a switching frequency of 9.195 kHz for I2C and 375 kHz for SPI. In drive application the switching frequency needs to be at least in order of 10 times higher than the electrical frequency of the motor. The electrical frequency depends on the speed of the drive (n[rpm]) and the number of pole pairs (p) as shown in the following equation.

$$f = \frac{n}{60 \cdot p} \tag{4.16}$$

Synchronous motor with permanent magnet used in the automotive industrie have a high pole pair number between 3 and 6. In addition with a maximum motor speed of up to 20k rpm the resulting electrical frequency is 4 kHz. Therefore to maintain low losses in the motor caused by harmonic distortion the switching frequency preferably is higher than 40kHz. However the I2C bus reaches a maximum frequency of about 9 kHz and is therefore limited to a speed around 5000 rpm and is not suitable for the application. Therefore it was decided to continue with the SPI bus.

| | SPI | I2C | Unit |
|---|---|---|---|
| Message length | 160 | 174 | bits |
| Baudrate | 15'000 | 400 | kbps |
| Maximum refresh rate | 93750 | 2299 | Hz |
| Submodule number | 4 | 4 | |
| Resulting switching frequency | 375 | 9.195 | kHz |

Table 4.2: Resulting switching frequency

### Modularity advantage of SPI in comparison to I2C

Another important advantage of the SPI bus in comparison with the I2C is the intrinsic knowledge of the number of slave in the daisy chain configuration. In a I2C setup the master needs to know all the addresses of the connected slave to be able to communicate. On the other hand the SPI bus can figure out the number of slave without the need of reprogramming the master. As the bus is built in a daisy chain the master can push and count till it gets the starting message back. The number of pushes is then equal to the number of slave in the bus. This offers the capability to have a modular system which does not need a reprogramming the master device.

## 4.3. System design in MATLAB Simulink

The former mathematically described system had to be realized into a detailed Simulink model first to validate the performance. The model in Simulink used the Simscape Power System toolbox to model the system. The toolbox contains very simple replication of the components. For the submodule a two MOSFET switches with integrated anti parallel diodes and a capacitor were used. The upper arm contains two submodule as well as the lower arm. The upper arm inlet is connected to an upper voltage source as the lower was connected at the ouput to the second voltage source. Two voltage sources were therefore set in series with the midpoint going to the load. The load is then connected to the coupled inductor. The coupled inductor is connected to the lower and upper arm via series resistor representing the the sum of resistances in upper and lower arm. The employed voltage source have unidirectional power flow. The component in Simulink does not have this option, therefore a diode was put in series with the power supply blocks. To compensate the negative circulating current capacitor are put in parallel to the string of power supply and diode. The figure 4.4 shows the previously explained model. The following subsections explain how the distributed control is implemented for the test set-up.

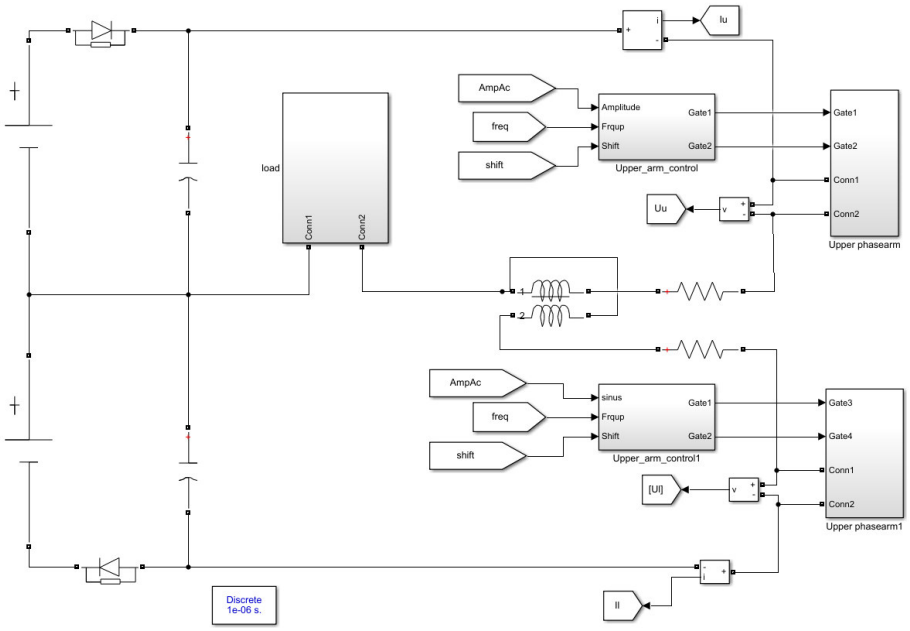



Figure 4.4: Simulink model

### 4.3.1. Open loop distributed control implementation in Simulink

Distributed control describes a variety of MMC control system where part of the control is handle over to the submodules as describes in the literature study. For the proposed test set-up it was decided to have two level of controller. First a high level controller and second a submodule controller. The high level controller is in charge of the internal and output control. Internal control refers to the voltage balancing and output control to the generated output waveform. Therefore the high controller requires upper and lower arm current information plus the capacitor voltage information of every submodule. Those information are used for energy balancing and circulating current control. The controller adapts the command signal and outputs the reference signal for the submodules. This is in contrast to the submodule controller which uses the reference signal and adapts that to control the voltage level of its capacitor. The adapted signal is therefore used to generate the PWM signal for the switches. As this thesis does not focus on the control only an open loop implementation was created in Simulink. Therefore every submodule contains a PWM signal generator as seen figure 4.5.

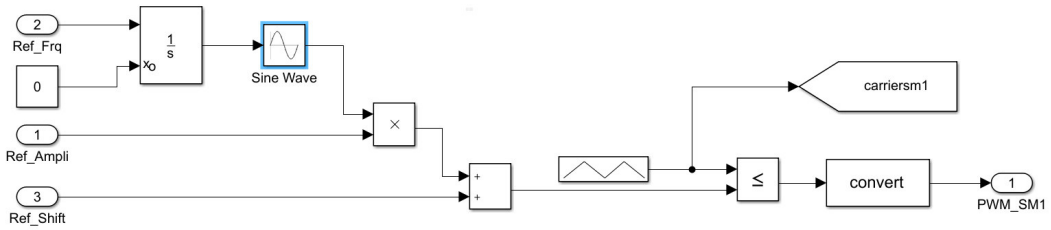



Figure 4.5: Submodule PWM generator

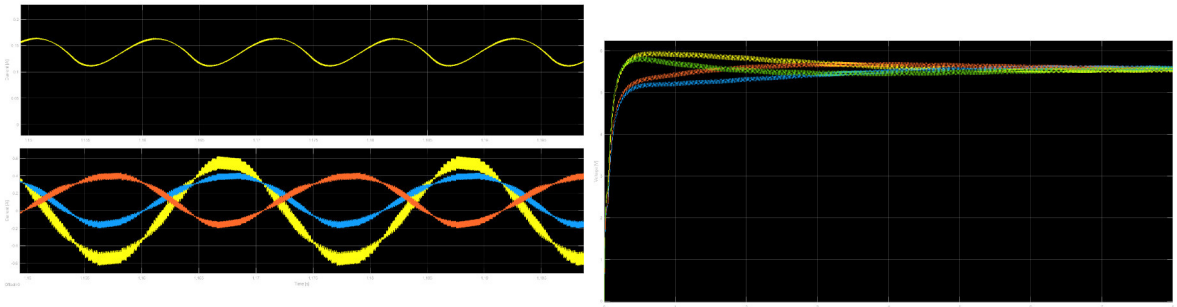
To generate the reference sine wave the controller depends on the integration constant for the integrator, amplitude and bias. Based on the generated sine signal and the carrier signal the PWM signal is created with a comparison operation. For the correct operation the carrier signal are phase shifted by $\pi$ in a phase arm and $\pi/4$ between upper and lower arm. The integrators of the upper submodules start at 0 whereas the lower integrators have an initial value of $\pi$. The high level controller only commands the frequency and amplitude of the output sine wave in an open loop implementation. The value for bias is set to 0.

### 4.3.2. Results from the open loop simulation in Simulink

The designed Simulink model is evaluated under the in table 4.3 shown parameters. The results are generated to compare subsequently with the physical set-up. The important information to show the correct operation are the upper and lower arm current plus the output current. Additionally the voltage waveform of the submodule voltage. The results shows that all those values reach a steady state in which they stay in a stable range. Especially the result of the capacitor voltage show the robustness of phase shifted modulation as all the voltage waveforms of the capacitors level out over time without any additional control.

| | Value | Unit |
|---|---|---|
| Modulation amplitude | 0.8 | |
| DC Bus voltage | 10 | V |
| Load resistance | 5.1 | Ohm |
| Load inductance | 0.1 | mH |
| Output frequency | 48.3 | Hz |
| Sinus bias | -0.2 | |

Table 4.3: Simulation parameters



(a) Top: Circulating current; Bottom: output, lower and upper arm current

(b) Submodule voltage waveform

Figure 4.6: Resulting current and voltage waveform for load and submodule capacitors with in table 4.3 defined simulation settings

## 4.4. Conclusion system modelling and bus selection

Based on the mathematical model this chapter showed which variables have to be manipulated to control internal and external power. In a next step different viable low level bus communication were analysed. The

SPI bus protocol showed the best performance because of the speed and low overhead content of the single message. Thereafter the proposed system was designed in Matlab Simulink to identify the information which have to be handle for a stable operation. The result shows the proposed open loop control together with phase shifted modulation reach a stable operation. Therefore giving the green light to implement the system in hardware.

# 5

# Design and implementation of the single phase system

The focus of the design procedure was to use off the shelf components with low prices because the setup is mainly used to validate different control procedure over the SPI bus. Therefore no specific power or voltage requirements were defined to select the components. Instead the specification were based on the following limitation and design simplifications.

- Maximum current of the lab bench power supply 50A
- Maximum voltage of the lab bench power supply 50V
- Limit EMI with low voltage components because of hard switching
- Low current to limit conductive losses and therefore the necessity of passive or active cooling
- Single low voltage source for all the submodules
- Gate driver power supply from the low voltage side

Based on those boundaries the submodule was designed and components therefore were selected.

## 5.1. Submodule design

According to the described boundaries the power PCB was separated into a high voltage (HV) and a low voltage (LV) part. The gate drive is powered by a galvanic isolated DC/DC converter from the LV side. The LV side has a female header for the control board and consists of the filtering of the switching and measurement signals. For measuring the capacitor voltage a galvanic isolated op-amp is used. All the signals are feed into the female headers. The HV side consists of the half bridge of two MOSFET and the capacitor. The capacitor voltage is measured with a voltage divider and feed into the galvanic isolated op-amp. For the high side switch a bootstrap methodology is used for switching. A single galvanic isolated gate drive is used to drive the half bridge. Both side use the same connector for simplification reason. Based on the named conceptual decision the components were selected. The figure 5.1 gives an overview of the PCB architecture concept.

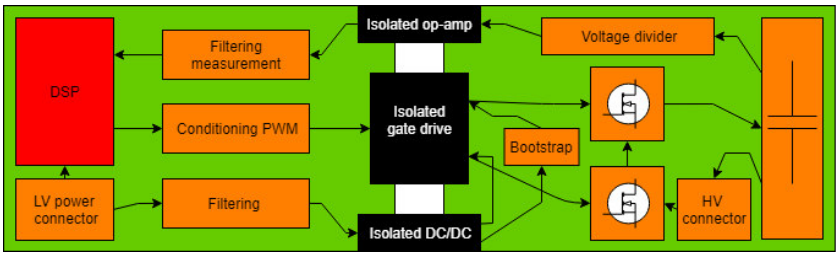



Figure 5.1: Conceptual PCB architecture

### 5.1.1. Component selection

It was chosen to select the components based on the limitation given by the PCB and the cost limitation. Therefore the copper traces together with the possible connectors limit the current rating for the switch. In this case the PCB is produced by the company JLCPCB. The company offers a maximum copper track thickness of $75\mu m$. By varying the width the current rating can be adjusted. The other bottleneck is the connector. It was decided to use the 5.08mm standard plug with two poles. This type is limited to a constant DC current of 15A. According to IPC-2221 for a track length of about 20mm and a temperature rise below 20°C the minium track requirements result in 3.8mm. Based on that outcome in a next step the MOSFET was selected. The MOSFET is selected based on two specification, firstly the current rating and secondly the breakdown voltage. For a precaution reason it was decided to select the component with a higher rating than required. In case of the current the switch needs to handle at least 15A and for the voltage rating 50V. Based on a price comparison on mouser the STP25N10F7 MOSFET from ST microelectronics. The switch comes in a TO-220 packaging and has a current rating of 25A and a blocking voltage of 100V. Thereafter the capacitor was selected accordingly to the switch. To keep the cost and size of the system small it was decided to use electrolytic capacitor. The disadvantage of such is that they are limited by a maximum rms current rating. This limitation comes results from the temperature rise of the component during high current circulation. The temperature rise could evaporate the electrolyte and then destroy the component. It is possible to increase the rating with better cooling of the capacitor. For this application the set-up will not go trough long continuous high currents and therefore the component was sized that under maximum current the voltage drop of the capacitor is bellow 10%. The capacitance required for that requirement is calculated with equation 5.1. The value for dt was selected to be a full period of a PWM cycle at 1kHz operation frequency. The minimum required capacitance resulted is 3 mF.

$$C = \frac{dt}{dU} \cdot I \tag{5.1}$$

Thus a capacitor with a voltage rating of 50V and a capacitance of 2.2 mF was selected. Four of the capacitor will be used in a two in series and two in parallel arrangement. The total capacitance is 4.4 mF with a voltage rating of 100V. With the capacitor all the power electronic components were selected and in a next step the gate drive, power supply and galvanic isolated op-amp had to be chosen. For the gate drive a dual channel driver with good documentation was searched. Texas Instruments offers with the UCC2150 a dual channel MOSFET driver with a 4A peak source and 6A peak sink output capacity. This gate drive is very good documented and has a hardware integrated deadtime control. The documentation included a reference design for a half bridge and therefore this component was selected for the gate drive. The gate drive is galvanic insulated between input, output and between the two output driver. Consequently the galvanic isolated power supply and op-amp had to be selected. The op-amp has to measure the capacitor voltage with a voltage divider towards ground. The capacitor voltage is a low frequency signal which is constantly positive, therefore the op-amp does not require a high bandwidth. Resulting in the Avago ACPL-C79. This component comes with good documentation and reference design to use it for current or voltage measurements. Lastly the isolated DCDC had to be selected. On the LV side the source voltage is selected to be 5V. For the HV side the switches need a 12V gate drive supply to drive the MOSFETs. The required power rating will depend on the PCB design and the passive components in between the switch and the gate drive. Therefore the components power rating was selected on a later step. The following table lists all the main components.

| # | Component | Component number | Manufacturer | Rating |
|---|---|---|---|---|
| 1 | Gate drive | UCC21520 | Texas Instruments | |
| 2 | MOSFET | STP25N10F7 | STmicroelectronics | Vdss 100V, Id 25A |
| 3 | Capacitor | C45656 | CHENGX | 2200uF 50V |
| 4 | Connector | WJ2EDGR-5.08-2P | Ningbo | 5.08mm 15A |
| 5 | Op-amp | ACPL-C790 | Avago | |
| 6 | DCDC | MDS02 | Mean Well | 5V in 12V out |

Table 5.1: List of main components for power PCB

### 5.1.2. Power PCB design and passive components selection

Following to the selection of the main components the additional passive components and PCB had to be designed. The PCB can be parted in four different areas of circuits. Firstly the gate drive on the HV switch driving side. Secondly the gate drive on the LV side. Thirdly the galvanic isolated measurement and lastly the DCDC converter. This subsection will go trough the design procedure for each of the named sections step by step. The final design files of the PCB can be found in the annex.

#### Gate drive circuit on HV side

On the HV side of the gate drive the auxiliary circuit for the MOSFET gates and the bootstrap is designed. The bootstrap circuit is required for the high side switch as his drain is floating and not connected to ground. As a reference design the documentation from the gate drive is used. The circuit in the reference design was remodelled in Simulink to evaluate the signal quality and therefore finding the right components. Moreover the power rating was calculated and simulated for worst case duty cycle. As upper and lower MOSFET are the same switch the Simulink model was implemented that the gate resistor and capacitor could be tested in the same time as the bootstrap circuit which can be seen on figure 5.2. By that design time could be saved. On the left side of the black line the bootstrap circuit is represented whereas on the right side the gate drive circuit is shown.

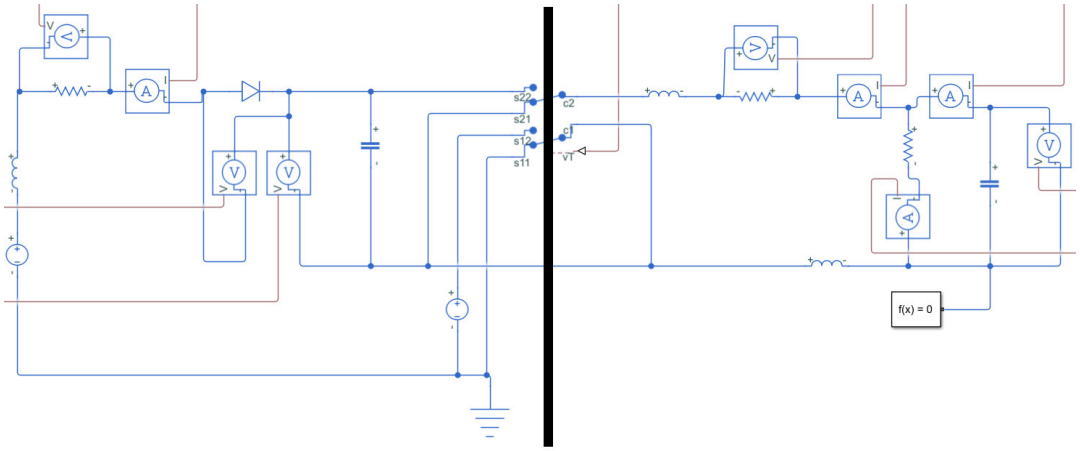



Figure 5.2: Gate drive Simulink model

The gate drive circuit on the right consists of the gate capacitor, parasitic trace inductors and two gate resistors. For the parasitic trace inductance the rule of thumb is applied which says about 5nH per 10mm. Resulting in a inductance value of 15nH for each. The gate capacitance can be looked up from the data sheet and is for the proposed switch 920pF. The two resistor are first a pull down resistor which is placed close to the switch and second a gate turn on and off resistor. In the datasheet of the switch a 4.7 Ohm resistor is used. To lower over shoot and damping the effect of the parasitics a 7 Ohm resistor is proposed. Together with a 5.1 kOhm pull down resistor it showed the best performance in the simulation of the circuit. After selecting the components for the gate drive the bootstrap components were specified. The bootstrap circuit consist of the bootstrap diode and resistor as well as a couple of capacitor to store the energy for the switch. The bootstrap resistors limits and damps the current charging the bootstrap capacitors and therefore is selected according to the diode maximum current. In this case a schottky diode with a maximum current of 2A and maximum dc blocking voltage of 150V was selected. To limit the current bellow 2A a 5 Ohm resistor is used. Thereafter the bootstrap capacitor was chosen that it keeps the gate voltage over 10V at a maximum duty cycle of 98%. The required capacity validated with the simulation resulted in minimum of $5\mu F$. The following table 5.2 gives an overview of the components and their rating.

| # | Component | Rating | Unit |
|---|---|---|---|
| 1 | Gate resistor | 7 | Ohm |
| 2 | Gate pull down resistor | 5.1 | kOhm |
| 3 | Bootstrap Schottky diode | 2 / 150 | A / V |
| 4 | Bootstrap resistor | 5 | Ohm |
| 5 | Bootstrap capacitor | 5 | $\mu F$ |

Table 5.2: Components for HV gate drive side

### Gate drive circuit on LV side

The focus on the gate drive LV side is to to filter the signal and supplying the gate drive. The components were selected based on the reference design in the data sheet. Texas instrument (TI) [46] gave boundary conditions for the maximum and minimum value of the components. The designed low pass filter at the inputs generate propagation delays which is in this application not a problem as the submodules will have a switching frequency around 1 kHz. Figure shows the proposed circuit by Texas Instruments which was used to select the components.

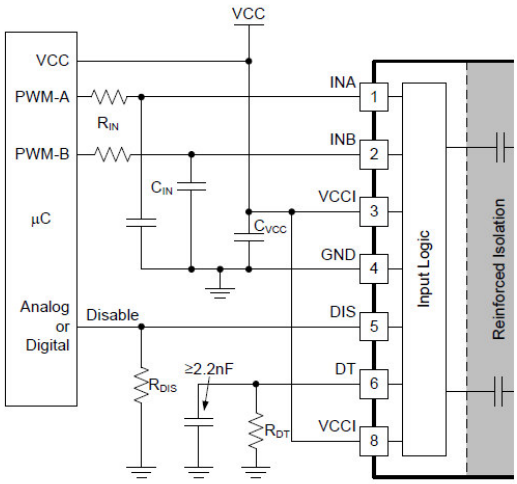



Figure 5.3: Gate drive LV side circuit by Texas Instrument [46]

The disable (DIS) and dead time (DT) inputs are used to first shut down the IC and second to set a dead time between the outlets. The disable input can be connected to the outlet of the $\mu C$. For this application the possibility was left open with an extra two pole male header which is for the beginning short cut with a jumper. The dead time inlet has a 2.2 nF capacitor in parallel with a 7.15k Ohm resistor which results in a deadtime of about 70ns, the capacitor in parallel is used to achieve a better noise immunity. The capacitor Cvcc is recommended by TI to be higher than $1\mu F$ and therefore a $4.7\mu F$ capacitor was selected. The two input filter between the $\mu C$ and the gate drive are identically designed. TI recommends values for Rin between 0 and 100 Ohm and 10 to 100 pF. The maximum values for both components were selected. The following table 5.3 gives an overview of the selected components and their value.

| # | Component | Rating | Unit |
|---|---|---|---|
| 1 | PWM noise filter resistor | 100 | Ohm |
| 2 | PWM noise filter capacitor | 100 | pF |
| 3 | Gate drive power supply filter capacitor | 4.7 | $\mu F$ |
| 4 | Dead time set capacitor | 2.2 | nF |
| 5 | Dead time set resistor | 7.15 | kOhm |

Table 5.3: Components for the gate drive LV side

### Galvanic isolated voltage measurement

For control purposes the $\mu C$ needs to read out the voltage of the submodule capacitor. As the capacitor is floating relatively to the LV ground it requires a galvanic isolation between measurement and the $\mu C$. The selected op-amp ACPL-C790 of Avago [12] is a differential op-amp and has a input voltage range from -0.3 to 0.3V with an output range between 0 to 2.5 V for each output channel. A voltage divider is used to scale down the voltage of the capacitor. At 100V capacitor voltage the measured voltage at the input of the isolated op-amp is 0.2 V.

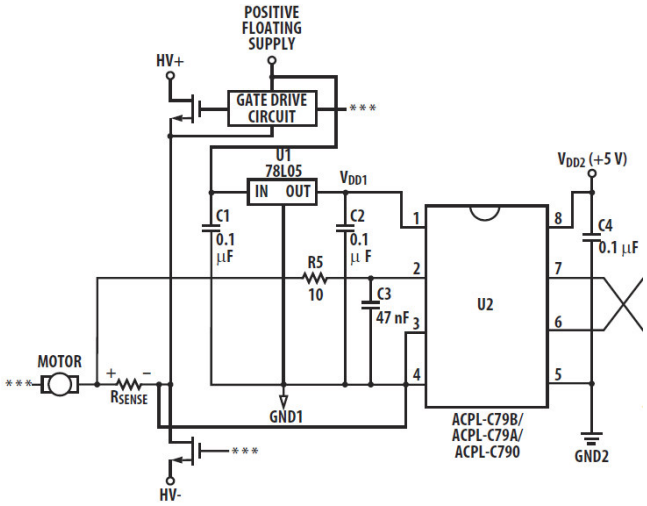



Figure 5.4: Galvanic isolated op-amp for voltage sensing by Avago [12]

Parallel to the measuring shunt of the voltage divider a 47nF capacitor is placed for noise rejection. The supply of the HV side of the op-amp is given by a linear voltage regulator which steps down the voltage from 12V to 5V. For noise rejection and stabilizing the power supplies two 100nF capacitor are used. The proposed designed is based on the reference design by the manufacturer Avago. Figure 5.4 shows the proposed voltage sensing proposed by Avago to measure the current for a motor.

| # | Component | Rating | Unit |
|---|---|---|---|
| 1 | Voltage divider resistor | 20k,10k,100 | Ohm |
| 2 | Voltage divider capacitor | 47 | nF |
| 3 | Linear regulator | 12->5 | V |
| 4 | Linear regulator filter capacitor | 100 | nF |

Table 5.4: Components for the voltage measurement

### Isolated DCDC for supplying power for switching

The input and output voltage of the isolated DCDC was defined by the maximum voltage on the LV side and the required voltage to activate the switches. The power rating was estimated based on simulation done for the gate drive circuit model.

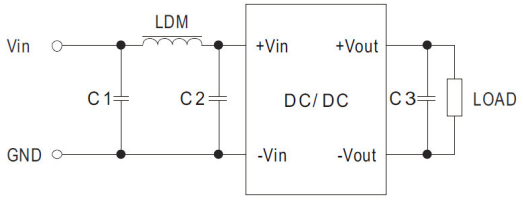



Figure 5.5: Auxiliary circuit for the DCDC converter by Mean Well [37]

For precautionary safety factor was added to have enough power and not driving the DCDC to its limits. Based on the results and the available components a 2W isolated DCDC was selected. The component is produced by the company Mean Well [37] and comes in a SIP7 package and a galvanic isolation up to 4.2kVAC. The manufacturer recommends for EMI reason an in- and output filter which is show in figure 5.5. The following in table 5.5 shown components were selected for the filter.

| # | Component | Rating | Unit |
|---|---|---|---|
| 1 | Capacitor C1 and C2 | 4.7 | $\mu F$ |
| 2 | Inductor LDM | 6.8 | $\mu H$ |
| 3 | Capacitor C3 | 2.2 | $\mu F$ |

Table 5.5: EMI filter components for the DCDC converter

### 5.1.3. Intermediate board

During the design process the decision was taken to use a different DSP platform with another footprint. Therefore a intermediate board had to be designed to make the new DSP platform adaptable to the power PCB. The whole set-up required apart of the power PCBs two current measurement boards. To save time and integrate functions the two current measurement boards were integrated onto two intermediate boards. In the basic version the board had a linear regulator to step down the voltage from 5V to the 3.3V required by the DSP and a precision instrumental amplifier for the voltage measurement signal. The current measurement board has additionally to the before described components an SMD shunt resistor, the same galvanic isolated op-amp and the precision amplifier. As the current signal can be positive and negative an additional dcdc with plus and minus 5V is required for the precision amplifier. The isolated op-amp is feed by the HV 12V on the measurement side. The 12V is stepped down with a linear voltage regulator to 5V. On the other side of the galvanic isolated op-amp the power is supplied by the +/-5V DCDC which powers as well the precision differential op-amp. The current is measured with a SMD power shunt resistor. The advantage of a SMD shunt is its low parasitic capacity and inductivity. All the components are listed in table with the schematic in the annex of this report.

| # | Component | Rating | Unit/Manufacturer |
|---|---|---|---|
| 1 | SMD shunt resistor | 0.02 | Ohm |
| 2 | Galvanic isolated op-amp | ACPL-C79 | Avago |
| 3 | Precision differential op-amp | INA128 | Texas instruments |
| 4 | Linear regulator | 12-5 | V |
| 5 | DCDC | 5->+/-5 | V |

Table 5.6: Components for the intermediate board

### 5.1.4. Arm inductor

The arm inductor for an MMC has two main functions. First of all to limit the DC bus short cut and secondly the circulating current. For the proposed set up the current will be limited by the power supplies. The circulating current is reverse proportional with the frequency of the outlet. Therefore for low frequency operation, additional methods are required to counteract the circulating current. Those methods are not in the scope of this thesis. An Inductor with 4mH is winded. The inductor uses laminated sheets as core material with a core EI66 core size. The inductor has 144 turns and a air gap of 1.9mm. This results in a inductance of 4.18mH. The advantage of sheet metal is the higher magnetic saturation value, this results in a smaller core at similar current rating of the inductor.

## 5.2. Implementation of the SPI bus

The former in subsection 4.3.1 described Simulink model had to be implemented in software. To minimize the complexity of the implementation it was decided to use Simulink and ability of it to directly compile models onto TI $\mu C$. TI offers in an extra toolbox more function blocks which can be use to set interrupts, ADC, DAC

and communication of the $\mu C$. During the implementation software codding issues were found in the generated code and had to be fixed with support from the manufacturer. This resulted in very extensive software fixing procedure and a lot of complications during the implementation process. Nevertheless a working implementation was generated. The main problem are coming from the uncertainty how Simulink implements the model. This resulted in unforeseeable working of the model. The following subsection describes how each submodule was implemented that it was able to work properly. Before describing each implementation the top level decision are explained.

### 5.2.1. Top level architecture for SPI communication for a single phase leg MMC

The SPI bus is implemented in a daisychain configuration as explained in section 4.2. The master is in control of the bus and can control the communication. Therefore the top level control is implemented on the master. This has an additional advantage of higher integration of different controls on same hardware components. Figure 5.6 shows in red the four $\mu C$ which are connected into a daisy chain. The master controller is in charge of sending the mandatory information to replicate the sine wave value on the slave submodules. To do that the master contains a discrete integrator with a fixed integration constant. The value of the integration constant specifies the frequency of the sinusoidal. Consequently, the integrated value is the angle which can be converted into a sine value with a look up table on the master and slave submodules. The knob is used to adjust the amplitude. Additionally for arm energy control the bias between zero crossing of the sinusoidal and the 50% duty cycle can be defined. In this implementation the bias is set to zero which is equal to no arm energy control. The integrator is executed at a higher speed than the PWM cycle to generate a high resolution of the integrator.

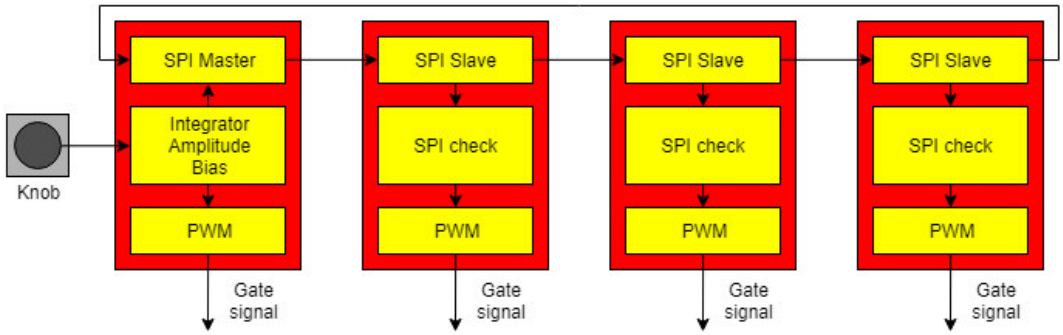



Figure 5.6: System architecture

The slaves in the other hand are triggered by the SPI receive hardware interrupt which is happening simultaneously with the PWM cycle. It is important that all the PWM cycles are in sync. TI has implemented a specific sync out and input therefore. For this implementation the master module sets a sync interrupt based on his PWM cycle and the slaves are restarting their PWM counter when receiving that interrupt. Synchronization of the PWM cycles is hardware based and does not need any computational power and makes it therefore a lot more stable and fault proof.

### 5.2.2. Master module software model

As explained before the master is in control of the SPI bus and the reference signal generation for all the slaves. Figure 5.7 shows the main model in Simulink which is then compiled onto the $\mu C$. The Master has two task to execute. They can be found on the left side of figure 5.7. The upper part consist of the integrator and a modulo operation of its output to generate the angle value for the sinus reference signal. Below that is the voltage measurement of the knob executed with an ADC. This value is used to define the amplitude of the sinus reference. Both are feed into the subtask. The subtask is executed by the PWM Hardware interrupt block which is connected from the top into the block by an arrow. At the output of the subtask is the PWM hardware connected which is receiving the reference value for the PWM modulation. The PWM hardware on the $\mu C$ is set with an up-down counter and therefore he will execute an internal interrupt after finishing every cycle.

The subtask contains the look up table to generate based on angle and amplitude the sinus signal which is

forwarded back to the higher level. This part of the model is shown on the top of the model in figure 5.8. Aside of the sinus reference generation the subtask handles the message generation for the SPI hardware. The amplitude, angle and bias is feed into a Mux block. The block combines multiple information together into an array. The position of the information in the array is very important for the communication. When the subtask is executed the SPI hardware will take the array and send every single information and then shortly pause. During the pause the new message is fed into the shift register of the master whereas the slave can read out their shift register. Every position in the array gets forwarded by a push of the master submodule. The master submodule pushes as many times as the array is long. In this case the array consist of 8 informations. The last submodule in the chain will first get twice an old or dummy message it is important that the message is initiated with a header word (information). The slave will know when it receive the header word that this is the first information in the array. Second information after the header is the phase angle. Thereafter the amplitude which is followed by the bias value. The last four message are dummy messages. Those are required that the master shifts enough times that all the slaves receive all the important messages.

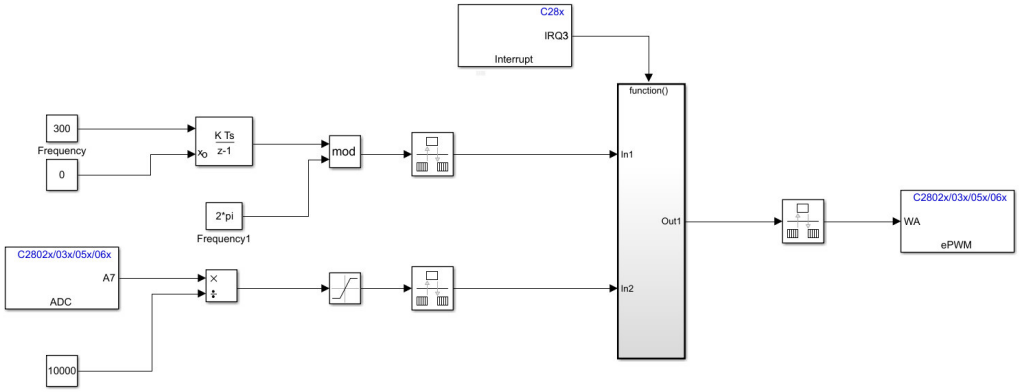



Figure 5.7: Main Simulink model of the master controller

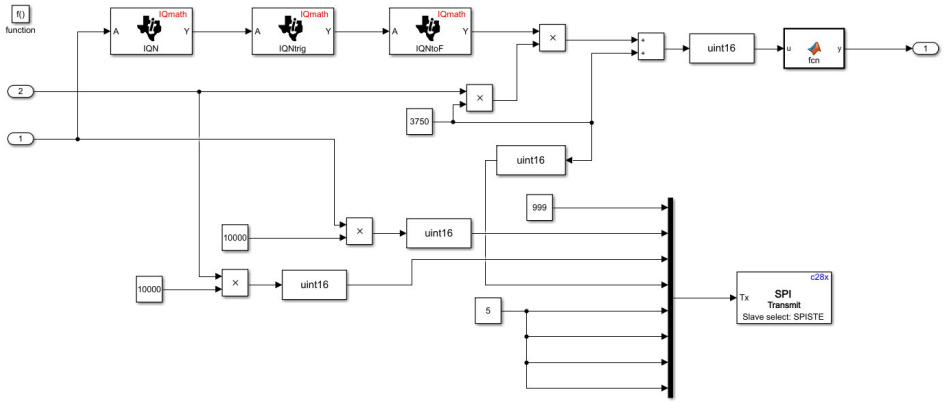



Figure 5.8: Subfunction Simulink model of the master controller

### 5.2.3. Slave module software model

The slave module software has a higher complexity as the master. This higher complexity is resulting from the SPI daisy chain. In the previous master model it is explained that the SPI hardware sends the array word by word. As the first slave will receive the header word first, the location of the important information in the array is equal with that of the master. For the following submodules this is not the case. Therefore the

slave Simulink models are executed with the SPI interrupt. In figure 5.9 the interupt block is connected to a flowchart function. The flowchart function has a single output connected to the PWM with the reference value. The interrupt is executed when the SPI hardware detects that the slave select is pulled low. The slave select pin is only controlled by the master and is used to indicate the transmission of a single information of the array. All the slaves will detect that the slave select gets pulled down 8 times for the 8 informations. Inside the flowchart function the slave receives the information. Than the slave will check every single information for the content, in case it receives the header it will continue to receive the rest of the message. Because the position of the header is know the function which reads out the array knows in which position is required information. Therefore the angle, amplitude and bias are selected to generate the sinus reference for the PWM modulation. In case the word which is received does not contain the header word the function will wait till it receives it. Is that the case it will continue with the before described procedure. The algorithm is shown in figure 5.10.

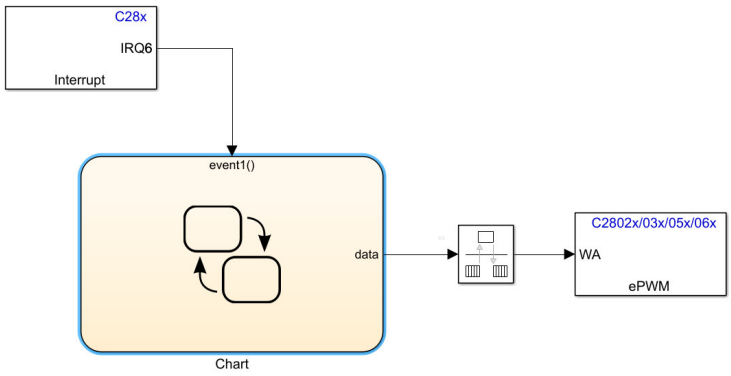



Figure 5.9: Top level task of the slave module

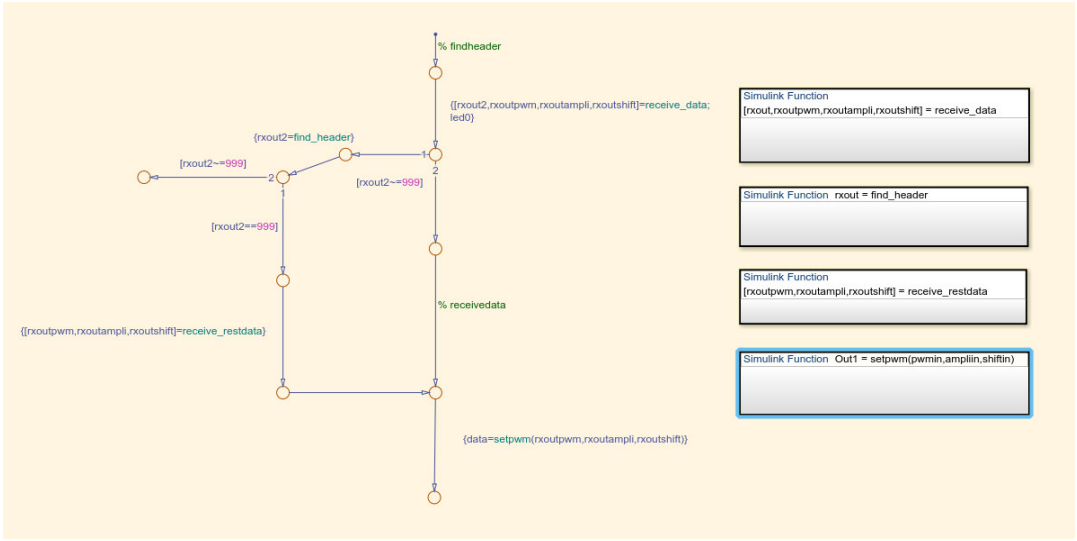



Figure 5.10: State flow process with subtasks

## 5.3. Conclusion of design and build process

The design process was initiated by a list of boundaries to keep the cost and the complexity of the submodule low. Based on the boundaries a conceptual schematic of the submodule was designed. Thereafter the main power electronic components were selected based on their rating. The next step was to sketch the PCB layout

and place the components. Moreover did the power component need auxiliary circuits. Those circuits like the gate drive were simulated on a Simulink model to verify stable operation. In addition to the main power PCB a intermediate board was designed for arm current measurement purpose. This board was not used for this thesis but would offer the possibility for further research. The last component which had to be designed was the arm inductor.

The design and build process was followed by the programming of the $\mu C$. The software architecture was based on the Simulink model designed in chapter 4. The software design phase resulted to be the most difficult and time consuming. Resulting in delays of the thesis and further simplification to operate the MMC. The problem most probably results from using Matlab/Simulink to program the microcontroller which generates a lot of overhead code and lack of clarity what the the compiled model is actually doing. Even a long and intensive correspondence with the Matlab support did not improve the code generation process. For further investigation it is recommended to program in C code instead of using a model based method.

# 6

# Validation of the single phase system

The validation process should proof the working principle of the designed and built MMC single phase system in a open loop control operation mode. To verify the operation of the bus only one variable can be changed during operation with the knob. This reduces the failures modes but still can prove the correct operation of the system. Therefore the amplitude was selected as it is directly related to the output power. The advantage of using phase shifted modulation is that no start up procedure is required. This makes the system robust and simple to test. The following chapter first explains the test set-up and then the results.

## 6.1. Experimental set-up

The goal of the experiment is to verify the correct operation of the MMC. The verification requires therefore a measurement of the circulating current and output current in addition with all the voltages of the submodules. To measures all those values two oscilloscope with four inputs each were used. The first oscilloscope measures with three current probes the output current and upper and lower arm current. The last input is used to measure the voltage over the load. The second oscilloscope was connected to four differential voltage probes to measure each submodule voltage. The set-up was built according to the Matlab Simulink model in chapter 4.3. The physical setup is show. on figure 6.1 with labels for the different components.

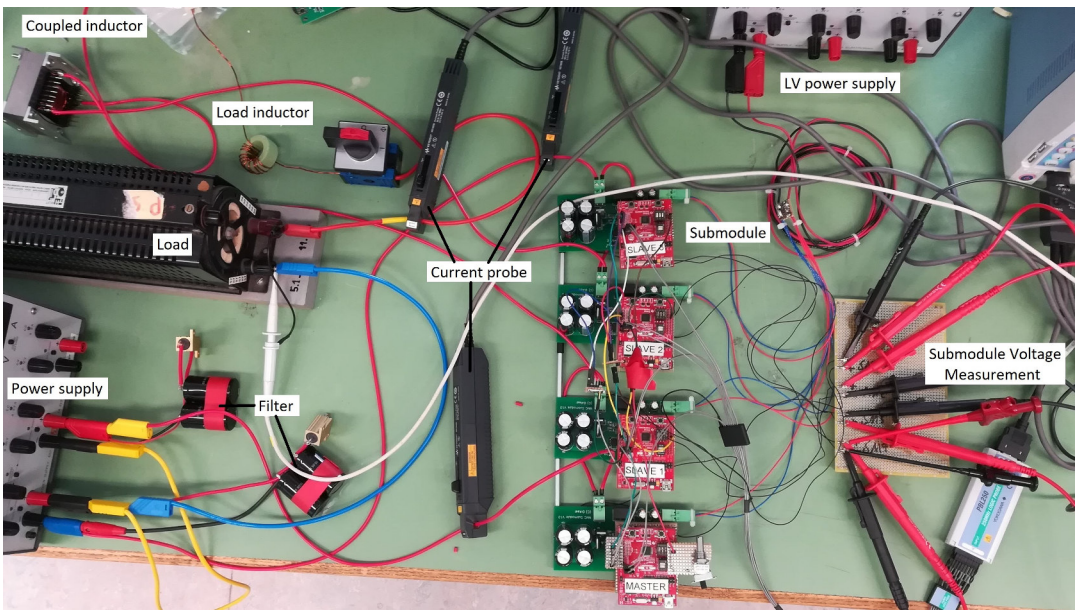



Figure 6.1: Set-up on the lab bench

As the inductivity of the load is not large enough to generate a smooth current signal therefore an additional in-line inductor was wound. The load is a rheostat with a maximum resistance of 5.1 Ohm. In line with the load is a power switch to disconnect the load. At the connection to the load are two filters in parallel. Their task is to take the negative current of the circulating current as the power supply is unidirectional. The supply has two outlet which can follow each other in voltage. The maximum voltage of the small supply is 20V at 2.5A. The $\mu C$ are powered by a single LV power supply with 5V. The start-up of the system was done in the following procedure.

- Disconnect the load
- Amplitude zero
- Power up LV power supply
- Start modulation of the submodule
- Power up HV power supply
- Connect load

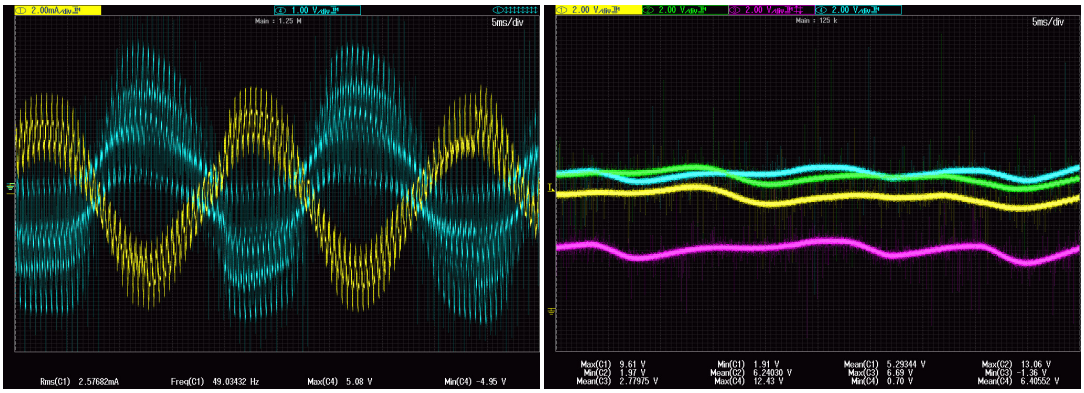
The measurement was done at 10V bus voltage to verify correct operation. The following section shows the results of the measurement. Following table 6.1 shows the specification of the test equipment and settings.

| | Value | Unit |
|---|---|---|
| Modulation amplitude | 0.9 | |
| DC Bus voltage | 10 | V |
| Load resistance | 5.1 | Ohm |
| Load inductance | 0.2 | mH |
| Maximum power supply current | 2.5 | A |
| Maximum power supply voltage | 10 | V |

Table 6.1: Experimental settings and specification of the test equipment

## 6.2. Results

In a first step the voltage and current waveform over the load is measured. Figure 6.2a shows the voltage and current waveform in blue respectively yellow. The waveform represents a sine wave at 50 Hz as configured on the master submodule. As the maximum and minimum voltage are nearly equal it shows that the generated waveform is also symmetrical. This initial measurement proved the system to work accordingly to its setting. Therefore it was tried to increase the voltage at the DC bus. Apart of having problems resulting from the negative circulating current the waveform became irregular from the waveform at lower power. Therefore in a next step the source for that irregularity was searched.




(a) Load current and voltage waveform

(b) Submodule voltage waveform

Figure 6.2: Current and voltage waveform for load and submodule capacitors

### 6.2.1. Identifying problems

On closer examination it can be seen that the waveform contains inconstancies for both the current and voltage waveform. Additionally it can be seen that the current varies over 2mA for a peak value of 5mA. For further identify the reasons of the anomalies the submodule voltage waveform was analysed. The figure 6.2b shows the voltage waveform of the submodules. It can be seen that two of the four modules are operating with similar mean voltage and the other twos are not at the same voltage. One module is below half the voltage it should have. The submodule can only have lower voltage if there is a malfunction with the switch or control of the switch. In a first step the correct operation of the gate drive and switch was tested which resulted to be correctly. Therefore a logic probe was connected to the $\mu C$ to measure the signal to the gate drive. Single measurement were conducted to analysis the signals of all the slaves. The analysis showed that sometimes the second and third slave randomly stop to set the duty cycle correctly. What they do instead is completely open one switch and close the second switch for a couple of PWM cycles. This results in reduction of the average voltage of the submodules. Figure 6.3 shows the measurement. The upper 8 signals in blue are coming from the logic probe and show the PWM signal for upper and lower switch from every submodule. The lower two signals are the master and towards the top the first, second and third slave follow. The signals appear very noisy on the oscilloscope which could lead to faulty switching. Therefore the signals on the traces to and from the gate drive where separately measured without a logic probe and showed no noise. The designed PCB has a filter in between the $\mu C$ and the gate drive to reduce that problem. Therefore the switch has to be set intentionally wrong by the $\mu C$. To specify if it is a problem of all the slaves, multiple measurements were made and showed that only the second and third slave are suffering from the problem. The problem is more sever on the third slave than the second. This is conflicting with the fact that all the three slaves uses the absolute identical software. Therefore the message handling on the slave submodule still does not perform correctly. The only difference between the slaves is the position of the information in the received array. The implemented algorithm in the flow chart function could be one source of the problem. Second possible source could be electrical interference of the experimental set-up which corrupts the signals.

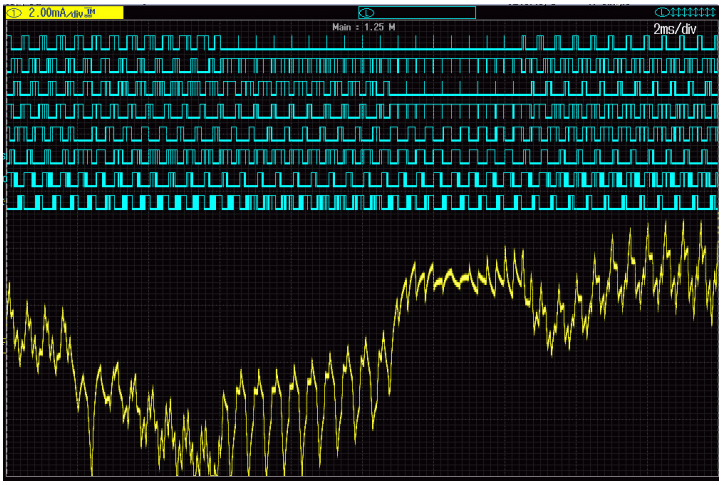



Figure 6.3: Investigation shows the faulty switching behaviour of two submodule

### 6.2.2. Suggestions

The validation shows that for robust operation a sanity check is required. During the implementation process other possible workarounds were elaborated but not implemented. One of the possibilities would be that the master pushes as many words trough till he receives it back for a check. This check could show if the slave or the electrical interference affect the message. Apart of implementing a sanity check and updating the software maybe Simulink itself generates the faulty code. The code composing part which is happening in Simulink showed glitches during the implementation process. Matlab Simulink was so kind to help out in short time with updates for the code composer. Still maybe for a more detailed and complex system it would make sense to write the code directly in C. The testing on higher power level had to be aborted because of the unstable operation. As the time was limited and first results were generated it was decided to not further invest time to solve problem.

## 6.3. Conclusion of the validation

To start the validation a the experimental set-up was built and a start-up procedure planned. The measurement were conducted under low DC bus voltage to avoid destructive operation resulting from malfunction. The generated results shows that an open loop operation with phase shifted modulation proved to be working accordingly with the Simulink results shown in chapter 4. By that it is shown that the SPI is capable of controlling a single phase MMC system made of four submodules. However the implemented software showed instabilities of sending the reference to the last two slaves. This resulted in missing PWM modulation on those two submodules which made it impossible to test the system at higher power. Therefore the system was analysed for the possible source of the error. All the gate drives and signals from the $\mu C$ showed a correct behaviour. Also the signals on the SPI showed the correct content. Therefore two possible sources could lead to the error. Firstly the software on the submodule or secondly the electromagnetic interference. Those two sources were not resolved during this thesis.

# 7

# Conclusion and recommendation

The United Nations decided to limit climate change in the Paris climate agreement. Based on the agreement the member states developed strategies to reduce their greenhouse gas emissions. Therefore a big focus is set on the transportation sector as it makes 14% of the total greenhouse gas emissions. One way to reduce the emissions is by electrification of the drive train. Automotive companies already presented their first generation of electric vehicle. With the goal to further improve efficiency and cost, new drive train topologies are developed. In this thesis the focus is set on the modular multilevel converter. The modular design together with the advantage of multiple levels and low voltage components makes the topology attractive for drive application. In the first chapter it is shown that common multilevel topologies require the same amount of power electronic component as the MMC at equal number of levels. This simple comparison shows that the complexity and resulting higher cost come from the hardware and software and or the auxiliary components such as gate drive power supply. Therefore in the second chapter the state of research was conducted to define the research contribution for this thesis. It was concluded that introducing an alternative to optic fibres with a centralized controller would lead to a further integration of the system and improve redundancy of the converter. By distributing the control over the submodules less connections can be established and the employed hardware requires less inputs and outputs. Based of that conclusion the research questions were established. The following section will recapitulate the method which was used to answer each question.

## 7.1. Distributed control based on low level communication protocol

The first research question is if distributed control can be implemented with a low level communication bus. This question goes in hand with the question which communication protocol qualifies for the MMC and what are the limitation. To answer that question it was decided first to replicate distributed control into a Simulink model to identify the information which has to be exchanged for a stable operation. Thereafter different bus protocol which are most widely available are compared.

The analysis showed that SPI in a daisy chain configuration results to be the best option because of the bit rate. The bit rate as shown is very crucial for the operation as the time to distribute the reference signal to the slaves limits the switching frequency of each submodule. It was shown that with SPI a single phase MMC with 5 level can be built with a resulting switching frequency of up to 375 kHz whereas I2C reaches its limit already at 9.195 kHz. This is all the more important for high speed output frequency operation of the converter for drive application. The switching frequency of the converter should be at least ten times higher than the motor output frequency to guarantee a smooth current waveform which results in low motor losses.

Therefore it was decided to build a experimental set-up based on the SPI bus protocol to verify the first question. The reason why it was decided to built an experimental set-up is to initiate a baseline for further research on distributed control with SPI as well as to showcase the simplicity of the set-up. To do that it was decided to use adorable and well known components to first of all avoid the chance of uncertainties in the commissioning phase and secondly to demonstrate the simplicity.

The open loop control algorithm was programmed with Simulink onto a TI launchpad micro controller. This TI launchpad offers very high performance (60 MHz CPU, 8 PWM channels, 12 bits ADC) for a very econom-

ical price. Therefore every submodule used one launchpad module.

The resulting experimental set-up consist of four absolutely identical submodules. The difference is only in the software programmed onto the launchpad modules. To proof if distributed control works with SPI a master module was defined. The master modules generates the reference waveform and is in charge of controlling the communication bus. The slave submodules on the bus sets depending on the reference signal the duty cycle. The results from the validation show a correct operation of the single phase system and therefore answers the first research question. However the software was very unstable and showed malfunction. Therefore it was not possible to run the converter to its power limits. The reason for the unstable software is resulting from the Simulink implementation. The code generation process was studied to understand the source of errors and to remove the malfunctions. The whole error finding and correction process was done in cooperation with the help of the Matlab support team but did not lead to a better solution. As basis operation was reached and further improvement was not foreseeable it was decided to stay with the present solution and recommend for further research to directly code onto the hardware without using a code generation software.

It was possible to answer the remaining research questions. The experimental set-up showed clearly the advantage of using a communication bus instead of a centralized configuration. The submodules have all identical inputs and outputs and are therefore easy to scale without any further hardware adoption. Further advantage of using the SPI bus in a daisy chain is the simplicity of the hardware, most micro controller have specific SPI integrated hardware and the bus consist only of four wire connection. The communication bus with the identical submodule leads to a high degree of integration in comparison with optic wire implementations. The resulting set-up is a baseline for further research of integrating the MMC to open up application which are not possible with recent size of the system.

## 7.2. Recommendation

The recommendation are separated into two fields depending on the focus of the application. The first field is the fully modular MMC. A fully modular MMC describes a system where the modules can be put together and they automatically can operation without extensive software adaptation, for the operation the master devices uses the bus for the system identification. The system designer only has to program the master what operation mode it has to work. For example as a single phase PV inverter or as a 9 phase motor drive. The designer can therefore built a power converter for a wide range of power and voltages without the need to redesign the hardware. Additionally every module could take control of in case a master module fails to operate which would lead in result to a very high level of redundancy.

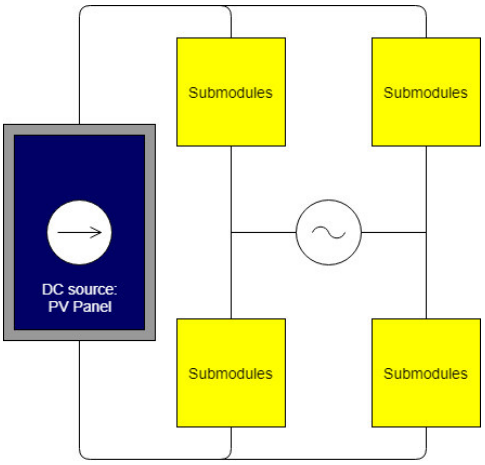



Figure 7.1: Single phase PV inverter example

The second field is the application of the set-up where redundancy and lifetime is important. The same system can be designed onto a single PCB as a fully integrated inverter. The advantage of using distributed control with the SPI bus is that in case a module fails even though it could be the master module the slave could take over the operation. This leads to higher redundancy and higher lifetime. Possible application

could be PV inverter as shown in figure 7.1 where low maintenance and long lifetime are selling points. For both fields this thesis built the baseline for both direction. The implemented hardware can be used to design both concept and show the business viability of such a system.

# A

# Appendix - PCB schematic and layout

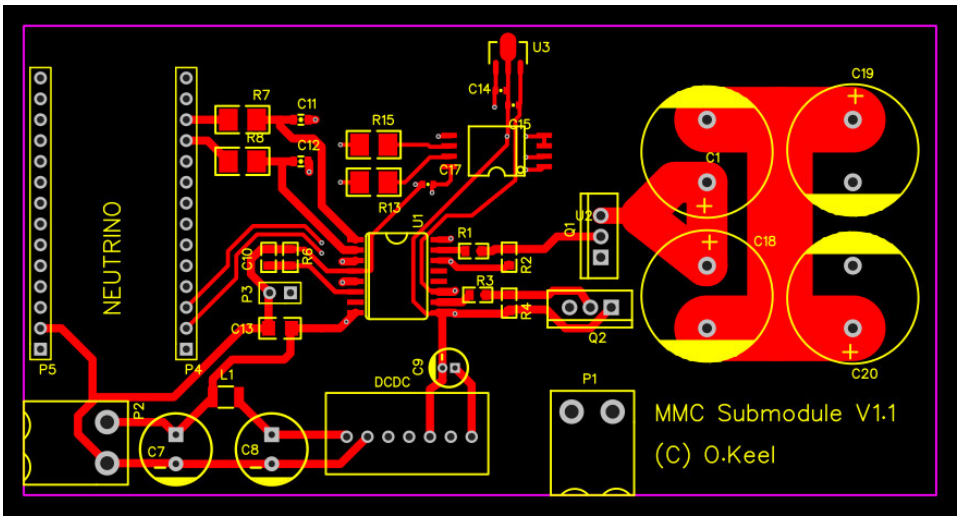



Figure A.1: PCB top layer

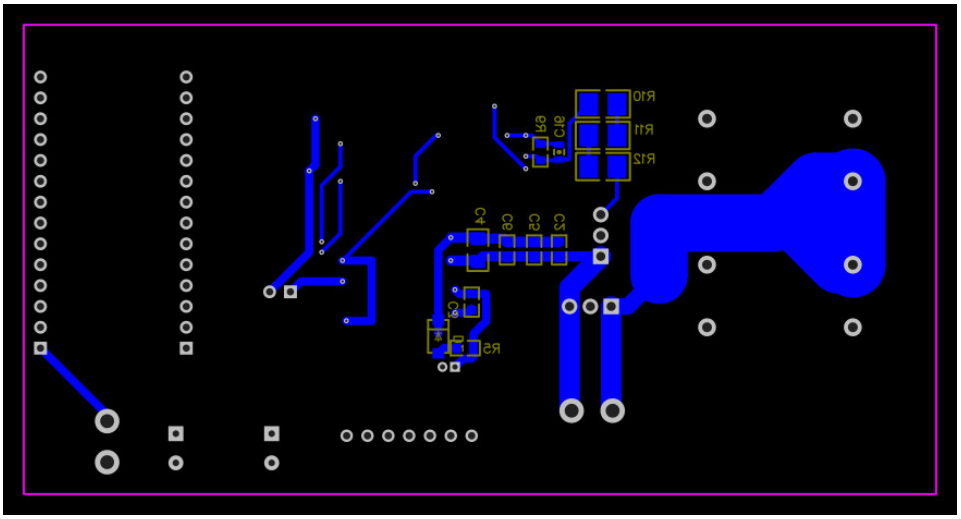
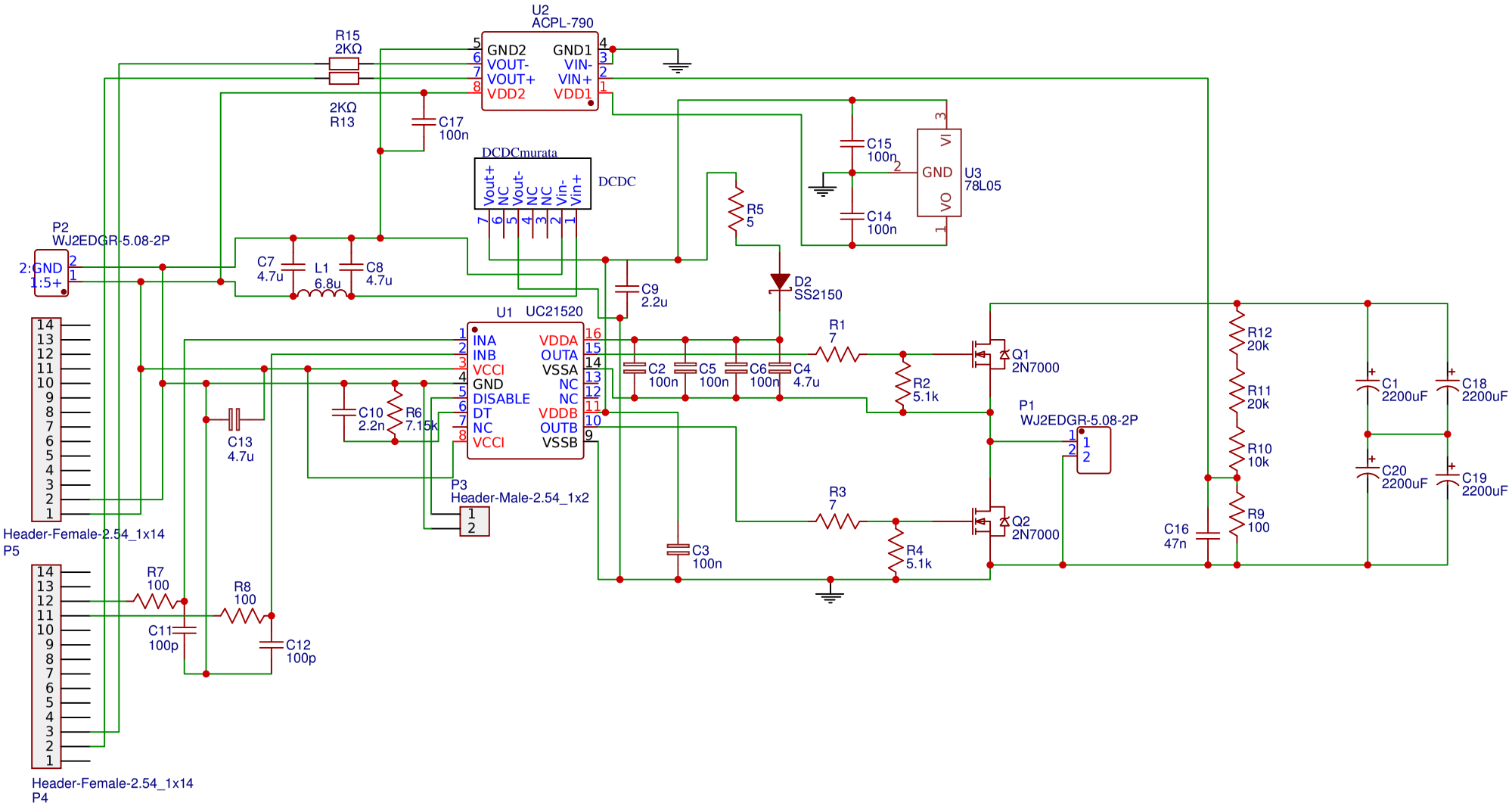


Figure A.2: PCB bottom layer

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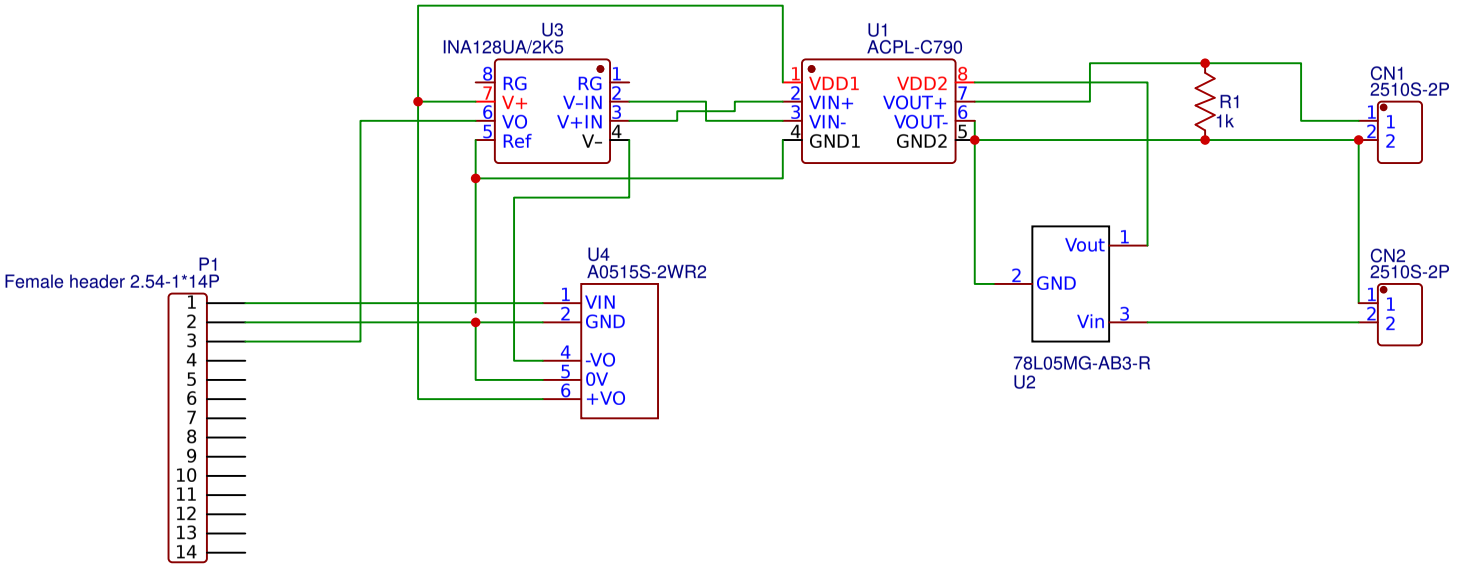


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