A 0.96-mW dB-Linear Variable Gain Amplifier With 0.4-dB Linearity Error Over a 62.4-dB Gain Tuning Range

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DOI
10.1109/LSSC.2022.3213055

Publication date
2022

Document Version
Final published version

Published in
IEEE Solid-State Circuits Letters

A 0.96-mW dB-Linear Variable Gain Amplifier With 0.4-dB Linearity Error Over a 62.4-dB Gain Tuning Range

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***Abstract*—This letter presents a low-power dB-linear variable gain amplifier (VGA) with a small linear-in-dB error over a wide gain tuning range. An exponential current ratio is realized in the linear-in-dB control circuit based on the subthreshold I–V characteristic. The VGA is built with subthreshold common-gate transistors as current steering, accurately replicating the exponential current ratio and forming a tunable gain. Implemented in 55-nm CMOS technology, the proposed VGA occupies a compact active area of 0.011 mm^2 excluding the buffer. It achieves a linear-in-dB error of 0.4 dB over a gain tuning range of 62.4 dB, corresponding to the state-of-the-art relative error of 0.6%. The proposed design shows constant 80-MHz bandwidth with a power consumption of 0.96 mW.**

***Index Terms*—Gain tuning range, linear-in-dB, low error, low power, variable gain amplifier (VGA).**

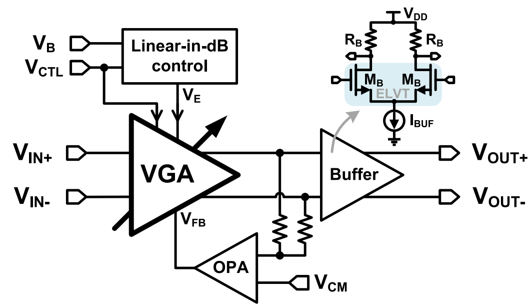

Fig. 1. Architecture of the proposed VGA.

I. Introduction

Variable gain amplifiers (VGAs) are widely adopted in analog front ends for wired and wireless communication systems [1]. With the proliferation of advanced portable devices, a low-power VGA is required to extend battery life. Besides, many applications, such as GPS and many mobile digital television standards, require a wide gain tuning range of over 60 dB with high linear-in-dB accuracy [2], [3].

Numerous dB-linear VGA topologies have been developed in previous works. Pseudo-exponential VGAs are widely used to obtain dB-linear characteristics [4], [5]. By using a single-branch negative exponential generator (NEG), the VGA in [4] achieves a gain tuning range of 40 dB with a linear-in-dB error of ±1 dB. To improve the gain range, the work in [5] includes additional compensated negative pseudo-exponential generation (C-NPEG), resulting in a gain tuning range of 51 dB with ±1-dB error. This comes at the expense of circuit complexity and power consumption, making gain ranges above 60 dB difficult to achieve and unsuitable for low-power applications. Open-loop VGAs in previous works typically attain gain variations by adjusting either the equivalent input transconductance [6], [7] or the active load [1], [8]. For example, the designs in [6] and [7] adjust the current of the input differential pair based on the current steering technique, attaining 51-dB gain tuning range with ±0.65-dB error and 40-dB gain tuning range with ±1-dB error, respectively. By tuning the active load, the designs in [1] and [8] achieve gain variations. However, regulating the load resistor has a direct impact on the dominant pole, which, in turn, has an impact on the bandwidth (BW).

This letter presents a low-power VGA with subthreshold common-gate transistors co-designed with a linear-in-dB control circuit, realizing a wide gain tuning range with an ultralow linear-in-dB error. The VGA achieves a constant BW of 80 MHz and a low linear-in-dB error of 0.4 dB over a 62.4-dB gain tuning range, consuming only 0.96 mW at the maximum gain.

II. Proposed Architecture and Circuit Design

Fig. 1 shows the architecture of the VGA. To minimize the power consumption, a single-stage VGA with common-mode feedback is proposed. The VGA gain is adjusted by a linear-in-dB control circuit. An output buffer with unity gain and 100-Ω differential output resistors is used to mimic the load in system integration and also facilitate the measurement. M_B has the aspect ratio of 10.8 μm/60 nm, which uses an extremely low threshold voltage (ELVT) transistor considering the low common-mode voltage.

A. VGA Gain Stage

The proposed single-stage VGA with a modified current steering technique is illustrated in Fig. 2. The amplifier is based on a modified folded cascode structure. To obtain linear-in-dB gain control, the output current is split into two parts (M5 and M6), which are adjusted by the gain control voltages V_{CTL} and V_E, respectively. The VGA gain is calculated as

$$A_V \approx -g_{m1} \cdot (R_1//R_2) \frac{I_{ds5}}{I_{ds5} + I_{ds6}} \tag{1}$$

where g_{mi} and I_{dsi} are the transconductance and drain current of transistor Mi, respectively.

Unlike other current-steering-based VGAs in [1], [6], [7], and [8], this topology maintains constant g_{m1} and $R_1//R_2$ when the gain is adjusted. Therefore, the only factor to adjust A_V is the ratio of I_{ds5} and I_{ds6}, which is replicated from the linear-in-dB control circuit using size-proportional subthreshold transistors, as described in the following section. If there is more than one device in the path from

Manuscript received 9 June 2022; revised 7 September 2022; accepted 3 October 2022. Date of publication 10 October 2022; date of current version 11 November 2022. This work was supported by the 2021 1st Key Science and Technology Program of Ningbo City under Grant 2021Z087. This article was approved by Associate Editor Seung-Tak Ryu. *(Corresponding author: Zhenghao Lu.)*

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Digital Object Identifier 10.1109/LSSC.2022.3213055

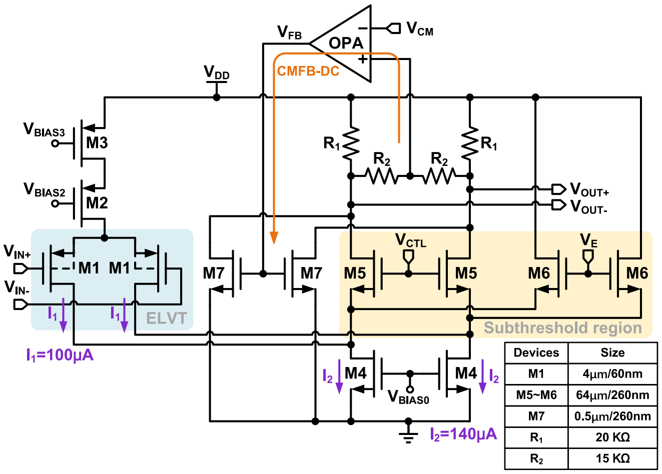


Fig. 2. Schematic of the proposed VGA with common-mode feedback.

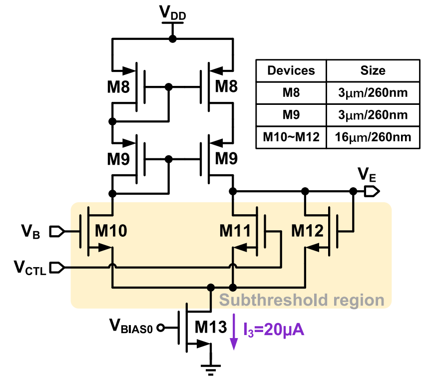


Fig. 3. Schematic of the linear-in-dB gain control circuit.

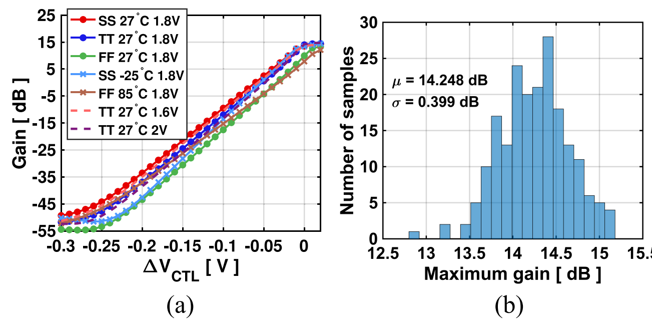


Fig. 4. (a) Simulated gain variations over different corners, temperatures, and supply voltages. (b) Simulated maximum gain histogram based on 200 Monte Carlo results.

generating exponential currents to replicating them into the VGA, the gain tuning range is determined by the device with the smallest tuning range. The proposed design simplifies the current replication path; hence, the gain tuning range is determined simply by the tuning range of the subthreshold transistors in the circuit, all of which have similar operating states. To maintain precise current replication at different common-mode voltages, cascode transistors M2 and M3 are used at the expense of supply headroom. Operating under a 1.8-V supply voltage, ELVT transistors are adopted in the input differential pair M1 to ensure that the input and output have the same common-mode voltage.

To achieve a constant BW and a precise dB-linear gain relationship in (1), a stable output impedance under different gain settings is necessary. The output resistance is described as

$$R_{\text{out}} = R_1//R_2//r_{o7}//\left[g_{m5} \cdot r_{o5} \cdot \left(r_{o1}//r_{o4}//\frac{1}{g_{m6}}\right)\right] \tag{2}$$

where r_{oi} is the output resistor of transistor Mi. In this work, by properly reducing $R_1//R_2$, the VGA's output resistance can be simplified as $R_1//R_2$ as described in (1). For a fixed common-mode voltage, a small R_1 results in a large current. Therefore, instead of reducing R_1, the common-mode sense resistor R2 is set to a small value of 15 kΩ to further reduce power consumption.

A common-mode feedback loop is used to stabilize the output common-mode voltage (VCMO) over the entire gain range. It consists of R_2, M7, and OPA. Thus, VCMO is well defined by the preset V_{CM}, which can be adjusted from 600 to 800 mV. This is also the range of the input common-mode voltage.

B. Linear-in-dB Gain control

The linear-in-dB gain control circuit is illustrated in Fig. 3. It is based on a modified telescopic amplifier, whose input transistors (M10 and M11) are controlled by V_{CTL} and a constant bias voltage V_B. A diode-connected transistor M12 is introduced to share current with M11, providing the relationship $I_{ds10} = I_{ds11} + I_{ds12} = 10\ \mu$A. M8 and M9 form a cascode current mirror, ensuring that this current relationship is accurate and insensitive to variations in V_B and V_{DD}. In this design, M10–M12 are biased in the subthreshold region to achieve exponential I–V characteristics. For both the VGA and the linear-in-dB control circuit, there is

$$\frac{I_{ds5}}{I_{ds6}} = \frac{I_{ds11}}{I_{ds12}} = \exp\left(\frac{V_{CTL} - V_E}{nV_T}\right) \tag{3}$$

where V_T is the thermal voltage kT/q, and n is the subthreshold slope parameter $dV_{gs}/d\lg I_{ds}$. Therefore, the ratio of I_{ds11} and I_{ds12} is precisely replicated into the VGA. With the relationship of $(W/L)_{5,6} = 4 \cdot (W/L)_{11,12}$ shown in Figs. 2 and 3, the current $I_{ds5} + I_{ds6}$ is set to 40 μA by I_1 and I_2 to optimize replication. The VGA gain in (1) is further calculated as

$$A_V = -g_{m1}(R_1//R_2)\frac{I_{ds11}}{I_{ds10}} = -g_{m1}(R_1//R_2)\exp\left(\frac{\Delta V_{CTL}}{nV_T}\right) \tag{4}$$

where ΔV_{CTL} is the input control voltage ($\Delta V_{CTL} = V_{CTL} - V_B$). Therefore, the VGA gain in dB is linearly tuned by ΔV_{CTL}. To improve the gain tuning range, high threshold voltage (HVT) transistors are used for all subthreshold transistors so that they can remain in the subthreshold region over a wide ΔV_{CTL} range.

Fig. 4(a) depicts the VGA gain variations under different PVT scenarios. The variations in buffer gain are de-embedded. As shown in (4), the maximum gain is decided by $-g_{m1}(R_1//R_2)$. The gain slope varies with temperature due to V_T, which is proportional to the temperature. Parameter n varies slightly with process corners and temperatures, causing the gain slope to change slightly. Besides, the gain is insensitive to V_{DD} variations. For all PVT scenarios, the VGA gain achieves high dB-linearity and a wide gain tuning range of over 60 dB. Fig. 4(b) shows the Monte Carlo results for the maximum gain, accounting for process variation and mismatch.

III. Measurement Results

Excluding the output buffer, the fully integrated VGA occupies a core area of 0.011 mm^2 in 55-nm CMOS technology, as shown in Fig. 5. Fig. 6 is the printed circuit board (PCB) for measurement. Based on two off-chip transformers ADT 2-1T and 100-Ω off-chip resistors in parallel with DUT input, the system achieves

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER DESIGNS

Parameter	**This work**	[5] TMTT'21	[9] ISSCC'16	[6] TCASI'19	[1] JSSC'15	[8] TMTT'16	[10] SSCL'18
Technology (nm)	55 CMOS	40 CMOS	180 CMOS	55 CMOS	180 CMOS	65 CMOS	130 CMOS
Gain range (dB)	-49.2 ∼ 13.2	-34 ∼ 17	15 ∼ 66	-37 ∼ 14	3.6 ∼ 59.6	2 ∼ 24	-20 ∼ 21
Gain tuning range (dB)	**62.4**	51	51	51	56	22	41
Linear-in-dB error (dB)	±0.4	±1	±0.6	±0.65	±0.3	±0.3	±0.6
Relative error[a]	**0.6%**	2.0%	1.2%	1.3%	0.5%	1.4%	1.5%
-3 dB BW (GHz)	0.08	7 ∼ 8	0.05	0.74	0.0635	2	0.58
Constant BW	Yes	Yes	Yes	Yes	No	No	No
Noise figure (dB)	24.4[c]	30.5[c]	27.6[b]	30	27.5[bc]	24 ∼ 29	27 ∼ 41
Input P1dB (dBm)	-12.9[c]	-25[c]	-37	-22[c]	-62.6[c]	-22.2[c]	-33[c]
Voltage supply (V)	1.8	1.1	1.8	1.2	1.8	1.2	1.2
Power (mW)	0.96[c]	27.06	0.42	2.49[c]	1.12	3.48	4.98
Core area (mm^2)	0.011	0.038	0.03	0.033	0.07	0.01	0.1
FoM1[d] [5], [11]	472.8	384.4	202.4	459.3	45.4	1264.4	47.8
FoM2[e] [10]	5.2	14.61	6.1	15.2	3.18	12.6	4.8

[a] Relative error = Linear-in-dB error / Gain tuning range (dB/dB). [b] Derived from the input-referred noise (IRN). [c] Maximum gain.
[d] $FoM1 = \frac{BW(GHz) \times dB\text{-}Linear\ Gain\ Range(dB)}{Power(mW) \times Active\ Area(mm^2)}$. [e] $FoM2 = \frac{BW(GHz) \times Gain\ Range(dB)}{Power(mW)}$.

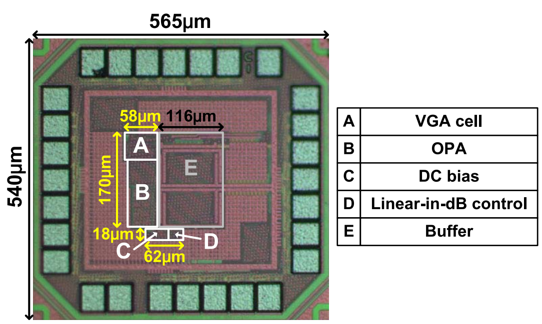


Fig. 5. Chip micrograph of the proposed VGA.

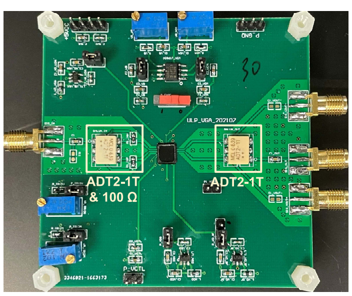


Fig. 6. PCB photograph of the proposed VGA.

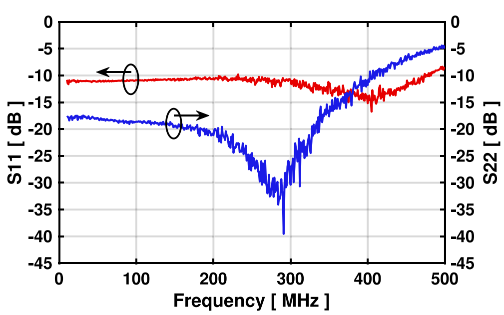


Fig. 7. Measured S11 and S22 of the proposed VGA.

good impedance matching (<−10 dB) within 400 MHz, as shown in Fig. 7. The measured gain and liner-in-dB error versus ΔV_{CTL} are shown in Fig. 8 and compared to the post-layout simulation results.

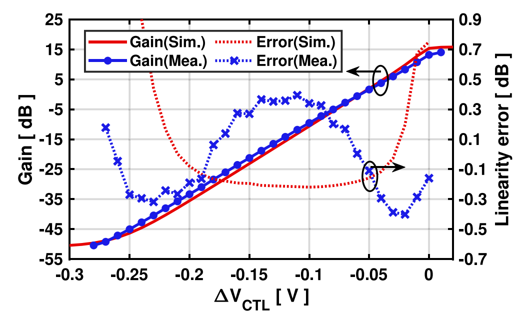


Fig. 8. Measurement and post-layout simulation results for VGA gain range and linear-in-dB error.

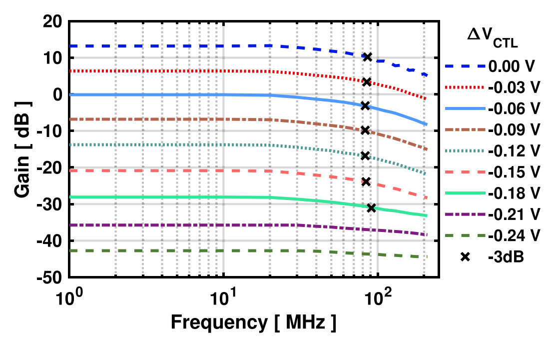
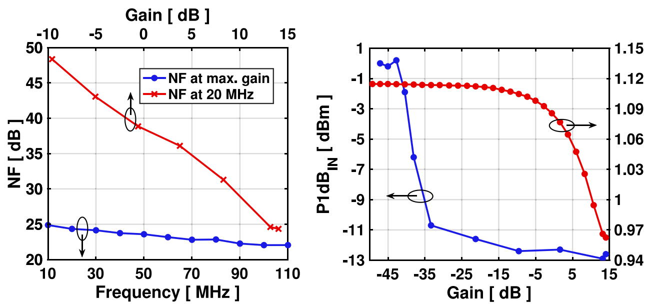


Fig. 9. Measured frequency response under different ΔV_{CTL}.

It shows that the proposed VGA achieves a peak linear-in-dB error of ±0.4 dB over a wide gain range of −49.2–13.2 dB. Fig. 9 depicts the measured frequency response under various ΔV_{CTL} values, which illustrates a constant BW of 80 MHz when $\Delta V_{CTL} \geq -0.18$ V.

Fig. 10(a) depicts the measured noise figure (NF) based on frequency and gain variations. The NF contribution from the buffer can be ignored. At the maximum gain, this VGA shows an NF of 24.9 and 22.8 dB at 10 and 80 MHz, respectively. Fig. 10(b) illustrates the measured input 1-dB compression point (P1dB) and power consumption. The VGA consumes 0.96 mW at the maximum gain. As the gain decreases, the power consumption increases to 1.1 mW because of the increase in I_{ds7} in Fig. 2. The input P1dB ranges from −12.9 to 0.2 dB for different gain settings. Table I presents the performance summary and comparison with other similar designs.



(a) (b)

Fig. 10. (a) Measured NF under different frequency or ΔV_{CTL}. (b) Measured input P1dB and power consumption under different ΔV_{CTL}.

Among the designs with constant BW, the proposed VGA achieves the minimum linear-in-dB error over the maximum gain tuning range, showing a minimum relative error of only 0.6%. It also achieves a low power consumption, a competitive NF and input P1dB, and a comparable figure-of-merit 1 (FoM1) and FoM2.

IV. Conclusion

A low-power VGA with a modified current steering structure was presented in this letter, achieving the maximum gain tuning range and an ultralow linear-in-dB error. The VGA includes subthreshold common-gate transistors that are co-designed with a linear-in-dB control circuit, resulting in the accurate replication of the current ratio and high dB-linearity in VGA gain tuning. At various gain settings, the VGA maintains constant input transconductance and output impedance, resulting in a wide gain tuning range and constant BW. The proposed design achieved a constant BW of 80 MHz with a low power consumption of 0.96 mW at the maximum gain. It also showed a linear-in-dB error of only ±0.4 dB over a wide gain tuning range of 62.4 dB, achieving the state-of-the-art relative error of 0.6%.

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