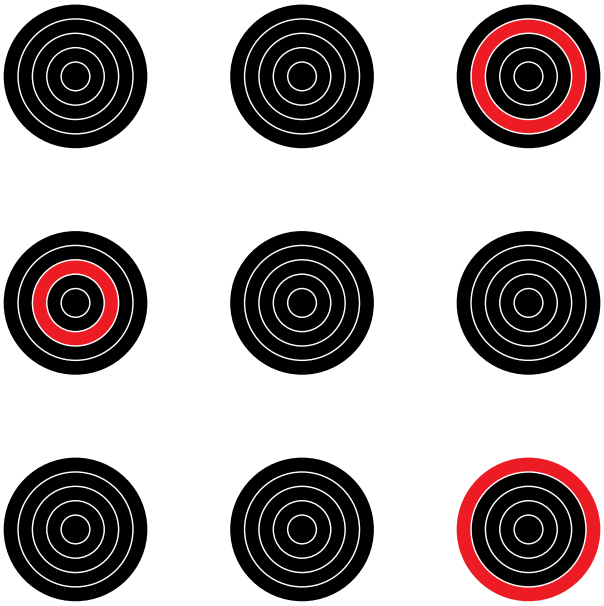
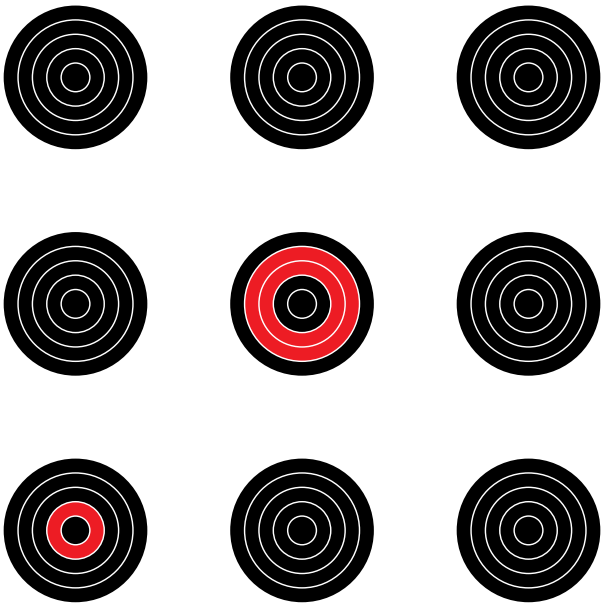


SILICON TECHNOLOGY FOR INTEGRATING HIGH-PERFORMANCE LOW-ENERGY ELECTRON PHOTODIODE DETECTORS

Agata Šakić



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PROEFSCHRIFT

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus Prof. ir. K. C. A. M. Luyben,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen

op woensdag 28 november 2012 om 10:00 uur

door

Agata Šakić
Diplomirani Inženjer Elektrotehnike,
van Universiteit van Zagreb, Kroatië
geboren te Split, Kroatië

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Dr. W. van Noort, Texas Instruments, USA
Prof. dr. E. Charbon, Technische Universiteit Delft, reserve lid

Agata Šakić,
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To my loving parents, Marija and Zdravko

It was the best of times, it was the worst of times, it was the age of wisdom, it was the age of foolishness, it was the epoch of belief, it was the epoch of incredulity, it was the season of Light, it was the season of Darkness, it was the spring of hope, it was the winter of despair, we had everything before us, we had nothing before us, we were all going direct to heaven, we were all going direct the other way - in short, the period was so far like the present period, that some of its noisiest authorities insisted on its being received, for good or for evil, in the superlative degree of comparison only.

Charles Dickens, *A Tale of Two Cities*

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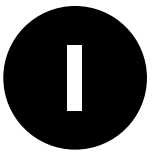
INTRODUCTION



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INTRODUCTION

The work presented in this thesis is centered around the fabrication of silicon photodiode detectors for application in Scanning Electron Microscopy (SEM) systems by using Pure Boron (PureB) technology. This technology was already well-established for the fabrication of ultrashallow p^+n photodiodes for detecting low-penentration depth beams such as vacuum ultraviolet (VUV) light. At 193 nm wavelength the absorption length of the light in silicon is very low, about 5 nm. Similarly low penetration depths are found for electrons with energies below about 1 keV. This is an energy range that had not yet been exploited in SEM systems, but imaging in this range was aspired for significantly increasing the sensitivity to surface topography and material analysis.

The success of the PureB technology as a solution for detecting low-penetration depth beams lies in the fact that it offers a robust photodiode for direct detection of the light or particles. The PureB photodiodes have nanometer-thin p^+ anodes that are sufficiently thin to allow the shallow-penetrating beams to reach the drift region of the diode where the generated carriers can be collected. In principle, Schottky diodes form the most shallow diodes with the light sensitive depletion region extending right up to the silicon surface. However, Schottky diodes are often an unattractive solution for SEM detectors because the reverse leakage current and surface recombination is high, there is reflection and absorption in the front metal as well as a low surface electric field. In contrast, the PureB photodiodes have attractive properties with respect to all these points. They are created by chemical-vapor deposition of a nanometer-thin layer of pure boron that not only creates a p^+-region at the silicon interface, but also forms a robust front-entrance window with a minimum of beam attenuation.

Besides the actual PureB depositions that are used to form the electron-sensitive photodiode itself, several new technological developments were required in order to produce a detector that could meet the demanding specifications set by the SEM imaging systems. A detector was designed that was built up of electrically-isolated, closely-packed PureB photodiodes arranged in annular configurations around a central through-wafer hole. For a sufficiently high scanning speed it was important to also achieve a low series resistance and low capacitance of the individual diode building blocks. Techniques for specially modifying the substrates were developed, either by growing very thick, intrinsically doped epitaxial layers on low-resistivity Si substrates, or by locally-thinning high-resistivity substrates in a manner similar to the approach used for back-illuminated CCDs or CMOS imagers. To lower the series resistance of each PureB photodiode, the patterning of a fine aluminium grid directly on top of the nm-thin PureB layer was accomplished by special etching methods. These made it possible to protect the nm-thin PureB layer while a through-wafer aperture in the middle of the detectors was micromachined.

Due to the low sensitivity of electron detectors for SEM systems, it also becomes very important to implement a suitably low noise amplification of the signal. In principle, the best signal-to-noise ratio can be achieved by integrating on-chip electronics. In several cases this has been realized in the form of a preamplifier stage comprising a junction field-effect transistor (JFET). In the course of this thesis work, different possibilities for integrating a JFET with the detectors without excessive increase in process complexity were considered. For low-noise performance the gate length should be as short as lithographically possible. All in all, it is advantageous to process the gate as one of the last steps in the overall process flow which means that the thermal processing temperature should be limited. Focus was placed on one very low-temperature processing technique: aluminium-induced crystallization (AIC) for solid-phase epitaxy (SPE) of aluminium-doped p^+-regions formed at temperatures of about 400°C. The results presented here show that it is a versatile process module for creating both small and large p^+n diodes, even as a post-metallization step.

The detection of charged particles and different radiation types is commonly applied in a multitude of analytical tools that serve the purposes of a wide range of scientific fields and industrial monitoring. It goes beyond the scope of this thesis to treat all these applications and their principles of operation in any form of detail. In this chapter, therefore, the focus is placed on the application in Scanning Electron Microscopy which has been the direct motivation for the described work. A general overview is presented of the signals involved in this type of microscopy, along with the basic characteristics that are relevant for future detector design principles. On the device level, the fundamental limits to detection of low-energy electrons using silicon photodiodes are discussed.

1.1 Signals in Scanning Electron Microscopy

When a focused beam of electrons is accelerated by an electric field and impinges upon a solid specimen, it produces a variety of distinct emission signals that carry information on topographical and compositional properties of the target material (Fig. 1.1). Collection and processing of these signals form the basis for numerous material analysis techniques that are utilized across the multitude of industrial sectors. The focused electrons are initially created in an electron gun and accelerated towards the sample - primary electrons E_0 - and they should be distinguished from the electrons that are subsequently emitted from the specimen atoms as a result of the interaction.

Once the beam of primary electrons penetrates the specimen, the electrons are subjected to a number of scattering events rather than travel the sample in a straight line. Based on the nature of the scattering events, the signals can originate either from elastic- or inelastic-scattering. The inelastic scattering is characterized by the dissipation of the energy of primary electrons during the interaction with the orbital electrons of the specimen atoms, whereas in the elastic scattering the velocity and kinetic energy of the primary electrons are only slightly perturbed, but their trajectory reverses due to the Coulombic interaction with the specimen nucleus. Belonging to the group of inelastic interaction are the following signals: phonon excitation, characteristic X-ray radiation, secondary electrons, Auger electrons, cathodoluminescence, and bremsstrahlung (continuum radiation) (Fig. 1.1). The elastic in-

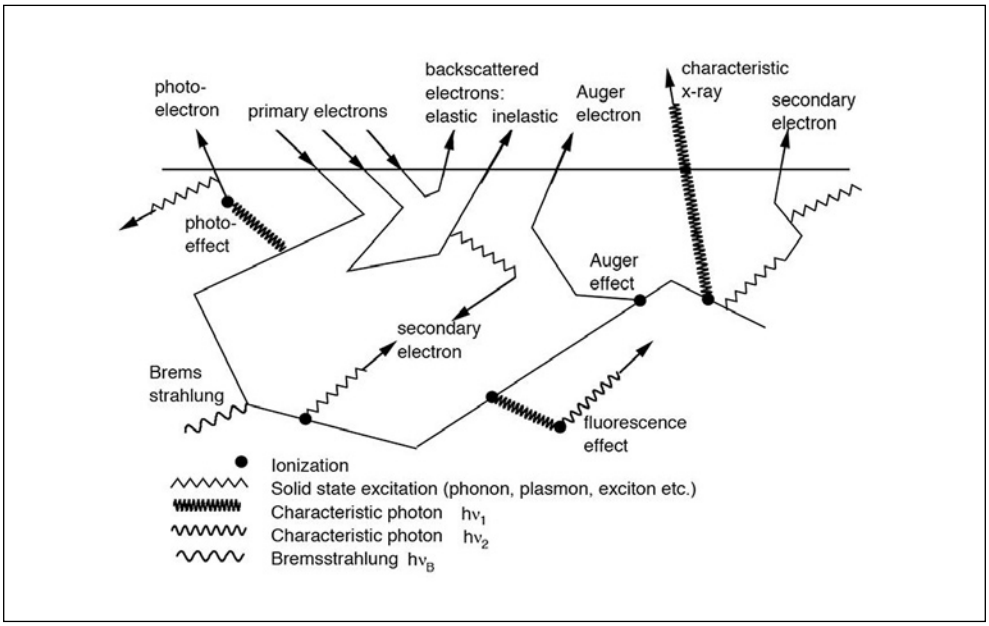


FIGURE 1.1:

Schematic interpretation of emission signals that are induced when an energetic electron strikes a solid surface.

teraction can result in backscattered electrons whose detection is the primary focus of this thesis.

In Scanning Electron Microscopy the two commonly detected signals are secondary (SE) and backscattered electrons (BSE). Strictly speaking, they are of different nature since the BSE is a reflected primary electron (elastically-scattered), while the SE is a specimen orbital electron to whom sufficient energy was transferred in order to escape the sample surface (inelastic scattering). However, in practice they are often separated by a 50 eV energy threshold, below which all of the electrons escaping the sample surface are tagged as secondary, and above which all of the electrons are considered to be backscattered. Although this division is used in practice, it is not truly valid since the BSE electrons are typically electrons that still have a considerable fraction of the initial energy of the electron beam. The energy spectrum and the number of emitted electrons is illustrated in arbitrary units in Fig. 1.2. Note that a single primary electron can give rise to both SE and BSE signals at the same time in a cascade-like manner, as shown in Fig. 1.1.

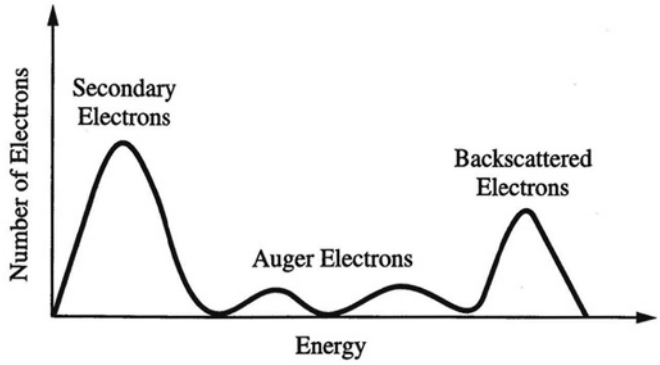


FIGURE 1.2:
Energy distribution of electrons emitted from a solid under electron bombardment [1].

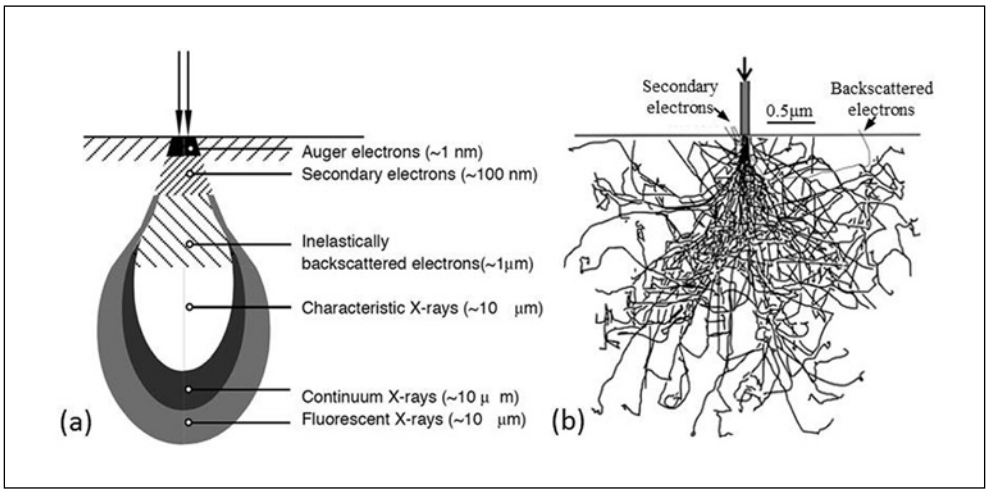
1.1.1 Electron Interaction with Matter:Volume

The interaction of a beam of electrons with a bulk material will take place within a limited volume called the *interaction volume*. In this volume all interaction takes place that can give rise to particles that can be detected, and it depends in shape and size on: the energy of the incident electrons - acceleration voltage; the composition of the target specimen - atomic number Z, morphology, and crystallinity; the angle of incidence of the primary beam; and the beam current. The shape of the interaction volume spans from bulbous-like geometries to pear-shapes, the example of the latter being shown in Fig. 1.3(a). Note that the well-shaped volume shown here is the idealized demonstration of the actual electron trajectories, that are often statistically predicted using Monte Carlo simulation tools, as shown in Fig. 1.3(b). Marked in the image in Fig. 1.3(a) is a generalized map of the interaction volume that depicts locations where specific signals are produced, and therefore illustrates the position of the information that is gathered from each signal. One reason that a restricted location can be mapped for each signal is that certain effects cannot be encountered at

FIGURE 1.3:

(a) Illustrative map depicting locations of various signals excited within the interaction volume of a solid sample.

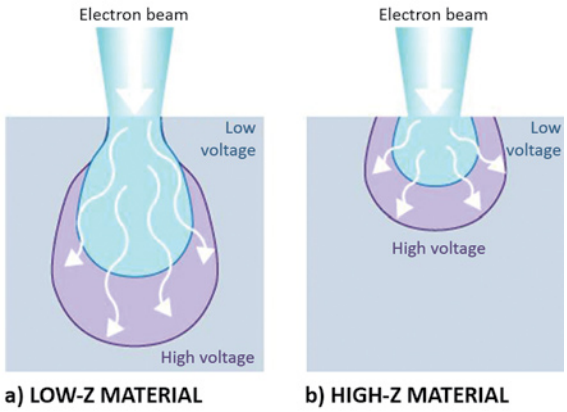
(b) Monte Carlo simulation of the electron trajectory in an Al sample (Z = 13). The energy of the electron beam is 20 keV.



all the depths. For example, electrons that propagate deeper in the sample volume have already undergone energy losses and might not have the energy required to produce some of the effects found in the shallow regions. Also, the signals produced deeper in the volume in some cases do not possess energy enough to escape the sample, therefore cannot be detected. An example of such signals are secondary electrons that are produced throughout the whole interaction volume, but due to their low energies of < 50 eV they can only traverse thin layers of material, so they will escape the specimen only when created near the sample surface.

FIGURE 1.4:

The characteristic shape of interaction volumes when the acceleration voltage is high (purple), and when it is low (blue) for a) material with low atomic number, and b) material with high atomic number.



The characteristic behaviour of interaction volume with regard to the energy of primary electrons and the atomic number of the sample is shown in Fig. 1.4. Generally, bulbous-like volumes are found for elements of higher atomic numbers, while pear-shaped volume is a characteristic of low-Z materials. Furthermore, given the same beam energy, electrons penetrate deeper into material with lower atomic numbers, while the increase in electron energy for a fixed material type elongates the interaction volume.

1.1.2 Electron Interaction with Matter: Range

In this work, it is of particular interest to estimate the path length covered by incident electrons, commonly referred to as the range of electrons in matter, in a relation with the electron energy. The range definitions found in the literature include mean range, extrapolated range, and maximum range, the differences of which have to be properly accounted for when comparing the data. For example, for deposited electron energy or dose distribution, the extrapolated range is defined as a tangent in the inflection point (the steepest slope). It is also referred to as 'practical range'. The maximum range, on the other hand, is defined at the end of the distribution tail, but it has the drawback of not giving a well-defined measurement point. The role of the electron range in microscopy is twofold: firstly, it defines the position in the specimen where the information originates from, and secondly, when fabricating an electron detector it is of benefit to design the photosensitive area to match the electron range. The range estimations are typically based on semiempirical and statistical models, and there are no accurate equations that provide prediction of the physics underlying the electron-specimen interaction over the wide energy range, particularly at low electron energies. Kanaya and Okayama calculated an expression for the maximum electron range for 10-1000 keV energies that takes into account the atomic number and the atomic weight of the material:

$$R_{K-O} = \frac{2.76 \cdot 10^{-11} A E_b^{5/3}}{\rho Z^{8/9}} \cdot \frac{\left(1 + 0.978 \cdot 10^{-6} E_b\right)^{5/3}}{\left(1 + 1.957 \cdot 10^{-6} E_b\right)^{4/3}} \tag{1.1}$$

where E_b is the energy of the electron beam, ρ the density of the material, and Z the atomic number. The expression is derived from the energy-loss relation

$$R = \int_0^{E_0} \frac{dE}{dE / dx} \tag{1.2}$$

where *dE/dx* is the total stopping power of the absorber, i.e. specimen [3]. However, the expression relies only on the first-order approximation of scattering events of electron trajectory in a solid target, and the reliability is satisfactory only at higher electron energies. When compared to several other semi-empirical models such as the extrapolated Gruen range

$$R_G = 45.7 \cdot \frac{E_b^{1.75}}{\rho} \tag{1.3}.$$

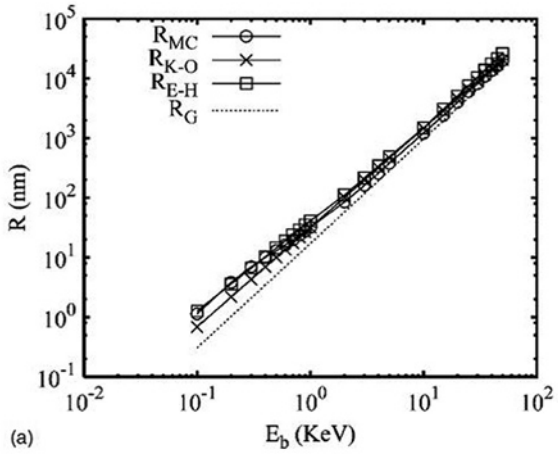


FIGURE 1.5:

Electron range for Silicon. R_{MC} is from Monte Carlo simulation, R_{K-O} is from the Kanaya and Okayama range, R_{E-H} is from the Everhart-Hoff universal curve calculation, and R_G is from the extrapolated Gruen range [2].

and the Everhart-Hoff universal curve that modifies the Gruen range by substituting constant 45.7 with 40, a mismatch of electron ranges is already observed at 5 keV, and below 1 keV it becomes more questionable (Fig. 1.5) [2]. This has led to the development of statistical methods using Monte Carlo simulations, that have recently been refined to track the low-energy interactions with matter down to very-low electron energies of < 50 eV [4]. Additionally, internet databases are available that collect the published experimental data on stopping power, BSE yields, and SE yields for the range of materials and electron energies that can be used when modelling the behavior of electrons in matter [5].

1.1.3 Low Voltage Scanning Electron Microscopy

The beam energy is a cardinal parameter in SEM imaging. At higher energies, the interaction volume reaches deeper into the specimen and consequently the collected BSE can carry information on the specimen bulk. Yet, if the low electron energies are used that have shallow penetrations in solid material, the information is gathered from the material surface for both, secondary and backscattered electrons. This is illustrated in the example shown in Fig. 1.6, where a 20-nm-thin carbon film is stretched over a copper grid [6]. When irradiated with 20 keV electrons, the carbon film is transparent to the incident electrons and only the copper grid below the carbon film is imaged. On the other hand, imaging at 1 keV electron energy restricts the electron interaction to the carbon film on the surface, and fully masks the underlying copper layer.

Recent trends in the semiconductor industry demand imaging of feature sizes in the nm-range that can more readily be visualized with low-voltage imaging. This is usually also complicated by the fact that most semiconductor structures contain insulating layers that charge when exposed to a beam of electrons. In this respect, Low Voltage SEM (LVSEM) is widely acknowledged to provide characterization with reduced sample charging for nonconducting materials, reduced damage of delicate samples, and enhanced surface sensitivity, due to the significantly reduced electron range and interaction volume in bulk samples. The potential of operation at low beam energies has been recognized by scientists at the early stages of electron microscopy, before SEM machines existed as commercial instruments (Knoll in 1935 [7] and von Ardenne in 1938 [8]). Despite high expectations, there has been a trade-off with decreased material contrast, stronger sensitivity to stray fields, higher contamination rate, and the need for special detector strategies [6]. The research described in this thesis focuses on solving the direct detection issues for low-energy BSE in SEM systems.

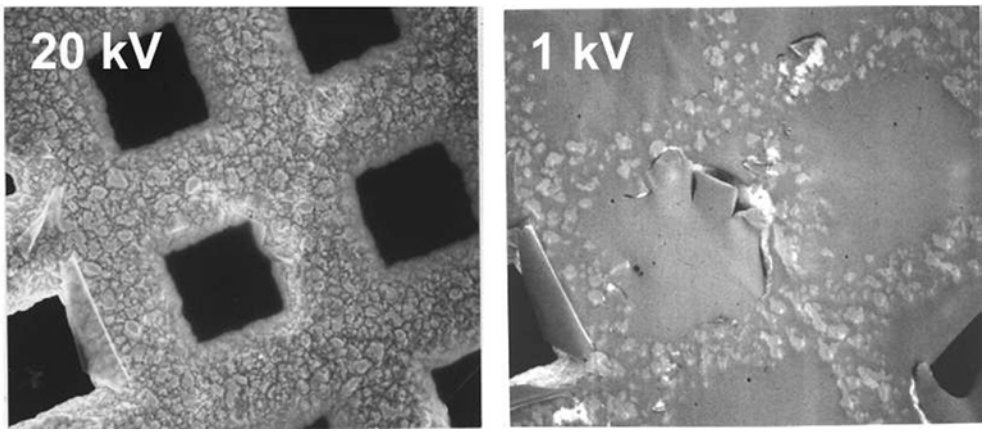


FIGURE 1.6:

Images of a 200-Å-thick carbon film stretched over a copper grid at 20 keV and 1 keV. Image is recorded on a Hitachi S-800 FEG SEM [6].

1.2 Backscattered Electron Detection

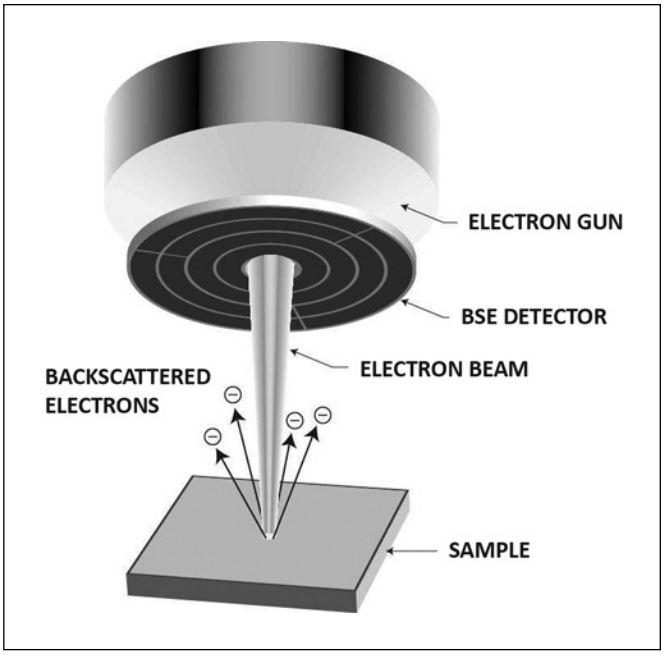


FIGURE 1.7:

Conceptual drawing of a SEM system showing the location of the annular PureB BSE detector.

The energy of the BSE is typically a considerable fraction of the initial energy of the primary beam. Hence, the commonly used Everhart-Thornley detector that collects secondary electrons is not suited for the detection of BSE signals as the voltage applied to it would have to be high and could therefore disturb (deflect) the primary electron beam. Since BSE are defined in SEM as > 50 eV energies up to around 30 keV, the first criteria for a good detector is a high responsivity in this range. Second, the detector should ideally be positioned vertically above the specimen if the normal beam incidence is used for primary electrons. In modern practice, the detector is implemented as a doughnut-shaped structure that encircles the electron beam on its way to the target (Fig. 1.7). In this way the electrons with highest reflection angles can be recorded by the detector.

There are two BSE detector structures that demonstrated promising results with high efficiency extended down to low accelerating voltages: scintillator-photomultiplier and solid state detector technology, for both of which there are recent reports of high-resolution detection down to 1 keV and below [9–12].

1.2.1 Scintillator Detectors

A scintillation detector is constructed using a scintillation crystal that is coupled to an electronic light sensor, such are photomultiplier tubes or photodiodes. The crystal emits photons in an amount that is proportional to the particle/radiation energy, and the photons are then converted using the light sensor into an electrical signal. A single crystal yttrium aluminium garnet (YAG) detector is an example of a promising BSE detector among scintillator detectors [13,14]. So far, the detector has been restricted by the existence of a threshold energy of the incident electrons below which the flux of the generated photons would not produce an image acceptable in terms of the noise level. The threshold energy for the YAG single crystal is approximately 1.3 keV and the detector was only used for primary beam energies down to 2 keV. Recently, Wandrol et al. introduced a new YAG scintillation detector capable of working at a primary beam energy as low as 0.5 keV [10]. However, the reduced energy threshold is facilitated by the boosted acceleration of low energy backscattered electrons, and applying the deflection of secondary electrons using an energy filter, thus it is not a direct detection. Other reported implementations of scintillator BSE detectors include the high performance phosphor material detector, the so-called Robinson detector, that generates and captures very high photon signals from low energy electrons. A few generations of Robinson detectors have been available on the market for the last few decades, and the most recent one claims appreciable performance in sub-keV energy domain [15].

1.2.2 Silicon Photodiode Detectors

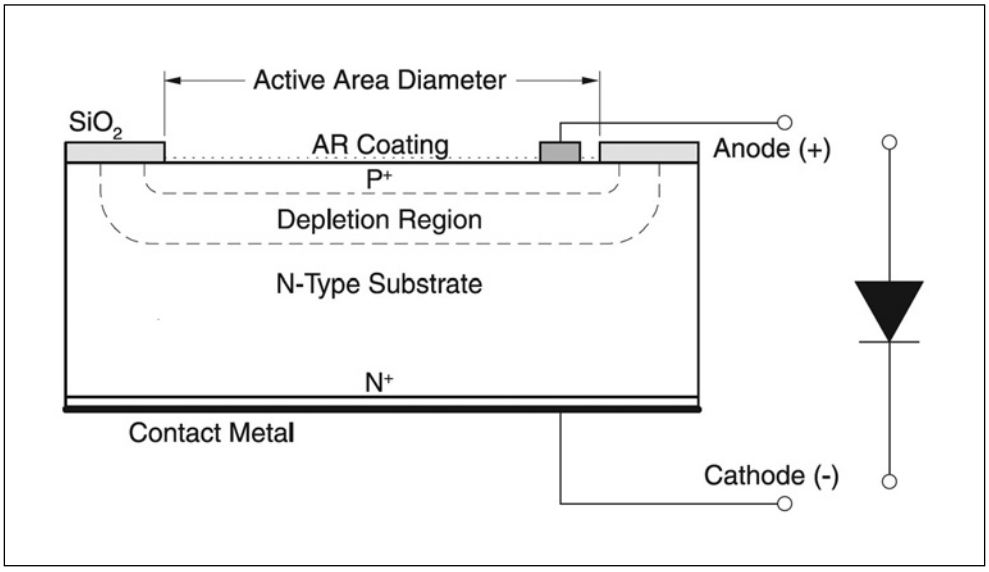


FIGURE 1.8:

Schematic cross-section of a p^+n diode structure showing the oxide-opening entrance window for the radiation, and the photosensitive depletion region at the diode junction.

Fig. 1.8 shows a cross-section of a basic p^+n diode structure. It consists of a highly doped p-type anode in turn covered by an antireflective (AR) coating on top of the depletion region formed on the n-type substrate. The resistivity of the substrate and the voltage applied across the diode define the width of the depletion region which is the absorber layer for the incident radiation. The basic requirement for the photodiode radiation detector is that the depletion region is positioned accordingly to the attenuation length of the radiation under detection. Only then, the radiation energy is used for creation of *electron-hole pairs (EHP*) that are separated by the electric field and contribute to the photocurrent. The diode is typically reverse biased, and the level of the dark current represents the noise floor of the detector. When illuminated (irradiated), the reverse current increases proportionally to the number of induced carriers N, which is the ratio of the deposited (absorbed) radiation energy E_D, and the average ionization energy ε in silicon, i.e. EHP creation energy:

$$N = E_D \,/\, \varepsilon \tag{1.4}$$

In the following paragraphs both the average ionization energy constant ε, and the absorbed (deposited) energy E_D which is dependent on the losses to the incident energy E_0, will be given further consideration.

1.3 Ionization Energy in Silicon

The average energy expended by the primary radiation on electron-hole pair creation in semiconductors determines the highest possible number of the electron-hole pairs that can be created for the semiconductor particle/radiation detectors. Already at the inception of the work in this field, it had been clear that the required energy to create an EHP is several times higher than the sole bandgap energy of the material, due to the losses to the crystal lattice. Shockley first proposed a model that accounts explicitly for the phonon losses, assuming that the threshold energy for EHP creation linearly depends on the bandgap width:

$$\varepsilon = 2.2E_g + r\left(\hbar w_r\right), \tag{1.5}$$

where E_g is the bandgap energy, and r the average number of optical phonons (or Raman quanta $\hbar w_r$) emitted between impact ionizations [16]. Following in his footsteps, several other authors proposed slightly modified linearity constants, finally arriving to the expression of Klein

$$\varepsilon = \left(14 \,/\, 5\right)E_g + r\left(\hbar w_r\right), \tag{1.6}$$

where r is treated as an adjustable parameter. The expression is used to this day as a reliable reference. In the work published in [17], Klein gives an overview of radiation ionization energy vs. bandgap energy for a number of materials, fitting the proposed semi-empirical

model to the experimental data obtained by using various incident radiations (γ rays, fast electrons, or α particles). The fitting curve is shown in Fig. 1.9, and crystalline Si is found to have EHP creation energy of (3.61 ± 0.01) eV for α particles, and (3.79 ± 0.01) eV for fast electrons. Even though a slight difference in ε is measured for the two radiations types, the general conclusions concerning experimentally extracted ε values are offered:

1. Pair-creation energies are essentially independent of the characteristics of the primary radiation; in particular, they do not reflect the nature of the incident particle in any distinct manner [17].
2. There is a remarkable correlation between ε and the bandgap energy; in effect it appears that a factor of about three may have some fundamental significance in this regard [17].

More recent studies, largely inspired by the advances in semiconductor detectors, focused on an extraction of ε in silicon for shallow-penetrating radiations, such as VUV/DUV radiation, soft X-rays, and sub-keV electrons. Scholze et al. reported on investigations of photon-induced pair creation in the 3 to 1500 eV spectral range, yielding a constant value of (3.66 ± 0.03) eV for photon energies above 50 eV, and a maximum value of 4.4 eV around 6 eV [18]. Funsten et al. calculated the response of Si for low-energy electrons using Mon-

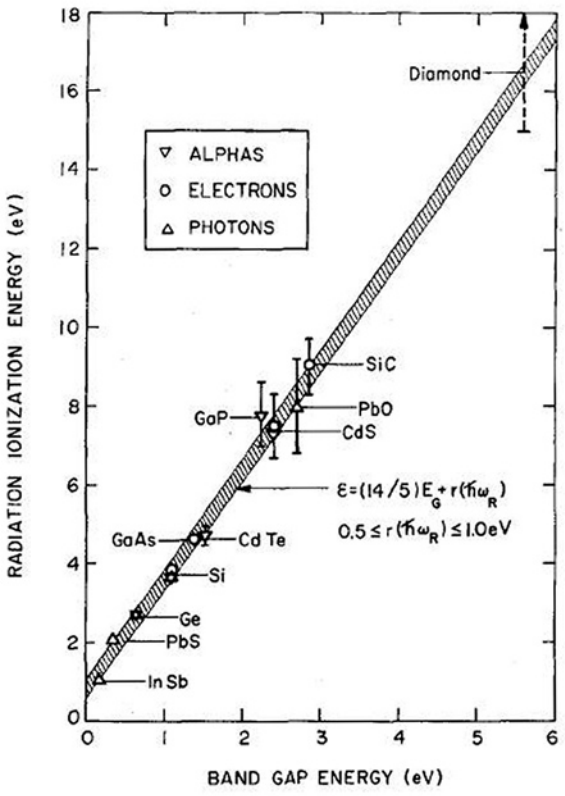


FIGURE 1.9:

Radiation-ionization energy, or average amount ε of incident radiation energy consumed per generated EHP, as a function of the bandgap width E_g [17].

te Carlo simulations to correct for detection losses, and reported the creation energy of 3.71 eV [11], and Fraser et al. showed the increasing trend of ε at low X-ray energies, while still maintaining the asymptotic value of 3.65 eV [19]. However, some issues remain yet unresolved related to measurements of ε for sub-keV electrons, where the lack of reliable measurement instrumentation causes a gap in the available experimental data.

It can be concluded that the pair-creation energy is mainly a material property and it poses a fundamental limit for detection efficiency. When using silicon detectors, the 3.6 eV ionization energy seems to be the limiting factor for a number of the induced carriers, if operating the device without the internal gain. For this reason many researchers have turned to compound semiconductor radiation detectors in a quest to engineer a perfect material for each radiation type [20]. Although semiconductor compounds with significantly lower pair-creation energies have been reported, their development has allegedly been plagued by material and fabrication problems. Specifically, the most severe limitations of compound semiconductors are poor transport of carriers through low mobility and low carrier lifetime, lack of native oxides, very limited choice of doping agents, and difficulties in fabricating stable and laterally uniform contacts.

1.4 Fundamental Limits of Si Photodiode Detection of Low–Energy Electrons

When detecting charged particles using Si photodiode detectors, the energy consumed per electron-hole pair is predefined. However, the energy that is deposited in the photosensitive region of the diode can be maximized by careful detector design and fabrication. It will be assumed further on that the photodiode devices fabricated here exhibit 100% internal quantum efficiency, i.e. that the recombination of the electron-induced carriers in the drift region is negligible. The deposited energy can be estimated from the incident energy by deducting the losses it encounters on its path to the responsive detector region. Two dominant loss mechanisms are backscatter losses Δ_{BS} and dead layer losses Δ_{DL}. The former is essentially a property of the material of the detector and changes with the incident electron energy and the incident beam angle. The latter loss is critical for shallow-penetration beams, in particular low energy electrons, and it is a technological challenge to create the necessarily thin thickness of the detector's front-entrance-window layer.

The deposited energy considered statistically over an ensemble of electrons can be calculated as

$$E_D = E_0 - \left(\Delta_{BS} + \Delta_{DL} + \Delta_R\right), \tag{1.7}$$

where Δ_R is the residual loss that can include, for example, the recombination at the boundaries of the active area of the detector [11].

1.4.1 Backscatter Loss

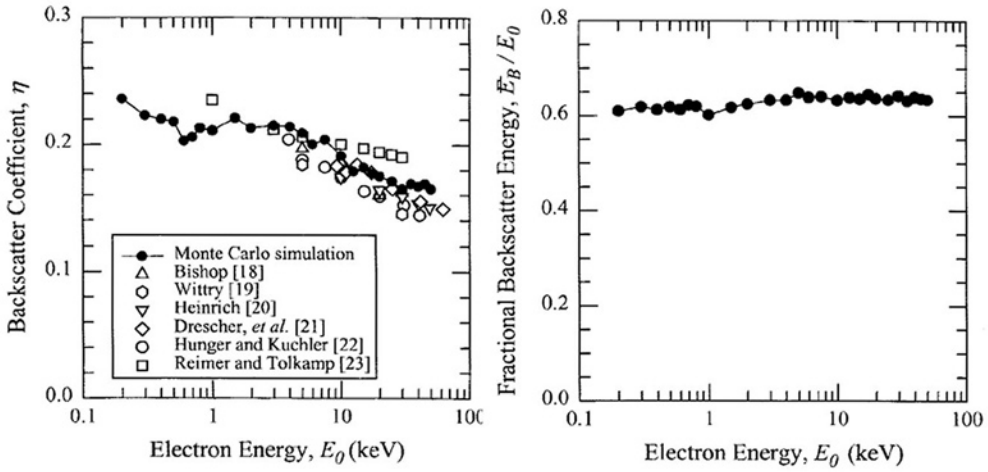
When the electrons backscatter from a specimen and impinge upon the detector surface, a fraction of the electrons can reiteratively scatter back from the detector surface and carry away a part of detectable signal. The loss is described by Funsten et al. as

$$\Delta_{BS} = \frac{\eta E_B}{E_0}, \tag{1.8}$$

where E_B is the average energy of backscattered electrons, E_0 the energy of the incident electrons, and η is the backscatter coefficient [11]. An example of the backscattering coefficient and Monte-Carlo-derived fractional backscatter energies are given in Fig. 1.10.

FIGURE 1.10:

(left) Backscatter coefficient for Si targets from experimental data (open symbols) and the Monte Carlo simulation (points), and (right) the average backscattered electron energy, derived using Monte Carlo simulation and normalized to the incident energy [11].



The coefficient η is dependent on the detector material, the energy of the electrons, and the incidence angle. Generally, η is diminished by materials of lower atomic number, as shown in Fig. 1.11. However, at low electron energies the backscattering trend follows closely to the atomic number in a way that the high-Z materials show a decreasing- η trend, while the low-Z materials exhibit slightly higher backscattering (Fig. 1.12) [5, 21, 22]. For this reason, the general models used to calculate the η with respect to Z dependancy typically deviate from expected values at low electron energies. Moreover, in the low energy range the backscattering phenomenon is more difficult to examine than at higher energies because of the reduced average penetration of the electrons. One of the widely used formulas based on

experimental data is given by Staub [21] for the energy range of $0.5 \le E_0 \le 30$ keV:

$$\eta(E_0) = n\left[1 - exp\left(-6.6 \cdot 10^{-3} n^{-5/2} Z\right)\right],\ n = 0.40 + 0.065 ln(E_0), \tag{1.9}$$

which after introducing the material parameters of Si (Z = 14) reduces to:

$$\eta(E_0) = n\left[1 - exp\left(-0.0924 n^{-5/2}\right)\right] \tag{1.10}$$

with E_0 taken in keV. The formula fits well with the experimental data collected by Joy [5].

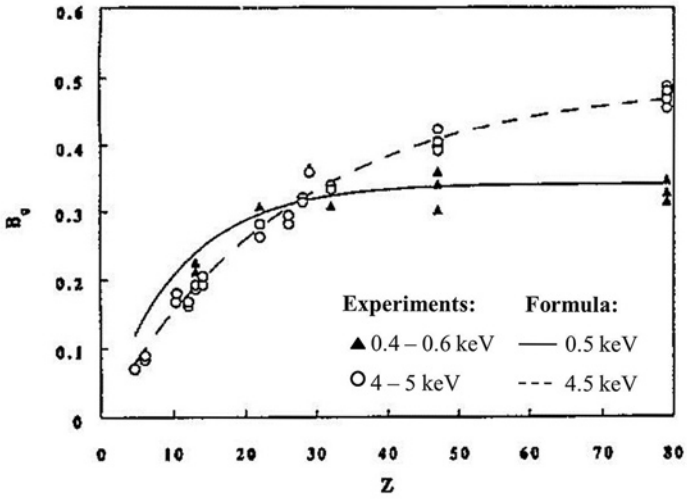


FIGURE 1.11:
Backscattering coefficient at normal incidence η_0 for different E_0 magnitudes, as a function of the atomic number Z of the scattering target [21].

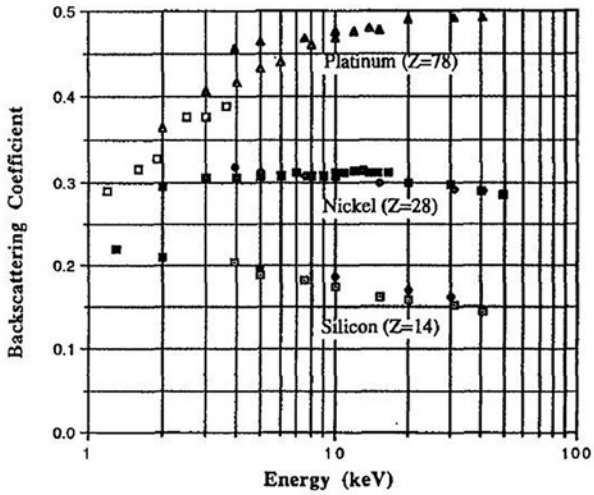


FIGURE 1.12:
Variation in the backscattering yield coefficient η for silicon, nickel and platinum as a function of the incident energy. Data taken from references in Joy [5].

Finally, a fact that should not be overlooked is that the BSE electrons have an angular dependance as they impinge on the detector surface. Then, the angular dependence of the η can be estimated for $\Theta \leq 60^{\circ}$ by

$$\eta_{\Theta}(E_0, \Theta) = \left[\eta(E_0)\right]^{1-k(1-cos\Theta)}$$
$$k = 1 - exp\left(-1.83E_0^{0.25}\right). \quad (1.11)$$

The very significant influence it can have on the backscattering coefficient is illustrated in Fig. 1.13.

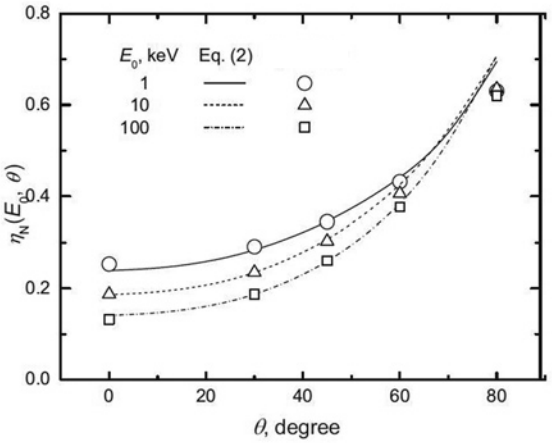


FIGURE 1.13:

The angular dependence of the backscattering coefficient for electrons with energies E_0 = 1, 10, and 100 keV, incident on a silicon surface at different angles. The lines were computed using Eq. 1.11. The symbols show the results of MC simulations [22].

1.4.2 Dead Layer Loss

In passing through matter, the electrons gradually lose their energy and the effect can be quantified by an average energy loss per unit path length - stopping power of electrons. For well-designed photodiode detectors the electron path is matched to the diode drift region, so that the expended energy can be directly converted into electron-hole pairs and collected at the device output. Nevertheless, for the specific case of low energy electrons, particularly sub-keV electrons, the bulk of the energy is deposited in the first few nanometers at the detector surface which complicates the energy conversion [23]. Fig. 1.14 shows an example of the deposited energy distributions as a function of penetration depth in Si, and it is evident that for sub-keV electron signals each nanometer at the detector surface counts [22]. Considering the lowest energy of 100 eV shown in the graph, it can be concluded that the whole energy package is delivered within the first 10 nm, moreover, the major part of it is only within the first few nanometers. In practice this implies that the detection of such electrons demands a detector which is responsive at the surface itself, which for photo-

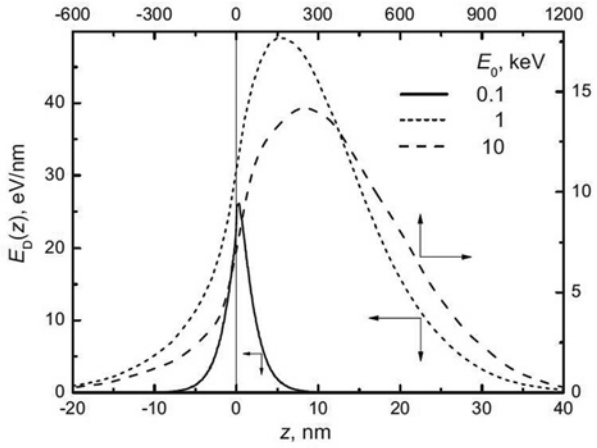


FIGURE 1.14:

Deposited energy distributions as a function of depth of penetration in an infinite silicon medium for different incident electron energies: 100 eV and 1 keV (bottom and left axes) and for 10 keV (upper and right axes) [22].

diode detectors translates into eliminating all the layers that are usually fabricated at the front entrance window. This includes the metallization layer, passivation layers, antireflective coatings, and the neutral p-type or n-type Si at the surface of the pn-junction where the carriers can recombine. This demand is in a direct conflict with the low-noise specification of the detector: if the diode's electric field, i.e. depletion region, reaches the unpassivated Si surface, the dark current of the diode will be much higher than the signal created by the sub-keV electrons. Therefore, it is vital that the diode is fabricated using a front-entrance layer sufficiently transparent to the low-energy electrons, but still providing reliable surface passivation to obtain the low noise. Since the losses at the entrance window cannot be entirely eliminated, they will hereafter be accounted for as a 'dead layer' phenomenon, and is commonly expressed as the non-responsive material thickness (in nm), or as the minimal detectable energy threshold (in eV).

1.4.3 Energy Loss Considerations for PureB Layers

In the light of the above-described losses, photodiodes made with PureB layer are obvious material choice for the detection of low-energy electrons. As briefly mentioned at the beginning of this section, PureB photodiodes can be fabricated with a nm-thin pure boron anode deposited on an n-type substrate. Apart from the obviously attractive thickness of only few atomic layers, PureB layer is also a low-Z material (Z = 5) for which the backscattering coefficient η is by nature minimized (see Eq. 1.9). Further, the compound of boron with silicon, if not favorable, surely does not have an amplifying effect on the overall backscattering when compared to the bulk silicon. Finally, the range of electrons is larger the lower the Z, so the electrons will readily traverse the PureB layer and reach the depleted silicon bulk.

Detailed considerations of the PureB layer that include fabrication parameters, layer composition, electrical characterization, and the response to the accelerated electrons are addressed in the following chapter.

1.5 Operation of Si Photodiode Detectors in SEM Systems

When using a Si photodiode as the detection device in a SEM system, the response time of the diode may be decisive for the imaging speed. On a device level, the response time translates to the RC constant of the detector, i.e. the series resistance R and capacitance C of the photodiodes comprising the detector. For a sufficiently high scanning speed, it is important to achieve both a low series resistance and low capacitance of the individual diode building blocks. This can be achieved by specially modifying the Si substrate that is used here as one terminal of the photodiode. The substrate can be either low-ohmic which provides low series resistance but is not suitable for meeting the low capacitance specifications, or high-ohmic by which the low capacitance is assured but the series resistance can become very high. Considering the junction capacitance of the diode, it will increase with the diode area A, and decrease with the depletion width x_d as follows:

$$C_j = \frac{\varepsilon_S}{x_d} \cdot A. \tag{1.12}$$

For backscattered-electron detectors, the diode areas are large and therefore the bulk junction capacitance is the main contributor to the overall capacitance, while perimeter effects, i.e., the oxide capacitance that arises from the metallization overlapping the oxide isolation, become less significant. The junction capacitance is high due to the large diode area and in order to lower it, wide depletion regions are required. The depletion region is governed by the doping concentrations N_A and N_D and the voltage V over the junction:

$$x_d = \sqrt{\frac{2\varepsilon}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)\left(V_b - V\right)} \tag{1.13}$$

Since the operating voltage of detectors in SEM systems is rather low, the doping concentration needs to be very low to facilitate wide depletion.

The series resistance, on the other hand, will increase with decreasing the doping concentration. For this reason, the highly-doped region that is beneficial for low capacitance has to be either avoided or fully depleted, to achieve the low series resistance. Taking both the resistance and the capacitance into account, two solutions of substrate modifications have been proposed for achieving the low RC constant:

1) a low-ohmic, i.e., highly-doped substrate on top of which a sufficiently thick high-doped epi-layer is grown, that is depleted during the detector operation,

2) a high-ohmic, i.e., low-doped substrate that is fully depleted either due to the very light doping or because the otherwise undepleted bulk material is etched away using a bulk micromachining step.

Both substrate modifications are investigated in this thesis, respectively in Chapter 3 and Chapter 5, and the trade-offs for both approaches are evaluated.

Further improvements can be implemented outside the detector itself, especially in the charge preamplifier stage that is connected directly to the detector anode. The most commonly used charge preamplifier is a Junction Field-Effect Transistor (JFET). In that case, the capacitance that is seen from the anode node will also include the gate capacitance of the JFET and the parasitic capacitance of the wiring between them. In such a configuration, the best performance has been demonstrated for the on-chip detection units, where the detector is integrated on the same chip with the preamplifier stage, thus lowering all the parasitics associated with the interconnections and wiring. Integration of JFETs on the same chip as the PureB detectors is possible but the processing scheme would be considerably simplified if a low-temperature processing module (< 400°C) for the JFET gate was available. Then the fabrication of this critical structure could be introduced as a post-PureB process step. In Chapter 6, an aluminium-mediated solid-phase-epitaxy technology is presented for post-metallization p^+ junction formation that can potentially be used for completing the fabrication of JFET amplifiers on top of fully processed BSE detectors.

1.6 Outline of the thesis

The work presented in this thesis focuses on the integration of the PureB layers in backscattered-electron detectors for the use in SEM systems. Moreover, the Al-mediated solid-phase epitaxy process is studied as a potential low temperature process for the integration of the front-end electronics on-chip with the detector. As for every type of detection, the efficiency and the operating speed are the central issues. These are treated in the following chapters as follows:

In Chapter 2 the PureB layer technology is introduced in relationship to the specific properties that make it suitable for the detection of low-energy electrons. In particular, the PureB layer is studied as a diffusion barrier between Si and pure Al, the PureB deposition process is evaluated in terms of uniformity over large deposition areas, and the stability of the layer is tested in vacuum conditions and under electron irradiation. The layer is integrated as a photodiode anode and the detection efficiency is measured for 0.5 keV and 1 keV electrons and compared to the state-of-art BSE electron detectors.

In Chapter 3 focus is placed on the capacitance of the PureB photodiodes. A special epitaxial process is tailored to be sufficiently thick and ultra-low doped to achieve a wide depletion region of the diode, thus obtaining a low capacitance value without significantly affecting the series resistance and the dark current of the device. For accurate profile engineering, the parameters such as the epi-layer thickness, growth cycle, and the starting doping value are closely studied. A sufficient degree of profile control is demonstrated when the epi-layer is applied to electron detectors.

In Chapter 4 the PureB detector design is presented. It consists of 8 closely-packed PureB photodiodes that combine the high detection efficiency demonstrated in Chapter 2 with

the low capacitance value shown in Chapter 3. The photodiode layout is designed so that the detector can measure the response of each diode separately, or grouped in adaptable configurations to obtain the required imaging contrast. Another special processing step is introduced that is patented for this sort of application: the method for patterning a metal grid on top of the nm-thin PureB anode that reduces the total resistance value of the detector while covering a minimal percentage of the photosensitive area. The electron detector is bulk-micromachined at the end of the fabrication process so it can be positioned coaxially around the electron beam in an SEM system. SEM images are shown for 50 eV landing energies.

In Chapter 5 a potential modification of the photodiode detector process is proposed for achieving even lower RC constant values. For this purpose, the PureB detector design is transferred to high-resistivity substrates, and all the associated trade-offs both process- and performance-related are evaluated. The most prominent issue then becomes the high series resistance that is overcome by etching away the non-active substrate volume.

Chapter 6 presents the process of the epitaxial growth of p^+ -regions using Aluminum-Induced Crystallization to form p^+n diodes. In this process, the Si crystallization on c-Si substrates is studied in terms of wafer surface preparation and the corresponding density of nucleation centers that are responsible for the growth dynamics. Special attention is dedicated to optimizing the process to fill the large window areas at the processing temperature of 400°C.

Finally, Chapter 7 summarizes the main conclusions covered by this thesis and gives the recommendations for the future work.

2

PURE BORON LAYER PHOTODIODES FOR HIGH-EFFICIENCY LOW-ENERGY ELECTRON DETECTION

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2

PURE BORON LAYER PHOTODIODES FOR HIGH-EFFICIENCY LOW-ENERGY ELECTRON DETECTION

2.1 Introduction

In this chapter a detailed description is given of the use of Pure Boron (PureB) layer photodiodes for detecting low-energy electrons [24, 25]. These diodes have in the past been used successfully for the detection of light that has a low penetration depth in silicon, as, for example, vacuum-ultraviolet light for which the absorption length is as low as 5 nm around the 200 nm wavelength [26, 27]. For electrons impinging on a solid, the penetration depth is determined by the interaction with the solid which is predominantly determined by the energy of the electrons. From 3 keV down to around 100 eV, the stopping power for an electron traveling in a bulk Si target increases from about 1 eV/Å to 4.5 eV/Å [28]. This rapidly decreases the distance that the electrons can travel. Moreover, in contrast to the behavior at higher energies, the resulting electron range does not have appreciable dependence on the target material, i.e., ranges in all solids are practically the same for the low energies. In the introductory Chapter 1, results were compiled of several theoretical and empirical models that estimate the electron range in Si as a function of electron energy. It is stated that at an energy of 1 keV the impinging electrons reach a depth of no more than a few tens of nanometers and this will decrease to a single nanometer range as the energy goes down to 100 eV. As a consequence, silicon photodiodes can only be used for low-energy electron detection if the separation of generated carriers can occur within the same small distance from the diode surface. More specifically, all additional layers on the photosensitive surface of the photodiode such as antireflective coatings, scratch-protection layers, band-pass filters, and metallization layers, as well as the distance in the Si to the active photodiode drift region, need to be minimized or completely removed. Everything that adds to the total thickness on the photodiode surface suppresses detection and is previously defined as the “dead layer”. For this reason, electron detectors in the past were essentially designed for measuring above 5 keV although a detection threshold down to 1.1 keV was reported in [29]. Today there is a great interest from various fields such as medical diagnostics [30], space missions [31], and the semiconductor industry [32], in solid-state detectors that can detect at 1 keV and below. A silicon photodiode with this capability was recently presented in which nm-thin oxide layers were used to passivate the Si surface [11]. As drawbacks, the oxide front-entrance window adds to the total thickness of the dead layer, and it is also prone to inherent instabilities related to a variable oxide charge and interface state density, both of which can vary from process to process and during use.

The silicon photodiodes presented here are fabricated using the PureB technology in a manner that makes it possible to eliminate these drawbacks and achieve exceptional detection properties for electron energies from 20 keV down to 200 eV. With this technology a nm-thin amorphous boron (α-B) layer is deposited by chemical-vapor-deposition (CVD) as described in [33]. Here the characterization is focused on the nm-thin PureB material integrated as front-entrance window to PureB photodiodes. Previous investigations of the PureB diodes have demonstrated that electrically the presence of the PureB layer suppresses minority carrier injection from the n-substrate to give a dark current of the same level as seen in conventional deep junctions. Moreover, at the interface with the Si the PureB gives an effective p^+-doping that protects the generated carriers from recombining at interface defects and supplies the doping for creating a conductive anode layer [34]. The fact that the PureB itself can function well as front-entrance window relies on two important material properties of this layer that will be discussed in the following sections: for the first, the PureB is very resistant to many metal etchants and it is shown here that the Al-metallization used to contact the anode can be removed completely from the photosensitive surface. Second, no signs of oxidation of the PureB layer have been found so that charging effects during exposure are less likely to occur. The effects of exposure on the electrical and optical behavior are investigated here under different circumstances and the PureB junction is found to be very robust to irradiation with low-energy electrons.

2.2 PureB Layer Properties

The PureB layer exhibits a distinguishing set of properties that make it specifically suited for integration in electron devices, or more specifically, in silicon photodiodes targeted for detection of low-penetration depth beams:

1. Formation of an effective nm-thin p^+-doping at the interface with Si,
2. Suppression of minority carrier injection from the substrate, i.e. low saturation currents of PureB-deposited p^+n diodes,
3. Deposition selectivity to clean Si surfaces -photosensitive junction areas are defined with the thermal oxide patterning,
4. Natural diffusion barrier layer between Si and pure Al layers -prerequisite for front entrance window formation in nm-low-penetration-depth radiation detectors (Section 2.3),
5. Deposition uniformity optimized for nm-thin layers over large deposition areas (Section 2.4), and
6. Stability in the vacuum environment, and under electron irradiation (Section 2.7).

For in-depth study of properties (1)-(3) readers are referred to the thesis of Sarubbi [35], where extensive research has been reported on characterization of PureB depositions. In

present thesis, the following sections offer an overview of PureB junction formation conditions and electrical properties, with the focus on integration properties to photodiode detectors listed in (4)-(6).

The PureB layers are deposited by chemical-vapor-deposition in a commercial epitaxial reactor (ASM Epsilon One) using diborane (B_2H_6) and hydrogen as gas source and carrier gas, respectively. The process can be performed either at atmospheric or reduced pressures for deposition temperatures ranging from 500°C to 800°C and various doping gas conditions. The formation of the boron layer is slower the lower the temperature and the diborane partial pressure, but at high gas flow rates, which provide good conditions for segregation of boron atoms on the Si surface, the final layer thickness is controlled by the exposure time. The effective B-doping and junction depth in the underlying c-Si are determined by the solid solubility at deposition temperatures and thermal diffusion/PureB-deposition duration. For standardly used 700°C deposition in photodiode fabrication on n-Si substrates, the obtained doping in c-Si is 2×10^{19} cm^{-3} and diffuses only nanometers away from the surface even for 30 min long depositions [25]. In this way, a highly-doped ultrashallow junction is formed in a tunable manner, which means that it can be designed for specific application by trading off the properties such are the junction depth, PureB thickness, c-Si doping level, layer resistivity, etc. An additional advantage for forming p^+n diodes using PureB deposition is the experimentaly proven fact that the deposition location is restricted with high selectivity to the oxide openings in the Si wafer, since the boron layer deposits exclusively to the oxide-free silicon surfaces. An example of the resulting diode characteristics for different deposition times and temperatures, including the case for which no boron is deposited, is shown in Fig. 2.1. All diodes show near-ideal behavior with ideality factors lower than ≈ 1.02, in accordance with the conclusion that the PureB fabrication does not introduce any defects that

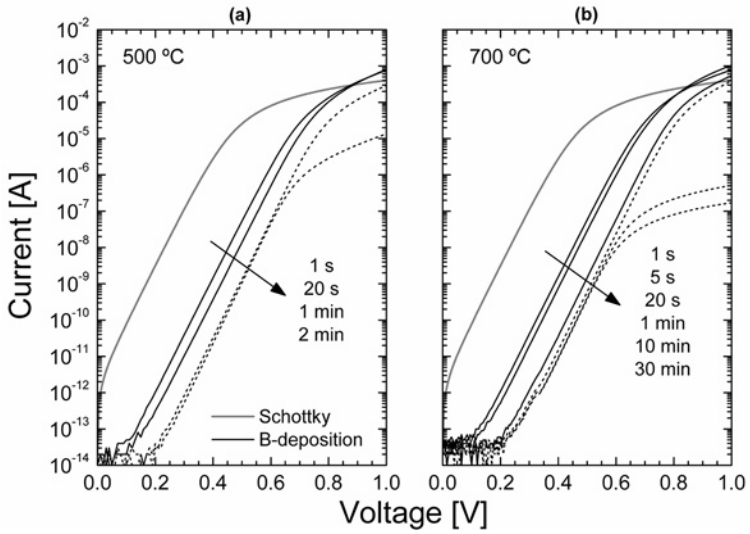


FIGURE 2.1:

Diode I-V characteristics for various deposition times at either (a) 500°C or (b) 700°C. The anode area is 2×1 μm^2. For comparison, the I-V curve of a Schottky diode is also included [33].

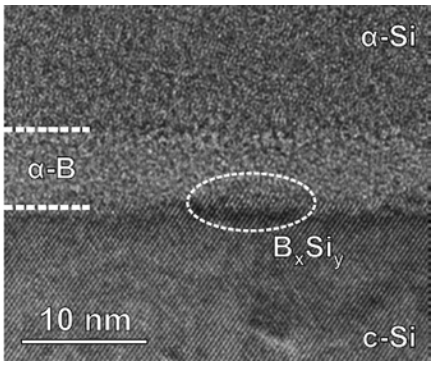


FIGURE 2.2:

HRTEM image of a boron layer formed after 10 min B_2H_6 exposure at 700°C. The sample has been covered with PVD α-Si as contrasting layer [35].

cause significant leakage currents. Further, at both deposition temperatures, increasing the B deposition time leads to a decrease of the saturation current, and a transition is seen from the high-current Schottky diode case to a low-current p^+n diode characteristic.

A HRTEM image of a PureB layer is shown in Fig. 2.2 for a temperature of 700°C and 10 min deposition time at a constant pressure and diborane flow-rate, conditions for which a constant deposition rate is obtained for depositions longer than 2 min. The deposition rate, i.e. PureB thickness values can be extracted from ellipsometry measurements by modelling the refractive index of the boron stack as 3.2, a value that was calibrated by Transmission Electron Microscope (TEM) analysis of the PureB layer. The resulting growth rate of 0.4 nm/min compares well with the rate found previously in [33] from SIMS analysis, but ellipsometry has the advantage of being a quick in-line measurement technique that appears to be applicable down to nm thickness of the B-layer (Fig. 2.3). The measured layer thickness includes both PureB and a boron/silicon transition layer on top of the c-Si wafer, the ratio of which varies with the deposition temperature set for B_2H_6 dissociation.

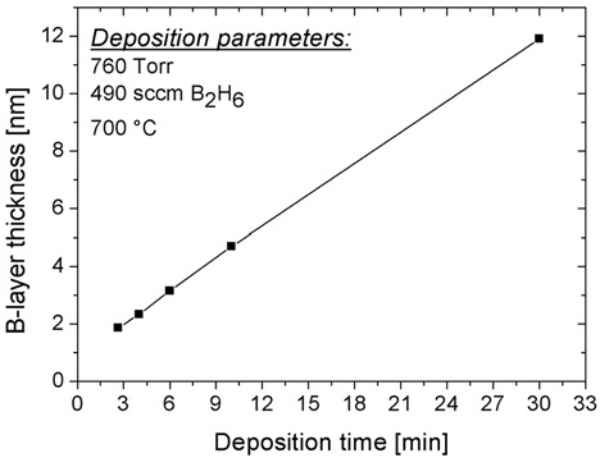


FIGURE 2.3:

Thickness of the boron layer (measured by ellipsometry) as a function of time at a pressure of 760 Torr, temperature 700°C, and diborane flowrate of 490 sccm [25].

2.3 PureB as Diffusion Barrier between Si and Pure Al

After the PureB layer of a required thickness is deposited in the pre-defined oxide openings, the layer can be contacted with a metallization layer of pure aluminium using physical vapor deposition (PVD). The pure Al is chosen for three reasons: it gives good ohmic contact to the PureB layer, does not react with the PureB layer, and can also be removed selectively to this layer. When deposited on a Si surface, pure Al will react with the Si to give large pits even at temperatures as low as 300 -400°C, which are commonly used for forming gas alloying after metallization. An example is shown in Fig. 2.4 for a 400°C alloy of windows where Al was deposited on Si with and without a PureB interface layer. To avoid the pitting problem, an Al alloy with 1-2% Si is commonly used for metallization, since this small extra Si is enough to saturate the Al. However, during alloying the extra Si will precipitate on the Si surface forming crystals, the size of which will depend on the surface morphology. For a very smooth surface, precipitates as high as the original Al thickness can coalesce and they will not be removed in the HF solution used to remove the Al layer. Although such large precipitates will only cover a few percent of the surface, optically their presence can be just as destructive as a more even coverage of smaller precipitates: the large precipitates will represent dark spots for detection of the low-energy electrons while a more even layer of smaller percipitates will reduce the overall efficiency.

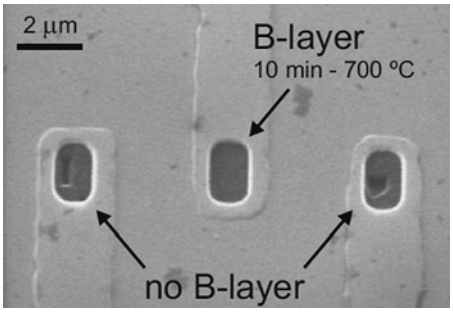


FIGURE 2.4:

SEM image after Al wet-etching of 2×1 μm^2 contact windows treated with and without a 10 min B-deposition at 700°C. The contact Al metallization was followed by a 20 min alloy step in forming gas at 400°C [35].

To avoid both spiking and Si-precipitates, a barrier layer such as TiN is commonly used between the Al and Si-substrate. Nevertheless, many researches have shown a failure mechanism on the grain boundaries and microcracks of TiN in a manner similar to conventional spiking when the temperature increases beyond 500°C [36]. Efforts to decrease the alloying temperature down to 300°C while keeping the quality of the contact have been reported [37]. However, if a barrier material such as TiN is applied to PureB photodiodes, difficulty arises in removing TiN selectively from nm thin PureB surface, while at the same time preserving the above-deposited pure Al layer. Therefore, the investigation is presented on the quality of amorphous boron itself as a new barrier layer between Si wafer and the pure Al metallization. From an extensive microscopy analysis with AFM, SEM, and TEM several previously unrecognized aspects of the layer will be discussed.

2.3.1 Experimental Material

The boron layer is deposited on n-type 2-5 Ωcm (100) bare silicon wafers in an ASM Epsilon One reactor designed for atmospheric-/reduced-pressure chemical vapour deposition (AP/RPCVD). To exclude the influence of native-oxide residues that can be found on Si wafers before the PureB deposition, different samples were prepared by using either in-situ 4 min thermal baking step at 800°C or a 30 min step at 900°C before the PureB deposition, with and without dip-etch in HF 0.55% for out-of-box wafers. The average thicknesses of the PureB studied here is 1.8 nm for a 2 min 40 s deposition (Fig. 2.5a), and 3.2 nm for a 6 min deposition (Fig. 2.5b).

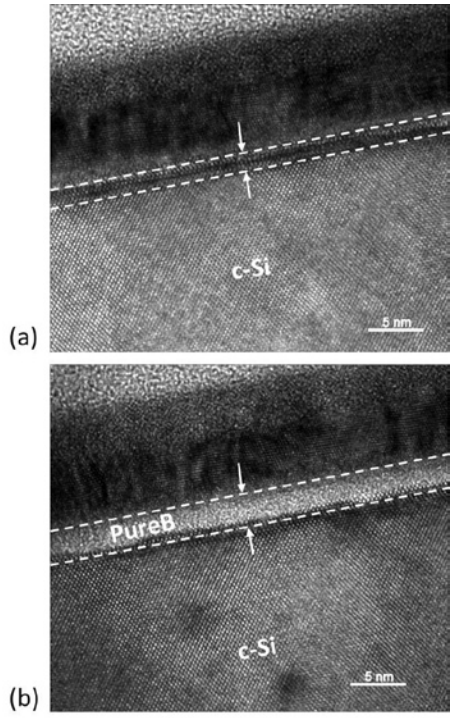


FIGURE 2.5:
TEM images of the marked boron layers formed by (a) 2 min 40 s and (b) 6 min deposition.

The 2 min 40 s deposition only just allows the layer growth to initiate while for the 6-min-long deposition a well-controlled uniform layer is formed. The thickness was monitored by ellipsometer measurements and the measured values represent the sum of the boron-silicon compound and the amorphous boron layer. After this, 875 nm of pure aluminium is sputtered at 350°C and alloyed at 400°C in forming gas on the two samples described above and one bare silicon wafer without boron deposition used to verify sufficient conditions for spiking occurrence. Finally, a thin metallic grid of pure Al is patterned in resist that mimics the processing steps that are eventually used on a full-detector design, and the Al is selectively etched to the boron layer. The samples are inspected with AFM, SEM, and TEM techniques.

2.3.2 Microscopy Studies

From the TEM analysis in Fig. 2.5a it can be seen that for the deposition time of 2 min 40 s the boron layer is neither uniform nor completely closed, and the border between the boron/silicon transition layer and amorphous boron layer is not well defined. The thickness of the amorphous boron goes below a nm, down to a monolayer and the layer tends to disappear. At such small dimensions the thickness can change 2 to 3 times along the wafer and properties of the layer can change locally, which means less stability and reliability. On the other hand, as seen in Fig. 2.5b, a sample with 6 min deposition time still has an ultra-thin layer, but with a consistent thickness around 3 nm. The deviation in thickness is negligible and the B-doped Si together with the boron-silicon compound is covered everywhere with the PureB.

From SEM examination of a sample formed with a 2 min 40 s deposition, as shown in Fig. 2.6a, considerable discolorations are observed. The bright lines are a 2.5-μm-thick aluminium grid and the large light/dark grey areas between are the bare boron layer from which the aluminium was etched away. The greyish pattern is random and does not follow any preferential orientation. The samples with other pre-boron deposition treatments (different dip-etch and thermal cleaning step) give results comparable to those shown in Fig. 2.6a. This eliminates the influence of native oxide residues on the Si surface before deposition. The SEM results correspond well with the TEM images if the discoloration is interpreted as PureB layer thickness deviation. On the other hand, SEM images of the samples with 6 min deposition time such as the one shown in Fig. 2.6b are monochrome, clear, and do not exhibit any surface roughness. The boron layer is covering the silicon surface without visible

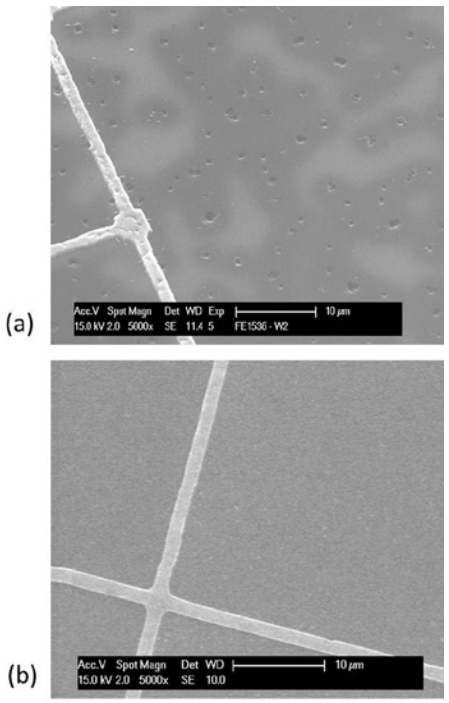


FIGURE 2.6:

SEM images of the silicon surface for the sample with a boron deposition time of (a) 2 min 40 s and (b) 6 min, after pure Al deposition, alloying at 400°C, and selective removal of the aluminum.

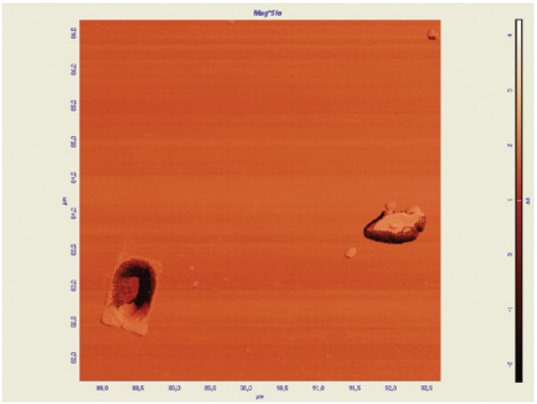


FIGURE 2.7:

AFM image of a single void and precipitate observed for the sample with a boron deposition time of 2 min 40 s, after pure Al deposition, alloying at 400°C, and selective removal of the aluminum.

variations, and the interface quality is comparable to what is achieved when using Al with 1% silicon, but with the advantage that Si precipitates cannot form in case of pure Al. SEM inspection was sufficient to conclude that longer deposition is instrumental in forming a uniform and continuous film that functions as a reliable barrier layer. To further characterize the observed surface roughness, samples were subjected to AFM inspection. It is clear that close to each void created with silicon migrating into aluminium, there is a hillock of silicon

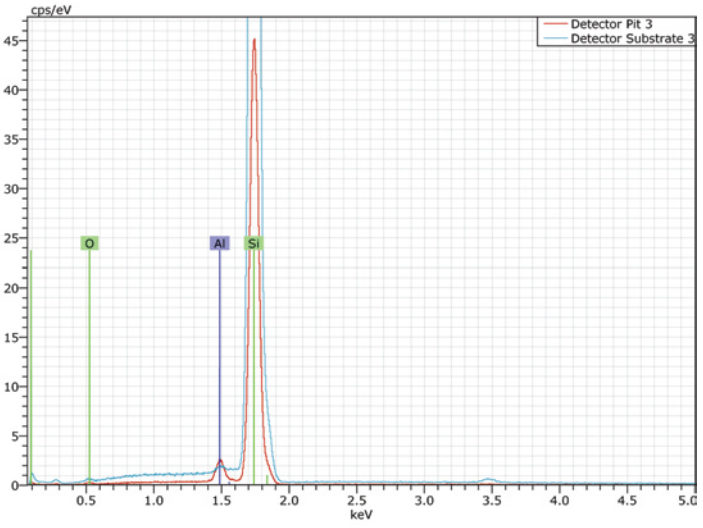


FIGURE 2.8:

EDX analysis of the boron interface (substrate) and inside of the pit for the sample with a boron deposition time of 2 min 40 s, after pure Al deposition, alloying at 400°C, and selective removal of the aluminum.

material that precipitates and stays on the surface after selective aluminium etch (Fig. 2.7). These imperfections can be as high or deep as 500 nm for 875 nm deposited Al which can considerably ruin the quality of contacts. In addition, energy dispersive X-ray spectroscopy (EDX) was used for the chemical characterization of the content of the hole. As seen in Fig. 2.8, aluminum is detected in the hole, confirming once again the origin of the presented roughness.

2.3.3 Conclusions

We investigated the robustness of two PureB samples that differed in the thickness of the layer. Although a very thin layer has been demonstrated to be a reliable p-type dopant for forming high-quality p^+n junction [33], it proves to be inadequate as a diffusion barrier. Non-uniformities of the PureB layer led to spiking/non-spiking regions as observed by SEM imaging, which confirmed that this problem is caused by insufficient boron-layer thickness, or more specifically, insufficient uniformity of the PureB depositions. By increasing the deposition time, much better uniformity and homogeneity of the layer were achieved. Indeed, the results showed a spike-and precipitate-free interface, even though the layer was still only a few nm-thick. In this way, a pure aluminium interconnection layer without any surface imperfections can be achieved. It is concluded that for a thickness of about 3 nm, a PureB layer can serve as a reliable diffusion barrier for pure aluminium.

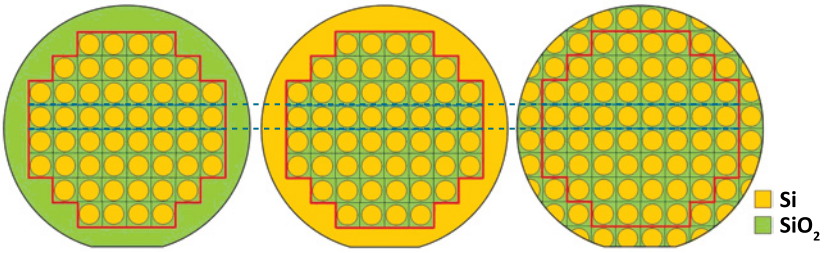
2.4 Uniformity of PureB Depositions

The uniformity of the PureB layer is a vital parameter in the fabrication of electron detectors due to the fact that even sub-nm non-uniformity of this layer causes responsivity variations of around 10-20% at electron energies below 1 keV. Moreover, PureB thickness inconsistency deteriorates the barrier layer properties as described in the previous section, which limits the deposited PureB layer to above-3-nm thickness, even though much thinner depositions suffice for low-leakage p^+n junction formation [33]. To downscale the PureB layer thickness in order to achieve higher detection efficiency, particularly in the low-energy range, while at the same time keeping reliable barrier layer properties, the uniformity of PureB layer is studied and a strategy is developed for uniform layer deposition down to 1.8-nm-thin PureB layers. The non-uniformity of the PureB layer can be explained by the boundary layer theory over Si openings, and local oxide per Si ratios [38]. This means that the larger the surrounding oxide area at the deposition site the thicker the PureB layer. As a result, a special mask design can provide better uniformity of the layer, and eventually higher efficiency of electron detector. The example is given of 3 distinct oxide-mask designs shown in Fig. 2.9, all of which correspond to the simple circular detector geometry and the 10×10 mm^2 die size:

1. Regular layout (RG): standard layout used for exposure of the process wafer. It can be divided in two parts: main and surplus margin. All dies are located in the main part and surrounded by surplus margin which is not used for the device fabrication purposes, and is usually covered with oxide (Fig. 2.9a).
2. Remove Margin layout (RM): RG layout with the oxide of the surplus margin etched-away (see Fig. 2.9b)
3. Continuous Dies to Edge layout (CDE): the surplus margin of the RG layout is patterned by the same mask which is used to expose the main wafer area, as shown in Fig. 2.9c.

FIGURE 2.9:

Different over-the-wafer designs of the oxide-etch mask: (left) Regular layout, RG (center) Remove Margin layout, RM (right) Continuous Dies to Edge layout, CDE. The red line shows the boundary of the main dies, and the dashed blue line mark the test dies for which the PureB-layer thickness is measured.



The PureB layer is deposited in all the three presented wafer layouts under the invariable deposition conditions. Layer thickness is measured by ellipsometry technique in different positions along the wafer at the middle of the circular openings (Fig. 2.9), and the results are shown in the Fig. 2.10. It can be seen from the PureB thickness measurements that the middle dies at RG layout have lower PureB deposition rate than the edge dies. It is explained by the loading effect of the huge amount of oxide at the surplus margin of the wafer that supplies additional PureB to the outer dies, thus creating die-to-die thickness variations [39]. Therefore, surplus margin oxide is removed in the RM layout. However, this does not improve the layer uniformity since in this case the outer dies have lower deposition rate compared to the central dies, due to consumption of the PureB layer at the large Si areas of surplus margin [39]. To achieve the optimized loading/consumption effect of the surplus

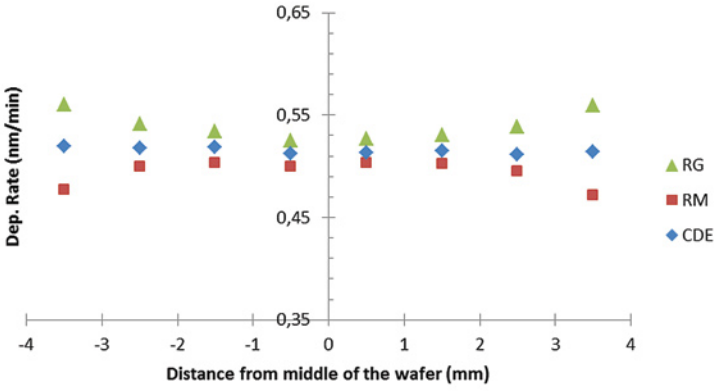


FIGURE 2.10:

The PureB deposition rate versus distance for RG, RM and CDE layouts of the Fig. 2.9 at 700°C.

margin area of the wafer, the same oxide-etch mask design is applied at surplus margin area as for the main wafer area as shown in CDE layout in Fig. 2.9c. This guarantees that all the dies have the same loading effect and, consequently, the same PureB deposition rate is obtained, as shown in Fig. 2.10.

The situation is further complicated by the fact that the oxide openings of electron detectors are typically segmented. In practice, the circular detector opening can be divided in up to 12 sub-openings, the role of which is separately discussed in Chapter 4. This provides an additional source of thickness variation that ranges up to 0.5 nm for a single detector. Therefore, additional deposition parameter optimizations are employed to minimize the non-uniformity of the PureB, which is the topic of the extensive study reported in [38]. It is finally shown that with using CDE layout in place of RG layout, and by optimizing the PureB deposition parameters, it is possible to deposit the uniform, reliable and reproducible 1.8-nm thick PureB-layer with only few angstrom thickness variations over the patterned wafer.

2.5 PureB Photodiode Fabrication Process

The photodiodes are fabricated on 100 mm n-type Si(100) wafers with a resistivity of 2-5 Ωcm. A 300 nm of silicon-oxide is thermally grown and the p^+-anode areas to be deposited with boron are defined by wet-etching of windows in the oxide with an area of 0.92×0.92 cm^2. In the present work a deposition temperature of 700°C is used and photodiodes were prepared with the minimum PureB layer thickness, about 1.8 nm, that can be reliably deposited. The 700°C temperature is a good compromise between PureB layer formation and doping of the Si surface: at higher temperatures the amorphous boron layer, necessary for obtaining a low dark current, will not form and a certain B-doping of the silicon, that will be inadequate at lower temperatures, is necessary for achieving a sufficiently low sheet resistance of the anode region. The processing sequence used for contacting the p^+-anode region is illustrated in Fig. 2.11. The amorphous B-layer itself has a high resistivity of about 10^4 Ωcm and the B-doping of the Si is essential for bringing the sheet resistance below the 10 kΩ/sq range. As shown by the simulations in Fig. 2.12, the doping at 700°C is extremely shallow. The simulations were performed without implementing any point defect model because previous work has shown that no detectable transient enhanced diffusion (TED) and boron enhanced diffusion (BED) effects are active during the deposition process or subsequent annealing steps and it is expected that the doping profile is determined by the thermal diffusivity and solid solubility at the given temperature [40]. At 700°C the solid solubility of boron in bulk silicon is 2×10^{19} cm^{-3}. For a substrate doping of 10^{15} cm^{-3}, the simulations predict a junction depth of 1.4 nm, 2.0 nm, 2.6 nm, and 3.7 nm for deposition times of 2 min 40 s, 6 min, 10 min, and 20 min, respectively. Although this is extremely shallow, a sheet resistance in the 10 kΩ/sq range is still obtained [40].

A lower series resistance can be achieved by introducing an in-situ thermal annealing step that provides higher dopant activation without considerable boron diffusion. To illustrate the difference with the 700°C case, the example with 1 min at 850°C thermal annealing is studied, the simulation of which is also included in Fig. 2.12. In this case, the junction depth

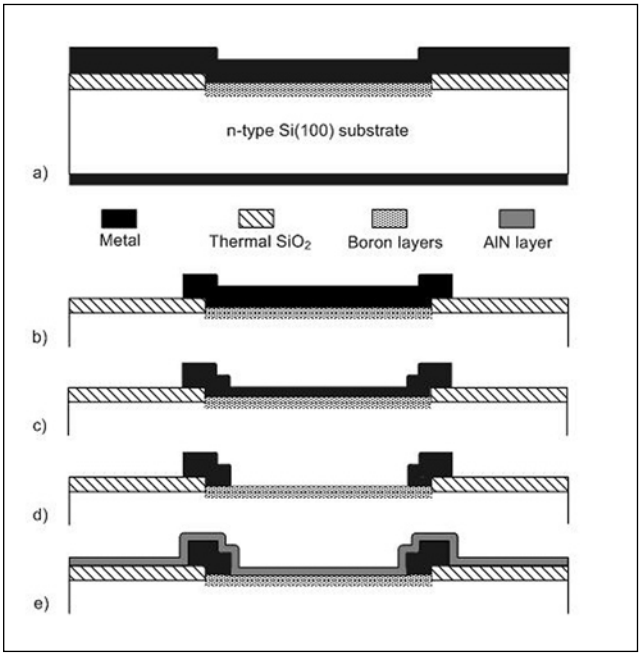


FIGURE 2.11:

Schematic of the process flow for formation of the anode Al-contacts: (a) pure Al deposition, (b) Al dry etching to define the metal patterns outside the anode region, (c) back-etching of the Al on the photosensitive area by dry etching, (d) wet-etching with diluted HF to the boron layer, and (e) AlN deposition.

increases to 14 nm and the sheet resistance is lowered four times, to 2.5 kΩ/sq [40]. However, this will result in lower responsivity to low-energy electrons, as will be shown in the following paragraphs. In addition, an extra B-doped epitaxial Si layer can be selectively grown in-situ on top of the amorphous B-layer either to improve the drivability of the active anode layer or to protect the surface. For comparison purposes, such a sample is also included in the investigations presented in this section.

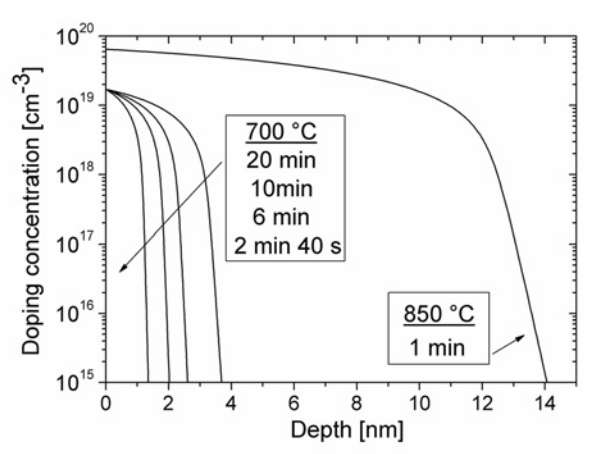


FIGURE 2.12:

TSUPREM simulations of boron doping profiles achieved by drive-in from a constant boron surface doping set at the solid solubility of the boron in Si. An anneal temperature of either 700°C or 850°C is applied with different drive-in times.

After PureB is deposited, a 1075-nm-thick layer of pure Al is sputtered at 350°C, as shown in Fig. 2.11a. This layer is patterned in three steps: the first one to define the tracks and metal contacting of the diode, the second step for plasma back-etching of the metal on the photosensitive surface, and the last one for wet landing on the boron layer. For maximum efficiency of the photodiode, Al needs to be completely removed. In the first step, the metal is plasma etched down to the SiO_2 leaving the whole diode area and a ring around the perimeter covered with Al (Fig. 2.11b). In the second step, the Al in the active area is first etched down to about 100 nm by plasma etching (Fig. 2.11c). Since the physical sputtering during plasma etching would easily remove the nm-thin boron layer below the Al, the last portion needs to be etched in a highly selective manner. Therefore, the actual opening of the photosensitive surface is performed by wet etching in diluted HF to which the PureB layer is highly resistant (Fig. 2.11d). Thus the front-entrance window is finally only covered with the PureB layer. For the further use of the photodiode in detectors it is also noteworthy that the PureB layer does not oxidize significantly in air. Moreover, it is also resistant to oxidation in low-power oxygen plasmas that are often used to clean the detector surface in SEM systems.

2.5.1 Additional Front-Entrance Window Layers

Photodiode	*Processing conditions*			
	B-layer [nm]	Anneal	epi-Si [nm]	AlN [nm]
P1.8B	1.8	-	-	-
P5B	5	-	-	-
P1.8B(AlN)	1.8	-	-	15
P1.8B(Si,AlN)	1.8	1 min 850°C	50	15
BSE	*commercially available detectors*			
vCD				

TABLE 2.1:
Description of the photodiode processing conditions

As indicated in Fig. 2.11e, after the processing of the Al-contacting of the p^+anode region, extra coating layers can be added to either protect the surface, or to serve as absorber layers or radiation filters with specific pass-bands. Depending on whether these layers are isolating or conductive, they must then be patterned with windows to the Al or removed in areas where isolation is desired. For low-energy-electron detection, any substantial coating layer thickness will readily extinguish the electron beam before it reaches the Si, so in this paper only the performance of devices with a thin coating of 15-nm-thick AlN has been included for comparison. This layer is isolating so windows to the Al-pads have been opened by plasma-etching. A list of all the samples discussed in this chapter is given in Table 2.1.

2.6 PureB Applied in Low-Energy Electron Detectors

2.6.1 Measurement Set-Up

The quality of the diodes was evaluated electrically by measuring the I-V characteristics, and the electrical stability was monitored during electron irradiation for unbiased devices by exposure to electrons in the Phillips XL50 SEM in scanning mode. In this way, these measurements could be performed on-wafer. For the efficiency measurements, on the other hand, the devices need to be biased during the exposure. Therefore, individual diodes were mounted and bonded, and then placed on an SEM holder. From the generated current during exposure, the relative electron signal gain was determined, i.e., the ratio of the current measured at the output of the photodiode, I_{ph}, to the current of the electron beam incident on the surface of the photosensitive region, I_{beam}. This is a measure of how many electron-hole pairs are produced by each incident electron. When the dark current of the photodiode is negligible with respect to the electron-induced photodiode current I_{ph}, then, at a given biasing voltage, the electron signal gain of the photodiode can be defined as

$$G_{PH} = \frac{I_{ph}}{I_{beam}}, \tag{2.1}$$

Ideally, if all the input energy is used to create electron-hole pairs, the theoretical maximum number of electron-hole pairs that can be created can be calculated as

$$G_{TH,ideal}\left(E_{beam}\right) = \frac{E_{beam}}{\varepsilon}, \tag{2.2}$$

where E_{beam} is the energy of the electrons in the beam, and ε is the mean energy of 3.61 eV required to produce an electron-hole pair in silicon [41]. In reality, backscattering of the incident electrons will cause losses, which means that the actual absorbed electron energy is less than the incident energy. To make a comparison of the efficiency of electron detection in the photosensitive material itself possible, a backscatter-coefficient η is introduced to give a theoretical maximum gain, G_{TH}, that is independent of backscatter effects:

$$G_{TH}\left(E_{beam}\right) = \frac{E_{beam}\left(1-\eta\right)}{\varepsilon}, \tag{2.3}$$

Generally, for Si photodiodes η is approximated to around 5%, and this value will be used in the following calculations, although may vary significantly in the particular case of PureB material and for the very-low energies used in this work (see Section 1.4). Also, η in this specific case represents the fraction of energy that is carried away by the backscattered electrons. To facilitate comparisons at different energies, the relative electron signal gain, G_R, is introduced as the ratio of photodiode gain to the theoretical gain:

$$G_R\left(E_{beam}\right) = \frac{G_{PH}\left(E_{beam}\right)}{G_{TH}\left(E_{beam}\right)} = \frac{I_{ph}\left(E_{beam}\right)}{I_{beam}\left(E_{beam}/\varepsilon\right)\left(1-\eta\right)}, \tag{2.4}$$

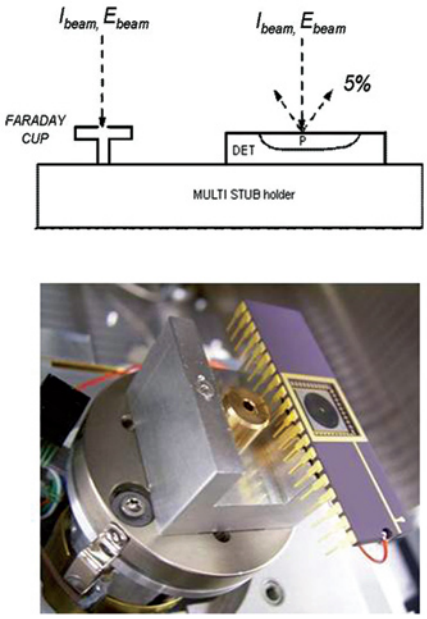


FIGURE 2.13:

Above: schematic of the optical measurement set-up with the Faraday cup and the photodiode mounted on a SEM stub and exposed to the electron beam. Below: a photograph of the measurement set-up.

The measurement set-up used to determine the relative electron signal gain is illustrated in Fig. 2.13. The beam of a scanning electron microscope (SEM) is used as the electron source and the photodiode is mounted on the multi-stub of the SEM next to a Faraday cup. In this way, calibration measurements on the Faraday cup and gain measurements on the photodiode can be carried out in a fast sequence ensuring invariable conditions. The controlled variable is the energy of the electron beam, while the beam current and the photodiode current are monitored on an externally connected picoammeter. An electron beam of energy E_{beam} and with a constant spot size and working distance, was first focused on the Faraday cup to determine the incident beam current I_{beam}. Immediately after this, the beam was directed towards the photodiode, biased at 0 V, and the photodiode current I_{ph} was measured. To verify that the beam current is stable over the whole range of acceleration voltages, measurements on the Faraday cup are repeatedly performed and compared to the initial results.

2.6.2 Low-Energy Electron Detection Efficiency

Photodiode	*Electron signal gain at 500 eV*			*Electron signal gain at 1 keV*		
	G_{TH}	G_{PH}	G_R[%]	G_{TH}	G_{PH}	G_R[%]
P1.8B	131.58	78	59.3	263.16	196	74.5
P5B		30	22.8		147	55.9
P1.8B(AIN)		-	-		34	12.9
P1.8B(Si,AIN)		-	-		-	-
BSE		18	13.7		46	17.5
vCD		52	39.5		156	59.3

TABLE 2.2:
Electron Signal Gain at 500 eV and 1 keV Electron Energies

A number of PureB photodiodes with different processing of the front-entrance window were optically characterized with 500 eV and 1 keV electron beams and the results are listed in Table 2.2. Typically a 5 nA beam current will give an I_{ph} of 1 μA at 1 keV, which means that the signal-to-noise ratio is sufficiently high to allow the use of Eq. 2.1 for calculating G_{PH} . In Fig. 2.14 the relative electron signal gain is plotted as a function of the energy of the incident electron beam. At energies below 5 keV there is a significant decrease in gain that follows the thickness of the layers covering the active Si region, while relative gain values of about 97% are reached for all the samples at energies around 10 keV. The influence of the inactive dead layers was described by Funsten et al. [11] in a formula that expresses the losses in the responsivity of the photodiode as

$$R_M = R_{TH}\left(1-\Delta_{DL}-\Delta_{BS}-\Delta_R\right), \tag{2.5}$$

where R_M is the measured responsivity, R_{TH} the theoretical responsivity, Δ_{DL} is the above mentioned dead layer loss, Δ_{BS} is the backscatter loss, and Δ_R represents the residual energy

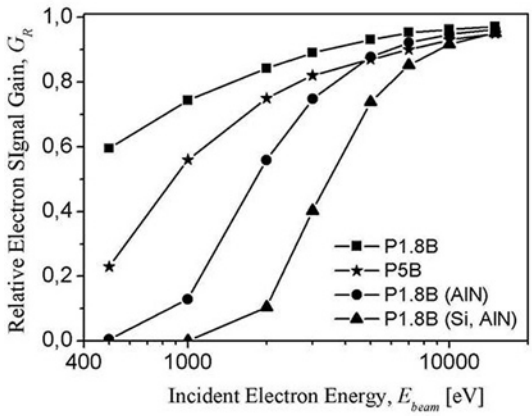
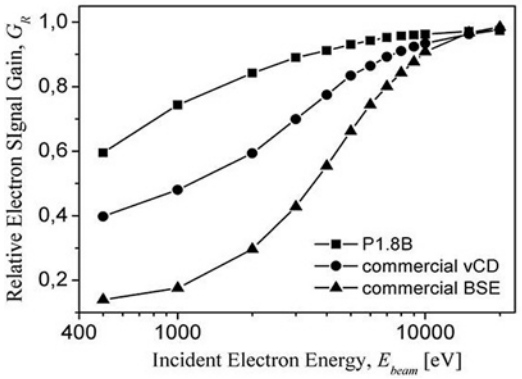


FIGURE 2.14:
Measured relative electron signal gain for the photodiodes listed in Table 2.1.

losses, e.g. electron-hole recombination within or at the boundaries of the active area of the detector. It was concluded by Funsten for the specific case he reports on the photodiode with 6 nm SiO_2 passivation layer that Δ_{BS} plays the most significant role for energies down to 1.5 keV while Δ_{DL} dominates below that value. The present results are also consistent with this picture. A slight increase in the boron layer thickness, from 1.8 nm to 5 nm, considerably affects low-energy electron detection lowering it from 60% to 23% for 500 eV, and from 74% to 56% for 1 keV. Adding 15 nm of AlN on top of the 1.8 nm boron layer suppresses 500 eV detection, while an extra annealing step combined with 50 nm epi-Si and 15 nm AlN completely blocks the photodiode from detecting energies less than 1 keV as specified in Table 2.2. In the analysis made here by extracting G_{TH} , the effect of backscatter losses is corrected for by the basckscatter coefficient η which is fixed at 0.05. This is a relatively small effect. Together with the fact that the samples P1.8B and P5B have a very similar surface, as do the pair P1.8(AlN) and P1.8(Si,AlN), it is very plausible that material-dependent backscatter-coefficient effects are not playing any significant role for the measured differences in gain.

FIGURE 2.15:

Measured relative electron signal gain for photdiode P1.8B with a 1.8 nm boron layer and 2 commercially available photodiodes: a backscattered-electron detector (BSE) and a low Voltage high Contrast Detector (vCD).



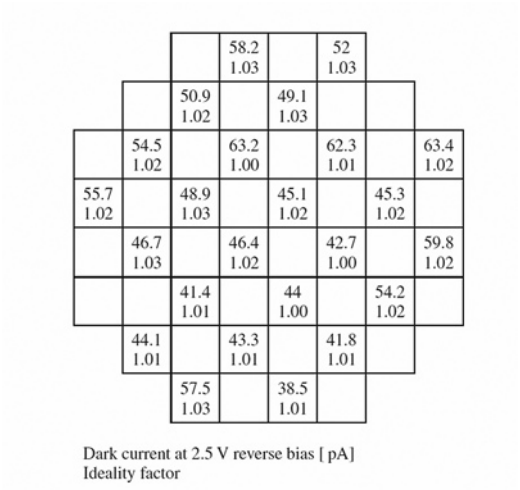
In Fig. 2.15, the B-layer photodiode P1.8B is compared to two commercially available detectors, a backscattered-electron (BSE) detector and a “low Voltage high Contrast Detector” (vCD) detector, that are both currently used in SEM systems. With such a thin front-entrance window of only 1.8 nm B, the B-layer photodiode achieves 60% of the theoretical gain value at 500 eV electron beam energy as compared to 14% for the BSE detector and 40% for the vCD detector [42]. Similarly, at 1 keV gain reaches 74% of the theoretical value that corresponds to 4.1 and 1.5 times improvement over the BSE and vCD detectors, respectively. A significant performance advantage is maintained up to almost 10 keV at which point they all tend towards the 97% level. For higher energies the electrons, as reported in [2], will start to travel so deep into the Si that a much wider depletion region, i.e., a much more lightly-doped Si, is needed to detect all of the incoming beam.

2.6.3 Dark Current Stability of PureB Photodiodes

To test the electrical stability of the PureB photodiodes during electron irradiation, the I-V characteristics were monitored for several different exposures. The characteristics over the wafer before exposure are given in the wafer map of Fig. 2.16, where the values of the dark current recorded at 2.5 V reverse bias are shown along with the corresponding ideality factors. An average dark current density of 0.595 pA/mm^2 is found with a standard deviation over the wafer of only 0.089 pA/mm^2. The small spread in values substantiates that the boron layer has a good Si-coverage on all dies over the whole wafer, even for this minimal thickness of only 1.8 nm. The overall behavior is ideal with a very narrow spread of the ideality factors of 1.02 ± 0.01 over the wafer.

FIGURE 2.16:

Over-the-wafer measurements of the dark current in pA at 2.5 V reverse bias (upper number), and the ideality factor *n* (lower number) of non-irradiated diodes.



The dark current is then measured after exposing the unbiased devices for 10 min to 1 keV, 5 keV, 10 keV, 15 keV, 20 keV, and 25 keV electrons in the Phillips XL50 SEM in scanning mode. For this microscope the maximum current on the specimen surface at the applied spot size is 10 nA. The devices are exposed on-wafer in areas of 1×1 mm^2. For one group of devices the center of the device is exposed far from the perimeter of the active photosensitive area (spot 1 in Fig. 2.17), and another group is exposed in 1×1 mm^2 areas at the edge of the device so that the spot covers part of the oxide isolation region, which in this case is completely covered with the contact metallization (spot 2 in Fig. 2.17). In this way, bulk and edge degradation effects can be separated. As can be seen in Table 2.3, the exposure in the center of the device did not modify the dark current, indicating that the B-layer junction is

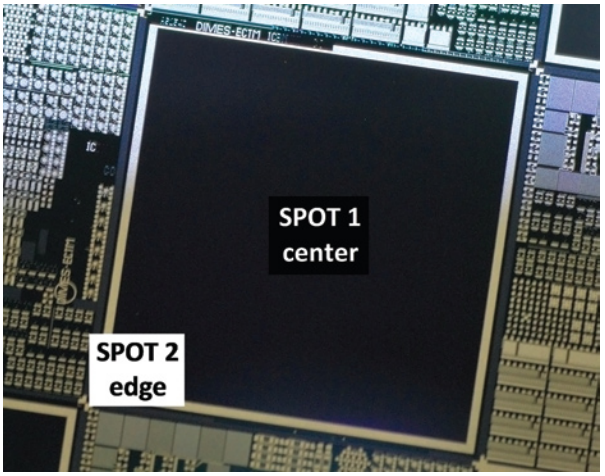


FIGURE 2.17:

A photograph of a diode where the 1×1 mm² irradiation sites are indicated (not drawn to scale).

not degraded by electrons with energies of 1-25 keV. However, exposing the edge of the device results in up to a factor 5 higher dark current values at 2.5 V reverse bias for electron energies of 10-25 keV. This is in accordance with the fact that electrons with energies lower than 10 keV are not expected to be able to go through the metal layer to the oxide. From the universal curve calculation of Everhart and Hoff [2], the electron range in Al will be only 283 nm for 5 keV electrons and 833 nm for 10 keV, which becomes comparable to the Al-thickness of 1 μm. Electrons that do not reach the oxide may charge the Al but they will be removed during biasing of the diodes. In contrast, higher energy electrons can reach the oxide. This can cause charging of the oxide and also degrade the interface passivation. Both effects can lead to an increased dark current, which is in fact observed here. The I-V characteristics of the diodes exposed with 25 keV electrons, both in the center and at the edge,

Electron energy [keV] (10 min exposure)		*1*	*5*	*10*	*15*	*20*	*25*
Exposure in the Center (Spot 1)	Initial dark current [pA]	41.8	43.3	41.4	54.2	44	50.9
	Dark current after irradiation [pA]	47.5	45.3	43.3	51.6	47.4	48.8
Exposure at the Edge (Spot 2)	Initial dark current [pA]	59.8	42.7	46.4	46.7	48.9	49.1
	Dark current after irradiation [pA]	47.3	48.4	77.2	236	204	206.9
	Dark current after irradiation and 1h @ 200°C bake	38.4	37	43.3	53.2	45.8	43.8

TABLE 2.3:

Measured dark current degradation at 2.5 V reverse bias in the center and at the edge of the device during 10 min electron irradiation.

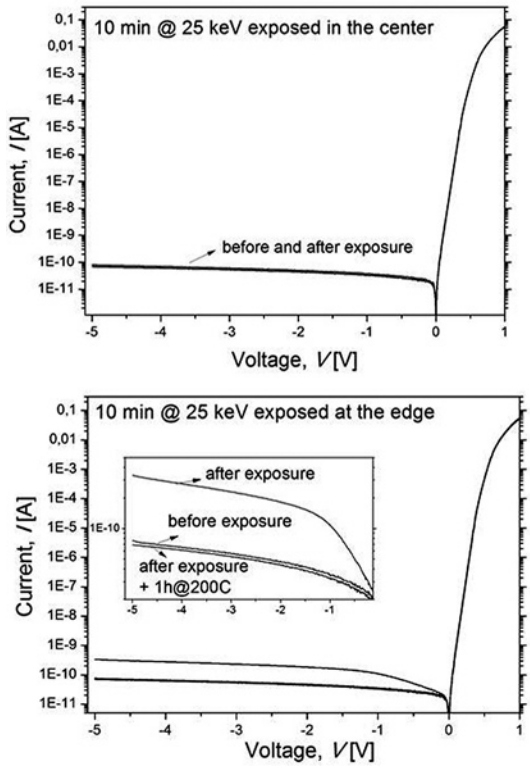


FIGURE 2.18:

(above) The I-V characteristics of a photodiode before and after a 10 min electron-irradiation at 25 keV when exposed in the center, and (below) when exposed at the edge of the device, with and without a final 200°C thermal annealing step.

are shown in Fig. 2.18. Also added in Fig. 2.18 and Table 2.3 are the current measurements after thermal annealing of the wafer at 200°C for 60 min. The current has returned to the pre-exposure level, indicating that the damage has been removed. This could be explained by the commonly observed effect that irradiation can disrupt hydrogen-bonds that are intentionally formed during alloying to reduce the oxide/silicon interface trap density [43]. It is well-known that these H-bonds can be restored by thermal annealing even at very low temperatures. Based on these results it can be concluded that dark current degradation is caused by perimeter oxide-related effects, and the PureB photosensitive region is not significantly affected by irradiation. In accordance with these results, also no optical degradation was observed during any of the optical testing.

2.7 Conclusions

The presented results demonstrate the high-quality of the PureB photodiodes for the detection of low-energy electrons measured down to 500 eV. The optical results confirm that minimizing the thickness of the PureB layers is the key to obtaining good efficiency at such low electron energies. For a 700°C deposition, the low boron diffusivity in the Si ensures a dead-layer of only a few nm when a 1.8-nm PureB is formed. The uniformity of 1.8-nm-thin PureB deposition is investigated over the wafer and optimized using oxide-etch mask design that balances the surrounding oxide area of the oxide-to-Si opening. Optimized oxide per Si ratio over the wafer evens out the consumption/loading effect of the oxide, thus providing uniform over-the-wafer PureB deposition.

Due to the etch resistance of the PureB and its ability to function as a barrier layer between the Si substrate and the pure-Al-metallization, all other processing layers can be removed, leaving only the thin PureB as a front-entrance window. For this 1.8-nm PureB device, the relative electron signal gain is high, reaching even 60% at an electron energy of 500 eV, as compared to a gain of respectively 14% or 40% for two current state-of-art electron detectors used in SEM systems. The diode I-V characteristics are ideal and uniform over the wafer with low dark currents of 0.595 ± 0.089 pA/mm^2 and ideality factors of 1.02 ± 0.01. Moreover, the PureB junction itself showed neither signs of optical nor electrical degradation. Only for electron energies above 10 keV some increase in dark current was observed for 10-min-long irradiation. This was related to the photodiode perimeter, probably due to damage of the isolation-oxide interface, and the pre-exposure dark current was restored by low-temperature annealing. All in all, the PureB technology offers a high-yield, high-performance photodiode process that can be valuable for low-energy (backscattered) electron imaging/detection.

ARSENIC-DOPED HIGH-RESISTIVITY SILICON EPITAXIAL LAYERS FOR INTEGRATING LOW CAPACITANCE DIODES

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ARSENIC-DOPED HIGH-RESISTIVITY SILICON EPITAXIAL LAYERS FOR INTEGRATING LOW CAPACITANCE DIODES

3.1 Introduction

The central issue studied in this chapter is the response time of the PureB photodiodes. It is ruled by the RC constant, i.e., the series resistance R and junction capacitance C of the photodiodes comprising the detector. In some cases the Si substrate is used as the one terminal of the photodiode, in which case the substrate doping can be decisive for the overall RC. The wider the depletion over the diode junction, i.e., the lower the doping, the lower the C, and the higher the doping is in the non-depleted region, the lower the R. Therefore, a trade-off should be made when choosing the doping level assuming it is uniform throughout the substrate. One solution is to use high-resistivity Si (HRS) substrates that can be fully-depleted, as has been demonstrated for single photodiode X-ray detectors [44]. The lateral spread of the depletion is then about the same size as the thickness of the wafer which is usually greater than 250 μm. This means that for multi-segment detectors the individual photodiodes should be electrically isolated by a distance that is much greater than this. However, modern solid-state detectors demand flexible multi-segmentation (pixelization) of the photosensitive surface with closely-packed segments [45]. This implies that their depletion region has to be vertically wide to obtain the low capacitance and series resistance, but laterally limited in order for neighboring detector segments (adjacent diodes) to function independently. One solution is to fabricate detectors on high resistivity, high-quality, thick epitaxial layers, grown on low-to-medium resistivity substrates, thus providing wide depletion, lateral isolation, and low series resistance through the substrate.

The use of epitaxially grown, thick, HRS layers for radiation detection has been investigated in the past for the ability to enhance the radiation hardness at high radiation fluences [46, 47]. Layers were grown > 100-μm-thick with a resistivity of a few kΩcm that contained a high concentration of deep level traps. These traps served as “sinks” for radiation induced interstitial defects, minimizing the radiation-induced damage of the detector. As a drawback, the dark current is increased to a level that is unacceptable for many applications such as the low-energy electron detectors that have motivated the work presented in this thesis. The PureB detectors have been developed for use in advanced Scanning Electron Microscope (SEM) systems and require speed that translates into an R of less than 100 Ω and a C of less than 5 pF/mm^2. This can be achieved with a depletion width over the photodiode junctions of about 30 μm. To maintain a separation of segments of 100 μm, this requires a doping of 10^{12}-10^{13} cm^{-3}.

In the present work, up to 40-μm-thick high-quality defect-free epi-layers are grown in a commercial Si/SiGe chemical-vapor-deposition (CVD) epitaxial reactor system [48]. For achieving the required light doping levels, doping from arsine rather than phosphine is preferred because of the much higher incorporation levels of phosphorus. However, using arsine is challenging due to its strong tendency to segregate on the surface and cause auto-doping effects. Past work has shown that these properties can be controlled and applied with benefit to create special doping profiles [49, 50]. Moreover, with the close to intrinsic n-type doping levels warranted for the application described here, the growth process needs to be proofed against p-type counter-doping at the wafer surface that can come from chamber contamination. This issue has been separately addressed in this chapter, and the methods for measuring and controling it are proposed. Finally, a technique is proposed for a controlled segregation, removal, and auto-doping of As to obtain the required very lowly doped profiles.

3.2 Experimental Material

3.2.1 Arsenic Doping Control

The growth of the n-type Si epi-layer is carried out in an ASMI Epsilon One reactor using dichlorosilane (DCS) and arsine (AsH_3) as precursors for Si and As, respectively. As a first step, a "seed" layer of As-doped Si is grown on the wafer. From this layer the As atoms segregate on the surface and are removed by a high temperature baking step (desorption step) at 1100°C. After that, the thick epi-layer is grown in several steps with only the DCS turned on, performing a desorption bake after each step to remove the As from the surface. The doping concentration and the doping profile of the obtained epi-layers are determined by As segregation where, depending on the temperature of the deposition, only a fraction of segregated As atoms gets incorporated into the as-grown layer, while the rest remains on the layer surface [51]. The final doping level can be calculated as

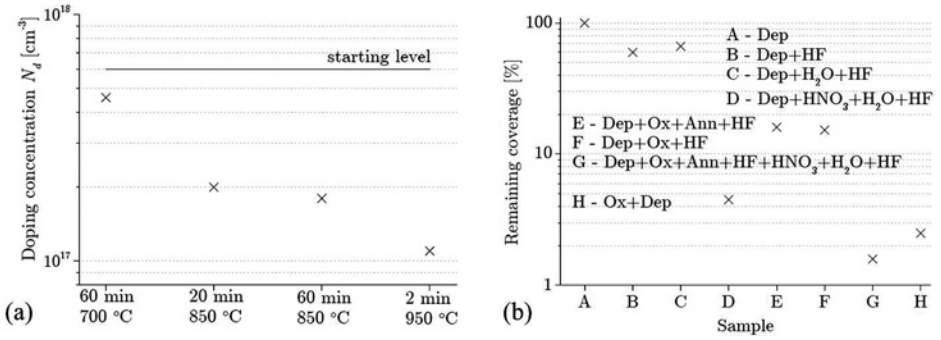
$$N_d(x) = i_R N_{Si}\theta(t), \tag{3.1}$$

where N_{Si} is the Si concentration of 5×10^{22} cm^{-3} , i_R the incorporation rate, and $\theta(t)$ the percentage of a full As monolayer, N_{ML} = 6.8×10^{14} cm^{-2}, covering the surface. While the incorporation rate depends mainly on the solid solubility of the As atoms in Si at the defined deposition temperature, the surface coverage $\theta(t)$ is governed by the mass balance of the following four processes: adsorption of the As atoms on the surface (*Ads*), segregation (*Seg*), desorption from the surface (*Des*), and incorporation into the epi-layer (*Inc*):

$$\theta(t) = Ads + Seg - Inc - Des, \tag{3.2}$$

FIGURE 3.1:

(a) Reduction in maximal doping level after baking the sample at different temperatures; (b) Reduction of the As surface coverage with different ex-situ chemical cleaning steps [49].



To obtain low doping concentrations, the surface coverage $\theta(t)$ should be low, and therefore the adsorption of the As atoms needs to be minimized and the desorption maximized. The surface concentration is then restricted by the segregation and incorporation rates and their mutual interactions. To minimize adsorption, the dopant gas AsH_3 is turned off during the growth of the low-doped epi-layer. Moreover, the desorption of the segregated atoms is enhanced by applying a high temperature baking step prior to each new growth cycle. The desorption baking step has been characterized in several studies of situations where it is important to have precise control of the As covering the Si (100) surface [52–54]. Some of the results are shown in Fig. 3.1 where it can be seen that there is a strong temperature dependence of the desorption, while the effect saturates in time so that 20 min or 60 min at 850°C give practically the same result [49]. The 2 min 1100°C bake step used in this work is commonly used, also in combination with high-dose As-implanted buried layers, to reduce the As surface coverage. The residual As segregated on the surface after the baking step supplies As for incorporation during the subsequent Si-epi growth, which is essentially an auto-doping mechanism. The segregated As atoms which neither desorb from the surface nor incorporate in the Si remain at the top surface of the epi-layer in a float-like manner, or more precisely, Si dangling bonds are replaced by lone pairs of As electrons. At the end of a growth sequence, the residual segregated As on the wafer surface can be removed chemically. The desorption efficiency as a function of chemical processing is illustrated in the Fig. 3.1b [52]. This is done here by cleaning successively in HNO_3, H_2O, and HF before further processing such as the deposition of the PureB anode region. When the supply of arsine is turned off, and an initial As coverage that gives an incorporated doping of $N_d(0)$ is present, then Eq. 3.1 can be reduced to describe the doping from further incorporation from the remaining As coverage as an exponentially decreasing profile

$$N_d(x) = N_d(0) exp\left(-\frac{i_R N_{Si} x}{N_{ML}}\right) \tag{3.3}$$

where $L = N_{ML}/i_R N_{Si}$ is the characteristic length which describes the incorporation rate at the given process temperature [52].

Since the overall doping level is very low, the resulting doping may be influenced by the background doping in the chamber which will set the minimal obtainable doping level. Therefore, it is vital to thoroughly clean the chamber before deposition. The growth of the seed layer itself may also contribute to the chamber background level. The final profile of the first few micron of the epi is dominated by up-diffusion of the As. Since the growth rate is around 1 μm/min, and layers as thick as 40 μm are grown, we can assume that the up-diffusion of As from the seed layer can be up to 10 μm when the growth temperature of 1050°C and the bake steps at 1100°C are taken into account.

3.2.2 Thick High-Resistivity Epi-Layer Growth

Experiments are performed using n-type (100) 2-5 Ωcm Si substrates. To ensure a native-oxide-free surface, they are dip etched for 4 min in HF 0.5%, Marangoni dried just before the epitaxy, and in the epitaxial reactor itself the wafers are baked at 1100°C. A 300-nm-thick As-doped seed layer is then grown at 1050°C with a doping concentration of either 10^{16} or 10^{17} cm^{-3}. The seed doping level has to be both low enough to produce the low capacitance values, and high enough to prevent the counter doping phenomenon. The trade-offs for the resulting doping profiles and capacitances for both 10^{16} or 10^{17} cm^{-3} will be discussed in the following sections. The seed layer formation is followed by a desorption step at 1100°C to remove the As atoms that have segregated on the surface. The arsine is turned off and a series of Si layers are grown at 1050°C to a thickness of 5 μm, 10 μm, 20 μm, and 40 μm. The latter two layers of 20 μm and 40 μm may be grown in steps of 10 or 20 μm, to lower the risk of excessive deposition on the chamber walls during the long growth cycles involved.

3.2.3 Photodiode Fabrication

The thick epi-layer substrates are used for fabricating sets of photodiodes with low capacitance. A schematic of two adjacent diodes is presented in Fig. 3.2. First, the wafers are cleaned as described in the previous section to remove native oxide and reduce the As coverage on the surface. Then 200 nm of the thermal oxide is grown through which n^+-and p-type guard rings are implanted. After annealing the implantations, LPCVD oxide is deposited

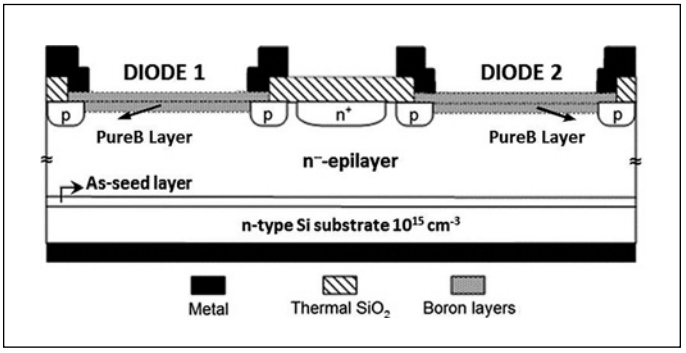


FIGURE 3.2:
Schematic cross-section of two adjacent PureB diodes fabricated on a low-doped epi-layer wafer.

and finally the oxide (both thermal and LPCVD) is patterned and etched, to form the anode openings of the photodiodes. The anode area used in the present work is 7.6 mm^2. The anodes are then deposited in an RPCVD reactor using the recently developed PureB technology, parameters of which are described in [33, 40]. In this technology a nanometer-thin amorphous pure boron layer is selectively deposited on an oxide-free Si surface at 700°C to form an ultrashallow junction that is reliable both electrically and optically [25]. Finally, metallization layers are deposited on the front and back of the wafer and patterned to form the anode contact pads and the cathode contact on the back of the wafer.

3.3 Epi-Layer Profile Engineering

When a high resistivity epi-layer is grown as described in the previous section, with a set temperature and pressure, the doping profile is essentially determined by three parameters: the total thickness of the epi-layer, the doping concentration of the seed layer, and the number of steps used to grow the lightly doped layer. In this section each parameter will be separately studied with respect to the resulting doping profile which is measured by C-V profiling [55]. The average carrier density *N(W)* and the space charge region width *W* are extracted from the C-V characteristics as follows:

$$N(W) = \frac{C^3}{q\varepsilon_0\varepsilon_s A^2 dC/dV} = \frac{2}{q\varepsilon_0\varepsilon_s A^2 d\left(1/C^2\right)/dV}, \tag{3.4}$$

$$W = \frac{\varepsilon_0\varepsilon_s A}{C}, \tag{3.5}$$

The C-V curve was measured with a capacitance meter set to series connection measurement at 1 MHz. According to [55], the instrumentation error in series connection can be calculated as

$$\%error = 0.1\sqrt{1+\left(2\pi f C_s R_s\right)^2}, \tag{3.6}$$

The typical values of capacitance and resistance measured in this work are 100 pF and 100 Ω, giving an instrumentation error of only 0.1%. The capacitance meter has a provision for the cable-length and contact corrections that were implemented prior to measuring.

In all the reported figures showing doping profiles, '0' depth on the x-axis corresponds to the upper surface of the detector where the detector anode is placed. Since the p^+-region is only a few nm deep, the depletion into this region can be set at 0 μm without loss of profiling accuracy. The left y-axis displays the carrier density, and the right y-axis the reverse voltage value at which the depletion width (x-axis) and the doping density (left-y-axis) are obtained. In the extraction of the profile it is assumed that parasitic capacitances can be neglected in view of the large diode area. These parasitics include the diode perimeter capacitance that gives higher contribution at the edge of the diode due to the guard ring distances, and the

MOS capacitance under the tracks and pads connecting the diode. An extensive simulation analysis of the perimeter effects of PureB diodes has been made and is in part published in [56], where it is found that for the present device structure the bulk capacitance is 3.52×10^{-18} F/μm^2 while the perimeter capacitance is 1.1×10^{-16} F/μm. These parameters are simulated for the 40-μm-thick epi-layer that has the uniform doping of 5×10^{12} cm^{-3}. Under these conditions, the toroidal-shaped diode considered here with an area of 7.6 mm^2, and a perimeter of 23 mm, has the bulk capacitance of 26.7 pF and the perimeter capacitance of only 2.53 pF. This 10% contribution of the perimeter will have some influence on the value of the extracted capacitance but, relatively, it will result in higher doping the higher the actual doping is. Therefore, the comparisons that are made remain valid. For an entirely correct extraction of the doping profiles, a differential C-V measurement should be made to completely eliminate perimeter effects. One more correction that has to be taken into account for very low doping concentrations that drop below 10^{12} cm^{-3} is the depletion region at 0 V bias that already penetrates the space charge region for more than 15 μm. Thus, a small forward voltage (up to 0.3 V) is required to profile the dopants in the upper parts of the epi-layer. At a certain voltage, measured here around 0.15 V, the diffusion capacitance starts affecting the measurement results, giving a non-physical increase in the doping concentration of the layer that will be disregarded.

3.3.1 Epi-Layer Thickness

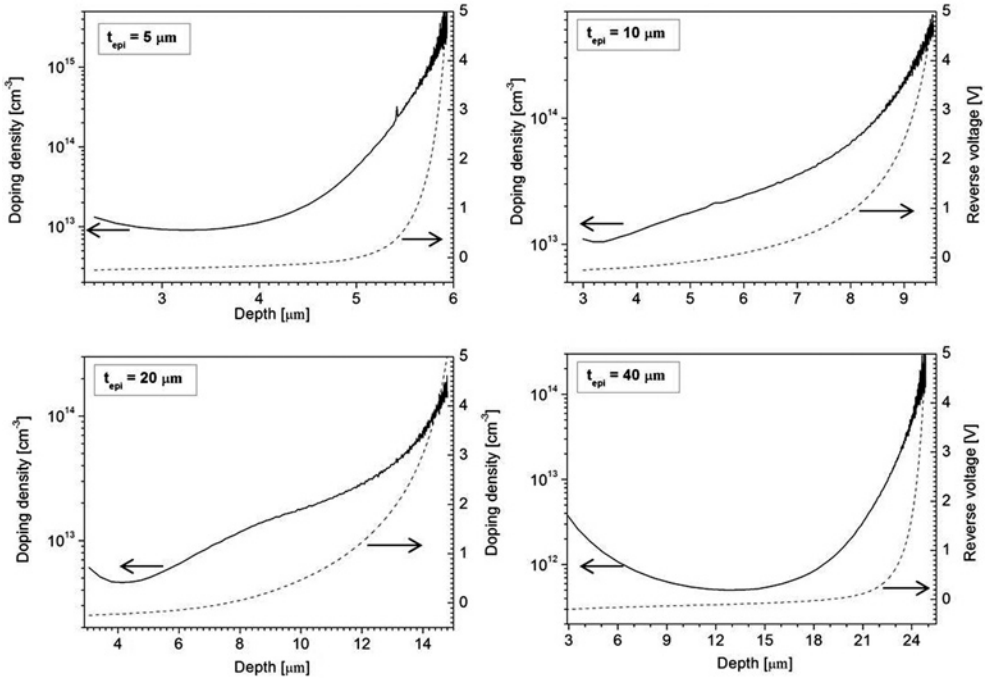


FIGURE 3.3:

CV-doping profiles and reverse bias as a function of depletion width for As-doped epitaxial layers grown to a thickness of 5 μm, 10 μm, 20 μm, and 40 μm.

The choice of the epi-layer thickness is determined by the application. In this work, the requirements were set by the application of the photodiodes in high-responsivity back-scattered-electron detectors used in SEM systems. In such systems, the electron energies typically range up to 30 keV at which the electrons will penetrate the Si bulk no more than 10 μm [2]. Hence, an epi-layer that can be depleted to 10 μm at the operating voltage needs to be fabricated. However, the capacitance specification of < 5 pF/mm^2 dictates a much thicker depletion width. Fig. 3.3 shows the doping profiles of four epi layers of thickness 5 μm, 10 μm, 20 μm, and 40 μm. It can be seen that the depletion widths at an operating voltage of 3 V reverse bias are around 6 µm, 9 µm, 14 μm, and 25 μm, respectively. Even if the 5 μm, 10 μm, and 20 μm layers were to be fully depleted by a higher voltage, only the 40-μm-thick epi-layer would meet the specifications of < 5 pF/mm^2.

The undepleted part of the layer must also be taken into account because it can be decisive for the series resistance. For example, the 20 μm and 40 μm epilayers are not fully depleted at 3 V and the undepleted region will contribute to the series resistance of the photodiodes. As demonstrated by the graphs in Fig. 3.4 the series resistance is about 20 Ω higher than for the 10-μm-epi case at voltages higher than 3 V, while it increases dramatically as the voltage goes to lower values at which the undepleted region is wider. Therefore, the epi-layer thickness should be as close as possible to the targeted depletion thickness for an optimal trade-off between capacitance and resistance. The respective capacitance values measured at 3 V are 135 pF, 86 pF, 56.5 pF, and 32 pF, as indicated in Fig. 3.5.

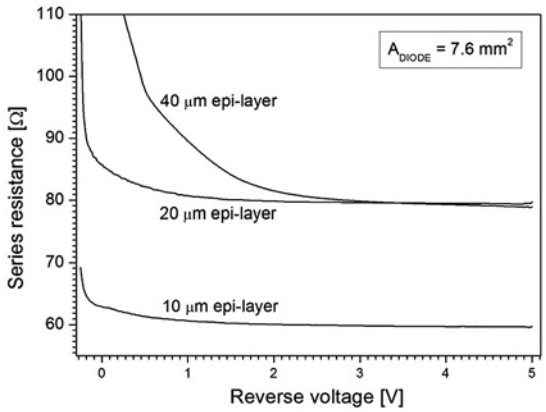


FIGURE 3.4:

Series resistance of the 7.6 mm^2-area diode for 10 μm, 20 μm, and 40 μm epi-layer thicknesses displaying the influence of the undepleted remnant of the epi layer.

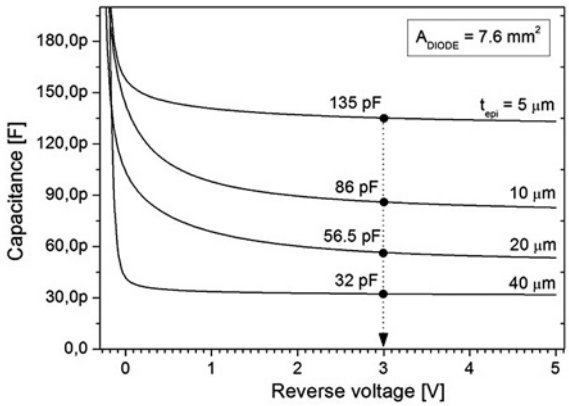


FIGURE 3.5:

Capacitance measurements for photodiodes with 7.6 mm^2 anode area fabricated on the substrates characterized in Fig. 3.3.

3.3.2 Arsenic Seed-Layer Doping

Since the growing of the As-doped seed layer defines the As-segregated surface doping and the background doping level of the chamber, its concentration is decisive for the doping of the lightly-doped epi. In the example shown in Fig. 3.6, several different 40-μm-thick substrates with seed layer concentrations of 10^{16} and 10^{17} cm^{-3} have been profiled.

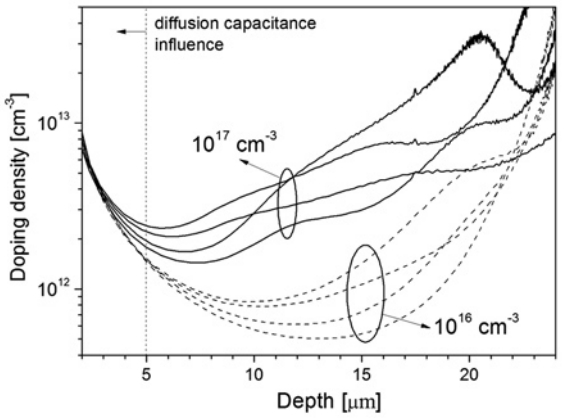


FIGURE 3.6:

CV-doping profiles of 40-μm-thick epi-layers with 10^{16} and 10^{17} cm^{-3} As-seed layer concentrations. The doping is profiled up to 5 V reverse bias (W = 25 μm).

The samples with a 10^{17} cm^{-3} seed-layer exhibit profiles which are up to an order of magnitude higher in concentration than the samples with the 10^{16} cm^{-3} seed-layers, as indicated in Fig. 3.6. For example, the doping density for the 10^{17} cm^{-3} seed-layer sample at the depth of 10 μm is 4×10^{12} cm^{-3}, while for the 10^{16} cm^{-3} sample it drops to 6×10^{11} cm^{-3}. Correspondingly, the voltage required to deplete the first 10 μm of the substrate differs around 0.5 V in value. This causes a spread of capacitance values at 3 V operating voltage of up to 30%, ranging from 30 pF to 40 pF as shown in Fig. 3.7.

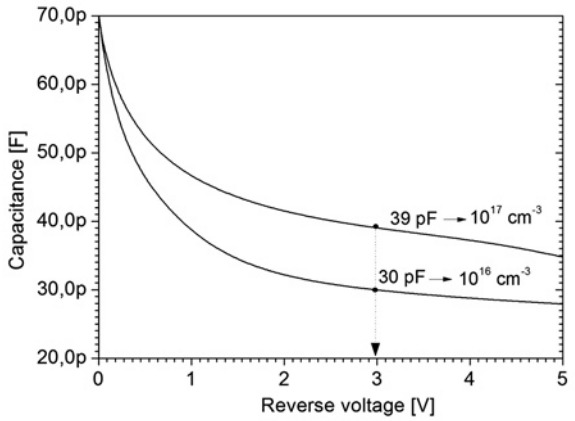


FIGURE 3.7:

Capacitance measurements of 40-μm-thick epi-layers with 10^{16} and 10^{17} cm^{-3} As-seed layer concentrations.

3.3.3 Epi-Layer Growth Cycles

Besides the differences in the doping level of epi-layers related to different seed layer concentrations, non-uniformities in the layer doping are also detected when different growth cycles are introduced. In Fig. 3.8 three distinct 40-μm profiles are shown, each grown in a different manner: in one go, in steps of 10 μm, or steps of 20 μm. With the 10-μm steps, bumps of increase in the doping are seen at about 10 μm and 20 μm, as marked in the figure. Likewise, for the 20-μm steps a bump is seen at about 20 μm. The increase in doping can be caused by a combination of increased segregation of As on the surface during the 1100°C baking step, as well as doping from the background contamination of the chamber. The shape of the bumps is determined by the total temperature processing. Both effects will be stronger when a high seed-layer doping is implemented. In the following Si growth that proceeds at 1050°C, the bump doping decreases in accordance with the fact that the As surface concentration is slowly built in, and at the same time the background level in the chamber is also slowly consumed.

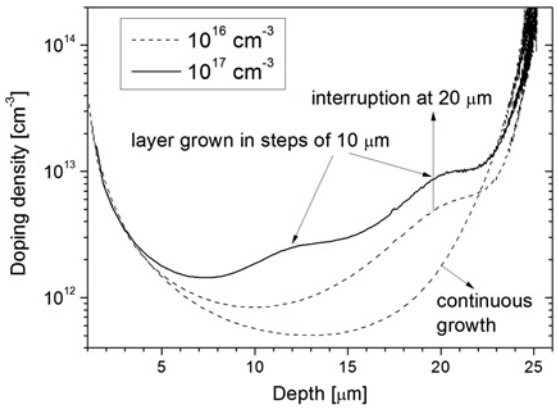


FIGURE 3.8:

CV-doping profiles for 40-μm-thick layer grown either in one go, in 10 μm steps, or 20 μm steps. The doping is profiled up to 5 V reverse bias (W = 25 μm).

Comparing the two 10^{16} cm^{-3} seed-layer samples, it can be seen that the doping density significantly depends on whether the layer was grown continuously, or with the interruptions. In the vicinity of the bump at 20 μm depth, the doping value rises from around 2×10^{12} cm^{-3} to 5.5×10^{12} cm^{-3} and further on remains slightly higher throughout the whole layer. The growth that is carried out in steps is favorable in cases when the epi-layer doping level drops low, typically at the end of the growth sequence as the available As doping gets consumed. This increases the danger of p-type counter-doping due to chamber contamination. In cases where such unintentional p-type counter-doping was encountered it was impossible to perform C-V profiling because the diode is not well isolated from the rest of the wafer and very high leakage currents result. However, the p-doping can be identified by connecting two adjacent diodes shown in Fig. 3.2 in a JFET operation mode where the two anodes function as source/drain and the cathode functions as a gate to modulate the channel. An example of such a measurement is shown in Fig. 3.9 where the output and transfer characteristics show a clear JFET-like behavior, with a pinch-off voltage of about 0.2 V. The pinch-off voltage

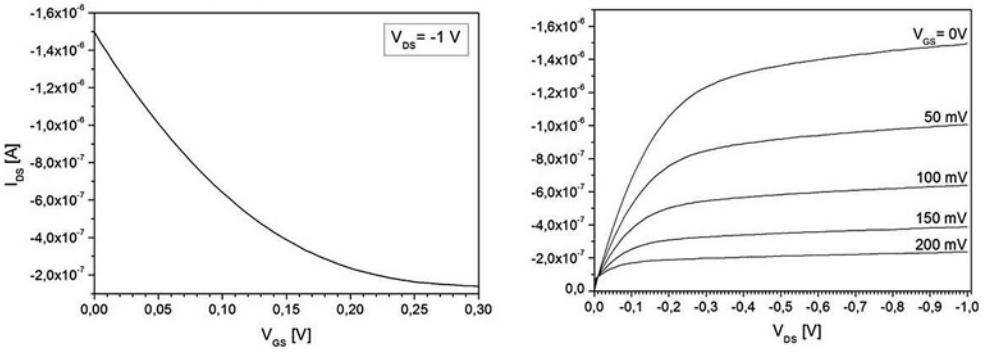


FIGURE 3.9:

Transfer and output characteristics of the parasitic JFET between two adjacent diodes caused by p-type counter-doping of the n-epi.

and the on-currents are much higher than the ideal case without p-type counter-doping. In Fig. 3.10 the measurement is shown as performed on well-isolated adjacent diodes and it can be seen that the current levels correspond to leakage current levels of about 50 pA of the diodes themselves.

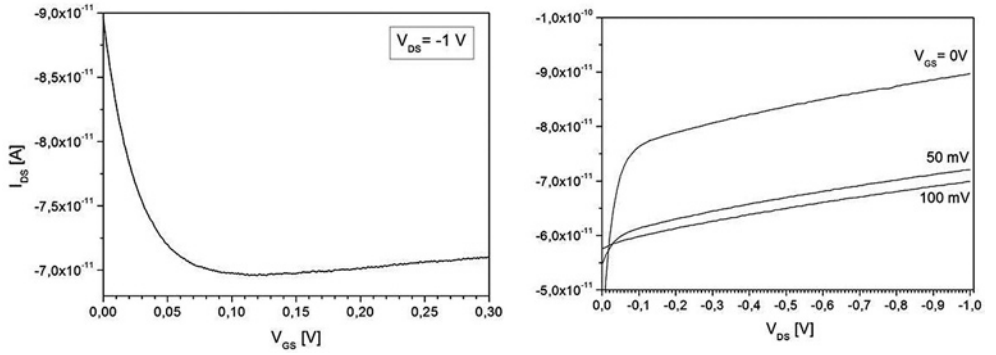


FIGURE 3.10:

Transfer and output characteristics between two adjacent diodes that are well isolated, i.e., have no p-type counter-doping of the n-epi.

3.4 Quality of the Epi-Layers

The quality of the epi-layers studied here is evaluated using three parameters: the stacking fault density, the level of the dark current of the fabricated diodes, and doping uniformity across the wafer. The density of stacking faults depends on the quality of the starting substrate, but for low levels these faults do not impact the final performance of the mm^2-large diodes as reported in [57]. The dark current level reflects the number of active generation-recombination centers in the epi-layer, and the doping uniformity is a measure of the reliability of the growth method.

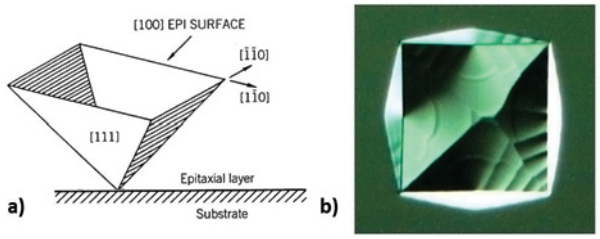


FIGURE 3.11:
(a) Stacking fault geometry on (100) silicon [58];
(b) SEM image of a stacking fault grown in a silicon epitaxial layer of 40 μm thickness.

Stacking faults are pyramid-shaped crystallographic defects caused by a lattice mismatch at the surface of the substrate, or during the growth. Typical geometries are shown in Fig. 3.11. The final size which is observed on the wafer surface depends on the depth of the first disruption that initiated the stacking fault, and is reported up to around 70×70 μm^2 in this work for 40-μm-thick layers (Fig. 3.12(a)). Despite the size, for the PureB diodes a limited number of such defects does not affect the performance in terms of dark current, capacitance, and optical responsivity of the photodiodes. This is because the diodes are large and the PureB technology provides conformal coverage of the anode surface even when deviating crystallographic orientations are present, as shown in Fig. 3.12(b) [40]. The density of the stacking faults is mainly counted to be about 2 per cm^2.

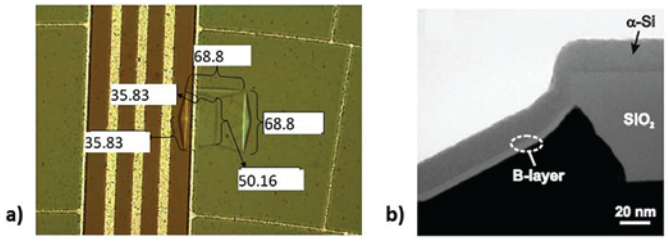


FIGURE 3.12:
(a) Optical image of a stacking fault at the edge of a photodiode surface showing neighbouring metal tracks and dimensions in microns, epi-thickness 40 μm.
(b) TEM image showing conformal growth of a PureB layer [40].

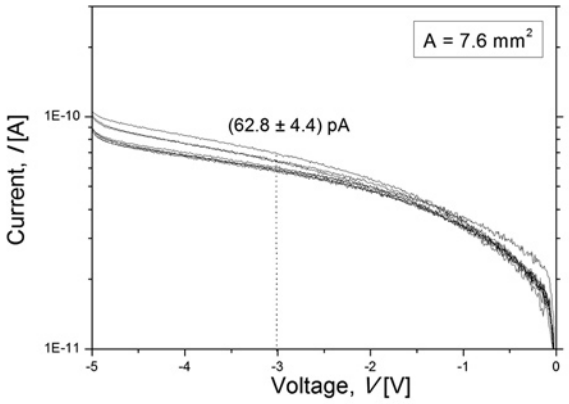


FIGURE 3.13:

Reverse current of a PureB photodiode fabricated on a 40 μm thick epi-layer.

The dark current is measured on several diodes fabricated on the 40-μm-thick epi-layer and exhibits a very low current level measured up to 5 V reverse bias with a small spread over the wafer as seen in Fig. 3.13. The average measured dark current is 63 pA at 3 V reverse bias and consists of bulk and surface generation-recombination currents as well as the diffusion current component. If, in the worst case, all leakage current is dominated by the bulk generation current in the epilayer, assuming the complete suppression of the surface generation current and a negligible diffusion current, it could be calculated as

$$I_{bulk} = q\frac{n_i}{2\tau_g}AW_{depl}, \tag{3.7}$$

where q is the charge unit, n_i is the intrinsic carrier concentration, τ_g is the generation lifetime, A is the anode area of the detector of 7.6 mm^2, and W_{depl} is the width of the depletion region of 25 μm at 3 V reverse bias (Fig. 3.13). Then the generation lifetime is estimated to be 2.5 ms. Moreover, due to the neglected leakage current components, it is safe to claim that the generation lifetime for the 40 μm thick epi-layer is > 2.5 ms. This is more than an order of magnitude higher than the 100 μs lifetime of the thick, high-resistivity epi-layers reported in [46]. The over-the-wafer doping uniformity is evaluated for the 40-μm-thick epi-layers from 52 measurement points over the 4-inch wafer. The circular spread of doping visible in Fig. 3.14 correlates with the rotation of the wafer on the susceptor during deposition, and the drop in doping density towards the wafer center is in accordance with dopant source depletion as is common in epitaxial processes. The values presented in the figure are extracted for a depth of 25 μm from the wafer surface that corresponds to 3 V reverse bias. The doping uniformity over the wafer is calculated as a standard deviation over the average doping (σ/average) to be 3.6%.

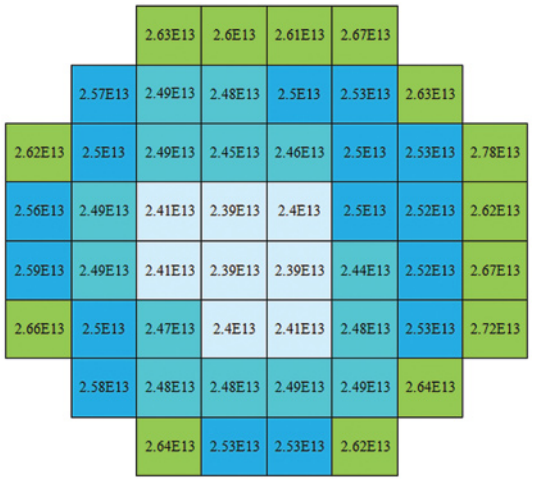


FIGURE 3.14:

Over-the-wafer doping density in atoms-cm^{-3} measured by CV-profiling on 52 diodes with 7.6-mm^2 anode-area at 3 V reverse bias.

3.5 Implementation of As-Doped Epi-Layer in SEM Backscattered-Electron Detectors

Modern solid-state electron detectors require a high degree of design freedom and flexibility. This includes the segmentation of the photosensitive surface of a large-area detector into a number of detector segments that can function independently, or in groups as the application dictates. The motivation for this is to detect not only the amount of incident particles, but also their position and the angular distribution. An example of an 8-segment layout is given in Fig. 3.15, and it is demonstrated how the individual segments can be grouped (Fig.

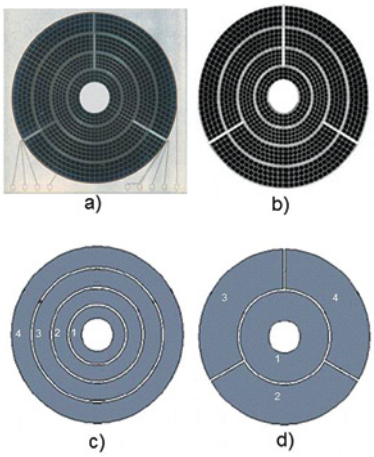


FIGURE 3.15:

(a) Photograph of the PureB detector;

(b) The electron detector consists of eight segments that can be used in two modes by combining the signal of segments into the

(c) CBS-Concentric Back-Scattered and

(d) ABS-AngularBack-Scattered mode.

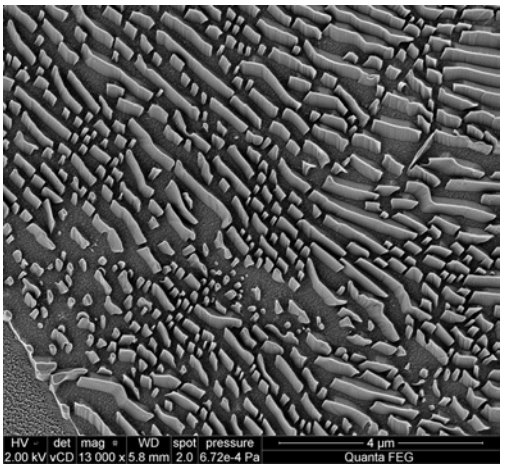


FIGURE 3.16:

SEM image of a metal surface taken at 2 kV with the Concentric-Backscattered configuration (Fig. 3.15(c)) of a PureB electron detector [59]. (*Image courtesy of FEI Company***)**

3.15(c, d)). When designing detectors for SEM systems, there is a trade-off between the packing density of the segments and the doping of the epi, i.e., the capacitance. In this work a separation between segments of 100 μm for the 40-μm-thick epi-layers was achieved together with a capacitance of 30 pF for the 7.6 mm^2 detector area. Thus the < 5 pF/mm^2 specification was reached. An example of imaging with the segmented layout is given in Fig. 3.16, where the Concentric-Back-Scattered mode illustrated in Fig. 3.15(c) is used to enhance the topographical contrast of the inspected sample.

3.6 Conclusions

A method of growing high-resistivity, high-quality, thick epi-layers using the segregation behavior of arsenic for doping has been discussed. The epi-layers are grown on 2-5 Ωcm substrates, to a thicknesses of 5 μm, 10 μm, 20 μm, and 40 μm, and the doping levels are successfully reduced down to 5×10^{11} cm^{-3}. The doping level and the profile are discussed in terms of three main parameters: the arsenic dopant source concentration (seed layer), the growth cycles, and the total thickness of the layer. The concentration of the initially grown seed layer, that is an As-doped Si layer of 300 nm thickness and 10^{16} or 10^{17} cm^{-3} As concentration, clearly controls the overall doping level of the epi layer. Second, growing thick epilayers with interruptions in growth sequence, followed by a 1100°C baking step before continuing the growth, promotes As segregation to the surface. This gives a slight increase in doping around the place of growth interruption which can be beneficial for preventing the doping level from becoming too light and therefore susceptible to counter-doping from contamination in the epi chamber. Several layer thicknesses have been fabricated and studied with respect to capacitance and the resistance values of the diodes fabricated on such substrates. For 7.6 mm^2 diode areas with 40-μm-thick epi-layers, capacitance values as low as 30 pF have been achieved, together with a diode series resistance of 90 Ω at 3V reverse bias. A low dark current level is achieved and the presence of small concentrations of stacking faults does not degrade the dark current or capacitance of the diodes. The light n-doping is uniform within 3.6% over the 4-inch wafer.

4

PureB

BACKSCATTERED-ELECTRON DETECTOR FOR SCANNING ELECTRON MICROSCOPY

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4

PureB BACKSCATTERED-ELECTRON DETECTOR FOR SCANNING ELECTRON MICROSCOPY

4.1 Introduction

Several groups of detectors have been investigated that tackle the problem of low energy backscattered-electron detection, among others solid-state detectors and scintillator detectors, but so far they have not succeeded in going below the 1 keV detection threshold. Recently, a few novel solid-state detector structures were demonstrated to have appreciable responsivity values for sub-keV electrons down to 200 eV [11, 12, 59]. For example, one type of photodiode detector with a 6 nm passivation SiO_2 has shown a remarkably high detection efficiency at low-energies [11]. Further, Nikzad et al. also demonstrated devices with an exceptional low energy efficiency, but there are some unclear points about these results since there was a drop in detection efficiency at higher electron energies [12].

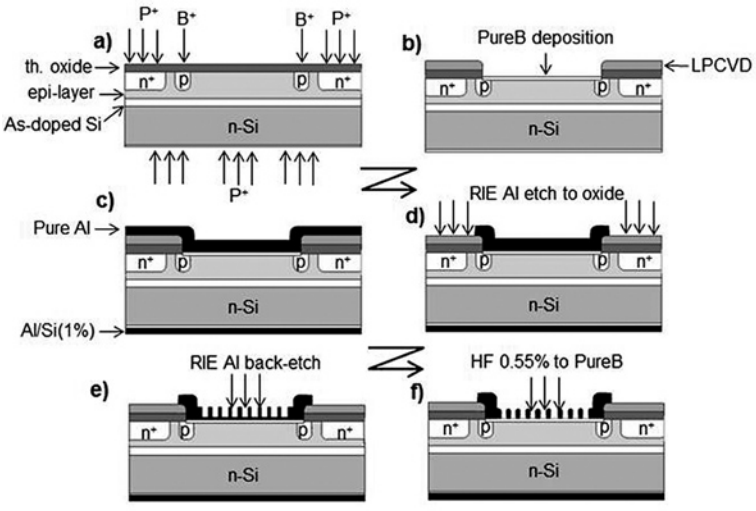
In this chapter, an alternative detector made in pure boron (PureB) technology is presented [25, 59, 60]. These diodes have been applied for the fabrication of next-generation BSE detectors and here a detailed description is given of the processing procedures employed to optimize the performance for use in advanced SEM systems. The main requirements are both a high detection efficiency for high-resolution imaging and a high scanning speed for fast imaging. The former is achieved by creating nm-thin anodes that are ultrashallow p^+n-junctions formed by PureB depositions, tailored for detection of low-penetration depth charged particles and radiation such as VUV, DUV, and EUV light [26, 34, 61] (Section 4.3).

The high scanning speed requirement translates into a low series resistance R and capacitance C, i.e., low RC constant of the photodiodes. This is implemented by combining a fine patterning of the aluminum electrode grid on the detector anode surface for lowering the series resistance (Section 4.5) with the growth of high-resistivity silicon epitaxial layers for obtaining the low capacitance (Section 4.4). In this work a segmentation of the detector surface into several closely-packed, electrically-isolated photodiodes was desired. To achieve both lateral electrical isolation of the segments, as well as low capacitance and low series resistance through the wafer, epi-layers of 40 μm-thick are grown on low resistivity wafers, rather than using high-resistivity wafers as is commonly done. The final processing step that is described in Section 4.6 is the bulk micromachining of through-wafer apertures that allows the positioning of the detector in the SEM system in such a manner that the electron beam can pass through the detector onto the sample from which the electrons are backscattered.

4.2 Basic Process Flow

The fabrication process is schematically described in Fig. 4.1. It starts with n-type (100) wafers with a resistivity of 2-5 Ωcm. The substrates are prepared as follows: a 300-nm-thick As-doped Si layer, doped to 10^{16} cm^{-3}, is grown in the ASMI Epsilon One epitaxial reactor at 1050°C and 60 Torr using arsine (AsH_3) as dopant gas. Immediately after this, the wafers are in-situ baked for 30 s at 1100°C in order to desorb the As atoms that have segregated on the layer surface. The epi-growth proceeds in cycles to achieve a total thickness of 40 μm. Dihlorsilane (DCS) gas is used and the doping of the layer in the range of 10^{12}-10^{13} cm^{-3} relies on the As segregation-incorporation dynamics from previously grown layers to supply doping. This As auto-doping process is described in more detail in Chapter 3, and the final parameters applied for the BSE detector fabrication are given in Section 4.4. The substrate preparation is completed with a thermal oxide passivation layer of 230 nm thick. Through the thermal oxide two guard rings are implanted. A p-type guard ring at the diode perimeter is formed by a B^+ implantation at 180 keV and an n-type guard ring separating neighboring diodes by a P^+ implantation at 300 keV. The significance of the n-type guard ring, that is an n^+-channel stop region, is separately discussed in Section 4.4.3. Ohmic contact to the back of the wafer is ensured by a blanket high-dose 150 keV P^+ implant (Fig. 4.1a). After the sequence of implantations, an additional 400 nm of tetraethoxysilane (TEOS) is deposited by low pressure chemical vapor deposition (LPCVD). The extra oxide is added in order to lower the contribution of the metal tracks to the device capacitance. The wafer is then annealed in argon gas for 35 min at 1000°C.

The boron layer anode formation is shown in Fig. 4.1b and described in detail in Section 4.3. It starts with lithographical anode area definition, from which the oxide is etched away in a buffered HF (BHF) solution down to the Si. An oxide-free surface is ensured by dip-etching in HF 0.55% followed by Marangoni drying. Finally, a baking step of 4 min at 800°C is performed in the epitaxial reactor just before deposition of an amorphous boron layer (PureB layer) for 2 min 40 s at 700°C. This results in a < 2 nm thickness of PureB and very limited diffusion of B in the Si. A detailed description of the PureB deposition conditions is given in [33]. When the wafers are taken out of the epitaxial reactor, both the front and back sides of the wafer are coated with Al (Fig. 4.1c). The metallization patterning directly on the PureB surface is a crucial step for obtaining optimal electron detection efficiency as well as low series resistance. It is carried out in three steps: first in Fig. 4.1d the diode interconnect and diode contact definition by dry etching of the aluminum to the oxide, then in Fig. 4.1e the Al-grid design on top of the PureB surface by reactive ion back-etching of aluminum down to a thickness of around 100 nm, and lastly in Fig. 4.1f the wet etch to the PureB layer that removes the remaining Al. Both dry-etching steps are performed in HBr/Cl_2 etching chemistries and the etched Al thickness is time-controlled at the given RF power and temperature. In the wet-etching step, landing on PureB layer is finalized in a HF 0.55% solution that is highly selective to the nm-thin boron layer. The obtained metal grid geometry lowers the series resistance of the diode as is discussed further in Section 5. However, before the landing on the delicate PureB layer the through-wafer aperture is micromachined. The 100 nm Al is explicitly left on the PureB surface to protect the PureB layer during bulk-micromachining. Additionally, layers of photoresist and polyimide are used when needed on the PureB to prevent any direct contact with chucks of the machines used during backside processing.

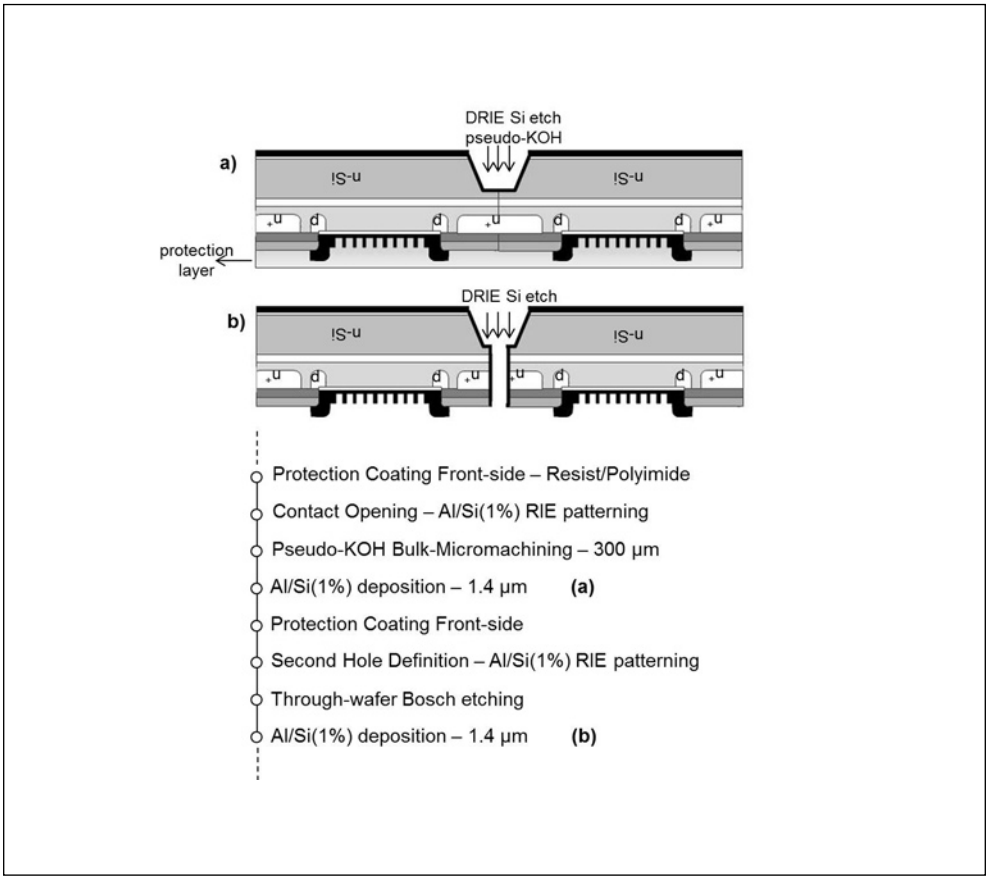


- *Epitaxy* – As-doped Si – 300 nm
- *Epitaxy* – 40 µm low-doped epi-layer
- Thermal oxidation – 230 nm
- Guard ring B^+, P^+ implantations
- Backside contact P^+ implantation **(a)**
- LPCVD oxide – 400 nm
- Annealing @ 1000 °C, 35 min
- Contact opening BHF, HF + Marangoni
- *Epitaxy* – PureB deposition 2 min 40 s **(b)**
- Pure Aluminium deposition – 1 µm
- Al/Si(1%) deposition – 675 nm, back-side **(c)**
- Metallization patterning by RIE **(d)**
- Contact grid patterning by RIE – 900 nm **(e)**
- *Bulk-micromachining of through-wafer aperture*
- Contact grid wet landing in HF(0.55%) – 3min **(f)**
- Alloying @ 400 °C, 30 min

FIGURE 4.1:
Schematic process flow for fabrication of the PureB electron detector.

FIGURE 4.2:

Bulk micromachining of the through-wafer aperture in two DRIE steps: a) with pseudo-KOH profile, and b) vertical sidewalls.



The bulk-micromachining is performed in two plasma-etch steps with resist masking: the first that etches around 300 μm that mimics the 55°-KOH profile, and the second that etches the remaining 250 μm with almost vertical sidewalls (Fig. 4.2). To prevent the micro-masking that can be caused by the Al presence in the etching system, additional lithographical steps are added to remove the Al from the resist-defined edges. Finally, the sidewalls of the through-wafer aperture are fully covered with an aluminum layer to prevent any charging and associated deflection of the electron beam as it passes through it in SEM system. When the through-wafer aperture has been processed, and the last 100 nm of Al etched away from the PureB in HF solution, the wafers are alloyed in forming gas for 30 min at 400°C.

4.3 PureB Photodiodes

4.3.1 Boron Layer Anode Formation

The main requirement for detection of electron beams with sub-keV energies is that the responsive region of the detector is within a nm-distance from the detector surface. This is because < 1 keV electron beams penetrate only a few nm into a solid material. The detection efficiency is therefore predominantly reduced by losses at the entrance window of the detector. For silicon photodiodes, this means that extra surface layers such are conductive metallization layers or scratch protection layers will have a negative impact on the efficiency [24].

The PureB layers are deposited from diborane (B_2H_6) at 700°C and the thickness is well controlled down to a nanometer by varying the deposition time. Here a 2 min and 40 s deposition is used, resulting in a 1.8 nm PureB layer. Under such conditions the doping of the underlying c-Si is limited to about 2 nm [25]. Going to thinner layers to achieve higher efficiency is a trade-off with the uniformity of the PureB layer surface coverage. The latter is vital for several reasons:

(i) a high concentration of holes at the Si wafer surface keeps the diode depletion region away from the defective interface and prevents the generated carriers from recombining at interface defects, (ii) it facilitates the patterning of the metallization layer directly on the PureB surface as will be described in detail in the following sections, (iii) the low atomic number of boron is instrumental in lowering the backscatter coefficient of the detector surface [62], and (iv) unlike the Si surface, the PureB layer does not oxidize to any significant degree in air and therefore does not charge when exposed to electrons with energies from 1 to 25 keV [25]. Further reduction of the deposition time to achieve a thinner PureB coating can result in an uneven coverage of the Si surface that would finally affect all of the aforementioned properties. The resulting p^+n junctions for the 1.8-nm-PureB are ideal with low dark currents and small over the wafer spread of values, substantiating that the nm-thin boron layer is reliably deposited over the wafer. An example of 2 photodiode segments of BSE electron detector is shown in Fig. 4.3. Finally, the extensive research carried out thus far on the PureB-layer photodiodes has established that they achieve a saturation current, ideality and yield comparable to their deep-junction counterparts [25, 26, 59–61].

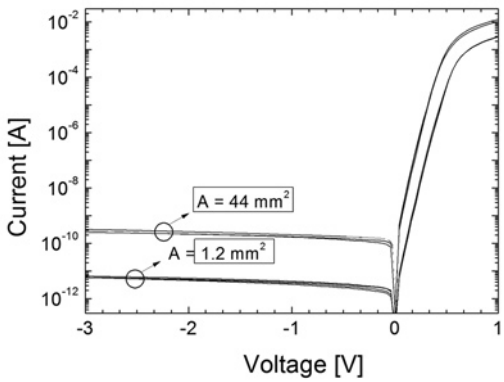


FIGURE 4.3:

Measured I-V characteristics of B-layer diodes on different positions on the wafer for photodiode areas of 44 mm² and 1.2 mm².

4.3.2 Electron Detection Efficiency

The electron detection efficiency is measured in a SEM system using the electron gun as the source of electrons. The measurement set-up is described in more detail in Section 2.6.1. The SEM electron beam delivers an input current I_{beam} on the photodiode surface and it will vary with the energy of the electron beam. In the present measurements the energy ranges from 200 eV to 10 keV and I_{beam} is determined for each point by directing the electron beam onto a Faraday cup. The output current I_{ph} is defined as the photodiode current at 3 V reverse bias and is measured on an external picoampmeter when the device is under exposure. The electron gain is given by

$$Detected\ Electrons\ /\ Incident\ Electrons = \frac{I_{ph} - I_{dark}}{I_{beam}} \tag{4.1}$$

where I_{dark} is the photodiode dark current, which can be neglected for electron energies above a keV in view of the fact that the value is typically a thousand times lower than the I_{ph}. Sub-keV electrons on the other hand generate a current comparable to the dark current of the diode, and the energy detection threshold will depend on the dark current level. The mean energy required to produce an electron-hole pair in silicon is 3.61 eV which determines the theoretical limit to e-h pair creation under a fixed electron exposure energy [18]. For example, with a beam energy of 200 eV the division into multiples of 3.61 eV gives a maximum of 55 generated e-h pairs. The theoretical electron gain calculated in this manner

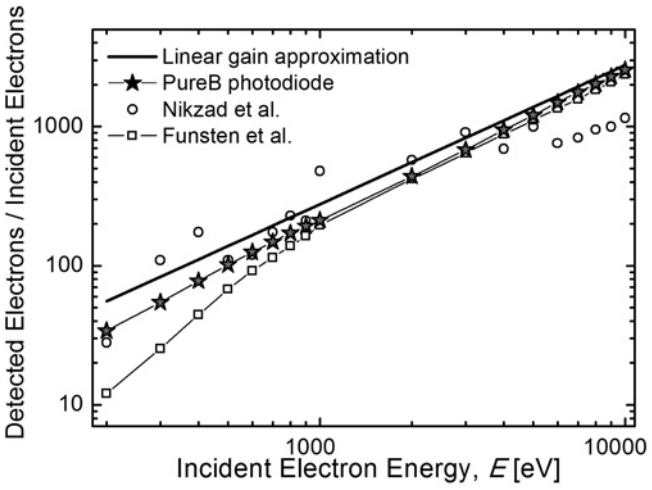
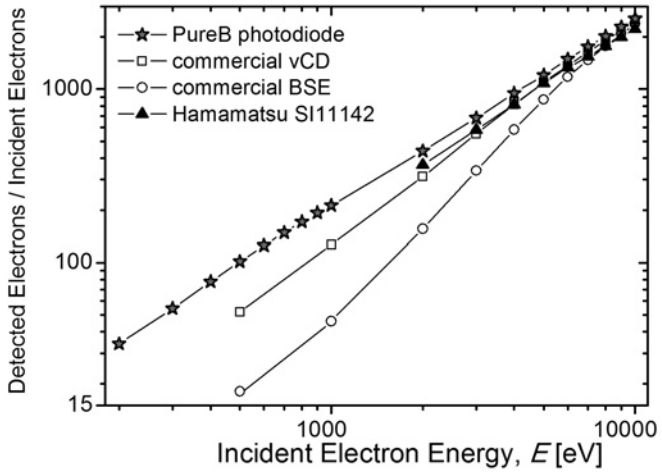


FIGURE 4.4:

Measured electron gain of a DIMES PureB photodiode compared to the data reported by Nikzad et al. [12], Funsten et al. [11], and theoretical electron gain.

FIGURE 4.5:

Measured electron signal gain for a DIMES PureB photodiode, a commercially available BSE detector, a low Voltage high Contrast Detector (vCD), and Hamamatsu SI11142 electron detector.



is included in Fig. 4.4. In the same figure, also the electron gain of a PureB photodiode with a 1.8-nm-thin boron-layer front entrance window is shown and it clearly follows the theoretical trend. The gain reaches 92% of the theoretical value at 10 keV, 87.5% at 5 keV, 73% at 1 keV, and an unprecedented 60% at the lowest energy of 200 eV. Compared to the other electron detectors reported in literature and also added to the graph, PureB diodes show record-high performance with a reliable energy dependence. Moreover, when compared to commercial implementations of Backscattered-Electron detectors (BSE) and low Voltage high Contrast Detectors (vCDs) as in Fig. 4.5, the PureB detector is clearly superior in terms of detection efficiency. Several points are also added for the latest Hamamatsu SI11142 BSE detector, but the supplied data is only for energies above 2 keV [63]. At 2 keV, the PureB detector performs at 80% of the theoretical efficiency, while this is a somewhat lower 65% for the SI11142.

4.4 Low Capacitance Detector Segments

4.4.1 Detector Segmentation Modes

There are two principal image-formation mechanisms employed in SEM systems: one supplies compositional information related to the atomic number Z, and the other topographical information, examples of both are shown in Fig. 4.6. For example, BSE with the small angles give material contrast, while the large angle BSE signal is dominated by the topographical contrast. To achieve an optimal signal contrast, the detector can be divided into an array of sub-detectors each connected to a separate terminal. The implementation used here with 8 sub-detectors is shown in Section 3.5. The signals acquired from each sub-detector can be processed either independently, all together as a single unit, or in grouped configurations such as the Concentric Back-Scatter (CBS) configuration (Fig. 3.15b) or the Angular Back-Scatter (ABS) configuration (Fig. 3.15c). In Fig. 4.7 the capability of the backscatter-electron detector operated in CBS mode is illustrated by the imaging of an uncoated pollen sample using beam deceleration with a landing energy on the sample of 50 eV.

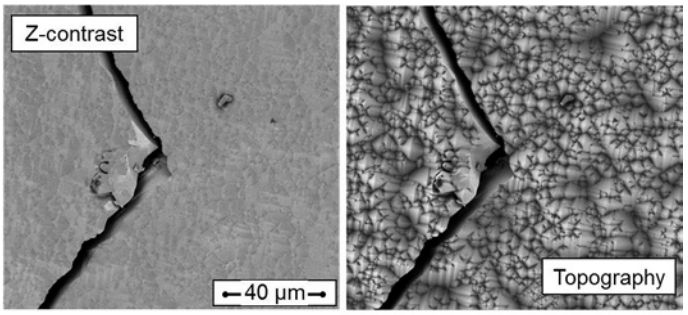


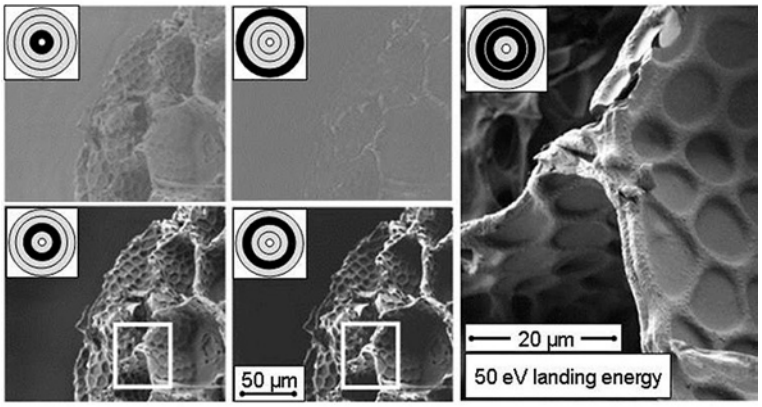
FIGURE 4.6:

Images of a solar cell sample taken at 2 kV with 2 different combinations of the diode segments of a BSE PureB detector. (*Image courtesy of FEI Company***)**

To operate sub-detectors separately, it is necessary to electrically isolate the individual photodiode segments. This effectively means that the photosensitive depletion regions of adjacent diodes should be separated at the operational voltage, which is set to 3 V reverse bias in the present work. To reach the desired low diode capacitance a lightly-doped substrate is needed to have a wide enough depletion region, but reach-through of the lateral depletion between the segments should be avoided. This effect determines how closely-packed the segments can be placed to each other to minimize the efficiency losses in the non-responsive separation regions that are specifically marked in the schematic of Fig. 4.8.

FIGURE 4.7:

Imaging of an uncoated pollen sample at 50 eV electron landing energy with beam deceleration applied, for each segment in CBS mode that is marked by dark ring, and the optimal combination of segments (right). (Image courtesy of FEI Company*)**



4.4.2 High-Resistivity Thick Si Epi-Layer Growth

A lightly-doped thick epitaxial n^{--}-layer is grown on n-type 2-5 Ωcm Si (100) substrates. The epi-layer thickness is tunable and can be matched with the separation distance of the adjacent diodes. The manner in which the n^{--}-epilayer is grown takes advantage of usually unintended arsenic segregation behavior as described in Chapter 3. In the first step, a 300-nm-thick As-doped layer with substantial As doping concentration is grown and forms

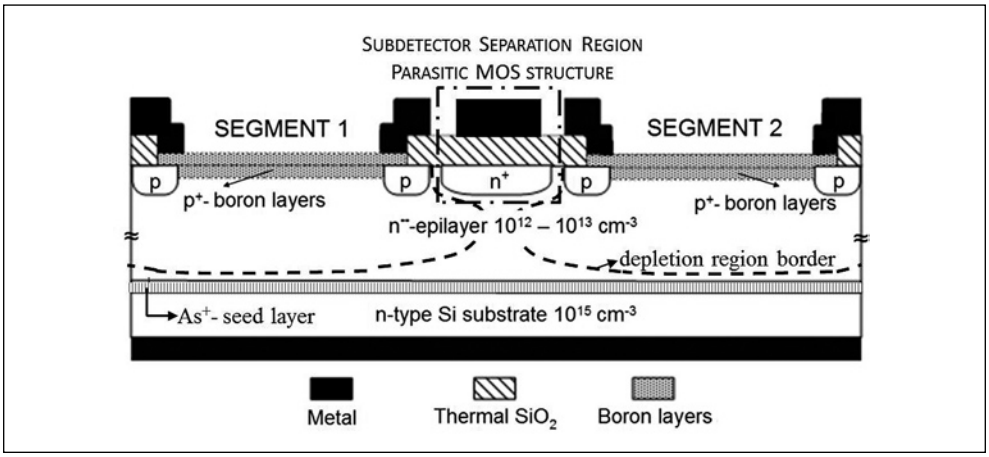


FIGURE 4.8:

Cross-section of adjacent diode segments of the PureB detector, indicating the separation region between them.

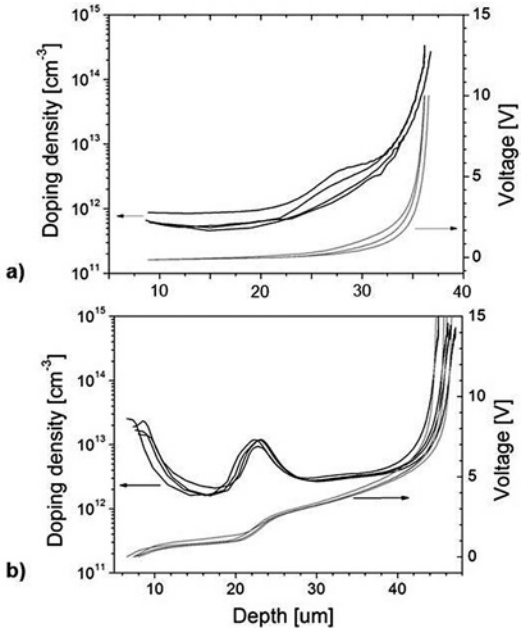


FIGURE 4.9:

C-V doping profiles of a 40-μm-thick n^{--} epitaxial layer showing the doping density and the corresponding voltages for: a) a layer grown in one step, and b) a layer grown with an interruption at 20 μm.

the source of As atoms for the subsequent growth of the n^{--} epi-layer. Three parameters control the final doping profile: the starting doping level of the As-doped seed layer, the total thickness of the as-grown layer, and the growth sequence of the intrinsic layer. For the BSE detector, the starting doping level is set to 10^{16} cm^{-3}, the total thickness is 40 μm, and different growth sequences were studied with the epi layers grown non-stop in one go (Fig. 4.9a), or in steps (Fig. 4.9b). The advantage of growing in steps is that each interruption in the growth cycle prevents the doping of the as-grown layer from dropping back to intrinsic values. As seen from the doping profile of the one-step epi-layer (Fig. 4.9a), the doping in the upper 20 μm drops below 10^{12} cm^{-3}. This gives a depletion region at 3 V reverse bias of about 70 μm wide. Although the spread would be limited vertically by the epi layer thickness, the lateral segment separation would be unnecessarily high. On the other hand, the bumpy doping profile of Fig. 4.9b, although grown above the same seed layer, retains a doping level above 10^{12} cm^{-3}. The 'bump' in the profile bears witness to the pause in the growth sequence and can originate from loadlock or chamber contamination of the epitaxial reactor, or from the substrate itself during a high-temperature bake at 1100°C between the growth steps. From Fig. 4.9 it is seen that the 3 V reverse bias places the depletion thickness at about 30 μm, which means that it should be safe to keep a 100 μm separation between segments. Various epi-layer thicknesses have been fabricated and, as shown in Fig. 3.5, the capacitance per unit area can be easily regulated with the layer thickness. The total diode capacitance is also determined by the capacitance of the metal tracks and pads, as well as the perimeter capacitance of the diode itself. Nevertheless, the dominant capacitance of these large diodes comes from the bulk depletion region. For thicknesses of 4 μm, 10 μm, and 20 μm the measured capacitance values at 3 V reverse bias are 15.4 pF/mm^2, 12 pF/mm^2, and 8.3 pF/mm^2, respectively, without having corrected for the the perimeter capacitance. For the 40 μm thick Si epi-layer, the targeted value of 3 pF/mm^2 is obtained.

4.4.3 N^+ Channel-Stop Opening

As illustrated in Fig. 4.8, an n^+ channel-stop layer is implanted between the detector segments. Besides the function to suppress the surface depletion of the epi-layer where MOS structures are formed by the metal tracks, this n^+-layer also limits the lateral depletion between the segments at the surface. This also reduces the area of depleted oxide interface, the defects of which are known to increase the dark current. On the other hand, limiting the lateral depletion component increases the perimeter capacitance of the photodiode which is then governed by the distance between the implanted n-region and the p-doped guard ring. For the mm^2-sized diode-areas used here, a distance of only 3 μm could be applied since the perimeter in this case contributes with less than 10% to the total capacitance value. More specifically, the perimeter capacitance for the present structure is simulated to contribute with 1.1×10^{-16} F/μm. An extensive simulation study of the trade-offs in terms of perimeter capacitance, breakdown voltage, and radiation hardness is published in [56].

4.5 Grid Processing for Low Series Resistance

4.5.1 Grid Geometry

A 1.8 nm-thin PureB layer has a sheet resistance of > 10 kΩ/sq which places a limitation on the series resistance of large area photodiodes. As described in Section 2.5, the sheet resistance can be lowered considerably by an in-situ thermal annealing of the as-deposited layer, or by depositing an extra B-doped epitaxial Si layer grown on top of the PureB layer. However, these measures will increase the distance to the photosensitive layer and for the present application this will reduce the efficiency as has been demonstrated in [24]. Alternatively, a metal grid can be formed on the PureB anode surface as an extension of the electrode geometry. An example of such a grid is shown in Fig. 4.10 where a rectangular mesh of µm-thin metal lines has been constructed so that the total photosensitive surface is covered by less than 2%. Since the distribution of the backscattered electrons that hit the detector surface can be considered stochastic, depending mainly on the specimen atomic

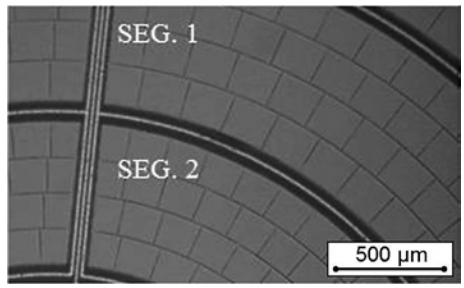


FIGURE 4.10:
Example of a topography of Al conductive grid on the photosensitive surface of the detector.

number and topography, we can assume that the loss in efficiency is also averaged out to be less than 2%. The resistance is lower as the grid is made denser according to the formula

$$R_{eq} = \frac{R}{N}, \tag{4.2}$$

where R_{eq} is the total series resistance of the photodiode detector unit, R is the resistance of a single rectangle unit marked by the grid lines, and N is the number of rectangles. If the large detector area is divided into N equal squares using the grid, each square can be represented with one resistor with the resistance R. Since all the squares of the same diode share the same cathode and anode electrodes on the bottom and the top of the device, they can be represented as N paralel resistors, each with the resistance R. Therefore, the total resistance of the device is the equivalent resistance of the N paralel resistors - R over N. For the large surfaces used here an attractive trade-off with efficiency is readily made. For example, a 50 mm^2 diode surface can be divided into more than 800 squares with 250×250 μm^2 geometry. If 2 μm-wide grid lines are patterned the grid still covers only 1.6% of the responsive surface.

4.5.2 Grid Fabrication

The grid processing is performed in the way described in Section 2.5 for contacting the anode at the diode perimeter. This method makes use of the high resistance of the PureB layer to HF etching, as well as the fact that Al does not react with PureB at the given processing temperatures while still forming a good ohmic contact to this material. The basic grid formation process is shown in Fig. 4.1d - Fig. 4.1f and described in Section 4.2.

For realizing the smallest possible micron-sized grid-line widths several points should be taken into consideration. Firstly, the initial plasma-etching of the Al to define the grid pattern should be performed as close to the PureB layer as possible (Fig. 4.1e). If only a wet-etching process is used, then with an Al film thickness of 1 μm the minimum linewidth that can be achieved reliably is 3 ± 0.25 μm [64]. This can be considerably reduced by pre-patterning the grid in a plasma-etch step. For a reliable process it was necessary to leave 100 nm of Al on the PureB because otherwise uneven etching along the Al grain boundaries can also lead

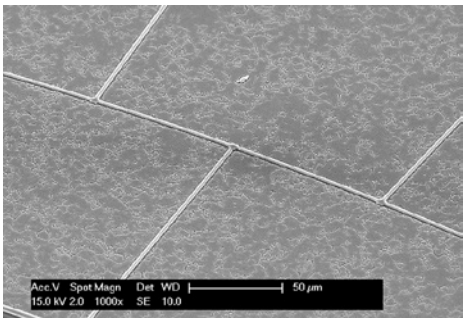


FIGURE 4.11:

Example of an uneven plasma-etching of the metallization layer during grid formation.

to etching of the PureB layer, as shown in Fig. 4.11. This can result in an undesirably high dark current. With the 100 nm of Al, an on-mask grid-line width of 2.5 μm could be defined, resulting in a final width of about 1.5 -2.0 μm after full processing. Diodes with and without a grid were processed on the same wafer and the I-V characteristics are compared in Fig. 4.12. With the grid, there is a clear drop in series resistance. The average extracted series resistance for a diode with an area of 50 mm^2 is 280 Ω without grid and 20 Ω with a mesh grid subdivided into around 800 squares.

The reliable etching-back of the pure Al to about 100 nm is not always possible. In the present case, the Al is deposited by physical vapor deposition (PVD) at 350°C to a layer thickness

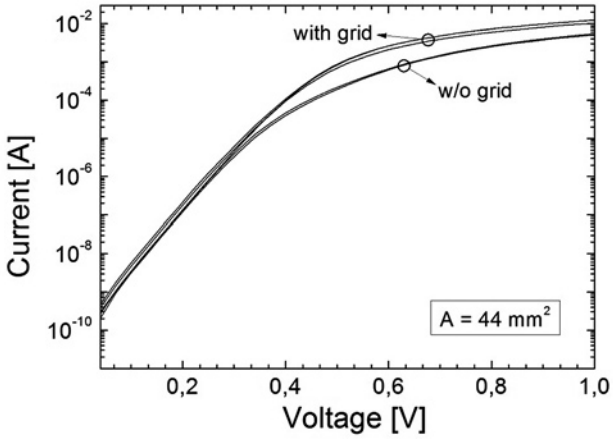


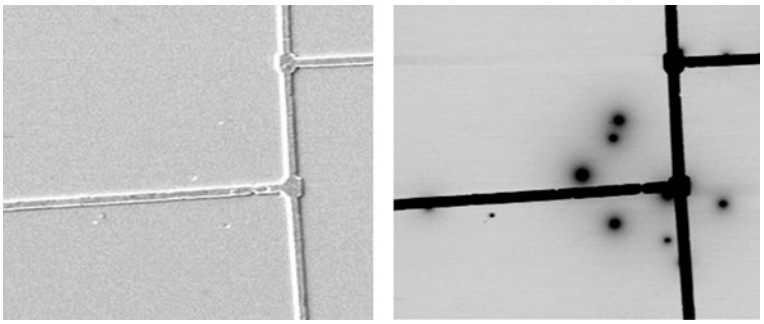
FIGURE 4.12:

Measured forward I-V characteristics of PureB diodes for photodiode areas of 44 mm^2, with and without a conductive grid on the photosensitive surface.

greater than 1 μm. This thickness and the elevated deposition temperature proved to be required to produce a uniform surface of tightly-packed large grains that do not change morphology during further temperature processing. For thinner layers or depositions at lower temperature, grain growth during subsequent processing steps can induce the formation of gaps between grains that lead to premature exposure of the PureB layer during etching. Although there is a high selectivity of Al to PureB during the HF dip-etch, excessive etching of the very thin PureB layer is not possible. In this respect, a uniform back-etching of the Al is also warranted. If there are small imperfections in the PureB layer that allow the Al to have direct contact with the Si, which would induce a “spiking” phenomenon at elevated temperatures, over-etching will also aggravate the situation.

FIGURE 4.13:

SEM image zoomed in on irregularities on a photosensitive surface. Corresponding EBIC image shows non-responsive dead areas. (**Image courtesy of FEI Company***)**



An example of an imperfect anode surface is seen in Fig. 4.13, where nonresponsive dead spots are located by inspection with Electron Beam Induced Current (EBIC) analysis. A comparison to the corresponding SEM image confirms that small surface imperfections are responsible for the dead areas. It is plausible that spiking pits are the cause of the relatively large dead areas. When Al is removed in an (over-)etch step any exposed Si surface in the pits will oxidize and be a source of recombination centers for electron-generated charge carriers produced in a wider area around the pit. In the spiking process that can occur when pure Al and Si are in contact and exposed to elevated temperatures, the Si that diffuses into the Al layer will subsequently be transported along the PureB surface in an Al-mediated process to be deposited elsewhere. Such unwanted material on the PureB surface will give more well-defined dark areas that are also seen in Fig. 4.13.

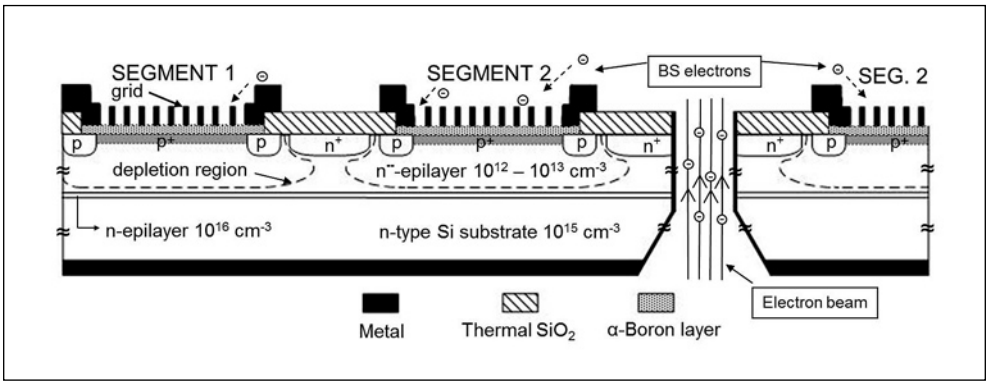


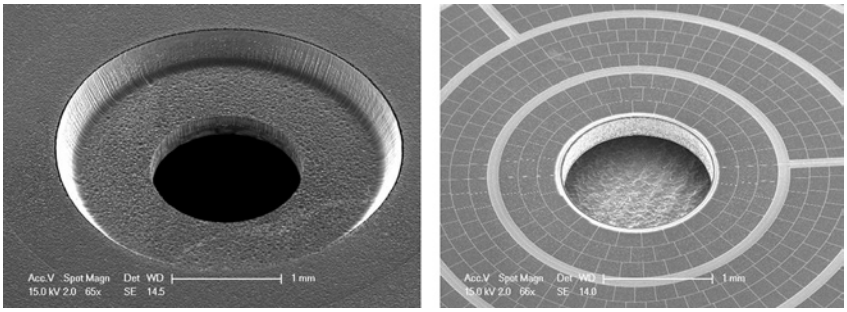
FIGURE 4.14:

Schematic cross-section of two neighboring segments of a PureB detector with a through-wafer hole as aperture for the electron beam. The depletion of the typically 40 μm deep n^{--} epitaxial layer is indicated.

4.6 Bulk Micromachining of Through-Wafer Apertures

In order to capture the very low-angle backscattered electrons the detector needs to be placed as closely around the incident beam as possible as shown in Fig. 1.6. Therefore, the through-wafer aperture must be etched close to the photosensitive diode area to maximize the angle detection range of the BSE detector. At the same time a safe distance must be kept from the diode depletion region so that it does not enter the etched-via region, the damage of which represents a significant source of dark current. Figs. 4.14 and 4.15 illustrate the position of the aperture with respect to the diode segment and the depletion region. If we assume a depletion region radius of 40 μm as described in Section 4, the resulting

FIGURE 4.15:
SEM image of a through-wafer aperture aligned to the inner-most segment of PureB detector.



hole needs to be at least 50 μm away from the diode edge, depending on the lithography accuracy and the profile control during micromachining. During the aperture processing, it is vital that the photosensitive surface of the detector is protected from both chemical and mechanical damage during micromachining of the through-wafer holes. Therefore, the 100-nm-thick layer of Al with a pre-imprinted grid pattern is kept throughout this processing as a protective layer, particularly against high power oxygen plasma removal of resist and high temperature oxidizing cleaning steps, both of which damage the PureB layer. By keeping this Al protection-layer it becomes possible to use an extra polyimide layer to protect the front of the wafer against mechanical damage while processing the back of the wafer. The fabrication process is completed with a blanket HF dip-etch to remove the 100-nm of Al and expose the PureB surface followed by alloying in forming gas.

4.7 Conclusions

It has been demonstrated that the PureB-layer silicon photodiode detector technology outperforms other technologies, both those on the market and those reported in literature, for the detection of low-energy electrons down to 200 eV where a 60% efficiency was obtained. For the application to backscattered electron detectors for SEM systems, the technology is proven to be highly flexible by the integration with several other special processing techniques, to increase the performance and functionality of the detectors. This includes special grid processing directly on the PureB surface to lower the series resistance, closely-packed segmentation of the detector into low-capacitance photodiodes, and through-wafer apertures. The 8-segment detector developed here produces excellent BSE imaging results, demonstrated using beam deceleration technique for landing energies on the sample as low as 50 eV.

5

PureB Electron Detectors Integrated on Locally-Thinned High-Resistivity Silicon

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5

PureB ELECTRON DETECTORS INTEGRATED ON LOCALLY-THINNED HIGH RESISTIVITY SILICON

5.1 Introduction

A special class of photodiode detectors is formed by large-area devices, often used in imaging for medical and astrophysics applications, where the operating speed is typically limited by the detector capacitance [65, 66]. Since the capacitance scales proportionally with the area, wide depletion regions are implemented to nevertheless achieve low capacitance values. So far, this has been achieved with Si PIN photodiodes by fabricating lightly doped epitaxial layers on heavily doped substrates, as described in the previous chapters. It is further common to design large-area photodiodes in segmented, closely-packed arrays to, for example, match the size of the scintillator crystals in positron-emission tomography (PET) [67], or in the present case to achieve optimal imaging contrast in Scanning Electron Microscopy [59, 60]. The detector segmentation will give lower capacitance values of the individual segments, but at the same time a high packing density is needed to achieve high area fill-factors to nevertheless preserve the detection efficiency. Therefore the distance between different segments must be small while still separating the wide depletion region surrounding them.

The PureB electron detectors require up to cm^2-large photosensitive areas consisting of densely arranged photodiodes that can be operated separately, in configurations to combine the individual signals, or as a single sensor unit. In the previously described electron detector process, p-i-n diodes were fabricated on a 40-μm-thick lightly-doped n-epitaxial Si grown on low-resistivity Si (LRS) to achieve both low capacitance and series resistance (Chapter 3). In this chapter an alternative approach is presented whereby the p-i-n technology is transferred to HRS substrates in order to achieve wider depletion layers. To keep the series resistance low, local thinning of the HRS is implemented. This is a well-known technique used in the fabrication of Charge Coupled Devices (CCDs), where the main goal is to make backside illumination of the CCD units possible without having to apply hundreds-of-volts biasing [68]. In the present detectors, (electron) irradiation takes place at the front-side anode covered with a nm-thin boron layer that serves as an entrance window. The operating voltage is increased from previously used 3 V on LRS to 20 V, to achieve the optimal RC constant. It can, if necessary, maintain the 3 V value if the substrate resistivity is preselected high, and with small spread of values. The density of the photodiode array is determined by the lateral depletion region, since the SEM application demands electrical isolation of the neighboring segments. Here the integration of the PureB SEM electron detectors on high-resistivity Si is implemented, and the devices are characterized in terms of RC constant, fabrication complexity, dark current (detection noise floor), and breakdown voltage.

5.2 Basic Process Flow

Schematic cross-sections of the electron detector fabrication steps are shown in Fig. 5.1. The process starts with n-type (100), 300-μm-thick, 1-10 kΩcm substrates, on which thermal oxide is grown and the photodiode guard rings and cathode contacts are implanted (Fig. 5.1a). After that, LPCVD oxide is deposited and the total isolation stack is patterned with the anode openings. On the back of the wafer, directly underneath the anode regions, the oxide is also removed and the Si substrate is thinned (Fig. 5.1c). In this paper, the Si etching is performed using Deep Reactive Ion Etching (DRIE) with a pseudo-KOH profile (≈ 55°), as an alternative to tetramethyl ammonium hydroxide (TMAH), standardly used in the fabrication of back-illuminated p-i-n photodiodes [65]. Here the backside is used merely as the photodiode cathode contact and the sensor does not operate in full depletion, therefore the demands on the etching quality and uniformity are more relaxed. The dry etching gives much more flexibility with respect to the cavity shape than TMAH etching, and here it is used to create the mirrored image of the sensor anode design. The resulting high-resistivity Si membrane is ≈ 100μm-thick, and it can optionally be implanted with phosphorus to form an ohmic contact (Fig. 5.1c). The implantations are annealed at 1000°C for 35 min. The process is finalized by a 700°C-deposition of a nm-thin PureB layer in the anode openings, and patterning of a pure Al metallization layer (Fig. 5.1d). The PureB layer deposits selectively on oxide-free Si surfaces which is provided by HF-dip and Marangoni-drying prior to the deposition. The layer thickness is time-controlled in an ASM Epsilon Si/SiGe epitaxial reactor,

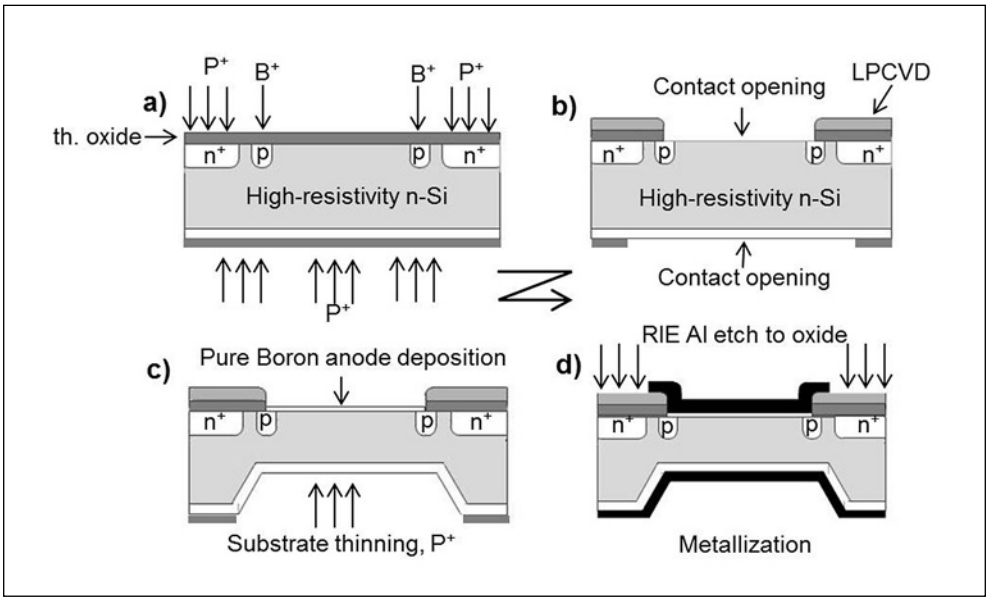


FIGURE 5.1:

Schematic process flow for fabrication of bulk-micromachined high-resistivity-Si PureB electron detectors.

and it can be controllably deposited down to a thickness of < 2 nm. Finally, for the detection of low-energy backscattered electrons, the PureB photosensitive surface needs to be fully exposed, i.e. the metal needs to be completely removed, leaving only the perimeter metallization for contacting. This is made possible by depositing pure Al that can be removed in HF 0.55% with high selectivity to even a nm-thin boron layer. More details of the Si surface preparation before PureB deposition, the PureB deposition parameters, and metallization using pure Al are given in Chapter 2.

In an alternative process flow, the PureB anode deposition and the metallization can precede the substrate thinning. This flexibility in the processing is possible because the Si is not fully-depleted to the cathode contact and it is therefore not necessary to create a defect-free n^+-contact in the cavities. Therefore, the high temperature processing otherwise needed to activate the n^+-implant can be avoided. Ohmic contact can, for example, be achieved by surface roughening after all the high-temperature steps. This considerably simplifies the processing and makes it very comparable in complexity/robustness to the low-resistivity Si version of the process.

5.3 HRS PureB Electron Detector

A schematic cross-section of two concentric detector segments and a top-view image of a possible segmented SEM detector are shown in Figs. 5.2 and 5.3, respectively. The scanning speed of the detector is determined by the RC constant. In general, a low RC is achieved on HRS substrates by fully-depleting the wafer. Here this is not a viable solution because of restrictions on the lateral depletion width. The electron detectors shown here are divided into several electrically-isolated photodiodes that are visible in Fig. 5.3, and shown earlier in Fig. 3.15. The electron beam is also passed through a hole in the center of the detector, to then impinge on and be back-scattered from the sample under investigation. The photodiode segments must be placed as closely as possible to the hole perimeter and to each other

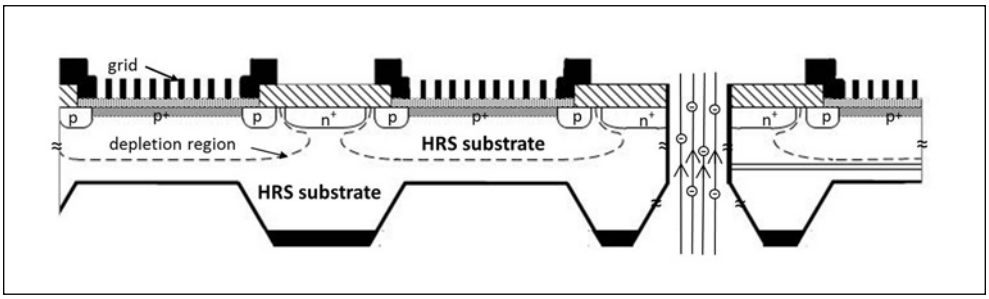


FIGURE 5.2:

Schematic cross-section of neighboring segments of a PureB detector fabricated on a locally-thinned HRS substrate with a through-wafer hole as aperture for the electron beam.

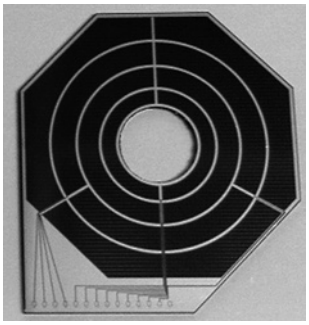


FIGURE 5.3:

The photograph of a 12-segment PureB BSE detector of total dimensions 18×18 mm^2. The inner segments are wrapped around the central through-wafer hole at a distance of 100 μm.

in order to obtain optimal imaging contrasts. Additionally, the non-responsive separation areas need to be covered with conductive material to avoid charging effects during electron irradiation. The irradiation of oxide, for example, would otherwise increase the dark current level of the photodiode, thus influence the detection efficiency. The distance between segments here is set to 100 μm, and is limited by the lateral depletion of the n-substrate, which is coupled to the width of the vertical depletion. This gives a trade-off between low capacitance and responsivity loss.

5.4 Optimization of Detector Capacitance and Series Resistance

In Fig. 5.4 it is seen that the obtained capacitance is reduced from 24 pF for LRS, to 15 pF for the HRS detector at 20 V reverse bias with a 6.6 mm^2 diode area. The values are measured for LRS and HRS electron detectors that correspond to the cross sections shown in Fig. 4.14 and Fig. 5.2. The LRS version has a very lightly n-doped 40-µm-thick epitaxial layer grown on low resistivity substrates by the technique described in Chapter 3. The doping of the as-grown epi-layers is controlled down to 5×10^{11} cm^{-3}. However, the obtainable quasi-intrinsic epilayer thickness is technologically limited and it is difficult to grow good quality layers thicker than 40 μm. Moreover, these epi-layers are grown on arsenic-doped seed layers, doped in the range 10^{16}-10^{17} cm^{-3}, so the first 10 μm contain a significant arsenic concentration from auto-doping. There is therefore no profit in terms of lower capacitance when the operating voltage is increased.

The measured value of 24 pF at 20 V is essentially the sum of the junction capacitance and the oxide capacitance. The former is dominated by the substrate doping, while the main contribution to the latter is from the metallization layer at the diode perimeter where the metal overlaps the oxide isolation, but the metal tracks and pads also contribute. For the present layout and 0.5 μm isolation oxide thickness, the contribution of the parasitic metal-oxide capacitance is 7 pF. The remaining junction capacitance of 17 pF is, without separating the perimeter capacitance, equivalent to a fully depleted ≈ 40-μm-thick epi-layer.

The HRS electron detectors operate with a 15 pF capacitance under the same biasing conditions. Since the oxide capacitance is equal to the epi + LRS case-7 pF, the remaining junction capacitance of 8 pF correlates well with the expected substrate doping of 4×10^{12} cm^{-3} (1.1 kΩcm resistivity), thus a ≈ 80-μm-wide depletion region is assumed. Therefore, the junction capacitance corresponds to a capacitance of only 1.2 pF/mm^2 for the selected 6.6 mm^2 area, and the high-resistivity membrane is left with 20 μm of the undepleted silicon substrate. The resistance of the undepleted layer, together with the PureB layer resistance and the contact resistance, results in a value of 100 Ω at 20 V, as shown in Fig. 5.5.

For comparison, an electron detector on HRS without substrate thinning is also characterized. The resulting 1700 Ω series resistance indicates that the resistivity of the wafer processed without bulk-micromachining step is very high, however still possible within the

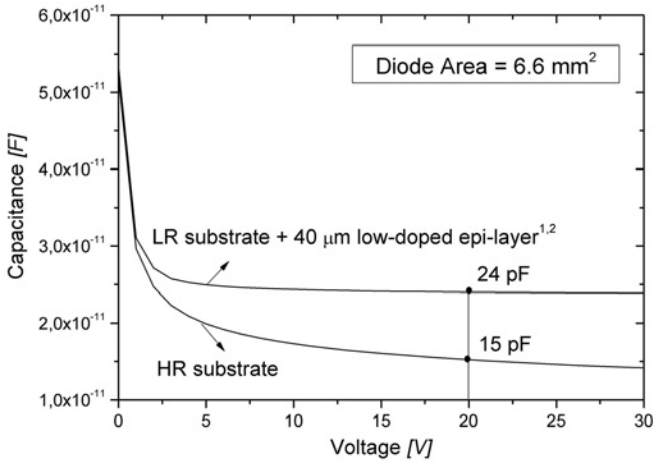


FIGURE 5.4:

Capacitance measurements for photodiodes with 6.6 mm² anode area fabricated using the LRS and HRS substrates.

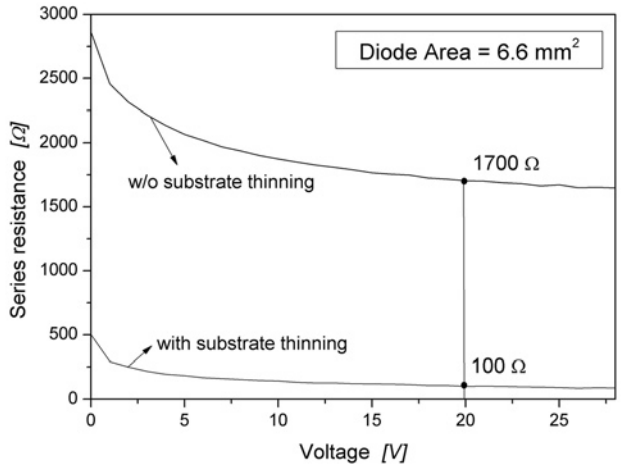


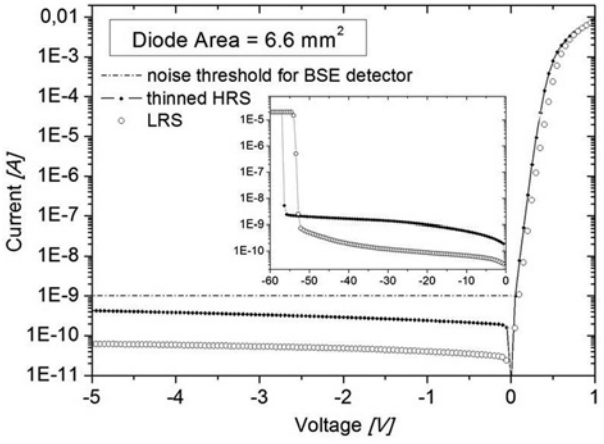
FIGURE 5.5:

Series resistance of the 6.6 mm²-area diode for HRS substrates, with and without bulk-micromachining of the substrate.

wafer resistivity specifications of up to 10 kΩcm. The high resistivity of the wafer is also confirmed by the capacitance measurements. The capacitance of 6.6-mm^2-area diode yields a total value of only 10.5 pF, or 3.5 pF junction capacitance corresponding to 0.5 pF/mm^2 . To maintain such a low capacitance value, the substrate thinning would have to be performed to deliver ≈ 200 μm-thick HRS membranes, since the depletion region is more then twice as wide as on the wafer with 1.1 kΩcm resistivity. This would also impact the spacing between adjacent photodiodes that would have to be redesigned accordingly. To avoid having to adjust the micromachining range and the sensor design for each wafer, it would be necessary to have the starting substrates with tighter specifications on the resistivity so that the critical depletion width could be predefined.

FIGURE 5.6:

I-V characteristics of HRS and LRS samples. The inset shows a stable dark current value up to 20 V reverse bias.



The dark current of HRS photodiodes is measured up to a breakdown voltage of > 50 V. It displays stable values in the measured bias range, though somewhat higher dark currents than for the LRS samples due to the increased depletion volume. In Fig. 5.6 the I-V characteristics are shown for both LRS and HRS electron detectors, and a line is added indicating the tolerable noise level for electron detectors used in SEM systems.

5.5 Conclusions

In this paper a production-ripe process for fabricating electron detectors for SEM systems is transferred to high-resistivity Si substrates. In this way, the photodiode detectors can reach lower capacitance values, and the resistance of the diode is adjusted by bulk-micromachining of the undepleted portion of the substrate. Here a 6.6-mm^2-area photodiode detector is characterized, and compared to the previously reported results obtained for low-resistivity Si substrates. The total capacitance is lowered from 24 pF to 15 pF at 20 V reverse bias, and junction capacitance values of < 1pF/mm^2 have been demonstrated. The resistance of the diode is successfully lowered by the substrate thinning, and measured value is 100 Ω at 20 V reverse bias. Further, for ≈ 1 kΩcm resistivity substrates, the distance between the neighboring diodes that form the electron detector is set to 100 μm, as was the case for LRS. The dark current level is slightly increased, but nevertheless remains within sub-nA levels that are typically indicated for SEM electron detectors.

EPITAXIAL GROWTH OF P^+N DIODES AT 400°C BY ALUMINUM-INDUCED CRYSTALLIZATION

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EPITAXIAL GROWTH OF P⁺N DIODES AT 400°C BY ALUMINUM-INDUCED CRYSTALLIZATION

6.1 Introduction

When Aluminum-Induced Crystallization process is used on c-Si wafers or seeded substrates, it results in a low-temperature epitaxy of Al-doped layers of Si, also known as Al-mediated Solid Phase Epitaxy (SPE) [69]. The applications of the as-grown p^+-doped layers include ultra-abrupt p^+-silicon elevated contacts and diodes [70], PNP bipolar transistor emitters [70], nanodevice integration [71], lateral SPE silicon-on-insulator growth [72], physical cryptography [73], solar cells [74], and counter-doping of Si thin-films [75]. When compared to the PureB technology which is also used for creating an ultrashallow p^+-anode and has established itself as the leading material for shallow-penetration radiation detection, the Al-mediated SPE holds less control over the layer thickness on one hand, while implicating lower fabrication temperature on the other. Since the Al-mediated SPE process can be performed at 400°C and below, it is attractive as a low-cost add-on to fully-processed CMOS wafers. However, as the layer thickness can vary significantly across the large areas, this technology is limited to the less-demanding applications of the ultrashallow junctions.

The initial motivation for the present work has been the fabrication of JFET transistor with ultrashallow top-gate in a 'gate-last' process. The JFET transistors were intended as high-frequency charge preamplifiers, integrated on-chip with the PureB electron/X-ray detectors [76–78], where the possibility to fabricate the JFET top-gate as a post-metallization step offers much-needed design flexibility. The previously realized ultrashallow-gate JFET devices, that used PureB technology for the top-gate p^+-plug, have already been demonstrated to achieve a good DC performance with notably high transconductance values [79]. The 1/f noise, however, remains the issue. The earlier attempts to create an ultrashallow-gate nJFET using Al-mediated SPE were limited due to the fact that the Al-mediated crystallization of Si was only reached for small contact window areas of a few microns large [69–71].

In the present chapter it is shown that the density and vicinity of nucleation sites on the substrate is decisive for the maximal area size that can be filled with Al-mediated SPE. In particular, the influence of the c-Si interface quality is studied with the aim of creating arbitrarily large defect-free Al-doped p^+n diodes at maximum temperature of 400°C. The characterization is carried out using scanning electron microscopy (SEM), high resolution transmission electron microscopy (HRTEM), nanobeam-diffraction (NBD), and atomic force microscopy (AFM) analysis. Finally, for the optimized surface treatment conditions, good quality diodes of adjustable anode shapes and sizes, up to 1×1 cm^2 in area, are fabricated and characterized.

6.2 Mechanisms Behind the Al-mediated SPE of High-Quality Silicon Diodes

The work described in this chapter was originally started by Civale et al. in 2006, and it is indispensable to review the previously reported theory underlying the process before moving on to the more recent results [69, 70]. The first fabricated SPE p^+ elevated contacts clearly established the possibility of growing highly-controllable and reproducible, low-defect density, uniform, Al-doped, c-Si layers at < 400°C temperatures. The initially reported devices were fabricated in the window sizes of 0.5×0.5 μm^2 and 1×1 μm^2, and corresponding IV-characteristics were found near-ideal in terms of dark current, ideality factor, and the contact resistance of the as-grown contacts (Figs. 6.1 and 6.2).

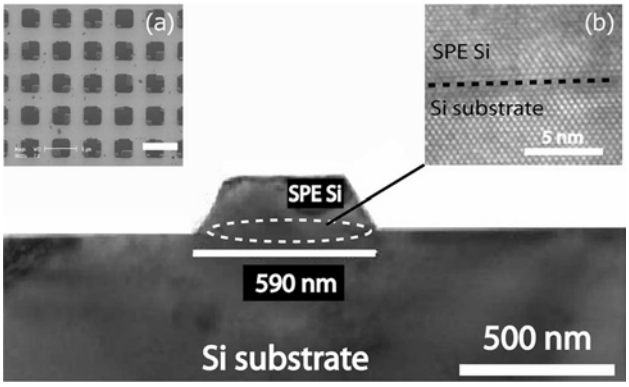


FIGURE 6.1:

Cross-sectional TEM image of SPE p^+ Si island showing the Si crystal facets. The inset (a) is an SEM micrograph (after wet Al removal) of the initial stages of SPE. In these larger windows, the initiation of crystallization in the corners is evident. The scale bar is 5 μm. The inset (b) is a high-resolution TEM (HRTEM) of the interface with the Si substrate demonstrating the epitaxial growth [70].

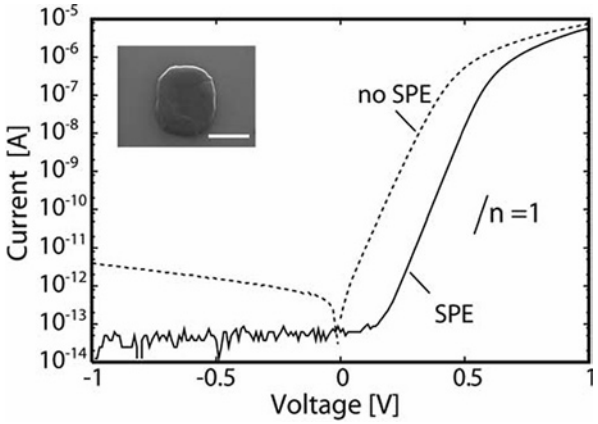


FIGURE 6.2:

IV characteristics of 1×1 μm^2 junctions fabricated on 2-5 Ωcm n-type substrate. The solid line is for a SPE p^+n diode and the dashed line for an Al/Si (1%) Schottky diode. The inset shows a SEM micrograph of SPE filled 1.2×1.2 μm^2 contact window (the scale bar is 1 μm) [70].

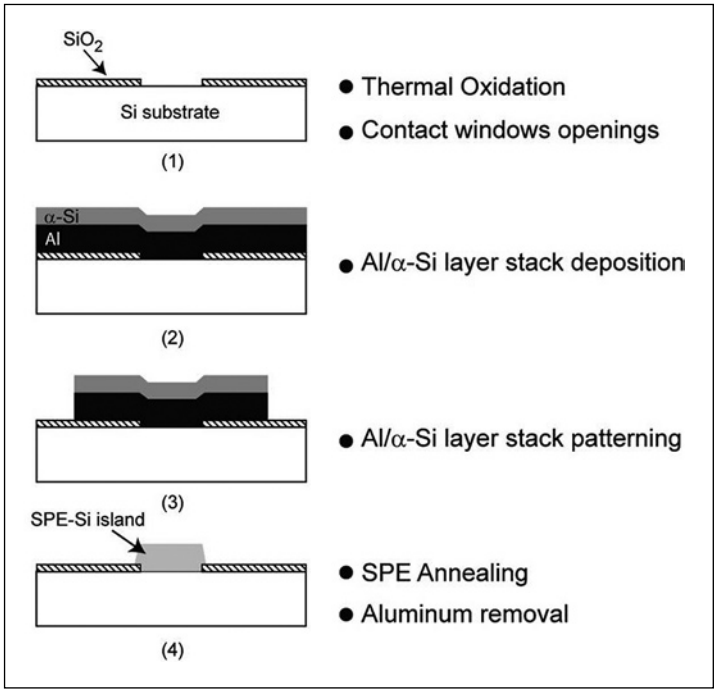


FIGURE 6.3:

Basic process flow of Al-mediated Solid Phase Epitaxy [69].

Later on, the mechanisms governing the Al-mediated SPE were elucidated through a series of tests on uniform wafers or in contact windows to the Si through a SiO_2 layer [69]. Here the patterning of the SiO_2 is followed by deposition of Al and α-Si layer of the desired thickness, stack patterning around the oxide-openings, and an annealing step at 400°C. The process flow is schematically shown in Fig. 6.3. In order to study the SPE process, the mediator Al layer is selectively removed after the anneal, i.e. the layer-exchange step. Using Scanning Electron Microscopy, the successive stages of the SPE-Si sequence are recorded as shown in Fig. 6.4, and the process sequence is described as follows: 1) formation of "free" Si at the Al/α-Si interface, 2) diffusion of Si along the Al grain boundaries, 3) nucleation at the Si substrate surface, 4) nuclei rearrangement and 5) crystal growth. The stages are monitored on patterned substrates, and it has been noted that the crystals grow predominantly at the contact window perimeter before they merge and close up towards the center of the opening (Fig. 6.4d). Further, when patterning the contact windows in SiO_2, the quality of the dielectric surface has proved decisive for the SPE-Si growth selectivity. If the dielectric has a high surface defect density, as for instance when SiO_2 is deposited using a PECVD process at 400°C, very little SPE-Si is deposited in the contact windows and the available α-Si is consumed by the formation of poly-Si on the SiO_2. If, on the other hand, the dielectric is thermally grown SiO_2 at 850°C, the surface is characterized by very low defect-density and the Si atoms can undisturbedly diffuse along SiO_2 surface before finding and depositing exclusively in the contact openings. These are very important experimental observations that reveal the nature of a diffusion mechanisms of Si atoms along the substrate surfaces and as such are very valuable for the following experiments.

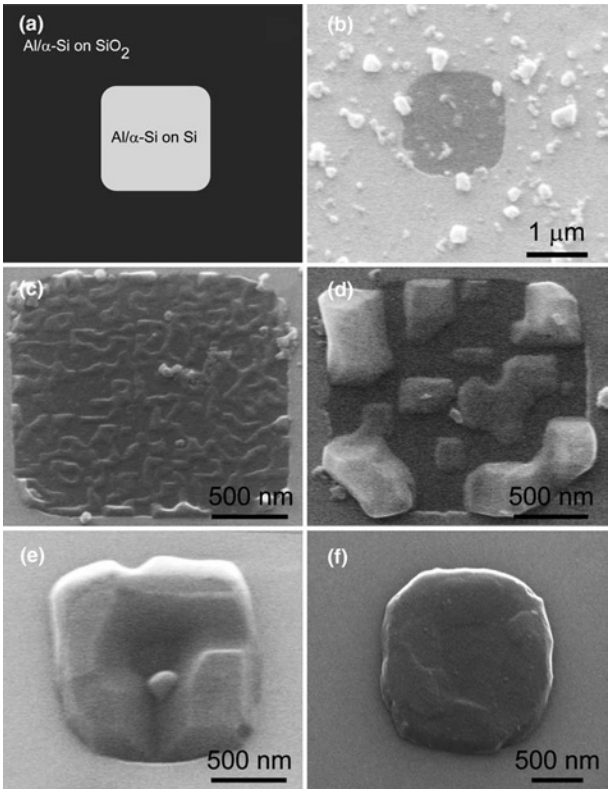


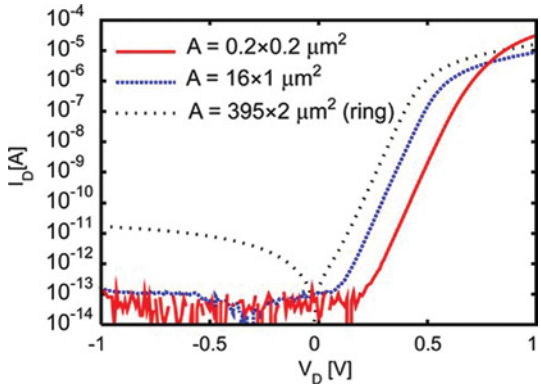
FIGURE 6.4:

(a) Schematic top-view of the SPE-Si test structure after Al/α-Si layer stack deposition and patterning. SEM micrographs of the contact windows for different growth times: (b) 1.5 min at 500°C, (c) 2 min at 400°C, (d) 6 min at 500°C, (e) 30 min at 500°C, and (f) 30 min at 500°C with optimal Al/α-Si layer stack geometry and thickness ratio. [69]

The main focus in this chapter is the growth of Al-mediated SPE in arbitrarily shaped large-area contact windows. The largest diode measured during earlier studies was a ring-shaped 395×2 μm^2-large diode that has already exhibited the signs of deterioration in the dark current behavior (Fig. 6.5) [69]. In order to promote the growth of high-quality c-Si in larger contact windows, the diffusion length of Si atoms along the substrate wafer surface is optimized by careful window etching and surface preparation.

FIGURE 6.5:

I-V characteristics of SPE-Si based p$^+$n diodes with three different geometries and junction areas [69].



6.3 Basic Process Flow

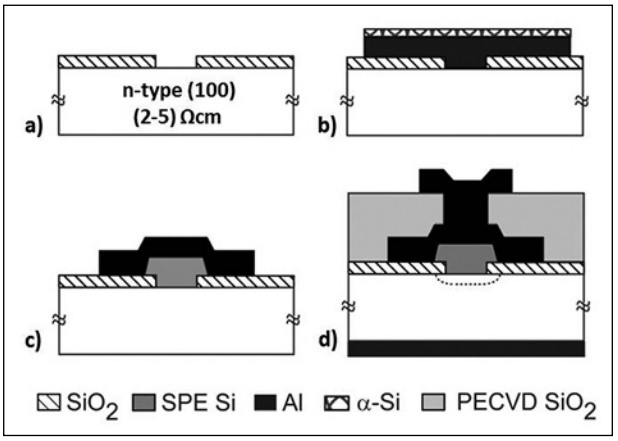


FIGURE 6.6:
Schematic process flow for fabricating Al-mediated SPE p⁺n diodes.

The fabrication process is schematically shown in Fig. 6.6. The starting substrates are n-type 2-5 Ωcm (100) wafers. First, thermal SiO_2 is grown and windows to the Si are patterned by either plasma etching or wet etching in buffered HF 1/7 (BHF 1/7) (Fig. 6.6a). Some of the wafers are then dip-etched for 4 min in a 0.55% HF solution and dried using the Marangoni effect of isopropanol alcohol (IPA) to ensure a native-oxide-free hydrogen-terminated surface. Then, a layer stack of Al and α-Si is sequentially deposited by physical vapor deposition (PVD) at room temperature without vacuum break between the depositions (Fig. 6.6b), in order to prevent oxidation of the Al surface which may otherwise slow down the migration of Si and deteriorate the final crystallized Si quality [80]. The thickness of the deposited Al is either 100 nm or 200 nm, and that of the *α*-Si either 20 nm or 50 nm. The Si target is sputtered at 0.5 kW in Ar-atmosphere. After deposition, the stack is patterned around the oxide openings, and annealed for 40 min at 400°C in forming gas. During the annealing, the layer exchange takes place and the resulting Al-doped c-Si layer is deposited preferentially in the oxide openings (Fig. 6.6c). To form the anode contacts, PECVD oxide is deposited and windows to the SPE islands are patterned. A second layer of metal (PVD Al/1%Si) is then deposited for interconnect patterning. Finally, the back of the wafer is metalized and the wafers are alloyed for 40 min at 400°C in forming gas (Fig. 6.6d). An overview of the different process variations are given in Table 6.1.

Sample name	Oxide pattering	Post-etching treatment	Stack thickness [Al, Si] in nm
WetHF	wet BHF 1/7	HF 0.55% Marangoni-IPA	[200, 20] [100, 50]
WetBHF	wet BHF 1/7	x	[200, 20]
DryHF	dry	HF 0.55% Marangoni-IPA	[200, 20]

TABLE 6.1:
Description of sample process variations.

6.4 Influence of the Substrate Interface on AIC

Two distinctly different SPE patterns are observed for the different samples listed in Table 6.1. Examples are shown in Figs. 6.7a and 6.7b where the Al remaining after SPE is selectively etched away from the Si surface. The Si epi-layer seen in Fig. 6.7a displays a wavy pattern covering the whole surface as is representative for the WetHF samples, while for all the other samples isolated well-defined crystals of Si are scattered randomly across the surface as illustrated in Fig. 6.7b. These different results can be related to the perfection of the Si surface that the Al/α-Si stack is deposited on. The WetHF samples have a smooth native-oxide-free Si surface whereas the WetBHF samples are not well hydrogen-passivated against native oxide formation and the DryHF samples will have some degree of plasma-induced damage of the Si surface. The appearance of well-defined crystals in the latter two cases suggests that a significant number of nucleation centers for silicon epitaxy have been generated by this type of surface treatment, in contrast to the WetHF samples.

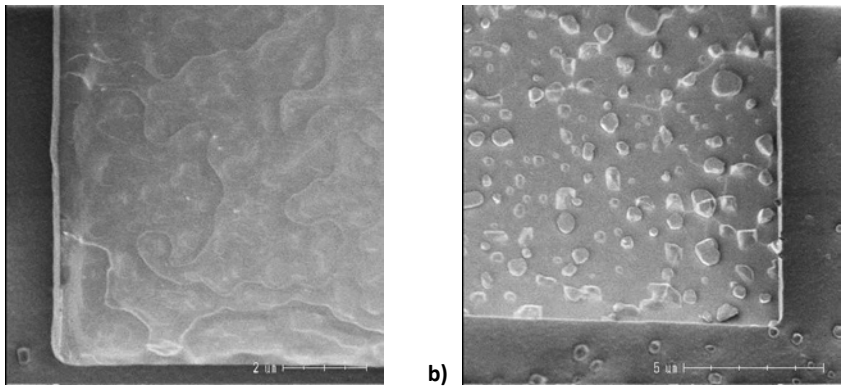


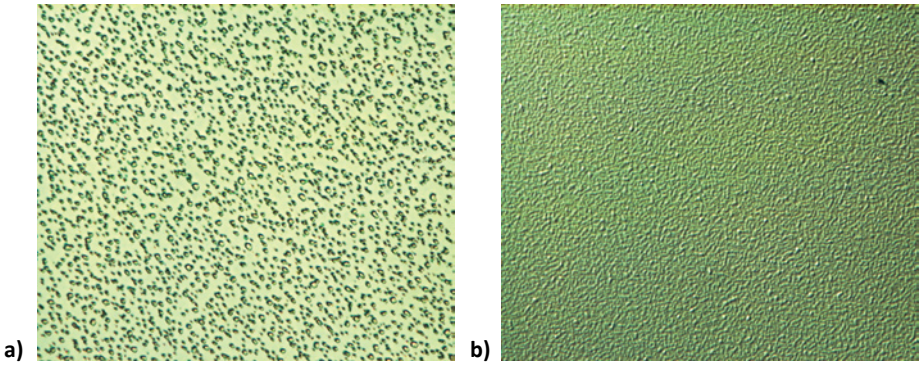
FIGURE 6.7:

SEM micrographs showing the SPE-Si structure after the Al/α-Si layer exchange at 400°C and selective Al removal, for a) WetHF[200, 20], and b) DryHF[200, 20] samples. The inset clearly shows remnants of the original Al grain boundaries.

Additional tests were conducted on bare Si wafers, some of which were immersed only in BHF (WetBHF), while others were further dipped in HF followed by Marangoni drying (WetHF) (Fig. 6.8). As expected, SPE on the WetBHF set resulted in a pattern of isolated Si crystals while the WetHF samples provided a continuous layer of thin Si across the whole wafer surface.

FIGURE 6.8:

Optical image of unpatterned Si wafers, showing the SPE-Si structure after the Al/α-Si layer exchange at 400°C and selective Al removal, for a) WetBHF[200, 20], and b) WetHF[200, 20] samples.



6.5 C-Si Growth Kinetics and Layer Properties

The close-up image shown in the inset of Fig. 6.7b reveals thin tracks decorated by crystal sprouts that are a witness of the former grain boundaries in the original Al layer. This shows that the Si atoms that travel through grain boundaries during the annealing step coalesce soon after reaching the substrate, rather than diffusing along the Al/c-Si interface, and the preferential growth direction of the crystal is vertical. The maximum observed crystal size is

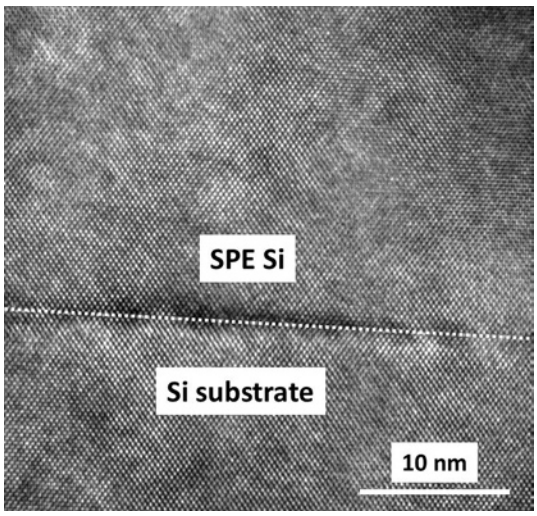
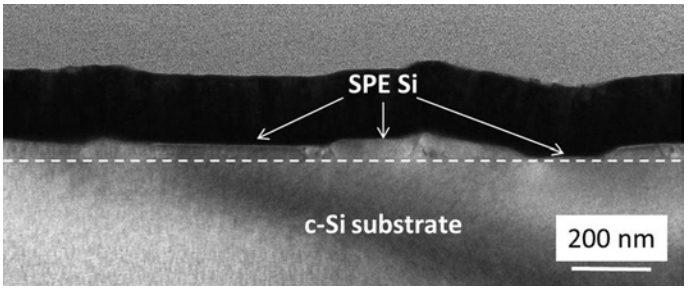


FIGURE 6.9:

HRTEM of SPE-Si on the c-Si substrate showing epitaxial growth. The sample is prepared according to the WetHF[100, 50] procedure.

FIGURE 6.10:

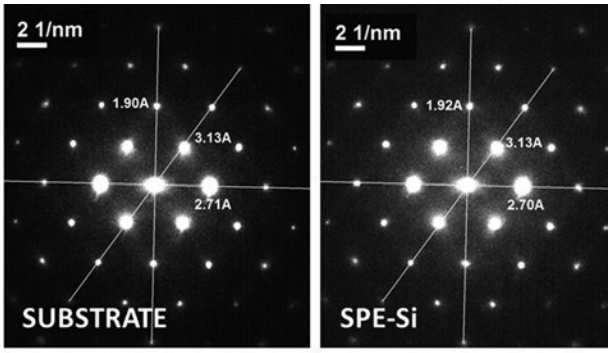
Lower magnification TEM of SPE-Si on the c-Si substrate showing the heigth varations of the Al-mediated SPE Si islands.



≈ 1–2 μm^2 and, in the case shown in Fig. 6.7b, crystals are too far apart to merge and form larger islands. This is the limiting factor in filling large areas with this type of Al-mediated SPE process. In contrast, Fig. 6.7a displays an example of how a defect-free Al/c-Si interface results in a long lateral diffusion length of the Si atoms supplied from the α-Si layer through the Al grain boundaries. Thus, the whole available open area can be covered with SPE Si. The remnants of Al grain boundaries are still visible, but the substrate surface is fully covered with the Al-doped epi-Si layer. This conclusion is substantiated by the electrical characterization discussed in the next section.

FIGURE 6.11:

Nanobeam-diffraction pattern of substrate Si and SPE-Si showing matching of the d-spacing for (111), (002), and (022) directions.



Microscopy analysis (TEM, NDA, AFM) was performed on 60×60 μm^2 large windows on the WetHF[100,50] samples. After the layer exchange of Al and Si at 400°C, Al is selectively removed in HF and the samples are cleaned in a HNO_3 solution. As can be seen in Fig. 6.9, the TEM analysis substantiates that the growth is epitaxial. On lower-magnification TEMs some facet twinning is observed where the individual Si islands join together, mainly at the former

Al grain boundaries, and the layer varies in height from a few atom layers up to 100 nm, which is the thickness of the original Al layer exchange mediator layer (Fig. 6.10).

In Fig. 6.11 the NBD pattern of the SPE Si is compared to that of the underlying c-Si substrate. The interatomic spacing (d-spacing) is determined and the lattice matching is within 0.01 Å, which is within the measurement error of the NBD technique. The crystal orientation follows the substrate (100) orientation having only a slight tilt of 0.05 degrees observed around the <110> zone axis.

The AFM analysis shown in Fig. 6.12 supports the TEM picture of large height variations with peaks up to 100 nm high. It also makes clear that there is a significantly higher average thickness at the edge of the window near the oxide. The thickening comes either from Si atoms deposited on the oxide layer that have sufficient diffusion lengths to reach the oxide-opening to silicon, or from defect-enhanced crystallization at the SiO_2 interface which has previously been documented for this type of Al-mediated SPE process [69].

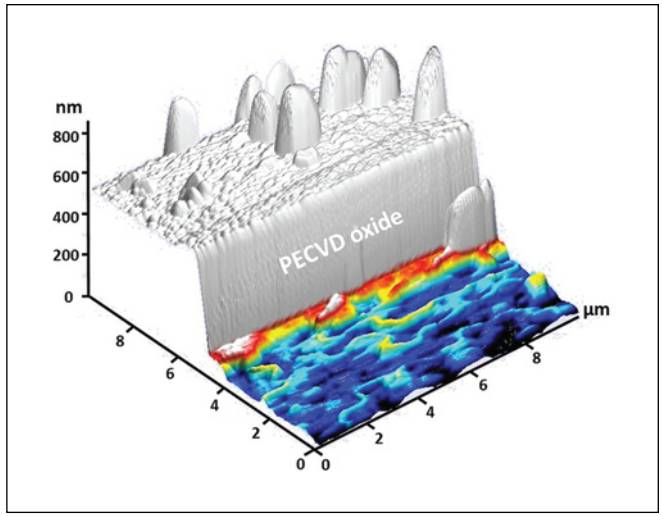


FIGURE 6.12:

AFM analysis of an SPE-Si surface near the oxide at the window perimeter where the SPE-Si layer is thicker (red color); for the WetHF[100, 50] sample.

6.6 Electrical Characterization of Al-doped SPE p^+n Diodes

The I-V characteristics of diodes fabricated in the WetBHF and DryHF procedures only show ideal p^+n behavior for the smallest window areas while for the larger sizes Schottky-like characteristics are observed. This is in accordance both with earlier results that were based on this type of processing and with the SEM analysis that shows that coalescence of the SPE silicon into crystals is limited to islands of 2 to 3 microns in size. All in all, it can be concluded that large areas of the c-Si substrate are not covered with SPE Si in these cases.

In contrast, the WetHF SPE diodes are ideal for all sizes. Representative I-V characteristics are shown in Fig. 6.13 for the smallest and largest fabricated areas of 1×1 μm^2 and 1×1 cm^2, respectively, and compared to Shottky diodes of the same sizes. It is remarkable that the large 1×1 cm^2 SPE diode has a saturation current per unit area that is of the same low level as the small diode, and also that an ideality factor as low as 1.02 is recorded. This indicates a good SPE Si coverage over the whole 1×1 cm^2 surface as already suggested by the SEM/TEM analysis. Moreover, it can be seen in Fig. 6.14 that both the forward and reverse currents

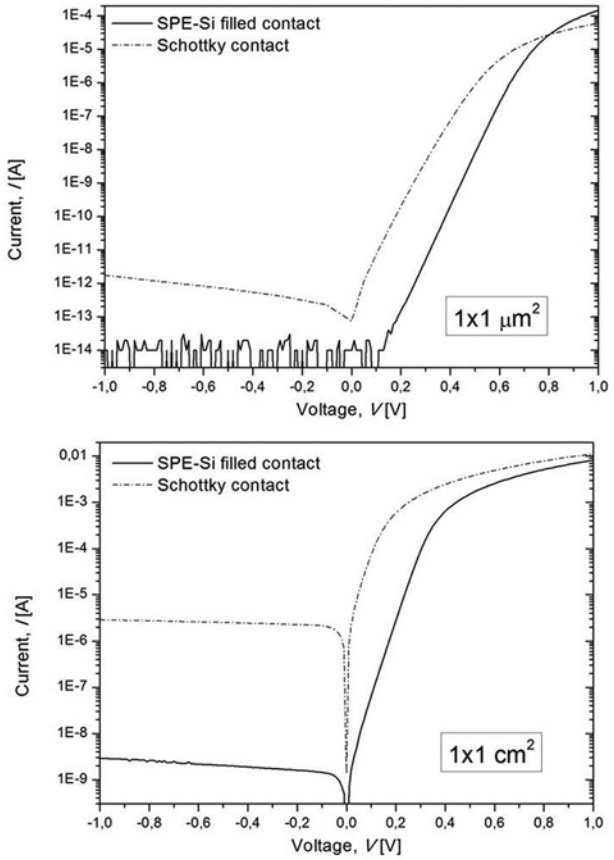


FIGURE 6.13:

Measured I-V characteristics of 1×1 μm^2 and 1×1 cm^2 WetHF SPE-Si diodes compared to those of Schottky diodes of the same size.

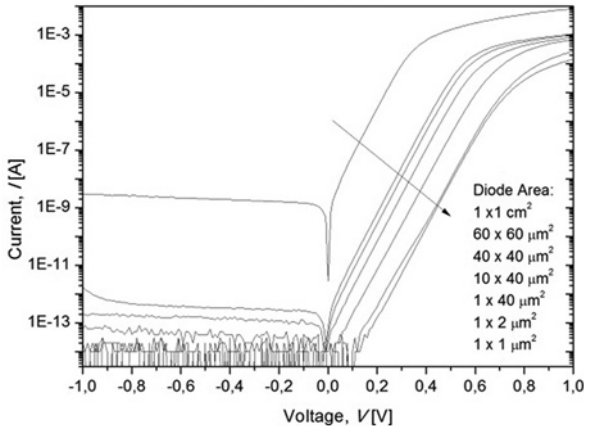


FIGURE 6.14:

Measured I-V characteristics for the set of WetHF[200, 20] SPE-Si diodes with anode areas: 1×1 cm², 60×60 μm², 40×40 μm², 40×10 μm², 40×1 μm²,1×2 μm², and 1×1 μm².

scale as expected with the diode area. The low leakage current corroborates that there is a very low defect-density at the interface of the SPE Si and the c-Si substrate as observed in the HRTEM (Fig. 6.9).

To determine the mechanism behind the leakage current, the temperature behavior was monitored using Arrhenius-like plots [81]. If we consider two main leakage contributors, drift and diffusion current component, the temperature behavior difference stems from the fact that the drift component depends linearly on the intrinsic carrier concentration, while diffusion component changes with its square:

$$J = q\sqrt{\frac{D_p}{\tau_p}}\frac{n_i^2}{N_D} + q\frac{d_B}{2\tau_0}n_i, \tag{6.1}$$

where J is the diode current density, D_p is the diffusion constant, τ_p the minority carrier lifetime, N_D the substrate doping, n_i the intrinsic carrier concentration, d_B the width of the depletion region, and τ_0 generation-recombination carrier lifetime. Further, using the relation for the temperature dependence of the intrinsic carrier concentration as follows

$$n_i^2 = CT^3 exp\left(-\frac{E_g}{kT}\right), \tag{6.2}$$

where C is the constant with negligible temperature coefficient, T is the temperature, and E_g the silicon energy bandgap, we can derive the temperature dependence of the reverse current. In this case, when plotting current versus temperature in a log-lin scale, the slope of the curve can be read out and will reveal the exponent argument of the Eq. 6.2. If the extracted energy from the argument, i.e. activation energy, corresponds to the Si bandgap E_g, the dominant influence of the n_i^2 indicates the contribution from diffusion current. If, however, the extracted energy is closer to $E_g/2$, the current depends stronger on the n_i, which is the indicator of the dominant generation-recombination mechanism.

Diode areas of 1×1 μm², 40×40 μm², and 60×60 μm² were measured from 25°C to 190°C and the Arrhenius plot is shown in Fig. 6.15. The extracted activation energy E_a is 1.05 eV, 0.97 eV, and 0.94 eV, respectively, at 2 V reverse bias. These values are all close to the Si bandgap value E_g, indicating that the dominant origin of the dark current is from ideal dif-

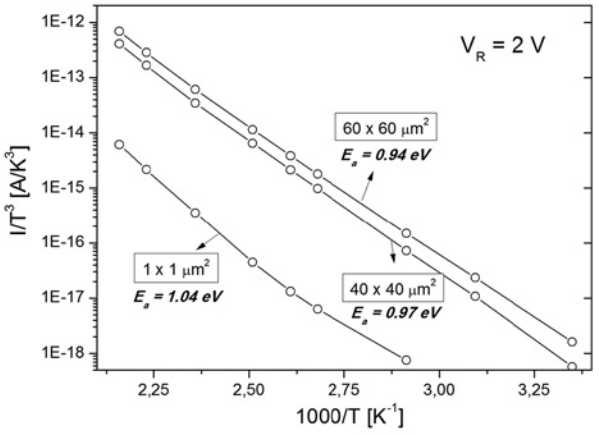


FIGURE 6.15:

Arrhenius plots of 1×1 μm², 40×40 μm² , and 60×60 μm² WetHF[200, 20] SPE-Si diodes, measured at 2 V. The values in figures are activation energies (eV).

fusion over the depletion regions and not from defect-related generation-recombination currents.

According to earlier SIMS analysis [82], the Al-mediated SPE-Si layer contains a high concentration of Al which p-dopes the layer up to the limits set by the solubility and diffusivity of Al in Si at the given annealing temperature, in this case at 400°C. Hole injection from this p-region can be verified by the method proposed in [83], where adjacent SPE islands are connected in a lateral pnp configuration. Measurements of this type confirmed that for the given layer-stacks and anneal cycle there is a high level of p-doping in the SPE islands, which is in accordance with the low saturation current and ideality of the diode characteristics. Due to the high anode doping, the diode breakdown voltage is set by the lower substrate doping, in this case the Si wafer with 2-5 Ωcm resistivity. The recorded 65 V breakdown for 1×1 μm² diodes matches well with previously reported 70 V [84], while for the larger diodes of 1×1 cm² the average measured breakdown occurs at ≈ 85 V. This suggests that the bulk breakdown is higher than the perimeter breakdown which is to be expected since no guard rings are implemented in these structures.

The Al layer used in the AIC process should not be less than about 50 nm thick, otherwise the resulting Si crystalline quality is compromised [85]. In this work an Al thicknesses of 100 nm or 200 nm is used and in this range no significant influence on diode properties is observed provided the same α-Si thickness is applied. With respect to the thickness of α-Si, samples were compared with either a 20 nm or 50 nm α-Si layer. While the saturation current and the ideality factor of the diodes remained unaffected by the available amount of Si, the series resistance did slightly increase as the Si thickness was increased. This is observed over several batches and for different diode sizes, and cannot be explained by the spread in the substrate wafer resistivity. It is assumed that the increase in resistance is caused by the limited annealing time and temperature made available for the layer exchange process: a layer of non-crystallized α-Si may remain on the surface, thus increasing the resistance of the layer. For example, 10 devices with an area of 40×40 μm² were measured to have a series resistance of 315 ± 20 Ω for the 20-nm-Si device, and 485 ± 65 Ω for the 50-nm-Si device. These are very high series resistances but previous work on Al-mediated SPE islands has shown that low-ohmic resistivity values less than 10^{-7} Ωcm can be achieved [71]. In this flow the corrupted AIC Al layer is removed before the final metallization.

6.7 Conclusions

Amorphous Si thin films have been crystallized over arbitrarily large c-Si surfaces at 400°C using an Aluminum-Induced Crystallization process. An epitaxial layer coverage that is continuous, monocrystalline, and highly p-doped with Al, is achieved by minimizing the density of nucleation centers on the wafer surface, achieved here by wet-patterning of the isolation oxide layer in BHF 1/7 and H-passivating the c-Si interface with a HF 0.55% dip-etch followed by IPA-Marangoni drying. The epitaxial growth of Si takes on the orientation and the lattice constant of the underlying c-Si substrate. A defect-free interface is verified by HRTEM imaging and by the low leakage of p^+n diodes of areas ranging from 1×1 μm^2 up to 1×1 cm^2. The very large diodes have ideality factors as low as 1.02, and leakage current levels of only 2-3 nA at 1 V reverse bias. The fact that such arbitrarily large high-quality diodes can be made at sub-metallization temperatures make this process very attractive as an add-on to fully-processed CMOS or for diode processing in large-area electronics and c-Si solar cells.

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CONCLUSIONS AND RECOMMENDATIONS

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CONCLUSIONS AND RECOMMENDATIONS

7.1 Conclusions

As a result of this thesis work, PureB backscattered electron detectors are now recognized as a new generation of detectors for Scanning Electron Microscopy. In the course of the project, the first FEI SEM machines equipped with PureB detectors were placed on the market. This means that the device, that initially was a pure research pursuit, has undergone a trajectory of prototyping, optimization for demanding industrial specifications such as reliability, robustness, and reproducibility, in order to reach a product that now can be called production-worthy. The whole project was from the start aimed at creating detectors that would meet the demands of industry and the interaction with the end users lead to a heighten awareness of many of the issues involved. One of these is the low signal-to-noise ratio, for which on-chip JFET preamplifiers were identified as a potential solution. To increase the possibilities for integration with the particle detectors, several low-temperature processes for fabrication of the JFET gate were considered. The work on Al-mediated solid-phase epitaxy presented in this thesis has shown that this could become a gate-fabrication process that enables integration as a post-metallization step.

This thesis work was performed in cooperation with several other projects involving the PureB technology for a variety of applications. Some of the overall results can be summarized as follows:

- The photodiode detector applications have demonstrated that the PureB technology enriches Si technology with new and potent processing capabilities. The boron films are formed at relatively low processing temperatures (< 700°C) resulting in ultrashallow p^+ junctions, far less than 10 nm deep. Besides the very good ideality of PureB diodes, the most unique feature is that saturation current is as low as in conventional deep p^+n junctions.
- The uniformity and reproducibility of the PureB-layer thickness are identified as vital factors for shallow-penetration radiation detectors. For optimized performance, the PureB depositions are operated at the limit of layer formation (< 2 nm), and it is shown that sub-nm non-uniformities of this layer have an enormous impact on detection efficiency at low electron energies. By optimizing the layout design and deposition parameters, the deposition of a uniform, reliable and reproducible 2-nm-thick PureB-layer is demonstrated.

- The PureB layer does not oxidize to any significant degree in air, which would otherwise be detrimental for charging effects in SEM systems. Additionally, PureB junctions show neither signs of optical nor electrical degradation when irradiated by SEM-energy-range electrons. Any rise in dark current is always related to the photodiode perimeter, probably due to damage of the isolation-oxide interface. The pre-exposure low dark current level is readily restored by relatively short low-temperature annealing. Similarly robust behavior is encountered when applying periodic cleaning of the PureB detector surface using aggressive gasses such as hydrogen radicals and oxygen plasmas, required to prevent the build-up of carbon contaminating layers that are typical for vacuum environments.
- Ultrashallow-junction technology makes it possible to make solid-state detectors that have high efficiency for electron detection at sub-keV energies, thus enabling an impressive enhancement of the performance of SEM systems. The use of nm-thin PureB layers to fabricate the electron detector anode facilitates the suppression of the main energy loss mechanism in the below-keV region, i.e., the dead layer losses.

The following results have issued specifically from the work presented in this thesis:

- The PureB layer acts as a reliable diffusion barrier between Si and pure Al, given that it completely covers the Si substrate. Combined with the fact that pure Al can be selectively removed from the PureB surface using a HF 0.5% metal etchant, this property is of crucial importance for achieving a spike- and precipitate-free PureB surface layer as front-entrance window for shallow-penetration beam detectors.
- The p^+-anode and α-B layers together have a sheet resistance of ≈ 10 kΩ. To nevertheless obtain a low series resistance on large diode segments, an Al grid is patterned directly on the diode surface. It is of utmost importance that the electrode grid covers only a small part of the photosensitive area, so as not to reduce the detection efficiency. Here a 1 μm grid dimension was used so that less than 2% of the front-window was covered. Nevertheless, this significantly lowers the series resistance, e.g. from 280 Ω to 20 Ω for a 44 mm^2 large diode.
- The overall performance of PureB detectors is well above that of state-of-the-art commercial photodiode detectors, nearly approaching the theoretical limits, measured in this thesis down to 200 eV energies. The measured electron gain is expressed as a ratio between the output PureB photodiode current and the input electron beam current, and it yields the following gain values at low electron energies: 34 at 200 eV, 101 at 500 eV, and 212 at 1 keV.
- The detector fabrication technology presented here is highly reliable and enables flexible configurations including segmented, closely-packed photodiodes and through-wafer apertures. The isolation of the individual photodiodes of the detector is facilitated by using low-resistivity wafers

on which a thick well-controlled lightly-doped epitaxial layer is grown. In this manner the isolation could be combined with capacitance values as low as 3 pF/mm^2. A method of growing near-intrinsic, high-quality, thick epi-layers by exploiting the segregation behavior of arsenic was developed.

- An alternative approach was explored for fabrication of closely-packed, large-area low-capacitance photodiodes. It is based on the use of high-resistivity-Si substrates that enable very wide depletion regions, i.e. low capacitance, at the expense of increased series resistance. To decrease the series resistance, local thinning of the undepleted detector substrate below the anode region was implemented. Devices were successfully fabricated with a junction capacitance below 1 pF/mm^2.
- Al-induced crystallization is a potent alternative to laser-induced crystallization by delivering several tens of microns large grains that can be further enlarged by annealing steps. When applied on c-Si substrates, it results in a low-temperature epitaxy of Al-doped layers of Si. It was demonstrated that the growth dynamics are strongly influenced by the density of nucleation sites on the underlying c-Si substrate. By optimized surface treatments, the density of nucleation centers was minimized and this allowed a defect-free epitaxial growth over mm^2-size areas. This has been verified by applying the AIC technology to the fabrication of p^+n diodes, where the good ideality of the diode and the low level of the saturation current confirmed the quality of the p^+ layer.

7.2 Future Work

- Since the efficiency of the PureB detectors is the highest recorded so far on the overall SEM energy scale, it would benefit the further development to trace and quantify the specific losses encountered in the sub-keV energy range. In particular, the backscattering from PureB Si diodes can be measured, and, for example, by incident angle tilt techniques the role of the dead layer loss can be quantified, and the possibilities for implementing further optimization can be evaluated.
- The ionization energy of silicon (or, the energy expended for the electron-hole pair creation) is a basic material property, that has so far been measured for several types of radiation and energies. However, the ≈ 3.6 eV threshold value has not yet been verified for low energy electrons (< 1 keV). The availability of a high efficiency Si electron detector operating in < keV energy range, opens the possibility of properly estimating the losses in this range so that the ionization constant could be extracted.
- If the ionization energy of silicon imposes the ultimate limit on the detector efficiency, it may be worthwhile to consider another material that requires less energy to create electron-hole pairs. For example, germanium has lower ionization for the detection of low-energy electrons. There is, however, a trade-off with a higher dark current.
- The RC constant of the detector can be further lowered in two ways: (a) the series resistance could probably benefit from a redesign of the anode grid metallization to optimize the grid line spacing, and (b) the capacitance value can be lowered either by using fully-depleted high resistivity wafers where the isolation of the detector pixels is achieved by etching the silicon to physically separate them (trench formation), or by making the anode size smaller and controlling the drift of the carriers towards the targeted anode, similar to silicon drift detectors.
- In order to integrate the photodiodes with JFETs using Al-mediated SPE gates, the key device parameter that should be measured is the 1/f noise. It is closely related to the quality of all junctions and may reveal imperfections of the interface forming the SPE junction.
- Although PureB layers do not show signs of optical or electrical degradation when exposed to electron irradiation, the deteriorating influence of the diode perimeter at the oxide interface has been identified. This aspect should be further investigated in order to design devices that are stable under prolonged electron irradiation.

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SUMMARY

Detection of low-energy electrons offers potent solutions to future challenges in nanometer-scale inspection and imaging. In particular, Low-Voltage Scanning Electron Microscopy (LVSEM) that is based on low-energy electron detection is becoming the preferred inspection method in the semiconductor industry. It provides atomic-scale resolution of the specimen surface due to the short range of electrons in matter, and the suppression of charging effects that for higher voltages obscure the imaging of the non-conducting materials often used in semiconductor device fabrication. Among the challenges facing LVSEM are high-performance low-energy backscattered-electron (BSE) detectors. The basic principles of LVSEM operation that determine the main requirements placed upon the detector design are given in Chapter 1. Specifically, the loss mechanisms are discussed that are involved in the direct detection of low-energy charged particles: the dead layer loss and the backscattering loss. The former arises due to the nm-range interaction volumes of such particles in bulk materials that demand high sensitivity at the very surface of the detector for a good responsivity. The non-responsive portion of the surface is designated as the 'dead layer'. The latter will depend highly on the material of the detector, the imaging energy, and the angle at which the electrons penetrate the surface. When designing a detector, advantage can be gained by using materials with low atomic number (low-Z materials), for which the backscattering effect is minimized.

In Chapter 2 a description is given of a new photodiode technology based on a recently developed boron layer (PureB) technology for creating nm-deep p^+n junctions that have been proven to give exceptionally high responsivity for low-penetration-depth radiation such as deep/extreme ultra-violet light (DUV/EUV) and low-energy electrons. The PureB forms front-entrance windows where the photosensitive depletion layer is only covered by a nm-thin p^+ anode under an equally thin amorphous boron layer, thus allowing record-high electron-signal-gain for electron energies as low as 200 eV. The thin layer can be uniformly deposited over large Si areas with only few angstroms thickness variations over a patterned wafer, which guarantees a correspondingly uniform detection efficiency. Furthermore, the PureB layer facilitates a straightforward metallization of the detector surface that otherwise is complicated by the requirement that the photodiode metallization has to be fully removed from the nm-thin PureB layer in order to allow the incident electrons to reach the responsive region. As a solution, it has been demonstrated that the PureB layer can be used in combination with pure Al metallization, since it provides a reliable diffusion barrier between the Al and the underlying Si substrate thus preventing Al-spiking of the Si that would spoil the critical surface quality. The more commonly used metallization for avoiding spiking is Al with 1% Si but this cannot be applied since precipitates of Al-doped Si on the PureB surface are left after the Al is selectively etched away. In contrast, pure Al can be completely

removed from the PureB layer by using a HF 0.5% solution to which the PureB is highly resistant. Finally, the resulting photodiode with the exposed PureB surface is tested in a vacuum environment and under SEM-energy-scale electron irradiation where it shows neither signs of optical nor electrical degradation.

In Chapter 3 the operating speed, i.e., the RC constant, of the photodiode detector is addressed. The Si substrate wafer is used as a cathode terminal of the device, and will therefore be decisive for the overall RC. The resistivity of the substrate has to be sufficiently low to allow for the low series resistance, while at the same time it also needs to be adequately high to promote the wide depletion region that is a prerequisite for obtaining low capacitance values. To reconcile these two conflicting demands, a technology has been developed to epitaxially grow very high-resistivity, tens-of-microns thick n-layers on low-ohmic substrates using an arsenic doping technique. In this way the capacitance is decoupled from the resistance because, once the high resistivity epi-layer is depleted, the resistance is governed only by the low-ohmic substrate, while the thickness of the depletion region in the high-resistivity layer defines the capacitance value. Here the tendency of arsenic to segregate on the Si surface during epitaxy is exploited to control the doping in the high-resistivity epi-layer down to almost-intrinsic values, thus allowing full depletion of the layer. The n-doping can be tuned using the three main process parameters: the As doping of a seed layer grown before switching to epigrowth without flowing AsH_3 over the wafer, the layer thickness, and the sequence of growth cycles. Increasing the As concentration of the seed layer increases the doping profile of the whole epi-layer although it gradually decreases as the layer growth progresses, i.e. the epi-thickness increases. Consequently, the thicker the layer the lower the doping at the surface. The doping level can be slightly readjusted during growth by stopping and resuming the growth cycle, which will result in a minor elevation of the doping profile that can, for example, prevent the layer from counter-doping when the doping levels are very low. To characterize the layers, verify the absence of defects, and control the doping uniformity, dark current measurements and the C-V profiling are employed.

When integrated with the PureB electron detectors, the As-doped high-resistivity thick epi-layers facilitate a segmentation of the detector anode layout. The photosensitive detector surface can be maximized and a low diode capacitance is combined with lateral junction isolation of the photodiode segments. As an example, the full detector design of an 8-photodiode-segment PureB backscattered-electron detector is presented and evaluated in Chapter 4. Besides the high detection efficiency obtained by the photodiode design described in Chapter 2, and the low RC constant obtained by using an epitaxial high-resistivity layer grown on a low-ohmic substrate as described in Chapter 3, the detector combines several other unique processing techniques that boost the performance: the series resistance of the PureB layer is additionally lowered by patterning a fine aluminium grid directly on the PureB surface, and through-wafer apertures are etched in the detectors close to the anode regions for beam-coaxial positioning designed to monitor back-scattered electrons in SEM systems. A variety of fabricated detectors have been tested for specific functions such as topographical and Z-contrast imaging, and high-resolution images are obtained for sub-keV electron energies.

An alternative method for obtaining a low RC constant is proposed in Chapter 5. The detector design is transferred to high-resistivity substrates which enables the further lowering of the capacitance values, while the series resistance is restrained by local thinning of the undepleted substrate bulk. The bulk-micromachining steps are combined with the through-

wafer aperture etching steps to keep the process complexity manageable, and the resulting detectors are finished with 100-μm-thick Si membranes.

To get full advantage of the low capacitance levels of the detectors it is also necessary to have suitable signal-processing electronics integrated with the detector in the SEM system. In particular, the preamplifier stage and the wiring that are connected directly to the detector have to match the low capacitance values, and it would be advantageous for many applications to integrate them on the detector chip. With such applications in mind, an Aluminum-Induced Crystallization (AIC) technology was developed and presented in Chapter 6. This technology enables post-metallization junction formation that in turn enables low-complexity process schemes for on-chip integration of the first amplifier stage. The AIC is specifically optimized to fill arbitrarily-shaped and -sized openings with high quality p-doped c-Si layers. The I-V characterization of fabricated p^+n diodes and HRTEM analysis substantiates that the junction interface is practically defect-free. This is achieved by minimizing the number of nucleation centers on the starting Si substrate by employing dedicated surface preparation steps: wet-patterning of the final window opening with a HF 0.5% dip and Marangoni-IPA drying. Moreover, the AIC p^+n junctions fabricated at sub-400°C process temperatures have low leakage currents which makes this process generally attractive as an add-on to fully-processed CMOS wafers, for diode processing in large-area electronics, and in c-Si solar cells.

SAMENVATTING

Detectie van lage-energie elektronen biedt een krachtige oplossing voor toekomstige uitdagingen in nanometerschaal inspectie en beeldvorming. In het bijzonder lage spanning rasterelektronenmicroscopie (LVSEM), welk is gebaseerd op lage-energie elektron detectie, is steeds meer de geprefereerde inspectie methode in de halfgeleider industrie aan het worden. Het biedt atoomschaal resolutie van het preperaatoppervlak dankzij de korte afstand van elektronen in materie en de suppressie van opladingseffecten welk voor hoge spanningen de beeldvorming van, in de halfgeleider industrie vaak gebruikte, niet-geleidende materialen vervaagd. Een van de uitdagingen voor LVSEM zijn hoge prestatie detectoren voor lage-energie teruggestrooide elektronen (BSE). De basis principes van de LVSEM werking welk de belangrijkste eisen van het detector ontwerp bepalen zijn gegeven in **Hoofdstuk 1**. Specifiek worden de verlies mechanismen behandeld die betrokken zijn in de directe detectie van lage-energie geladen deeltjes, namelijk de dode laag en terugstrooings verliezen. De eerste ontstaat door de nm-bereik interactie volumes van zulke deeltjes in bulkmaterialen hetgeen hoge gevoeligheid aan het oppervlak van de detector vereist voor een goede responsiviteit. Het non-responsieve gedeelte van het oppervlak wordt aangeduid als de 'dode laag'. De laatste hangt zeer veel af van het materiaal van de detector, de beeldvormingsenergie en de hoek waaronder de elektronen het oppervlak penetreren. Tijdens het ontwerpen van een detector kan voordeel worden behaald in het gebruik maken van materialen met een laag atoomnummer (lage-Z materialen), waarvoor het terugstrooings effect geminimaliseerd is.

In **Hoofdstuk 2** wordt een beschrijving gegeven van een nieuwe fotodiode techniek gebaseerd op een recent ontwikkeld boor laag (PureB) technologie voor het creëren van nm-diepe p^+n juncties welk zijn bewezen uitzonderlijk hoge responsiviteit te geven voor lage penetratie- diepte straling zoals diep/extreem ultraviolet licht (DUV/EUV) en lage energie elektronen. De PureB vormt vooringang openingen waar de fotosensitieve depletie laag alleen bedekt is door een nm-dunne p^+ anode onder een even dunne amorfe boor laag, dat op deze manier recordhoge elektronen-signaal-versterking toestaat voor elektron energie zo laag als 200 eV. De dunne laag kan uniform over grote Si gebieden worden gedeponeerd met een dikte variatie van slechts een paar ångström over een gepatroneerde wafer, welk een overeenkomstige uniforme detectie efficiëntie garandeert. Bovendien faciliteert de PureB laag een eenvoudige metallisatie van het detector oppervlak die anders ingewikkeld wordt gemaakt door de vereiste dat de fotodiode metallisatie volledig moet worden verwijdert van de nm-dikke PureB laag zodat de inkomende elektronen het responsieve gebied kunnen bereiken. Het is aangetoond dat de PureB laag kan worden gebruikt in combinatie met puur-Al metallisatie, aangezien het een betrouwbare diffusie barrière biedt tussen het Al en onderliggende Si substraat, waardoor Al *spiking* van het Si wordt voorkomen welk de

kritische oppervlaktekwaliteit zou bederven. De meer gebruikelijke metallisatie om *spiking* te voorkomen is Al met 1% Si, maar deze kan niet worden gebruikt aangezien neerslag van het Al gedoteerde Si overblijft nadat het Al selectief is weggeëtst. Puur Al kan, in tegenstelling, volledig worden verwijdert van de PureB laag door middel van een 0.5% HF oplossing, waartegen PureB zeer resistent is. Tenslotte is de resulterende fotodiode met het blootgestelde PureB oppervlak getest in een vacuüm omgeving en onder SEM-energieschaal elektronen irradiatie, waarbij het geen tekenen van optische of elektrische degradatie toonde.

In **Hoofdstuk 3** wordt de werksnelheid, dat wil zeggen de RC constante, van de fotodiode besproken. De Si substraat wafer wordt gebruikt als de kathode-aansluiting van de diode, en zal daarom bepalend zijn voor de totale RC. De resistiviteit van het substraat moet voldoende laag zijn om een lage serie weerstand toe te staan, terwijl het op hetzelfde moment afdoende hoog moet zijn om een groot depletiegebied te promoten, welk een eerste vereiste is om lage capaciteitswaarden te verkrijgen. Om deze twee conflicterende vereisten te verzoenen is er een techniek ontwikkeld om een zeer hoog resistieve, tientallen micronen dikke, n-lagen epitaxiaal te groeien op laag-ohmische substraten doormiddel van een arseen dotering techniek. Op deze manier wordt de capaciteit ontkoppelt van de weerstand, omdat (zodra de hoge resistiviteit epi-laag uitgeput is) de weerstand alleen beheerst wordt door het laag-ohmische substraat, terwijl de dikte van het depletie gebied in de hoge resistiviteits laag de capaciteitswaarde definieert. Hier wordt de neiging van arseen om zich op het silicium oppervlak te segregreren tijdens de epitaxie uitgebuit om de dotering in de hoge resistiviteit epi-laag naar bijna intrinsieke waarden te verlagen, zodat volledige depletie van de laag mogelijk is. De n-dotering kan worden afgestemd door middel van de drie voornaamste proces parameters: de As dotering van een zaadlaag gegroeid voordat er naar epigroei zonder AsH_3 toevoeging wordt geschakeld, de laagdikte en de volgorde van groei cycli. Het verhogen van de As concentratie van de zaadlaag verhoogt het doteringsprofiel van de gehele epi-laag, hoewel het geleidelijk vermindert wanneer de laaggroei vordert, d.w.z. de epi-dikte toeneemt. Zodoende is de dotering van het oppervlak lager als de laag dikker is. Het doteringsniveau kan licht worden bijgesteld gedurende de groei door het stoppen en hervatten van de groei cyclus, welk resulteert in een kleine verhoging van het doteringsprofiel dat bijvoorbeeld kan voorkomen dat de laag tegen-doteert wanneer het doteringsniveau erg laag is. Voor het karakteriseren van de lagen, het verifiëren van de afwezigheid van defecten en het controleren van de doteringuniformiteit, worden donker stroom metingen en CV-profilering gebruikt.

Wanneer geïntegreerd met de PureB detectoren faciliteren de As-gedoteerde hoge-resistiviteit dikke epi-lagen een segmentatie van de lay-out van de detector anode. Het fotosensitieve detector oppervlak kan worden gemaximaliseerd en een lage diode capaciteit wordt gecombineerd met een laterale junctie isolatie van de fotodiode segmenten. Als voorbeeld wordt een volledig detector ontwerp van een ringvormige 8-fotodiode-segmenten PureB terugstrooings elektronen detector gepresenteerd en geëvalueerd in **Hoofdstuk 4**. Naast de hoge detectie efficiëntie behaald door het fotodiode ontwerp beschreven in hoofdstuk 2 en de lage RC constante behaald door middel van een epitaxiale hoge-resistiviteits laag gegroeid op een laagohmig substraat zoals beschreven in hoofdstuk 3, combineert de detector verschillende andere unieke verwerkingstechnieken die de prestaties faciliteren: de serie weerstand van de PureB laag is verder vermindert door het aanbrengen van een fijn aluminium raster direct op het PureB oppervlak en door-wafer openingen worden geëtst in de detectoren dichtbij de anode gebieden voor straal-coaxiale positionering ontworpen om de terugstrooings elektronen in een SEM systemen te controleren. Een verscheidenheid van

gefabriceerde detectoren is getest voor specifieke functies zoals topografische en Z-contrast beeldvorming, en hoge resolutie beelden zijn behaald voor sub-keV elektronen energieën.

Een alternatieve manier om een lage RC constante te verkrijgen wordt voorgesteld in **Hoofdstuk 5**. Het detector ontwerp is overgedragen naar hoge-resistiviteit substraten waardoor een verdere vermindering van de capaciteitswaarde mogelijk is, terwijl de serieweerstand wordt teruggehouden door lokale verdunning van de onuitgeputte substraat bulk. De bulk-micromachining stappen worden gecombineerd met de door-wafer opening etsstappen, om de procescomplexiteit controleerbaar te houden, en de resulterende detectoren worden afgewerkt met 100-µm-dikke Si membranen.

Om volledig te profiteren van de lage capaciteitswaarden van de detectoren is het ook nodig om geschikte signaalverwerking elektronica te integreren met de detectoren in het SEM systeem. In het bijzonder moeten de voorversterkingstrap en de bedrading die direct verbonden zijn met de detector de lage capaciteitswaarden matchen en is het gunstig voor vele applicaties om deze op de detector chip te integreren. Met dergelijke toepassingen in het achterhoofd is een aluminium-geïnduceerde kristallisatie (AIC) techniek ontwikkeld en gepresenteerd in **Hoofdstuk 6**. Deze techniek maakt na-metallisatie junctie formatie mogelijk, die op zijn beurt lage-complexiteit bewerkingschema's voor *on-chip* integratie van de eerste versterkingstrap mogelijk maakt. De AIC is specifiek geoptimaliseerd om willekeurig vormgegeven en gedimensioneerde openingen te vullen met hoge kwaliteit p-gedoteerde c-Si lagen. De I-V karakteristieken van gefabriceerde p^+n diodes en HRTEM analyse onderbouwt dat het junctie grensvlak praktisch defectvrij is. Dit is bereikt door het minimaliseren van het aantal nucleatiecentra op het beginnende Si substraat middels toegewijde oppervlakte preparatie stappen: nat etsen van de uiteindelijke openingen met een 0.5% HF dip en Marangoni-IPA drogen. Bovendien hebben de AIC p^+n juncties gefabriceerd op sub-400°C bewerkingstemperaturen een lage lekstroom waardoor dit proces over het algemeen aantrekkelijk is als een toevoeging aan volledig bewerkte CMOS wafers voor diode verwerking in grote oppervlak elektronica en in c-Si zonnecellen.

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