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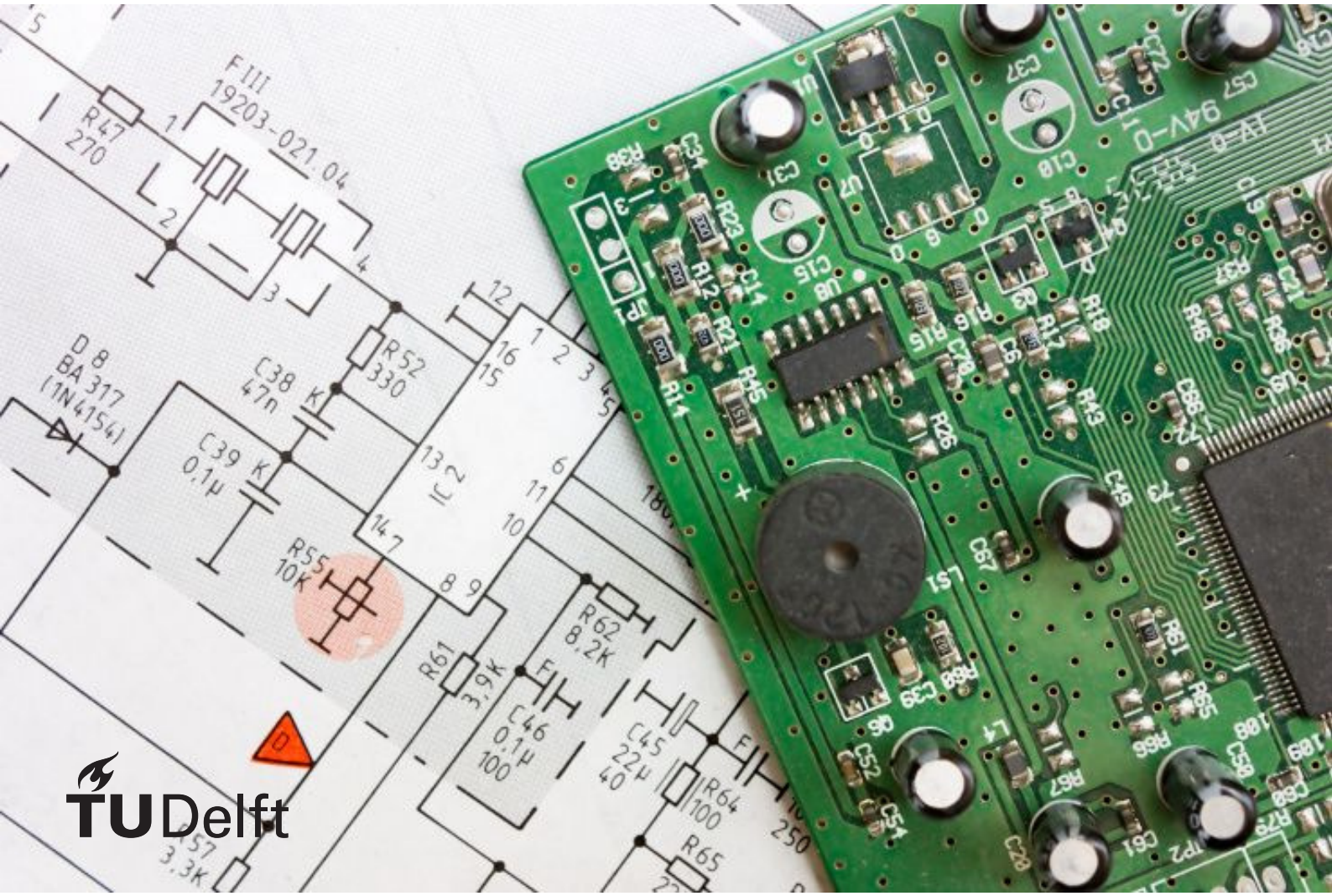
2019



Optimal design of a non-isolated high power density buck-boost converter

by

Yufan Cao

to obtain the degree of Master of Science
at the Delft University of Technology,
to be defended publicly on Friday, August 23, 2019, at 15:00.

Student number:	4748484	
Project duration:	November 19, 2018 – August 23, 2019	
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TU Delft

Preface

This thesis concerns the MSc graduation project at the Delft University of Technology co-operateing with Prodrive Technologies, Eindhoven, Netherlands, under the supervision of Prof. Pavol Bauer, Jordi Everts and Michel Hagenaar.

In this process, many difficulties came up and I can not finish it without the help from many people. I would therefore like to thank the following people:

- Prof. Bauer, my supervisor in TU Delft.
- Jordi Everts and Michel Hagenaar, my supervisors in Prodrive .
- Zian Qin and Gregory Pandraud, thesis committee members.
- My parents and friends.
- Prodrive Technologies company
- My parents and friends.
- Everyone who ever helps me.

I really appreciate these people, I can not finish my thesis without their help.

Yufan Cao
Delft, August 2019

Abstract

Semiconductor lifetime and power density are considered to be two important development directions of power converter design in the future. Especially in some high dynamic application, the operation condition is changing frequently causing the temperature swing of semiconductor, and it leads to thermal expansion and contraction which affects the lifetime or reliability of semiconductor. A high maximum temperature or a large temperature swing leads to short lifetime. Meanwhile, high power density is a general trend. If the size of a whole system is limited, a high power density converter enables more functionality of the system. Also, high power density also leads to high portability. Works have been done to use interleaved and high switching frequency converter to get a high power density. However, those converters such as interleaved buck converter do not help to improve semiconductor reliability because it can only operate in synchronous conduction mode (SCM) and triangular current mode (TCM).

In this work, a $20kW$ DC/DC converter for highly dynamic application is designed. The four-switch buck-boost converter is chosen because of its flexibility and its possibility to get longer semiconductor lifetime and higher power density. It is possible to offer a freewheeling interval in which no voltage is applied on the inductor, the transferred power can be regulated by adjusting the duty cycle of this interval. In addition, an optimal modulation scheme is proposed for this topology which further helps improve the reliability of semiconductor. An optimal power stage design is given which is a two-stage interleaved structure. Plus, a close-loop control strategy is given according to the design.

The proposed modulation scheme is tested with a low voltage level prototype, and the performance prediction is verified.

Contents

List of Figures

List of Tables

1

Introduction

1.1. Background

Over the last several decades, science and technology are developing rapidly. A significant change happens to people 's lives in many respects. For instance, personal communication technology is an obvious example which developed greatly. In 1980s, people's cell phone was weighing 2 kilograms with single calling function. However, today, almost everyone has a tiny smartphone, people can use it to do many things, for instance photographing, surfing the Internet, video chatting, mobile payment, etc. People could never image those activities could be done within a cell phone back to 1980s. Another example is the rapidly developing renewable energy which is one of the most popular topics due to the increasingly serious environment and energy crisis. More and more renewable energies are applied in daily life, for instance electrical vehicles are getting more and more popular all over the world. In addition to this, the computer science, robotics and artificial intelligence are all rapidly developing.

Integrated circuits (ICs) development does a great contribution to the technologies mentioned above and the demands of integrated circuits will keep rising. The state-of-the-art equipment for the automated production of integrated circuits are wafer scanners. In 1998, deep ultraviolet (DUV) lightsources were replaced by a more advanced one extreme ultraviolet (EUV) lightsource. The extreme ultraviolet (EUV) reduces the wavelength from $193nm$ to $13.5nm$, and smaller features can be produced on the integrated circuits. The wafer must be extremely accurately positioned in six motion degrees-of-freedom in a highly dynamic condition [21].

Fig. 1-1 shows the general structure of the power supply block in the wafer stage of the scanner. The 3-phase AC is rectified to a $960V$ DC by a rectifier, and it is converted to $630V$&$360V$ respectively. It is used to drive the long stroke and short stroke motors of the scanner. This thesis is focusing on the DC/DC converter which is non-isolation one in the

block.

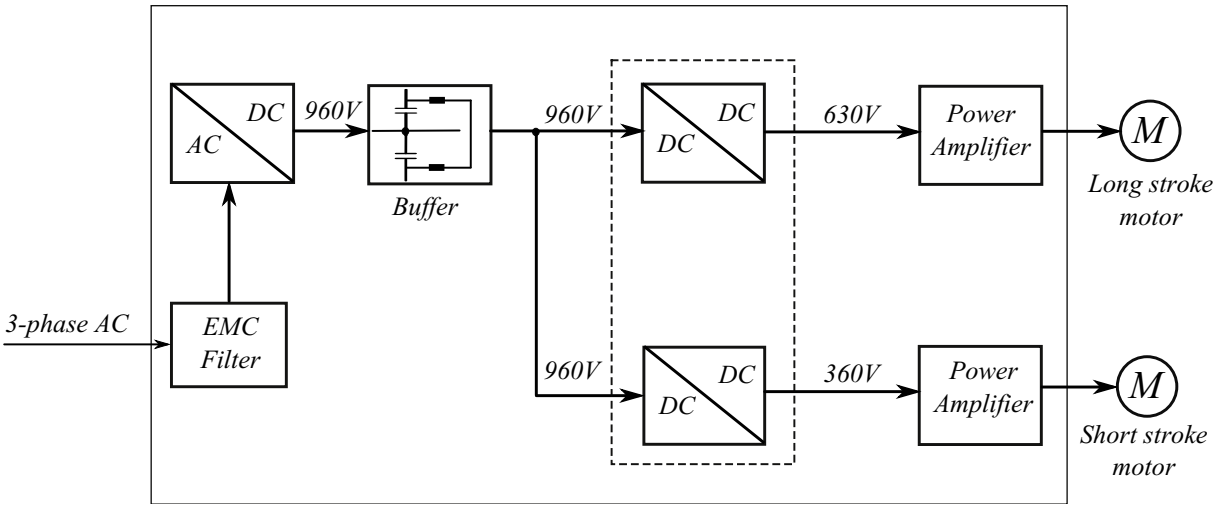


Figure 1.1: Application of the DC/DC converter

1.2. Objectives of this thesis

The thesis is focusing at the $20kW$ DC/DC converter for the application mentioned in the previous section. The specification of this converter is:

- Input voltage: 960V
- Output voltage: 630V and 360V
- Maximum power: 20kW
- Power density: 15kW/L

The content of this thesis is

- To select the most possible topology for this application
- To Determine the optimal modulation scheme
- To have a good modelling of each part of the converter
- To have an optimal design of the converter
- To work on hardware to verify the performance prediction

Due to the application, the DC/DC converter is working in a high dynamic condition, in other word, the transferred power is varying frequently. Therefore, the semiconductor switch power cycle (lifetime) is important to increase reliability and save maintenance cost. Hence, the first goal in the design is a longer semiconductor switch power cycle. Secondly, a higher power density is the second goal in the design. High power density is a general trend. It enables more functionalities within a limited volume, and possibilities to be portable.

1.3. Thesis outline

In Chapter 2, some possible non-isolation DC/DC converter topologies are introduced at first. The advantages and disadvantages of these topologies are described. The most possible topology is selected. Next, The semiconductor technology which is suitable for high power and high frequency application is introduced as well.

In Chapter 3, all the modelling methods used to analyse and design in this thesis are introduced. It first starts with a zero voltage switching method modelling including the principle and the way to ensure the zero voltage switching. An advanced way based on datasheet to estimate losses on semiconductor switches is introduced, including switching losses, conduction losses and gate losses. Furthermore, advanced inductor modelling methods are introduced which are better than conventional methods, including air gap reluctance calculation method, core losses calculation and winding losses calculation method. In the end, the thermal modelling is given.

In Chapter 4, five modulation schemes of the four-switch buck-boost converter are analyzed analytically one by one, typical inductor waveforms are given and the switching sequence of each switch is illustrated. The numerical comparison is given in terms of losses, loss swing and inductor size. According to the analytical and numerical analysis, zero voltage switching modulation has a smallest losses and loss swing. Furthermore, in order to further reduce the loss swing, a new modulation scheme is proposed.

In Chapter 5, an optimal power stage densign is described. It first starts with proposing a two-stage four-switch buck-boost converter in order to reduce the switching losses in a single switch, this structure reduces the voltage across the switch by half. Therefore a GaN switch can be implemented in the two-stage structure. After that, the number of phase is determined by several aspects including the losses in each switch, total inductor volume and output capacitance value. Consequently three phases would be the optimal choice. A mechanical 3D modelling is given. The thermal design according to the recommendation provided by the manufacturer is illustrated. Finally the overall estimation efficiency, temperature swing and power density are given.

In Chapter 6, the control strategy is illustrated. This chapter starts with showing the overall control system block. Afterwards, each part of the control system is explained respectively. The main control strategy is explained at first. It is a current mode control with two feedback loops. The voltage is always controlled to the reference value no matter how the load changes. Because of the two stage structure, a balancing controller is required which can keep the high and low stage operating at a same condition. The duty cycle of each switch is calculated instantaneously by the micro-controller or FPGA, so the equations to calculate the duty cycle are illustrated in this chapter. Next, the way to ensure the zero voltage switching is also explained. It is done by using zero crossing detection. Finally, the simulation result is given.

In Chapter 7, a 48/12 four-switch buck-boost converter is used to verify the proposed low loss swing modulation. The test setup is illustrated at first. It follows with some measure-

ment result. Finally the comparison between the traditional zero voltage switching modulation and proposed zero voltage switching are given.

In Chapter 8, the summarize of the thesis and the conclusion of each chapter are given. Also, there are still many works to be done in terms of this topic, so the outlook and future work are discussed in the end.

2

Literature review

The DC/DC converter is defined as power electronics circuit which converts a DC voltage to another DC voltage with a certain power transfer requirement. More than 10 non-isolation DC/DC converter topologies are developed over the last decades, including buck converter, buck-boost converter, Cuk converter, SEPIC converter. Today, a high power density is a general trend in many application, multiphase and high switching frequency are two solution to reach a high power density. Furthermore, some new semiconductor technologies are also implemented by engineers to reach a high power density. In this chapter, topologies introduced in literature are discussed in section 2.1, the optimal one is selected. The new generation semiconductor switches, wide bandgap devices are briefly introduced in section 2.2.

2.1. High power density non-isolated DC/DC converter

In high power applications, multiphase or interleaved structure is the most common used solution. The interleaved DC/DC converter has inherent advantages[14]:

- The output current ripples can be greatly reduced making the output capacitor much smaller
- When multiphase converter is considered, it is possible to improve the transient responses due to a smaller filter
- Multiphase converters release the current stress on devices

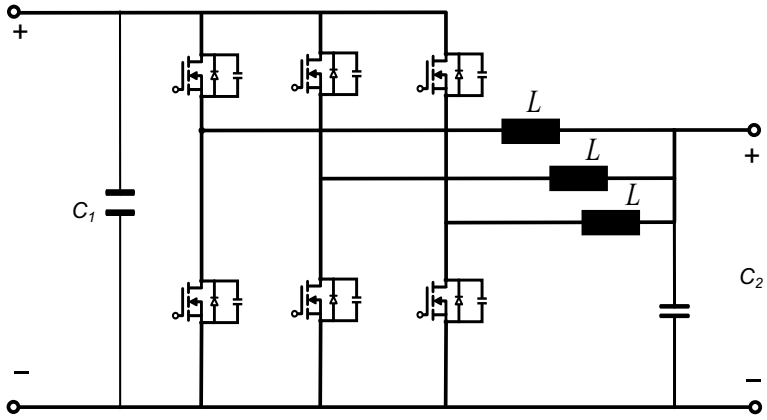


Figure 2.1: Interleaved DC/DC buck/boost converter

Fig.2-1 shows a multiphase DC/DC converter[22], which is a three phases bidirectional DC/DC converter. Each phase in the multiphase converter has a $360/n$ phase shift, where n is the number of phases. Fig. 2-2 shows output voltage ripple cancellation [22]. As shown in Fig. 2-2, it is affected by the number of phases and the duty cycle.

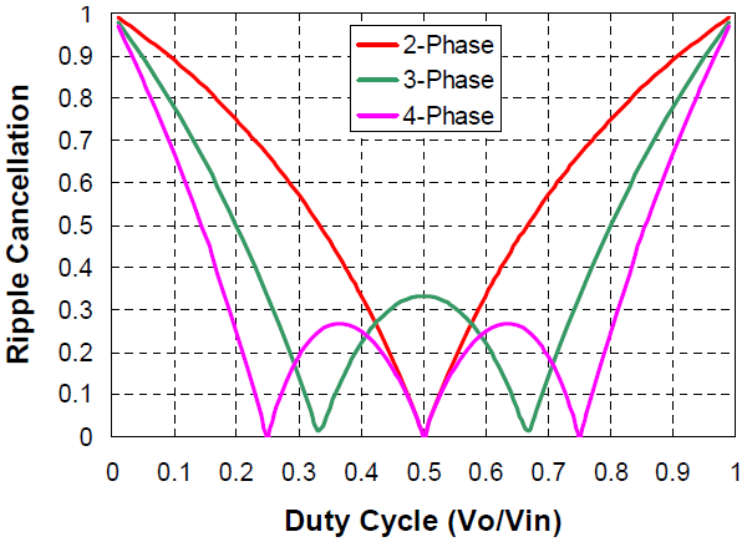


Figure 2.2: Interleaved DCDC converter ripple cancellation

[22]

In [33], a three phases buck converter is implemented with $100kW$ power. A 36-phase interleaved converter is reported in [31], the prototype has a 95% efficiency at full load (1000W). State of the art engineering for multiphase DC/DC converter proposes the use of three to five paralleled buck stages to build the converter [20][8].

For multiphase DC/DC converter, intercell transformers can be implemented to further reduce the volume and increase the power density[5] [6] . As illustrated in Fig. 2-3[6] , three windings share a same core which reduce the inductor volume for a large extent.

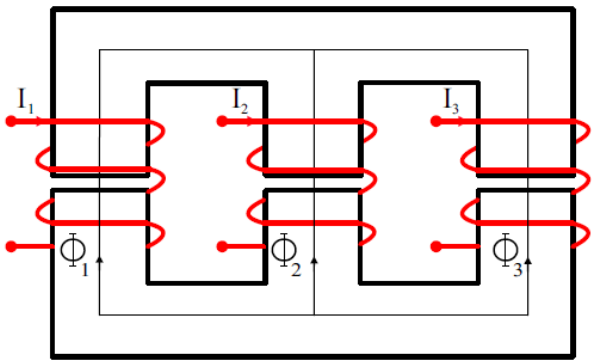


Figure 2.3: Coupled inductor

Apart from the interleaved buck converter, the interleaved buck-boost converter is also proposed in literature[24]. Semiconductor switches suffer from large current stress in this topology, in addition, the polarity is inversed at two sides which makes the control more complicated.

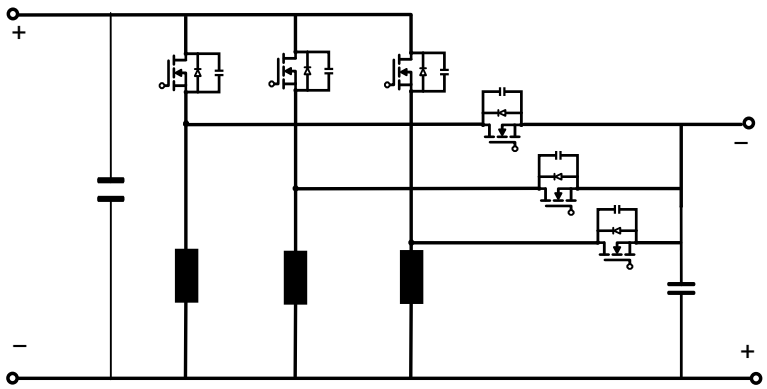


Figure 2.4: Interleaved buck-boost converter

In [1][30][32], a non-inverting four-switch buck-boost converter is discussed, as illustrated in Fig.2-5. The most important advantage of this topology is the flexibility. Taking the $Phasea$ in Fig. 2-5 as an example, several operation modes can be achieved as follows

- Buck mode: Always open S_{a4} and close switch S_{a3}
- Boost mode: Always open S_{a2} and close switch S_{a1}
- Buck-boost mode: Switch S_{a1} & S_{a4} and S_{a2} & S_{a3} diagonally

Therefore, this topology is suitable for many applications.

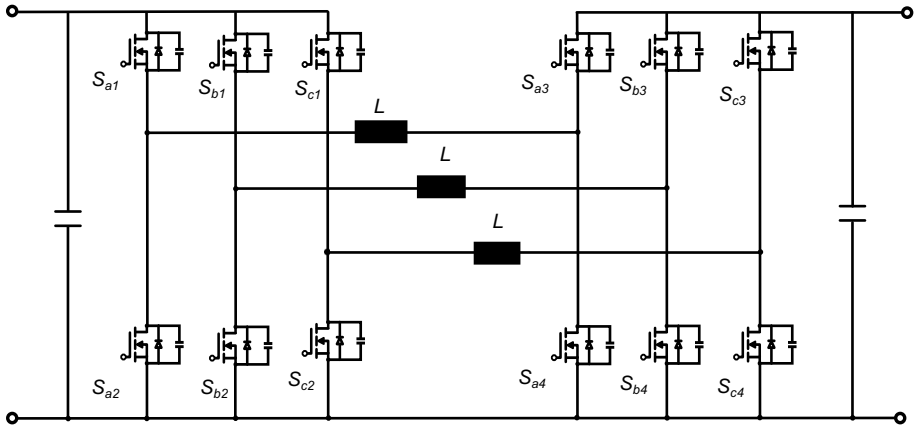
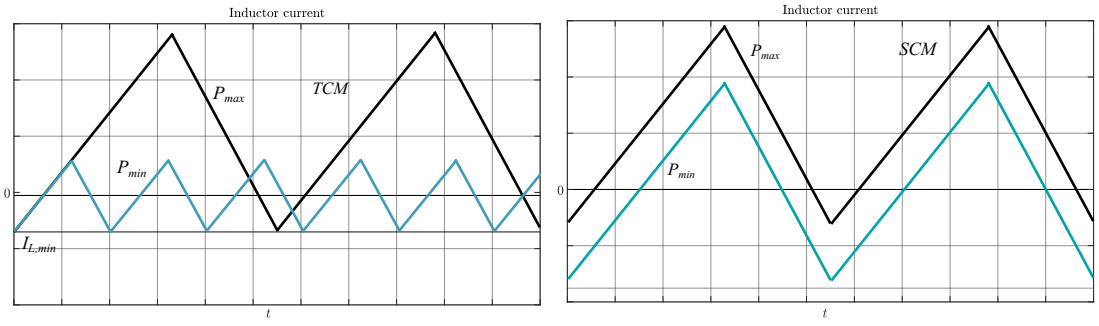


Figure 2.5: Interleaved four-switch buck-boost converter

Among these three topologies illustrated above, for the multiphase buck converter and multiphase buck-boost converter, there are two operation modes Synchronous Conduction Mode (SCM) [23][13] and Triangular Current Mode (TCM) [9][25]. Taking the multiphase buck converter as an example, the inductor waveform of the TCM and SCM are shown in Fig. 2-6 for minimum and maximum output power. In SCM operation, the peak-to-peak inductor current is kept constant and independent of the output power. As a result, the inductor current waveform is pushed up and down for a large extent, and the losses on each device swing a lot. The TCM operation has a better performance, because the minimum inductor current is kept constant $I_{L,min}$. The output power is regulated by changing the frequency. However, the switching frequency will increase significantly when the output power decreased from maximum to minimum. In addition, the frequency variation strongly limited by the time delays in the measurement and control circuit[12].



(a) TCM. (b) SCM.

Figure 2.6: Sychronous Conduction Mode and Triangular Current Mode

As illustrated previously, four-switch buck-boost converter is a very flexible converter which makes more operation modes possible to overcome drawbacks of TCM and SCM. As illustrated in Fig.2-7(a), it shows one of the modulation schemes, and at the end of each cycle there is a free-wheeling interval in which no voltage is applied on the inductor (Switch S_2 and S_4 are switched on), and output power can be regulated by adjusting the length of free-

wheeling interval. As a result, the switching frequency is not increasing while the current waveform is not going up and down.

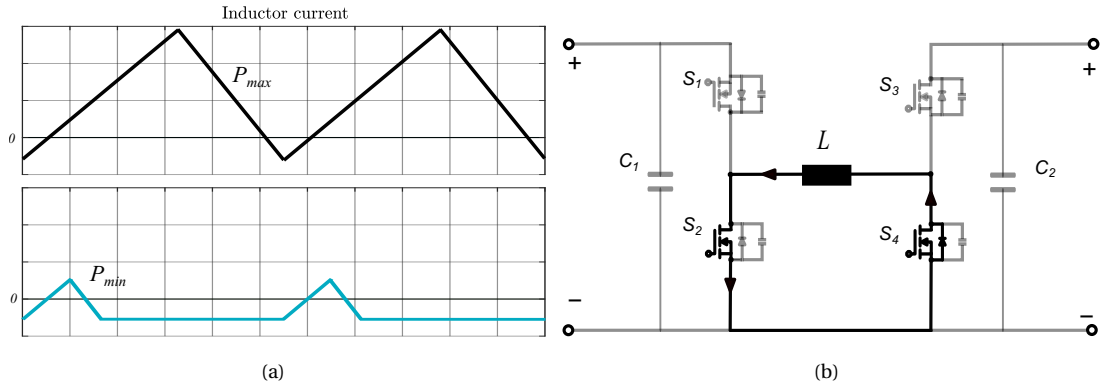


Figure 2.7: To illustrate free-wheeling interval

In conclusion, an interleaved four-switch buck-boost converter would be the optimal topology for the application in this thesis.

2.2. Semiconductor technology

2.2.1. MOSFET & IGBT

There are many kinds of transistors available for switch-mode power supply (SMPS) today. Metal-oxide semiconductor field effect transistor (MOSFET) and insulated-gate bipolar transistor (IGBT) are two most popular devices.

The MOSFET is a three-terminal (Gate, Drain, Source) fully-controlled switch. The gate control signal is applies between the gate and source, and its switch terminals are the drain and source. The gate terminal is made of metal, the other two terminals are made of metal oxide. The IGBT is also a three terminal (Gate, Collector, emitter) fully-controlled switch. The gate signal is applied between the gate and emitter, and its switch terminals are the drain and emitter.These two transistors have their own advantages[10].

MOSFET:

- Higher switching speed.
- Higher dynamic performance.
- Lower gate-to-drain capacitance
- Lower thermal impedance which allows more power dissipation
- Smaller rise and fall time

IGBT:

- Mature production techniques resulting in a lower cost.

- Higher durability to overloads.
- Improved parallel current sharing.
- Smoother turn-on/-off waveforms.
- Lower input capacitance.

2.2.2. SiC & GaN

Si based devices have some important limitations in terms of its voltage blocking capability, operation junction temperature and switching frequency[15]. As a result, a new generation of power semiconductor switches are required. Novel and innovative power devices based on wide bandgap semiconductors are developed to overcome the limitation of Si devices. SiC(Silicon carbide) and GaN(Gallium Nitride) are the two most popular new devices with better performance.

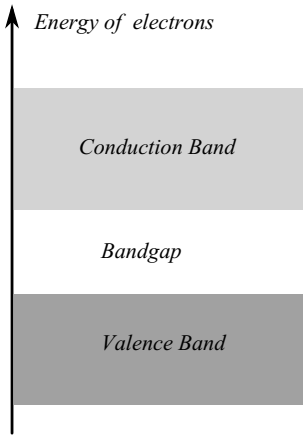


Figure 2.8: Electrons energy band

Material	Bandgap
Si	1.12
GaAs	1.4
3C-SiC	2.3
6H-SiC	2.9
4H-SiC	3.2
GaN	3.39
Diamond	5.6

Figure 2.9: Different materials bandgap

The movement of free electrons is the reason why materials are capable to conduct. In conductor materials, electrons are free to move while in non-conductor materials electrons are fixed by chemical bond. Those electrons fixed by chemical bond are in valence band while free electrons are in conduction band. Bonded electrons need enough energy to jump from valence band to the conduction which in between is called bandgap. Materials like carbon, silicon and phosphorus have strong capability to bond the electrons and low conductivity. For instance, pure silicon and carbon are crystal can not conduct. They are Group 4 element, if Group 5 elements such as phosphorus and arsenic are doped into silicon, there is one more free electrons corresponding to N-type semiconductor. In a same way, if Group 3 elements are doped into silicon, there is one more hole corresponding to P-type semiconductor. Compared to silicon, the capability to bond electrons of carbon is stronger, so more energy is required to break the the chemical bond between silicon and carbon, as a result, the bandgap of SiC is wider than pure Si. The same also applies to GaN, although gallium itself is weaker than silicon, nitrogen is a very strong elements. Because these wide bandgap material needs more energy to be conducted, they are naturally capable to handle a higher

voltage and a higher temperature. As a result, the die of them can be much smaller and also the depletion region. Consequently, smaller parasitic parameters, especially parasitic capacitance and on-resistance is reachable. Because of the smaller parasitic capacitance, it takes less time to charge and discharge, so the switching losses are much smaller and higher switching frequencies are possible. In section 2.3 semiconductor failure power cycle or lifetime is introduced briefly.

2.2.3. Semiconductor switch power cycle (Lifetime)

The temperature of semiconductor switch rises and falls according to the operating conditions as illustrated in Fig. 2-6 and Fig. 2-7(a) (different power level). The interior structure of the semiconductor is exposed to the heat stress caused by the temperature rise and fall and thus suffers fatigue and deterioration. Fig. 2-10 shows the general relation of semiconductor power cycle and temperature.

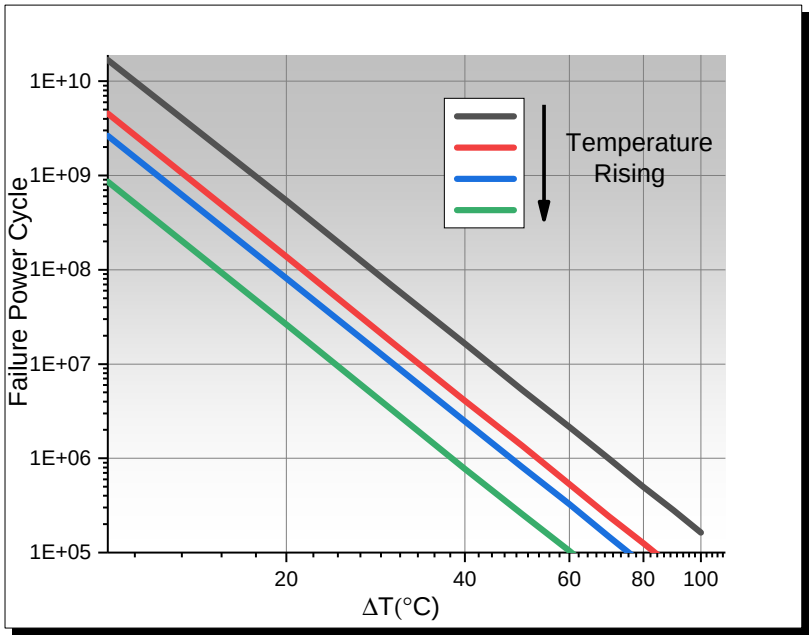


Figure 2.10: Failure of power cycle as a function of temperature and temperature swing

As illustrated, the failure power cycles are inversely proportional to junction temperature swing and maximum junction temperature. In another word, a longer semiconductor lifetime can be obtained by a lower maximum temperature or a smaller temperature swing.

3

Modelling of main component of four-switch buck-boost converter

Based on goals, increasing the lifetime of semiconductor switches and getting a high power density, good models are required to analysis, design and optimize the four-switch buck-boost converter, including semiconductor modelling, inductor modelling and thermal modelling. The performance of converters are mostly dominated by these three aspects. Although filters are required in the input and output side, they are not dominated. Hence in this chapter, the following models are introduced.

- Zero voltage switching modelling
- Semiconductors modelling
- Inductor: Magnetic circuit modelling and loss modelling
- Thermal modelling

3.1. Semiconductors modelling

The zero volatge swithing principle is explained in section 3.1.1. In section 3.1.2 to 3.1.5 an advanced and accurate semiconductor losses estimation model, based on datasheet, is provided including switching losses, conduction losses, gate losses and diode losses.

3.1.1. Zero voltage switching modelling

The maximum temperature is one of the domination of semiconductor device lifetime, smaller maximum temperature leads to longer lifetime. Switching loss is one of the main contribution of temperature rising, and it could be quite large in hard switching operation.

Soft switching can reduce the losses to a large extent, hence, it is worth investigating and implementing.

Fig.3-1 shows a bridge leg which is commonly seen in switched mode power converters. The switch S_1 or S_2 in the bridge can be seen as a combination of three components which are a transistor, a diode and a capacitor. The diode is the body diode of the device or an external diode if the device does not have it internally. Sometimes, even there is a body diode inside the switch, people will use an external one, especially schottky diode, to reduce the diode reverse recovery losses during commutating. The capacitor represents the output capacitor of the device. It is defined as the sum of the gate to drain capacitance and drain to source capacitance, $C_{oss} = C_{DS} + C_{GD}$.

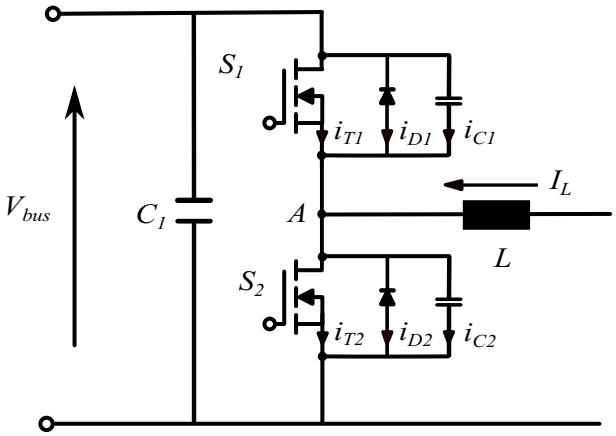


Figure 3.1: A general bridge leg

The zero voltage switching (ZVS) principle can be explained as follows. In Fig. 3-1, assuming the commutating transition is from S_2 to S_1, and the inductor current is flowing from the right side to the left side. The detailed commutation procedures can be illustrated with Fig. 3-2 which shows the current flowing path during each time interval[3].

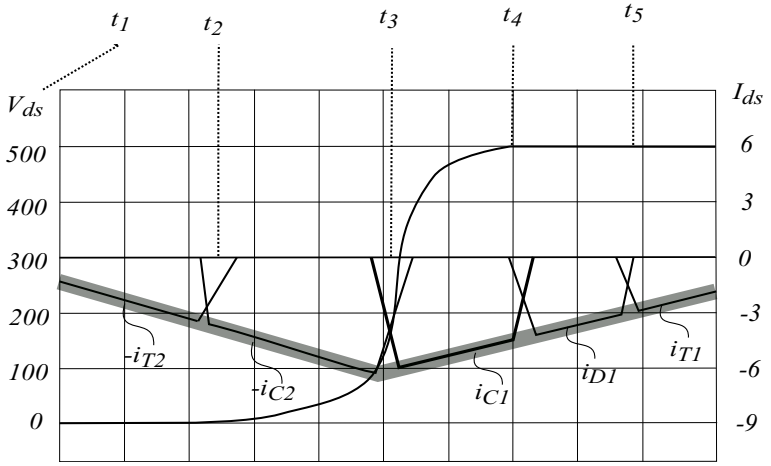


Figure 3.2: Example of ZVS commutation from S_2 to S_1

- $t = t_1$

At time instant t_1, the gate signal of switch S_2 is turned off, the current is flowing in the transistor of switch S_2 at this moment and will keep flowing in the transistor for a short interval before the gate voltage fall below its threshold voltage.

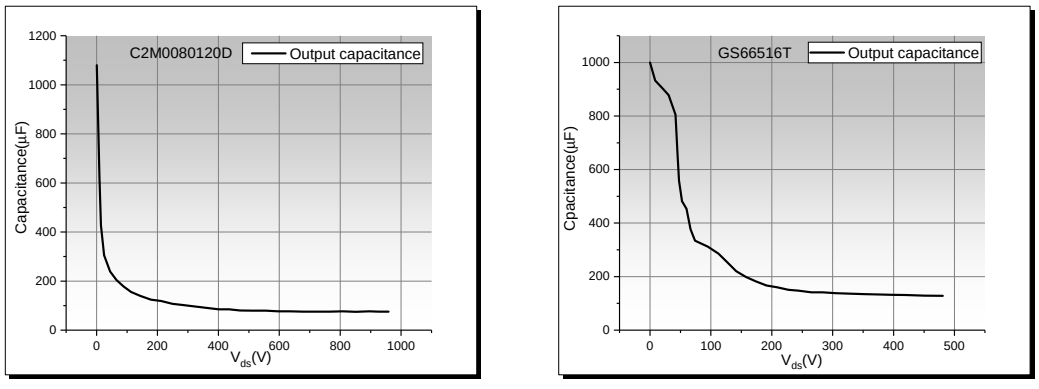
- $t = t_2$
  At time instant t_2, the gate voltage of S_2 reaches its gate threshold voltage, and its channel resistance rises dramatically. Therefore, the current starts to flow on the leg capacitance, mostly on C_2 at this moment. Meanwhile, the leg capacitance ($C_{leg} = C_1 + C_2$) is charged.

- $t = t_3$
  At time instant t_3, the transition happens when C_1 becomes larger than C_2. Starting from this moment, the current is mainly flowing on the capacitance C_1 ,and C_{leg} is further charged.

- $t = t_4$
  At this moment, the drain to source voltage v_{ds2} reaches the bus voltage, and the voltage across the switch S_1 is zero which makes the diode D_1 conducting. Now a positive gate signal can be applied to switch S_1. The current will still flow on the diode D_1 for a short time before it reaches the gate threshold voltage.

- $t = t_5$
  When the gate voltage reaches the threshold voltage, the switch S_1 is switched on under a zero voltage.

The same principle also applies to the commutation from the top switch to the bottom switch. Fig.3-3 shows the output capacitance as a function of drain to source voltage across it, in terms of a SiC MOSFET $C2M0080120D$ manufactured by $Wolfspeed$ [29] and a GaN $GS66516T$ manufactured $GaNSystem$[26]. As shown in Fig. 3-3, when the drain to source voltage is small the capacitance is large and vice versa. Hence, during the commutation explained above, the current is mainly flowing on the C_2 at first and then going to the C_1.



(a) C2M0080120D.

(b) GS66516T.

Figure 3.3: Output capacitance as function of drain to source voltage

In order to ensure a zero voltage switching, enough charges should be provided to charge the leg capacitance $C_{leg} = C_1 + C_2$. In other words, a large enough offset current I_0 at commutation instant is required. The current I_0 can be calculated by the following steps, given by[11]

- `step 1`
  The first step is to determine how many charges are needed for a certain switch. It can be derived by

$$Q_1 = \int_0^{V_{bus}} C_{oss}(v)\,dv \tag{3.1}$$

  Meanwhile, parasitic capacitance existing of the PCB should be taken into consideration, which is around $200nF \sim 500nF$. Therefore, the total charge required is

$$Q_{req} = N \cdot Q_1 + Q_{PCB} \tag{3.2}$$

  where N is the number of switches on the bridge in total.

- `step 2`
  The charge provided by the current, as illustrated by Fig. 3-4, is calculated by

$$Q_2 = \int_{t_2}^{t_4} i_L(t)\,dt = \int_{t_2}^{t_3} [I_0 + \frac{V_{L1}}{L}(t - t_3)]\,dt + \int_{t_3}^{t_4} [I_0 + \frac{V_{L2}}{L}(t - t_3)]\,dt \tag{3.3}$$

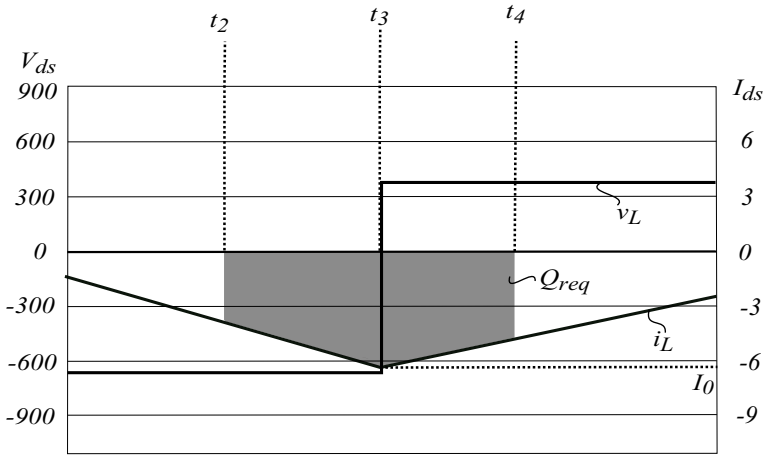


Figure 3.4: Required charge for ZVS

- `step 3`
  It is very hard to determine the time interval length $t_2 \sim t_3$, and $t_3 \sim t_4$, but the dead time from t_1 to t_5 is fixed. Therefore we can use the dead time t_{dead} to calculated Q_2 and make a certain compensation.

- `step 4`
  The relationship $Q_2 \geq Q_{req}$ should be fulfilled. By solving the inequation, a minimum current I_0 which ensure the zero voltage switching can is obtained.

However, although zero voltage switching can be obtained, there is still switching off losses caused by the overlap of drain to source voltage and transistor current as illustrated in next section Fig. 3-6. The switching off losses could be quite large when the switched off at a high current or a high voltage. In order to reduce the switching off losses, an external capacitance can be connected in parallel, as illustrated in Fig.3-5, to slow down the rising of drain to source voltage.

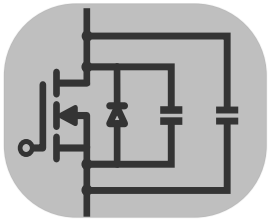


Figure 3.5: MOSFET with external capacitance

3.1.2. Switching losses

As mentioned in the previous chapter, there are several modulation schemes for the selected topology, and hard switching happens to some of them discussed in Chapter 4. In addition, the zero voltage switching discussed in last section also has turn-off losses. Hence, it is important to have a detailed modelling of switching losses and conduction losses.

The ideal semiconductor switch has the following characteristics:[16]

- Block arbitrarily large forward and reverse voltages with zero current flowing when it is off.
- Conduct large currents with a small voltage drop when it is on.
- Switch transistion happens instantaneously when gate signal changes.

However, obviously real devices is not ideal, they do not have these ideal characteristics and always have power dissipation in real application. If the power dissipation is too high, the device temperature will exceed the limitation and will not only destroy themselves but also damage other components in the system. Hence, power dissipation of semiconductors should be analysed.

Fig. 3-6 illustrates the typically drain-source voltage and current waveform during switching transition (switch-on and switch off).

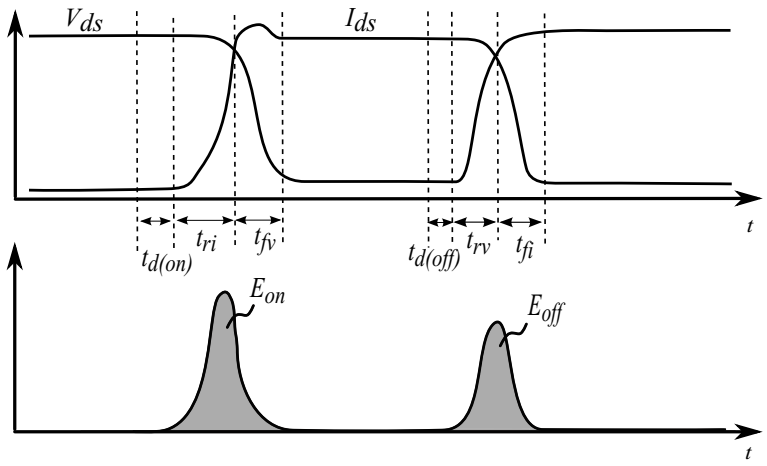


Figure 3.6: Generic-switch switching characteristics

When the switch is open, it can be turned on by applying a positive signal to switch gate, as illustrated in Fig.3-6. During the turn-on transition, the current is built up after a short delay time $t_{d_{on}}$ and a rise time t_{ri}. Just after the current I_d flows entirely through the transistor, the diode can become reverse biased and the switch voltage fall to a small on-state value in a voltage fall time t_{fv}. The waveform in Fig. 3-6 shows that large values of switch voltage and current are present simultaneously during switch-on interval. The energy dissipation in the device during switch-on can be approximated by

$$E_{on} = \frac{1}{2} V_{ds} I_d (t_{fv} + t_{ri}) \tag{3.4}$$

When the device has to be switched-off, the positive signal is removed from the gate terminal of the switch. During the turn-off transition, the voltage is built up after a short turn-off delay time $t_{d_{off}}$ and a voltage rise time t_{rv}. The current in the switch falls to zero with a current fall time t_{fi}, and large values of voltage and current occur simultaneously during the transition. The switching energy losses during this transition can be calculated by

$$E_{off} = \frac{1}{2} V_{ds} I_d (t_{rv} + t_{fi}) \tag{3.5}$$

The average switching power dissipation can be calculated by

$$P_s = \frac{1}{2} \times f_s \times (E_{on} + E_{off}) \tag{3.6}$$

where f_s is the switching frequency.

However, the approach discussed above is an ideal way which has a large gap with reality switching performance. The real switch performance is highly dependent with gate driver, gate resistor value, junction temperature and parasitic parameters as illustrated in Eq. 3-7

$$
\begin{aligned}
P_{sw}(I_{on}, I_{off}, V_{on}, V_{off}, T_j, V_{gate,on}, V_{gate,off}, R_{gate,on}, R_{gate,off}) = \\
\frac{1}{T}\sum_{i=1}^{N_{sw,on}} E_{on}(I_{on,i}, V_{on,i}, T_j, V_{gate,on}, R_{gate,on}) + \\
\frac{1}{T}\sum_{i=1}^{N_{sw,\,\mathrm{off}}} E_{\mathrm{off}}\left(I_{\mathrm{off}\,i}, V_{\mathrm{off},i}, T_j, V_{\mathrm{gate,\,off}}, R_{\mathrm{gate,\,off}}\right)
\end{aligned}
\tag{3.7}
$$

Where:
- $N_{sw,on}$ and $N_{sw,off}$ are the number of turn-on and turn-off switching transitions within a pulse period T.
- E_{on} and E_{off} are the turn-on and turn-off switching losses energies with a function of the current and voltage at the switching instant, also corresponding to junction temperature T_j, gate voltages $V_{gate,on}$ and $V_{gate,off}$ and the gate resistances $R_{gate,on}$ and $R_{gate,off}$.

It can be modelled by the following approach. Fig. 3-8 shows the switching energy of $C2M0080120D$ as a function of drain to source current, as a function of junction temperature and as a function of gate resistor at a certain drain source voltage and a certain gate voltage given in the datasheet. These curves can be approximated by second order equations ($Eq.3-8 \sim Eq.3-10$), which are also illustrated in Fig. 3-8. However, most manufacturers do not give the switching energy data as a function of drain to source voltage and gate drive voltage V_{GS} continuously, but just few points are given. In this case, for drain to source voltage, a proportional approximation can be used.

$$
E(T_j)|_{R_{gate,ref}, V_{gs,ref}, I_{ds,ref}} = a_0 + a_1 T_j + a_2 T_j^2 \tag{3.8}
$$

$$
E(I_{ds})|_{T_{j,ref}, V_{gs,ref}, R_{gate,ref}} = b_0 + b_1 I_{ds} + b_2 I_{ds}^2 \tag{3.9}
$$

$$
E(R_g)|_{T_{j,ref}, V_{gs,ref}, I_{ds,ref}} = c_0 + c_1 R_g + c_2 R_g^2 \tag{3.10}
$$

It is worth noting that an offset should be compensated to the switching-off energy. The reason is explained as follows. Fig. 3-7 illustrates a switch including the body diode and output capacitance. Manufacturer measures the switching energy by measuring the drain to source voltage V_{ds} and the drain to source current I_{ds} (It is not able to measure the transistor current I_T directly). However, the switching losses only occur on the transistor of the switch, therefore, the switching energy given in the datasheet contains the energy storing in output capacitance. Hence, an offset needs to be compensated.

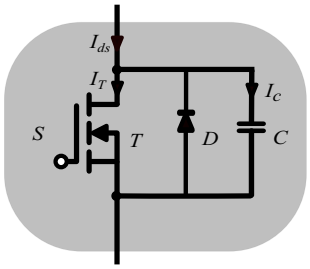
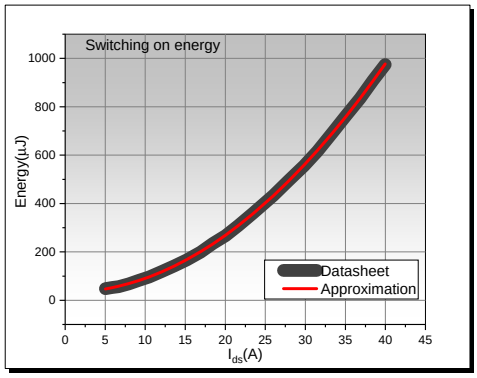
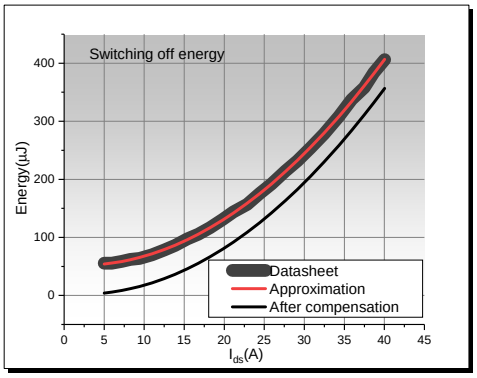


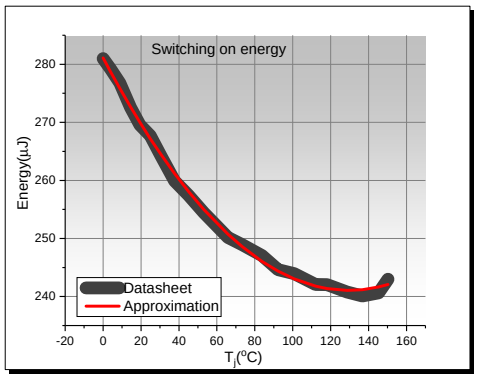
Figure 3.7: MOSFET equivalent circuit



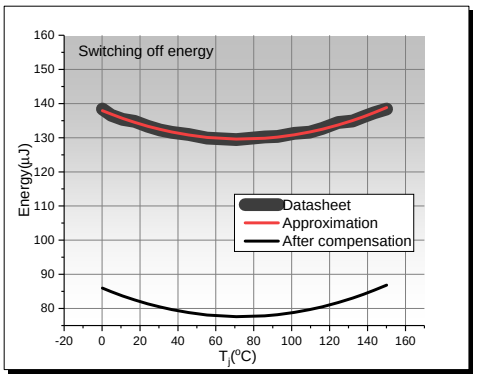
(a) Switching on energy as funcion of I_{ds}.



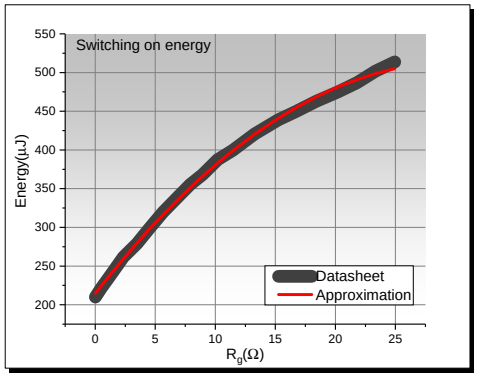
(b) Switching off energy as funcion of I_{ds}.



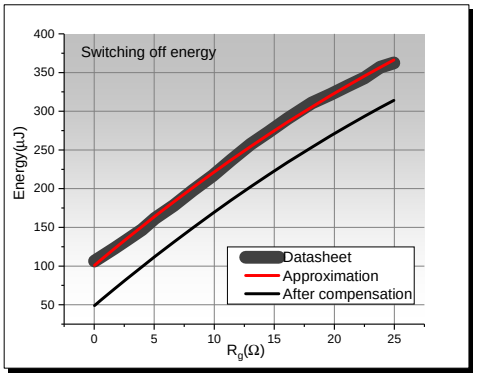
(c) Switching on energy as funcion of T_j.



(d) Switching off energy as funcion of T_j.



(e) Switching on energy as funcion of R_g.



(f) Switching off energy as funcion of R_g.

Figure 3.8: The switching energy from datasheet and approximation (a) Switching on energy as funcion of I_{ds}. (b) Switching off energy as funcion of I_{ds}. (c) Switching on energy

The coefficients $a_0, a_1, a_2,\ b_0, b_1, b_2,$ and c_0, c_1, c_2 in Eq. 3-8, Eq. 3-9 and Eq. 3-10 can be derived by MATLAB function $polyfit$. The coefficient are given in Table. 3-1. A generalized function is derived by combining Eq. 3-8, Eq. 3-9 and Eq. 3-10 together, which is given by

$$\begin{aligned} E_{sw} =& E_{sw,ref}|_{T_\mathrm{J}=T_{\mathrm{J,ref}}, I_\mathrm{ds}=I_{\mathrm{ds,ref}}, V_\mathrm{GS}=V_{\mathrm{GS,ref}}} \\ & \cdot(1+\alpha_1\Delta T_\mathrm{J}+\alpha_2\Delta T_\mathrm{J}^2)(1+\beta_1\Delta I_\mathrm{D}+\beta_2\Delta I_\mathrm{D}^2)(1+\gamma_1\Delta R_g+\gamma_2\Delta R_g^2) \end{aligned} \tag{3.11}$$

$I_{ds}=20A, V_{ds}=800V, R_g=2.5\Omega$			$V_{ds}=800V, T_j=25°, R_g=2.5\Omega$			$T_j=25°, I_{ds}=20A, V_{ds}=800V$		
Switching on energy approximation coefficients								
a_0	a_1	a_2	b_0	b_1	b_2	c_0	c_1	c_2
281.0878	-0.618	0.0024	31.6567	-0.0029	0.5921	214.5801	19.8994	-0.3310
Switching off energy approximation coefficients								
a_0	a_1	a_2	b_0	b_1	b_2	c_0	c_1	c_2
137.9872	-0.2292	0.0016	52.7374	-0.96	0.2449	100.59	13.0836	-0.0979

Table 3.1: Switching energy approximation coefficient

$I_{ds}=20A, V_{ds}=800V,\ R_g=2.5\Omega, T_j=25°C$					
Switching on energy approximation coefficients $E_{ref}=262.3\mu J$					
α_1	α_2	β_1	β_2	γ_1	γ_2
-1.859e-3	8.959e-6	8.940e-2	2.210e-3	6.810e-2	-1.236e-3
Switching off energy approximation coefficients $E_{ref}=132.7\mu J$					
α_1	α_2	β_1	β_2	γ_1	γ_2
-1.8462e-3	1.9811e-5	0.1094	3.0323e-3	0.1559	-1.2122e-3

Table 3.2: Switching energy approximation coefficient

Table. 3-3 given the parameters for switch selected in Chapter 5 ($GS66516T$). The manufacturer gives the switching on energy as a function of drain to source voltage v_{DS}, drain to source current I_{DS} and junction temperature T_j, the switching off energy as a function of v_{DS} and I_{DS}. Hence, the equations are given as

$$\begin{aligned} E_{swon} =& E_{sw,ref}|_{V_\mathrm{ds}=V_{\mathrm{ds,ref}}, I_\mathrm{ds}=I_{\mathrm{ds,ref}}, T_\mathrm{J}=V_{\mathrm{T_j,ref}}} \\ & \cdot(1+\alpha_1\Delta I_{ds}+\alpha_2\Delta I_{ds}^2)(1+\beta_1\Delta V_\mathrm{ds}+\beta_2\Delta V_\mathrm{ds}^2)(1+\gamma_1\Delta T_j+\gamma_2\Delta T_j^2) \end{aligned} \tag{3.12}$$

$$\begin{aligned} E_{swoff} =& E_{sw,ref}|_{V_\mathrm{ds}=V_{\mathrm{ds,ref}}, I_\mathrm{ds}=I_{\mathrm{ds,ref}}} \\ & \cdot(1+\alpha_1\Delta I_{ds}+\alpha_2\Delta I_{ds}^2)(1+\beta_1\Delta V_\mathrm{ds}+\beta_2\Delta V_\mathrm{ds}^2) \end{aligned} \tag{3.13}$$

$I_{ds} = 20A, V_{ds} = 200V$, $R_{gon} = 10\Omega$, $R_{goff} = 1\Omega$ $T_j = 25°C$					
Switching on energy approximation coefficients $E_{ref} = 48.9\mu J$					
α_1	α_2	β_1	β_2	γ_1	γ_2
3.45e-2	1.9866e-4	21.03	5.26e-2	0.2624	-5.59e-6
Switching off energy approximation coefficients $E_{ref} = 4.52\mu J$					
α_1	α_2	β_1	β_2		
5.834e-2	1.32e-3	5.7e-3	3.87e-6		

Table 3.3: Switching energy approximation coefficient

It should be noted that the switching energy data given by the datasheet is measured under hard switching on and hard switching off condition. If zero voltage switching off happens, in other words the current goes from source to drain during the transition, the losses only occur on the body diode, and it is extremely low. The way to calculate the losses is illustrated in Section 3.1.5.

As mentioned in the last section, even in zero voltage switch condition, there is still switching off losses, and an external capacitor can help reduce it. If an external capacitance is connected, the switching off losses can be approximated as follows. Fig.3-9 shows the simplified equivalent circuit of MOSFET during switching off.

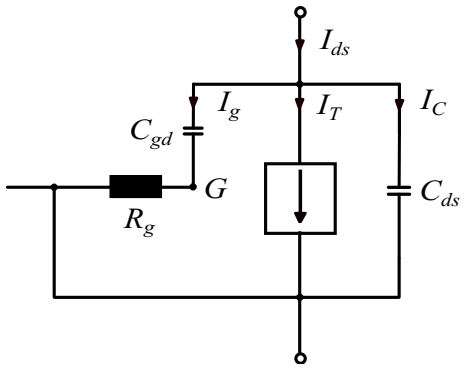


Figure 3.9: Equivalent circuit of MOSFET during switching off

At the beginning of switching off, the drain to source current is divided to I_g, I_T and I_C as illustrated in Fig. 3-9. According to the equivalent circuit, the following equation can be derived.

$$\frac{dV_{ds}}{dt} = \frac{I_C}{C_{ds}} = \frac{I_g}{C_{gd}} \tag{3.14}$$

Assuming the $I_g = V_{th} / R_g$, and the time required to charge the C_{gd} can be calculated by

$$t = \frac{\int_0^{V_{ds}} C_{gd} dV_{ds}}{I_g} \tag{3.15}$$

If the drain to source capacitance is larger, with the same charge time, the drain to source voltage is smaller, as a result, the switching off losses is lower.

3.1.3. Conduction losses

The other major contribution to the power loss in switches is the average power dissipated during the on-state P_{on} which is proportional to the drain to source on-resistance R_{ds} and to the squared RMS value of the current flowing on the switch. Assuming the junction temperature changing of MOSFET is negligible during every single cycle, the equivalent conduction losses can be calculated by:

$$P_{con} = R_{\mathrm{DS(on)}} \cdot I_{\mathrm{rms}}^2 \tag{3.16}$$

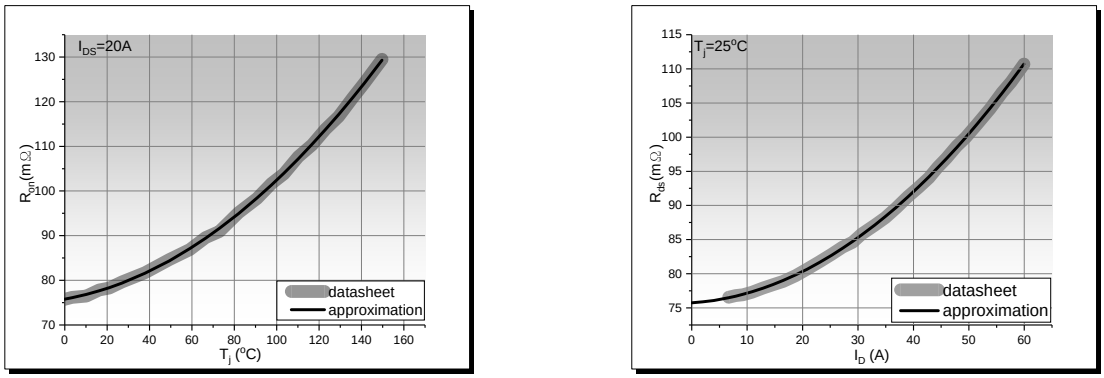
where I_{rms} is determined by

$$I_{\mathrm{rms}} = \sqrt{\frac{1}{T_{\mathrm{L}}} \int_0^{T_{\mathrm{L}}} I_{\mathrm{S}}(t)\mathrm{d}t} \tag{3.17}$$

The drain to source on-resistance R_{on} is dependent on the junction temperature and on the drain to source current. It can be modelled by the following approach[3]. Fig. 3-10 shows the drain source on-resistance as a function of drain-source (Fig. 3-10 (a))current and as a function of junction temperature (Fig. 3-10(b)). The on-resistance curve can be approximated by a 2^{nd} order function,

$$R_{DS_{on}}(T_j)|_{I_{ds,ref},V_{gs,ref}} = a_0 + a_1 T_j + a_2 T_j^2 \tag{3.18}$$

$$R_{DS_{on}}(I_{ds})|_{T_{j,ref},V_{gs,ref}} = b_0 + b_1 I_{ds} + b_2 I_{ds}^2 \tag{3.19}$$



(a) On-resistance as a fucntion of T_j

(b) On-resistance as a fucntion of I_{ds}

Figure 3.10: On resistance as function of channel current and the junction temperature

The coefficients a_0, a_1, a_2 and b_0, b_1, b_2 in Eq.3-18 and Eq.3-19 can be derived by MATLAB function $polyfit$. Take the silicon carbide MOSFET $C2M0080120D$ as an example, the coefficients are given in Table. 3-4. A generalized function is derived by combining Eq.3-18 and Eq. 3-19 together, which is given by

$$\begin{aligned} R_{\mathrm{DS(on)}} = \Big[& R_{\mathrm{DS(on)}}\big|_{T_\mathrm{J}=T_{\mathrm{J,ref}}, I_\mathrm{D}=I_{\mathrm{D,ref}}, V_{\mathrm{GS(on)}}=V_{\mathrm{GS(on),ref}}} \\ & \cdot \left(1+\alpha_1 \Delta T_\mathrm{J} + \alpha_2 \Delta T_\mathrm{J}^2\right) \cdot \left(1+\beta_1 \Delta I_\mathrm{D} + \beta_2 \Delta I_\mathrm{D}^2\right)\Big] \end{aligned} \tag{3.20}$$

Where:
- ΔT_j is the deviation between junction temperature and reference junction temperature $\Delta T_j = T_j - T_{j,ref}$
- ΔI_D is the deviation between drain source current and reference drain source current $\Delta I_D = I_D - I_{D,ref}$

$T_j = 25, V_{gs} = 20V$			$I_{DS} = 20A, V_{gs} = 20V$		
a_0	a_1	a_2	b_0	b_1	b_2
75.7399	0.0527	0.0089	75.7985	0.0839	0.0018
$R_{ref} = 80m\Omega$					
α_1	α_2	β_1	β_2	$T_{j,ref}$	$I_{DS,ref}$
6.221e-3	1.113e-4	1.949e-3	2.25e-5	$25°C$	20 A

Table 3.4: On-resistance approximation coefficient $C2M0080120D$

For the switch selected in Chapter 5(GS66516T), parameters are given in Table. 3-5.

GS66516T $R_{ref} = 25m\Omega$		$I_{DS} = 18A, V_{gs} = 6V\, T_j = 25$	
α_1	α_2	β_1	β_2
-5.03e-3	6.9e-5	7.8e-3	2.70e-5

Table 3.5: On-resistance approximation coefficient of $GS66516T$

Hence, a more accurate on state drain to source resistance $R_{ds,on}$ is derived.

3.1.4. Gate Drive Losses

Gate drive losses is a power loss ascribed to device gate charging. It depends on the gate electric charge (or the gate capacity) of the semiconductor device. The gate charge loss can be calculated by

$$P_G = \left(Q_g\right) \times V_{gs} \times f_s \tag{3.21}$$

where Q_g is device gate electric charge, V_{gs} is gate drive voltage, f_s is the switching frequency.

3.1.5. Diode losses

As discussed in the previous section, there is a body diode in MOSFET or external diode anti-parallel contacted with the device. During the transition, especially in ZVS (Zero-Voltage-Switching) condition, the diode will conduct the current for a short time in which power dissipation is existing. This power dissipation can be calculated by

$$P_{diode} = \int_0^t I(t) V_F dt f_s \tag{3.22}$$

where V_F is the forward voltage of the body diode, $I(t)$ is the current flowing on the diode. It should be noted that the forward voltage V_F is dependent by junction temperature and current, but it just conducts for a short time, so it can be negligible.

3.2. Inductor modelling

3.2.1. Magnetic reluctance model

An inductor is a passive two-terminal electrical component stores energy in a magnetic field when current flows through it. Especially in switched converters, inductors are key components. The inductor is also one of the components which contributes to the volume and losses largely.

The inductance value L is defined as[16]

$$L = \frac{N\phi}{i} \quad \text{or} \quad N\phi = Li \tag{3.23}$$

where N is the number of turns, i is the current flowing on the inductor, and ϕ is the magnetic flux crossing a certain area, which can be obtained by the surface integral of the $B-field$ or the flux density representing the density of flux lines per unit area, the unit is weber per square meters $\mathrm{Wb/m^2}$ or tesla (T).

$$\phi = \iint_A B dA \tag{3.24}$$

On the other hand, the flux density can also be defined as

$$B = \mu_r \mu_0 H \tag{3.25}$$

The magnetic reluctance can be defined as

$$R = \frac{l}{\mu_0 \mu_r A} \tag{3.26}$$

and another relation can be obtained by Ampere's law

$$\phi R = Ni \tag{3.27}$$

With Eq. 3.21 and Eq. 3.25, the required winding turn is :

$$L = \frac{N^2}{R_{tot}} \rightarrow N = \sqrt{L \cdot R_{tot}} \tag{3.28}$$

The peak flux density can be derived as :

$$R = \frac{F}{\Phi} = \frac{N \cdot I}{B \cdot A_e} \rightarrow B_{pk} = \frac{N \cdot I_{pk}}{R \cdot A_e} \tag{3.29}$$

Where :
- I_{pk} is the peak current through the inductor.

With the theory above, we can analyze the magnetic inductor, the magnetic circuit can be transferred to electrical circuit by analogy. Fig. 3-11 shows a typical E-core inductor and Fig. 3-12 shows its electrical analog, which helps to analyse the magnetic characteristic[16]. With this method, an accurate reluctance calculation is required.

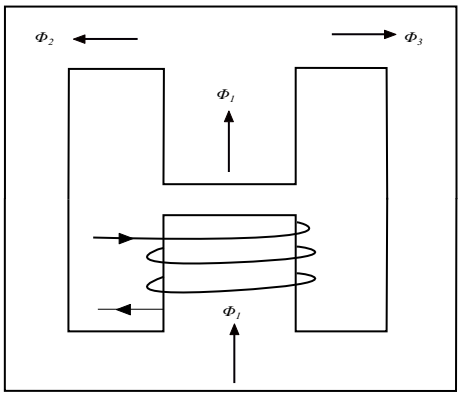


Figure 3.11: Example of Appere's law in the case of winding on a magnetic core with an airgap

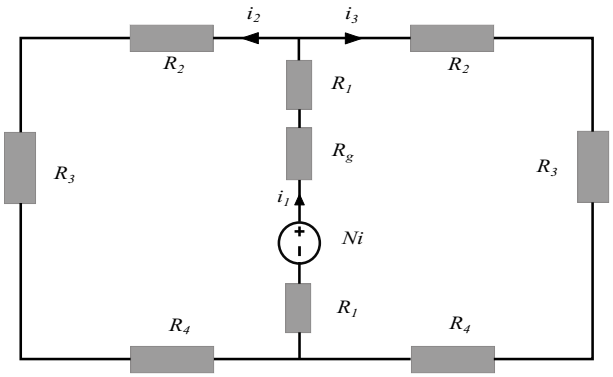


Figure 3.12: Magnetic electrical analog

The reluctance of within the ferrite core, shown in Fig. 3-12 is expressed as :

$$\mathrm{R_{fe}} = \frac{\mathrm{l_e}}{\mu_0 \mu_{\mathrm{fe}} \mathrm{A_e}} \tag{3.30}$$

Where:
- l_e is the effective magnetic path length.
- A_e is the effective core cross section .

The flux in the air gap called fringing flux tends to have a larger cross section area. Relative permeability of air gap is $\mu_r \approx 1$ whereas for the core material is usually much greater $\mu_r >> 1$. The magnetic flux is forced to flow through the gap which represents significantly greater reluctance than a comparable length of the core.

As a result, the fringing effect lowers reluctance of the magnetic path and thus increases inductance of the winding made on such a gapped magnetic core. The traditional air gap reluctance is given by [16] but no explanation is given, as illustrated in Eq. 3-31

$$R_{\mathrm{g}} = \frac{l_{\mathrm{g}}}{\mu_0 \left(a + l_{\mathrm{g}}\right)\left(b + l_{\mathrm{g}}\right)} \tag{3.31}$$

Where:
- l_g is the air gap length.
- a and b are cross section dimension of the airgap.

An advanced approach for air gap reluctance calculation is used in this thesis which is proposed by [17] . This approach has the following advantages:

- The three-dimensionality has been taken into consideration
- It is easy to handle.
- It is capable to calculate the reluctance of different air gap shapes.
- It has a high accuracy

Fig. 3-13 is the most basic air gap geometry which is used as a basis. The reluctance of the basis is determined by which is given by [17]

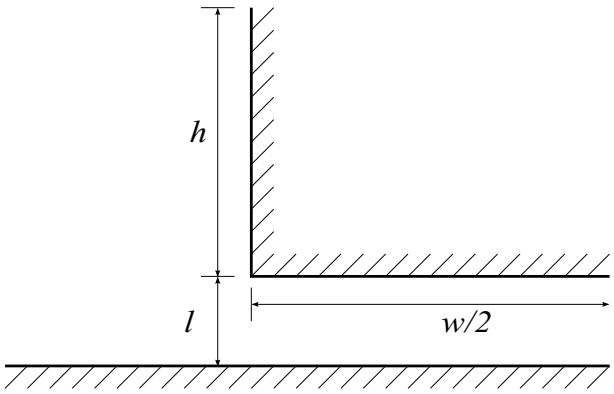


Figure 3.13: Basic geometry for air gap calculation

$$R'_{\text{basic}} = \frac{1}{\mu_0 \left[\frac{w}{2l} + \frac{2}{\pi} \left(1 + \ln \frac{\pi h}{4l} \right) \right]} \tag{3.32}$$

where parameters w, h and l are as illustrated in Fig. 3-13 .

Normally, there are three kinds of air gap geometries, Fig. 3-14 shows the most typical central core air gap for E-shape and ELP-shape core in 2D. This geometry can be seen as the assembling of the basis geometry in Fig. 3-13. The equivalence is illustrated in Fig. 3-14.

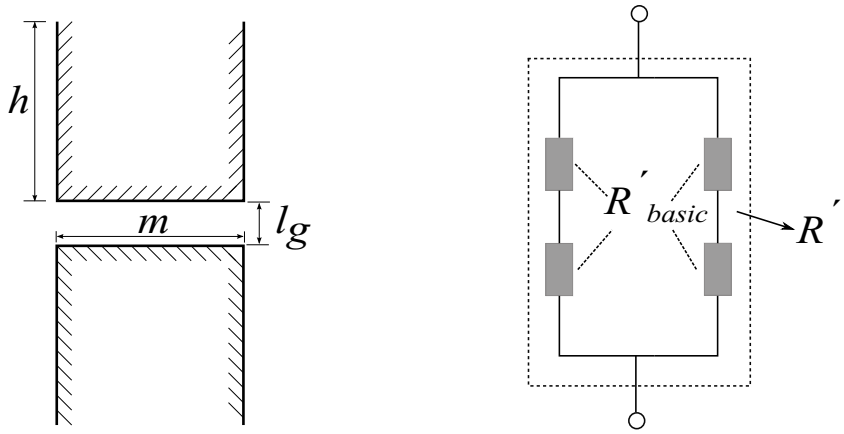


Figure 3.14: A typical geometry of air gap

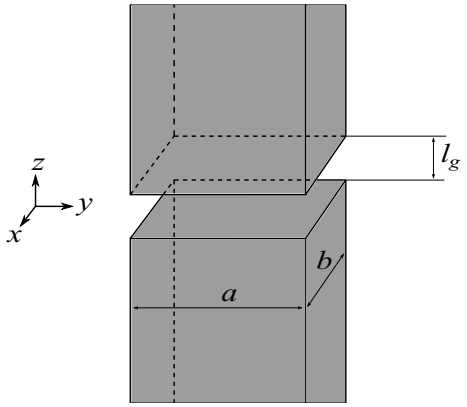


Figure 3.15: 3D airgap

A fringing factor is introduced which is used to describe the reluctance decreases in the air gap. Taking Fig. 3-15 as the example to explain. In order to consider the three dimensionality, the fringing factor of xz-plane and yz-plane are both considered. In xz-plane, assuming the air gap length b is infinitely long, and the air gap boundary in the y-direction is neglected. The fringing factor in this plane is determined by using air gap reluctance R'_{xz} divided by 2D reluctance without fringing effects

$$\sigma_x = \frac{R'_{\mathrm{xz}}}{\frac{l_g}{\mu_0 b}} \tag{3.33}$$

In yz-plane, assuming the air gap length a is infinite, the air gap boundary in x-direction is neglected. The fringing factor in this plane is determined by using air gap reluctance R'_{xz} divided by 2D reluctance without fringing effects

$$\sigma_y = \frac{R'_{\mathrm{yz}}}{\frac{l_g}{\mu_0 a}} \tag{3.34}$$

With these two 2D fringing factors, the 3D fringing factor can be determined. Fig. 3-16 shows the procedures step by step. The first step, the idealized air gap reluctance without fringing effect is multiplied by xz-plane fringing factor σ_x , which is equivalent to the air gap cross-section area is multiplied by $1/\sigma_x$. The mid of Fig. 3-16, a new cross section area $A_{g,x}$ which describe the cross section increase resulting from the fringing effect in xz-plane. Secondly, the new cross section area $A_{g,x}$ section area is multiplied by $1/\sigma_y$ resulting the final cross section area $A_{g,xy}$ in which xz-plane and yz-plane are both taken into account as shown in Fig. 3-16 right side. Hence, the final fringing factor which considers the three-dimensionality is given by

$$\sigma = \sigma_x \sigma_y \tag{3.35}$$

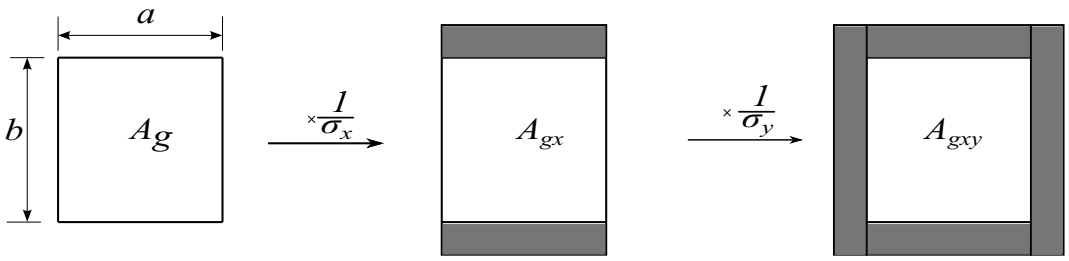


Figure 3.16: The derivation of 3D fringing factor

With the 3D fringing factor given above, the air gap reluctance is calculated by

$$R_{\mathrm{m,\ airgap}} = \sigma \frac{l_g}{\mu_0 \cdot a \cdot b} \tag{3.36}$$

This reluctance calculation approach has higher accuracy compared to the conventional approach, especially for a large air gap condition[17].

Hence, the total reluctance is the sum of Eq-3.30 and Eq-3.36

$$R_{tot} = \mathrm{R_{fe}} + R_{air} = \frac{\mathrm{l_e}}{\mu_0 \mu_{\mathrm{fe}} \mathrm{A_e}} + \sigma \frac{l_g}{\mu_0 \cdot a \cdot b} \tag{3.37}$$

For a round cross-section core illustrated in Fig.3-17, the fringing factor is calculated by

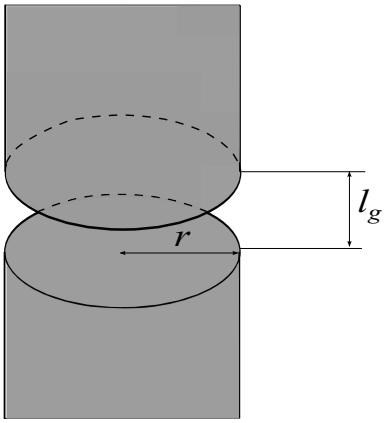


Figure 3.17: Round core air gap

$$\sigma_r = \frac{R'}{\frac{a}{\mu_0 r}} \tag{3.38}$$

Where:
- l_g is the air gap length.
- r is the radius of the round core.
- R' is the 2D air gap reluctance of half of the core leg.

The reluctance of a round core is calculated by

$$R_g = \sigma_r^2 \frac{l_g}{\mu_0 r^2 \pi} \tag{3.39}$$

3.2.2. Inductor core losses

There are three physical core loss mechanisms basically: a) hysteresis losses, b) eddy current losses, c) residual losses.

Hysteresis losses

For the hysteresis loss, it is due to the reversal of magnetization of magnetic core whenever it is subjected to alternating nature of magnetizing force. When the core is subjected to an alternating magnetic field, the domain present in the material will change their orientation alter every half cycle. The power consumed by the magnetic domains for changing the orientation after every half cycle is called Hysteresis loss.

Fig. 3-18 shows a B-H curve, even if the current is zero, the material is still containing some amount of flux, which is known as Retentivity. Any material has a property to retain some flux and to make that flux zero, a cohesive force is applied. That extra force is Hysteresis loss.

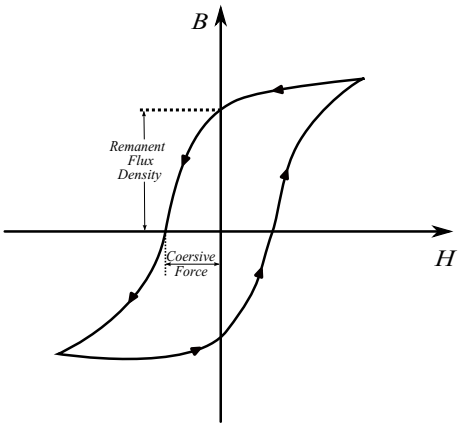


Figure 3.18: B-H characteristic of a inductor

Eddy current losses

Eddy current losses caused by the fact that the inductor core itself is composed of conducting material, so the voltage induced in it by the varying flux produces circulating current in the core. This current is so called eddy current, the loss caused by this current called eddy current losses. Fig. 3-19 shows the basic principle of eddy current losses.

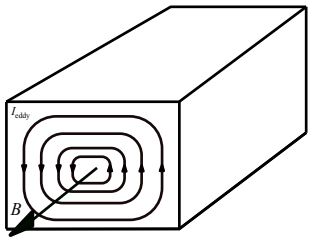


Figure 3.19: Illustration of eddy current losses

Core losses calculation

The most commonly used equation to calculate core losses is so called Steinmetz Equation:

$$P_{\mathrm{v}} = k f^{\alpha} \hat{B}^{\beta} (C_{t1} T^2 + C_{t2} T + C t) \tag{3.40}$$

Where $\hat{B}$ is the peak flux density of a sinusoidal flux density waveform with the frequency f. The left side of the equation P_v is the core losses per unit volume. K, α, β are material coefficients, which are referred to as the Steinmetz parameters. These parameters are determined by experiment and only valid for a limited f and $\hat{B}$ range. T is the temperature, and C_{t2}, C_{t1} and C_t are the temperature coefficients. Some Steinmetz parameters are given in Table 3-6 [4]

Material	k	α	β	C_t2	C_t1	C_t0
3C90	3.2	1.46	2.75	1.65e-4	3.1e-2	2.45
3C91	2.5	1.4	2.5	1.42e-4	1.3e-2	0.88
3F36	6.83	1.439	3.27	8.39e-5	1.08e-2	1.23
3C98	2.5	1.4	2.85	2.5e-4	0.05	3.5

Table 3.6: Steinmetz parameters

However, the Steinmetz Equation is not accurate enough to calculate core losses in many conditions because of following reasons:

- The flux density waveform is always non-sinusoidal in power electronic applications, especially for switched-mode power supply.
- A DC bias premagnetization H_{DC} is not taken into consideration

For the four-switch buck-boost converter, the flux density waveform is always non-sinusoidal, and a DC bias premagnetization is always existing, so the Steinmetz Equation is not capable in this application. An improved equation, the improved Generalized Steinmetz Equation (iGSE), proposed in [18], is applied:

$$P_{\text{core, } V} = \frac{1}{T}\int_0^T k_i \left|\frac{\mathrm{d}B}{\mathrm{d}t}\right|^{\alpha} (\Delta B)^{\beta-\alpha}\mathrm{d}t, \tag{3.41}$$

Where the ΔB is the peak-to-peak flux density, and k_i is determined by:

$$k_{\mathrm{i}} = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi}|\cos\theta|^{\alpha}2^{\beta-\alpha}\mathrm{d}\theta} \tag{3.42}$$

The parameters α, β and k are the same with which is used in Steinmetz Equation. Fig. 3-20 shows a trapezoidal flux density waveform which is a typical waveform for the ZVS modulation scheme of the four-switch buck-boost converter (see Chapter 4), and the Eq. 3-43 tells how to calculate the core losses with improved Generalized Steinmetz equation.

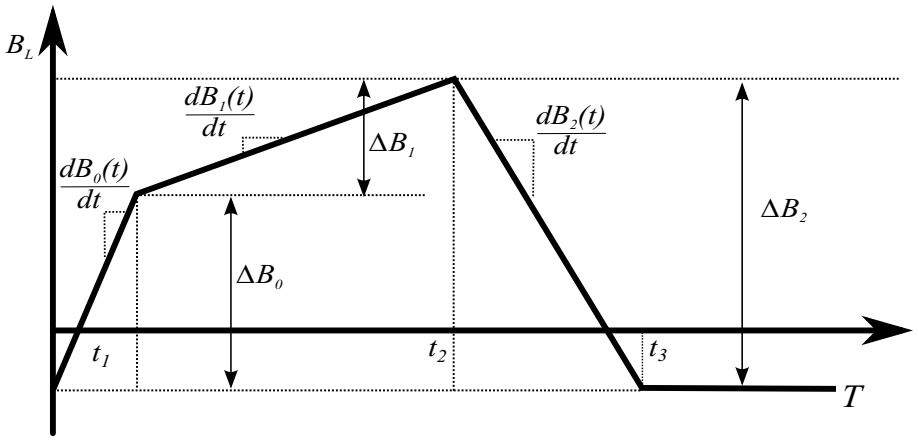


Figure 3.20: Example of iGSE

$$\begin{cases} P_{v1} = \frac{1}{T}\int_0^{t1} k_i \left|\frac{\Delta B_0}{t_1}\right|^{\alpha} (\Delta B_0)^{\beta-\alpha} dt, & 0 < t < t_1 \\ P_{v2} = \frac{1}{T}\int_{t_1}^{t_2} k_i \left|\frac{\Delta B_1}{t_2-t_1}\right|^{\alpha} (\Delta B_1)^{\beta-\alpha} dt, & t_1 < t < t_2 \\ P_{v3} = \frac{1}{T}\int_{t_2}^{t_3} k_i \left|\frac{\Delta B_1}{t_3-t_2}\right|^{\alpha} (\Delta B_1)^{\beta-\alpha} dt, & t_2 < t < t_3 \\ P_{v4} = 0, & t_3 < t < t_4 \\ P_v = P_{v1} + P_{v2} + P_{v3} + P_{v4} \end{cases} \tag{3.43}$$

3.2.3. Inductor winding losses

The ohmic losses in the winding is the second source of losses in the magnetic components. The resistance of conductors increases as frequency increases due to eddy currents. Skin-effect is caused by the self-induced eddy currents, while the proximity effect is caused by the eddy current which is induced by the external alternating magnetic field such as the air gap fringing field or the magnetic field from other conductors.

Skin effect

The magnetic field of a conductor which has current flowing is determined with Ampere's law

$$\oint H \mathrm{d}l = \iint J \mathrm{d}A \tag{3.44}$$

Where H is the magnetic field strength vector and J is the current density vector. If the current in the conductor is an alternating current, the magnetic field is also alternating.

According to Faraday's law,

$$\oint E\mathrm{d}l = -\frac{\mathrm{d}}{\mathrm{d}t}\iint B\mathrm{d}A \tag{3.45}$$

where E is the electric field vector and B is the magnetic flux density vector. An alternating magnetic field induces an electric field inside the conductor . The excitation current mainly occurs in the center of the conductor, and the major current flows in the outer layer of the conductor. This effect is so called skin effect.

The current density in the outer layers of the conductor is larger than it in the inner layers. The length from the diameter to where the current density falls to the $\frac{1}{e}$ of the maximum current density is the skin depth δ, which can be calculated by equation

$$\delta = \frac{1}{\sqrt{\pi\mu_0\sigma f}} \tag{3.46}$$

where
- μ_0 is the nature permeability.
- σ is the conductivity of the conductor material.
- f is the frequency of the alternating current.

To simplify, assuming the current concentrates in a skin layer depth σ with a constant current density. The losses caused by the skin effect can be calculated by the equation [19]

$$P_{\mathrm{S}} = F_{\mathrm{R/S}}(f)\cdot R_{\mathrm{DC}}\cdot \hat{I}^2 \tag{3.47}$$

Where:
-$F_{\mathrm{R/S}}(f) = R_{AC}/R_{DC}$ is the ratio between AC resistance and DC resistance.

Proximity Effect

Proximity effect is another factor which contributes to the winding losses. The current flowing in one conductor leads to a magnetic field which induces eddy currents in another conductor, vice versa. If currents in these two conductors have a same direction, on the adjacent side, the eddy current flowing opposite to the current in two conductors, the major current tends to flow at the other side of the conductor. The proximity effect losses can be calculated by the equation[19]

$$P_{\mathrm{P}} = R_{\mathrm{DC}}\cdot G_{\mathrm{R/S}}(f)\cdot \hat{H}_{\mathrm{e}}^2 \tag{3.48}$$

Where:
-$\hat{H}_{\mathrm{e}}$ is the peak external magnetic field.

- $G_{\mathrm{R/S}}(f)$ is a factor which describes the amount of winding losses due to the proximity effect. This factor is different for different conductor geometry.

In order to reduce the high frequency losses in terms of skin effect and proximity effect, in some application litz wire is selected. For Litz-wire, the factor F_R can be determined by [19]

$$F_{\mathrm{R}} = \frac{\xi}{4\sqrt{2}}\left(\frac{\mathrm{ber}_0(\xi)\,\mathrm{bei}_1(\xi) - \mathrm{ber}_0(\xi)\,\mathrm{ber}_1(\xi)}{\mathrm{ber}_1(\xi)^2 + \mathrm{bei}_1(\xi)^2} - \frac{\mathrm{bei}_0(\xi)\,\mathrm{ber}_1(\xi) + \mathrm{bei}_0(\xi)\,\mathrm{bei}_1(\xi)}{\mathrm{bec}_1(\xi)^2 + \mathrm{bei}_1(\xi)^2}\right) \tag{3.49}$$

The Equation.3-47 can be further developed to

$$P_{\mathrm{S,L}} = n \cdot R_{\mathrm{DC}} \cdot F_{\mathrm{R}}(f) \cdot \left(\frac{\hat{I}}{n}\right)^2 \tag{3.50}$$

Where:
- n is the number of strands of a litz wire

The proximity effect losses in litz-wire can be calculated by

$$P_{\mathrm{P,L}} = P_{\mathrm{P,L,e}} + P_{\mathrm{P,L,i}} \quad = n \cdot R_{\mathrm{DC}} |G_{\mathrm{R}}(f)\left(\hat{H}_{\mathrm{e}}^2 + \frac{\hat{I}^2}{2\pi^2 d_{\mathrm{a}}^2}\right) \tag{3.51}$$

Where:
- $P_{P,L,e}$ is the proximity effect caused by external magnetic field.
- $P_{P,L,i}$ is the proximity effect caused by internal magnetic field.
- the factor $G_R(f)$ is calculated by equation

$$G_{\mathrm{R}} = -\frac{\xi\pi^2 d^2}{2\sqrt{2}}\left(\frac{\mathrm{ber}_2(\xi)\,\mathrm{ber}_1(\xi) + \mathrm{ber}_2(\xi)\,\mathrm{bei}(\xi)}{\mathrm{ber}_0(\xi)^2 + \mathrm{bei}_0(\xi)^2} + \frac{\mathrm{bei}_2(\xi)\,\mathrm{bei}_1(\xi) - \mathrm{bei}_2(\xi)\,\mathrm{ber}_1(\xi)}{\mathrm{ber}_0(\xi)^2 + \mathrm{bei}_0(\xi)^2}\right) \tag{3.52}$$

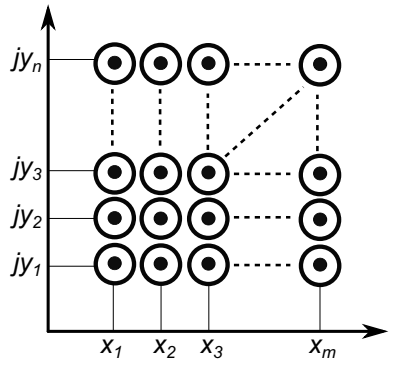


Figure 3.21: Winding example

The H_e, in the Eq. 3-51, is the external magnetic field generated by air gap fringing field and neighboring conductors. For a winding as illustrated in Fig. 3-21, in a certain conductor q_{mn} the magnetic field generated by an external current i_{ul} can be expressed as [19]

$$\hat{\mathbf{H}}_{\mathrm{e}} = -\mathrm{j}\frac{\hat{i}_{x_u,y_l}}{2\pi\sqrt{(x_u - x_i)^2 + \left(y_l - y_k\right)^2}} \cdot \frac{(x_u - x_i) + \mathrm{j}\left(y_l - y_k\right)}{\sqrt{(x_u - x_i)^2 + \left(y_l - y_k\right)^2}} = \frac{\hat{i}_{x_u,y_l}\left(\left(y_l - y_k\right) - \mathrm{j}\,(x_u - x_i)\right)}{2\pi\left((x_u - x_i)^2 + \left(y_l - y_k\right)^2\right)} \tag{3.53}$$

And the total external field $\hat{H}_e$ across the conductor q_{x_i,y_k} can be calculated by

$$\hat{H}_{\mathrm{e}} = \left| \sum_{u=1}^{m} \sum_{l=1}^{n} \epsilon(u,l) \frac{\hat{i}_{x_u,y_l}\left(\left(y_l - y_k\right) - \mathrm{j}\left(x_u - x_i\right)\right)}{2\pi\left(\left(x_u - x_i\right)^2 + \left(y_l - y_k\right)^2\right)} \right| \tag{3.54}$$

The wall of the winding window influences the magnetic distribution. The magnetic field is always almost perpendicular to the winding window wall since the permeability of the core material is much larger than the air[27]. The core material can be replaced by the conductor with a same direction current flowing in it, as illustrated in Fig. 3-22, this method is so called mirroring method. At the same time, the magnetic field distribution around the air gap can be modelled by a conductor with a opposite direction current which is also illustrated in Fig. 3-22.

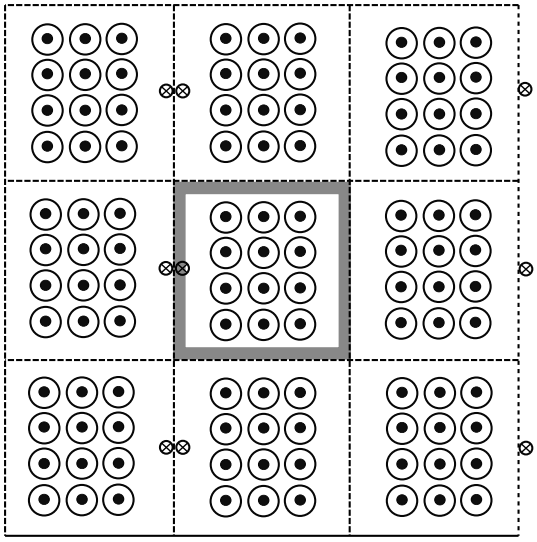


Figure 3.22: Winding example

By the mirroring method, the proximity and fringing effect both can be calculated.

3.3. Thermal modelling

In power electronics, temperature is one of the most important parameters because almost all the semiconductors are highly temperature dependent components. All semiconductor components have a maximum temperature limitation, and the semiconductor components will be damaged permanently if the maximum junction temperature is exceeded. On the other hand, even the maximum temperature is below the limitation, the semiconductor lifetime is dominated by temperature swings. The temperature swing leads to mechanical deformation according to expansion and contraction principle, and it causes mechanical pressure and affects the lifetime of semiconductor devices.

There are three physical mechanisms conduction, radiation and convection to transfer heat. For a semiconductor component, conduction is the dominated mechanism. The

Electrical Domain			Thermal Domain		
Variable	Symbol	Units	Variable	Symbol	Units
Current	I	Amperes	Power or heat flux	P	Watts
Voltage	v	Volts	Temperature	T	$^{\circ}C$
Electrical Resistance	R	Ohms	Thermal Resistance	R_θ	$^{\circ}C/W$
Electrical Capacitance	C	Farads	Thermal capacitance	C_θ	$Joules/^{\circ}C$
$\Delta V = I \times R$			$\Delta T = P \times R_\theta$		

Table 3.7: Thermal and electrical domain equivalence

basic principle of heat conduction is similar to the electrical circuit. Table. 3-7 illustrates the equivalences relationship between thermal conduction and electrical circuit.

Fig. 3-23 shows a certain material section which has a temperature difference on two sides. The heat flux transferring per unit time is given by

$$P = \frac{\lambda A \Delta T}{d} \tag{3.55}$$

Where:
-A is the cross section area $A = a \times b$.
-d is the length of the cross section.
-λ is the thermal conductivity of the material.
-ΔT is the temperature difference $\Delta T = T_A - T_B$

According to the relationship in Table. 3-7, the thermal resistance is defined as

$$R_\theta = \frac{d}{\lambda A} \tag{3.56}$$

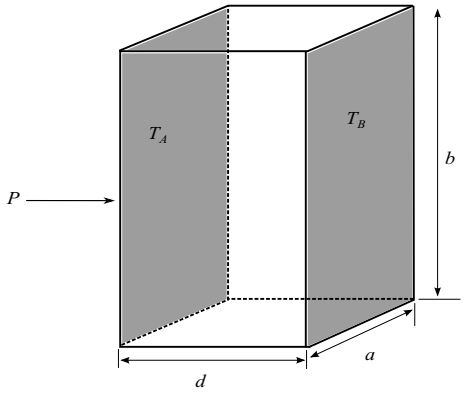


Figure 3.23: Heat conduction

For semiconductor switches, typically, there a two kinds of package, through hole and surface mount. Fig. 3-24 shows the thermal layout of a TO-220 (through hole) package device, and the equivalent circuit is shown in Fig.3-25 in which R_{JC} is the thermal resistance between junction to case, R_{TIM} is the thermal resistance of thermal interface material, R_{HSA} is the thermal resistance from heatsink to ambient. On the other side of the device, the heat is also be transferred by radiation or convection to ambient. Among these thermal resistance, TIM represents thermal interface material which is a layer of isolation material between semiconductor device and heatsink, and its specific thermal resistance can be calculated by Eq. 3-56. For the thermal resistance R_{HSA}, it is strongly dependent on the geometry of the heatsink and the air flowing speed surrounding the heatsink. If the liquid cooling is applied, the liquid temperature is assumed to be constant, and R_{HSA} is relatively small. The thermal resistance of the path A is much smaller than it of the path B as illustrates in Fig. 3-24, therefore the path A is dominant. According to the equivalent thermal circuit, the junction temperature, in this case, is calculated with

$$T_J = T_A + \frac{R_{JA} \cdot (R_{JA} + R_{TIM} + R_{HSA})}{R_{JA} + R_{TIM} + R_{HSA} + R_{JA}} \cdot P \tag{3.57}$$

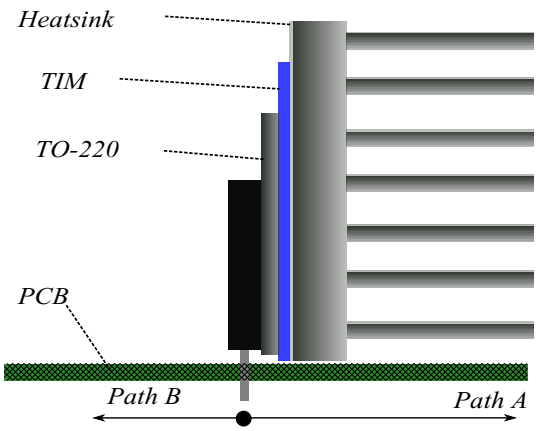


Figure 3.24: Thermal layout of a through hole device

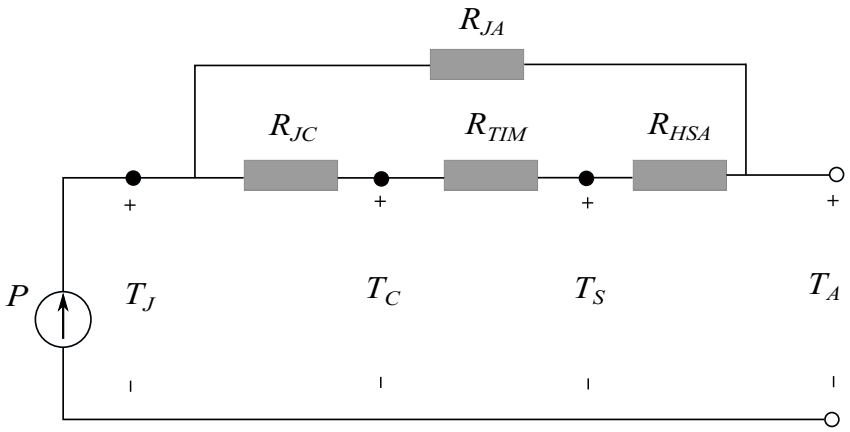


Figure 3.25: The equivalent thermal circuit

Fig. 3-26 shows the thermal layout of a surface mount device, and Fig. 3-27 shows the thermal equivalent circuit. The device is attached on the PCB board, and the top side of the device is attached to heatsink with a layer of TIM in between. On the bottom side, the heat is transferring from the junction to the board and through the PCB board to the ambient. Those vias inside the PCB help heat transferring, in other words, the thermal resistance of PCB R_{PCB} is reduced by those vias. In this case, the path A is also dominate due to lower thermal resistance. According to the equivalent thermal circuit, the junction temperature is calculated with

$$T_J = T_A + \frac{(R_{JB} + R_{PCB}) \cdot (R_{JC} + R_{TIM} + R_{HSA})}{R_{JC} + R_{TIM} + R_{HSA} + R_{JB} + R_{PCB}} \cdot P \tag{3.58}$$

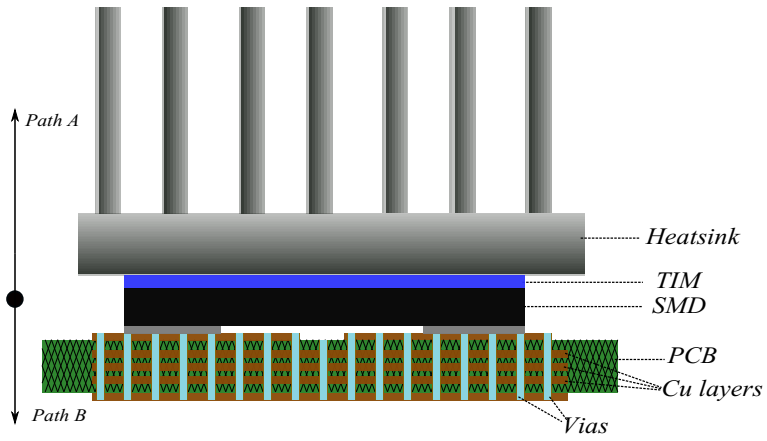


Figure 3.26: The thermal layout of a SMD device

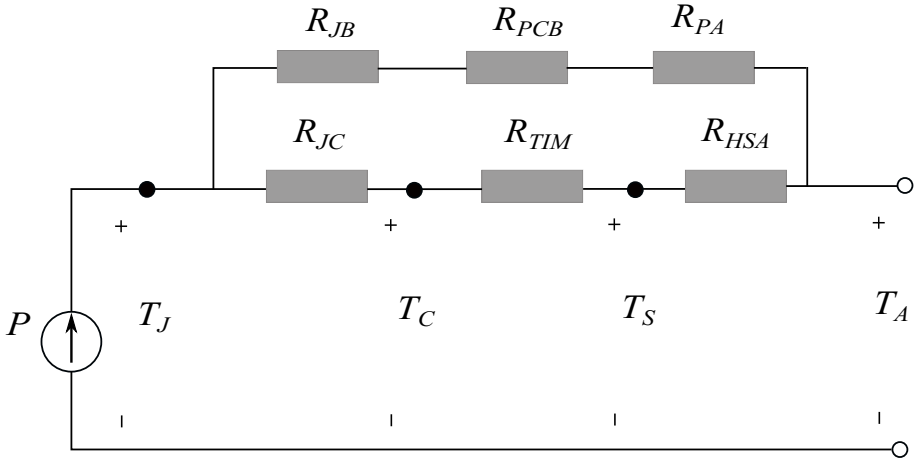


Figure 3.27: The equivalent thermal circuit

4

Modulation scheme

It is possible to operate in several modulation schemes with the selected topology which could be suitable for different applications. In this chapter, these modulation schemes are introduced respectively. A comparison is made between these modulation schemes analytically and numerically. In order to achieve a smaller temperature swing of semiconductor devices when transferred power changes, which leads to longer lifetime and better reliability of semiconductors, a new modulation scheme is proposed at the end of this chapter.

4.1. Modulation I: S_4 hard switching modulation

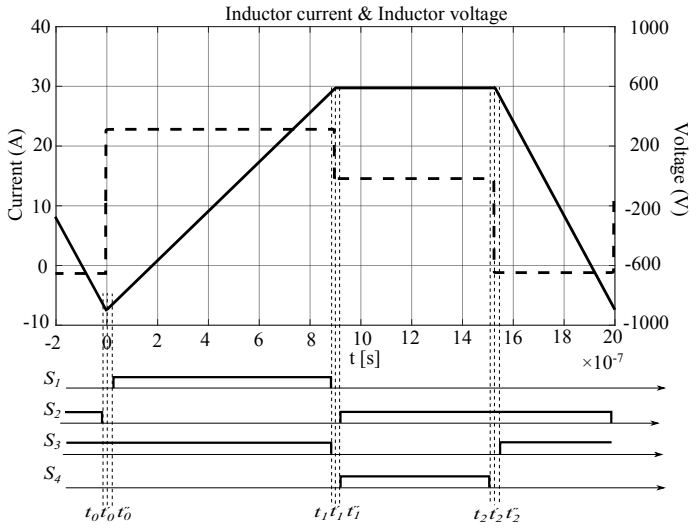


Figure 4.1: Inductor current waveform, inductor voltage waveform and gate signal of each switch of Modulation I

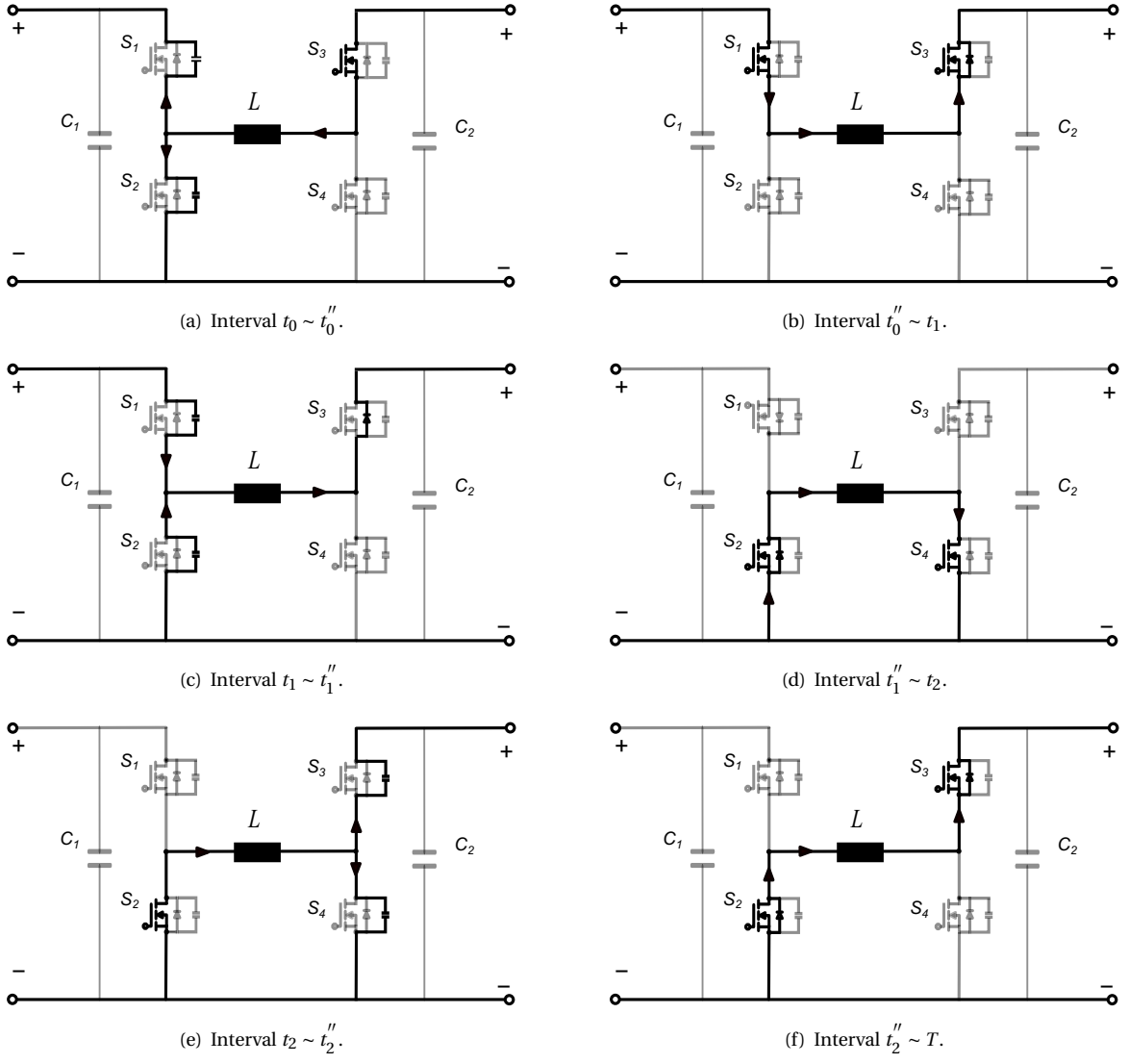
Fig. 4-1 shows the first modulation scheme, in terms of inductor current waveform, voltage across the inductor and gate signal of each switch. This waveform is based on an input voltage $960V$, output voltage $630V$, switching frequency $500kHz$, inductor value $8\mu H$ and output current $8A$ at the low voltage side.

Fig. 4-2 shows the detailed operation sequence of each time interval.

- $t < t_0$
  Before the start of the switching cycle, the switch S_2 and S_3 are switched on, and a negative voltage is applied on the inductor L. The inductor current is flowing from the right to the left side, assuming to be a negative current.
- $t_0 < t < t_0^{'}$
  At time instant t_0 the switch S_2 is open, the resistance of the transistor channel is increased rapidly, and the current starts to flow on the parasitic output capacitance of S_2. The output capacitor is charged, which caused the voltage across it rising.
- $t_0^{'} < t < t_0^{''}$
  After time instant $t_0^{'}$, the current start to flow on the output capacitor of switch S_1, and the output capacitor is discharged, and the voltage of midpoint will reach the bus voltage at a certain time which drives the body diode of S_1 to conduct, now the transistor can be switched on at zero voltage.
- $t_0^{''} < t < t_1$
  Before the time instant t_1, the switch S_1 and S_3 are switched on, and a positive voltage $V_{in} - V_{out}$ is applied on the inductor L. The inductor current flowing from left to right side.
- $t_1 < t < t_1^{'}$
  At time instant t_1 the switch S_1 is open, the resistance of transistor channel is increased rapidly, and the current starts to flow on the parasitic output capacitance of S_1. The output capacitor is charged which caused the voltage across it rising. At the same time, the switch S_3 is open, the diode takes over the current which makes the S_3 switch off in almost zero voltage.
- $t_1^{'} < t < t_1^{''}$
  After time instant $t_1^{'}$, the current start to flow on the output capacitor of switch S_2, and the output capacitor is discharged, and the voltage of midpoint will reach the zero at a certain time which drives the body diode of S_2 to conduct, now the transistor can be switched on at zero voltage. At the same time, on the other side of the inductor, and switch S_4 is switched on at the peak current. The voltage across the switch S_4 is the same with low side bus voltage, which means S_4 suffers high switch-on losses.
- $t_1^{''} < t < t_2$
  Before the time instant t_2, the switch S_2 and S_4 are switched on, and no voltage is applied on the inductor L causing a freewheeling period making the inductor current constant. The inductor current flowing from left to right side.
- $t_2 < t < t_2^{'}$

At time instant t_2 the switch S_4 is open, the resistance of transistor channel is increased rapidly, and the current starts to flow on the parasitic output capacitance of S_4. The output capacitor is charged which caused the voltage across it rising.

- $t_2^{'} < t < t_2^{''}$
  After time instant $t_2^{'}$, the current starts to flow on the output capacitor of switch S_3, and the output capacitor is discharged, and the voltage of midpoint will reach the bus voltage at a certain time which drives the body diode of S_3 to conduct, now the transistor can be switched on at zero voltage.



(a) Interval $t_0 \sim t_0^{''}$.

(b) Interval $t_0^{''} \sim t_1$.

(c) Interval $t_1 \sim t_1^{''}$.

(d) Interval $t_1^{''} \sim t_2$.

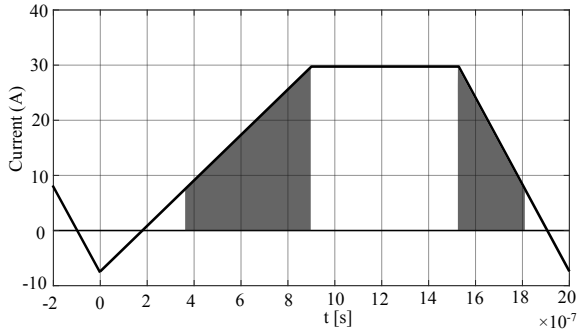
(e) Interval $t_2 \sim t_2^{''}$.

(f) Interval $t_2^{''} \sim T$.

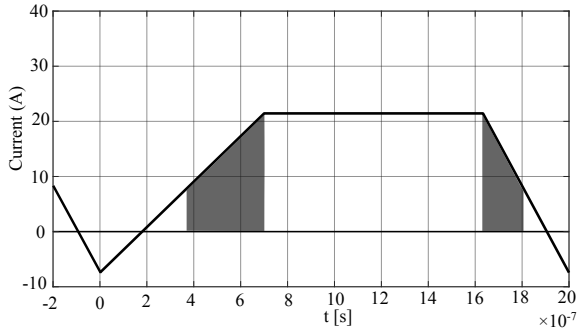
Figure 4.2: The path of the inductor current i_L during each time intervals (a) $t_0 \sim t_0^{''}$. (b) $t_0^{''} \sim t_1$. (c) $t_1 \sim t_1^{''}$. (d) $t_1^{''} \sim t_2$. (e) $t_2 \sim t_2^{''}$. (f) $t_2^{''} \sim T$.

The transferred power is regulated by adjusting the duty cycle of each interval. More power is transferred by increasing the length of interval $0 \sim t_1$, and the interval $t_2 \sim T$ is also in-

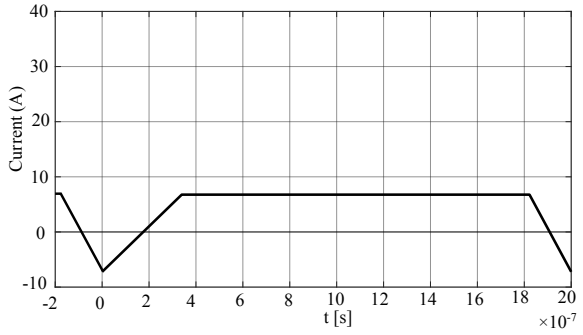
creased to fulfill the voltage second balance. In maximum power, $t_1 = t_2$ Hence, the freewheeling interval is shortened. Less power is transferred by shortening the intervals $0 \sim t_1$ and $t_2 \sim T$ but lengthen the freewheeling interval.



(a) 20 kW .



(b) 10 kW.



(c) 0 kW.

Figure 4.3: Power regulation of Modulation I.

In this modulation scheme, as is illustrated in Fig. 4-2(c) to Fig. 4-2(d), the switch S_4 is switching on hardly at a peak current which makes S_4 suffers high switching on losses. As the transferred power growing, the peak inductor current increases a lot. Therefore, the losses on switch S_4 also changes a lot. For switch S_3, when it is switched off, the diode takes over the current, hence, the switching off losses just occurs on the diode, which makes the switching off losses very small. Meanwhile, for this modulation, it does not transfer power during the interval $t_1 \sim t_2$ which not only makes the conduction losses of switch S_2 and S_4 larger but also leads to a larger RMS inductor current and a larger inductor size.

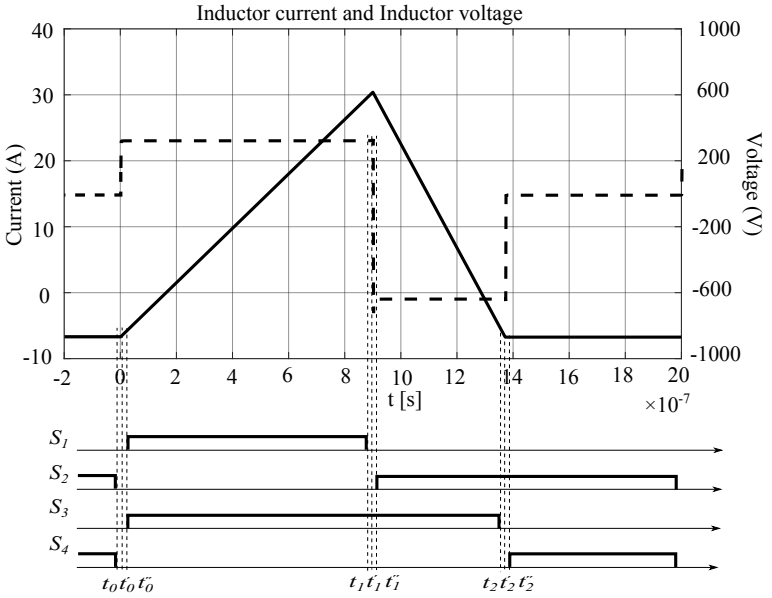


Figure 4.4: Inductor current waveform, inductor voltage waveform and gate signal of each switch of Modulation II

4.2. Modulation II: S_3 hard switching modulation

Fig. 4-4 shows a typical inductor current waveform ($V_{in} = 960V, V_{out} = 630V, I_{out} = 8A$,)of the second modulation scheme, which is similar to the Modulation I, but the free-wheeling interval is at the end of each cycle. Fig. 4-4 also illustrates the gate signal of each switch and Fig. 4-5 shows the operation sequence respectively.

- $t < t_0$
  Before the start of the switching cycle, the switch S_2 and S_4 are switched on, and no $-V_{out}$ is applied on the inductor L which keeps the inductor current constant. The inductor current flowing from right to left side, assuming to be a negative current.

- $t_0 < t < t_0^{'}$
  At time instant t_0 the switch S_2 is open, the resistance of transistor channel is increased rapidly, and the current starts to flow on the parasitic output capacitance of S_2. The output capacitor is charged which caused the voltage across it rising. At the same time, the switch S_4 is open, and the body diode of S_4 takes over the current.

- $t_0^{'} < t < t_0^{''}$
  After time instant $t_0^{'}$, the current starts to flow on the output capacitor of switch S_1, and the output capacitor is discharged, and the voltage of midpoint will reach the bus voltage at a certain time which drives the body diode of S_1 to conduct, now the transistor can be switched on at zero voltage. Meanwhile, the switch S_3 is switched on under the output bus voltage, which causes a significant switched-on losses.

- $t_0^{''} < t < t_1$
  Before the time instant t_1, the switch S_1 and S_3 are switched on, and a positive voltage

$V_{in} - V_{out}$ is applied on the inductor L. The inductor current is flowing from left to the right side.

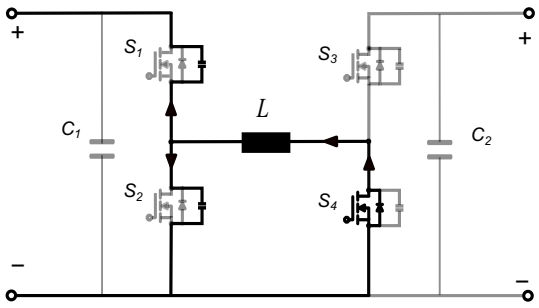
- $t_1 < t < t_1^{'}$
  At time instant t_1 the switch S_1 is open, the resistance of transistor channel is increased rapidly, and the current starts to flow on the parasitic output capacitance of S_1. The output capacitor is charged which causes the voltage across it rising.

- $t_1^{'} < t < t_1^{''}$
  After time instant $t_1^{'}$, the current starts to flow on the output capacitor of switch S_2, and the output capacitor is discharged, and the voltage of midpoint will reach the zero at a certain time which drive the body diode of S_2 to conduct, now the transistor can be switched on at zero voltage.

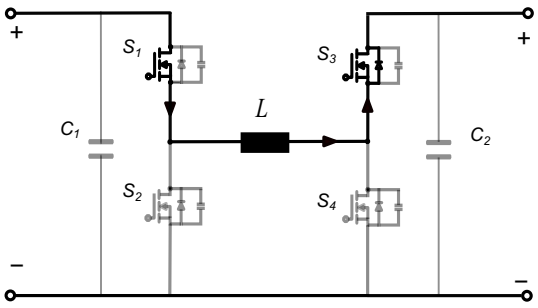
- $t_1^{''} < t < t_2$
  Before the time instant t_2, the switch S_2 and S_3 are switched on, and a negative voltage $-V_{out}$ is applied on the inductor L causing the inductor current decreasing. The inductor current flowing from left to right side.

- $t_2 < t < t_2^{'}$
  At time instant t_2 the switch S_3 is open, the resistance of transistor channel is increased rapidly, and the current starts to flow on the parasitic output capacitance of S_4. The output capacitor is charged which causes the voltage across it rising.

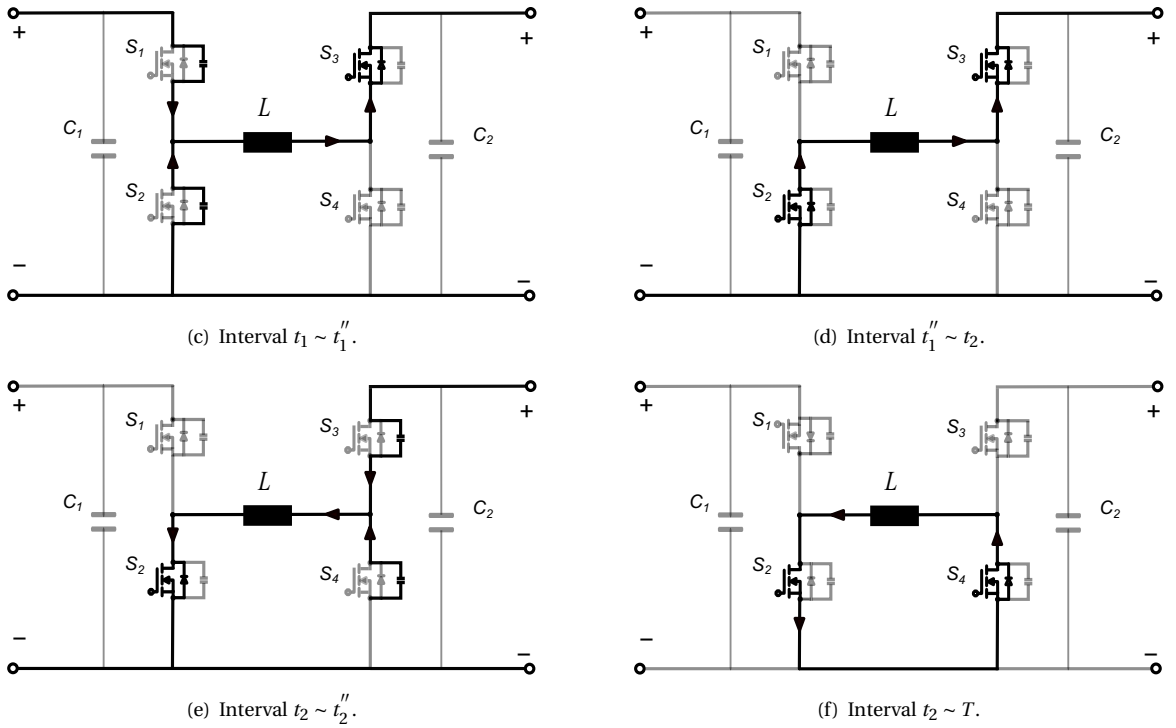
- $t_2^{'} < t < t_2^{''}$
  After time instant $t_2^{'}$, the current start to flow on the output capacitor of switch S_4, and the output capacitor is discharged, and the voltage of midpoint will reach zero at a certain time which drives the body diode of S_4 to conduct, now the transistor can be switched on at zero voltage.



(a) Interval $t_0 \sim t_0^{''}$.



(b) Interval $t_0^{''} \sim t_1$.



(c) Interval $t_1 \sim t_1^{''}$.

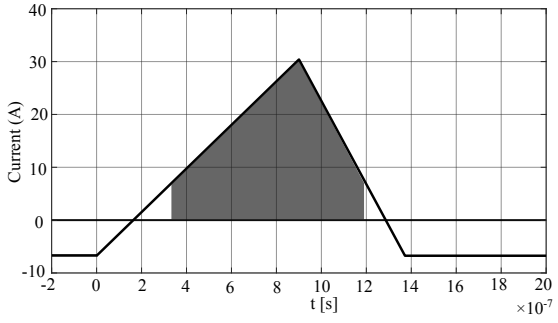
(d) Interval $t_1^{''} \sim t_2$.

(e) Interval $t_2 \sim t_2^{''}$.

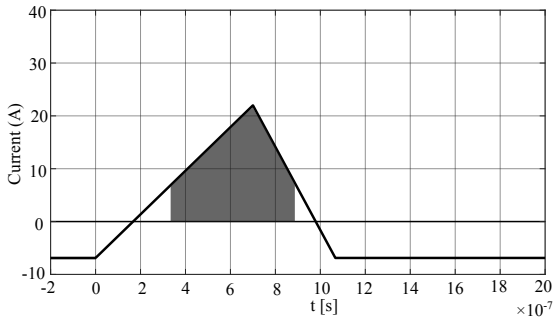
(f) Interval $t_2 \sim T$.

Figure 4.5: The path of the inductor current i_L during each time intervals (a) $t_0 \sim t_0^{''}$. (b) $t_0^{''} \sim t_1$. (c) $t_1 \sim t_1^{''}$. (d) $t_1^{''} \sim t_2$. (e) $t_2 \sim t_2^{''}$. (f) $t_2^{''} \sim T$.

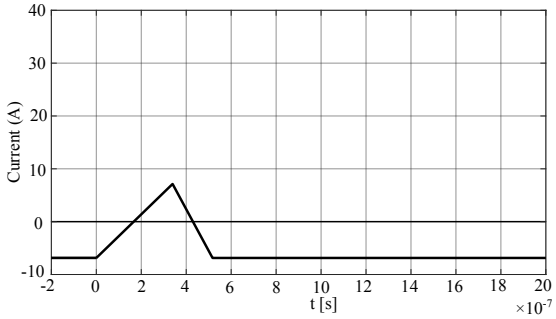
For this modulation scheme, Fig. 4-6 shows the power regulation principle, which is the same as Modulation I, by adjusting the duty cycle of each time interval.



(a) 20 kW.



(b) 10 kW.



(c) 0 kW.

Figure 4.6: Power regulation of Modulation II.

If the four-switch buck-boost converter operates in this modulation scheme, the switch S_3 is always in hard switching mode. However, compared with switch S_4 in Modulation I, in this modulation scheme, S_3 is switched on at a much lower current which makes the losses much lower. The switch S_4 is switched off softly. The free-wheeling interval is at the end of each cycle with lower current value compared with Modulation I, a lower conduction losses occurs on switch S_2 and S_4. In addition, the RMS current on inductor is smaller leads to a smaller inductor size.

4.3. Modulation III: High trapezoidal current modulation

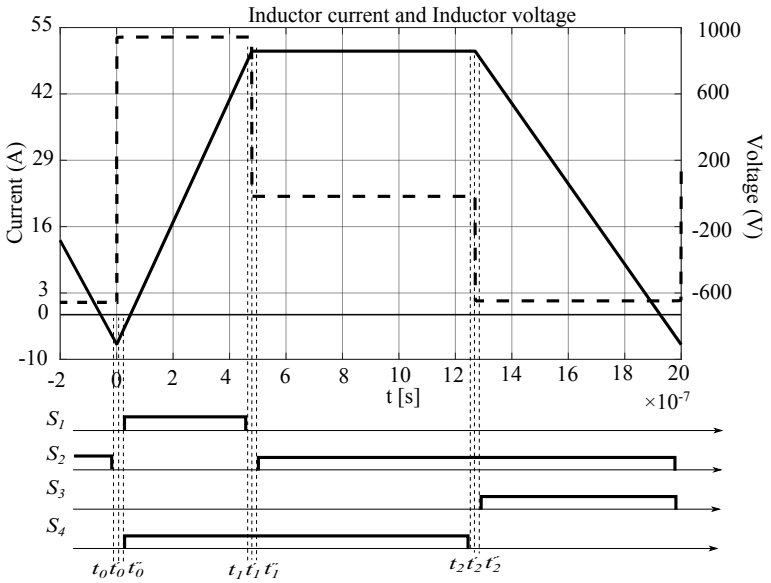
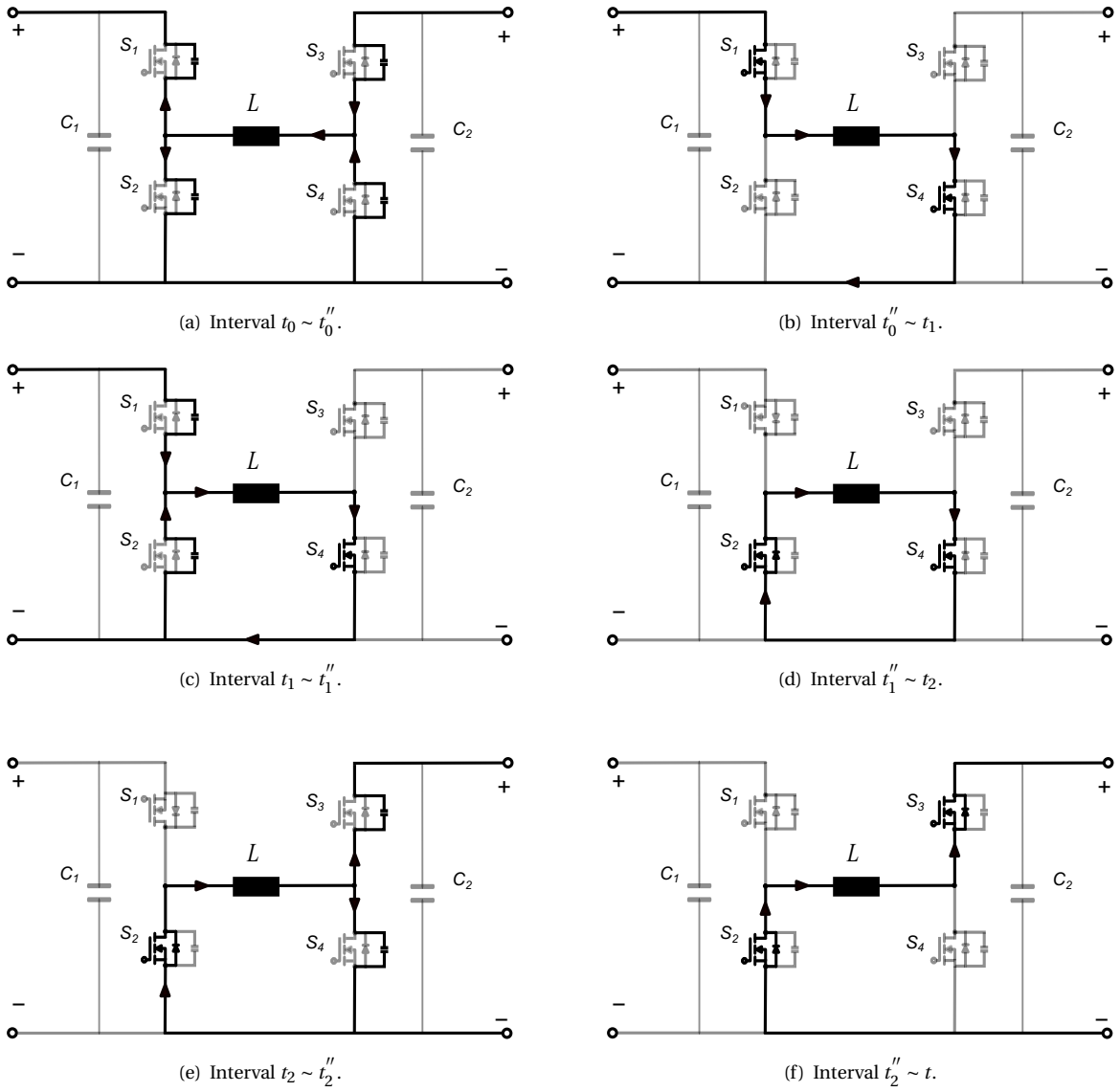


Figure 4.7: Inductor current waveform, inductor voltage waveform and gate signal of each switch of Modulation III

Fig. 4-7 shows another modulation scheme which also has a trapezoid inductor current waveform. Fig. 4-8 shows the operation sequence respectively.



(a) Interval $t_0 \sim t_0^{''}$.

(b) Interval $t_0^{''} \sim t_1$.

(c) Interval $t_1 \sim t_1^{''}$.

(d) Interval $t_1^{''} \sim t_2$.

(e) Interval $t_2 \sim t_2^{''}$.

(f) Interval $t_2^{''} \sim t$.

Figure 4.8: The path of the inductor current i_L during each time intervals (a) $t_0 \sim t_0^{''}$. (b) $t_0^{''} \sim t_1$. (c) $t_1 \sim t_1^{''}$. (d) $t_1^{''} \sim t_2$. (e) $t_2 \sim t_2^{''}$. (f) $t_2^{''} \sim T$.

- $t < t_0$
  Before the start of the switching cycle, the switch S_2 and S_3 are switched on, and a negative voltage $-V_{out}$ is applied on the inductor L. The inductor current is flowing from right to left side, assuming to be a negative current.
- $t_0 < t < t_0^{'}$
  At time instant t_0 the switch S_2 is open, the resistance of transistor channel is increased rapidly, and the current starts to flow on the parasitic output capacitance of S_2. The output capacitor is charged which causes the voltage across it rising.
- $t_0^{'} < t < t_0^{''}$
  After time instant $t_0^{'}$, the current start to flow on the output capacitor of switch S_1,

and the output capacitor is discharged, and the voltage of midpoint will reach the bus voltage at a certain time which drives the body diode of S_1 to conduct, now the transistor can be switched on at zero voltage.

- $t_0^{''} < t < t_1$
  Before the time instant t_1, the switch S_1 and S_4 are switched on, and a positive voltage V_{in} is applied on the inductor L. The inductor current is flowing from left to right side.

- $t_1 < t < t_1^{'}$
  At time instant t_1 the switch S_1 is open, the resistance of transistor channel is increased rapidly, and the current starts to flow on the parasitic output capacitance of S_1. The output capacitor is charged which causes the voltage across it rising.

- $t_1^{'} < t < t_1^{''}$
  After time instant $t_1^{'}$, the current starts to flow on the output capacitor of switch S_2, and the output capacitor is discharged, and the voltage of midpoint will reach the zero at a certain time which drive the body diode of S_2 to conduct, now the transistor can be switched on at zero voltage.

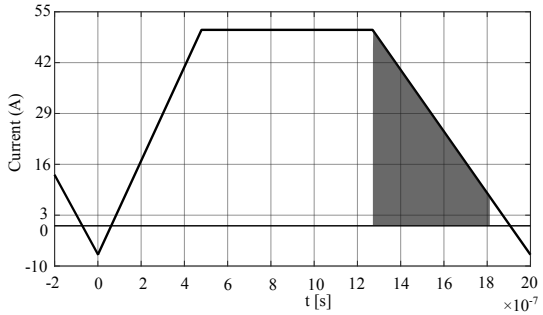
- $t_1^{''} < t < t_2$
  Before the time instant t_2, the switch S_2 and S_4 are switched on, and no voltage is applied on the inductor L causing a freewheeling period making the inductor current constant. The inductor current is flowing from left to right side.

- $t_2 < t < t_2^{'}$
  At time instant t_2 the switch S_4 is open, the resistance of transistor channel is increased rapidly, and the current starts to flow on the parasitic output capacitance of S_4. The output capacitor is charged which causes the voltage across it rising.

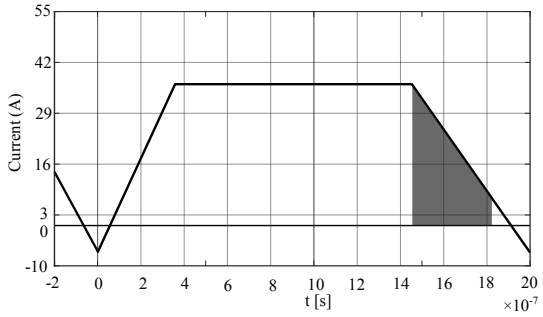
- $t_2^{'} < t < t_2^{''}$
  After time instant $t_2^{'}$, the current starts to flow on the output capacitor of switch S_3, and the output capacitor is discharged, and the voltage of midpoint will reach the bus voltage at a certain time which drives the body diode of S_3 to conduct, now the transistor can be switched on at zero voltage.

If the current at the beginning of each cycle I_0 reaches the minimum ZVS current, and the peak current I_1 is also large enough to ensure zero voltage switching, in this modulation scheme, these four switches can all achieve zero voltage switching on.

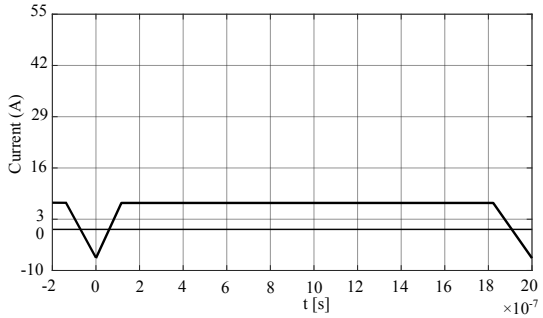
Fig. 4-9 shows the power regulation principle of Modulation III .



(a) 20 kW .



(b) 10 kW .



(c) 0 kW.

Figure 4.9: Power regulation of modulation III

In this modulation scheme, the power is transferred in the interval $t_2 \sim T$, it suffers from a large reactive current, although zero voltage switching is obtained for all switches. The peak current is much higher than the previous two modulation schemes which means the switch S_1 and S_4 suffer from high switching off losses. Meanwhile, all switches have lager conduction losses. The peak current varies for a large extent, which makes the losses on switches also vary a lot.

4.4. Modulation IV: High triangular current modulation

Fig. 4-10 shows the fourth modulation scheme, in terms of inductor current waveform, voltage across the inductor and gate signal of each switch. Fig 4-11 shows the operation sequence of each state.

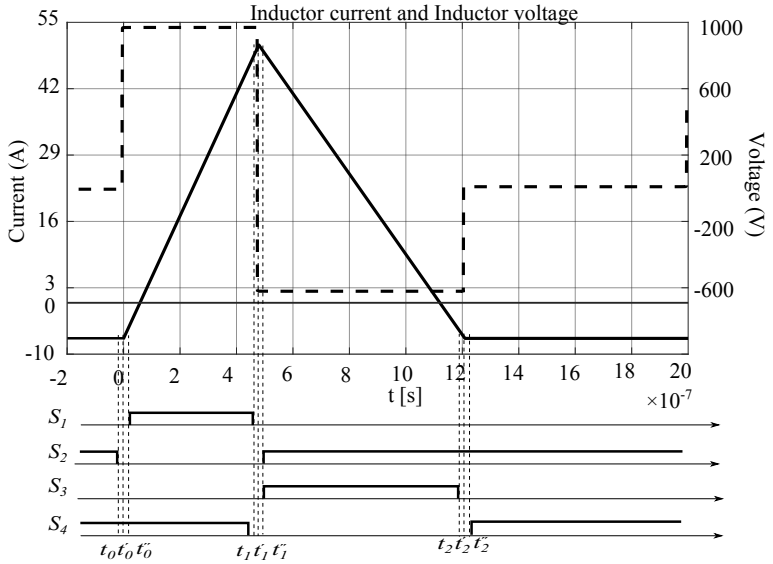


Figure 4.10: Inductor current waveform, inductor voltage waveform and gate signal of each switch of Modulation IV

- $t < t_0$
  Before the start of the switching cycle, the switch S_2 and S_4 are switched on, and no voltage is applied on the inductor L which keeps the indcutor current constant. The inductor current flowing from right to left side, assuming to be a negative current.
- $t_0 < t < t_0^{'}$
  At time instant t_0 the switch S_2 is open, the resistance of transistor channel is increased rapidly, and the current starts to flow on the parasitic output capacitance of S_2. The output capacitor is charged which causes the voltage across it rising.
- $t_0^{'} < t < t_0^{''}$
  After time instant $t_0^{'}$, the currents start to flow on the output capacitor of switch S_1, and the output capacitor is discharged, and the voltage of midpoint will reach the bus voltage at a certain time which drives the body diode of S_1 to conduct, now the transistor can be switched on at zero voltage.
- $t < t_1$
  Before the time instant t_1, the switch S_1 and S_4 are switched on, and a positive voltage V_{in} is applied on the inductor L. The inductor current is increasing and flowing from left to right side.
- $t_1 < t < t_1^{'}$
  At time instant t_1 the switch S_4 is open, the resistance of transistor channel is increased rapidly, and the current starts to flow on the parasitic output capacitance of S_4. The output capacitor is charged which caused the voltage across it rising.
- $t_0^{'} < t < t_0^{''}$
  After time instant $t_1^{'}$, the current start to flow on the output capacitor of switch S_3, and the output capacitor is discharged, and the voltage of midpoint will reach the bus

voltage of the low voltage side at a certain time which drive the body diode of S_3 to conduct, now the transistor is switched on at zero voltage.

- $t < t_2$
  Before the time instant t_2, the switch S_1 and S_3 are switched on, and a positive voltage $V_{in} - V_{out}$ is applied on the inductor L causing the indcutor current increasing. The inductor current flowing from left to right side.

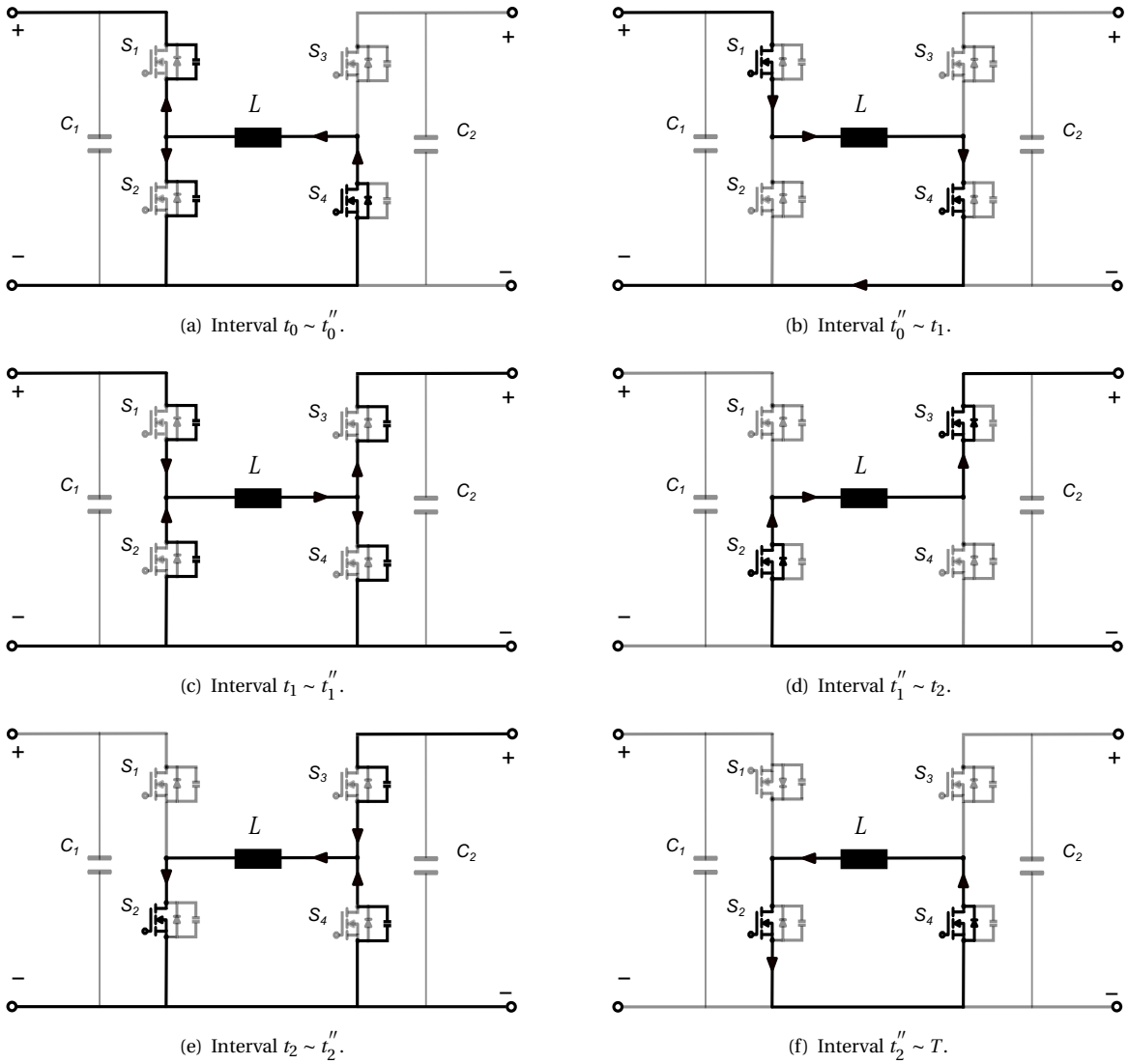
- $t_2 < t < t_2^{'}$
  At time instant t_2 the switch S_1 is open, the resistance of transistor channel is increased rapidly, and the current starts to flow on the parasitic output capacitance of S_1. The output capacitor is charged which causes the voltage across it rising.

- $t_2^{'} < t < t_2^{''}$
  After time instant $t_2^{'}$, the current start to flow on the output capacitor of switch S_2, and the output capacitor is discharged, and the voltage of midpoint will reach zero at a certain time which drives the body diode of S_2 to conduct, now the transistor can be switched on at zero voltage.

- $t < t_3$
  Before the time instant t_3, the switch S_2 and S_3 are switched on, and a negative voltage $-V_{out}$ is applied on the inductor L causing the indcutor current decreasing. The inductor current flowing from right to left side.

- $t_3 < t < t_3^{'}$
  At time instant t_2 the switch S_3 is open, the resistance of transistor channel is increased rapidly, and the current starts to flow on the parasitic output capacitance of S_3. The output capacitor is charged which causes the voltage across it rising.

- $t_3^{'} < t < t_3^{''}$
  After time instant $t_3^{'}$, the current start to flow on the output capacitor of switch S_2, and the output capacitor is discharged, and the voltage of midpoint will reach zero at a certain time which drives the body diode of S_4 to conduct, now the transistor can be switched on at zero voltage.



(a) Interval $t_0 \sim t_0''$.

(b) Interval $t_0'' \sim t_1$.

(c) Interval $t_1 \sim t_1''$.

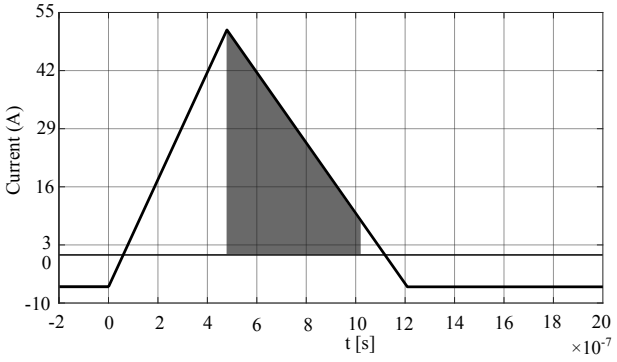
(d) Interval $t_1'' \sim t_2$.

(e) Interval $t_2 \sim t_2''$.

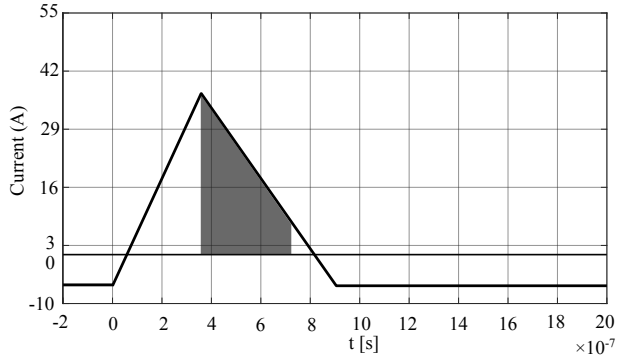
(f) Interval $t_2'' \sim T$.

Figure 4.11: The path of the inductor current i_L during each time intervals (a) $t_0 \sim t_0''$. (b) $t_0'' \sim t_1$. (c) $t_1 \sim t_1''$. (d) $t_1'' \sim t_2$. (e) $t_2 \sim t_2''$. (f) $t_2'' \sim T$.

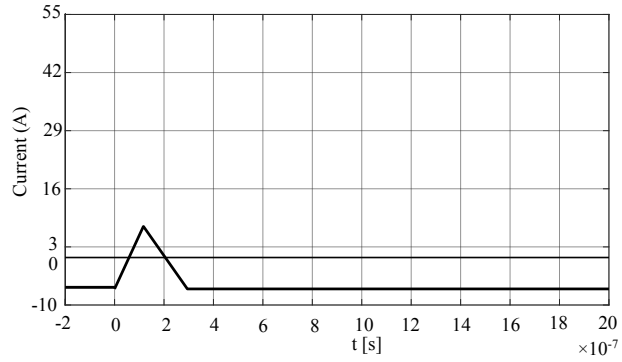
Fig. 4-12 shows the power regulation principle of Modulation IV .



(a) 20 kW .



(b) 10 kW .



(c) 0 kW.

Figure 4.12: Power regulation of modulation IV

The Modulation IV is similar to the Modulation III but shifts the free-wheeling interval to the end of each cycle. Therefore, the conduction losses on switch S_2 and S_4 will be smaller than it in Modulation III. Similarly, this modulation also suffers large reactively current, the switch S_1 and S_4 are both switched off at the large peak current which makes the switching off losses large and also the loss swings for a large extent.

4.5. Modulation V: Zero voltage switching modulation

Fig.4-13 shows the fifth modulation scheme introduced by[28], in terms of inductor current waveform, the voltage across the inductor and gate signal of each switch. This waveform is based on a input voltage $960V$,output voltage $630V$, switching frequency $500kHz$, inductor value $8\mu H$ and output current $8A$ at the low voltage side. All four switches achieve zero voltage switch, so it is called zero voltage switching modulation. The current I_0 is the minimum negative offset current to ensure the zero voltage switching of switch S_1.

- $t < t_0$
  Before the start of the switching cycle, the switch S_2 and S_4 are switched on, and no voltage is applied on the inductor L which keeps the inductor current constant. The inductor current flowing from right to left side, assuming to be a negative current.
- $t_0 < t < t_0^{'}$

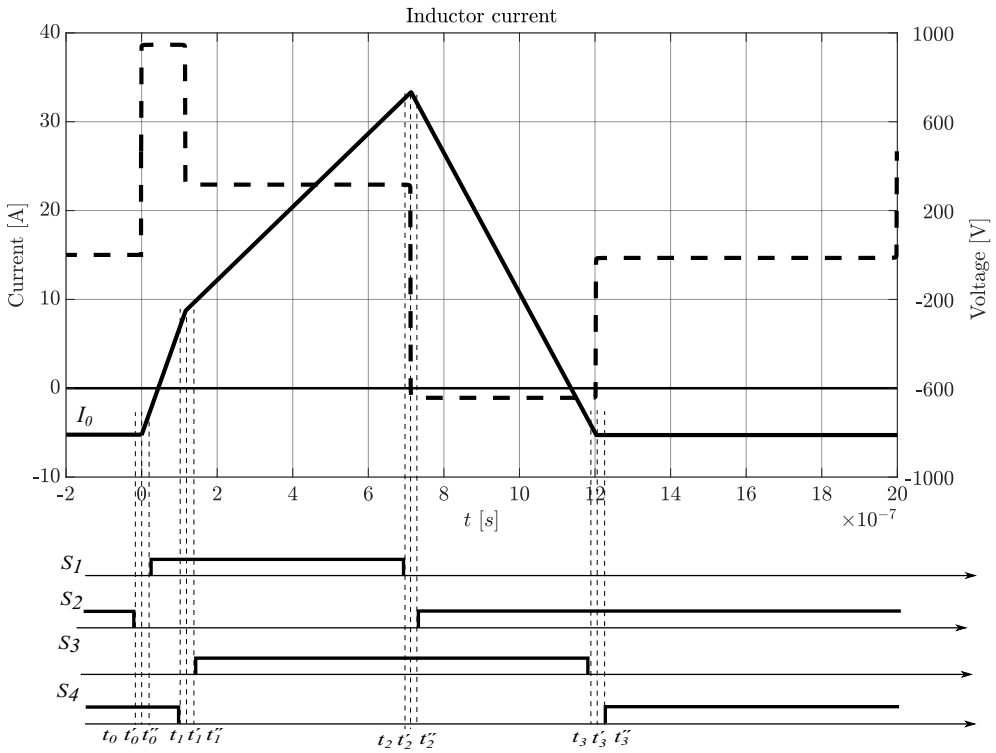


Figure 4.13: Inductor current waveform, inductor voltage waveform and gate signal of each switch of ZVS Modulation

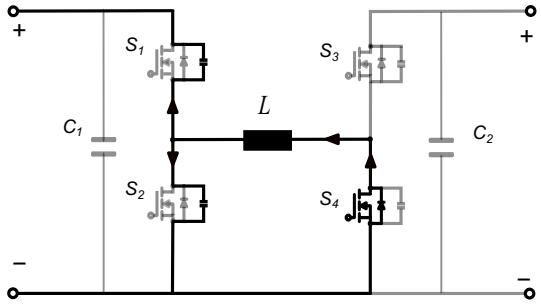
At time instant t_0 the switch S_2 is open, the resistance of transistor channel is increased rapidly, and the current starts to flow on the parasitic output capacitance of S_2. The output capacitor is charged which caused the voltage across it rising.

- $t_0^{'} < t < t_0^{''}$
  After time instant $t_0^{'}$, the current starts to flow on the output capacitor of switch S_1, and the output capacitor is discharged, and the voltage of midpoint will reach the bus voltage at a certain time which drive the body diode of S_1 to conduct, now the transistor can be switched on at zero voltage.

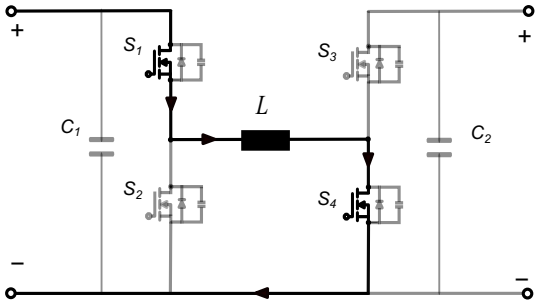
- $t < t_1$
  Before the time instant t_1, the switch S_1 and S_4 are switched on, and a positive voltage V_{in} is applied on the inductor L. The inductor current is increasing and flowing from left to right side.

- $t_1 < t < t_1^{'}$
  At time instant t_1 the switch S_1 is open, the resistance of transistor channel is increased rapidly, and the current starts to flow on the parasitic output capacitance of S_1. The output capacitor is charged which causes the voltage across it rising. The same situation applies to the switch S_4.

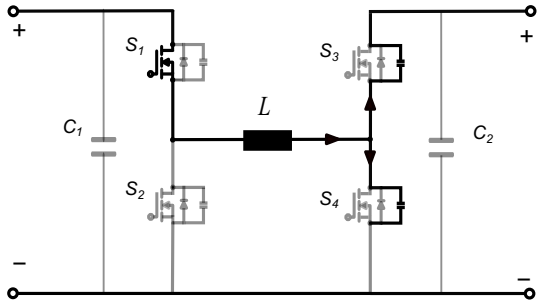
- $t_0^{'} < t < t_0^{''}$
  After time instant $t_1^{'}$, the current starts to flow on the output capacitor of switch S_2, and the output capacitor is discharged, and the voltage of midpoint will reach the zero at



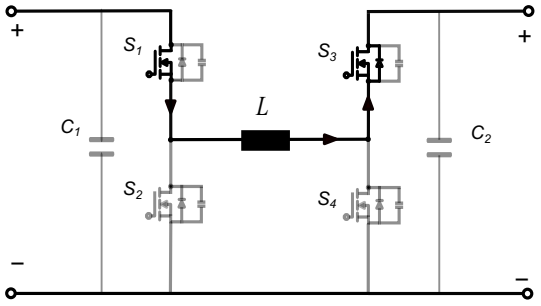
(a) Interval $t_0 \sim t_0''$.



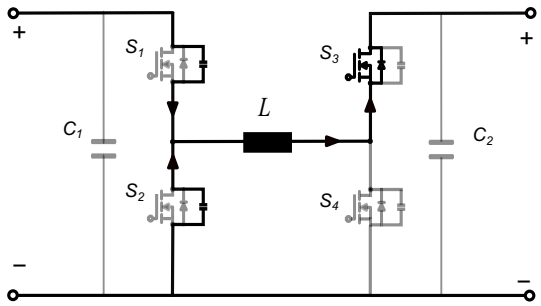
(b) Interval $t_0'' \sim t_1$.



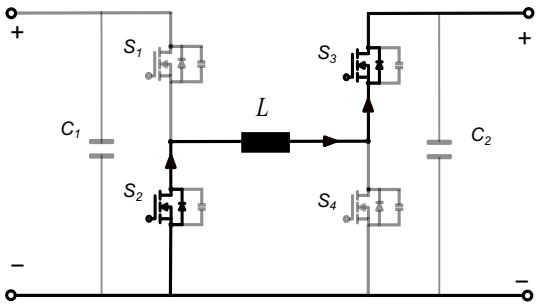
(c) Interval $t_1 \sim t_1''$.



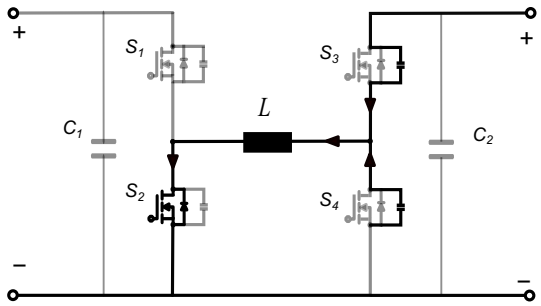
(d) Interval $t_1'' \sim t_2$.



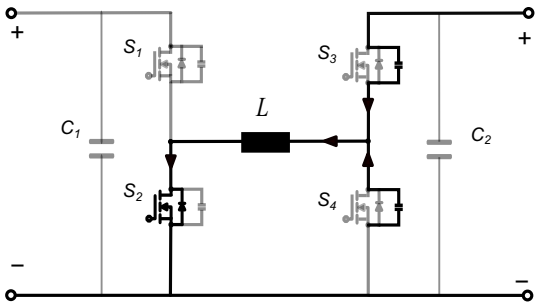
(e) Interval $t_2 \sim t_2''$.



(f) Interval $t_2'' \sim t_3$.



(g) Interval $t_3 \sim t_3''$.



(h) Interval $t_3'' \sim T$.

Figure 4.14: The path of the inductor current i_L during each time intervals (a) $t_0 \sim t_0''$. (b) $t_0'' \sim t_1$. (c) $t_1 \sim t_1''$. (d) $t_1'' \sim t_2$. (e) $t_2 \sim t_2''$. (f) $t_2'' \sim t_3$. (g) $t_3 \sim t_3''$. (h) $t_3'' \sim T$.

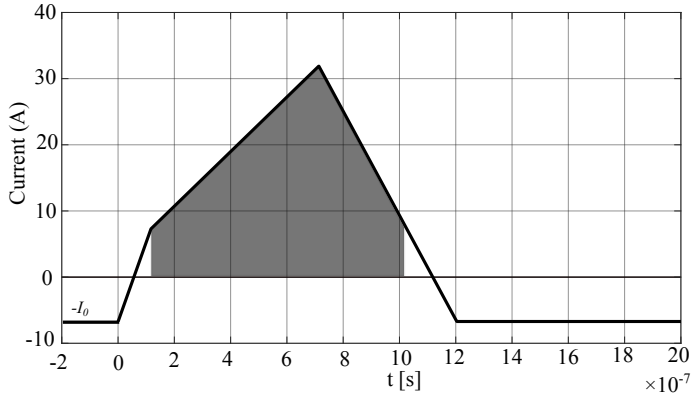
a certain time which drives the body diode of S_2 to conduct, now the transistor can be switched on at zero voltage. At the same time the switch S_3 is switched on at zero voltage condition.

- $t < t_2$
  Before the time instant t_2, the switch S_2 and S_3 are switched on, and a negative voltage $-V_{out}$ is applied on the inductor L causing the inductor decreases. The inductor current flowing from right to left side.

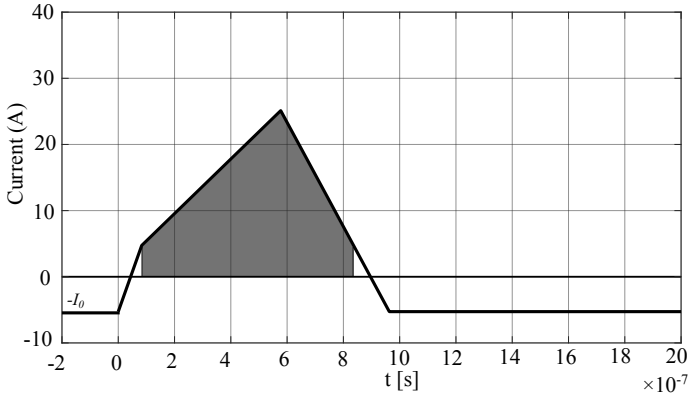
- $t_2 < t < t_2^{'}$
  At time instant t_2 the switch S_3 is open, the resistance of transistor channel is increased rapidly, and the current starts to flow on the parasitic output capacitance of S_4. The output capacitor is charged which causes the voltage across it rising.

- $t_2^{'} < t < t_2^{''}$
  After time instant $t_2^{'}$, the current start to flow on the output capacitor of switch S_4, and the output capacitor is discharged, and the voltage of midpoint will reach zero at a certain time which drives the body diode of S_4 to conduct, now the transistor can be switched on at zero voltage.

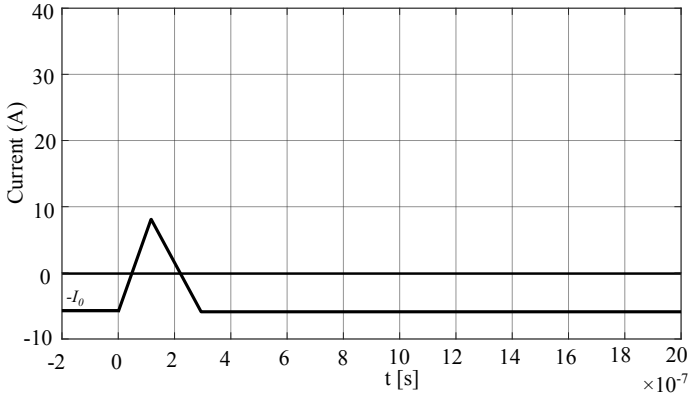
The power regulation principle shows in Fig. 4-15. In order to keep the current RMS value small, the interval $t_0 \sim t_1$ is kept as short as I_1 is large enough to ensure the zero voltage switching of switch S_3, and push the time instant t_3 to the end of each cycle to increase the transferred power. If an even larger power is required, the interval $t_0 \sim t_1$ is extended.. If a smaller power is required, the time instant t_3 is pushed to t_2 the average output current is decreasing, in other words, the transferred power is lower.



(a) $20kW$



(b) $10kW$



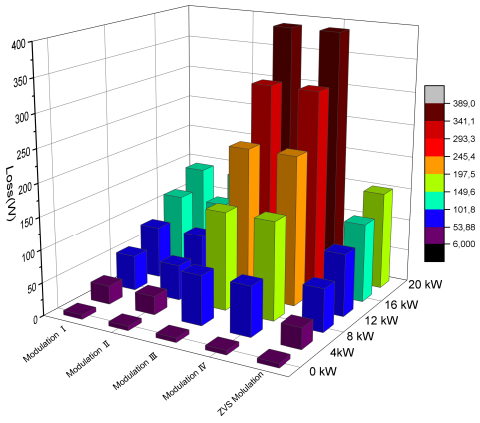
(c) $0kW$

Figure 4.15: Power regulation of ZVS modulation.

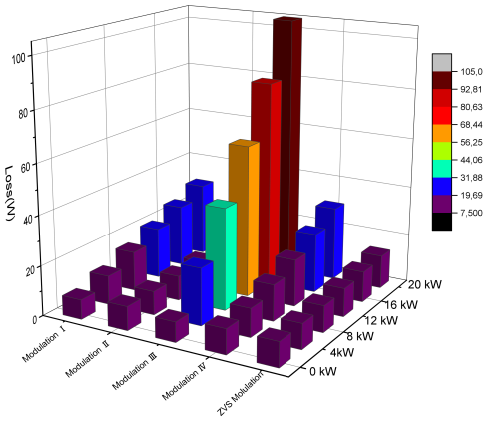
The zero voltage switching modulation can get rid of the large switching on losses on all four switches. Plus, in contrast to Modulation III and IV, the ZVS modulation does not have large reactive current which does not transfer power, and the peak current is relatively smaller. Switch S_2, S_3 and S_4 are switched off at the minimum zero voltage switching current $I_{zvs_{min}}$ which is always smaller than 10A. Therefore the losses swing on these three switches are not large.

4.6. Numerical Comparison

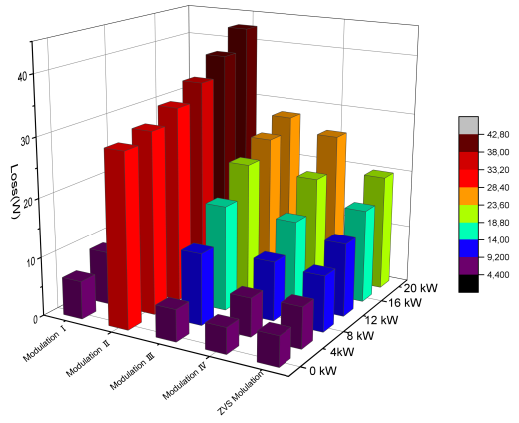
In order to determine an optimal modulation scheme, in terms of a low temperature swing in the semiconductor, high efficiency and smaller inductors, a numerical comparison is made according to the specific application ($V_{in} = 960V, V_(out) = 630V, 20kW$). Taking a 4-phase interleaved structure as an example, which means each phase transferred $5kW$. The inductor value in the following calculation is $8\mu H$, and a silicon carbide MOSFET $C2M0080120D$ is selected.



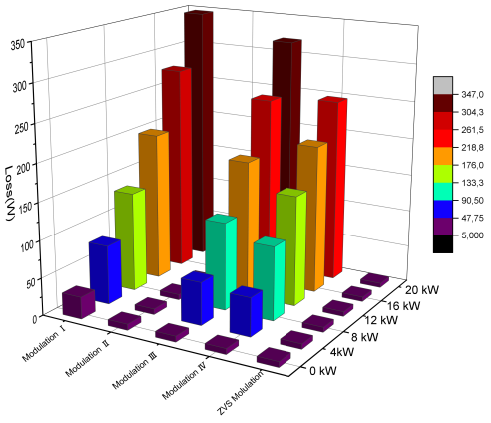
(a) Loss of switch S_1



(b) Loss of switch S_2



(c) Loss of switch S_3



(d) Loss of switch S_4

Figure 4.16: Losses on each switch in terms of different modulation scheme (a)S_1. (b)S_2. (c) S_3. (d)S_4.

Fig. 4-16(a) to Fig. 4-16(d) show the losses in each switch under different modulation schemes. According to the bar chart above, for Modulation I, switch S_4 has high losses and loss swings; for Modulation II, switch S_3 has high losses and losses swings; for Modulation III and Modulation IV, switch $S1$, $S2$ and $S4$ all suffer high loss swing. For ZVS Modulation scheme, all four switches suffer relatively low total losses and losses swing. Fig. 4-20 shows the inductor area product for each modulation. According to Fig. 4-17, the inductor size of the Modulation II always is always the smallest, and inductor size of ZVS modulation is also relatively small.

In conclusion, the ZVS modulation is the most suitable modulation scheme for this application.

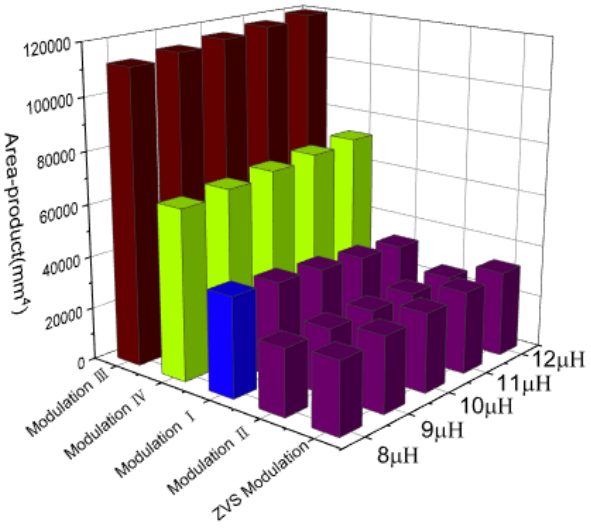
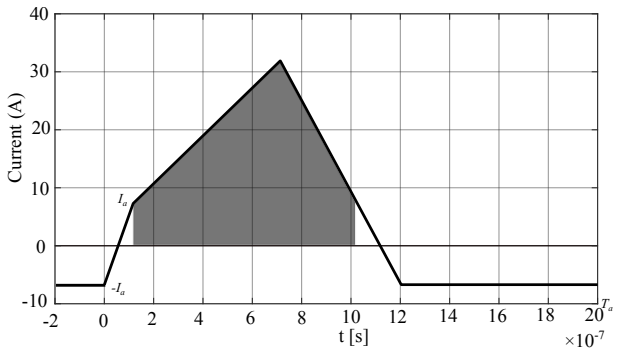


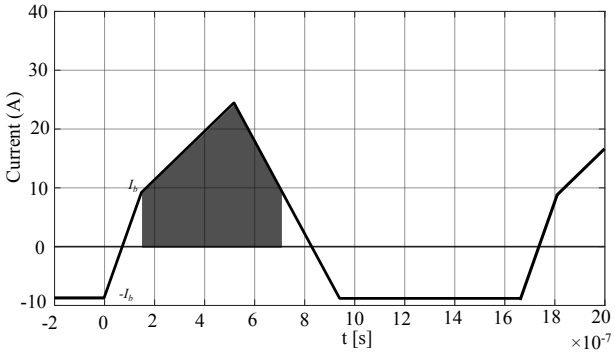
Figure 4.17: Inductor Area-product in terms of different modulation schemes

4.7. Modulation VI: Proposed low loss swing modulation

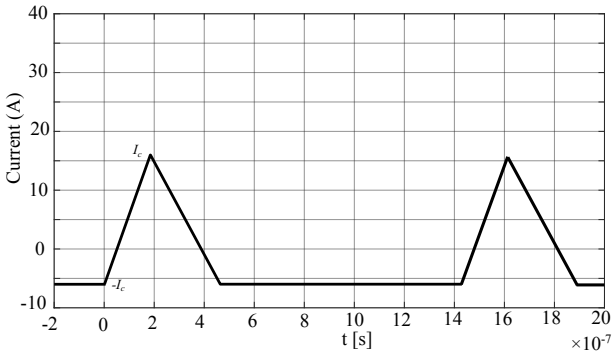
According to Fig. 4-16, for ZVS modulation scheme, switches also have a high loss swing, in order to further increase the life time of these four switches, a new modulation scheme is proposed. For S_1, the switching off losses is dominated, in order to reduce the loss swing in S_1, the offset current for zero voltage switching is increased as the transferred power decreases, then the loss swing on S_1 will be more flat. However, this will increase the loss swing on S_2, S_3 and S_4, hence, the switching frequency is increased, which reduces the conduction losses. Fig. 4-18 shows the operation of this proposed modulation scheme.



(a) 20 kW



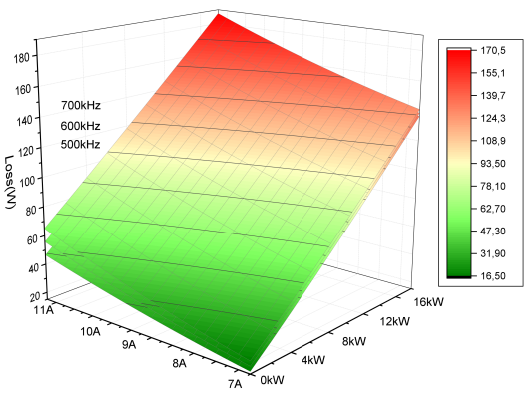
(b) 10 kW



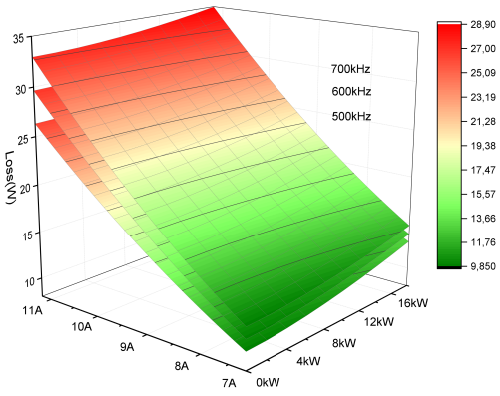
(c) 0 kW

Figure 4.18: Power regulation of the proposed low loss swing modulation.

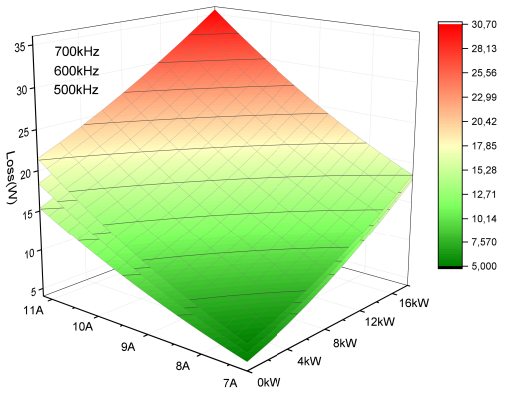
In Fig. 4-18,the power $P_1 > P_2 > P_3$, and as the power decreases, $I_a < I_b < I_c$, meanwhile, the switching frequency is increasing as the power decreases $T_a > T_b > T_c$. Hence, the losses changing will be flatter than ZVS modulation scheme. Although the S_4 is sacrificed due to a larger loss swing, it is still small.



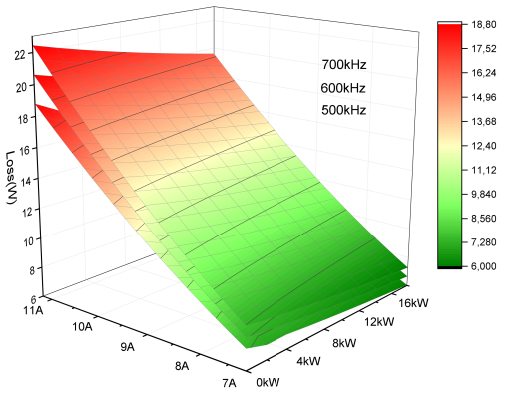
(a) Losses on S_1.



(b) Losses on S_2.



(c) Losses on S_3.



(d) Losses on S_4.

Figure 4.19: Losses on each switch for proposed low loss swing modulation scheme (a)S_1. (b)S_2. (c) S_3. (d)S_4.

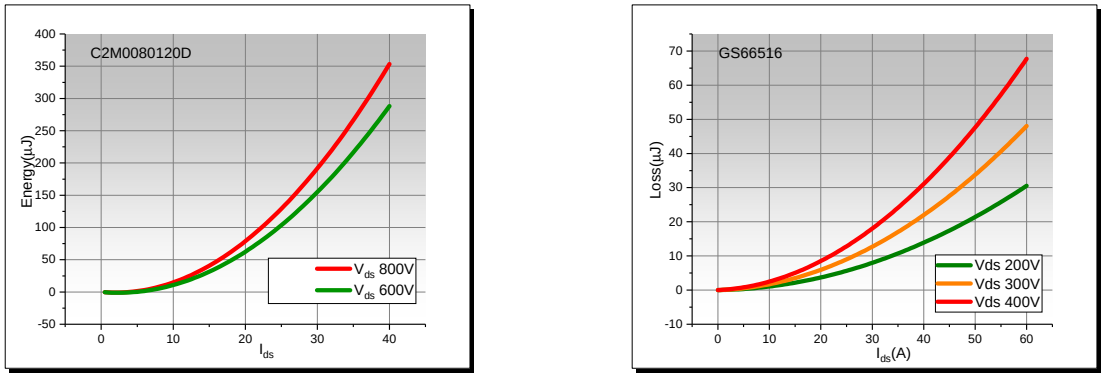
5

Power stage optimal designing

In this chapter, an optimal design of the four-switch buck-boost converter is described. It should be noted that the converter has two output voltage level ($360V$&$630V$), and both are taken into consideration in the optimal design. In order to get a high power density, normally, the multiphase structure is a common solution which reduces the output capacitance. High operating frequency is an other solution, however, a high frequency will cause high switching losses even if in zero voltage switching modulation. In order to have less losses and a longer life time, a two-stage structure is selected, in this case, $650V$ GaN switches can be used which further reduce losses. An optimal inductor design result is also illustrated in this chapter. The estimated efficiency, losses and temperature swing of the optimized four switch buck boost converter are given. A 3D modelling is also illustrated in this chapter, and based on it the power density estimation is given.

5.1. Two stage structure

The high side bus voltage is $960V$, a switch with $1200V$ drain to source voltage should be selected. However, all switches on the market with such a high drain to source voltage always have high switching losses. For instance, the SiC MOSFET used in Chapter IV $C2M0080120D$, when it is switched off at a high current the losses is very high which is impossible to design the cooling. If the drain to source voltage can be reduced, the switching losses also decrease at the same switching frequency. As shown in Fig.4-1, for instance, the data for the SiC MOSFET $C2M0080120D$ and the GaN FET $GS66516$ have a similar trend.



(a) Switching energy of C2M0080120D

(b) Switching energy of GS66516

Figure 5.1: Switching energy of C2M0080120D and GS66516

In order to reduce the drain to source voltage across the switch, the two-stage structure or multilevel structure can be implemented as Fig. 5-2 shows

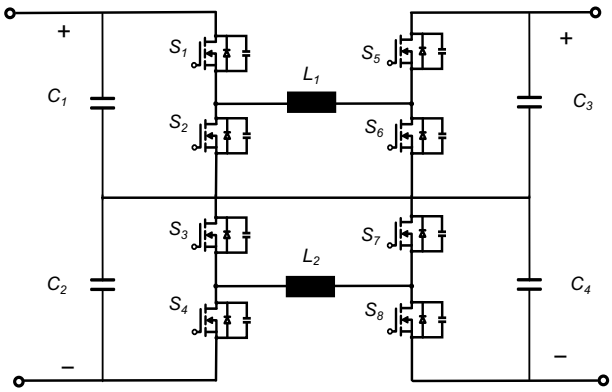
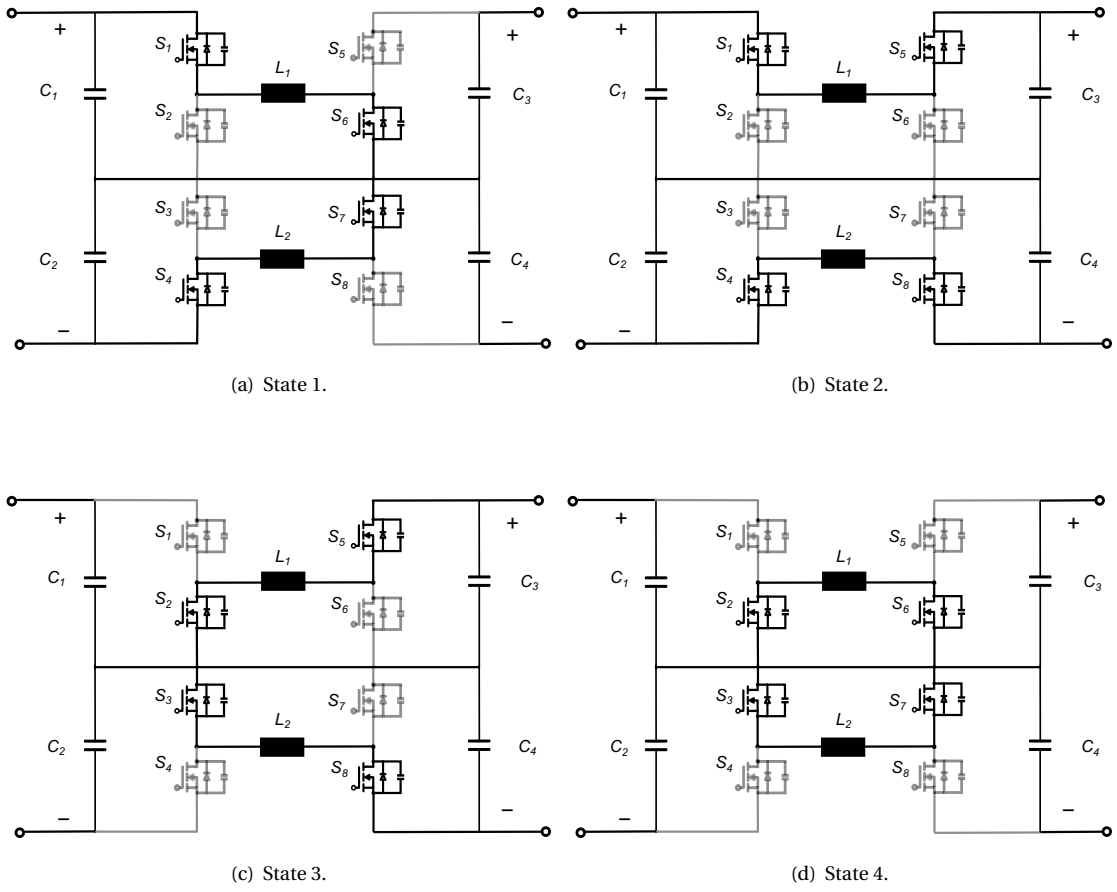


Figure 5.2: Two-stage four-switch buck-boost converter

Fig.5-3 shows the switching sequence of each switch.

- State 1 Switch S_1,S_6, S_7 and S_4 are switched on.
- State 2 Switch S_1,S_5, S_8 and S_4 are switched on.
- State 3 Switch S_2,S_3, S_8 and S_5 are switched on.
- State 4 Switch S_2,S_3, S_6 and S_7 are switched on.

If the upper and lower stage are balanced, the voltage across C_1 and C_2 are the same, no current is flowing on the neutral line. The voltage across each switch is half of the bus voltage which can do a large contribution to the reduce the losses on each switch.



(a) State 1.

(b) State 2.

(c) State 3.

(d) State 4.

Figure 5.3: Operation sequence of two-stage converter

In this case, a GaN transistor $GS66516T$ manufactured by $GaNSystem$ is selected due to its extremely low switching losses and relatively low conduction losses. It should be noted that although the GaN does not have a body diode, the devices are naturally capable of reverse conduction, an external diode is not required.

5.2. Interleaved structure

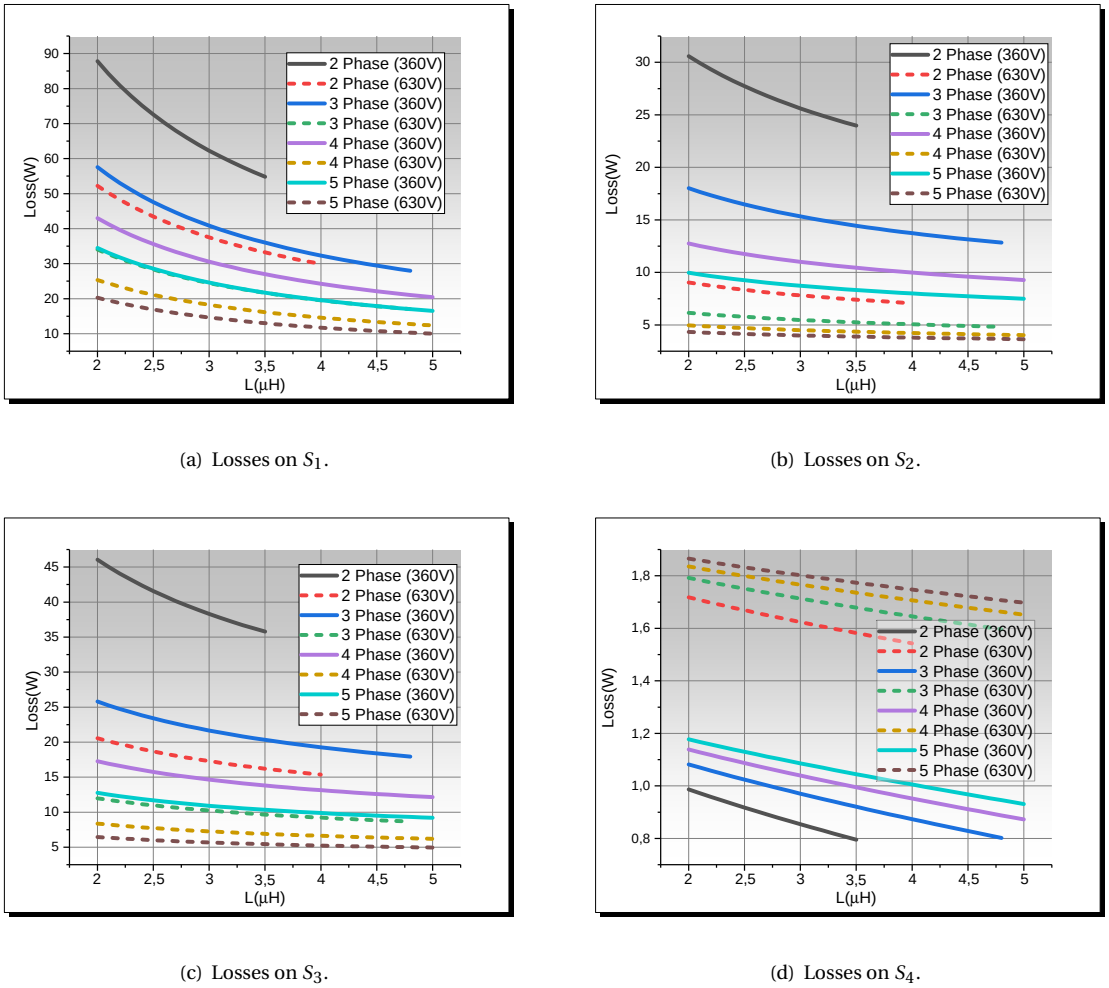
As been mentioned in the previous chapter, the interleaved structure has several advantages:

- The interleaved structure spreads the current stress on each switch, which reduces the losses on a single switch. For four-switch buck-boost converter in zero voltage switching modulation scheme, the interleaved structure mainly lowers the switching off losses of S_1, and lowers the conduction losses of S_2 and S_3

- The interleaved structure has output ripple cancellation. The ripple current is smaller depending on the duty cycle, and the ripple current frequency is n times of a single phase (n is the number of phases.). This effect reduces the stress on the whole filter

and the size of it.

The losses of each switch at full load ($20kW$) as a function of inductor value, regarding to the number of phases and two different output voltage ($630V, 360V$) are illustrated in Fig. 5-4



(a) Losses on S_1.

(b) Losses on S_2.

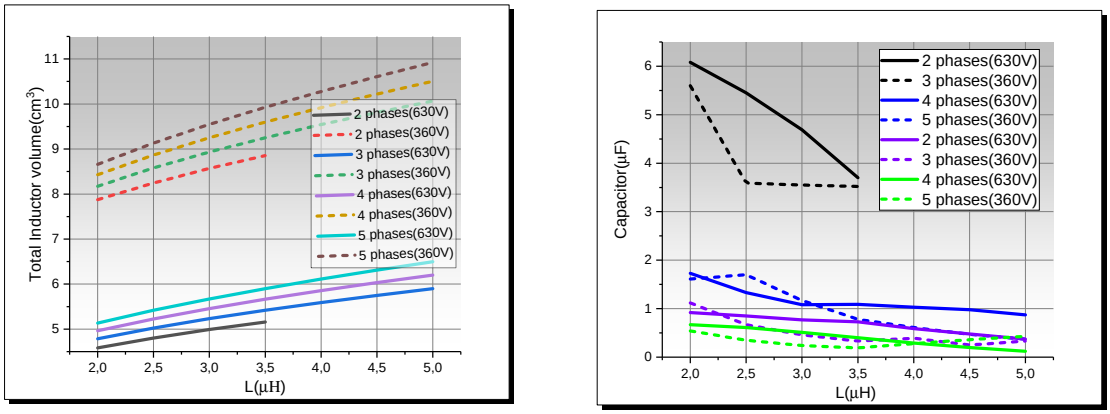
(c) Losses on S_3.

(d) Losses on S_4.

Figure 5.4: Losses of each switch (a)S_1. (b)S_2. (c) S_3. (d)S_4.

Fig. 5-5(a) shows the total inductor volume estimation as function of inductance value, in terms of different number of phases. Fig. 5-5(b) shows the required output capacitor to keep the ripple voltage $\Delta V < 2V$. These results are not like a multiphase buck converter whose output capacitor shows a linear relationship as a function of the duty cycle and number of phases as illustrated in Section 2.1. For multiphase four-switch buck-boost converter, the phase output current is irregular, and the total output current is also irregular, which makes it difficult to describe the relation between total output current and phase output current by a single equation.

According to the result illustrated in Fig. 5-5, although more number of phases leads to



(a) Total inductor volume estimation

(b) Required output capacitance

Figure 5.5: Total inductor volume and required capacitance

less losses on each switch, it also leads to higher total inductor volume and a large heatsink volume. In summary, three phases should be the optimal option.

It can be found from Fig. 5-4 that the losses on switch S_1 is still high when the output voltage is $360V$ especially, in order to further decrease the losses on switch S_1, an external capacitance is put in parallel to slow down the rising of the drain to source voltage as explained in Section 3.1. The value of the external capacitance is $100pF$.

The complete power stage circuit is illustrated in Fig. 5-8, a three-phase two-stage four-switch buck-boost converter. Each phase has a 120 degrees phase shift. The total output current and phase output current at $360V$ output with inductor value $4.5\mu H$ is shown in Fig. 5-8 from which we can see the total output current ripple is $9.5A$ while phase current ripple is $45.8A$. Fig. 5-7 shows the ripple current at $630V$ output voltage.

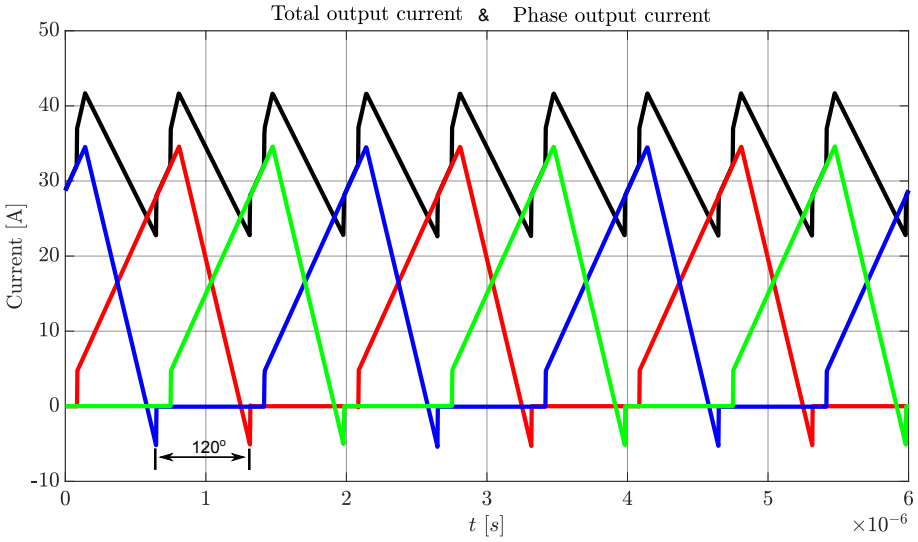


Figure 5.6: Phase current ripple and total output current ripple

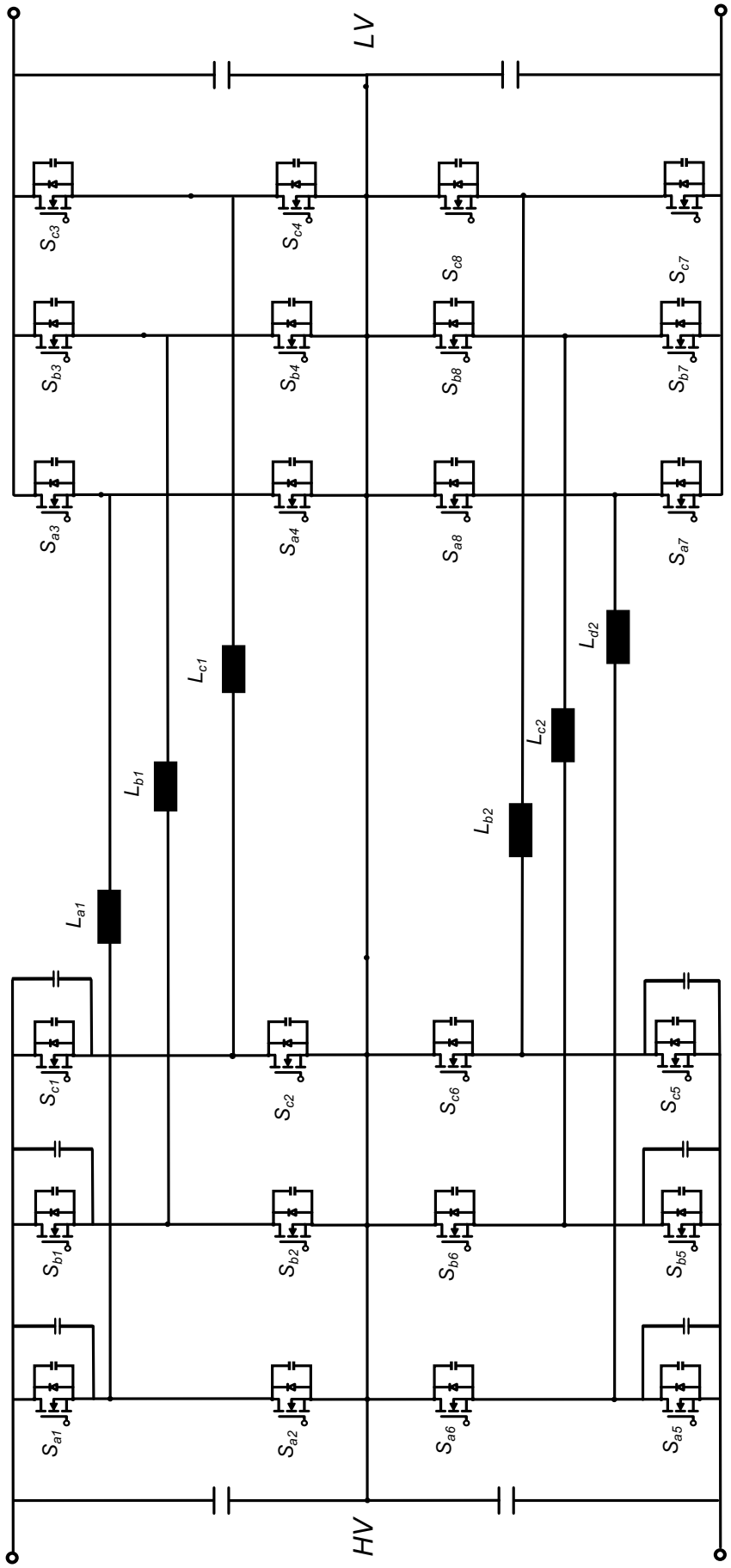


Figure 5.7: Overall Power stage structure

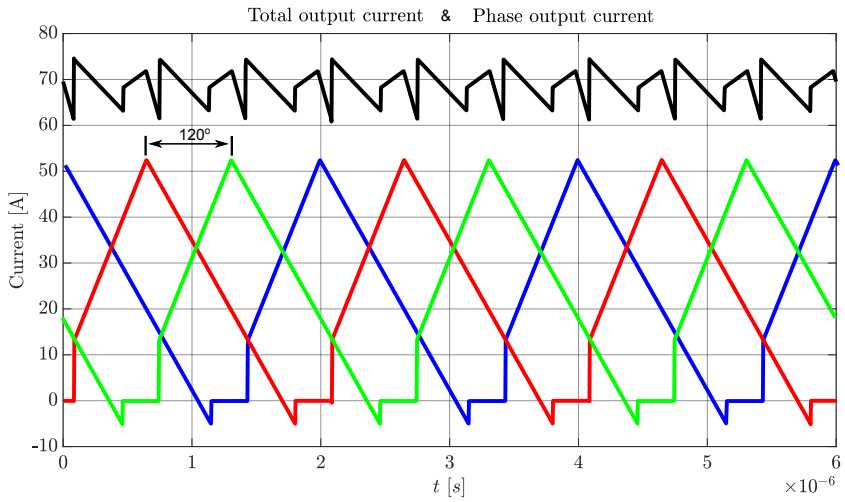


Figure 5.8: Phase current ripple and total output current ripple

5.3. Inductor design

According to the two-stage and interleaved structure, and based on the result from previous sections, an inductor around $4.5\mu H$ is designed. At first, the a suitable material should be selected, especially the operation frequency is up to $500kHz$. Referring to the documents provided by manufacturers, $N49$ and $3F36$ is suitable for high frequency and high power application. A EELP 58/11/38 core is selected after comparison in terms of size and core loss density. Parameters are given in Table. 5-1. Fig. 5-10 shows the designed inductor in finite element simulation software.

Inductance L	4.54 μH
Material	N49
Effective magnetic cross section	310 mm^2
Effective magnetic path length	80.7 mm
Effective magnetic volume	25000mm^3
Litz wire	0.05mm ×2800
Number of turns	4
Air gap length	2mm

Table 5.1: Inductor parameters

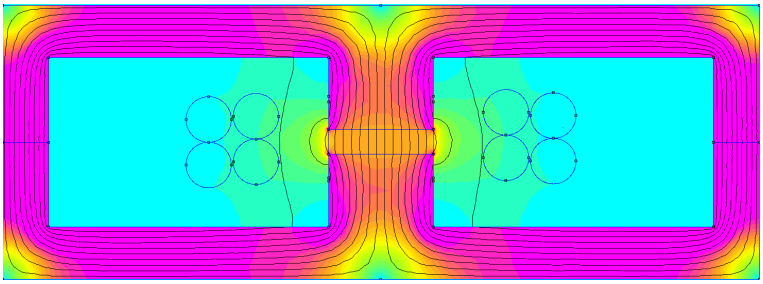


Figure 5.9: 2D cross section of designed inductor

5.4. Thermal consideration

Water cooling will be used in this converter. The selected GaN switch $GS66516T$ is a top side cooling device, so the topside is pasted on the cooling plate as illustrated in Fig. 5-9. The heat is transferred from the device junction to the water cooling plate through junction-to-case and thermal interface material. The thermal resistance of junction to case is $R_{jc} = 0.3°C/W$. The manufacturer recommends several different designs, the corresponding thermal resistance calculating by Eq. 3-56 are illustrated in Table. 5-2, provided by [7].

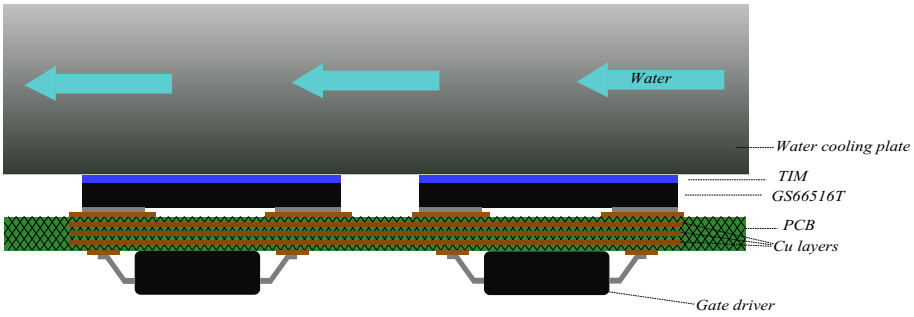


Figure 5.10: Total current ripple and phase current ripple corresponding to 360V

In order to reduce the size, the gate driver circuit can be put at the other side of the PCB, usually vias are not existing in this case. The thermal resistance through junction-to-board and board-to-ambient is very large, this heat transfer path can be neglected (two transfer paths are in parallel). The temperature of the water cooling plate can be assumed to be constant, hence, the junction temperature can be estimated by

$$T_j = T_{plate} + (R_{jc} + R_{TIM})P_{loss} \tag{5.1}$$

5.5. Overall efficiency ,temperature swing and power density estimation

At heavy load the switching frequency is $500kHz$, and the negative offset current is $-6.5A$. At light load assuming the switching frequency is increased to $700kHz$, and the negative

	SIL-PAD K-4	SIL-PAD 1500ST	GAP3000S30	HI-FLOW 300P	GAPFILLER GS 3500S35-07
TIM Thickness (mm)	0.152	0.203	0.25	0.102	0.178
Thermal conductivity ($W/m \cdot K$)	0.9	1.8	3.0	1.6	3.6
Thermal resistance ($^\circ/W$)	4.12	2.94	2.29	1.84	1.49

Table 5.2: Recommended TIM design

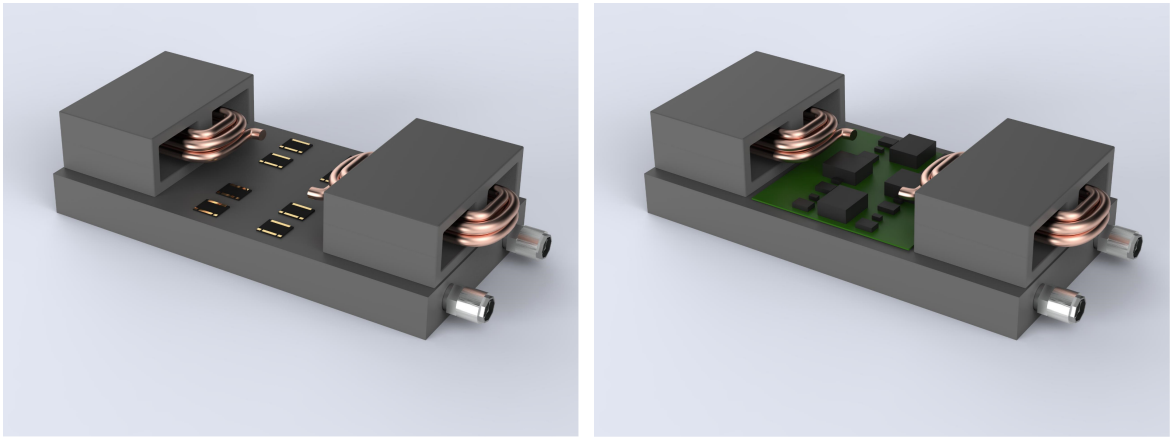
offset current is increased to $-10A$. Losses of each switch, temperature swing, core losses, winding losses and overall efficiency in terms of two output voltage value are given in the table below. For other modulation schemes, the efficiency and temperature are illustrated in Appendix A.

	630V		360V	
Core losses (W)	4.01		4.77	
Winding losses (W)	3.85		7.88	
	P_{max} (W) & T_{max} ($^\circ C$)	ΔT ($^\circ C$)	P_{max} (W) & T_{max} ($^\circ C$)	ΔT ($^\circ C$)
$S1$	13.1 & 58.7	8.5	20.9 & 56.2	14.3
$S2$	7.8& 36.2	3	14.5 & 51.1	13.7
$S3$	9.8 & 42.6	10.3	19.8 & 54.5	16.8
$S4$	4.3 & 32.7	2.7	1.1 & 29.0	2.2
Overall efficiency in $20kW$	98.5 %		97.7 %	

Table 5.3: Overall losses, temperature and efficiency

A 3D modelling of one phase of this converter is illustrated in Fig .5-12, inductors and

switches are pasted on the water cooling plate, and PCB board are on the top of the plate.



(a) (b)

Figure 5.11: 3D modelling of one phase

The size of one phase is $13.5cm \times 6.3cm \times 3.6cm$ and the total power stage volume is $0.96L$. The capacitor is selected to be 2 DC link film capacitors $B32774P$ with total volume $0.044L$. In addition, a control board and other auxiliary components are required, assuming the volume of these components are $0.2L$. Hence, the power density can be estimated to be $16.6kW/L$.

6

Close loop control

In this chapter, the close-loop control of the four-switch buck-boost is introduced. Firstly, Section 6.1 shows the overview of the close-loop control block. The control principle is introduced in Section 6.2. Since the power stage is a two-stage structure, a balancing controller is required to keep the voltage balance of the high and low stage which is explained in Section 6.3. The duty cycle of each interval is determined by the transferred power, and it is calculated instantly with the input and output voltage and output current, the way how to calculate those duty cycles is explained in Section 6.4. Furthermore, in order to ensure the zero voltage switching, the zero crossing detection is implemented, and the principle and function of it are introduced in Section 6.5, and a basic zero crossing detection circuit is illustrated. In Section 6.6, close-loop control simulation results are given.

6.1. Overview of close-loop control structure

Fig. 6-1 shows the block diagram of the close-loop control. The output voltage is the set value, and the input and output voltage and output current are measured. The current zero crossing signal is also detected which is used to ensure the zero voltage switching. A balancing control loop (differential loop) by which the high stage and low stage can be balanced is also included, hence, the midpoint voltage is also measured. Filters are required to reduce the noise before signals going into the ADC. Those signals are feedback to the FPGA or micro-controller. A current mode control strategy is implemented to generate a target output current. The input voltage, output voltage and target output current are going to the duty cycle calculator whose results are input to modulation block. The Table. 6-1 shows the signal corresponding to Fig. 6-1.

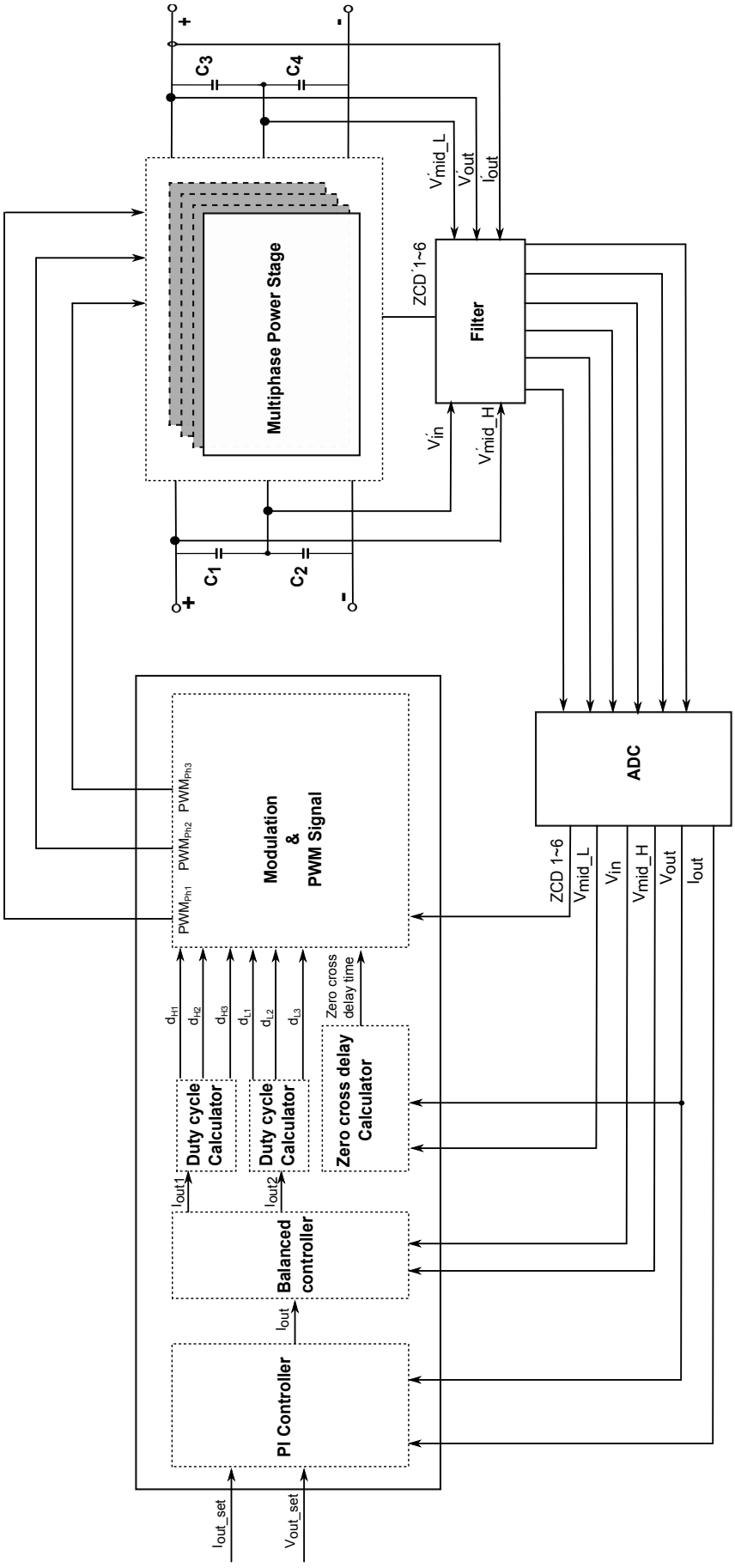


Figure 6.1: Overview of close-loop control

$V_{out}^{'}$ & V_{out}	Output voltage analog and digital signal
$V_{mid_L}^{'}$ & V_{mid_L}	Low side midpoint voltage analog and digital signal
$I_{out}^{'}$ & I_{out}	Output current analog and digital signal
$ZCD^{'}1 \sim 8$ & $ZCD1 \sim 8$	Zero cross detection analog and digital signal
$V_{in}^{'}$ & V_{in}	Input voltage analog signal and digital
$V_{mid_H}^{'}$ & V_{mid_H}	High side midpoint voltage analog and digital signal
$I_{out_{set}}$	Output current set value
$V_{out_{set}}$	Output voltage set value
d_{H1}&d_{H2}&d_{H3}	High stage duty cycle
d_{L1}&d_{L2}&d_{L3}	Low stage duty cycle
PWM_{Ph1}&PWM_{Ph2}&PWM_{Ph3}&PWM_{Ph3}	PWM signal of each phase

Table 6.1: Signals corresponding to Fig-6.1

6.2. Current mode control

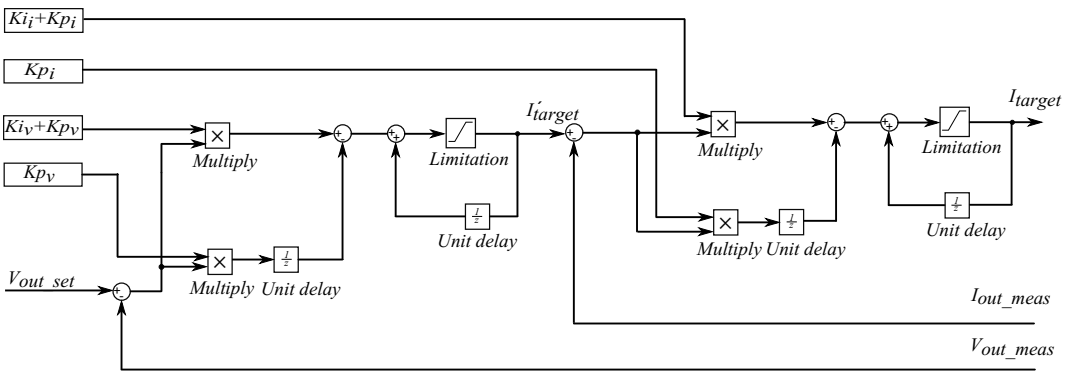


Figure 6.2: Current mode control

Fig. 6-2 shows the current mode controller in $z-domain$. In this controller, the output voltage V_{out_set} is the set value. The outer loop is the voltage loop and the inner loop is the current loop and these two loops constitute a cascade control strategy. The transfer function of the PI controller there can be derived step by step as below, taking the current loop as the example

$$I^{'}(z) = I_{error}(z) \times (Ki_i + Ki_p) - I_{error}(z) \times Ki_p \times \frac{1}{z} \tag{6.1}$$

$$I^{'}(z) + \frac{1}{z} \times I_{target}(z) = I_{target}(z) \tag{6.2}$$

$$I_{error}(z) = I^{'}_{target} - I_{out\_meas} \tag{6.3}$$

Substituting the $I^{'}(z)$ in Eq.6-2 with Eq.6-1, than we can get the transfer function of the controller, and it is very clear this controller is a PI controller.

$$H(z) = \frac{I_{out}(z)}{I_{error}(z)} = Ki_i \frac{z}{z-1} + Ki_p \tag{6.4}$$

Where:
- Ki_i is the current loop integrate coefficient.

- $P_{P,L,i}$ is the current loop proportional coefficient.

6.3. Balance controller

Ideally, the voltage across the input capacitor C_1 and C_2 are the same which is half of the bus voltage $V_{bus}/2$, and the high stage and low stage will work evenly. However, in practice, it is possible that the voltage across the capacitors C_1 would be pulled away by C_2 (vice versa), which might higher than the switches break down voltage. Switches, even the whole system, will be damaged by this phenomenon. Therefore, a balance controller is required. For instance, if the voltage V_{C_1} is higher than voltage V_{C_2}, more power should be transferred by the high stage, vice versa.

Fig. 6-3 shows the structure of the balancing controller. The input bus voltage and the voltage across the capacitor C_2 are measured and feedback to the controller. The difference value of half of the bus voltage and voltage V_{C_2} are compensated by a PI controller. This value is either add or subtract to the main controller output which is input into the duty cycle calculator.

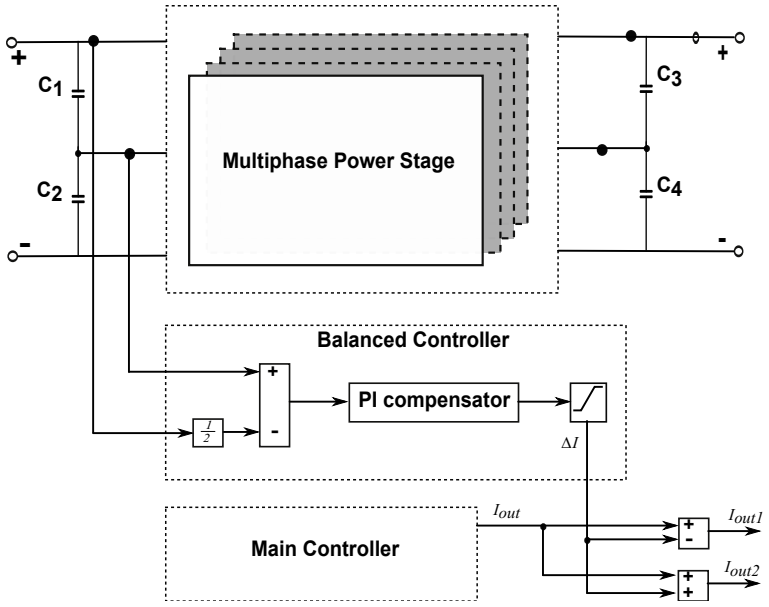


Figure 6.3: Balance controller

6.4. Duty cycle calculation

The zero voltage switching modulation scheme is illustrated below. Defining duty cycle of the interval between time instant $0 \sim t_1$ as d_1, $t_1 \sim t_2$ as d_2, $t_2 \sim t_3$ as d_3 and $t_3 \sim T$ as d_4. As be discussed in chapter 4, in this modulation, when the power required is below a certain value, the duty cycle of the first interval is kept constant, but increasing d_2 and d_3 correspondingly until $d_1 + d_2 + d_3 = 1$ (time instant t_3 reaches the end of the cycle.). In this condition, d_1 is calculated by

$$d1 = \frac{(I_1 - I_0)L}{V_{in}} \tag{6.5}$$

The average output current be derived by

$$I_{out} = \frac{(I_1 + I_2)d_2T}{2} + \frac{(I_2 + I_0)d_3T}{2} \tag{6.6}$$

$$d3 = \frac{(I2 - I0)L}{TV_{out}} \tag{6.7}$$

where I_1 and I_2 can be derived by

$$I_1 = I_0 + \frac{V_{in}d_1T}{L} \tag{6.8}$$

The duty cucle d_3 is calculated by

$$I_2 = I_0 + \frac{(V_{in} - V_{out})d_2 T}{L} + \frac{V_{in} d_1 T}{L} \tag{6.9}$$

Substituting I_1, I_2 and $d3$ in Eq. 6-5 with Eq. 6-6, Eq. 6-7 and Eq. 6-8, and solve the second order formula as a function of d_2,

$$d2 = -\frac{I_0 L + d_1 T V_{in} - \frac{\sqrt{I_0^2 L^2 V_{in} + 2 d_1 I_0 L T V_{in} V_{out} + d_1^2 T^2 V_{in}^2 V_{out}}}{\sqrt{V_{in}}}}{T(V_{in} - V_{out})} \tag{6.10}$$

Once the required output current is large than a certain value, in an other word, t_3 reaches the end of the cycle, then increase d_1, as illustrated in Fig. 6-5. In this case, the average output current can be calculated by

$$I_{out} = \frac{(-I_0 + I_1)(d_1 - \frac{-2I_0 L}{VT})}{2} + \frac{(I_1 + I_2)d_2}{2} + \frac{(I_2 + I_0)d3}{2} \tag{6.11}$$

In Eq. 6-10 I_1 and I_2 are the same with Eq. 6-7 and Eq. 6-8, and $d3 = 1 - d1 - d2$, hence, the three duty cycle is

$$d1 = -\frac{I_0 L V_{in} - 2TV_{out}^2 + \sqrt{V_{in}(I_0^2 L^2 V_{in} + 4I_0 LTV_{out}(2V_{in} + V_{out}) + 4TV_{out}(TV_{in}V_{out} - 2I_{out}L(V_{in} + V_{out})))}}{2TV_{out}(V_{in} + V_{out}))} \tag{6.12}$$

$$d2 = \frac{I_0 L V_{in} + \sqrt{I_0^2 L^2 V_{in}^2 + 4TV_{in}V_{out}(2I_0 LV_{in} + 2I_{out}LV_{in} + I_0 LV_{out} - 2I_{out}LV_{out} + TV_{in}V_{out})}}{2TV_{in}V_{out}} \tag{6.13}$$

$$d3 = -\frac{I_0 L V_{in} - 2TV_{in}^2 + \sqrt{Vin(I_0^2 L^2 V_{in} + 4I_0 LTVout(2Vin + Vout) + 4TV_{out}(TV_{in}V_{out} - 2I_{out}L(V_{in} + V_{out})))}}{2TV_{out}(V_{in} + V_{out}))} \tag{6.14}$$

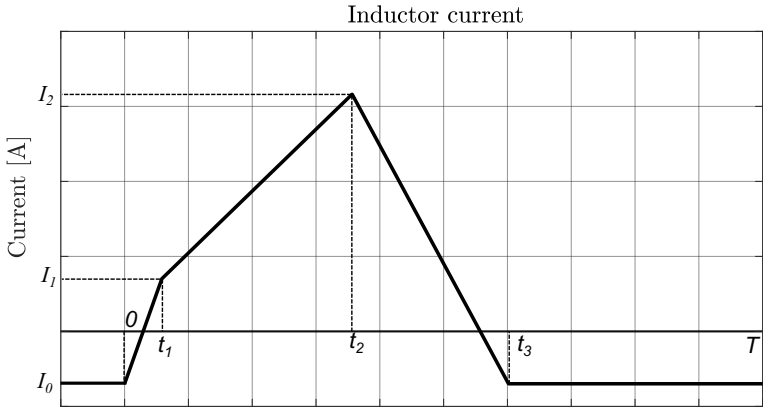


Figure 6.4: Illustration of each duty cycles

6.5. Zero cross detection

In order to ensure the zero voltage switching of the switch S_1, enough negative offset current, as I_0 illustrated in Fig. 6-4, is required to charge and discharge the leg capacitance. Although the duty cycle is calculated which should be able to reach the current ideally. However, in reality, it might be either larger or smaller than the required value due to the hardware delay time or some other non-ideal conditions. Hence, other way should be taken to make sure the negative offset current is enough. The zero crossing detection is always used.

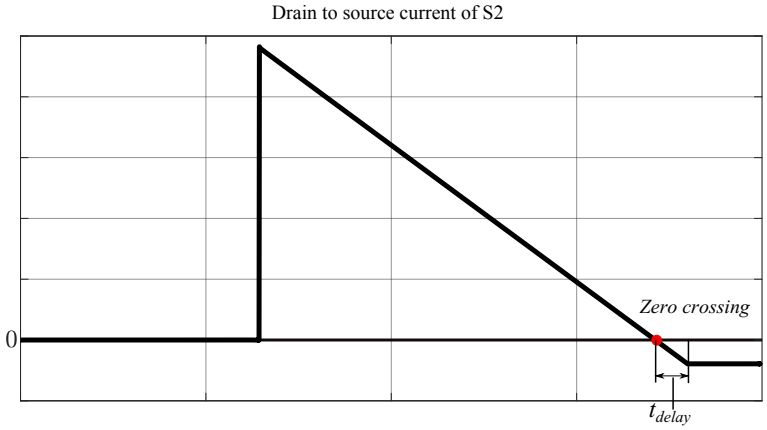


Figure 6.5: Illustration of zero crossing detection

Fig. 6-5 shows the drain to source current of switch S_2, and there is a point where the drain to source current is crossing zero. After this zero crossing point, this state will still last for a time interval t_{delay} which can be calculated by

$$t_{delay} = \frac{I_0 L}{V_L} \tag{6.15}$$

After t_{delay}, the we can ensure the I_0 is reached. Then the zero voltage switching is ensured. To detect the zero crossing point, a resistor is put at the source of switch S_2 and at the drain side of S_3, as illustrated in Fig. 6-6

The zero crossing detection topology is illustrated in Fig. 6-7. An operational amplifier is used to amplify the resistor voltage zero crossing, and it is input to a comparator. The output of the comparator is going to the controller through an isolated level shifter.

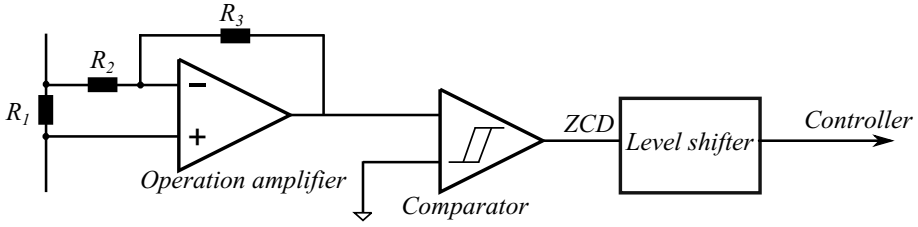


Figure 6.7: Illustration of ZCD principle

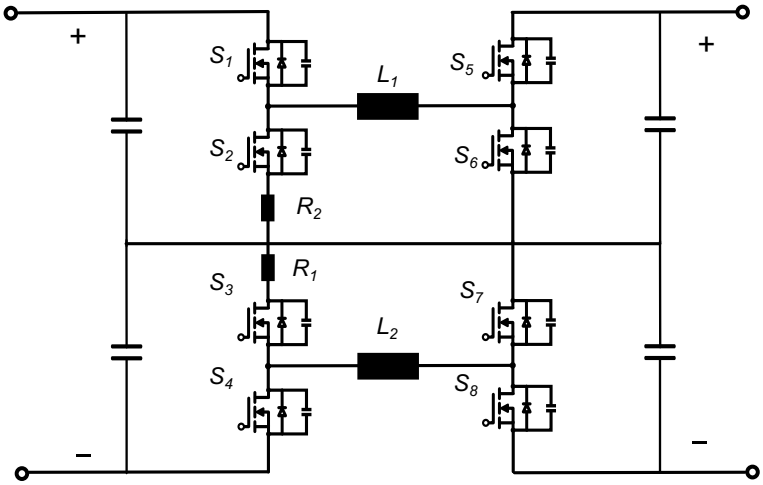


Figure 6.6: Illustration of ZCD principle

6.6. Simulation result

The simulation results of close-loop control are illustrated in Fig. 6-7 and Fig. 6-8 in terms of $630V$ and $360V$ output respectively.

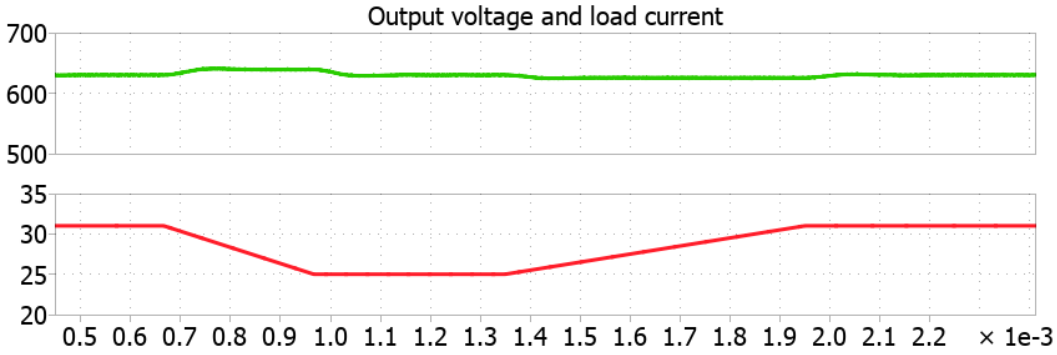


Figure 6.8: Close loop control simulation result in terms of 630V output

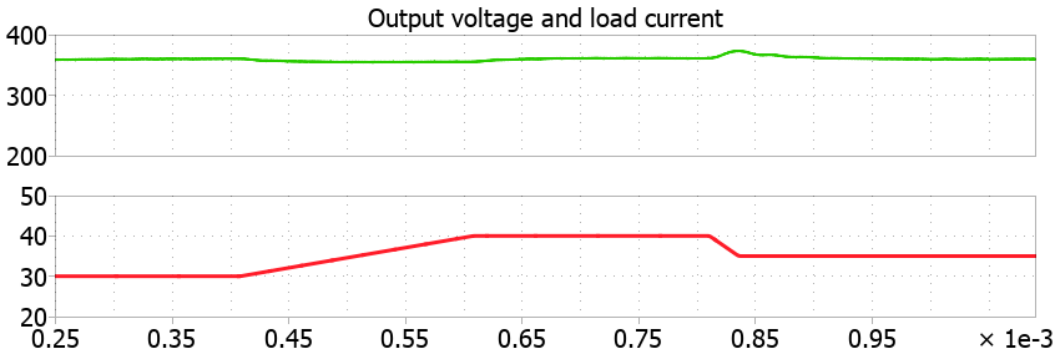


Figure 6.9: Close loop control simulation result in terms of 360V output

Fig. 6-10 illustrates the simulation results of balance control. The inductor value of high

stage is set to be larger than the low stage inductor, so the voltage is pulled by the high stage as illustrated in Fig. 6-10. Before $t = 2.2ms$ when the balance control is not enabled, after this time instant, two voltage values become equal because the balance control is enabled.

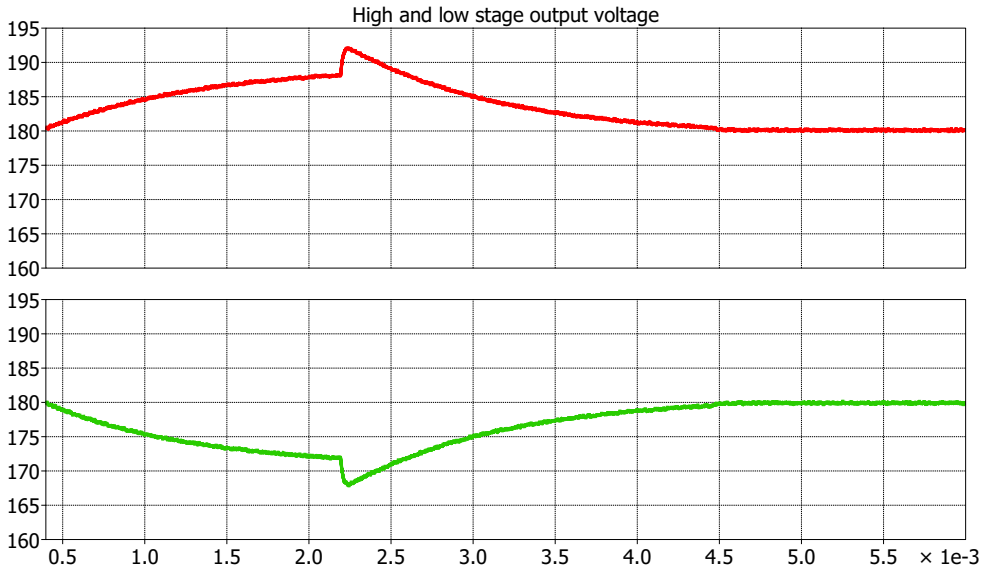


Figure 6.10: Balance control simulation result

7

Testing and Measurement

A two-phase four-switch buck-boost converter (48/12) is used to verify the performance prediction, in terms of the zero voltage switching and the proposed modulation scheme.

7.1. Testing setup

Fig. 7-1 shows the basic structure of the testing prototype, a two-phase interleaved four-switch buck boost converter which converter 48 volts to 12 volts with maximum 40A output (During testing, the maximum current is limited to 20A). The Table. 7-1 gives some key parameters of this prototype.

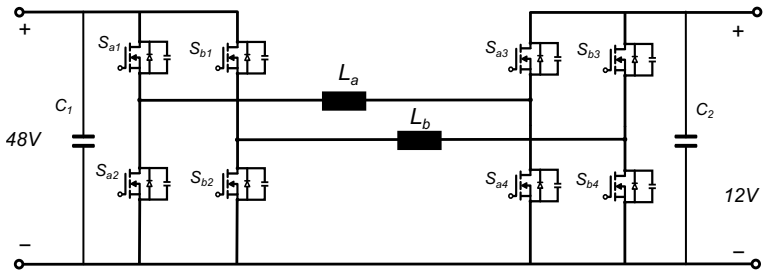


Figure 7.1: Prototype structure

Fig. 7-2 illustrates the testing setup in the lab, and Fig.7-2 illustrates the equivalent diagram. The high voltage side is connecting to a power supply ($0 \sim 200V, 0 \sim 210A, 0 \sim 15kW$), and the low voltage side is connecting to an electrical load ($0 \sim 80V, 0 \sim 300A, 0 \sim 2.6kW$). The parameters in the micro-controller can be changed with UART interface.

S_1&S_2	STL135N8F7AG
S_3&S_4	STL190N4F7AG
Inductor core	EELP38
Core material	N95
Inductance value	$1.45\mu H$
Litz wire	0.071×821

Table 7.1: Prototype specification

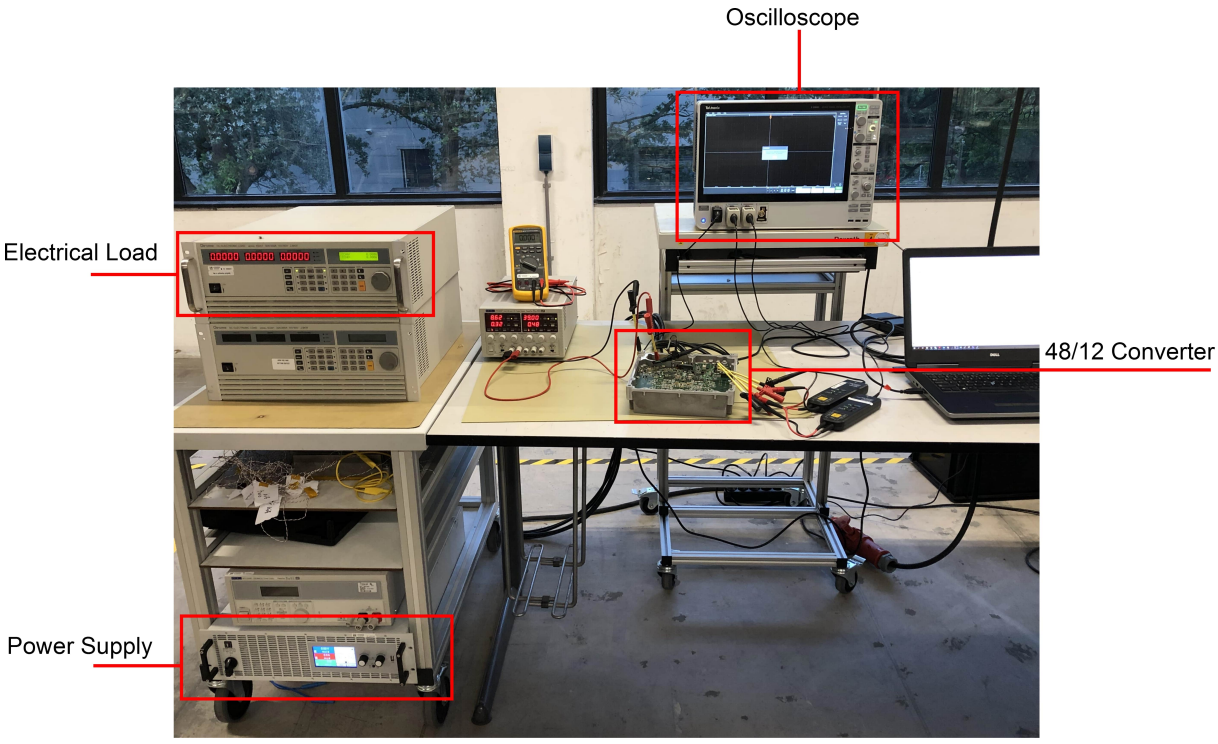


Figure 7.2: Measurment setup

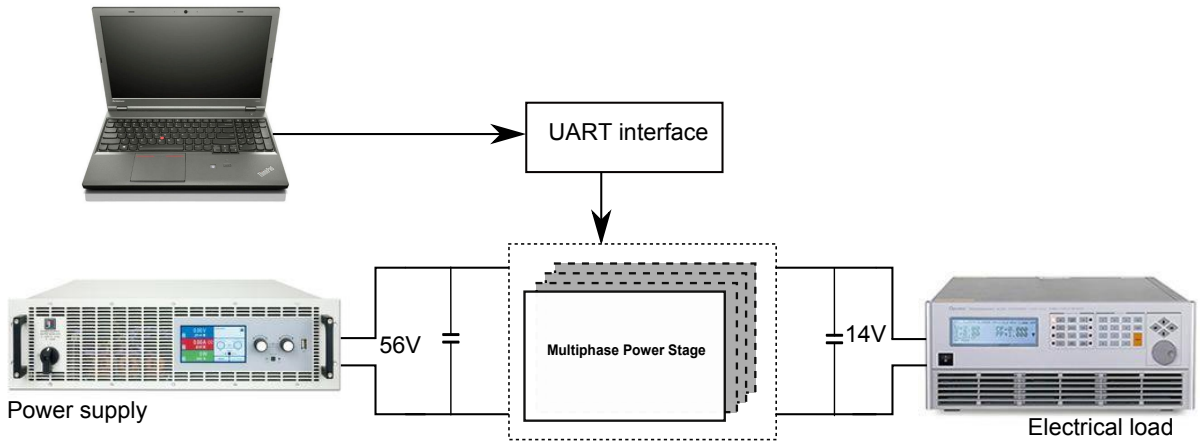


Figure 7.3: Measurment setup

7.2. Experimental Results

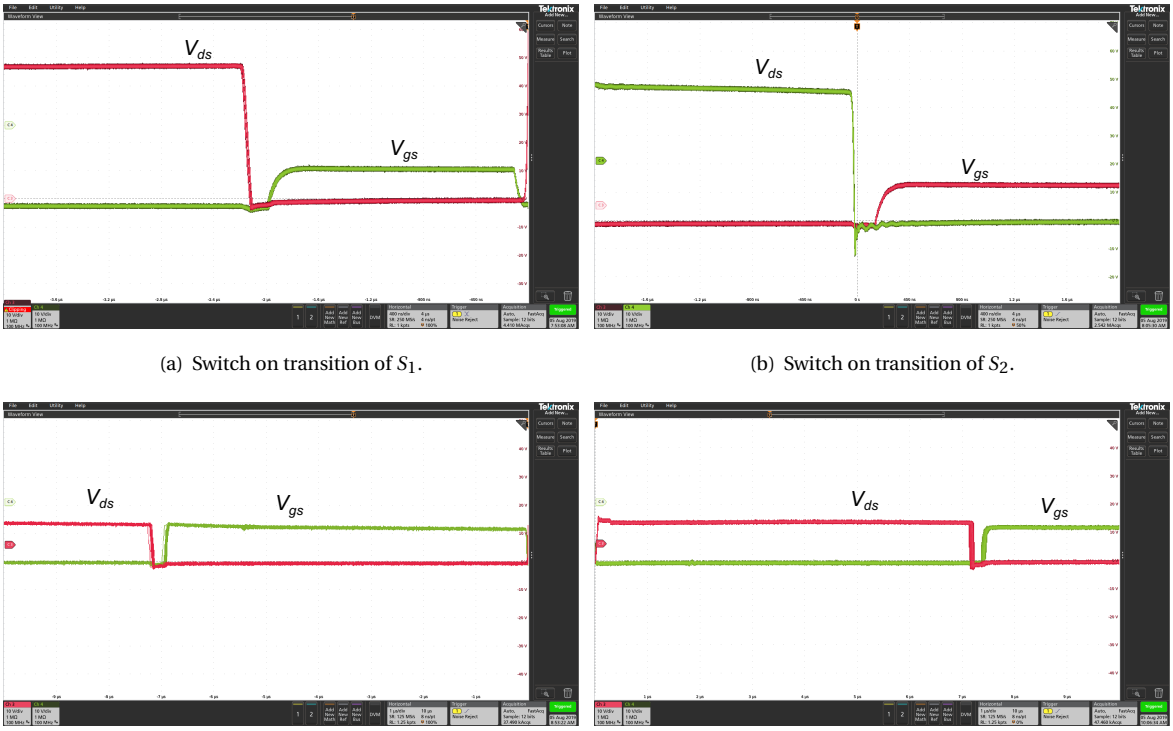
In this section, the experimental results of the 48/12 two-phase four-switch buck-boost converter are shown.

The voltage across the inductor is illustrated in Fig. 7-4. There are four voltage levels which shape the inductor current to be as zero voltage switching modulation.

Figure 7.4: Inductor voltage waveform

Fig. 7-5 shows the drain to source and gate to source voltage of those four switches in the first phase (The red waveform is drain to source voltage V_{ds}, the green waveform is gate to source voltage V_{gs}). As illustrated, the gate voltage always rises after the drain to source voltage reaches zero, hence, all four switches can reach zero voltage switching.

Fig. 7-6 shows the overall converter losses as a function of output power and different I_0(the current at the beginning at each cycle as illustrated in Fig .6-4. As illustrated, the overall losses is increasing as the output power increases. In addition, the overall losses is also



(a) Switch on transition of S_1.

(b) Switch on transition of S_2.

(c) Switch on transition of S_3.

(d) Switch on transition of S_4.

Figure 7.5: Switch on transition of each switch (a)S_1. (b)S_2. (c) S_3. (d)S_4.

increasing as the I_0 increases.

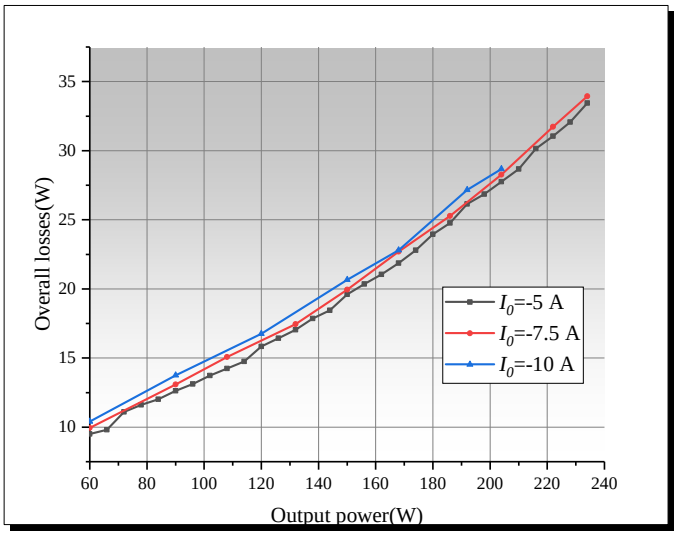


Figure 7.6: Experimental data

However, as illustrated from the measurement result, the difference is quite limited, it can be explained by the following reason:

- Firstly, the voltage rate of the prototype is low ($48V$&$12V$), and the switching frequency of the prototype is low as well ($65kHz$). Hence, the switching frequency is quite small. When I_0 is enlarged, the switching losses increment is very limited.
- Secondly, the MOSFET used in the prototpye is $STL135N8F7AG$ which has a extremely low on-state resistance (typical value $3.15m\Omega$), through RMS current is enlarged when the I_0 is increased, the conduction losses do not increase much either.

8

Summary and Outlook

In this chapter, a summary based on the information presented in the previous chapters is given.

8.1. Summary

The aim of this thesis is to design a high power density DC/DC converter for high dynamic application. The DC/DC converter is implemented to drive the high dynamic motors in the wafer stage.

First, due to the highly dynamic application, a suitable topology four-switch buck-boost converter is selected. The four-switch buck-boost converter has high flexibility, it can work in several modes such as buck mode, boost mode and buck-boost mode. The most important feature, compared to the conventional buck converter, boost converter, it can offer a free-wheeling interval in which no voltage is applied on the inductor. As a result, the power can be regulated by adjusting the duty cycle of a free-wheeling interval to overcome of the drawbacks of synchronous conduction mode and triangular current mode. Secondly, compared to conventional Si MOSFET and IGBT, new generation wide bandgap semiconductor devices can achieve higher switching frequencies due to low parasitic parameters, as a result, wide bandgap semiconductor devices are suitable for the application in this thesis.

In four-switch buck-boost converter, it is possible to implement a zero voltage switch method without any auxiliary component. If a large enough amount of charge can be provided by the inductor current to charge the leg capacitance, the diode will take over the current before the transistor is turned on, and it can be turned on at zero voltage. The minimum offset current to ensure the zero voltage switching can be determined by solving the equations in chapter 3. In order to analysis and design the converter, each part of losses has to modelled. The semiconductor switching energy can be estimated, based on the datasheet, by using

second order approximation. The same method can also apply to the conduction losses. Another key component is inductor, reluctance equivalent circuit is the common way to design the inductor, and the air gap reluctance is complicated to get. The conventional way to calculate it out of accuracy, so a more advanced way which consider the fringing effect in 3D is used in this thesis. In switch mode power converter, the current in the inductor is always non-sine, also in the selected four-switch buck-boost converter, so the conventional Steinmetz equation is no more capable, so a improved generalized Steinmetz equation is implemented in this thesis. Winding loss in inductor is also worth to pay attention to, in high frequency application, skin effect and proximity effect lead to higher winding losses, and the fringing effect caused by the air gap also affects winding losses, mirroring method is implement to calculate it in this thesis.

Several modulation schemes are compared analytically and numerically in chapter 4 in terms of efficiency, losses on each component and inductor volume. In conclusion the zero voltage switching modulation is the best modulation scheme. In order to further decrease the losses swing on each switch, a new modulation scheme is proposed. The negative offset current and switching frequency is increased as the power is falling. Consequently, the switching off losses and conduction losses is larger than original.

After the topology and modulation scheme are selected, details of the converter can be determined. The bus voltage is $960V$, as a result, the switch is switching at the bus voltage. Consequently, a high frequency is not reachable due to large switching off losses. A two-stage structure is proposed, so switches at high voltage side are switching at half of the bus voltage ($480V$). In this case, a $650V$ GaN switch can be selected due to its extremely low switching losses and relatively low conduction losses. After that, the number of interleaved phases is determined in terms of maximum losses on each device, output capacitance value and total inductor volume. In conclusion, three phases is the optimal. It should be noted in $360V$ output, the high voltage high side switch S_1 still has $30W$ losses, so a external capacitance should be connected in parallel with the switch to reduce the switching off losses. The inductor is designed and simulated in finite element software. The power stage of the converter can reach 98.5%($630V$) and 97.7%($360V$) respectively. A $16.6kW/L$ power density can be achieved, according to the 3D mechanical modelling.

Next, the close loop control is determined . The control strategy is the current mode control in which there are two feedback loops, a voltage loop and a current loop. According to the two-stage structure, a balancing controller is implemented to keep the balance of the high stage and low stage, otherwise, the voltage may drift between the two stages and over the breakdown voltage of the devices and damage them even the entire system. The duty cycle of each state is calculated instantly according to the input/output voltage and output power, equations are given in chapter 6.In order to ensure the zero voltage switch, the zero crossing detection is applied. The drain current zero crossing point of high voltage low side switch S_2, and the state remains until a certain time delay t_{delay} after the zero crossing. With all discussed above, the close-loop control for the converter can be achieved.

A 48/12 two phases four-switch buck-boost converter is used to verify the zero voltage switching, and the proposed modulation scheme. From the testing results, the efficiency is

more flat as the output power changes. From the waveform, the zero voltage switching is proved.

8.2. Future work and outlook

Due to the time limitation, the prototype is not finished, so in the future, it should be finished and tested. Moreover, coupled inductors should be designed to further decrease the total volume of inductors in order to increase the power density. In terms of close-loop control, the bandwidth of this multiphase four-switch buck-boost has not been clarified, it would be very interesting to investigate the bandwidth and phase margin of the close-loop control. Further, it is worth to apply other control strategies and controllers to this converter to verify which one is the best. Meanwhile, for the proposed new modulation scheme, there is a trade-off between the variation of frequency and offset current which needs to research for every specific design.

This topology probably is also suitable for there applications such as UPS (Uninterruptible Power supply), EV (Electrical Vehicle) charging, microgrid, etc. Because of the advantages of this topology, it could be a good candidate for these applications, which is worth investigating.

A

Appendix A

In this appendix, losses **Modulation I: S_4 hard switching modulation**

	630V		360V	
	P_{max} (W) & T_{max} $(^\circ C)$	ΔT $(^\circ C)$	P_{max} (W) & T_{max} $(^\circ C)$	ΔT $(^\circ C)$
$S1$	17.4 & 51.1	17.7	34.3 & 76.1	42.8
$S2$	14.7& 46.9	14.2	41.7 & 87.1	54.2
$S3$	7.8 & 36.6	6.8	14.1 & 46.0	18.0
$S4$	84.1 & 150.3	72.8	130.4 & 219.3	140.2

Table A.1: Losses on each switch Modulation of I

Modulation II: S_3 hard switching modulation

	630V		360V	
	P_{max} (W) & T_{max} $(^\circ C)$	ΔT $(^\circ C)$	P_{max} (W) & T_{max} $(^\circ C)$	ΔT $(^\circ C)$
$S1$	17.4 &51.1	17.7	34.3 & 76.1	42.8
$S2$	7.2 & 35.7	2.7	14.5 & 46.5	12.9
$S3$	38.7 & 82.6	7.2	48.6 & 97.4	21.9
$S4$	1.9& 27.8	0.9	1.9 & 27.8	0.8

Table A.2: Losses on each switch of Modulation II

Modulation III: High trapezoidal current modulation

	630V		360V	
	P_{max} (W) & T_{max} $(°C)$	ΔT $(°C)$	P_{max} (W) & T_{max} $(°C)$	ΔT $(°C)$
$S1$	41.7& 87.1	53.6	45.3 & 92.5	58.1
$S2$	51.5& 101.7	68.5	76.2 & 138.5	104.3
$S3$	14.9 & 47.2	17.4	23.3 & 59.7	31.3
$S4$	73.1& 133.9	99.8	113.2 & 193.7	160.9

Table A.3: Losses on each switch of Modulation III

Modulation IV: High triangular current modulation

	630V		360V	
	P_{max} (W) & T_{max} $(°C)$	ΔT $(°C)$	P_{max} (W) & T_{max} $(°C)$	ΔT $(°C)$
$S1$	41.7 & 87.1	53.6	45.3 & 92.5	58.1
$S2$	16.8 & 50.0	16.5	26.3 & 64.2	30.5
$S3$	14.9 & 47.2	17.4	23.3 & 59.7	16.8
$S4$	34.4 & 76.1	41.7	42.0 & 87.6	53.6

Table A.4: Losses on each switch of Modulation IV

Modulation V: Zero voltage switching modulation

	630V		360V	
	P_{max} (W) & T_{max} $(°C)$	ΔT $(°C)$	P_{max} (W) & T_{max} $(°C)$	ΔT $(°C)$
$S1$	13.1 & 58.7	12	30.6 & 78.0	35.2
$S2$	7.9 & 36.2	4.2	14.5 & 51.1	15.8
$S3$	11.1 & 41.5	11.5	19.8 & 54.5	25.6
$S4$	3.5 & 30.2	0.9	2.6 & 28.9	2.3

Table A.5: Losses on each switch of Modulation V

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