

Design of an Integrated Hybrid configuration of a Modular Multilevel converter and an Impulse generator

N. M. Kulkarni



KEMA Labs

TUDelft

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by

N. M. Kulkarni

to obtain the degree of Master of Science
at the Delft University of Technology,
to be defended publicly on Friday August 19, 2022 at 9:00 AM.

Student number:	5347939	
Project duration:	December, 2021 – August, 2022	
Thesis committee:	Prof. ir. Peter Vaessen,	TU Delft, supervisor
	Dr. ir. Mohamad Ghaffarian Niasar,	TU Delft
	Dr. ir. Aleksandra Lekic,	TU Delft
	Ir. Dan-Andrei Gumeni,	KEMA Laboratories
PhD supervisor:	Ir. Dhanashree Ganeshpure,	TU Delft

This thesis is confidential and cannot be made public until December 31, 2023.

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Summary

The penetration of power electronics into the grid is growing rapidly due to the increasing number of renewable generation systems. These power electronic converters introduce electrical stresses in the form of complex waveforms into the grid caused by their switching operations. The High voltage (HV) equipment is subjected to these stresses. To maintain the reliability of the power system it must be able to withstand these kinds of complex stresses. To test the HV equipment with such stresses and assess its correct functioning, it is important to be able to reproduce such complex waveshapes. A new Modular Multi-level Converter (MMC) based arbitrary waveshape generator with 67 sub-modules in each arm rated for 100 kV is being designed to target the testing of medium voltage (MV) class equipment. Since the MMC has its own limitations in generating superimposed Lightning impulse (LI) waveforms, an integrated hybrid configuration combining the conventional Marx generator circuit and MMC is needed to generate the superimposed LI. This thesis intends to design and demonstrate the feasibility of such an integrated hybrid configuration focusing on two major goals. Firstly, to investigate the capabilities of the Typhoon HIL to implement the control of MMC and compare this with the existing OPAL-RT controller, and secondly, to design an integrated hybrid configuration to produce superimposed waveforms. To achieve the first goal the Typhoon HIL hardware, software, MMC topology, and the various modulation techniques were studied in depth. Phase shifted carrier (PSC) modulation-based open loop control was implemented on the CPU and FPGA of the HIL device. The results were compared with the offline simulations, and it was found that the control implemented on the CPU is suitable for up to 1 kHz, and the FPGA control is recommended for higher frequencies. The performance of Typhoon HIL is better than OPAL-RT regarding generating accurate gate pulses at higher fundamental frequencies. The approach for the second goal used is to study the literature on existing composite test setup to understand the requirements to design the decoupling circuit between impulse generator and MMC. A downsized model of an integrated hybrid configuration was designed and validated by offline simulation. Next, a 300 V hardware prototype was implemented in a step-by-step manner. First, Rapid control prototyping was performed separately on the MMC comprising 2 sub-modules in each arm with the FPGA control developed using the Typhoon device. Thereafter, the impulse circuit was coupled with the MMC to test for both power frequency and DC superimposed impulses. It was observed that the real-time simulation results were identical to the offline simulations and the superimposed impulses could be generated with high accuracy. Finally, the output of the MMC for higher signal bandwidth was tested using the Typhoon FPGA control. It was found that the MMC could generate sinusoidal waveforms up to 3 kHz.

Acknowledgements

The last two years have been more dynamic than I could have ever imagined. Studying at the Delft University of technology has been a wonderful experience overall, and I am truly grateful for this opportunity. I owe the completion of this thesis to several people.

To *Peter Vaessen*, for introducing me to the world of High voltage technology. You have taught me the practical approach needed in academia and industry. You have instilled an interest for High Voltage in me, which I intend to carry on lifelong. Your tips and feedback have helped me to learn a lot. I am extremely grateful for your advice and support.

To *Mohamad Ghaffarian Niasar*, for your constant support and guidance throughout the thesis. Your curiosity and quest to always find answers to ambitious problems have inspired me. Those long technical discussions with you have helped me gain a thorough understanding of various topics of High voltage.

To *Dhanashree Ganeshpure*, for teaching me valuable lessons during the thesis. You have taught me how to remain patient when things get difficult. Your systematic approach toward research and passion for perfection has always been a great inspiration. I truly aspire to learn and adopt the same attitude for myself. I am immensely thankful for your invaluable support, guidance, and suggestions. Your insights have helped me strengthen my understanding of Power electronics converters and hardware.

To *Luis, Wim, Geert Jan, and Mladen* for helping me utilize the resources of the HV and Power electronics lab in the best possible way.

To *Typhoon HIL Team*, for their support. I am thankful to the team for being approachable and available every single time. The prompt and detailed assistance from the team has helped me expedite the progress of my thesis.

To *Dan Andrei-Gumeni and Erik de Jong* for sharing your valuable insights and experience to help me understand Real-time simulators better. I am thoroughly grateful for your assistance.

To *my friends and family*, for believing in me and showing their relentless support and confidence in me during the tough times.

Nitish Kulkarni
Delft, 2022

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1

Introduction

1.1. Background and Motivation

The electrical power system today is facing new electrical stresses due to the addition of an increased number of renewable energy sources (RES) through Power electronics converters [1]. Therefore, the power system components, particularly High Voltage (HV) equipment such as Transformers, Power Cables, and Protective equipment must withstand these kinds of new stresses which arise due to the switching operation in these converters and circulating current harmonics. Figure 1.1 illustrates a few examples of the complex waveforms that are subjected to the HV equipment. Complex waveform 1 in the figure represents AC superimposed impulse, waveform 2 corresponds to DC superimposed wave and complex wave 3 refers to a combination of three waveforms (DC, High order Harmonic AC and Switching Impulse) Conventional test sources can generate test waveforms of different shape including sinusoidal, lightning impulse, switching impulse and DC with high accuracy, however, they are limited when it comes to the signal bandwidth.

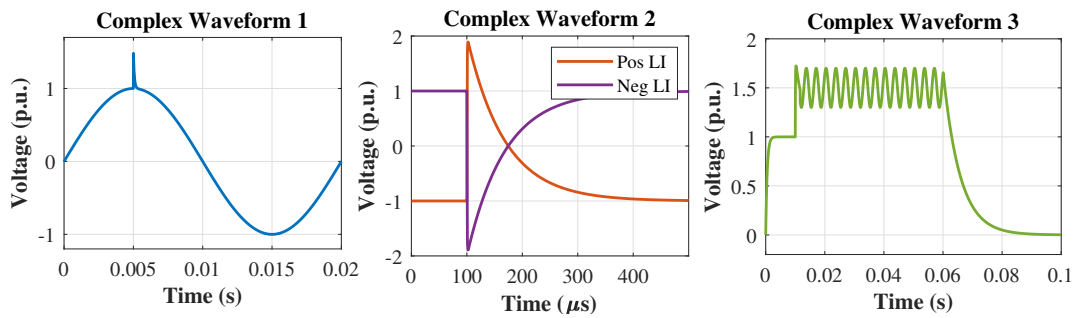


Figure 1.1: Complex waveforms [1]

The performance of an HV insulation in an AC system can be determined by the lightning impulse voltage test, switching impulse voltage test, and Power frequency Voltage test. The impulse voltage tests help to check the performance of the insulation under any kind of voltage surges, whereas the power frequency test validates the performance under normal operating

conditions. These tests are usually performed separately, however in reality the surge voltage is in most cases superimposed over the power frequency waveform [2]. Consequently, there is a need for testing insulation systems with superimposed voltages to have increased reliability. For instance, defects in the insulation can serve as a major threat to the safety and stable operation of the HV systems, PD measurements help in detecting such defects in HV equipment [3]. In most cases, these measurements are carried out at either Power frequency or Impulse voltages separately, whereas for a safer design of insulation it is also important to understand the behavior of PD under superimposed voltages.

Moreover, with the growing trend to move toward HVDC Systems, HVDC equipment, particularly the DC Cables are becoming of great importance. When DC is applied to cables, space charges are formed which remain inside. Therefore, when these cables are subjected to transients (both lightning and switching) during their operation, superposition and distortion of the local field take place due to the external field because of the over-voltage and the electric field due to the presence of these space charges which can cause breakdown[4]. Consequently, DC superimposed tests are crucial for the design of such cable insulations.

Using conventional methods, it is possible to couple two or more HV test sources to generate superimposed waveforms. However, designing and implementing this coupling every time for research and testing is a challenging task. As a result, this calls for the need to have an integrated test source inherently capable of generating superimposed waveforms of desired shape and polarity. Recent research in the field of Power Electronics has suggested that multi-level converter topologies such as the Modular multilevel converters (MMC) could be a better solution to generate arbitrary shape test voltages with high accuracy and signal bandwidth higher than conventional test sources such as HV amplifier.

The capabilities and design trade-offs of MMC being used for conventional and unconventional HV testing have been discussed and demonstrated in [1]. The topology explained in [1] has been mathematically modeled and validated using MATLAB. The implemented topology is intended to be developed in the future as a full-scale prototype testing source rated for 100 kV with 67 sub-modules in each arm. As a part of the development procedure, it is important to validate the performance of the control system of the topology on a small scale with reduced voltage levels and sub-modules. A real-time simulation study emulating the behavior of the controller can be helpful to verify the functionality and accuracy of the control system.

1.2. Research Objectives

This thesis has primarily two goals, which are illustrated in figure 1.2 below. The first goal of this thesis is to understand the capabilities of the Real-Time simulator (Typhoon HIL) to implement the control system of the MMC for HV testing application and compare this with existing OPAL-RT controller. This is done by primarily performing model in loop (MIL) testing using Typhoon HIL, where both the converter and the control strategy are developed in the real-time simulator software and results are validated with an offline simulation. After validation, this control strategy is implemented for the down-scaled topology to carry out Rapid

Control Prototyping (RCP). The second goal of this thesis is to investigate and demonstrate the feasibility of an integrated Hybrid configuration of the MMC and an Impulse generator to obtain superimposed waveforms. This is carried out by first developing a coupling circuit for such a hybrid configuration. Followed by performing offline simulations to validate the integrated hybrid, and finally implementing the model in hardware to obtain superimposed waveforms.

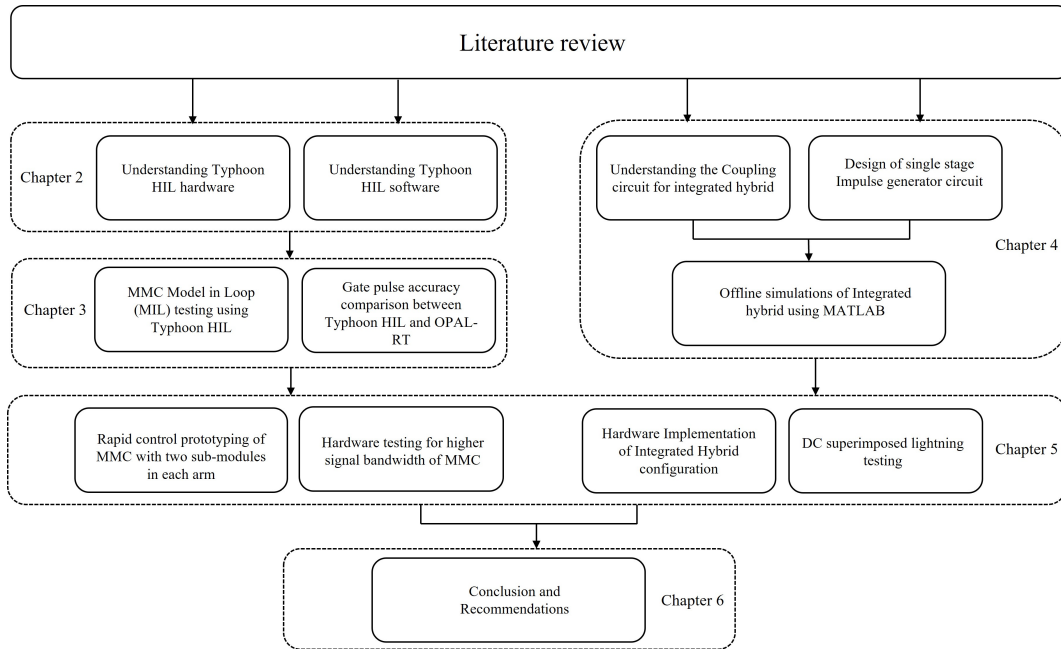


Figure 1.2: Structure of Thesis

To achieve the two above-mentioned goals of this thesis, the following research questions need to be answered which are summarised below:

- RQ1** What are the capabilities of Typhoon HIL with regards to real-time testing?
- RQ2** What are the differences in performance between the Typhoon HIL and OPAL-RT in implementing the control for MMC based test source?
- RQ3** How to implement Open loop control for MMC based HV testing application?
- RQ4** How to design a coupling circuit for the integrated hybrid configuration of MMC and impulse generator?
- RQ5** How can Typhoon HIL generate accurate gate pulses for fundamental reference frequencies beyond 50 Hz?
- RQ6** How to realise an integrated hybrid configuration of an impulse generator and MMC?

1.3. Outline of Thesis Report

This section describes an overview of each chapter:

Chapter 2 provides some background information on the different kinds of Real-time testing methodologies. A detailed introduction to the Typhoon HIL is provided, along with the details of the hardware architecture and software tools by Typhoon. The limitations of the HIL 404 device for implementing the control are also discussed.

Chapter 3 discusses the open loop control for the MMC HV testing application in detail. The chapter depicts the control developed in the typhoon environment to perform MIL. The MIL testing results are analyzed and compared with offline simulation. The results of Typhoon HIL and OPAL-RT are compared and highlighted.

Chapter 4 describes the requirements for the coupling circuit for the hybrid configuration. The chapter also discusses the selection of suitable components for the Hybrid configuration. The design of the impulse generator is discussed in detail. The chapter presents two configurations for generating superimposed waveforms, which are simulated and validated through an offline simulation.

Chapter 5 depicts the hardware setup for RCP using Typhoon HIL. The results of the RCP are analyzed and validated with the results of an offline simulation. This chapter further depicts the hardware implementation of the Integrated hybrid configuration and discusses the results of the superimposed waveform testing. The chapter also discusses the output of MMC for higher fundamental frequencies.

Chapter 6 is the last chapter of the thesis, and it provides a conclusion based on the findings of this thesis and summarises the results. Additionally, the recommendations for the future are suggested in the chapter.

2

Introduction to Typhoon HIL

In this chapter, the fundamentals of RT testing and the key differences between RT simulation and offline simulation are discussed. A detailed introduction to Typhoon HIL hardware and software is presented.

2.1. What is Real-time Simulation ?

Different simulation software have been developed as simulations have been in use for decades for extensive planning and design of electrical systems. These simulation studies have been very critical in the development of a large number of applications. The solutions in this simulation software are based on the choice of solver and the choice of simulation step. The simulation step can be fixed or variable time. When time moves forward in equal steps, it is referred to as fixed time step simulation[5]. There are simulations that employ variable time step solving techniques, which are usually used for solving non-linear systems and high-frequency dynamics, and are not suited for RT simulation [6].

During fixed time step simulations, the mathematical equations and functions are successively solved as a function of states by the end of each previous time step. The simulation is categorized as either Real-time or offline, based on the amount of actual time it takes to compute all functions and equations during a given time step. Figure 2.1 and Figure 2.2 represent cases of offline simulation, where the actual computing time is less than the fixed time step and where the computing time is greater than the fixed time step respectively. During the offline simulation, the goal is to obtain the results as quickly as possible, and the exact moment at which the result is obtained is not that important. Therefore, the complexity of the model and the computational power determine the system's solving speed. On the contrary, for real-time simulation, the accuracy of the results depends on the time required to generate the results and also the complexity of the model [7]. Figure 2.3 shows an example of RT simulation, it is seen that during RT all the computations including accessing the inputs and outputs are performed accurately and results made available within the given fixed time-step. In short, it means that the time required to solve the model must be less than the clock duration of the time step. One may get confused between an RT simulation and an accelerated simulation. However, the

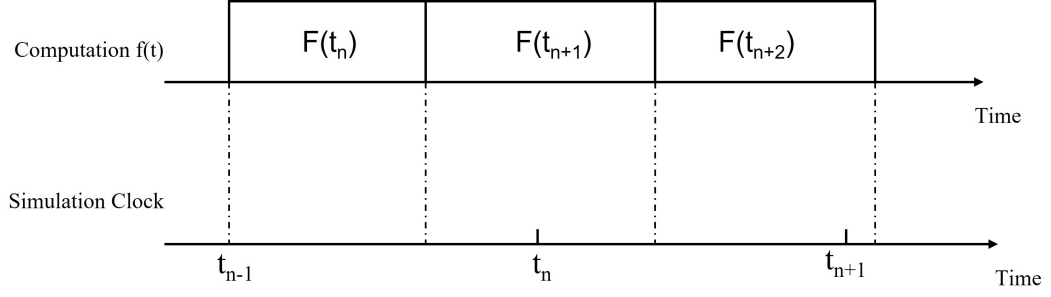


Figure 2.1: Offline Simulation (Accelerated Simulation)

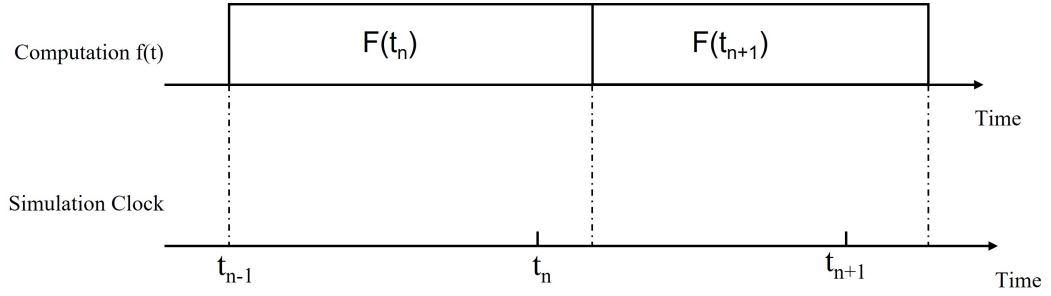


Figure 2.2: Offline Simulation (Slower simulation)

difference between the two is, that in the former the idle time following the operations of the simulator is lost, whereas in the latter the idle time is used to calculate for the next time-step. If computations by the RT simulator are not performed within the required fixed time-step, then the simulation is considered erroneous and this is referred to as an 'overrun'. The selection of the right simulator and correct time step depends on the following factors [7]:

1. The complexity of the model to be simulated
2. The max frequency of the transient to be simulated (this defines the minimum fixed time-step needed)
3. Hardware requirements (Eg. Number of Input and Output [I/O] ports needed to interface the RT simulator with the physical plant or/and controller).

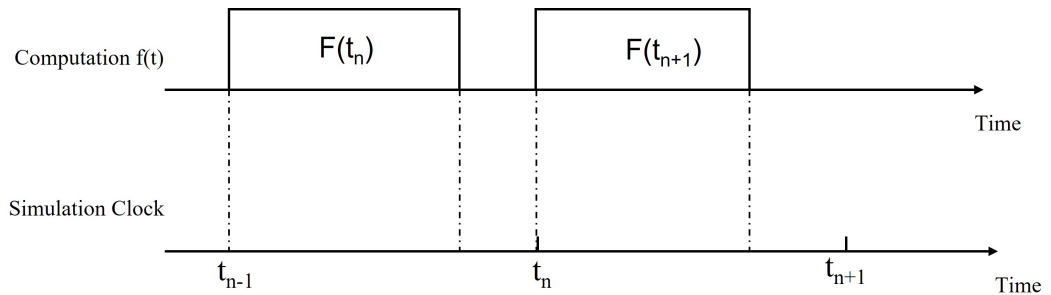


Figure 2.3: Real-Time simulation (Synchronized)

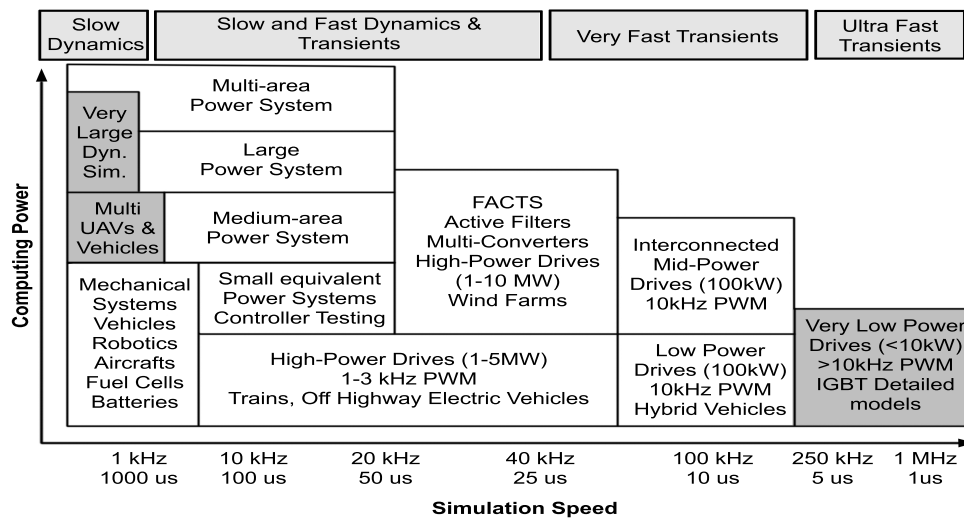


Figure 2.4: Simulation time-step vs Computing power [7]

Figure 2.4 portrays the range of simulation time steps and Computing power for a range of applications. As a ballpark figure, the fixed time step for simulation should be smaller than 5-10 % of the smallest time constant of the system[7].

2.2. RT testing methodologies

2.2.1. Rapid Control Prototyping

In this type of testing, the controller of the system is modeled in the RT simulator, which is used to control the physical plant. Since the controller is implemented in the RT simulator, it is very flexible and easy to debug [7]. It is possible to tune the controller on the fly (i.e it is possible to modify the controller model during the RT simulation). This type of testing is often used, when the controller design is needed to be validated before implementing it in hardware.

2.2.2. Hardware in the loop (HIL)

HIL testing involves interfacing a physical controller with an RT simulator that emulates the Plant. HIL testing allows the testing of controllers at an early stage when test benches are not available. Furthermore, Virtual plants through HIL testing allow to cut the costs of testing [7]. It is also possible to test the controller for certain extreme conditions. This testing helps to check whether the designed controller is compatible with the plant.

2.2.3. Model in Loop (MIL)/ Software in Loop (SIL)

MIL represents a logical step above the combination of HIL and RCP. In MIL, both the controller and the plant are implemented on the RT simulator. The benefit of implementing MIL is that the quality of the signal is not affected, since there is no physical plant, controller, Input ports, and Output ports.[7].

This thesis intends to investigate the capabilities of Typhoon HIL to implement the control

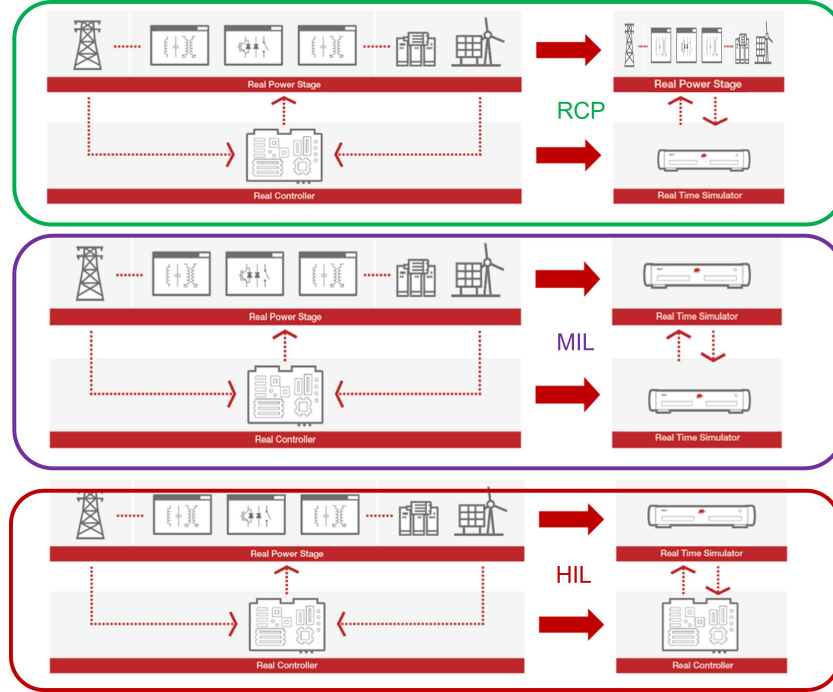


Figure 2.5: Methods of RT testing [Courtesy Typhoon HIL]

of MMC. Typhoon HIL was selected to investigate for its smaller possible simulation step (200 ns) and industrial robustness. Furthermore, it is intended to compare its performance with the existing controller OPAL-RT.

2.3. Typhoon HIL Hardware

The Typhoon HIL devices differ in the processing power; however, all have a similar multi-processor hardware architecture which consists of CPUs (both system and user) and a typhoon FPGA Solver. Figure 2.6 depicts the layout of the Typhoon HIL 404 hardware architecture. The multi-core FPGA is optimized to deliver the time-exact simulation of the electrical domain of the model[8]. The main application of the FPGA solver is to simulate the electrical part of the plant.

The FPGA architecture consists of the following components:

1. Standard processing core (SPC): This is the basic element of the circuit solver. It is responsible for simulating the electrical domains of the model consisting of :
 - Linear passive elements- both constant and time-varying
 - converter blocks made up of ideal switches
 - contactors based non-ideal and ideal switches

There are multiple number of such cores available on the HIL device, depending on the model. (For instance, the HIL 404 device has 4 SPC)These cores are connected via

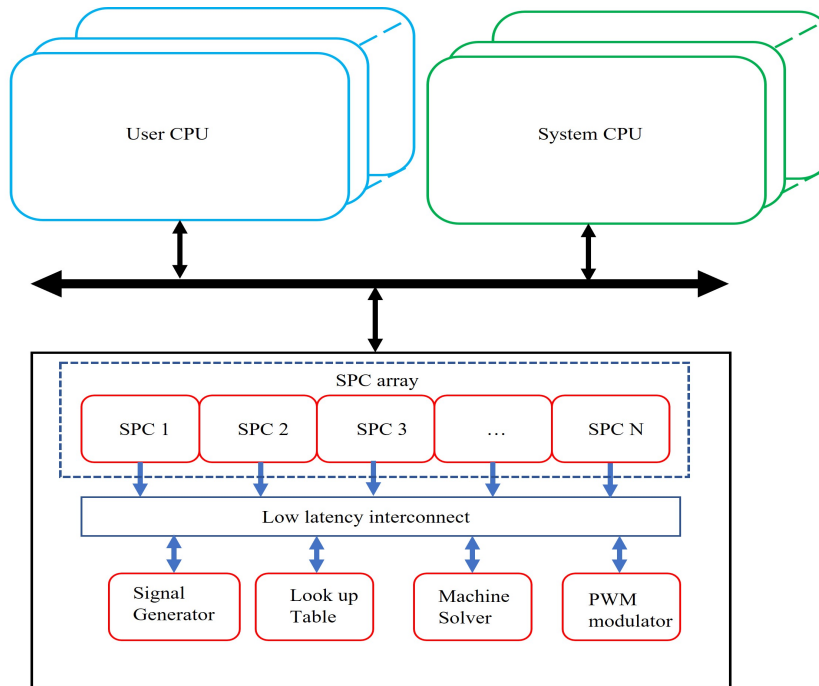


Figure 2.6: Typhoon HIL Architecture

separate communication links, which allow for an exchange of information with a delay of a single simulation step [8].

2. **Signal Generator:** This block is responsible for generating waveforms of arbitrary shape at a full simulation rate. It is mainly used as an independent voltage and current source in a model. The number of such generators that can be used in a model depends on the configuration of the solver.
3. **Lookup table (LUT):** It is mainly used to simulate elements that have a non-linear behavior such as Photo voltaic (PV), battery, and non-linear passive elements. The Number of LUTs depends on the solver configuration.
4. **Machine Solver:** The machine solver block emulates one electrical machine including the mechanical part, electrical part and the speed measurement part [8] (such as an encoder and resolver). The number of electrical machines that can be modeled and simulated depends on the configuration of the solver.
5. **PWM Modulators:** A dedicated hardware is provided on the FPGA to generate triangular-based PWM signals. It operates at the clock frequency of the device [9](E.g. 280 MHz for HIL 404). The carrier signals are integrated within the hardware, and the reference signals are given externally (i.e physically externally or separately within the model)

The low latency interconnect represents the communication link between the different hardware resources with the Typhoon FPGA solver. The CPUs are used to simulate the non-electrical domains of the model. The User CPU being a general-purpose CPU that can be

controlled by the user and used to simulate mechanical, thermal or signal processing systems of the model. It is used to validate controller algorithms and perform RCP. Whereas, the system CPU cannot be directly controlled by the user, and is used for simulating communication protocols and low dynamics processes.

The Typhoon HIL 404 has 16 analog I/O and 32 Digital I/O, in front of the device. The analog I/O has a resolution of 16 bits with a range of ± 10 V, the digital ports are standard 5 V CMOS logic I/O. The absolute maximum limit when one pin is loaded for both Analog and digital I/O is 24 V. The HIL 404 device has one RS232 port for serial communication, 2 Ethernet ports for executing different communication protocols, 1 USB port to connect the HIL device to a PC, and 2 CAN ports for CAN communication. Figure 2.7 and 2.8 show the front and back of the HIL 404 device.



Figure 2.7: HIL 404 front side



Figure 2.8: HIL 404 back side

2.4. Typhoon HIL Software

Typhoon HIL has its own software named as 'Typhoon HIL Control Center'. The software consists of three main components: 1) Schematic editor, 2) HIL SCADA and 3) Typhoon test IDE. Apart from these three main tools, the control center also has some additional tools such as the signal analyzer, script editor, waveform generator, LUT extraction tool, and firmware manager.

2.4.1. Schematic editor

The editor allows the user to build the desired schematic model using pre-defined components from the library explorer. The model can be simply built by dragging and dropping the required components from the library located on the left part of the screen and connecting them together. The schematic editor has an inbuilt feature named 'Model initialization script' located in the model menu on the top of the screen. This allows the user to easily define the variables for the model, it, therefore, makes it very convenient to modify these parameters globally for simulation. Furthermore, Python commands can be written in the initialization script. For example, it is possible to load parameters from a file or write a code that fetches from a particular web page, GitLab, or any other DevOps platform and takes the relevant parameters).

Another feature available in the schematic editor is the 'SCADA Inputs', these allow the user to set values in real-time while interacting with the simulation using HIL SCADA. Once the model is built based on the type of components used the components are either colored blue or black. These represent different domains of the system architecture. The part colored black of the model schematic represents the electrical domain, which will be executed on the FPGA solver. Whereas the part in blue represents the non-electrical part and will be executed on the CPUs. Figure 2.9 shows the schematic editor window. On the left side of the screen, the li-

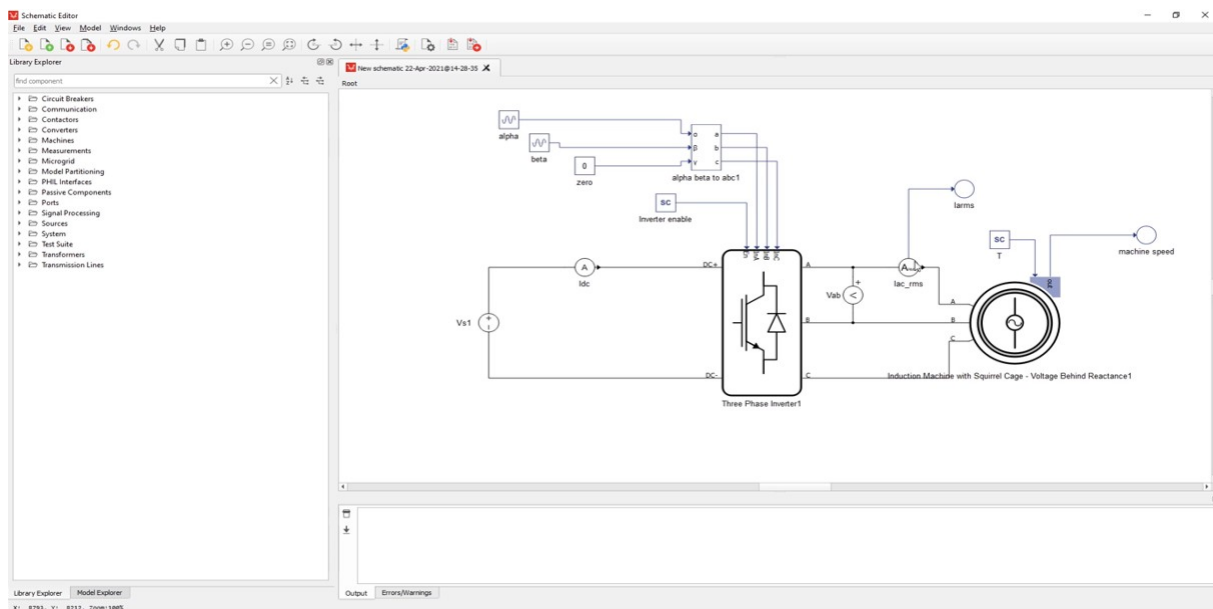


Figure 2.9: Schematic editor window

brary explorer is located. For ease of access the components are grouped in various categories, however, it is also possible to search components via the search field provided. Furthermore, it is possible to model a component with any arbitrary function using the C programming language. The C function consists of inputs, outputs, and functionality that determine the function of the block. An additional extension to the C function is another function named 'Advanced C function', this allows the user to import dynamic link library (DLL) and h files. The schematic editor also allows the integration with other simulation tools, FMI, open source interfaces with Xyce, and OpenDSS [10]. A step-by-step procedure to build a model in the schematic editor is described in detail in the Appendix.

2.4.2. HIL SCADA

HIL SCADA is a unique tool that allows the user to create an interface with the model running in RT [10]. It can be opened directly from the typhoon HIL Control center or can be launched after compiling the model from the schematic editor. If the HIL device is connected and active, then the model can be simulated in RT, or it is also possible to load the compiled model in Virtual mode. The virtual HIL mode is a special mode in which the software can emulate the HIL series 4 and 6 devices to give results[11], however, in this mode the model is not run in RT and there is no external I/O support. HIL SCADA allows the user to interact with the model during the simulation through the use of widgets. These widgets can be used to measure/monitor or take actions during simulation. They are classified into various groups based on their function:

1. **Action widget:** As the name suggests, these are used to change the settings in the model. The function of this widget is determined through an embedded python script. These widgets, therefore, perform the specified action based on the macro code written in the script editor of the macro widget. There are different types of action widgets [12]:
 - **Button:** As the user clicks on this widget during the simulation, the script execution is commenced.
 - **Text box:** The execution of the macro code begins when the user enters a value in the text box. The value entered can be used as an input value to a particular variable in the code
 - **Combo box:** When a new combo box value is selected, it can be used in the macro script to perform a task. (A combo box can be understood as a drop-down menu in which the user can select one value that is used as a parameter in running the macro code)
 - **Check box:** Checking or unchecking the tick box will start or stop the running of the macro code. The state of the check box can be used as an input value to the script.
 - **Slider and Knob:** These can be used to change the values of the certain parameter during RT simulation. The values set can be used as input parameters for a macro code script.

- **Macro:** This is an action widget that has different event handlers whose code is executed in different ways[12]:
 - On start: The script written in this handler will be executed after the start of the simulation, after the execution of the main initialization script.
 - On click: The code execution will start on a button click. It is very similar to the button action widget mentioned above.
 - On Timer: The code will be executed on a timer event of the HIL SCADA time slot.
 - On stop: the script will be executed after the simulation is stopped.
2. **Monitoring Widget:** These widgets can display the values of any digital or analog signals in RT. It is also possible to display the value defined by a python expression [13]. Therefore it is possible to have any desired relationship between the signal values obtained and the values being displayed. It is possible to set the sampling rate individually for all these monitoring widgets. There are different types of monitoring widgets available in HIL SCADA:
- **Digital display, Text graph, XY graph, phasor graph, gauge, bar graph:** These widgets are usually used to display analog signals.
 - **LED:** It is mainly used to read digital signals.
 - **PV monitor:** This widget is used to locate the operating point of the PV panel.
 - **Scope:** This widget is similar to an Oscilloscope and allows the user to read, display and capture analog and digital signals for the desired duration of time. The sampling rate of the scope can be defined by the user.
3. **Data logging widgets:** As the name suggests, these widgets can be used to store data from simulation to a data file. There are two types of widgets:
- **Signal data logger:** It stores the data points from an analog signal or a digital signal to the desired file type such as .mat, .csv. the logging of the data can be started at the start of the simulation or at any other arbitrary time during the simulation. It can be paused or stopped using a dedicated button as well. The data however cannot be logged at any arbitrary sampling rate.
 - **Stream data logger:** This widget stores a stream of data points of a digital or analog signal to either .csv, .h5 or .mf4 format. Here it is possible to define a sampling rate as per need.

Figure 2.11 below shows the HIL SCADA interface. The library explorer and panel explorer can be used to add the widgets to the panel. The model explorer can be used to access the model variables (Eg, current and voltage measurements, Mechanical speed of the machine, torque, etc.) The simulation input and outputs can be directly accessed and controlled through the model settings located on the right part of the screen.

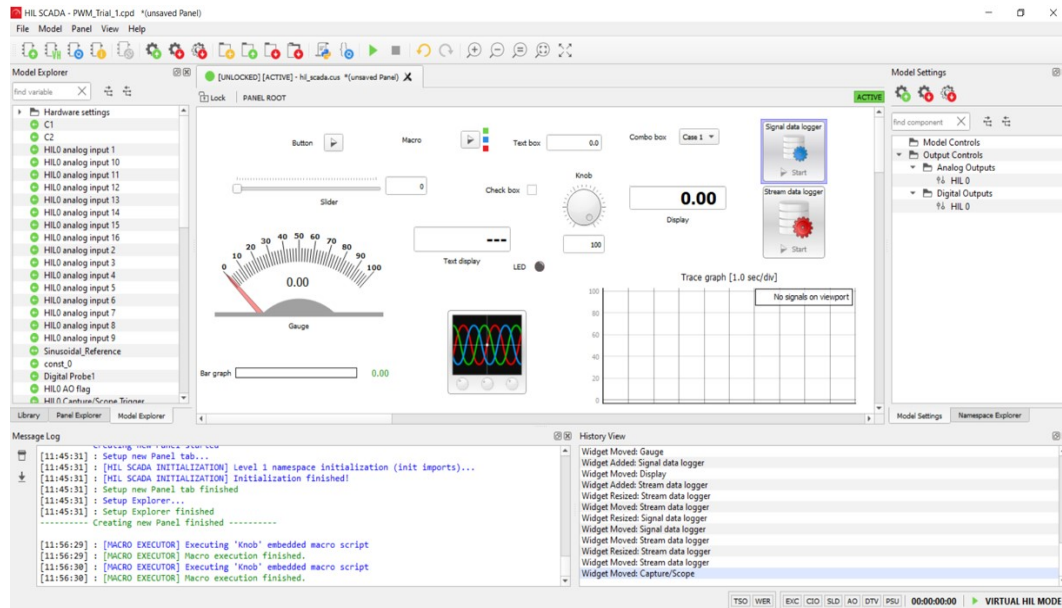


Figure 2.10: HIL SCADA user interface

4. **Analysis Widget (Frequency response widget):** This widget allows the user to evaluate the frequency response of the model or system in RT. It can be used for the impedance analysis of an electrical system in RT, measurement of the transfer function including sensitivity transfer function, loop gain, load disturbances, etc [14]. These measurements can be done on FPGA Solver with a bandwidth of 0.5 Hz - 500 kHz or on a CPU with a reduced bandwidth of 0.5 Hz - 50 kHz [14]. The figure 2.11 below shows the graphical interface of the frequency analysis widget.

The status of the simulation is well depicted by the HIL device flags which are displayed in the status bar of HIL SCADA. There are 8 HIL device flags which are available when the device is running in RT mode, they are not functional in the virtual HIL mode. However, the exception is the arithmetic Overflow (AO) flag which is also available in the virtual HIL mode. The status bar consists of the following flags [15]:

1. **Time slot Overrun (TSO):** This flag is raised when the time needed for the HIL SCADA Computations exceeds the allocated time slot.
2. **Widget Errors (WER):** This flag is raised when there is some error in the active panel widgets.
3. **Signal Processing Exception (EXC):** This particular flag is raised when the generated code throws an exception on either of the CPUs (User, System, or communication). When the simulation stops, the flag is reset.
4. **Computing interval overrun (CIO):** The flag is raised when the signal processing computing time exceeds the reserved time slot.

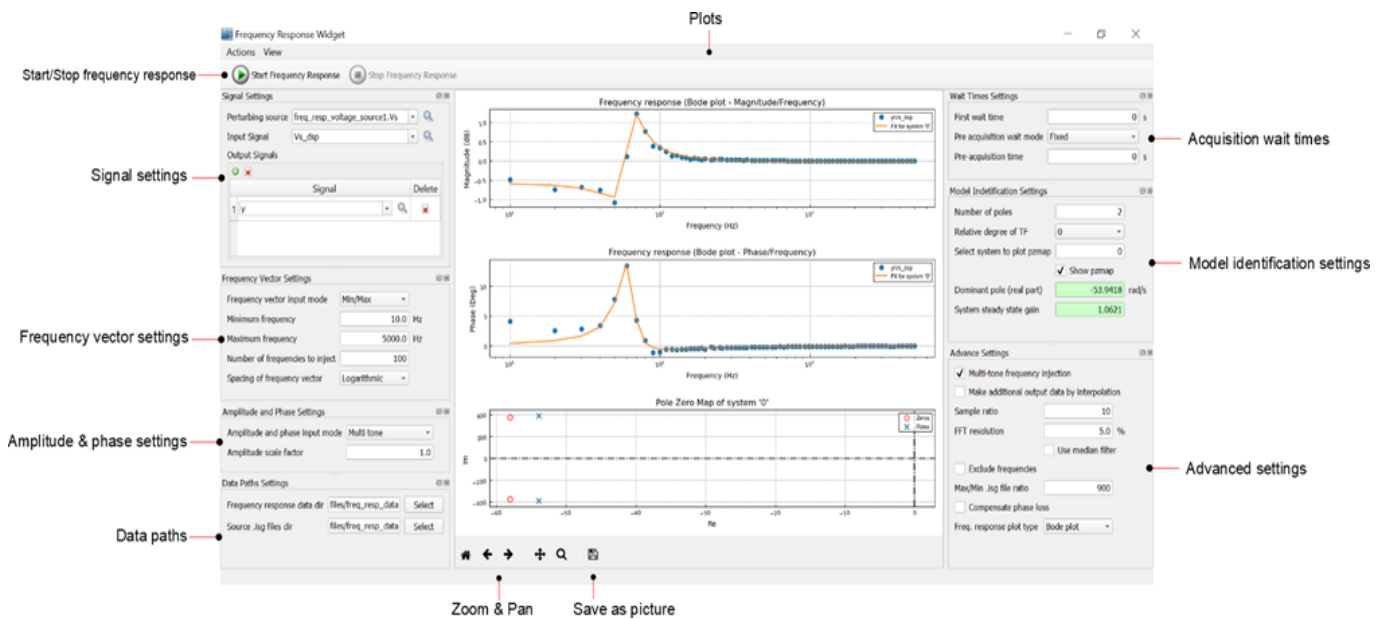


Figure 2.11: Frequency response widget [14]

5. Serial Link status (SLD): This flag is raised when the serial link is down.
6. Arithmetic overflow (AO): The flag is raised when the computed values of the model are above the numerical range of the device.
7. Dead time violation (DTV): The flag is raised when there is a shoot-through situation in one of the phase legs of a converter.(i.e. when the dead time requirement for switching is not respected)
8. Power supply unit fault (PSU): The flag gives information about the condition of the externally connected power supply output.

Figure 2.12 below depicts the status bar available in the HIL SCADA. The mode of operation of the HIL device is also displayed in this bar.

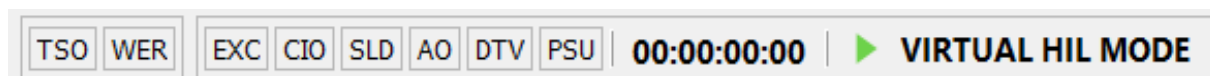


Figure 2.12: HIL SCADA Status bar[14]

2.5. Real Time constraints for Typhoon HIL

The FPGA solver of typhoon solves the model and simulates with a fixed time step which is pre-defined. The simulation step is fixed and discrete and cannot be altered dynamically during the course of the simulation to carry out iterations, therefore the time for computations is limited. The HIL 404 can be configured manually to maximize the use of the FPGA resources.

For example, the HIL 404 has 3 SPCs in configuration 1. The different configurations available for HIL 404 can be found in the figure 2.13 below.

Device Configuration Table

HIL Device: HIL404

	Configuration 1	Configuration 2	Configuration 3	Configuration 4	Configuration 5
Number of SPCs	3	4	2	3	3
Machine solvers	1	0	1	2	0
Signal generators	12	12	12	12	12
Look Up Tables	8	8	8	8	8
PWM channels	12	12	12	12	12
SPC peak processing power [GMAcs]	1.12	1.12	1.12	1.12	1.12
SPC matrix memory [KWords]	16.0	16.0	16.0	16.0	16.0
SPC output memory size [variables]	512	512	512	512	512
Max converter weight (ideal switches) / SPC	3	3	4	3	4
Contactors (ideal switches) / SPC	6	6	6	6	6
Non-ideal switches / SPC	0	0	32	0	32
Time varying elements / SPC	16	16	16	0	16
Nonlinear machine support	yes	no	yes	no	no
Nonlinear machine LUT size [KWords]	32	0	32	0	0
Converter power loss calculation	yes	yes	yes	no	yes
Converter forward voltage drop	yes	yes	yes	yes	yes
Switch-level GDS oversampling	no	no	yes	no	yes

Close

Figure 2.13: Device table for HIL 404

Converter Modelling: The number of switches in a converter increases the computational load, and increasingly complex converters demand more computational power. In the Typhoon HIL environment, the computational load from a converter is represented in terms of weight, therefore every converter has a pre-defined weight. This weight can be found simply by double clicking the converter block in the schematic editor. One of the main limitations of modeling the system in a typhoon is that individual power electronic switches cannot be modeled. It is possible to use Power electronic switches indirectly through Converter blocks. As the number of switches increases, the overall weight per SPC increases, and hence based on a given configuration this puts a limit to the maximum number of switches or converter blocks that can be modeled. By carefully implementing parts of the model on separate SPC, it is possible to model more complex systems with more number of converter blocks or switches. This is also valid for modeling the controller on the CPU, parts of the control system can be modeled on a separate CPU to increase the efficiency and reduce the time slot utilization. This can be achieved through model partitioning. It can be done in two ways: 1) Core partitioning (Partitioning across multiple GPUs) 2) Device Partitioning (Partitioning across different HIL devices)

For Each switch state permutation, the circuit model is considered to be a linear and time-invariant. This is referred to as the permutation mode of the circuit. For every mode of the

circuit, there is a designated linear and time-invariant model which is discretized and represented using a state space matrix. The matrix memory size defines the maximum size of the SPC, in terms of the number of available ideal switches and passive components. Increasing the number of components, increases the size of the matrix and the number of ideal switches increases the number of matrices. The simulation run time load needs to be reduced, in order to do that all state space matrices are pre-calculated and stored in the solver memory of the FPGA. The number of modes per circuit is 2^n where n is the number of switch elements. Hence, as the number of switches increases, the memory requirements increase exponentially, this increases the strain on memory. For example, if we have two sections of the circuit, one having $n = 5$ switches and other having $m = 5$ switches, then the total number of modes $= 2^{n+m} = 1024$, whereas if we do partitioning and split the model onto separate cores or devices, then the total number of modes $= 2^n + 2^m = 64$. Therefore, it can be seen that partitioning helps in reducing the memory requirements significantly. Moreover, it also makes it possible to maintain lower simulation time steps in large and complex models, which ultimately leads to shorter compilation time.

2.5.1. Model Partitioning

The built-in components of the Typhoon editor can be used to split complex models into several smaller models which are run in parallel to improve the speed of simulation and to utilize the HIL resources optimally. There are primarily two kinds of partitioning possible in Typhoon:

1. Electrical Circuit Partitioning
 - (a) Core partitioning
 - (b) Device partitioning
2. Signal processing partitioning
 - (a) Core partitioning
 - (b) Device partitioning

Electrical Circuit partitioning

The basic principle behind partitioning is the identification of independent circuit networks. By default, the typhoon editor assigns independent electrical circuit sections on separate cores. For instance figure, 2.14 depicts three separate (not interconnected) circuits are assigned to three different cores for computation. The three circuits highlighted by red-colored boundaries are each assigned to a different core.

The components used for the circuit partitioning are Ideal Transformer (IT) based coupling, Transmission line model (TLM), and core marker components.

The IT coupling is often used to split a complex model consisting of a power electronics circuit or a power system into subcircuits. The IT coupling behaves like an ideal transformer with a unity ratio. This type of coupling adds a time delay equivalent to one simulation step in the simulation. IT coupling is an asymmetrical type of coupling, which is depicted in the figure 2.15. There are two sides, marked with separate colors, the green side represents the voltage

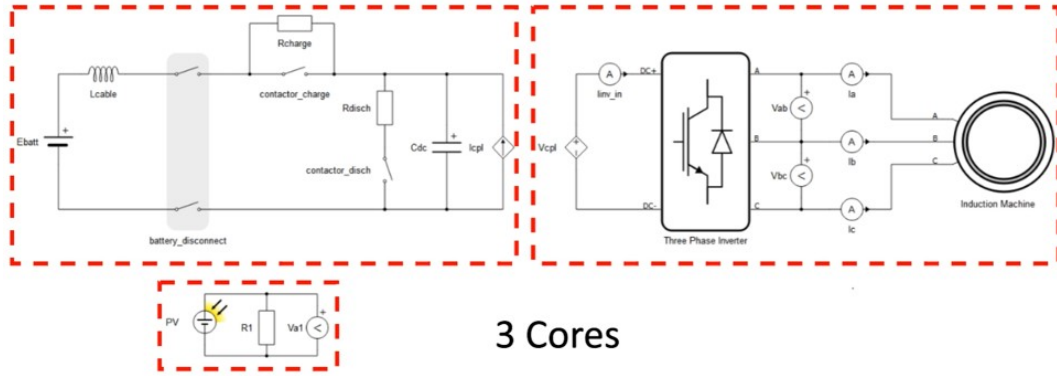


Figure 2.14: Principle of Electrical circuit partitioning [Courtesy Typhoon HIL]

source side and the red side represents the current source side. Due to this, the way in which this component is connected is crucial as it may bring some circuit instabilities during the simulation. In case of any circuit instability, circuit snubbers can be added in parallel to either or both sides of the coupling element [16].

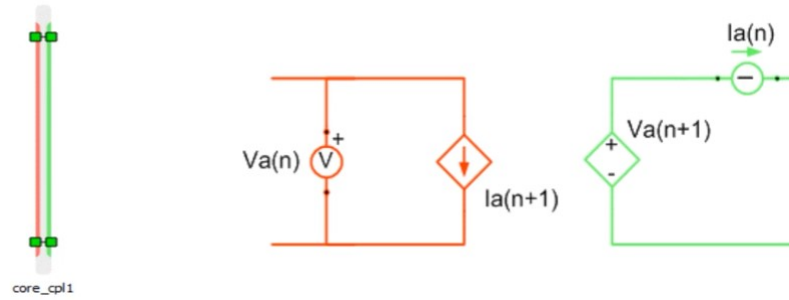


Figure 2.15: IT coupling component [reference]

The Transmission line model (TLM) coupling is also an element that helps to divide a large circuit into smaller sub-circuits. It is based on a transmission line connection. This coupling element unlike the IT coupling is a symmetrical component. Therefore the way in which it is connected doesn't affect the stability of the system simulation. It can be of two types, either capacitive or inductive. Usually, during the coupling of two sub-circuits, an existing capacitor or an inductor is replaced with the TLM. The equivalent model of this element represents a voltage source in series with a resistor. Figure 2.16 illustrates the TLM model component. Based on the working principle of this component, the *Bi-linear* method of discretization must be used, however, when the value of the parameter (inductor/capacitor) is small, the *trapezoidal* method for discretization must be used [17].

As stated previously that Typhoon automatically assigns the unconnected networks to be computed on separate cores, core markers can be used to define and assign explicitly which part of the model or sub-circuit has to run on a particular core [18]. The marker ID on each core marker determines the ID of the core assigned for a particular sub-circuit. Figure 2.17 shows

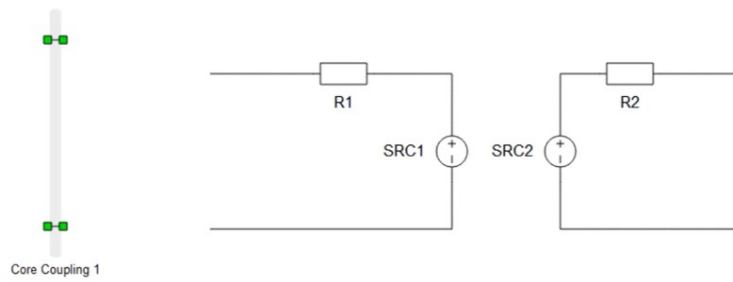


Figure 2.16: TLM coupling component [reference]

how the selected part of the model can be executed on specified cores using the core marker.

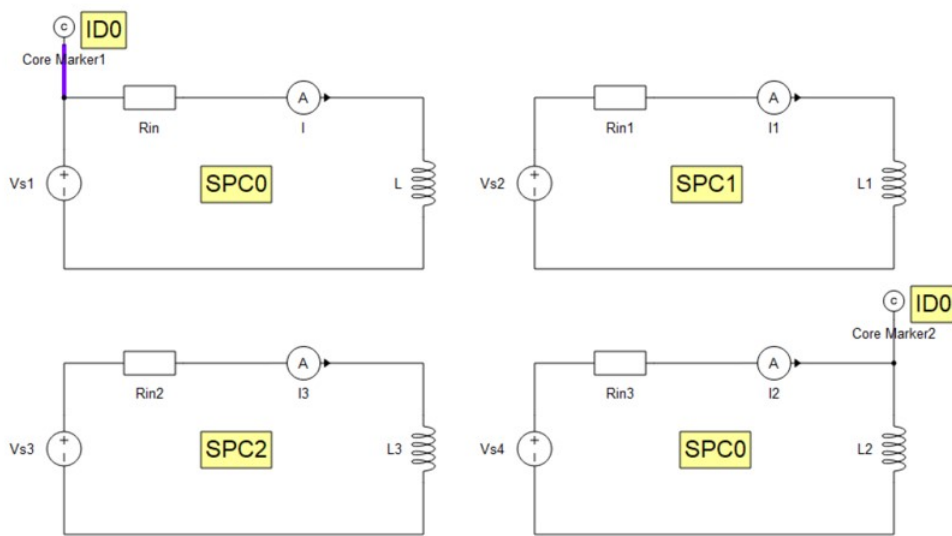


Figure 2.17: Partitioning using core markers [Courtesy Typhoon HIL]

Signal Processing circuit partitioning

As mentioned earlier the signal processing part of the model is executed on a CPU, the execution rate of the signal processing component is an important parameter during the simulation. When the execution rate for the component is reduced the computational load on the CPU increases. However, in certain situations, it is needed to simulate the model with lower execution rates in a few components. When the simulation is carried out at a very low execution rate directly, the time slot utilization of the HIL device is violated and the CIO flag will be raised. In order to simulate with lower execution rate, signal processing partitioning components such as CPU Marker and CPU transition can be used. The CPU marker is used to assign a particular part of the model to a particular CPU [19]. By default, the components that are not assigned any core marker are mapped to CPU Core0. The CPU transition block is used to allow the interaction between the different CPUs of the same HIL device for easy transfer of data. It is important to note that the CPU transition blocks bring an additional time delay of a single

simulation step [20]. Based on the CPU mapping option selected from the model settings, The model partitioning for the signal processing components works in two modes. When the default mode is selected the signal processing components are mapped to the respective CPUs based on the CPU marker ID. In this mode of operation, CPU transition blocks are needed to facilitate communication between different CPUs. When the CPU mapping option is set to execution rate based, then the rate transition block needs to be used. The rate transition block allows the data to be transferred between parts of the model that operate on different execution rates. However, when this is used the entire model is on the same CPU core. Figure 2.18 depicts the different signal processing circuit partitioning components. Figures 2.19 and 2.20 illustrate the use of the CPU core marker, CPU transition, and the rate transition block use.



Figure 2.18: Signal Processing model partitioning components [Courtesy Typhoon HIL]

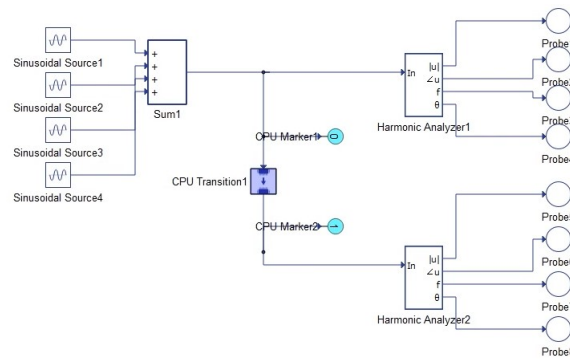


Figure 2.19: CPU Core Marker and CPU transition components usage [Courtesy Typhoon HIL]

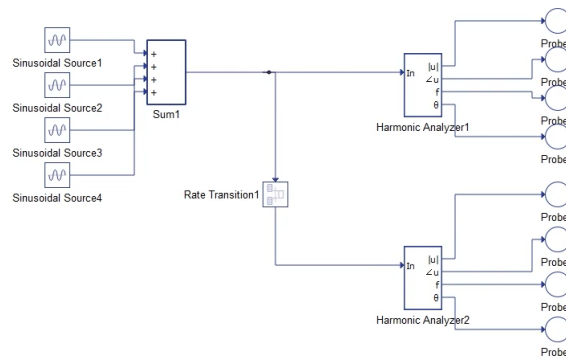


Figure 2.20: Rate transition component usage [Courtesy Typhoon HIL]

2.6. Summary

This chapter summarises the literature review done for Typhoon HIL software and hardware. Primarily before investigating the capabilities of the HIL device, the concept of real-time testing and RT testing methods were studied in detail. The Typhoon HIL 404 architecture was explored in detail with hands-on experience through trials in modeling. The various available tools (Schematic Editor, HIL SCADA, Firmware manager, etc.) within the Typhoon HIL environment were investigated. During the study, the real-time simulation constraints for Typhoon HIL in terms of the number of components that can be modeled and the parameters for the RT simulation were understood. It was concluded that HIL device FPGA resources can be configured manually using the software to utilize them as per the user's need. Through the study, it was found out that, by default, it is not possible to model individual Power electronic switches (such as IGBT/MOSFET) however an IGBT leg or converters can be modeled directly. It was concluded that the model partitioning technique could be used to split the model onto separate cores to be able to implement larger complex models with a significantly large number of components. In a nut shell, this thesis aims to serve as a compiled user handbook on the fundamentals of Typhoon HIL.

3

Open Loop Control of MMC using Typhoon HIL

In this chapter the fundamentals of MMC for HV Testing application are discussed. The different types of Modulation techniques for MMC are described. The Phase Shifted Carrier (PSC) Modulation and its advantages are presented in detail. PSC modulation is implemented in the Typhoon Environment to perform MIL testing. The results of MIL are analyzed and compared with offline simulation.

3.1. MMC Topology

Figure 3.1 below shows the schematic of the MMC with a single leg. For HV testing application, the MMC has to produce test signals across the test object without the transfer of active power, hence a single leg of MMC is sufficient. At the input side of the MMC, the DC link consists of a split capacitor configuration, with the midpoint being grounded. The single leg of MMC is made up of two identical arms called the upper arm and the lower arm. Each arm is made up of several number of cells or Sub-Modules (SM) connected in series along with an inductor and a resistor. The arm inductor is provided to limit the circulating current that flows in the circuit. Since most of the test objects in HV are insulations which can be electrically represented by a capacitor, the load of this converter is a capacitor which represents HV equipment under the test (DUT). Consequently, a resonance is generated between the load and the inductor of the arm, this leads to oscillations. The arm resistance aids in damping these oscillations. Figure 3.1d depicts the structure of the SM of the MMC. These are the fundamental building blocks of the converter and are adapted from the two-level phase leg [21]. As shown in the figure, the SM could either be a Half-bridge or a Full bridge. The half-bridge SM consists of a DC capacitor connected across a phase leg, and the phase leg is usually realized using MOSFET or IGBT switches with anti-parallel diodes. The midpoint of the phase leg and the lower terminal of the capacitor forms the external terminals for the SM. When the switch S1 is turned ON the Voltage across the output terminals of the SM is the voltage of the DC capacitor (V_{cap}). The SM is said to be inserted in this state. When the switch S2 is turned ON, the voltage across the terminals of SM is zero, and the dc capacitor and the SM is said to

be bypassed. It is also possible that both the switches are kept OFF, then the SM is said to be in blocking state. During the blocking state, the direction of the current determines the voltage across the terminals as only the anti-parallel diodes can conduct during this state. When Full Bridge sub-modules are used, it is also possible to achieve a state in which the capacitor is inserted in the opposite way and the voltage across the terminals of SM is $-V_{cap}$. Unlike the half-bridge SM, the full bridge SM in the blocking state will behave like a diode rectifier regardless of the current direction. The voltage across the terminals during this state is (V_{cap}) . Therefore, full bridge SM is capable of producing bi-polar voltage whereas the Half-bridge SM can produce only uni-polar voltage. The string of these SM in each arm can be understood as a controllable voltage source [21], provided that its DC capacitor voltage remains constant. However, this thesis focuses on the analysis of the MMC with Half bridge SM for its simplicity.

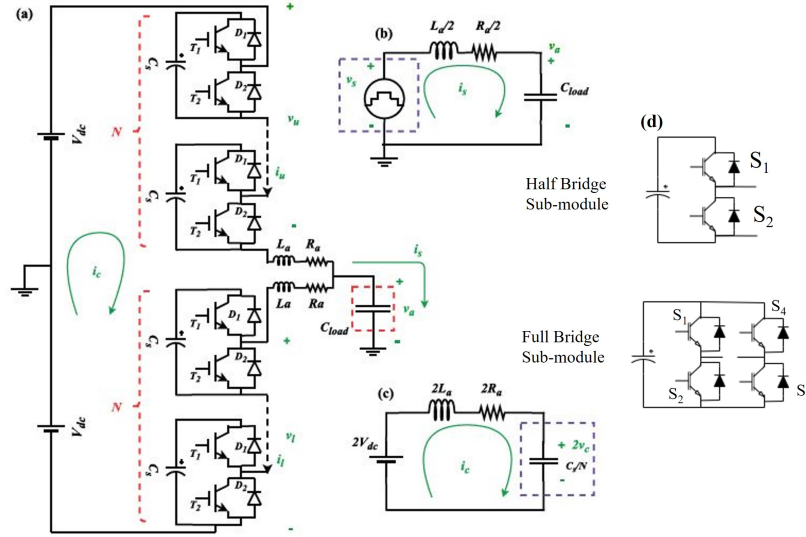


Figure 3.1: (a) MMC schematic (b) Switching voltage equivalent circuit (c) Circulating current equivalent circuit (d) MMC sub-Module topology

To understand the operating principle of the MMC shown above, it is important to obtain the dynamic equations. On applying Kirchoff's Voltage rule on both the arms of MMC, we get equation 3.1 and 3.2 respectively.

$$V_{dc} - v_u - R_a i_u - L_a \frac{di_u}{dt} - v_{load} = 0 \quad (3.1)$$

$$V_{dc} - v_l - R_a i_l - L_a \frac{di_l}{dt} + v_{load} = 0 \quad (3.2)$$

In the above equation, V_{dc} is the voltage across the split capacitor, V_u and V_l is the sum of the inserted SM capacitor voltages of the upper and lower arm respectively. i_u and i_l are the current that flows through the upper and lower arm respectively. Equation 3.3 and 3.4 can be

obtained by adding 3.1 and 3.2 and subtracting 3.2 from 3.1 respectively.

$$2V_{dc} - v_l - v_u - R_a(i_u + i_l) - L_a\left(\frac{di_l}{dt} + \frac{di_u}{dt}\right) = 0 \quad (3.3)$$

$$v_l - v_u + R_a(i_l - i_u) + L_a\left(\frac{di_l}{dt} - \frac{di_u}{dt}\right) = 0 \quad (3.4)$$

The Switching voltage v_s is defined as the internal Electromotive force (EMF) which is generated due to the insertion and bypassing of different SM capacitors. The circulating current is represented as i_c and the difference between the upper arm and the lower arm current is the output current i_s . The equations 3.3 and 3.4 are coupled equations. In order to partially decouple them, we can use the relation between the quantities of the upper and lower arm as shown below.

$$i_s = i_u - i_l, \quad V_s = \frac{v_l - v_u}{2} \quad (3.5)$$

$$i_c = \frac{i_u + i_l}{2}, \quad V_c = v_u + v_l \quad (3.6)$$

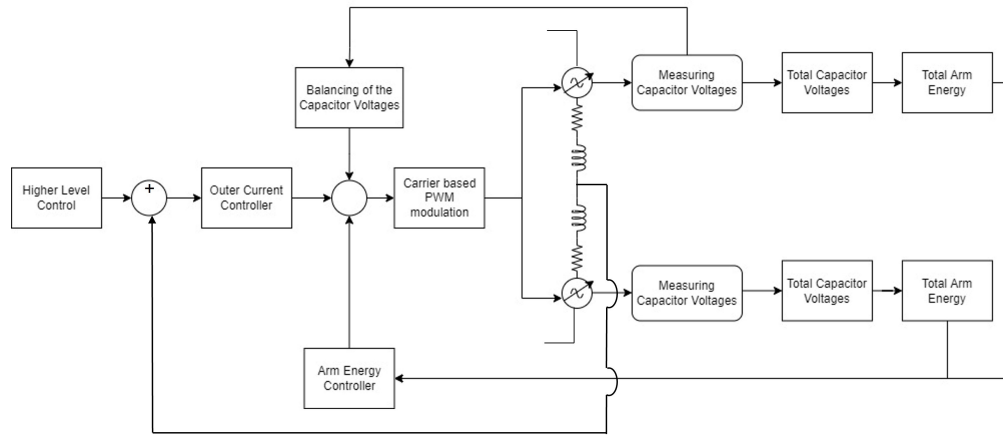
$$V_{dc} - v_c - R_a i_c - L_a\left(\frac{di_c}{dt}\right) = 0 \quad (3.7)$$

$$v_s - \frac{R_a}{2} i_s - \frac{L_a}{2} \frac{di_s}{dt} - v_{load} = 0 \quad (3.8)$$

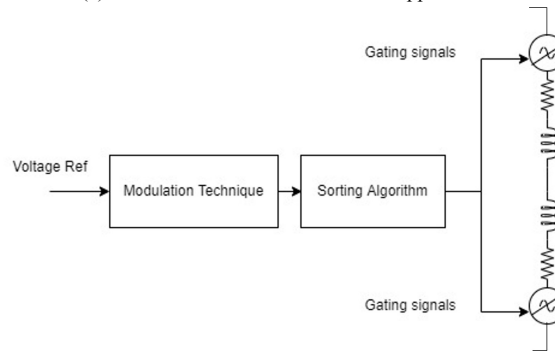
v_c can be interpreted as the voltage which generates the circulating current in the circuit, and is called the circulating voltage. After multiplying equation 3.7 with two, it is possible to represent this equation with the circuit shown in figure 3.1c, where two times the circulating voltage can be represented as the voltage across an equivalent capacitor which is C_s/N (As the sub. As the two arms of the MMC are in parallel, an equivalent circuit as shown in figure 3.1b can be formed which represents equation 3.8 as an RLC circuit.

3.2. Control Strategy

As mentioned in Chapter 1, this thesis intends to investigate the potential of MMC to obtain conventional (Sinusoidal power frequency) and non-conventional (Lightning impulse superimposed) waveforms for HV testing application. Therefore, it is important to understand that the HV testing application imposes a different set of challenges than the conventional HVDC Power application [1]. When the MMC is operating as an HV test source, the transfer of active power to the load is very low as compared to a conventional HVDC converter application, the only power transfer that takes place is the reactive power transfer to the load. This is used to charge the DUT to the given voltage. Moreover, the MMC test source is used only during the test duration and hence not designed for continuous operation, which is the case for MMC-based Power converter. Since the transfer of active power is really low in an MMC-based test source, the performance of the test source is measured not by the converter efficiency, but by the ability of the MMC to generate voltage waveforms with higher accuracy and large signal



(a) MMC control scheme for Power Application



(b) MMC Control for HV testing application

bandwidth.[16]. Therefore, it can be seen that the choice of control strategy will be crucial in determining the performance of the test source. The control scheme for MMC-based HVDC converters is made up of several closed loops which are interleaved [21]. The Higher level control consists of a Phase locked loop (PLL), which synchronizes the ac bus voltage vector with the dq reference frame of the converter control system. The DC bus voltage and the AC bus voltage are synchronized by controlling the reactive and active power in an open loop manner. The voltage of the DC bus is regulated by the means of active power control. The output current of the converter is sensed and given to a Proportional Resonant converter (PR) to produce the reference for voltage. Either the Arm energy controllers or sorting algorithms are used to balance the capacitor voltages in a particular arm [21]. For an HV testing application, the control system for the MMC is significant since there is no output current control as the active power transfer is too low. The control system for power application and HV testing application is shown below in figure 3.2a and 3.2b respectively.

3.3. Modulation Techniques

Based on the switching frequency of the output signal, the modulation techniques are classified as high-frequency or low-frequency modulation. Pulse width Modulation (PWM) waveforms are generated as a result of the high-frequency modulation technique, whereas staircase signals close to fundamental frequency are generated as a result of low-frequency modulation.

3.3.1. High Frequency Modulation

The high-frequency modulation includes the approach of using either space vectors for modulation or the conventional carrier-based modulation.

Space Vector Modulation (SVM)

Carrier signals are not needed in the SVM technique to generate the gate pulses for the switches of the converter. For example, in a three-phase two-level converter there are total 6 switches (Two complementary switches per leg) and therefore 8 states are possible. The 8 states are listed below in table 3.1. The reference vector is generated by taking the time average of the

Vector	Leg state 1	Leg 2 state	Leg 3 state
U_1	1	0	0
U_2	1	1	0
U_3	0	1	0
U_4	0	1	1
U_5	0	0	1
U_6	1	0	1
U_7	0	0	0
U_8	1	1	1

Table 3.1: Possible State for Two level converter

adjacent vectors of a particular sector [22]. For example, in the figure 3.3 shown below the reference vector U_{ref} is created by adjacent vectors U_3 and U_4 of sector 3. For a two-level converter, the implementation of the SVM technique is quite straightforward and requires less effort, however for Multi-level converter topologies such as MMC, the number of possible states is very high and hence the hexagon structure is very complicated, hence the implementation of this technique is quite cumbersome. Therefore, this type of modulation technique is not investigated further in this thesis.

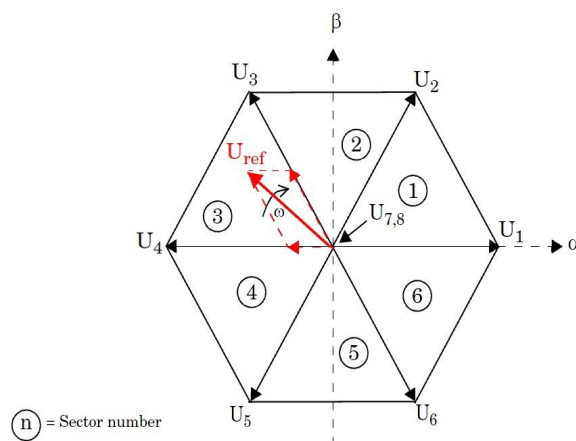


Figure 3.3: SVM for two-level converter [23]

Carrier Based PWM

Sine width Pulse width modulation (SPWM) for multi-level converters is also called multi-carrier PWM. This modulation technique is used very often as it is relatively easy to implement for low voltage modules [24]. The multi-carrier PWM can be divided into two categories: 1) Level Shifted PWM and 2) Phase Shifted PWM.

Level Shifted Carrier Modulation

The level shifted PWM is further divided into three types: Phase opposition disposition (POD), Phase disposition (PD), and Alternative phase opposition disposition (APOD). The main difference between them is the phase angle between the carriers. In PD Level shifted PWM, the phase angle difference between the carriers is zero (i.e all are in phase). In the POD method, the carriers above the axis are in phase but are out of phase with the ones below [24]. In the APOD method, all carriers are phase shifted by 180° (i.e two adjacent carriers are out of phase).

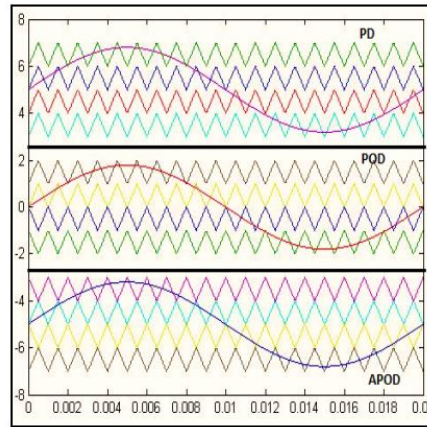


Figure 3.4: Carrier signals for Level Shifted Carrier PWM [25]

Phase shifted Carrier (PSC) Modulation

For a multilevel Converter with N number of SM per arm, each SM has a dedicated carrier signal which is phase shifted by $\frac{2\pi}{N}$. However, all the SMs are given a common reference signal. The phase difference between the upper arm carriers and lower arm carriers could either be zero or $\frac{\pi}{N}$. The PSC modulation can generate $N+1$ levels or $2N+1$ levels in the output voltage. Based on the phase difference between the carrier signals of both arms, the output voltage can have either $2N+1$ or $N+1$ levels. This is summarised in the table 3.2 below. When PSC with $N+1$ level is used, the output voltage has the carrier harmonics shifted to N^{th} carrier frequency [26]. Likewise, when PSC with $2N+1$ is used the output signal has carrier harmonics moved to $2N^{th}$ Carrier Frequency. The advantage that the PSC modulation has over the level shifted carrier modulation is that in PSC inherently all the SMs are utilized evenly [27]. Therefore, sorting and capacitor voltage balancing needs are drastically reduced as compared to Level shifted carrier modulation.

	N+1	2N+1
N is Even	Phase shift between Upper and Lower arm carrier is 0	Phase shift between Upper and lower arm carrier is π/N
N is odd	Phase shift between upper and lower arm carrier is π/N	Phase shift between upper arm and lower arm carrier is 0

Table 3.2: PSC parameters

3.4. Low Frequency modulation

The low-frequency modulation techniques do not use carrier signals to generate gating signals. There are two techniques under this category: Selective Harmonic Elimination (SHE) and Nearest level control (NLC). These techniques generate a staircase-type signal in the output.

Selective Harmonic Elimination

In this type of modulation, based on the required harmonic performance gate pulses are generated. The switching angles in the converter are controlled to control the notches in the PWM signals to get the desired harmonic performance. Therefore, this type of modulation technique is more suitable for power applications and not for HV testing applications.

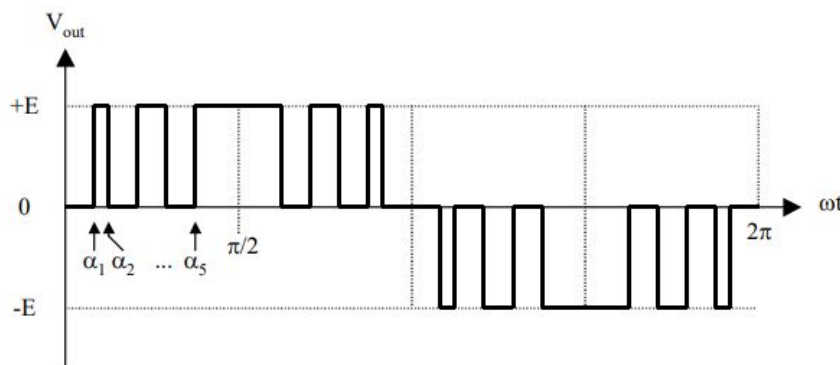


Figure 3.5: Working principle of SHE[23]

Nearest Level Control

In this technique, the number of SMs to be inserted is calculated. Both N+1 and 2N+1 levels can be achieved using the NLC modulation. However, here the modulation index and the number of SM determine the frequency of switching. The advantage of this technique is that the circulating current magnitude is small and therefore the voltage ripple across the SM capacitor is very small compared to other techniques. When the modulation index is low then not all SM

will be inserted, only some of them always get inserted. Therefore, all SMs are not evenly used as in the case of PSC. Therefore, to make sure all SM are inserted evenly, a sorting algorithm is usually implemented with this technique. One of the main disadvantages of this method is that the output voltage has many lower order harmonics [26], therefore the filter requirements are very high. The staircase output is shown in figure 3.6b

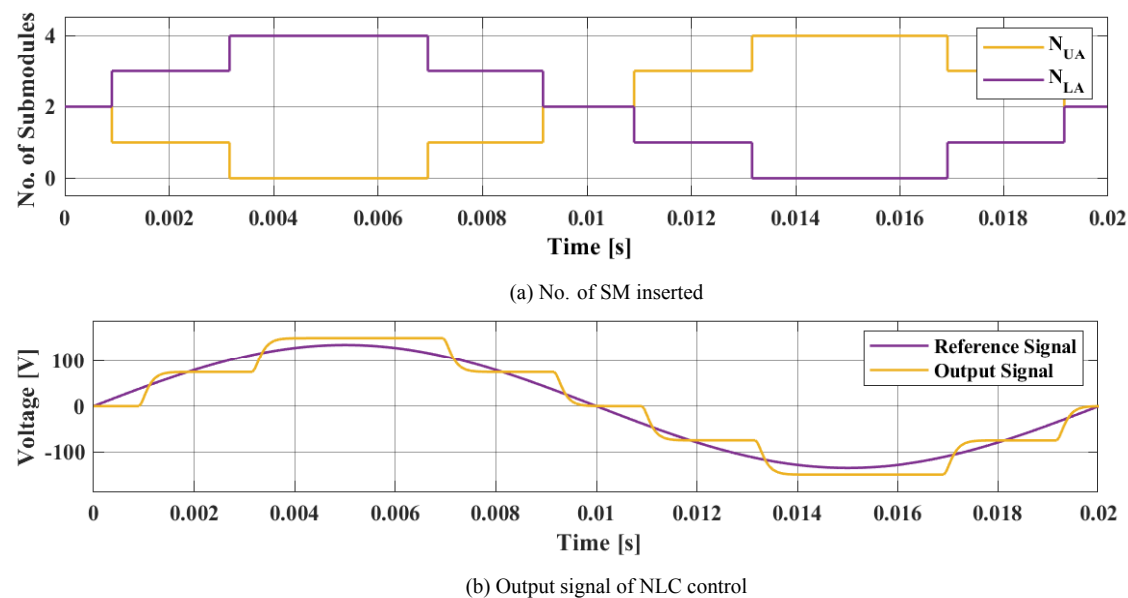


Figure 3.6: NLC modulation technique

The PSC modulation technique has better harmonic performance than NLC and therefore has lesser filter requirements. However, it is easier to implement physically the NLC technique than the PSC technique, especially when the number of SMs increases and closed loop control is implemented. Considering the fact that one of the goals of this thesis is to investigate the computational capabilities of Typhoon HIL, the PSC modulation has been selected for the implementation of the control of MMC as it is more computationally demanding. Open loop control of MMC using typhoon HIL is depicted in the next section.

3.5. Open Loop control of MMC on CPU of Typhoon HIL

In this section, the implementation of the open loop control of MMC on the user CPU of Typhoon HIL is described in detail. Primarily, a MIL simulation was performed with a reduced number of SMs to validate the control strategy developed in the Typhoon HIL Schematic editor. Later on, this control strategy was extended for a higher number of SMs.

Typhoon HIL 404 is used as the RT simulator for all the research and testing carried out during the thesis. MIL simulation refers to developing the Control algorithm and the Plant as models within the software. The electrical Power Electronics components were modeled on the

FPGA Solver, whereas the control was implemented using the signal processing components on the user CPU. Since the HIL 404 device belongs to the HIL 4 series, there is a limitation to the number of Signal Processing and Power Electronics components that can be modeled at a given time. The number of components available depends on the HIL device itself and the configuration of the HIL device. As mentioned in chapter 2, the configuration of the device helps to utilize the resources available on the HIL hardware to be used flexibly. The configuration of the device can be changed by going to the 'Firmware Manager' tool at the beginning in the Typhoon HIL control Center. Hence, **Configuration 3** was selected to get the maximum available converter weight per Core of the device. The specifications of Configuration 3 are depicted in table 3.3 below:

Feature	Configuration 3
Number of SPCs	2
Number of Signal Generators	12
PWM Channels	12
Max converter Weight/SPC	4
Switch-Level GDS Oversampling	ON

Table 3.3: Relevant features of Configuration 3

The Half bridge topology was implemented for modeling the SMs. Since Typhoon does not provide Semiconductor switches to be modeled individually (However, IGBT and Thyristor switch models can be made available on special request), Converter block sets in the form of IGBT legs were used to model the Half-bridge SMs. As each IGBT leg holds a converter weight of 1, a total of 4 SMs were implemented on the FPGA solver. The passive network in the MMC which consists of the capacitive load (DUT), arm inductor, and arm resistor acts as an RLC filter, which can be tuned accordingly to improve the quality of output voltage across the test object. The values of arm Inductance (L_a) and arm resistance (R_a) were taken based on the filter designed in [1]. Despite the ability of Typhoon HIL 404 to simulate the model in RT with a simulation time step of 200 ns, due to the complexity of the model with many Power and Signal processing components modeled within the software, the simulation time step was set to 500 ns. The CPU is usually used to simulate sub-models of the signal processing system, therefore the simulation step for the CPU is either equal to the simulation time step of the FPGA circuit solver or a multiple of it. Here, the simulation step for the CPU was equal to the FPGA time step as the time utilization constraints were met. The discretization method for the circuit solver was set to the exact method. There are four options available: 1) Exact 2) Trapezoidal 3) Euler and 4) Bilinear. The first one is used the most and recommended to use, the other three are used only in special cases, such as when there are memory constraints or in the case of Electrical core partitioning using TLM(Transmission line model) [17]. The circuit parameters considered for modeling on both the CPU and FPGA are listed in the table 3.4

The PSC control strategy implemented in the Schematic editor is depicted in figure 3.7 below. The control strategy was implemented to achieve $2N + 1$ Levels in the switching output voltage. Therefore, the phase difference between the carriers of each arm was $\frac{2\pi}{N} = \frac{360^\circ}{2} = 180^\circ$. Moreover, the phase difference between the upper arm and lower arm respective carriers was

Variables	Values
Fundamental frequency	50 Hz
Switching frequency(f_{sw})	10 kHz
Modulation Index of reference	0.8
Arm Inductance (L_a)	3 mH
Arm Resistor (R_a)	60 Ω
Load Capacitance (C_{load})	100 nF
SM Capacitance	75 μ F

Table 3.4: Simulation Parameters of MMC control

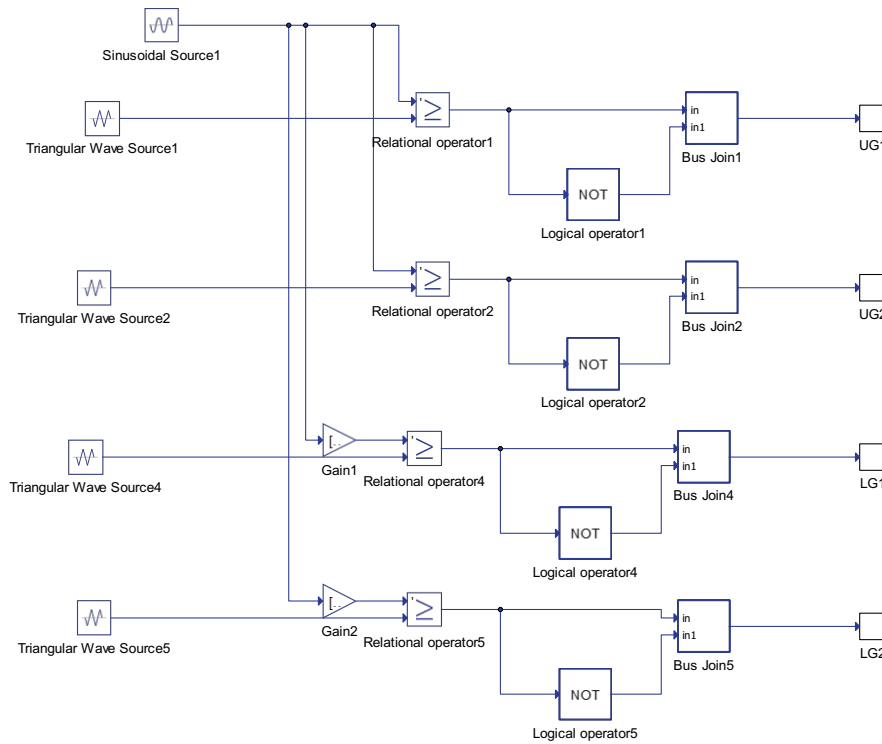


Figure 3.7: PSC control strategy for MIL testing of MMC in Typhoon HIL

set to $\frac{\pi}{N} = \frac{180^\circ}{2} = 90^\circ$. The MIL simulation was performed in RT, and the Voltage and currents across various components of the circuit were measured and compared with that of an offline Simulation. MATLAB was used as an offline simulation tool. The simulation criteria were kept similar in both the offline and RT simulation so that the results are comparable. The Output voltage across the DUT, output current, circulating current, and the switching voltage were measured and analyzed. The comparison between the RT and offline simulation is shown below from figures 3.9-3.11 below. In Figure 3.8, the $2N + 1$ levels (i.e For $N=2$, 5 levels) were observed in the output switching voltage. In figures, 3.9, 3.10 and 3.11, The output sinusoidal voltage, output current, and the circulating current were observed respectively and found identical to the offline simulation results. Therefore the results from the comparison

help to validate the control strategy developed in typhoon HIL.

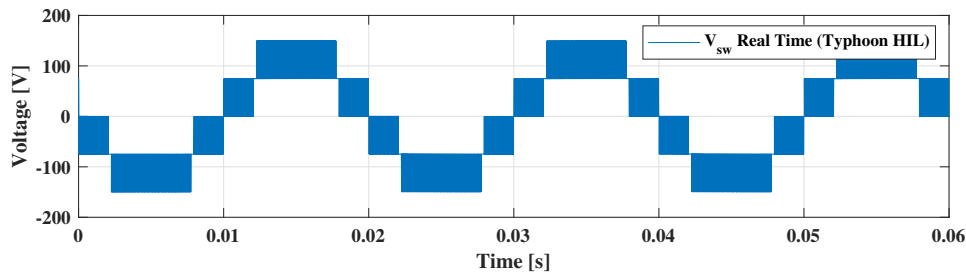


Figure 3.8: Switching voltage - Real-time Simulation

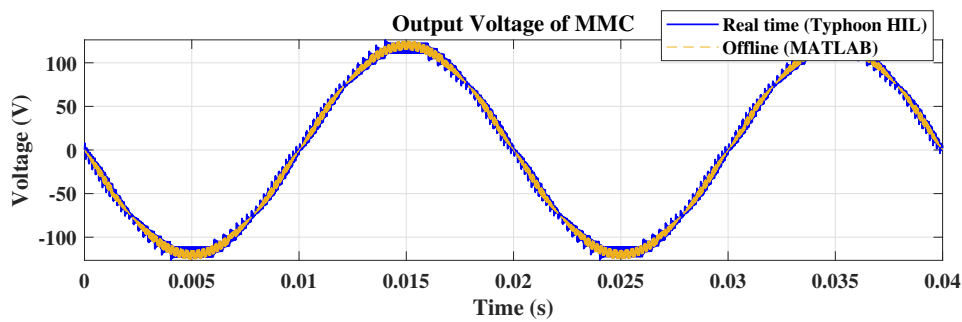


Figure 3.9: Output voltage across DUT

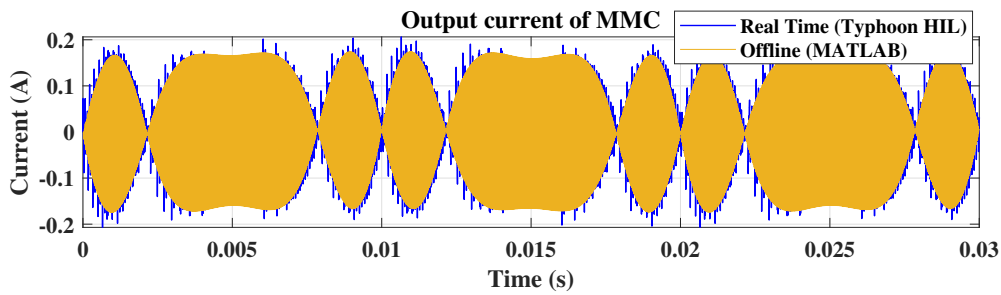


Figure 3.10: Output current of the MMC HV Test source

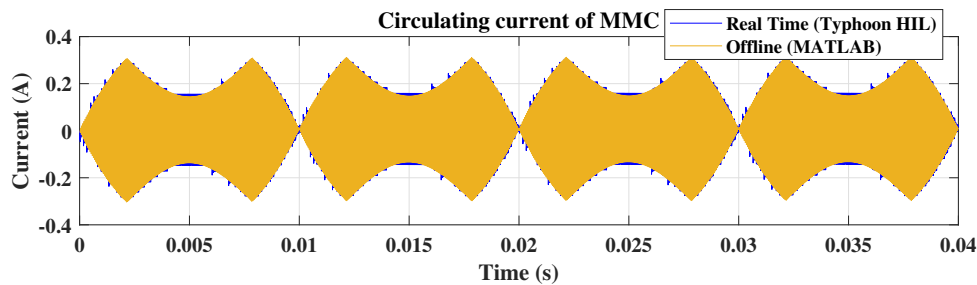


Figure 3.11: Output current of the MMC HV Test source

3.6. Output Voltage at Higher Frequencies

One of the main features of the MMC-based HV Test source is that it should be able to generate HV sinusoidal output voltage over a significant bandwidth. However, this depends mostly on the accuracy of the control technique used to generate high-frequency output signals. Since the PSC control was discussed and implemented in the previous section, the discussion on the accuracy of the control strategy will be limited to this technique only. The accuracy of the gate pulses generated by PSC control is mainly dependent on the quality of the Carrier signal and the reference signal. Therefore, in this section, the abilities of the Typhoon HIL RT simulator to generate high-frequency control signals are investigated.

An open loop control model was developed on the User CPU for 8 SMs (4 in each arm). The gate pulses generated were accessed through the digital Output ports of the HIL Device via the HIL Breakout Board. The HIL breakout board is an interface which can be used for accessing all the I/Os of the device with ease. The breakout board is a passive board which can be connected to all series HIL devices. The signals from the board are made available via toolless spring cage terminal blocks[28]. The layout of the board is shown below in figure 3.12.

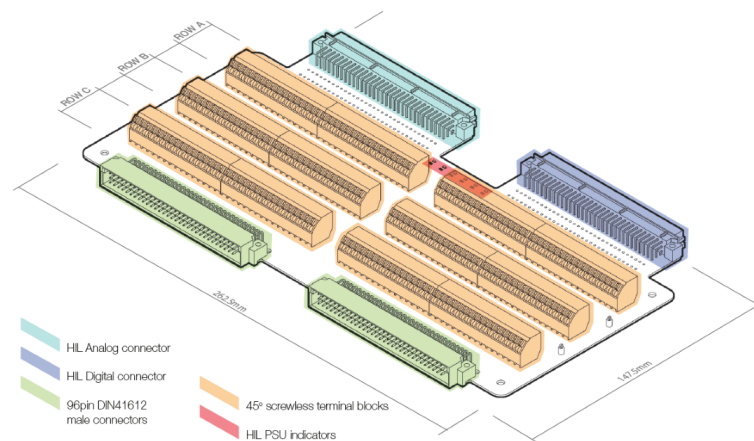


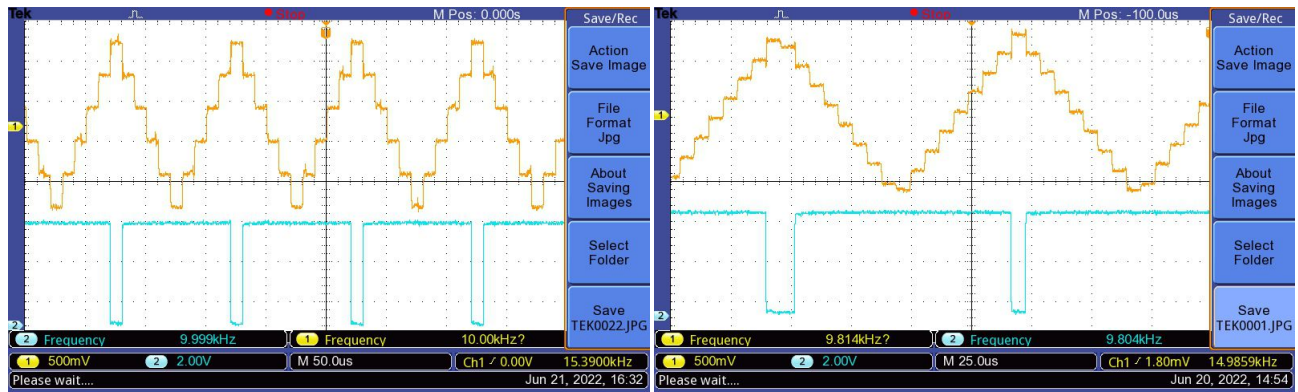
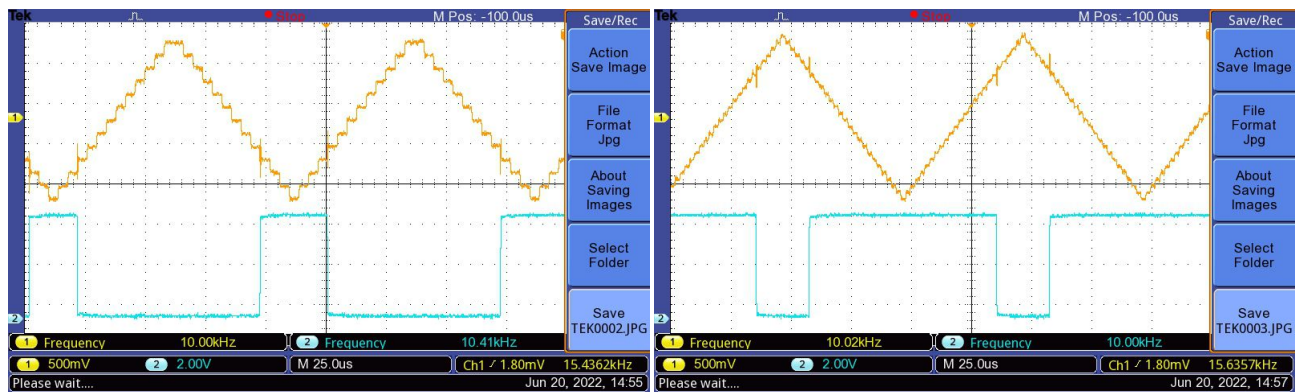
Figure 3.12: Typhoon HIL Breakout Board

The Digital signals from the board were connected to an oscilloscope to analyze and record the signals. The accuracy of the gate pulse was analyzed by simulating the open loop control in RT for different switching frequencies, fundamental frequencies, and execution rates. The execution rate can be understood as the rate at which the signal processing component transmits data. Typhoon HIL toolbox supports only discrete-time execution rates[29]

Case I

The switching frequency (f_{sw}) was set to 10 kHz and the Fundamental reference frequency (f_{ref}) was set to 50 Hz. The carrier frequency signal and the output gate pulse signal were recorded using the scope. The yellow-colored signal in the figures below corresponds to the triangular carrier wave and the cyan-colored waveform refers to the PWM gate pulse.

The simulation for case 1 was carried out with a simulation time step of 500 ns. From figure 3.13 and 3.14 it was observed that the quality of the triangular carrier improved as the execution

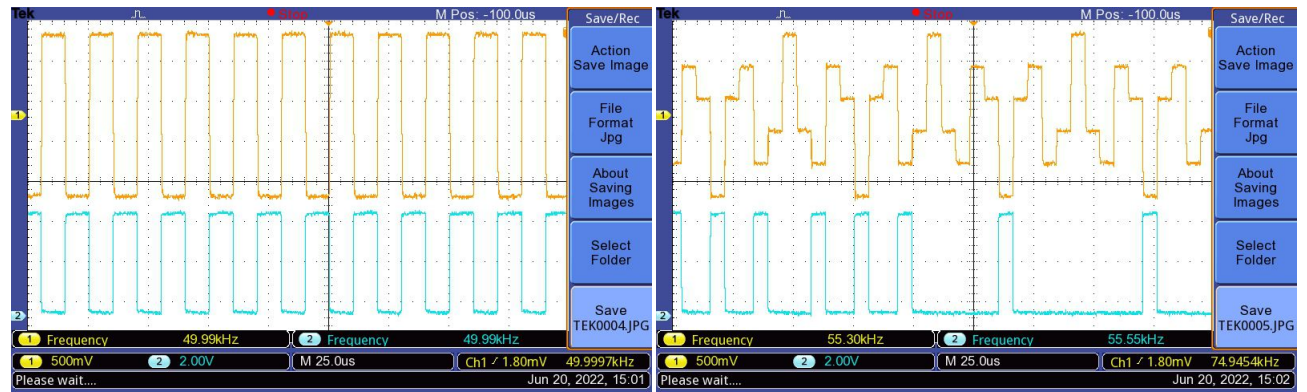
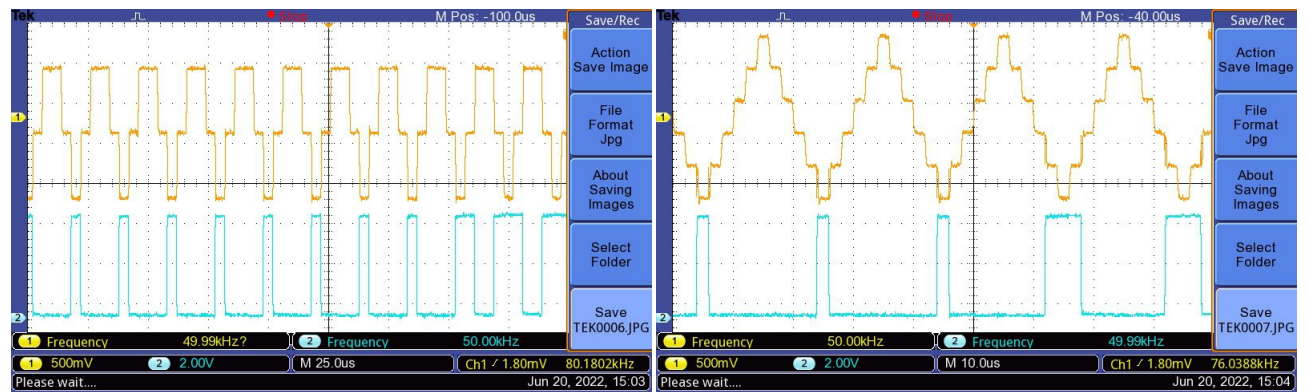
Figure 3.13: a) Execution rate of 10 μ s b) execution rate of 6 μ sFigure 3.14: a) Execution rate of 4 μ s b) execution rate of 2 μ s

rate was reduced from 10 μ s to 2 μ s. However, there is a trade-off associated, as the execution rate reduces, the time slot utilization increases rapidly. This is due to the fact that now in RT simulation, within the same time step, data from the signal processing component is executed at a faster rate.

Case II

In this case, the switching frequency (f_{sw}) was set to 50 kHz and the Fundamental reference frequency (f_{ref}) was set to 1 kHz. The carrier frequency signal and the output gate pulse signal were recorded using the scope. The yellow-colored signal in the figures below corresponds to the triangular carrier wave and the cyan-colored waveform refers to the PWM gate pulse. It is usually expected that as the frequency increases the number of steps in the waveform would increase for a given time step and a given execution rate. This is also seen from the simulation results in figure 3.15 and 3.16.

When the execution rate was 10 μ s and 6 μ s, typhoon HII could not generate a triangle carrier signal with 50 kHz frequency. The waveform somewhat improved when the execution rate was kept to 2 μ s. Despite a very small simulation time-step of 500ns and an execution rate of 2 μ s, the carrier waveform still has steps and is not as smooth as required for accurate PWM gate pulse generation.

Figure 3.15: a) Execution rate of 10 μ s b) execution rate of 6 μ sFigure 3.16: a) Execution rate of 4 μ s b) execution rate of 2 μ s

Accuracy of Sinusoidal reference

The Sinusoidal reference determines the frequency of the the output voltage across the test object, when the conventional method of Sine Wave Pulse width modulation (SPWM) technique is used. Similar to the triangular carrier, as the frequency of the reference signal is increased, the quality of the signal reduces as more and more steps are introduced. This is depicted from figure 3.17. It was observed that up to 5 kHz, there are almost no steps in the reference signal. However, more significant steps are seen from 10 kHz onwards as the frequency increases. Therefore, both the triangle wave and the sinusoidal reference generation at higher frequency puts a limitation on the generation of PWM pulses through control implemented on the CPU. However, this can be resolved to a significant extent by modeling the control on FPGA. This is because the FPGA comprises of a multi-core processor which has a higher computational power than the CPUs. The implementation of the Open-loop control on the FPGA and the comparison of the gate pulses with the CPU is described in the next section.

Control of MMC on FPGA

The FPGA-based PSC modulation can be implemented using the PWM modulator block available in the Typhoon HIL library explorer. A dedicated hardware is allocated to the PWM modulator to generate very accurate high-frequency symmetrical triangular signals[27]. The PWM

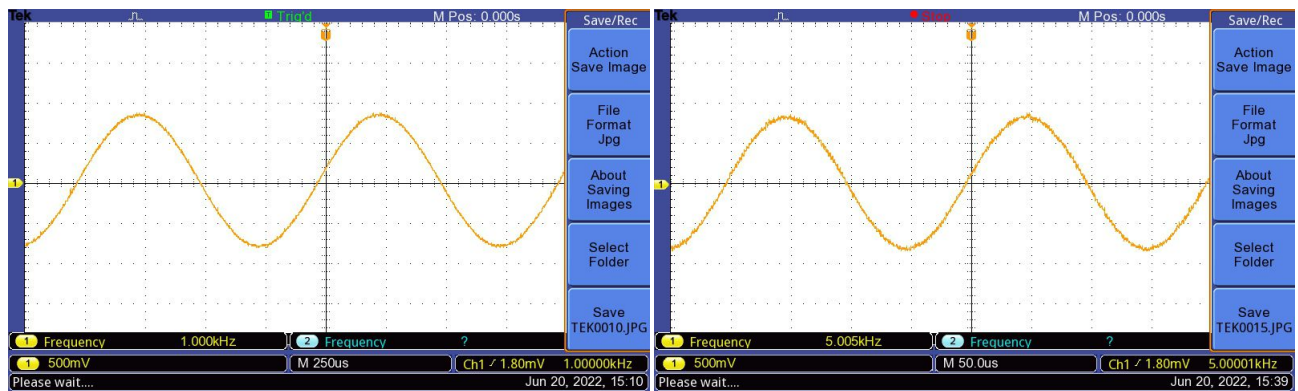


Figure 3.17: a) Sinusoidal reference at 1 kHz b) Sinusoidal reference at 5 kHz

modulator operates at the device clock frequency, which is 280 MHz for HIL series 4 devices. Carriers from 100 Hz to 500 kHz can be generated with very high-resolution [8]. The triangular signals are hardware integrated, therefore, they cannot be individually accessed. However, the reference signals for PWM modulation need to be provided externally either through a physical signal or through a source modeled on the CPU. The modulator can be configured manually to operate in various modes such as 'fixed/variable phase offset' mode or 'fixed/variable carrier frequency mode'. The execution rate of this component can be set by the user to improve the accuracy of the PWM pulses. The component can also incorporate, dead times of the desired duration between the complementary switches to prevent shoot-through of the DC source. The modulator allows the use of up to 12 channels. figure 3.18 below shows the properties of the PWM modulator.

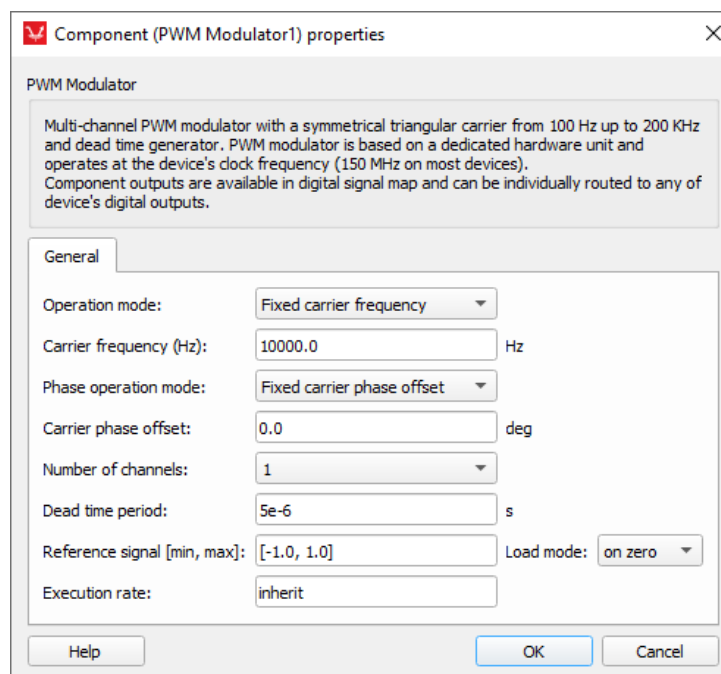


Figure 3.18: PWM modulator Properties[27]

Implementation of PSC modulation using PWM modulator

The PSC control was developed for 8 SMs using the PWM modulator. The phase offset feature was used to create the desired phase difference between the carriers. The reference terminal of the modulator was connected to a sinusoidal source modeled on the user CPU. The gate pulses were recorded in the form of digital signals using an oscilloscope. The gate pulses obtained from the PWM modulator and CPU control were compared with the help of Fast Fourier Transform (FFT) Analysis. Figures 3.19 and 3.20, depict the comparison between the gate pulses when the switching frequency was set to 10 kHz and 50 kHz respectively. For both cases, the sinusoidal reference was set to 1 kHz. In figures 3.19, 3.20 and B.3, the green signal

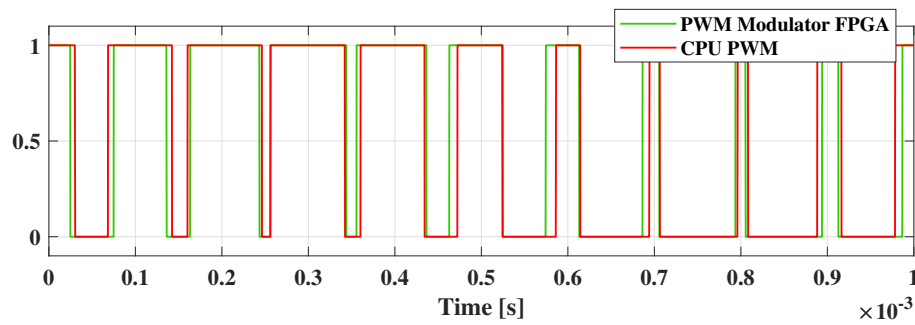


Figure 3.19: Gate Pulse comparison for 10 kHz switching frequency

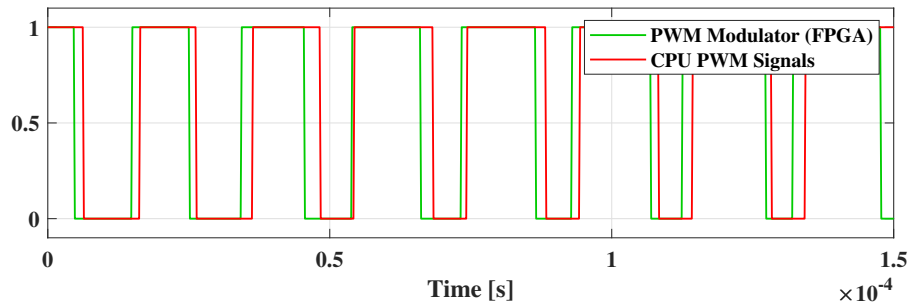


Figure 3.20: Gate Pulse comparison for 50 kHz switching frequency

corresponds to the gate pulse generated from the PWM modulator whereas the red signal corresponds to PWM signal generated from CPU control. It was observed from the figures above that when the switching frequency was 10 kHz, the gate pulses from CPU control and FPGA control were somewhat similar. This was also reflected in their FFT Analysis, as it can be seen that both the FFT plots are quite similar. However, when the switching frequency was increased to 50 kHz, the gate pulses were no longer identical. It was observed that the FFT Plot of the PWM signal generated using the PWM modulator and the CPU were significantly different. In fact, the FFT of the PWM signal from the modulator was very identical to that from offline simulation, as shown in figure 3.22.

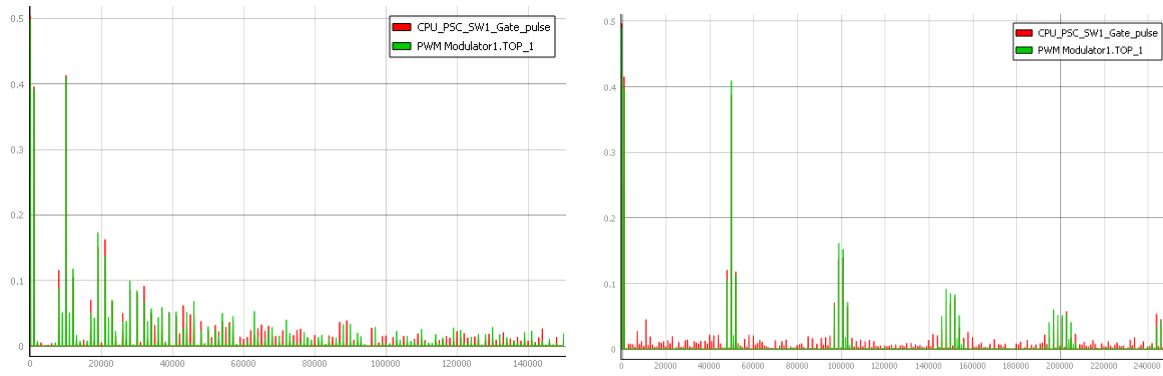


Figure 3.21: FFT of Gate pulses with a) 10 kHz b) 50 kHz

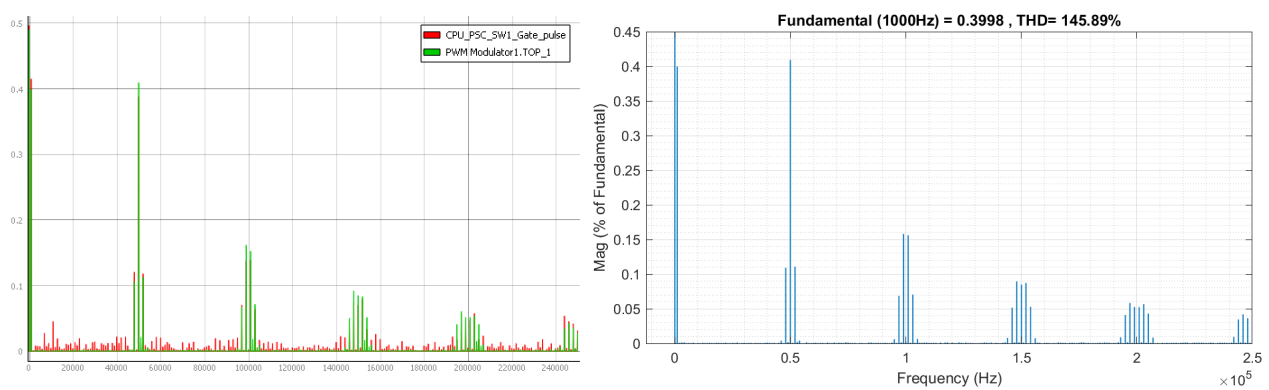


Figure 3.22: FFT of Gate pulses with a) 50 kHz b) 50 kHz (Offline Simulation)

The difference in the FFT plot of the PWM signal generated from CPU control and an offline simulation is due to the fact that as the switching frequency increases, the carrier signals generated from the CPU have an increased number of steps in them. This results in an inaccuracy during the comparator operation with the reference wave. Therefore, it can be concluded that at the lower switching frequency, the CPU can generate PWM gate pulses with reasonable accuracy, however, at higher frequencies, the FPGA-based PWM modulator should be used to generate Accurate Pulses.

3.7. Comparison with OPAL-RT

Like the Typhoon HIL, OPAL-RT is a real-time simulator, which is made up of a multi-core CPU and an FPGA board from Xilinx [30]. One of the goals of this thesis is to investigate the capabilities of the Typhoon HIL RT simulator and compare its performance with OPAL-RT in regards to generating accurate gate pulses. In this section, the ability of the RT simulator to generate accurate sinusoidal references has been discussed in detail. For the comparison, Typhoon HIL 404 and the OPAL-RT 5600 simulator were taken. Almost, identical simulation conditions were implemented to develop a PSC-based open-loop control in the CPUs of the respective RT simulator. Figure 3.23 and 3.24, are an indicative of the difference between the two RT simulator. It was observed that for a fundamental frequency of 1000 Hz, the signal

generated by Typhoon was very smooth without any steps in the waveform, whereas the signal generated by OPAL-RT had many steps, thereby reducing the accuracy of the gate pulses generated as compared to Typhoon HIL. The situation became even worse when the fundamental frequency was made to 5 kHz, OPAL-RT signal was made up of huge steps, whereas the signal from typhoon HIL was much smoother and with relatively small-sized steps. This is due to the fact that the minimum time step of the CPU that could be achieved with the OPAL-RT was around $10\text{ }\mu\text{s}$, whereas it was possible to execute the simulation with a CPU time step of around $1\text{ }\mu\text{s}$. Moreover, with relatively simplified models, it is possible to execute the simulation in RT using typhoon HIL with a time step less than $1\text{ }\mu\text{s}$. This concludes that the CPU performance of the Typhoon HIL is superior to that of the CPU of OPAL-RT to generate accurate gate pulses for higher fundamental frequencies.

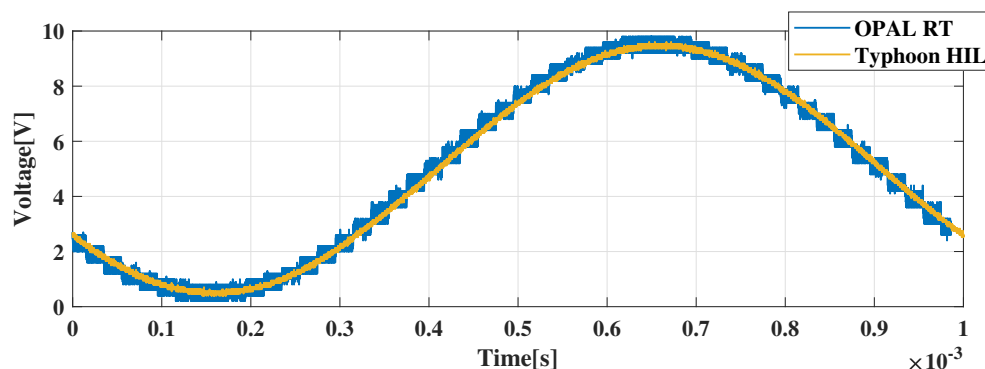


Figure 3.23: Sinusoidal Reference Comparison (1 kHz)

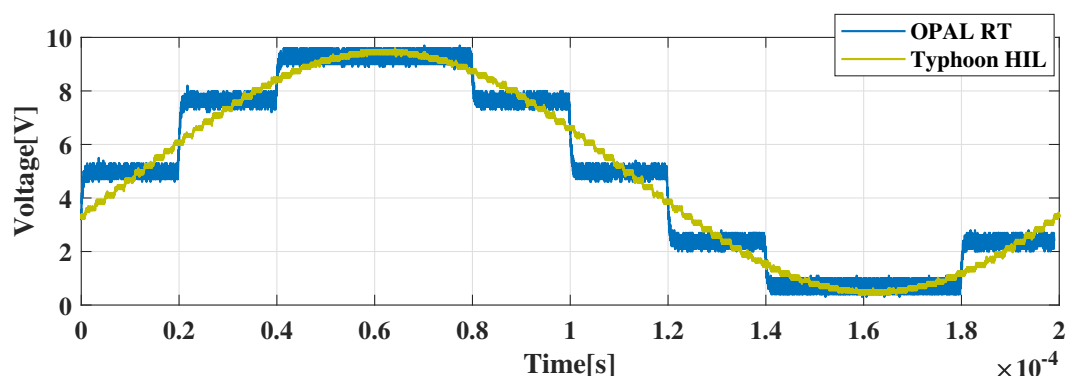


Figure 3.24: Sinusoidal Reference comparison (5 kHz)

3.8. Summary

The chapter summarizes the implementation of the Open Loop control for MMC-based HV testing applications. The MMC topology work was studied and analyzed in detail. A thorough literature review was carried out on the different Modulation techniques to implement the open-loop strategy. The Phase shifted carrier (PSC) modulation technique was selected

over the nearest level control (NLC) technique. This was because in PSC modulation all the sub-modules in any given arm are evenly utilized which helps to ensure balancing of the capacitor voltages. Also, one of the objectives of this thesis is to test the capabilities of Typhoon HIL, therefore PSC was selected over NLC as it is computationally more demanding. Due to the real-time simulation constraints specified in the previous chapter MIL testing was performed with 2 Sub-modules in each arm. It was inferred that the results of the MIL were identical to the simulation results from the offline simulation. Furthermore, the Open loop strategy with PSC modulation was implemented in the typhoon environment on the CPU. It was observed that the execution rate drastically affects the quality of reference and carrier signals generated on the CPU of the HIL device. It was concluded that at a given execution rate when the switching frequency of the PWM technique was increased the quality of the triangular carriers was affected (i.e it shows steps). It was deduced that on reducing the execution rate of the signal processing components the quality of the carrier signals and gate pulses was improved. However, on decreasing the execution rate the computational load on the CPU increases and this violates the timing constraints. In order to implement the control with higher switching frequencies, the open loop control was implemented using PWM Modulator (based on dedicated FPGA hardware). The results from FPGA and CPU were compared with offline simulation and it was observed that the gate pulses generated from FPGA closely resembled the pulses from offline simulation. One of the objectives of this thesis is to compare the capability of Typhoon HIL and OPAL-RT in terms of implementing the control for MMC-based test source. The ability to generate accurate gate pulses at higher fundamental frequencies was analyzed. It was observed that Typhoon HIL could generate smooth sinusoidal reference signals up to 5 kHz with very small steps. However, OPAL-RT showed large steps in the reference waveform starting from 1 kHz itself. Therefore, it was concluded that Typhoon HIL is capable of generating more accurate gate pulses than OPAL-RT under the same set of simulation parameters for higher signal bandwidth.

4

Integrated Hybrid Configuration

In this chapter, the background theory of Superimposed impulse voltages is presented in detail. The conventional test setup for composite HV testing is described, and a suitable impulse generator for the integrated hybrid configuration is designed. The requirements for the coupling circuit are discussed in detail. The chapter also presents two possible hybrid configurations along with their offline simulation results.

4.1. Superimposed Impulse Voltages

As the name suggests, Superimposed impulse voltages can be understood as the instantaneous addition of two waveforms at a given point. These types of voltages can be generated using a composite test setup, meaning it requires two separate voltage sources which apply voltage together at the same terminal of the test object, therefore it demands special requirements for connecting the measuring system and the two voltage sources [31]. A relevant circuit that couples the two circuits and suitable measuring equipment capable of measuring superimposed voltages are needed, this is because the voltage from one source tends to interfere and affect the other source as the connection terminals are the same. Since, in the majority of the cases today the superimposed tests are of growing importance as they are used to emulate the condition of a lightning/switching impulse transient superimposed on a power frequency sinusoidal wave, the analysis and the implementation of the superimposed circuit in this thesis is carried out for superimposition of Power frequency wave and lightning impulse.

For instance, IEC 60230 can be taken to understand the conventional superimposed wave generation circuit. The standard provides two possibilities for the test setup to obtain superimposed waveforms [32]. These possibilities are depicted in the figure 4.1. According to [33] there are two ways of measuring the superimposed voltage: 1) Measure the voltage separately at individual voltage sources and then add them up to get the superimposed voltage or 2) Measure the total superimposed voltage across the test object. However, since there is a significant value of the voltage drop on the blocking and coupling elements the results of measurements from the first method are slightly inaccurate. In the case of DC superimposed impulse testing, a Blocking resistor is provided on the DC side to protect the DC source from getting dam-

aged due to the impulse voltage. Moreover, this blocking resistor must also be of significantly high value to prevent the impulse to flow through the DC source instead of the front and tail resistors. Similarly, a blocking resistor is connected on the ac side during AC superimposed impulse testing to protect the HV AC source from the high-frequency impulse (In some cases, a low pass RC filter is kept on the ac side to attenuate the impulse signal). In order to couple the impulse generator to the test circuit, spark gaps or Coupling capacitors are used [31]. Spark gaps provide connection to the test object only when the impulse is triggered, else it provides complete isolation. Whereas a coupling capacitor is permanently connected to the test object. In the case of DC superimposed impulse testing, the coupling capacitor provides infinite resistance (open circuit condition) to the DC side, thereby completely isolating the impulse generator from the DC source. During AC superimposed impulse testing, The coupling capacitor provides a huge impedance to the AC side and helps to protect the impulse generator from the HV AC source.

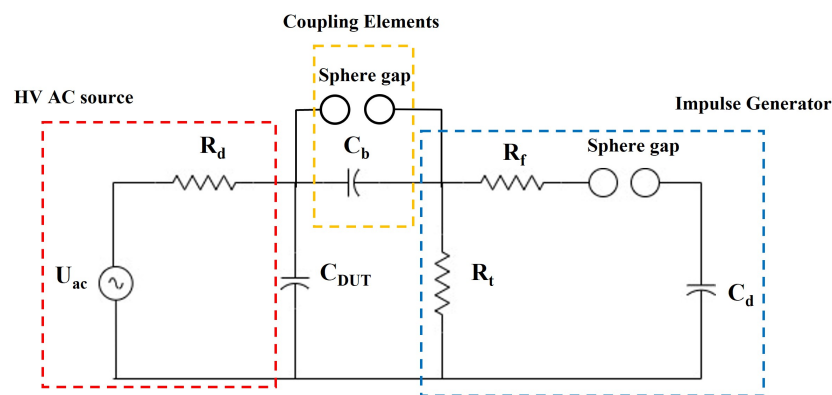


Figure 4.1: Conventional Superimposed impulse test circuit

Spark gaps or blocking condensers can be used to protect Impulse generators, however, there are some challenges that stem out as a result of using spark gaps over blocking condensers. Spark gaps lead to heavy distortions of the standardized waveforms, meaning using the spark gaps could greatly affect the wavefront, tail, or both wave-shape. It has been proven that Helmholtz decomposition can be used to determine the behavior of the protective element. When a blocking capacitor is used, the output voltage obtained at the terminal of the DUT is the summation of the impulse voltage and DC/AC voltage, however, when spark gaps are used the voltage measurement across the DUT is the value of the Impulse voltage [34]. Furthermore, when using spark gaps care has to be taken to maintain a minimum dU_{sg}/dt (where U_{sg} is the voltage across the spark gap) to ensure that the gap doesn't extinguish, however, this is very difficult to achieve during switching impulses[31]. Therefore, it can be suggested that the blocking condenser is a slightly better blocking component as compared to the spark gaps, despite the fact that the latter is less complicated and easy to implement.

4.2. MMC Based Integrated Hybrid configuration

As stated in Chapter 1, complex test setups comprising two or more sources are needed to generate complex wave shapes such as the superimposed lightning impulse wave for testing

HV components. Therefore, there is a need for a single HV testing source that can generate complex wave shapes. The MMC itself has capabilities to generate Arbitrary shapes ranging from low frequency to High-frequency signals for HV testing, which is demonstrated in [1]. However, the MMC itself cannot generate superimposed impulse wave shapes, as there are two major challenges associated with impulse generation. First, as the MMC for HV arbitrary wave generation will be made of valves, comprising several Semiconductor device switches connected in series, controlling the jitter in the string of these switches is difficult. Second, since the load in HV testing is a capacitive load and the testing demands a high dV/dt stress, the switches in the MMC need to be able to withstand high values of peak pulsed currents. Therefore, an integrated hybrid solution of an impulse generator and an MMC is needed to be able to generate superimposed impulse waveforms. This thesis demonstrates the feasibility of such a configuration.

Figure 4.2 below illustrates a possible hybrid configuration, it is derived from the conventional test circuit depicted in the previous section. The circuit highlighted in Purple corresponds to the waves shaping network consisting of the consisting of R_f and R_h . The region highlighted in yellow represents the source of the MMC in the form of a split capacitor. This split capacitor is rated for half of the DC link Voltage. The green highlighted part refers to the coupling element used to couple the impulse circuit with the MMC leg. Learning from the challenges mentioned in the previous section about spark gaps, a blocking condenser was used as the coupling element to protect the impulse side circuit from the nominal AC stresses. C_{load} refers to the capacitive HV DUT. The impulse wave circuitry is triggered by the sphere gap provided.

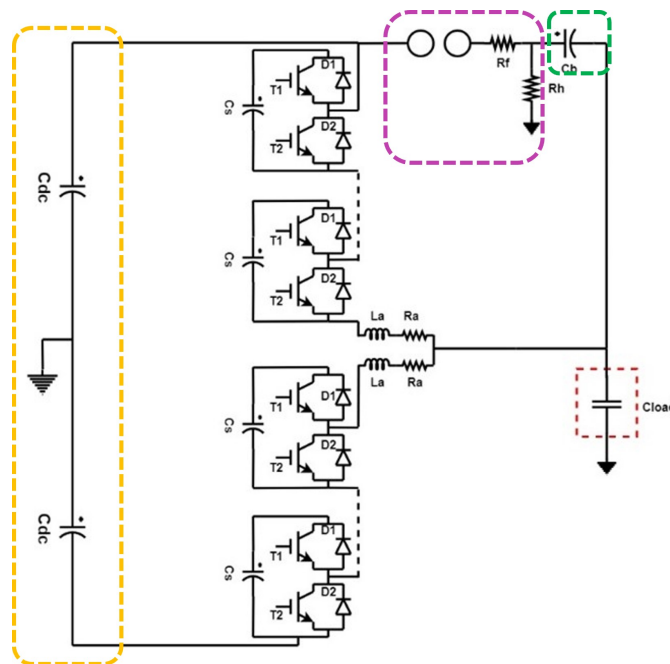


Figure 4.2: Integrated Hybrid Configuration 1

4.2.1. Working of the Hybrid Configuration

The working principle of the circuit illustrated is such that, under normal operating conditions when the impulse voltage is not being applied, the output voltage across the test object is a Power frequency signal. However, when the sphere gap is triggered, the Upper DC source capacitor C_{dc} acts as a discharge capacitor of the impulse generator, and the charge is transferred through the sphere gap and the waveshaping network to the test object. (Note: During the high-frequency impulse the blocking condenser serves as a short circuit) An impulse waveform is obtained superimposed on the power frequency waveform. The characteristic of the impulse wave shape can be varied by adjusting the front and the tail resistors. The exact phase at which the superposition of the two waves occurs can be controlled by firing the sphere gap at the desired point in time.

4.2.2. Simulation of the Hybrid Configuration

The hybrid configuration model with four SMs in each arm was developed and simulated in MATLAB. The MMC leg parameters mentioned in table 3.4 were used for simulation. Typically, the value of the DC source capacitance could either be in the range of a few hundreds of nanofarads or a few hundreds of microfarads. Therefore, two cases were simulated to analyze the effect of the value of the DC source Capacitance. The value of the blocking condenser was set to $1 \mu\text{F}$. A considerably large value of C_b was selected because the larger the value of the blocking capacitor lesser is the impedance it provides during the high-frequency impulse. Moreover, the blocking capacitor is connected in series to the test object during the discharge in the impulse generator path, therefore the two elements constitute a capacitive voltage divider and the value of the blocking condenser should be significantly high as compared to the load in order to maintain high efficiency of the generator circuit [31]. A suitable wave shaping network for the impulse generator was designed to produce the desired wave shape.

Design of Impulse generator

The impulse side in the hybrid configuration corresponds to a single stage of the Marx generator, a single stage impulse generator shown in figure 4.3[35] was used as reference to determine the values of R_f and R_h .

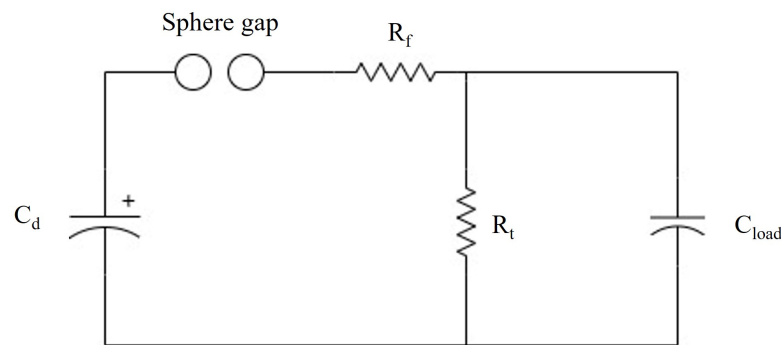


Figure 4.3: Single stage impulse generator

If V_0 is the voltage to which the impulse discharge capacitor is charged then after applying

Laplace transform to the circuit above we get the following voltage across the test object:

$$V_{Load}(s) = \frac{V_0}{s} \frac{Z_2}{Z_1 + Z_2} \quad (4.1)$$

$$Z_1 = \frac{1}{C_d s} + R_f \quad (4.2)$$

$$Z_2 = \frac{\frac{R_h}{C_{load} s}}{R_h + \frac{1}{C_{load} s}} \quad (4.3)$$

By substituting the value of Z_1 and Z_2 in equation 4.1 to get :

$$V_{Load}(s) = \frac{V_0}{m} \frac{1}{s^2 + ps + q} \quad (4.4)$$

where

$$p = \left(\frac{1}{R_f C_d} + \frac{1}{R_f C_{Load}} + \frac{1}{R_d C_{load}} \right) \quad (4.5)$$

$$q = \frac{1}{R_f R_h C_d C_{load}} \quad (4.6)$$

$$m = R_f C_{load} \quad (4.7)$$

$$V_{Load}(s) = \frac{V_0}{R_f C_{load}} \frac{1}{s^2 + s \left(\frac{1}{R_f C_d} + \frac{1}{R_f C_{Load}} \right) + \frac{1}{R_f R_h C_d C_{load}}} \quad (4.8)$$

Taking inverse Laplace transform of equation 4.8, we get the voltage across the test object in the time domain as [34]:

$$V_{load}(t) = \frac{V_0}{k} \frac{1}{\alpha_2 - \alpha_1} [e^{-\alpha_1 t} - e^{-\alpha_2 t}] \quad (4.9)$$

where α_1 and α_2 are the roots of the equation $s^2 + ps + q$. Therefore $\alpha_1 + \alpha_2 = p$ and $\alpha_1 \times \alpha_2 = q$. By using equation 4.5 and 4.6 the values of R_f and R_h can be calculated.

$$R_f = \frac{1}{2C_d} \left[\left(\frac{1}{\alpha_1} + \frac{1}{\alpha_2} \right) - \sqrt{\left(\frac{1}{\alpha_1} + \frac{1}{\alpha_2} \right)^2 - \frac{4(C_d + C_{load})}{\alpha_1 \alpha_2 C_{load}}} \right] \quad (4.10)$$

$$R_h = \frac{1}{2(C_d + C_{load})} \left[\left(\frac{1}{\alpha_1} + \frac{1}{\alpha_2} \right) + \sqrt{\left(\frac{1}{\alpha_1} + \frac{1}{\alpha_2} \right)^2 - \frac{4(C_d + C_{load})}{\alpha_1 \alpha_2 C_{load}}} \right] \quad (4.11)$$

Two cases were simulated for the hybrid configuration. For each case the value of R_f and R_h was calculated using the equations 4.10 and 4.11. Based on the table 4.1, α_1 and α_2 were calculated such that the output impulse wave has a rise time of $1.2 \mu s$ and a tail time of $50 \mu s$. The calculation of these Resistances was carried out through a MATLAB program, which is mentioned in the appendix. Initially, The simulation was performed for a DC link voltage of 300 V. For simplicity, during the simulation the sphere gap was replaced by a power electronics Switch.

$T_1/T_2 (\mu s)$	$1/\alpha_1 (\mu s)$	$1/\alpha_2 (\mu s)$
1.2/5	3.48	0.80
1.2/50	68.2	0.405
1.2/200	284	0.381
250/2500	2877	104

Table 4.1: α_1 and α_2 for standard impulse wave shape [34]

Case I

Figure 4.4 illustrates the schematic of the simulated circuit. Since the load to the converter was fixed to 100 nF, In this case, the DC source capacitor was kept at 500 nF. Such a value was selected for the source capacitor in-order to be able to design suitable values of R_f and R_h for the impulse generator. Therefore, during the calculation of R_f and R_h the value of C_{load} was considered as the series combination of the blocking capacitor and the DUT. Hence, using these values and equations 4.10 and 4.11, R_f and R_h were calculated as 5.45Ω and 111.48Ω respectively. Since the waveshaping network was designed for an impulse wave of $1.2/50 \mu s$, the IGBT switch was configured to have an ON time of $100 \mu s$. (This was done to ensure that the complete impulse wave was produced after the trigger)

Figure 4.5 represents the MATLAB simulation results of the hybrid configuration. In the figure 4.5 it can be seen that when the IGBT switch was not turned ON, the sinusoidal voltage across the test object was much lower than the reference voltage. This was because the voltage across the DC source capacitor (shown in yellow) had a peak-to-peak ripple of roughly 140 V. This can be accounted to the fact that a less stiff capacitor in the range of a few hundreds of nanofarads was used. Since the voltage ripple was too huge, the DC source in the form of a split capacitor was not able to generate the required ac output voltage. At a time instant of 0.055 s (at the peak of the ac output) the IGBT switch was turned on and an impulse wave was superimposed at the peak of the AC output. At the instant when the impulse was applied the DC source capacitor was discharged nearly to 0 V, however after the impulse wave died out the voltage did not restore to the nominal AC voltage. As a result, the ac voltage after the impulse trigger was offset in voltage.

Case II

In order to solve the problem of the large Capacitor voltage ripple, the value of the DC source capacitor for this case was set to $220 \mu F$. Since the load of the converter is 100 nF. The difference between the load and the discharge capacitor is of the order of 1000. Therefore the

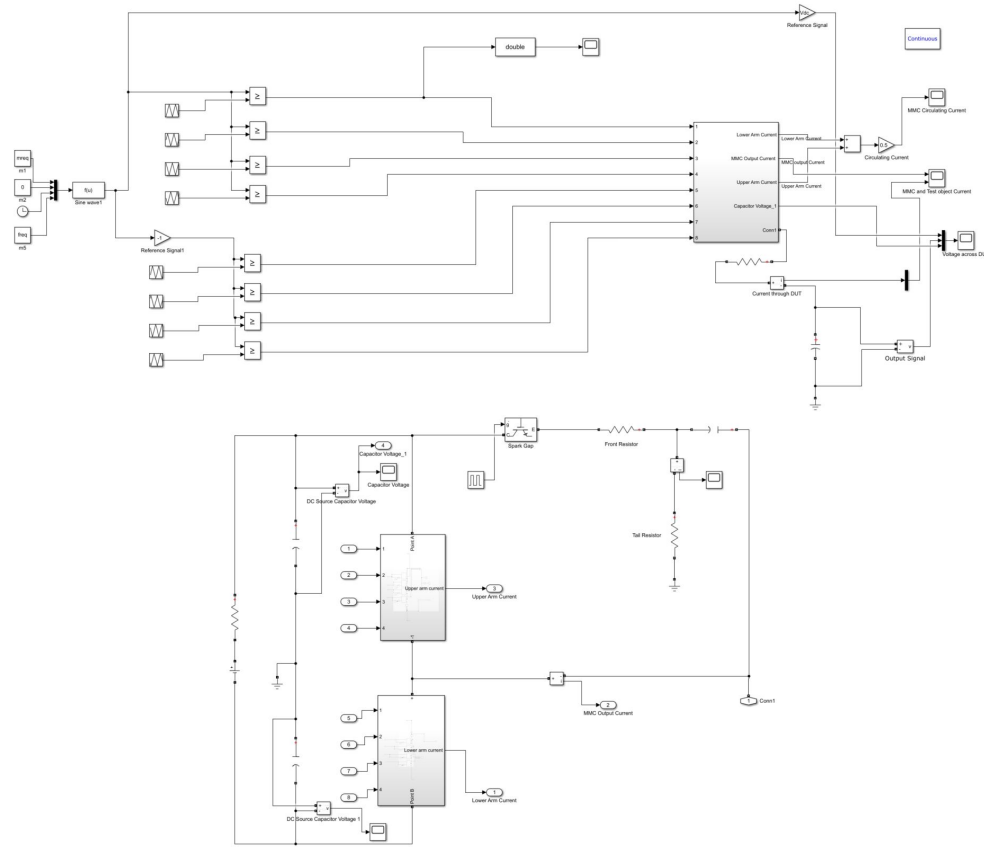


Figure 4.4: Simulated circuit diagram for Configuration 1

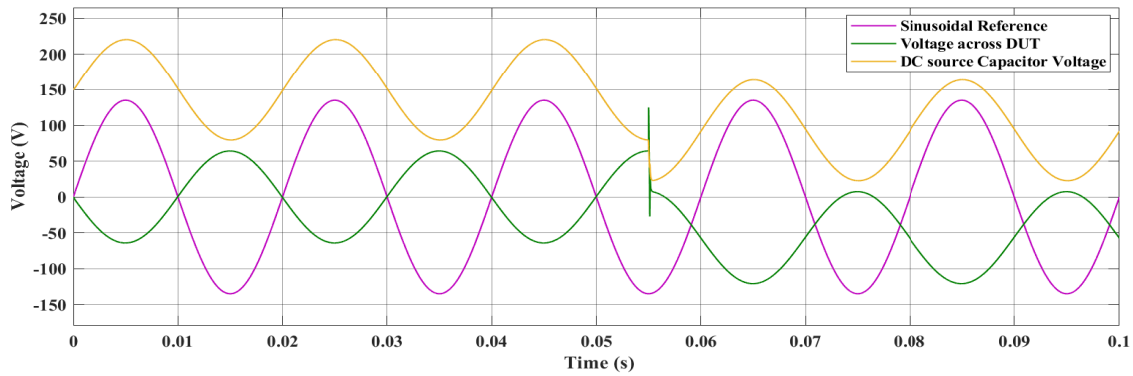


Figure 4.5: Simulation results of Hybrid Configuration 1

efficiency of such an impulse generator would be extremely poor, which is depicted through the efficiency curve of a single-stage impulse generator circuit shown in figure 4.6. In the figure, C_2 represents the cumulative load capacitance and C_1 corresponds to the total equivalent source capacitance. Consequently, based on design equations 4.10 and 4.11 the values of R_f and R_h came out as complex values, which is practically impossible.

As a result, in order to be able to keep the DC source capacitance value high and at the same

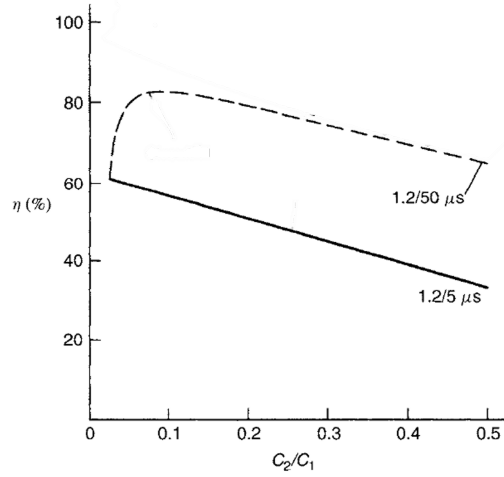


Figure 4.6: Efficiency curve of the Impulse generator [35]

time realize practical values for R_f and R_h the Hybrid configuration needs to be slightly modified. This can be achieved in two ways, either with increasing load by connecting an additional capacitor in parallel to the test object, or by decreasing the effective capacitance on the source side. The former method has a problem that, when an additional capacitor is connected in parallel to the DUT, under normal conditions when the impulse is not applied the overall load seen by the MMC is very large which would lead to a large capacitor ripple and a huge circulating current in the MMC leg. Therefore the latter method is investigated in the next section by reducing the effective capacitance on the source side.

Modified Hybrid Configuration

Figure 4.7 corresponds to the schematic of the modified Hybrid converter. Here an additional small capacitor (Highlighted in red) in the range of a few hundreds of nanofarads is connected in series to the DC source capacitor so that the effective source capacitance during the impulse wave is in the range of nanofarads. The modified schematic showed in 4.7 was simulated with the value of C_s equal to 500 nF. During the impulse discharge the newly added capacitor is in series with the DC source capacitance, therefore for calculation of R_f and R_h , C_d is taken as the series combination of C_{dc} and C_s . Using the equations 4.10 and 4.11 the values of R_f and R_h were calculated as 5.42 Ω and 111.71 Ω respectively. The simulation results depicting the sinusoidal reference, Output voltage, and the DC source capacitor voltage are shown below in figure 4.8.

From the simulation results, it can be seen that the DC capacitor voltage ripple was negligible and therefore the voltage across the DUT was not compromised and was identical to the sinusoidal reference. The impulse trigger was applied at a time instant of 0.035 s (at the peak of the ac voltage), and after the impulse died out the ac waveform was restored. This is because now the MMC circulating current and capacitor voltage ripple was very small, during the impulse discharge the drop in capacitor voltage is negligible and consequently there is no offset.

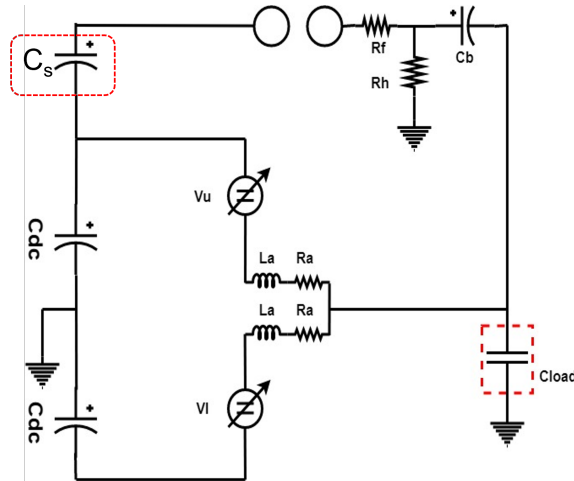


Figure 4.7: Schematic diagram of the modified hybrid configuration

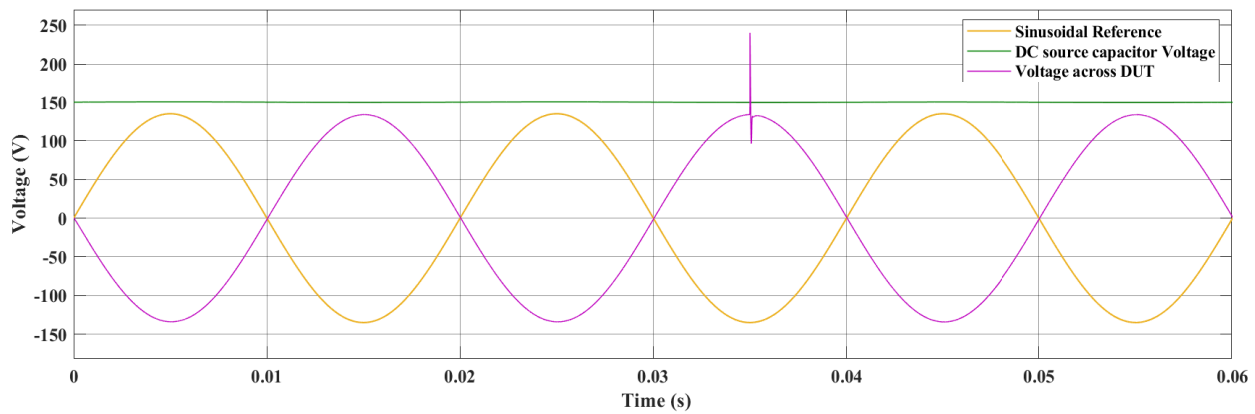


Figure 4.8: Simulation result of the modified hybrid configuration

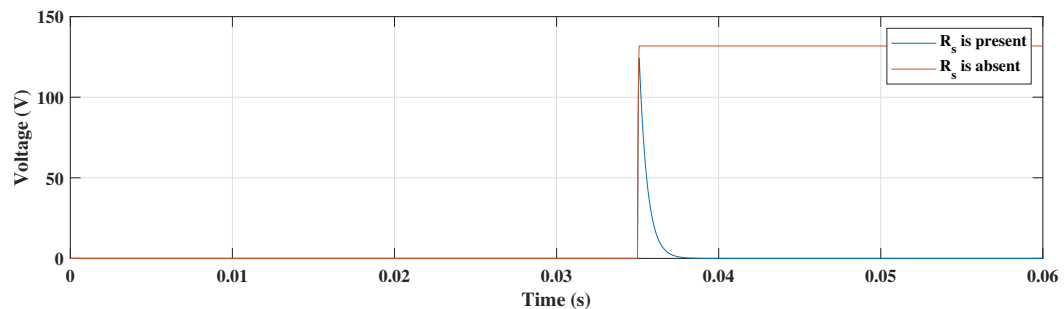
Effect of the coupling element

As previously stated that the value of the coupling condenser was set to $1 \mu\text{F}$ for analysis, however, the effect for different values is investigated in this section. The modified hybrid configuration was simulated for a range of values for C_b , and the peak values of the AC output and Superimposed Impulse waveform were recorded and are presented in table 4.2 below. It can be observed that as the value of C_b increases the value of the AC peak decreases. This can be accounted to the fact that when the impulse is not triggered the series combination of R_h and C_b is in parallel with the DUT which reduces the current flowing through the DUT. Moreover as C_b increases, the superimposed impulse peak, and impulse voltage value increase, this is due to the fact that larger values of C_b provide a lesser impedance to the high-frequency impulse. Since a DC link voltage of 300 V and a modulation index of 0.9 was chosen for simulation, the peak value of the AC reference was 135 V. Therefore from the results in the table, it can be concluded that a blocking capacitor of $1 \mu\text{F}$ is an ideal compromise between the AC peak and superimposed impulse.

Blocking Capacitor (C_b)	AC peak (V)	Superimposed peak (V)	Impulse Voltage (V)
300 nF	135.2	240.1	88.9
400 nF	135.1	229.5	94.4
500 nF	135	232.9	97.9
900 nF	134.7	239.4	104.7
1 μ F	134.5	240.1	105.6
2 μ F	133.4	242.8	109.4
5 μ F	129.6	237.8	108.2

Table 4.2: Effect of coupling capacitance

During the simulation, it was observed that after applying the impulse discharge, the additional capacitor C_s remained charged with nearly half of the DC link voltage. Consequently, it is not possible to generate multiple impulses in a given power frequency cycle. Meaning, this limits the circuit to supply back-to-back superimposed impulses. To solve this problem, the Capacitor C_s needs to be discharged before the application of the next impulse. Therefore, a resistor was connected in parallel with the capacitor C_s to discharge it after the impulse died out. Ideally, the value of the resistor should be as small as possible to permit the quick discharge, however, keeping a small value of the resistor can affect the impulse shape and magnitude. As a result, a resistor (R_s) of 1 k Ω was used to limit the current and minimize its effect on wave output. The voltage across the Capacitor is shown before and after inserting a resistor in figure 4.9.

Figure 4.9: Voltage across additional capacitor (C_s)

In a typical Impulse generator when the impulse discharge is triggered, a large pulsed current is drawn through the source to generate the impulse wave across the test object. Extending the same principle to the MMC-based HV test source, when the sphere gap gets triggered, a pulsed current flows through the hybrid circuit. This is of important concern as it can damage the components of the MMC leg (particularly the Power electronics Switches and SM capacitances). The voltage and current stresses on the MMC leg and Sphere gap are shown in figure 4.10. During the simulation, it was observed that the majority of this pulsed current flows through the sphere gap (Modelled as an IGBT switch), and a small fraction of this pulse flows through the MMC leg itself. Consequently, even after the impulse discharge, the voltage across individual SM capacitors changes negligibly. Inside the MMC leg, however, the maximum of this

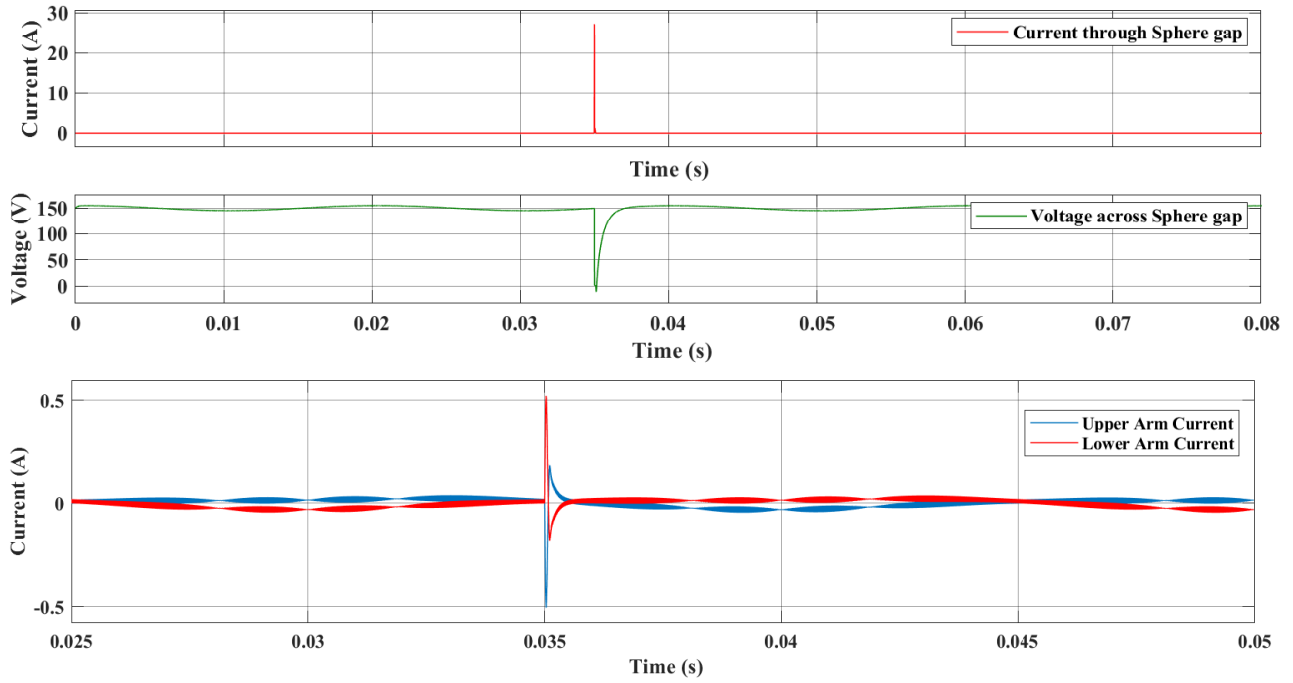


Figure 4.10: Current and Voltage stress on sphere gap and MMC leg

stress during the impulse is seen by the arm reactor and resistor. This is illustrated in figure 4.11. Therefore, the arm resistor and inductor must be designed to withstand the peak value of impulse voltage.

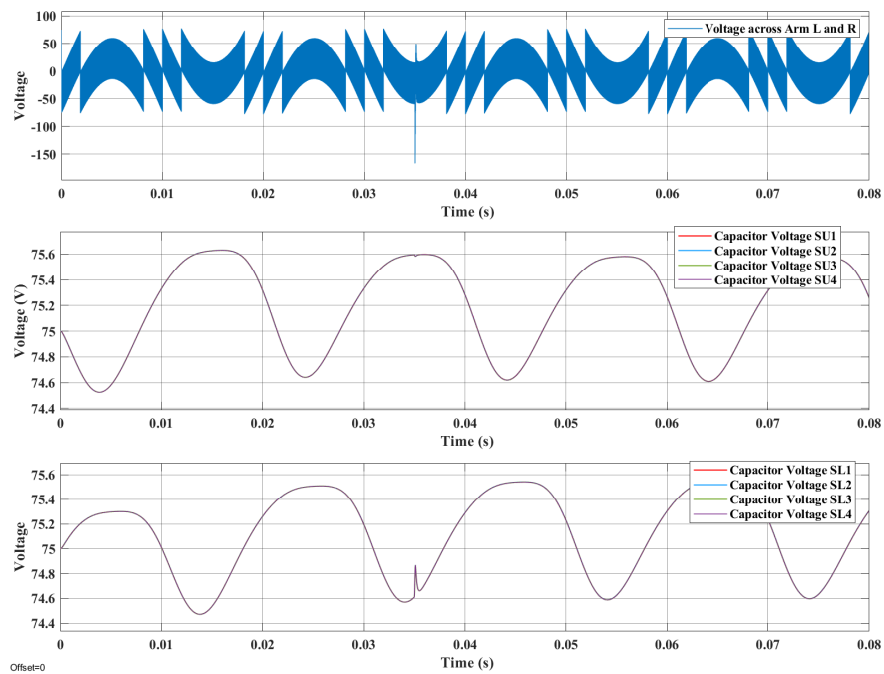


Figure 4.11: Voltage across Capacitance of SM and Arm reactor and Resistor

4.3. Generation of Negative impulses

The IEC standards for lightning/ stitching impulses and superimposed impulses both constitute testing conditions for either polarity (i.e negative and positive). As a result, the MMC-based HV test source should be capable of generating superimposed negative impulses. In conventional impulse generators, the direction of the diode is changed to charge the impulse discharge capacitor with opposite polarity to generate negative impulses. For the MMC-based generator, this can be achieved by using the bottom split capacitor as the discharge capacitor. The schematic in figure 4.12 depicts the use of the bottom half of the DC link as the source.

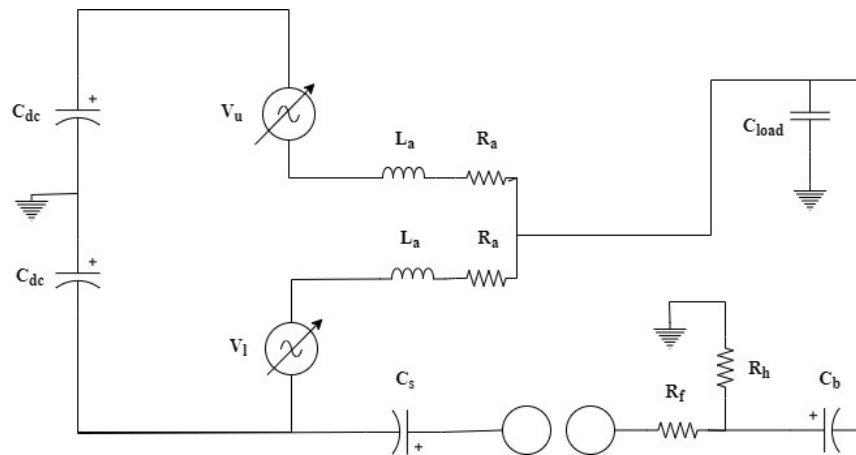


Figure 4.12: Hybrid configuration for negative impulses

The schematic was simulated in MATLAB with similar conditions as for the previous configuration. However, the impulse trigger was applied at a time instant of 0.025s (at the negative peak of the Power frequency wave). The simulation results depicting the output voltage, reference signal, and the voltage across the DC source capacitance are presented in figure 4.13.

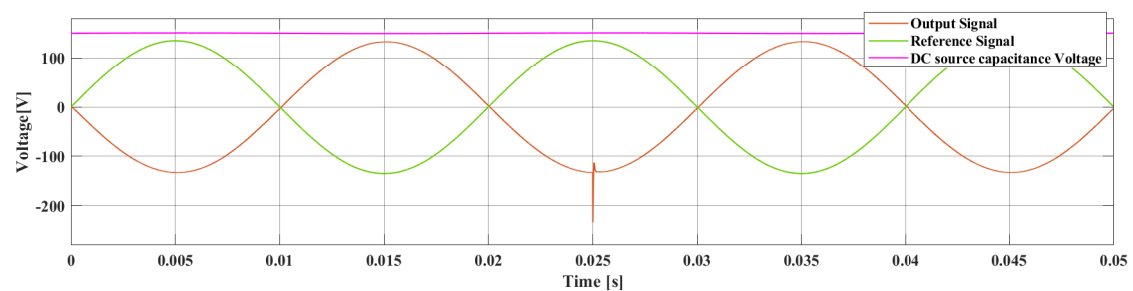


Figure 4.13: Simulation results for the generation of negative impulses

4.4. High Voltage MMC Simulation

As mentioned in chapter 1, it is intended to build an MMC-based HV test source capable of generating arbitrary signals with significantly high bandwidth. As a part of it, this thesis intends to validate the design of this MMC-based test source to produce Superimposed waveforms. The approach adopted in this thesis is to first test the design for Low Voltage up to 300 V and then extend it to High Voltage. So far in the previous sections, the MMC-based test source model was developed and simulated for Low voltage in MATLAB for 4 SMs in each arm. In this section, however, the model for HV is simulated and analyzed. A 20 SM (in each arm) based MMC hybrid with $2N+1$ level PSC control was developed using MATLAB. During the low voltage simulation, the capacitive load was set to 100 nF to emulate the high voltage testing conditions (As capacitance draws more current at higher voltage). Consequently, for HV simulation, the load was reduced to 10 nF. The additional capacitor was changed to 100 nF so that the R_f and R_h could be designed to obtain the 1.2/50 μ s impulse wave. The blocking capacitor was set to 100 nF. A DC link voltage of 100 kV was used to simulate the model. Due to the increased number of components, the simulation time step was set to 10 μ s with a relative tolerance of 1 ms. Since, it was expected that in an offline simulation, merely increasing the voltage level would not change the simulation behavior or output drastically, The goal of this simulation was to investigate the values of the current and the voltage stresses on various components in order to design them for HV. Primarily the peak value of the pulsed current during the impulse discharge was analyzed. Figure 4.14 below shows the current through the Upper and lower arm of the MMC.

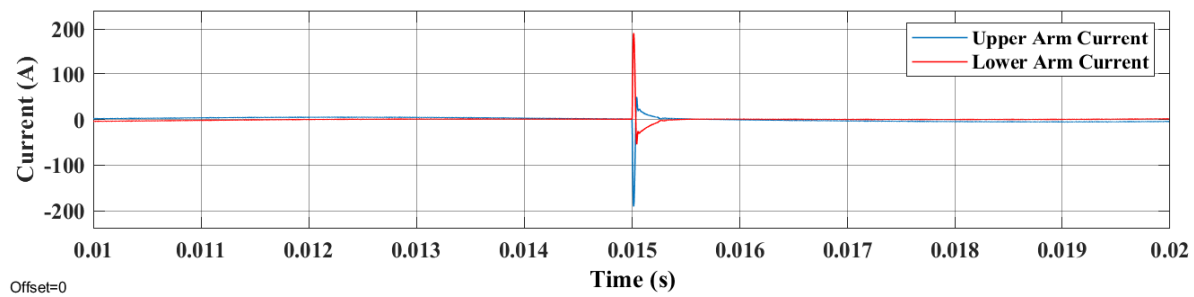


Figure 4.14: MMC upper and lower arm current (No additional resistance)

It was observed that during the impulse discharge the maximum current peak obtained was around 190 A. This is a concern as the Power Electronics switches used in the SMs would get damaged if they are subjected to such high currents frequently during testing. This current therefore needs to be limited to reduce the current stress in the Semiconductor devices and Voltage stress across the arm resistor and inductor without compromising the output voltage across the DUT. This can be solved by connecting an additional resistor in between the MMC leg and the Test object as shown in the schematic in figure 4.15.

Increasing values of resistance starting from 100 Ω were selected and simulated. It was observed that on increasing the value of resistance the current decreased, but beyond 1 k Ω , the output voltage deviated from the reference voltage. Therefore, 1 k Ω resistance was used as R_s , and the value of the peak current fell to roughly 35 A from 190 A. Figure 4.16 illustrates the

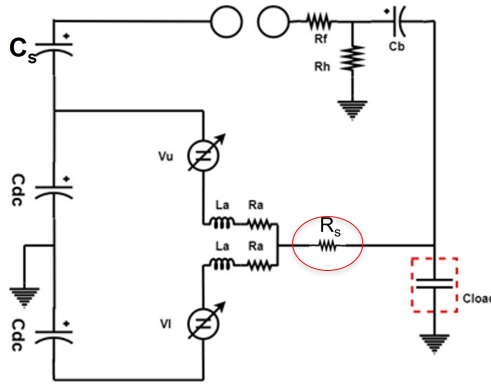


Figure 4.15: Hybrid circuit with an additional resistance

reduction of current stress. Figure 4.17 depicts the capacitor voltage of the first 6 sub-modules of the upper arm. It is found that the superimposed impulse has a very small impact on the capacitor voltage of the individual cell.

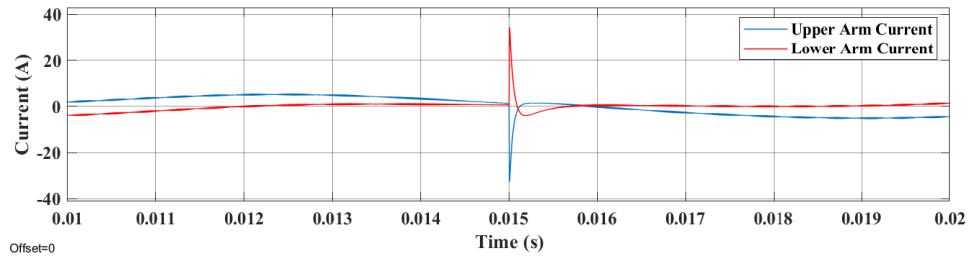


Figure 4.16: Current in the upper and lower arm after inserting the resistor

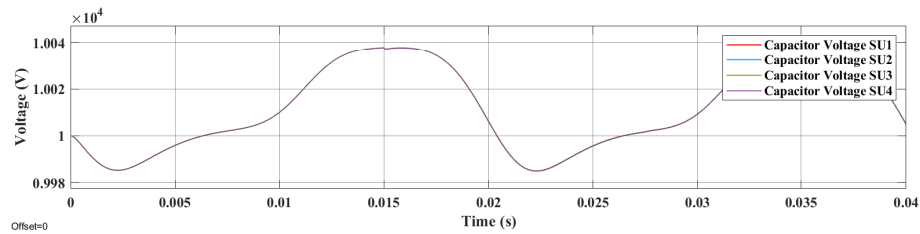


Figure 4.17: Upper arm capacitor voltages

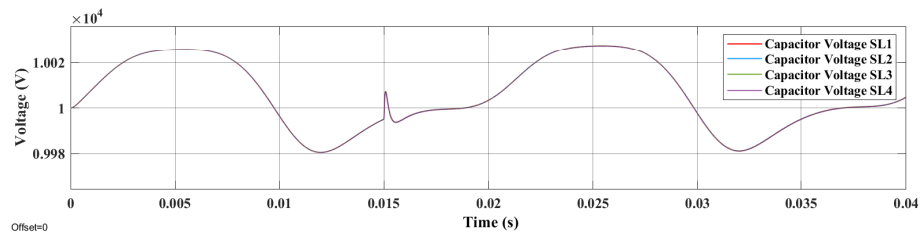


Figure 4.18: Lower arm capacitor voltages

4.5. Summary

This chapter summarises the design and simulation of the integrated hybrid configuration. The conventional circuit for composite testing was studied in detail. The requirements for designing the decoupling circuit were understood from the existing conventional superimposed test setup. Based on these requirements, the MMC-based integrated hybrid configuration was designed and simulated. The capacitive load was fixed to 100 nF. It was concluded that in order to minimize the DC source capacitor voltage ripple, a large value of DC link capacitance was needed. However, it was observed that when the source capacitance was too large the wave shaping network cannot be designed for smaller loads to get the desired impulse shape. Therefore, an additional small capacitor was connected in series with the source capacitor to reduce the overall source capacitance during impulse. The wave-shaping network of the impulse circuit was designed based on the single-stage impulse generator equivalent circuit. It was concluded that the MMC hybrid could also generate negative superimposed impulses if the low side source capacitor was used instead of the high side. The model developed for low voltage was extended further to increase the number of sub-modules to simulate the hybrid configuration at high voltage. It was observed that at HV, an additional resistor needs to be connected at the output of MMC to limit the individual arm currents to protect the Power electronic switches of the converter.

5

Hardware Implementation

With having performed the simulations for the MMC-based HV Test source in Chapters 3 and 4, the final task is to implement the hybrid configuration in hardware to verify the results with offline simulation. The subsequent sections in this chapter present the hardware requirements and setup developed to perform RCP and superimposed impulse tests.

5.1. Rapid Control Prototyping

As discussed in chapter 2, RCP involves the use of a controller in the form of an RT simulator to control a real (Physical) plant for testing. Although the MMC test source was intended to be developed and tested for HV, the testing was performed on a downscaled prototype with a reduced number of MMC cells with lower voltage up to 300 V. Typhoon HIL 404 installed with a fiber optic interface board was used to control the MMC cells with the FPGA based open loop control designed and developed in chapter 3.

5.1.1. MMC Sub-Module

For the RCP setup, the hardware of MMC was controlled by a real-time simulator. MMC sub-modules were connected in series to build the converter. Each sub-module board is comprised of the Power board and the gate driver board. Figure 5.1 depicts the power module of the MMC cell. The schematics of the connections to the power switches, sub-module capacitance, and the connections to the gate driver board are presented in figures 5.2a, 5.2b and 5.3 respectively. It can be seen from the figure 5.2a, that each sub-module represents the full bridge converter topology with 4 switches named Q1, Q2, Q3, and Q4. Since the control scheme developed in chapter 3 was for half bridge topology-based sub-modules, each MMC cell was configured to be used as a half-bridge. Switches Q1 and Q2 were used for the operation. The output of the sub-module was taken across the terminals, PhOutA and PDCn_IN. Diodes Dg1, Dg5, Dg3, and Dg7 were placed on the drain terminals of switches Q2 and Q1 respectively for over-voltage protection. Figure 5.2b illustrates the arrangement of the DC capacitors in series-parallel to constitute the sub-module capacitance. 12 DC electrolytic capacitors of each 100 μ F value were used to obtain an equivalent capacitance of 75 μ F. In order to ensure regular distribution of voltage across the capacitors, resistances were connected in parallel to the

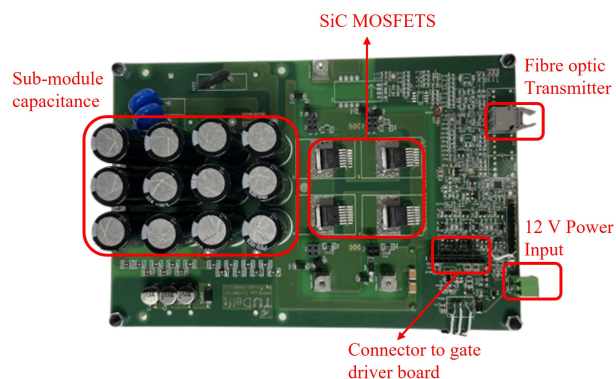


Figure 5.1: MMC power module

branch.

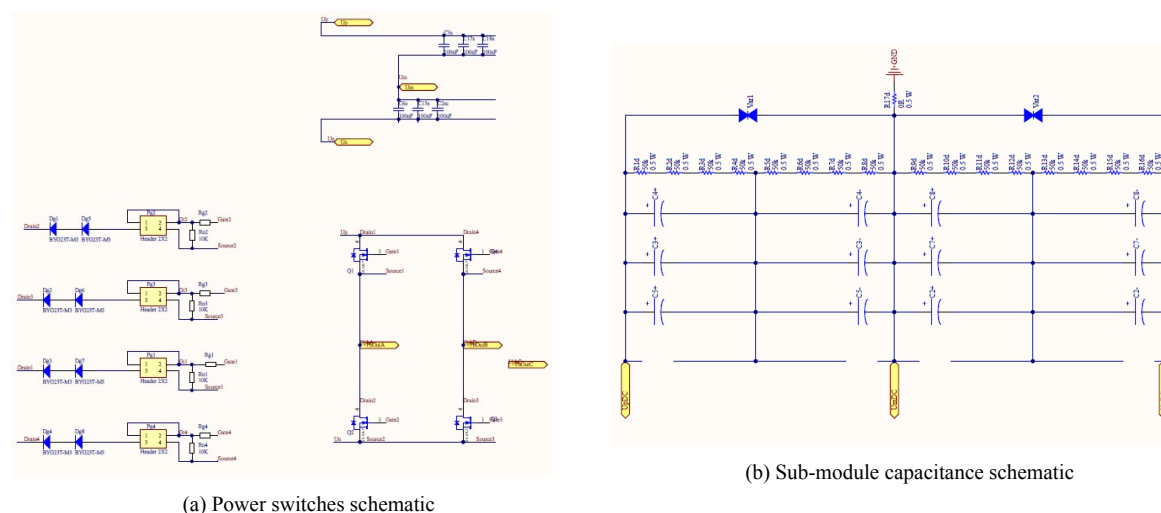


Figure 5.2: MMC power module schematics

Another important part of the MMC sub-module is the gate driver board. The schematic in the figure 5.3 illustrates the connection of the gate driver board with the Power board. The board has 4 Fibre optic receivers mounted to receive gate pulses from a controller. Alternatively, the gate pulses can also be provided through the 8th and 9th pin of the 9 pin Input at the bottom of the power board. These pulses are transferred to the gate of the respective switches only when the board is enabled, this is done by shorting the First pin of the 9-pin input with the 7th pin (Clear pin). The MMC sub-module also has its own circuit installed on the power board to generate dead time between the switches of the leg. However, this was not used during the testing as the dead time was generated using Typhoon HIL. Figure 5.4 shows the front and back of the gate driver board of the MMC submodule. In this gate driver board, the ACPL-344JT IC gate driver was used. The IC has a peak output current of 2.4 A and a wide operating voltage range. Figure 5.5 depicts one of the stages of the gate driver. It can be seen that based on the requirement either of the two MOSFETs can be turned on to either supply VCC or VDD at the

gate terminal.

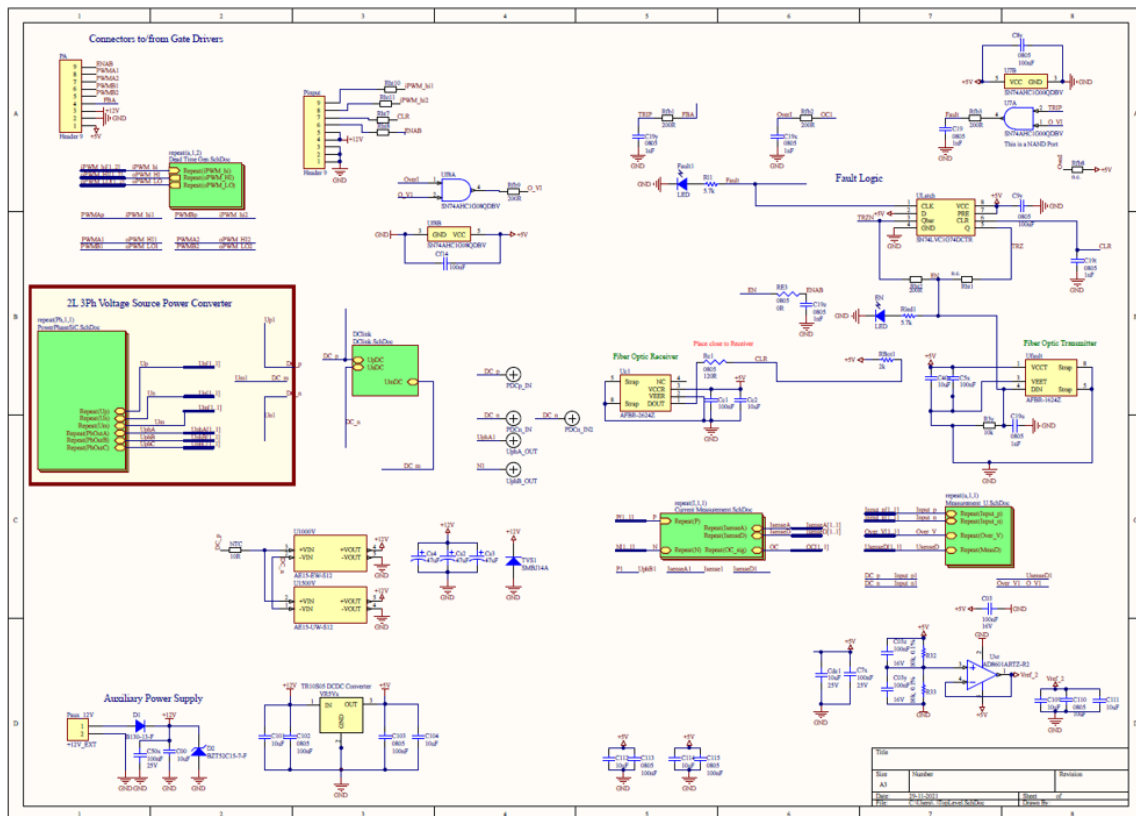


Figure 5.3: Schematic representing the connectors to gate driver

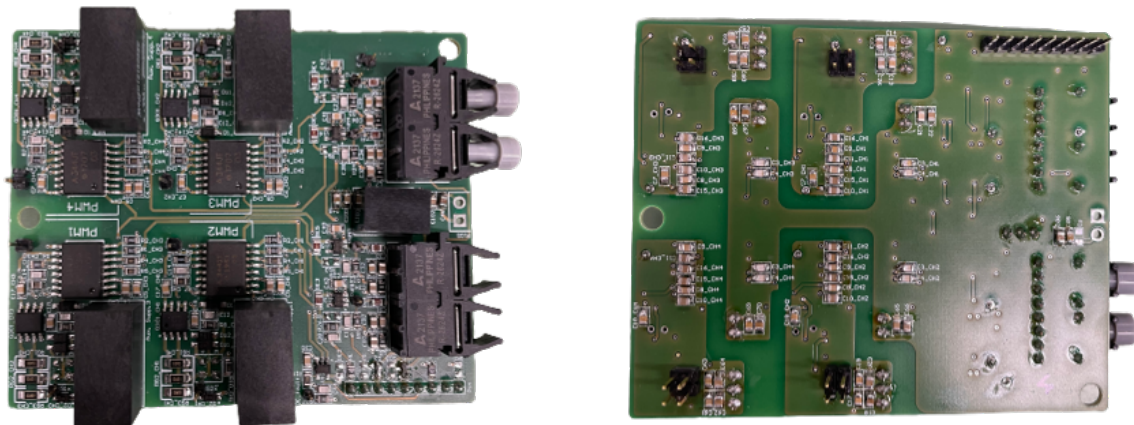


Figure 5.4: Front and back of a gate driver

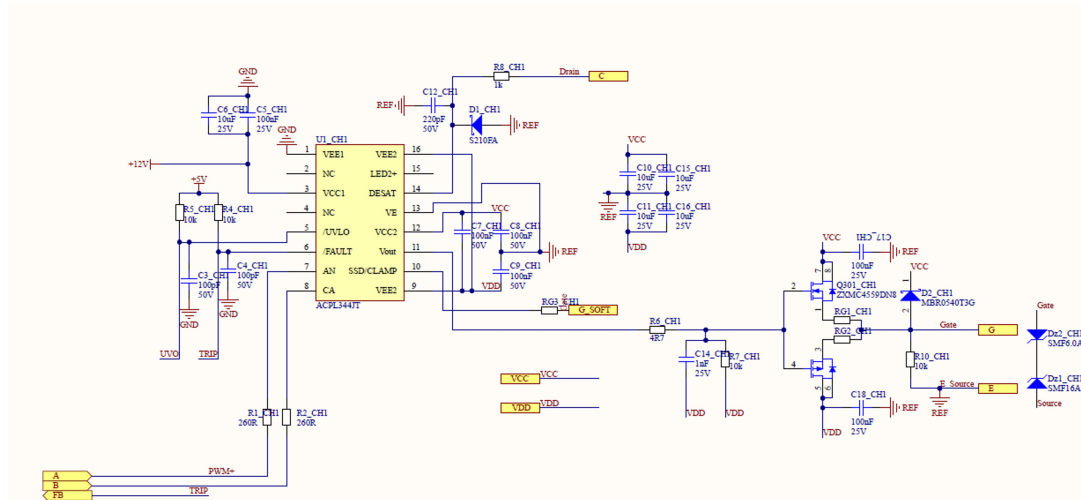


Figure 5.5: Gate driver schematic

5.1.2. Fiber optic Interface

One of the most important aspects of real-time testing is the communication between the hardware and the RT simulator. The communication usually involves either sending or receiving control signals or retrieving Voltage/Current measurement signals. Therefore an interface must be selected in such a way that it allows communication without any loss of data and at the same time be compatible with the hardware being used. Since the MMC sub-modules rely on communication through fiber optic cables, the Typhoon HIL Fiber optic interface was used. The fiber optic board has a standard DIN 41612 connector to connect to the HIL device. This board can also be connected in series with the HIL breakout board to gain easy access to the I/O. The Schematic diagram of the fiber optic interface is shown in figure 5.6.

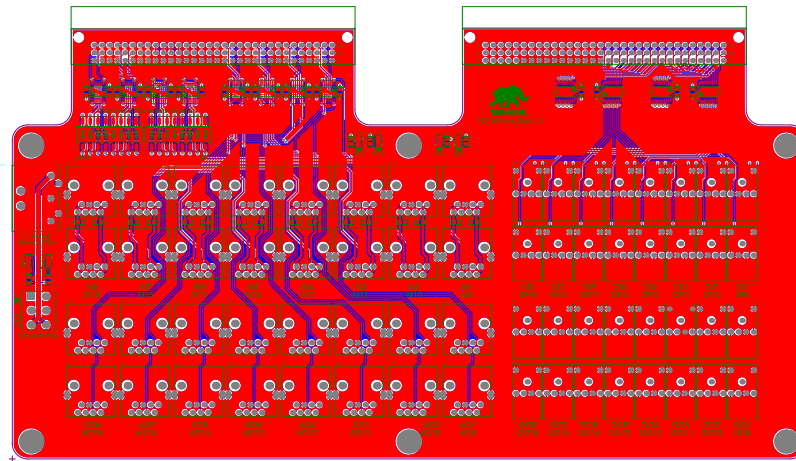


Figure 5.6: Fibre Optic Board interface Schematic [Designed by Typhoon HIL]

The fiber optic interface board can be powered either from the HIL device itself or externally through a DC power supply. The interface board provides 16 Fiber optic digital inputs/outputs and 16 Ethernet port analog input/outputs.

The RCP tests were carried out in a step-by-step manner, first, a single MMC sub-module was tested as a two-level converter followed by an MMC with one sub module in each arm, and finally an MMC with two sub-modules in each arm.

5.1.3. MMC cell as a two-level converter

Figure 5.7 shows the lab setup to test the single cell of MMC. Two DC power supplies were used; one of them was used to provide 12 V input to the MMC cell and the other was used as the main DC source to the two-level converter. The DC input to the converter was set to 100 V. Since the DC supply was direct across the DC terminals of the board, the sub-module capacitor was used as the DC link capacitor of the converter. Typhoon HIL was configured with FPGA control to generate PWM Digital signals for a single leg with a dead time of 250 ns.

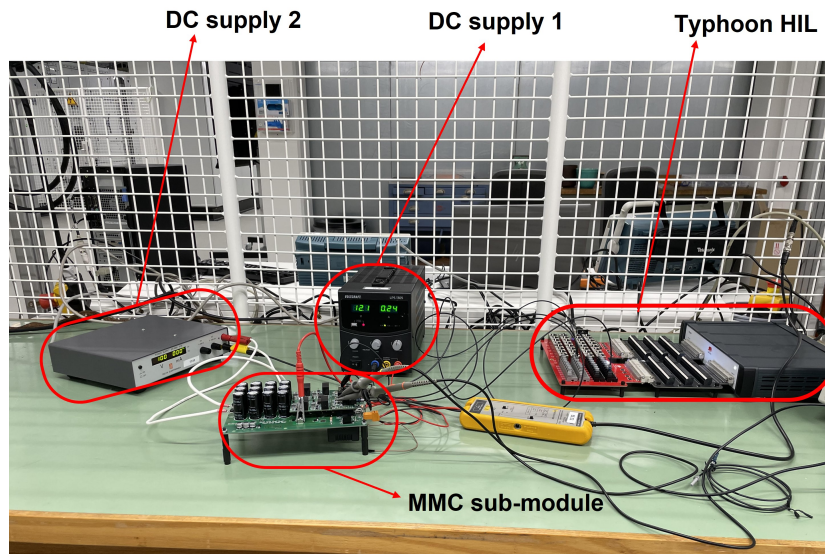


Figure 5.7: Lab setup for testing single Cell

A differential probe was used to measure the output voltage of the sub-module. The fiber optic transmitter on the MMC board was connected to the digital input of the Typhoon HIL. This was used to measure the Sub-module capacitor voltage. Figure 5.8 shows the output voltage of the two-level converter. Table 5.1 summarises the parameters used for the control of the sub-module. The output voltage obtained was nearly 90 V.

Parameter	Value
Modulation index	0.9
Reference frequency	50 Hz
Switching frequency	10 kHz
Dead Time	250 ns

Table 5.1: Parameters for control of Sub-module

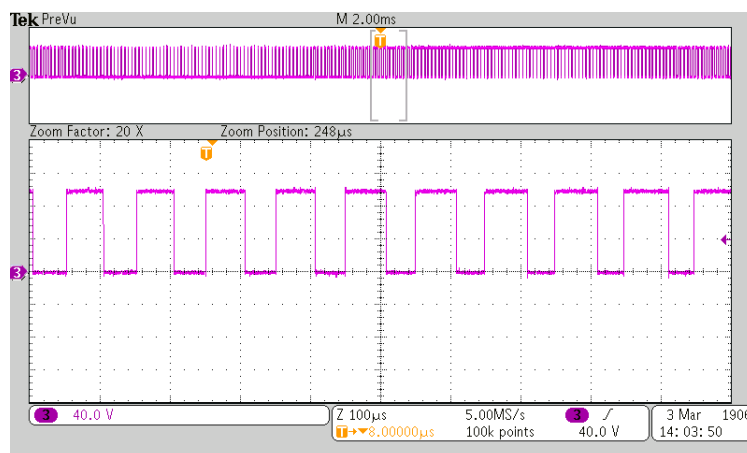
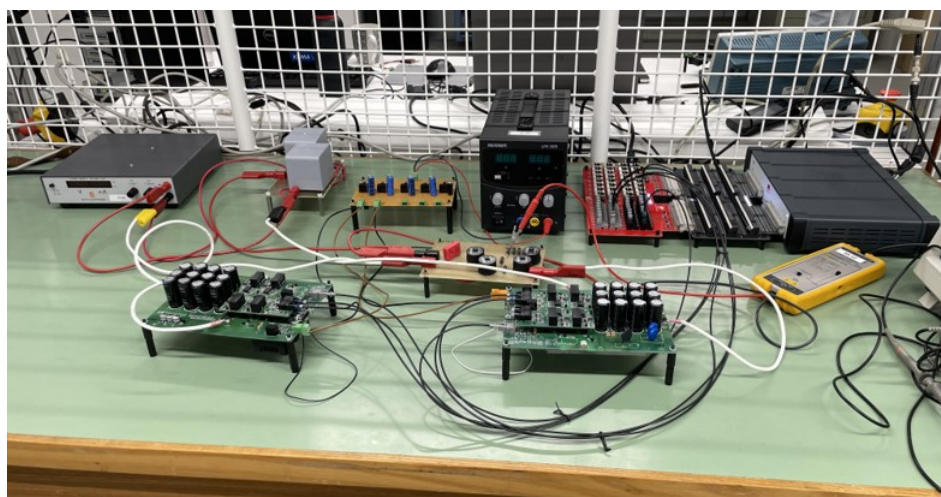
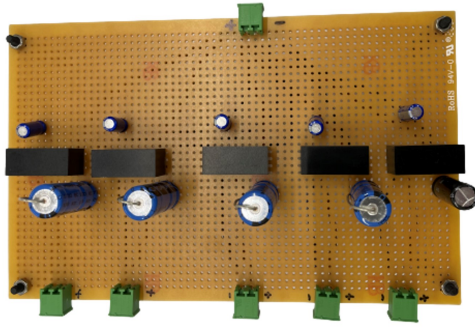


Figure 5.8: Output of single MMC sub-module

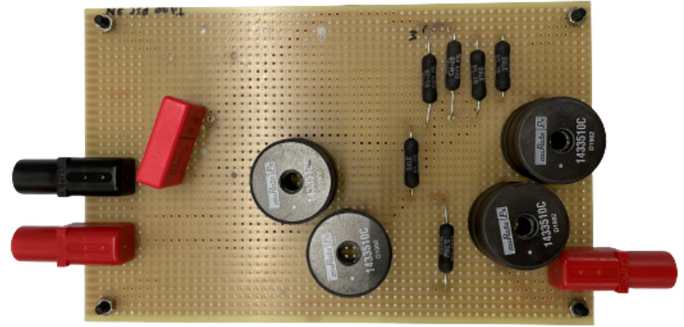
5.1.4. MMC with one sub-module in each arm

After testing a single sub-module as a two-level converter, the next step is to test the MMC converter with a single sub-module in each arm. Figure 5.9 illustrates the setup for testing. The setup consists of a DC source connected to a DC link comprising of a split capacitor configuration. Another DC source was used to supply an auxiliary power supply board (shown in figure 5.10a). The auxiliary power supply board consists of five 24 to 12 V converters connected in parallel. The output of this board is fed to the individual MMC sub-module. The arm inductor, arm resistor, and capacitive load are placed on a general purpose board shown in figure 5.10b. The value of the arm inductor and resistor used during MIL simulation in chapter 3, was slightly modified as the number of sub-modules during the hardware implementation was reduced. This was done primarily to meet the filtering requirements to achieve a sinusoidal output across the load. Typhoon HIL 404 was used to send gate pulses to the MMC cells and receive voltage signals from individual sub-modules.

Figure 5.9: RCP setup for MMC with $N = 1$



(a) Auxiliary Power Board



(b) Arm inductance, arm resistance, and load board

Figure 5.10: MMC power module schematics

Each MMC cell has an inbuilt analog voltage measurement circuit which continuously measures the voltage across the sub-module capacitor. The measured analog signals are converted into PWM digital pulses using a voltage circuit and these signals are sent to Typhoon HIL via fiber optic cables. Since the data of capacitor voltage is embedded in the form of frequency values of the PWM signals, each MMC sub-module needs to be calibrated to convert the frequency information into an exact voltage value. Therefore, in order to monitor the capacitor voltage continuously, the frequency of the PWM pulses sent to the RT simulator needs to be measured. Consequently, the PWM Analyser block from the Typhoon HIL library was used to measure the frequency in real-time. This block works on the same dedicated hardware as that of the PWM modulator on FPGA and operates at the device clock frequency (i.e 280 MHz for HIL 404). During the calibration process, DC voltage was applied across the terminals of sub-module capacitance and the frequency was noted. The voltage was applied in steps of 25 V up to 300 V. The data obtained was imported to MATLAB, and the polyfit function was used to get the relation between the DC Capacitor voltage and the frequency of input signals. (The MATLAB script illustrating the use of the Polyfit function can be found in the Appendix). After the calibration process, the Voltage was applied to the setup shown in figure 5.9. Table 5.2 below shows Real-time simulation parameters used.

Parameter	Value
Modulation index	0.9
Reference frequency	50 Hz
Switching frequency	50 kHz
Dead Time	250 ns
DC link voltage	300 V
Arm Inductance	6 mH
Arm resistance	90 Ω
Load Capacitance	100 nF

Table 5.2: Parameters for MMC control for N = 1

The RT simulation was performed with a simulation time step of 500 ns. The results obtained were compared with that of an offline simulation such as MATLAB. Figure 5.11 and 5.12 illustrate the comparison of the Output voltage and output current of the MMC setup. It was observed that the results from experiments were very close and almost identical to the expected results from offline simulation.

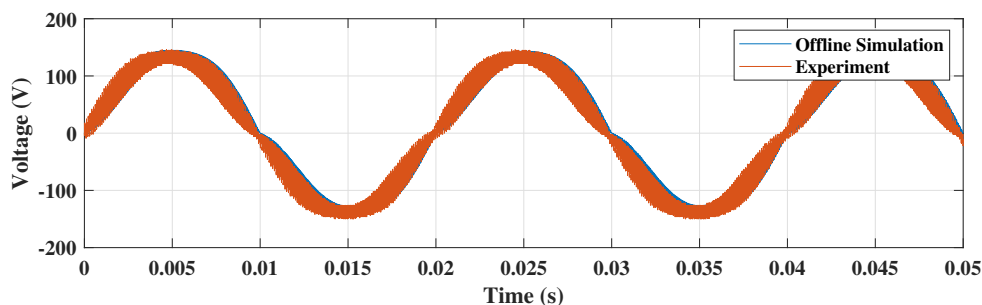


Figure 5.11: Output Voltage across Load for $N = 1$

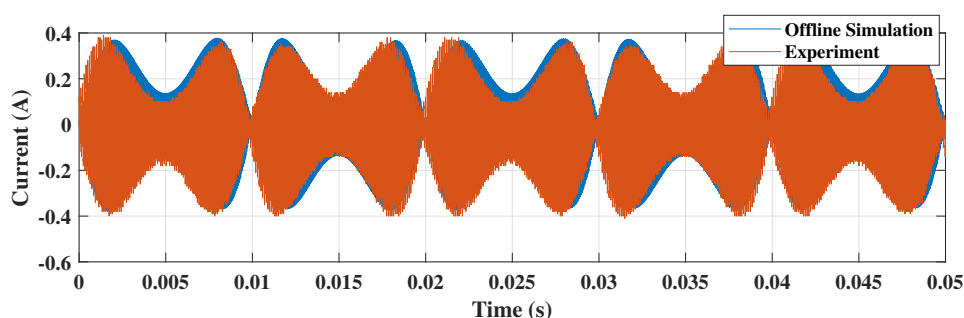
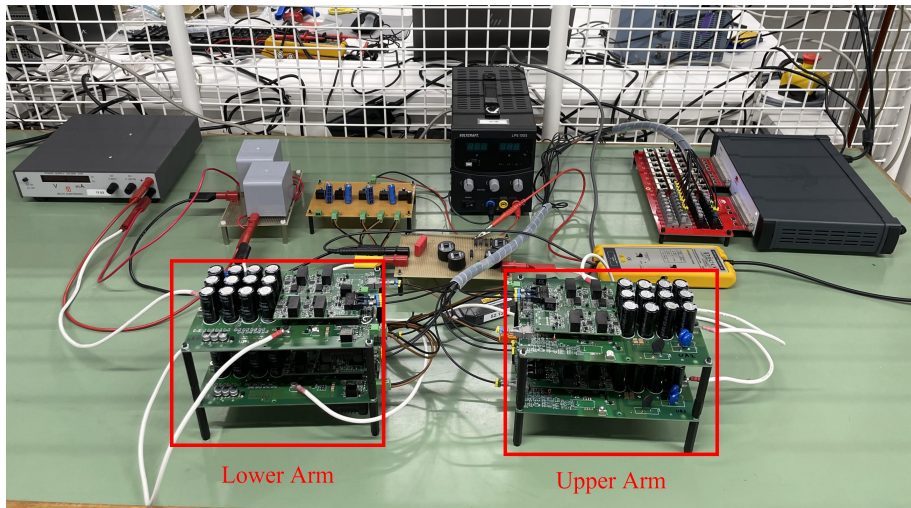
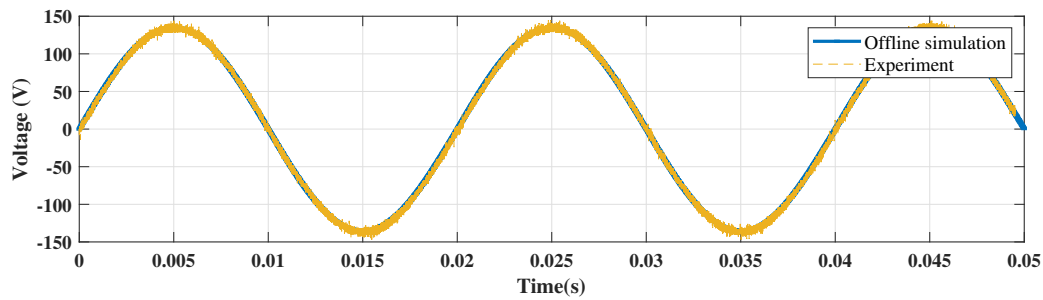
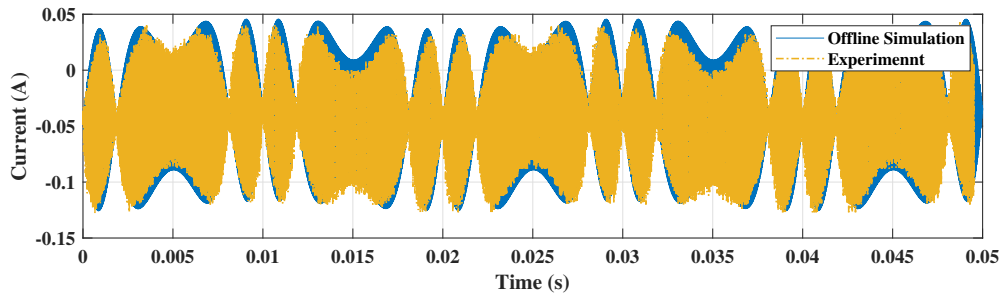


Figure 5.12: Output current across Load for $N = 1$

5.1.5. MMC with two sub-modules in each arm

Once the MMC setup is tested for $N = 1$, the next step is to verify the operation of the converter with $N = 2$. In order to do so a similar setup for testing was used which can be seen in figure 5.13 below. Two sub-modules were stacked on top of each other for each arm. The real-time simulator was configured to send gate pulses to sub-modules of the MMC. A current probe was used to measure the output current through the load, and a differential probe was used to measure the output voltage. In order to measure the capacitor voltage, all four boards were calibrated using the same way as described earlier. The parameters for the simulation used were the same as that mentioned in table 5.2. The output voltage and output current waveform results were analyzed and compared with that of offline simulation. The simulation step for Real-time testing was set to 500 ns. It was observed that the results from the experiment were identical to the results from the simulation. This can be confirmed by figures shown in 5.11 and 5.12.

Figure 5.13: RCP setup for MMC with $N = 2$ Figure 5.14: Output voltage across load for $N = 2$ Figure 5.15: Output current across load for $N = 2$

5.2. Impulse Generator Circuit

As mentioned in chapter 4, in a conventional impulse generator circuit when the spark gap is triggered a large pulsed current flows through the circuit corresponding to the discharge. As a result, usually, the sphere gap and the wave shaping network are designed to withstand this current stress. However, in this case, since the sphere gap was modeled as a MOSFET, the implementation of this switch is very important for the proper functioning of the impulse circuit. Consequently, in order to select the appropriate switch, the peak value of the current

flowing through the switch was calculated. When the DC link voltage was set to 300 V and the impulse trigger was applied at 0.035s, the current was analyzed and this is depicted in Figure 5.16

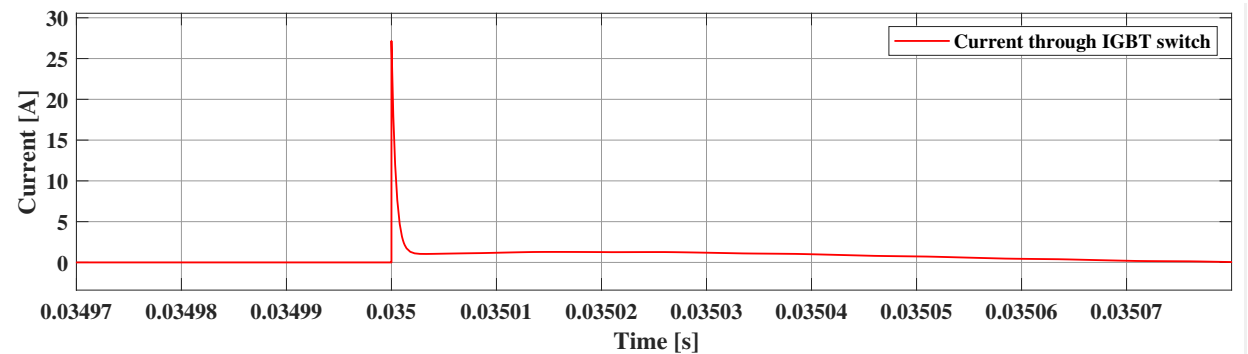


Figure 5.16: Current through Impulse switch

From the simulation results, it was evident that during the impulse discharge roughly 25 A flowed through the MOSFET switch. Therefore, the switch SiC MOSFET H090 was used as it had a current capability of 25 A rated. A single switch was soldered and implemented on the PCB board shown below in figure 5.17. The gate driver ADUM4135BRWZ was used to drive the MOSFET switch. The Board was configured with Fiber optic receivers to gate pulses at the desired time instants. The PCB board can be powered using a 12 V DC input supply, and a 12/5V DC-DC converter is used to power the fiber optic receiver.

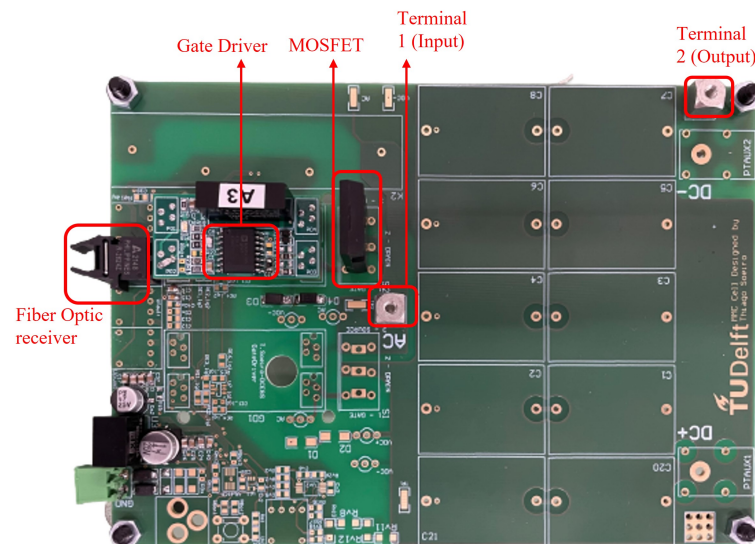


Figure 5.17: MOSFET switch Implementation

The wave shaping network including the front and the tail resistors, blocking condensers, and the additional capacitor designed in chapter 4, were implemented on a general purpose board

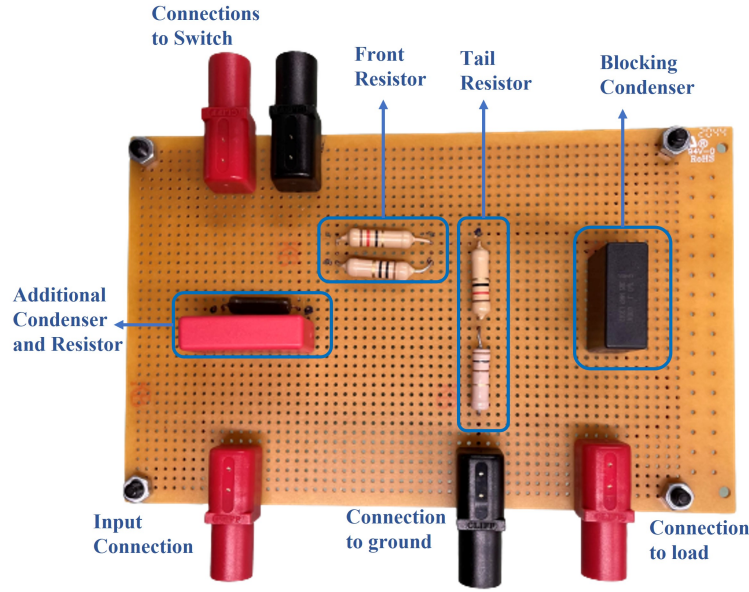


Figure 5.18: wave shaping network

as shown in figure 5.18 above. Film-type capacitors were used to implement the additional, blocking, and load capacitor. Wire wound resistors were used to implement R_f , R_h and R_d (discharge resistor in parallel with an additional condenser). The wire wound resistors were selected based on the nominal power requirements derived from the simulation results, which are summarised below in the table 5.3. Before implementing the hardware setup for the super-

Resistor	Value (Ω) [from Off. sim]	Value (Ω) Selected	RMS current (mA) [from Off. sim]	Power Rating (W)	Rating Selected (W)
Front resistor (R_f)	5.43	10 12 (5.45)	80.04	0.03	0.25
Tail resistor (R_h)	111.11	100 + 12 (112)	33.15	0.12	0.5
Discharge resistor	10^6	10^6	0.1	0.01	0.25

Table 5.3: Selection of Resistors

imposed lightning impulse test on the capacitive load, the waveshaping network and the Impulse trigger switch were tested to obtain a conventional lightning impulse waveform across the 100 nF load. The setup for this test is shown in figure 5.19. A DC source was used to supply the high side capacitor of the split capacitor configuration, and the midpoint of the DC link capacitor branch was connected to the negative of the DC source. The positive of the DC source capacitor is connected to the General purpose board to introduce the waveshaping network via the MOSFET modeled switch. Typhoon HIL was used to set the impulse trigger pulse to the switch. A square wave pulse was used to trigger the impulse, with an on period of 300 μ s. A load of 100 nF was connected between the common ground and the output of the

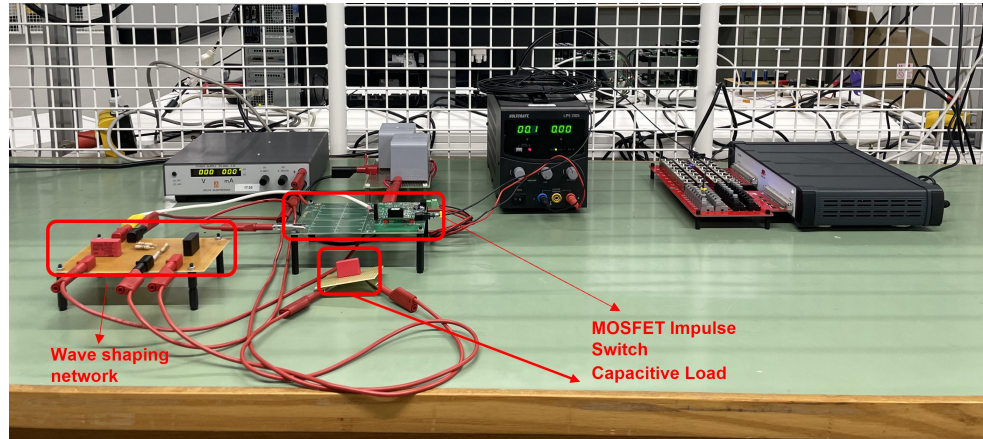


Figure 5.19: Setup for Lightning impulse

general purpose board. A differential probe was used to measure the voltage across the load. The current through the load was measured using a current probe. Both the waveforms were plotted on an oscilloscope which is shown in figure 5.20. The green waveform in the figure represents the voltage across the DUT and the purple-colored waveform corresponds to the current flowing through the load.

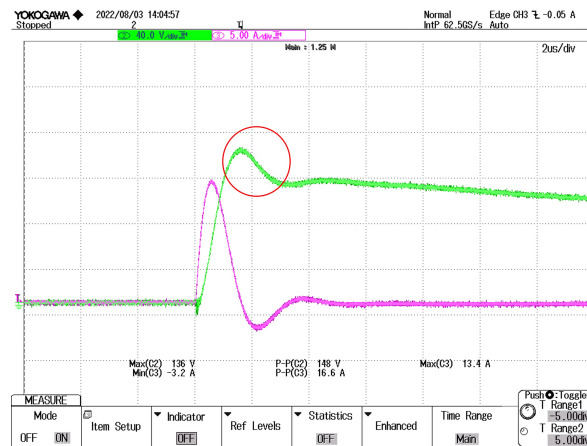


Figure 5.20: Impulse voltage across the 100 nF load

The input DC voltage was set to 150 V, and the output voltage peak obtained was around 136 V. It can be observed that the impulse voltage across the load has an overshoot (highlighted in red), this is due to the presence of stray inductance in the test loop.

5.3. Integrated hybrid test circuit

After validating the impulse generating circuit, the following step is to implement the setup for the integrated hybrid of the MMC and Impulse generator to obtain superimposed lightning impulses. The MMC configuration with two sub-modules in each arm was used and the impulse generation circuit was connected to it according to the schematic designed in chapter 4.

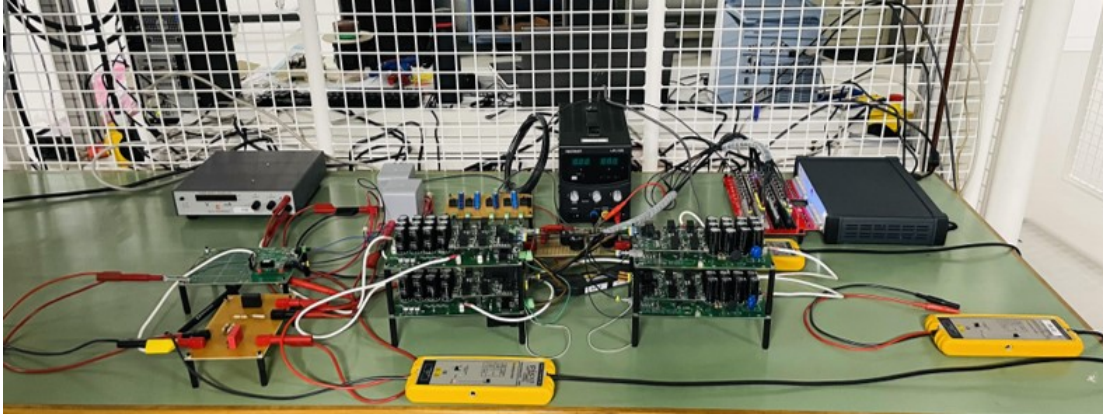


Figure 5.21: Hardware setup for the Integrated Hybrid

to obtain an integrated hybrid configuration. Figure 4.7 illustrates the circuit schematic and figure 5.21 depicts the Hardware setup for the superimposed test. During the simulation the DC link voltage was set to 300 V. The HIL device was configured to send gate pulses to the MMC sub-modules and a trigger pulse to the Impulse switch. In order to have control over the instant at which the impulse is applied on the power frequency waveform, the gate pulses to the MOSFET impulse switch were fed to an AND gate with a constant block which could be changed by the user on the fly. The constant block was set to 0 by default, however, during the simulation when this was set to 1, the output of the AND gate was high and impulses were enabled and superimposition took place. Based on the Offline simulation results shown in chapter 4 for the integrated hybrid, the pulse generator was configured in such a way that once enabled the impulse would be triggered at the peak of the Power frequency AC. This can however be changed by adjusting the phase shift in the square wave pulse generator block.

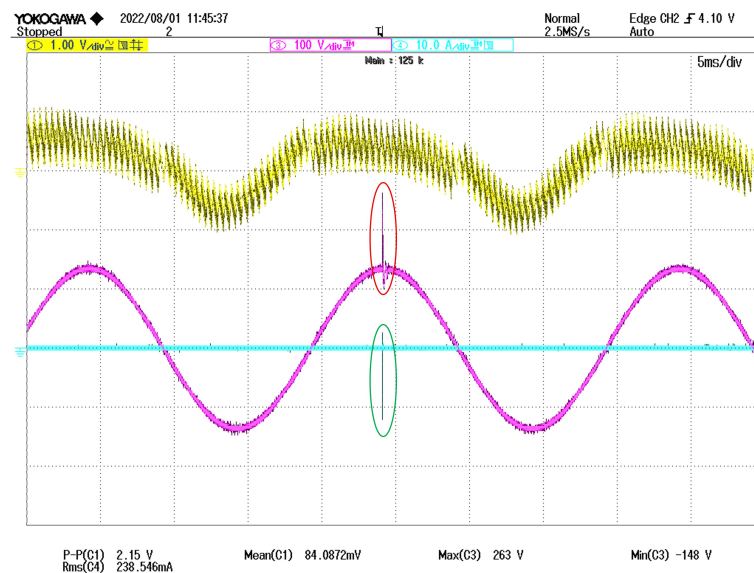


Figure 5.22: AC Superimposed Impulse across Capacitive load

Figure 5.22 shows the output voltage across the capacitive load when the superimposed waveform was applied. In the figure, the purple waveform represents the voltage across the load, the cyan-colored waveform corresponds to the current through the load and the yellow-colored waveform represents the capacitor voltage ripple of the upper arm sub-module. It was observed that when the impulse was triggered, a lightning impulse was superimposed on the peak of the power frequency curve. However, during this, the voltage across the sub-module capacitor was not affected significantly. Figure 5.23 reveals that the results obtained from the experiments resembled quite closely to those from offline simulations. 5.24 shows the zoomed comparison of the lightning impulse on the power frequency waveform. It was observed that the impulse wave obtained during the experiment had an overshoot as compared to the offline simulation, this is due to the fact that during the offline simulation the components and connections were ideal (ie without any stray inductance) however in reality there are a lot of stray inductances in the test loop which cause an overshoot[36].

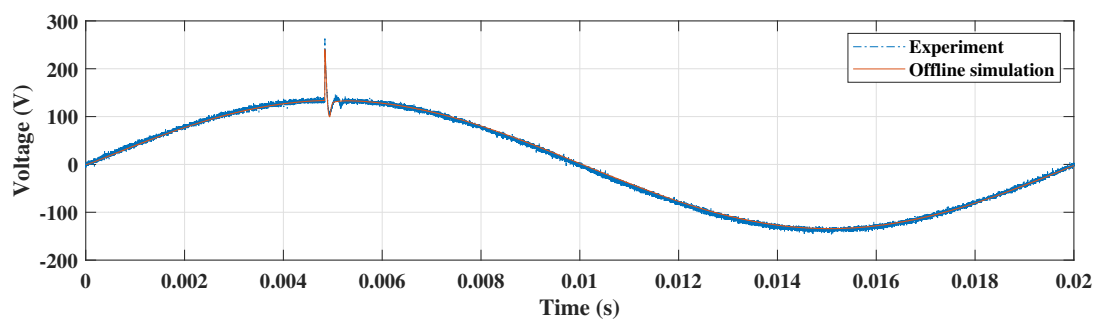


Figure 5.23: Superimposed voltage Comparison between Offline simulation and experiment

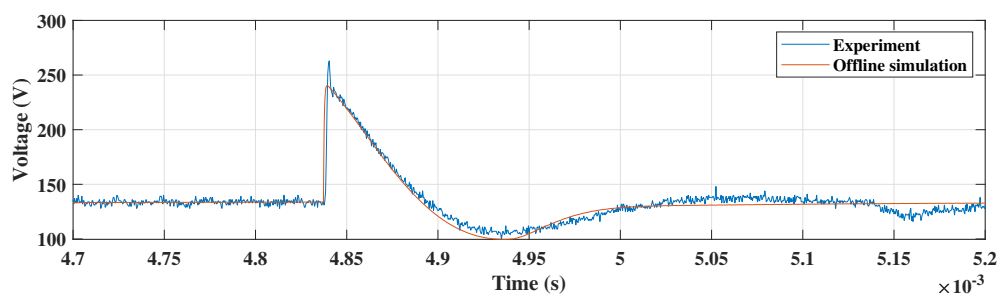


Figure 5.24: Zoomed comparison of superimposed lightning impulse

5.4. DC superimposed test

As stated in Chapter 1, with the growing trend towards transmitting power via the DC power lines, there is a strong need to test HVDC power cables for their reliable operation [4]. The IEC standard 62895 elaborates upon the testing requirements for HVDC cables. One of them is the DC superimposed impulse test. This test is a compounded test and helps to validate the performance of the cable against transient overvoltages due to lightning and switching impulses. One of the abilities of the MMC-based HV test source is to generate complex wave

shapes, therefore the MMC setup constructed in the previous section with two sub-modules in each arm was used to test its capability to generate DC superimposed voltage waveforms. Two tests were performed on a capacitive load of 100 nF - 1) Superposition of + DC and + Impulse and 2) superposition of -DC and - Impulse.

Table 5.4 summarises the testing parameters.

Parameter	Value
Modulation index	0.9
Input DC Voltage	300 V
Switching frequency	50 kHz
Dead Time	250 ns
Arm Inductance	6 mH
Arm resistance	90 Ω
Load Capacitance	100 nF

Table 5.4: Parameters for DC superimposed test

The HIL device was used to send gate pulses to the sub-modules to generate the required DC reference. It was observed that for both the conditions the voltage across the DUT very closely resembled the waveform from offline simulation. However, due to the stray inductance of the test loop, there was an overshoot in the impulse peak. Figure 5.25 and 5.26 illustrates the comparison of the experiment results with offline simulation.

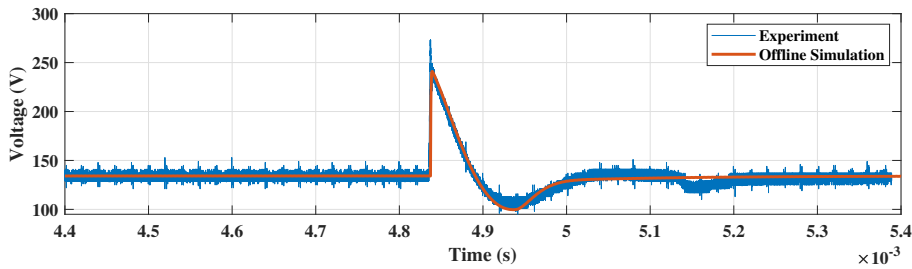


Figure 5.25: Positive DC and Positive Impulse wave superposition

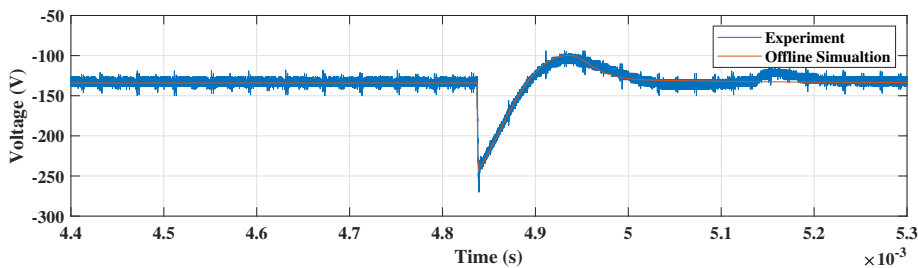


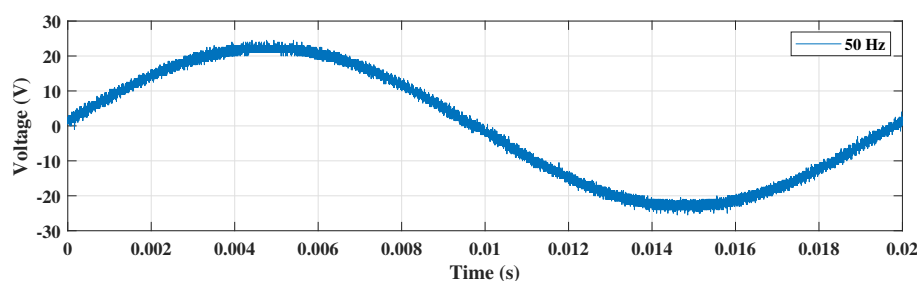
Figure 5.26: Negative DC and Negative Impulse wave superposition

5.5. Test Signal Bandwidth

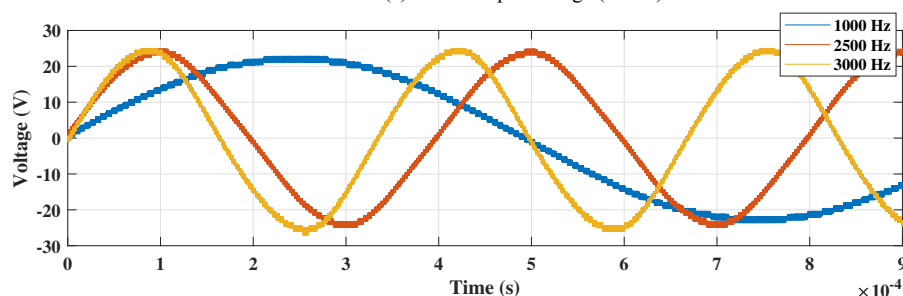
Conventional test sources are capable of generating test waveforms with very high accuracy, however, a single test source is limited in terms of its bandwidth capabilities (i.e it cannot produce signals of identical type for a range of frequencies). One of the objectives of this thesis is to investigate the capabilities of the MMC-based HV source to generate accurate test signals for a range of frequencies, and also to investigate the ability of Typhoon HIL to generate control signals for the same with high accuracy. *It is important to note that the discussion for the bandwidth of test signals in this thesis is limited to sinusoidal waveforms.* The MMC setup with two sub-modules in each arm was used. Gate pulses based on FPGA control were used to obtain the required sinusoidal reference at the output of MMC. Since the sinusoidal reference used for the PSC modulation is modeled on the CPU, the execution rate of the source is crucial in determining the quality (resolution) of the reference. The open loop control developed in chapter 3 was used to obtain sinusoidal output from the MMC. The real-time simulation was carried out for 4 cases - with a fundamental frequency of reference as 50 Hz, 1 kHz, 2.5 kHz, and 3 kHz. Table 5.27 summarises the simulation parameters used.

Fundamental Freq (Hz)	Switching Freq (Hz)	Execution rate
50	10004	2 μ s
1000	100787	2 μ s
2500	143291	2 μ s
3000	177969	2 μ s

Table 5.5: Simulation Parameters for High-frequency simulation



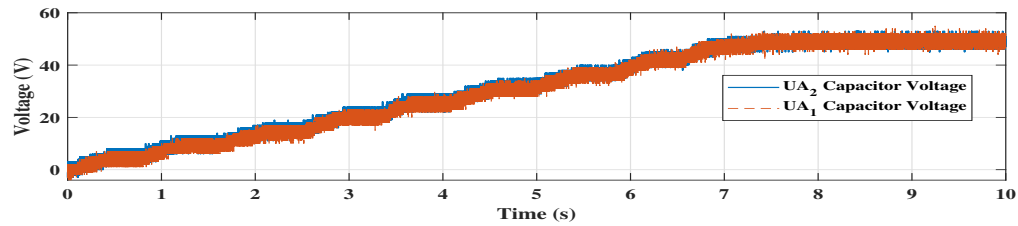
(a) MMC output voltage (50 Hz)



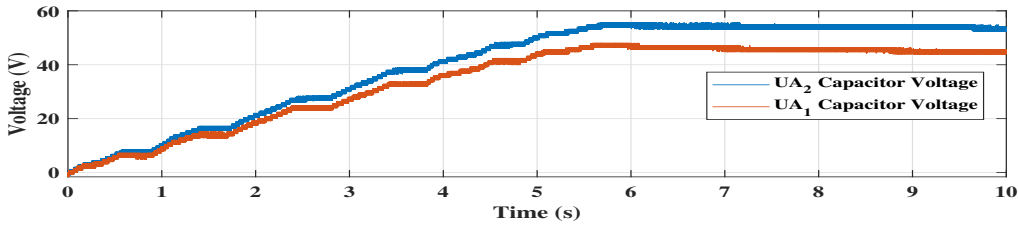
(b) MMC output voltage (1, 2.5 and 3 kHz)

Figure 5.27: MMC output voltage for higher fundamental frequency

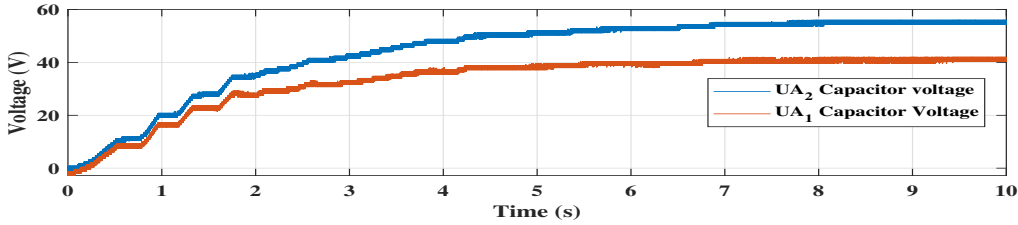
The correct choice of the switching frequency affects the way in which capacitor voltages are balanced in an arm [27]. Therefore, in order to balance the capacitor voltages switching frequency was selected in such a way that it was not an integral multiple of the fundamental reference. Figure 5.27 above summarises the results from the simulation. It was observed that the MMC is able to generate a sinusoidal output of the desired frequency across the load. However, it can be seen that the output voltage has small steps, which can be improved by increasing the number of sub-modules in each arm. Furthermore, during the high-frequency operation, it was noted that the capacitor voltages get un-balanced, this might be due to the selection of the switching frequency during the switching. Figure 5.28 illustrates the capacitor voltage distribution between the upper two arm sub-modules for each case.



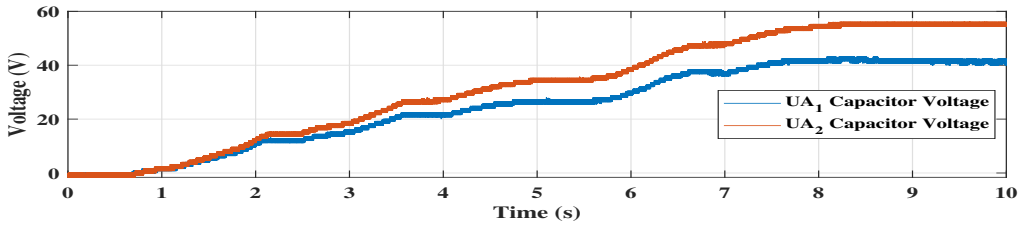
(a) Capacitor Voltage distribution between upper Sub-modules at 50 Hz fundamental



(b) Capacitor Voltage distribution between upper Sub-modules at 1000 Hz fundamental



(c) Capacitor Voltage distribution between upper Sub-modules at 2500 Hz fundamental



(d) Capacitor Voltage distribution between upper Sub-modules at 50 Hz fundamental

Figure 5.28: Capacitor Voltages for upper and lower arm

5.6. Summary

This chapter summarises the hardware implementation of the MMC-based test source and the Integrated hybrid configuration to validate the results obtained. The hardware implementation was carried out in a step-by-step manner. First, a single MMC sub-module was tested as a two-level inverter leg, and later on the full converter with one and subsequently, two sub-modules in each arm were implemented. Each board was calibrated to be able to measure the capacitor voltage of the sub-module. It was inferred that the results from hardware experiments (for both Rapid control prototyping and superimposed impulse tests) were coherent with the expected results from offline simulation. However, it was observed that the impulse voltage waveform obtained from experiments had an overshoot due to the stray inductance of the test loop. Furthermore, the integrated hybrid was also used to test for superimposed DC waveforms. It was concluded that the MMC integrated hybrid could successfully produce DC superimposed waveforms of both polarities with very high accuracy. Finally, the MMC setup developed for RCP was used to test the output of the MMC at higher frequencies. For all the hardware experiments, Typhoon HIL was connected to the MMC setup through a fiber optic interface. It was concluded that during the test for signal bandwidth, the output voltage obtained was a smooth Sinusoidal wave of the desired frequency. However, as the frequency of the fundamental reference increases, the capacitor voltages get unbalanced. This is due to the choice of the switching frequency used for the PSC modulation. It needs to be optimized for the future.

6

Conclusion and Recommendations

This chapter being the final chapter of the thesis presents a consolidated conclusion for the research carried out. The limitations are discussed and recommendations for future work are suggested

6.1. Conclusion

The two main objectives of this thesis - to implement the open loop control of MMC using Typhoon HIL and, to investigate and demonstrate the feasibility of an integrated Hybrid configuration of an impulse generator and MMC have been met successfully. An open loop control based on PSC modulation technique was developed on the CPU and the FPGA of Typhoon HIL. A 300 V down-sized prototype of consisting of 4 sub-modules was used to build the MMC. An integrated hybrid configuration was designed based on the requirements of composite testing. The following conclusions can be drawn answering the research questions:

- A user handbook compiling detailed information about Typhoon HIL hardware and software is made available as a result of this thesis.
- The HIL device can be configured manually using the software to utilise the HIL FPGA resources flexibly.
- By default, it is not possible to model individual Power electronic switches such as MOS-FET/IGBT. Also, There are limitations on the number of components that can be modeled on a given core. As a result, model partitioning can be used to split a complex model on to separate cores while meeting RT constraints.
- For PSC modulation, the CPU control is suitable for up to 1 kHz of fundamental reference frequency, beyond which FPGA control is recommended.
- While testing the MMC for higher signal bandwidth, The accuracy of the gate pulses generated by the RT simulator largely depend on the quality of the sinusoidal reference used. Typhoon HIL can generate a smooth sinusoidal signals up to 5 kHz, whereas OPAL-RT

begins to steps in the sinusoidal reference from 1 kHz itself. For a model with similar complexity, the minimum time-step achieved in Typhoon HIL is 200 ns whereas it is 10 μ s for OPAL-RT. Therefore concluding that the Typhoon HIL out performs OPAL-RT in generating accurate gate-pulses for higher signal bandwidths.

- With careful choice of the coupling capacitor, additional capacitor and the discharge resistor, it is possible to design an integrated hybrid configuration.
- The designed integrated hybrid configuration can successfully produce positive and negative polarity superimposed impulses on the power frequency and DC waveform.
- The MMC developed can produce sinusoidal voltage output up to 3 kHz (with Typhoon FPGA control). As the fundamental frequency increases the capacitor voltages get unbalanced.

6.2. Future Recommendations

The following recommendations can be made for further improvements:

- The conventional impulse generator has a relatively low input voltage and the output is a much higher voltage. This is because an impulse generator has multiple stages and usually two or more are used to achieve higher voltage levels. The integrated hybrid configuration designed and developed in this thesis is based on a single-stage impulse generator i.e. if the DC source voltage is charged to some 'x' V then the output magnitude of impulse voltage is also roughly in the same order 'x' V. Therefore, the integrated hybrid configuration can be further improved to incorporate a multi-stage circuit to have high impulse voltage.
- The Typhoon HIL device is capable of generating accurate FPGA-based gate pulses for higher fundamental frequencies up to 3 kHz. However, as the fundamental frequency increases the capacitor voltages get unbalanced. This can be improved by optimizing the value for the switching frequency. Alternatively, the capacitor voltage distribution can be improved by implementing a closed-loop control based on the arm-energy controlling principle.

Bibliography

- [1] D. Ganeshpure, T. B. Soeiro, M. G. Niasar, P. Vaessen, and P. Bauer, “Design trade-offs of modular multilevel converter-based arbitrary wave shape generator for conventional and unconventional high voltage testing,” *IEEE Open Journal of the Industrial Electronics Society*, vol. 2, pp. 584–605, 2021, ISSN: 26441284. DOI: 10.1109/OJIES.2021.3125747.
- [2] G. Ueta, T. Tsuboi, J. Takami, S. Okabe, and A. Ametani, “Insulation characteristics of gas insulated switchgear under lightning impulse and ac superimposed voltage,” *IEEE Transactions on Dielectrics and Electrical Insulation*, vol. 21, 2014. DOI: 10.1109/TDEI.2014.004436.
- [3] J. Yang, Y. Ma, K. Zhao, *et al.*, “Partial discharge characteristics of typical insulation defect under ac and impulse superimposed voltage in sf6 gas,” Institute of Electrical and Electronics Engineers Inc., Sep. 2020, ISBN: 9781728155111. DOI: 10.1109/ICHVE49031.2020.9279500.
- [4] Z. Liu, B. Ouyang, Z. Chen, P. Zhao, and J. Zhao, “Research on circuit parameter configuration of dc superimposed impulse voltage test on uhv dc cable,” Institute of Electrical and Electronics Engineers Inc., Oct. 2020, pp. 3372–3377, ISBN: 9781728196060. DOI: 10.1109/EI250167.2020.9346768.
- [5] H. W. Dommel, “Electromagnetic transients in single- and multiphase networks,” *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-88, pp. 388–399, 4 1969. DOI: 10.1109/TPAS.1969.292459.
- [6] “Variable time step, implicit integration for extended-term power system dynamic simulation,” IEEE, 1995, pp. 183–189. DOI: 10.1109/pica.1995.515182.
- [7] J. J. Belanger, P. Venne, and J. Paquin, “The what, where and why of real-time simulation,” *Planet RT*, vol. 1, pp. 25–29, 2010.
- [8] *Fpga solver basics*. [Online]. Available: https://www.typhoon-hil.com/documentation/typhoon-hil-software-manual/concepts/fpga_solver_basics.html#concept_dtw_dvp_kz__signal_gen.
- [9] *Pwm modulator*. [Online]. Available: https://www.typhoon-hil.com/documentation/typhoon-hil-software-manual/References/pwm_modulator.html.
- [10] *Cfunction*. [Online]. Available: https://www.typhoon-hil.com/documentation/typhoon-hil-software-manual/References/c_function.html.
- [11] *Hilscada*. [Online]. Available: https://www.typhoon-hil.com/documentation/typhoon-hil-software-manual/concepts/hil_scada.html.

- [12] *Action widgets*. [Online]. Available: https://www.typhoon-hil.com/documentation/typhoon-hil-software-manual/References/action_widgets.html#reference_glg_fsp_q1b.
- [13] *Monitoring widgets*. [Online]. Available: https://www.typhoon-hil.com/documentation/typhoon-hil-software-manual/References/monitoring_widgets.html.
- [14] *Analysis widgets*. [Online]. Available: https://www.typhoon-hil.com/documentation/typhoon-hil-software-manual/References/analysis_widgets.html.
- [15] *Status bar*. [Online]. Available: https://www.typhoon-hil.com/documentation/typhoon-hil-software-manual/concepts/status_bar.html.
- [16] *Core couplings - ideal transformer*. [Online]. Available: https://www.typhoon-hil.com/documentation/typhoon-hil-software-manual/References/core_couplings_IT.html.
- [17] *Core couplings - tlm*. [Online]. Available: https://www.typhoon-hil.com/documentation/typhoon-hil-software-manual/References/core_couplings_TLM.html.
- [18] *Core marker*. [Online]. Available: https://www.typhoon-hil.com/documentation/typhoon-hil-software-manual/References/core_marker.html.
- [19] *Cpu marker*. [Online]. Available: https://www.typhoon-hil.com/documentation/typhoon-hil-software-manual/References/cpu_marker.html.
- [20] *Cpu transition*. [Online]. Available: https://www.typhoon-hil.com/documentation/typhoon-hil-software-manual/References/cpu_transition.html.
- [21] K. Sharifabadi, L. Harnefors, H.-P. Nee, S. Norrga, and Teodorescu, *Design, control and application of modular multilevel converters for HVDC transmission systems*. Sep. 2016, pp. 1–386. DOI: 10.1002/9781118851555.
- [22] A. Lesnicar and R. Marquardt, “An innovative modular multilevel converter topology suitable for a wide power range,” vol. 3, IEEE Computer Society, 2003, pp. 6–11, ISBN: 0780379675. DOI: 10.1109/PTC.2003.1304403.
- [23] *Svpwm (space vector pulse width modulation) reference generator*. [Online]. Available: https://www.typhoon-hil.com/documentation/typhoon-hil-software-manual/References/svpwm_generator.html.
- [24] J. al-Wādī. Department of Electrical Engineering, I. of Electrical, E. E. A. Section, I. of Electrical, and E. Engineers, “Ccssp 2020 : 020 1st international conference on communications, control systems and signal processing : 16-17th march, 2020, el-oued, algeria,” ISBN: 9781728158358.
- [25] P. Omer, J. Kumar, and B. S. Surjan, “Comparison of multicarrier pwm techniques for cascaded h-bridge inverter,” IEEE Computer Society, 2014. DOI: 10.1109/SCECS.2014.6804463.

- [26] D. Ganeshpure, "Modular multilevel converter (mmc) based high voltage test source demonstration of a proof of concept with a mathematical model and simulation study for arbitrary wave shapes generation," Ph.D. dissertation, Feb. 2021.
- [27] K. Ilves, L. Harnefors, S. Norrga, and H. P. Nee, "Analysis and operation of modular multilevel converters with phase-shifted carrier pwm," *IEEE Transactions on Power Electronics*, vol. 30, pp. 268–283, 1 2015, ISSN: 08858993. DOI: 10.1109/TPEL.2014.2321049.
- [28] *Cpu transition*. [Online]. Available: https://www.typhoon-hil.com/documentation/typhoon-hil-software-manual/References/cpu_transition.html.
- [29] *Execution rates*. [Online]. Available: https://www.typhoon-hil.com/documentation/typhoon-hil-software-manual/References/execution_rates.html.
- [30] *Real-time digital simulation platform □ real time system □ op4512*. [Online]. Available: <https://www.opal-rt.com/simulator-platform-op4512/>.
- [31] I. of Electrical and E. Engineers, "2019 international conference on high voltage engineering and technology (ichvet2019).," ISBN: 9781538675762.
- [32] *Iec 60230 ed.2.0," impulse test on cables and their accesories"*, 2018.
- [33] *Iec 60060 ed.3.0," high voltage test techniques- part 1: General definitions and test requirements"*, 2011.
- [34] O. Pischler and U. Schichler, "Challenges resulting from the use of spark gaps for superimposed voltage tests," vol. 2018-May, Institute of Electrical and Electronics Engineers Inc., Jun. 2018, pp. 678–681, ISBN: 9781538657881. DOI: 10.1109/ICPADM.2018.8401142.
- [35] E. Kuffel, W. S. Zaengl, and J. Kuffel, *Chapter 2 - Generation of high voltages*, Second Edition, E. Kuffel, W. S. Zaengl, and J. Kuffel, Eds. Newnes, pp. 8–76, ISBN: 978-0-7506-3634-6. DOI: <https://doi.org/10.1016/B978-075063634-6/50003-4>.
- [36] F. Kreuger, *Industrial High Voltage*. 1992, vol. 2, pp. 48–54.



Typhoon HIL

A.1. Creating a new model using Typhoon HIL

The following steps can be used to build a simple model:

1. Open Typhoon HIL Center.
2. If you want to test the model in RT, make sure the HIL device is connected via the USB or ethernet port.
3. After physically connecting the HIL to the computer, click on the device manager prompt on the top left corner of the Typhoon HIL control center menu.
4. Select the device to be connected on the right-hand part of the screen and then click on the green arrow to connect the HIL device to the computer as shown in figure A.1. (Note that steps 2-4 can be skipped if you want to run a model in Virtual HIL mode)

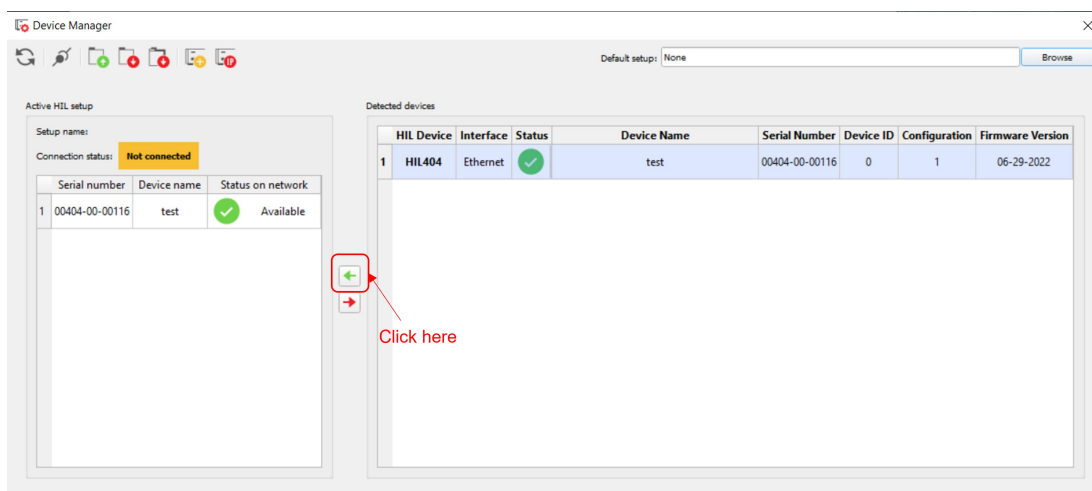


Figure A.1: Connecting the HIL device

5. Click on the schematic editor prompt from the main typhoon HIL control center menu.
6. This will open the schematic editor window, to create a new blank model click on the first prompt on the toolbar located on the top of the screen as shown in the figure A.2.

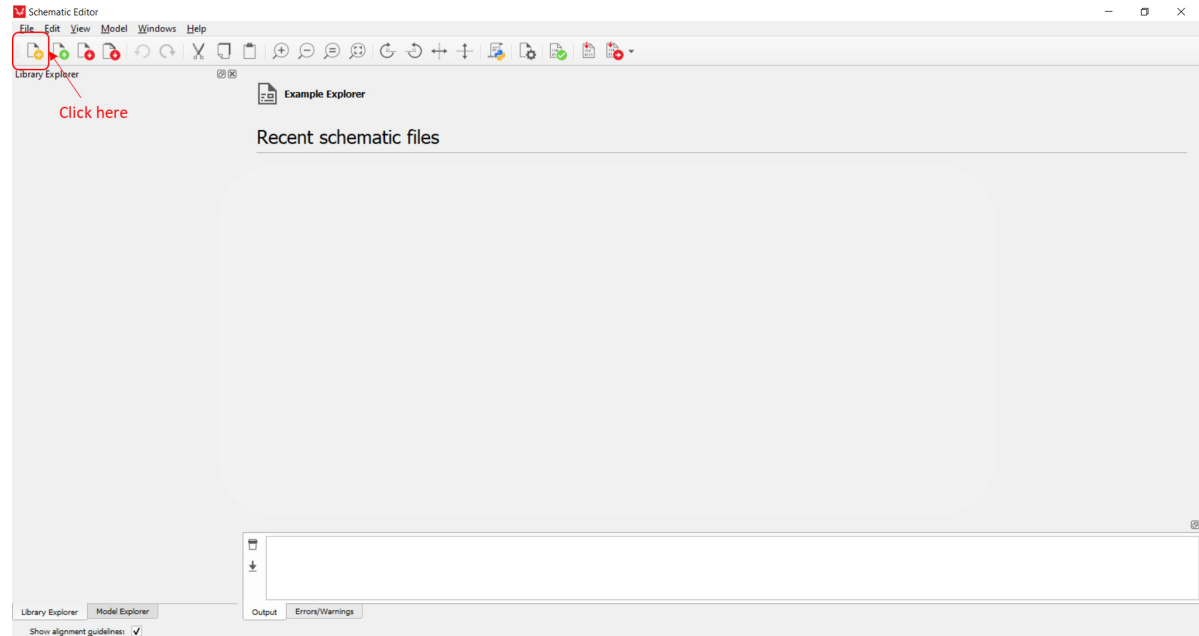


Figure A.2: Schematic editor user interface

7. Alternatively, it is also possible to create a new model by clicking on File, then new and new model.(or Ctrl + N)
8. Once a new model is selected, a model wizard window will pop up. This allows the user to define the model settings needed to test the model.
9. Select the HIL device connected manually or simply click on the detect hardware menu which will automatically detect the HIL device and the configuration being used.
10. The configuration can be changed manually if needed. The device table can be used to identify the distribution of HIL resources in each configuration type.
11. Select the time step and the method needed for the simulation and click ok. (Note if it is left auto then Typhoon will take the minimum possible to meet the RT simulation constraints).
12. After selecting the model settings, a blank model space appears where the desired model can be constructed.
13. Components to be added to the model can be found from the library explorer located on the left part of the screen. Drag and drop the components to the editor space. As an illustration, building an IGBT-based two-level inverter is shown here.

14. Add an IGBT leg, a Voltage source(DC), a resistor, and a ground reference from the library explorer.
15. The switches in the converter leg can be controlled using the internal PWM modulators. To set the control, double-click on the IGBT leg block.
16. In the window that appears set the control to Internal modulator as shown in figure A.3. Thereafter, select the switching frequency to 10 kHz and dead time of 200 ns, and click ok.

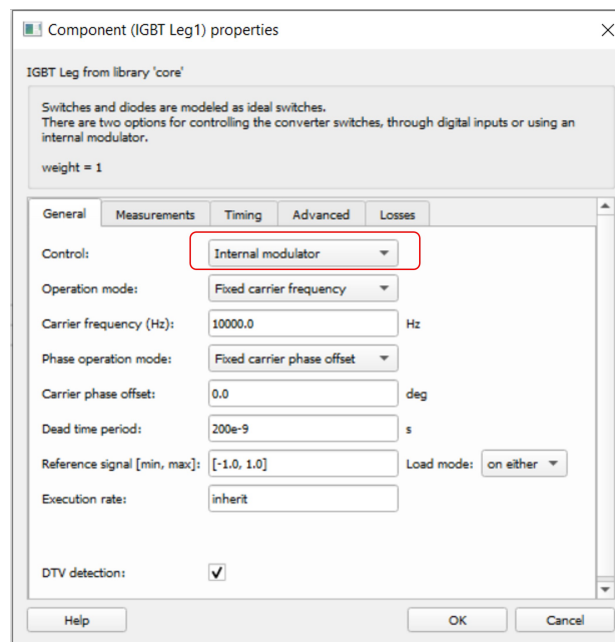


Figure A.3: IGBT Leg Control

17. To use the internal PWM modulator block, the control needs an enable and a reference signal. Connect a constant block with value 1 to the enable port and a sinusoidal source of 50 Hz with modulation of 0.9 to the reference port of the IGBT leg block as shown in figure A.4 for connections.
18. To measure the voltage across the output resistor add the voltage measurement component from the library. To visualize the output voltage on an oscilloscope within the typhoon, a probe needs to be connected to the output of the voltage measurement component.
19. Double click on the voltage measurement component and a properties window will appear. Click on the signal processing tab and enable the output signal. Now the probe can be connected to the voltage measurement component. Select a lower execution rate (2 μ s) for the signal processing. Figure A.5 shows the final connections of the components.

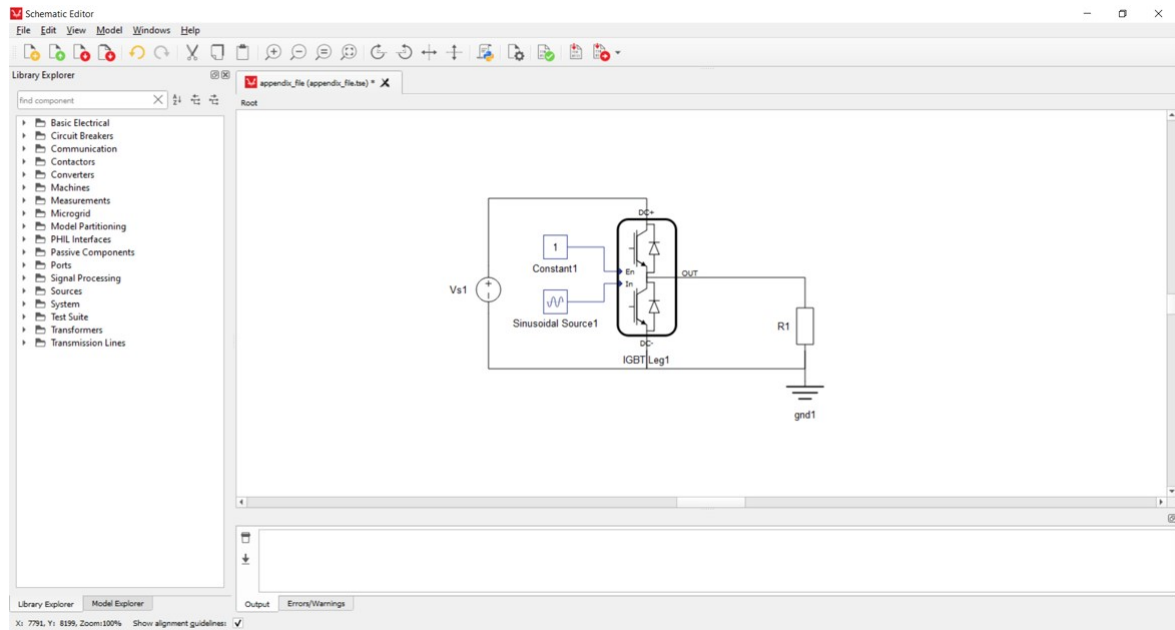


Figure A.4: Connection of components

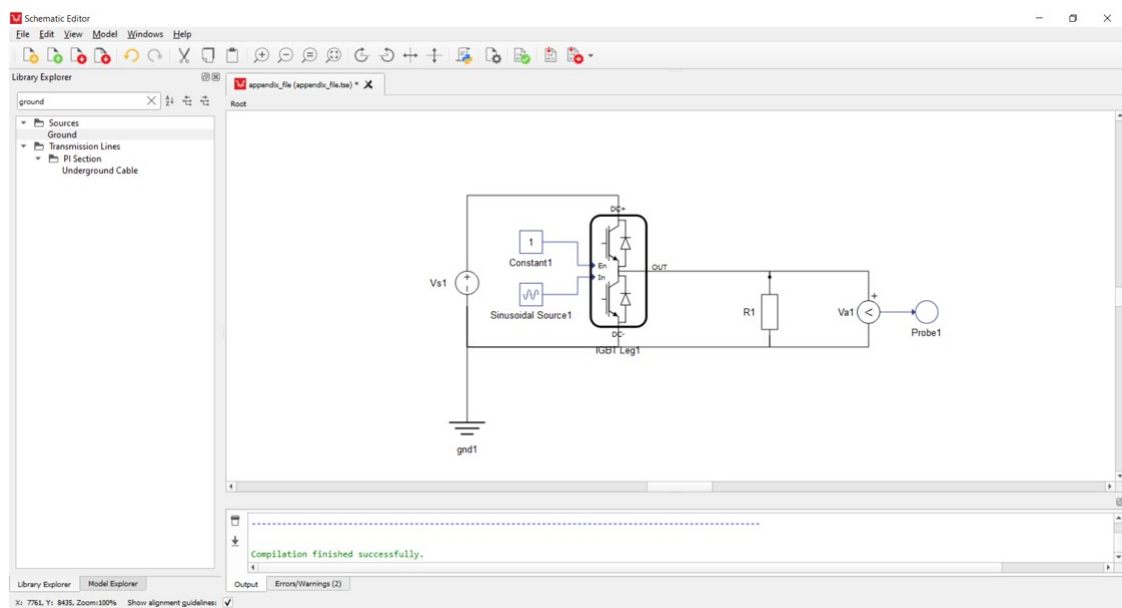


Figure A.5: 2 level IGBT leg model

20. It is also possible to define variables that can be used to initialize certain parameters in the simulation. To do so, click on the initialization script from the toolbar.
21. The initialization script accepts commands in python or C. For this illustration, set the DC voltage value to 100 V and resistor value as 10 Ω as shown in figure A.6.
22. After the model is constructed, the model needs to be validated before its run. To do

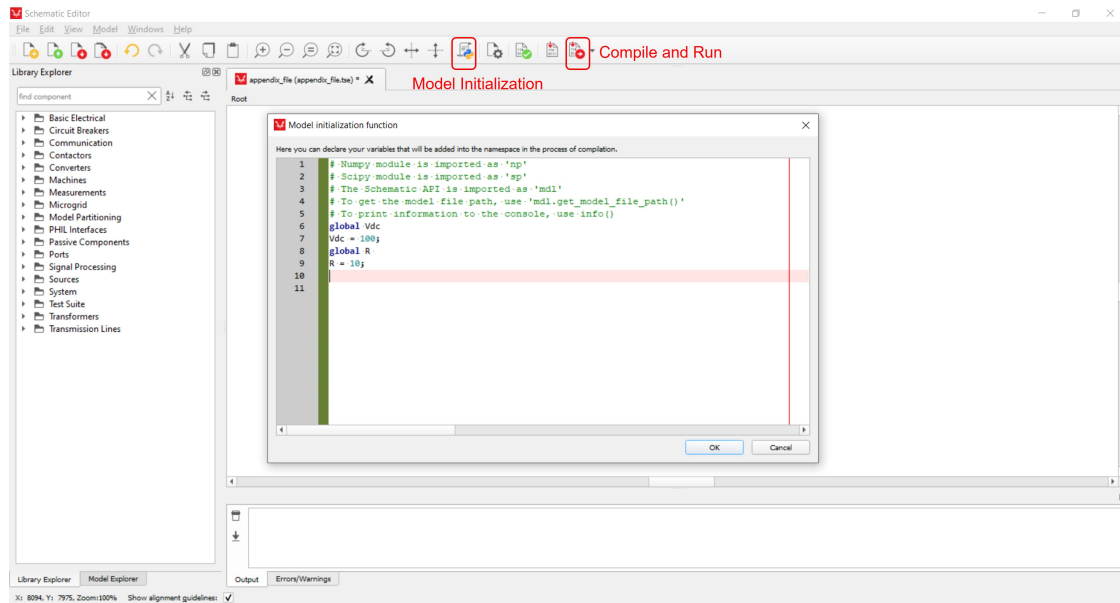


Figure A.6: Model initialization script

so click on the compile button from the toolbar. The log of the compilation process is shown in the message window as shown in the figure A.7.

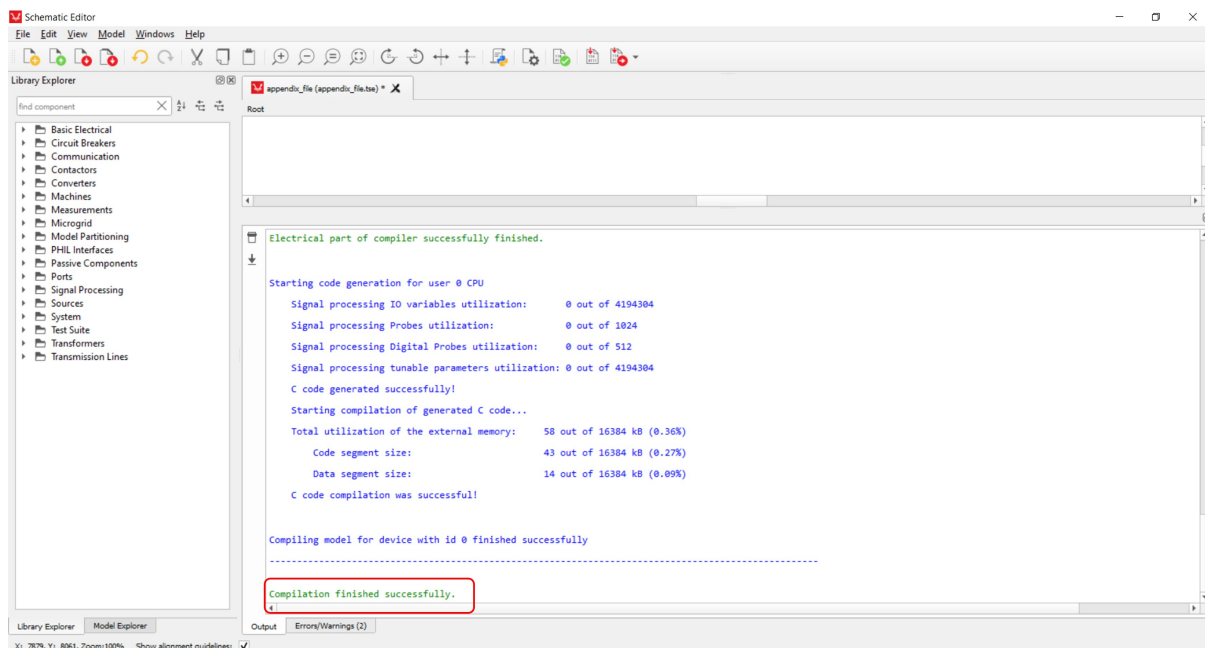


Figure A.7: message log

On successful compilation of the model, HIL SCADA is launched by default to run the simulation.

A.2. Running the model in HIL SCADA

The following steps can be used to run a Typhoon model (.tse) in HIL SCADA.

1. As mentioned in the previous section, the HIL SCADA tool is directly launched once the model is compiled successfully.
2. If you are not connected to the HIL device (i.e. running on virtual HIL mode). A screen will appear as shown in figure A.8, select virtual HIL mode.

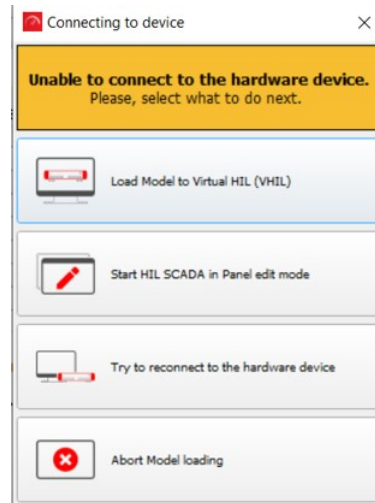


Figure A.8: Virtual HIL Mode

3. However, if the HIL device is connected step 2 is skipped, and the HIL SCADA window will open.
4. To begin the simulation and analyze parameters a panel file needs to be created. This can be done by clicking on the 'New panel' option as shown in figure A.9.
5. A blank space for the panel is created, where widgets can be added to interact with the simulation. As a part of the illustration, the model developed in section A.1 is run and analyzed.
6. Add Capture/scope widget from the library of HIL SCADA.
7. Double click on the scope to open the properties. Select capture mode and click on the 'Signals' prompt to add signals as shown in figure A.10. Add probe 1 signal to viewport 1 (which is the output voltage across the Resistor).
8. To add a trigger, click on the trigger settings as shown in the figure A.11. Select analog trigger (since the signal being measured is an analog signal) and select rising edge. Click ok.

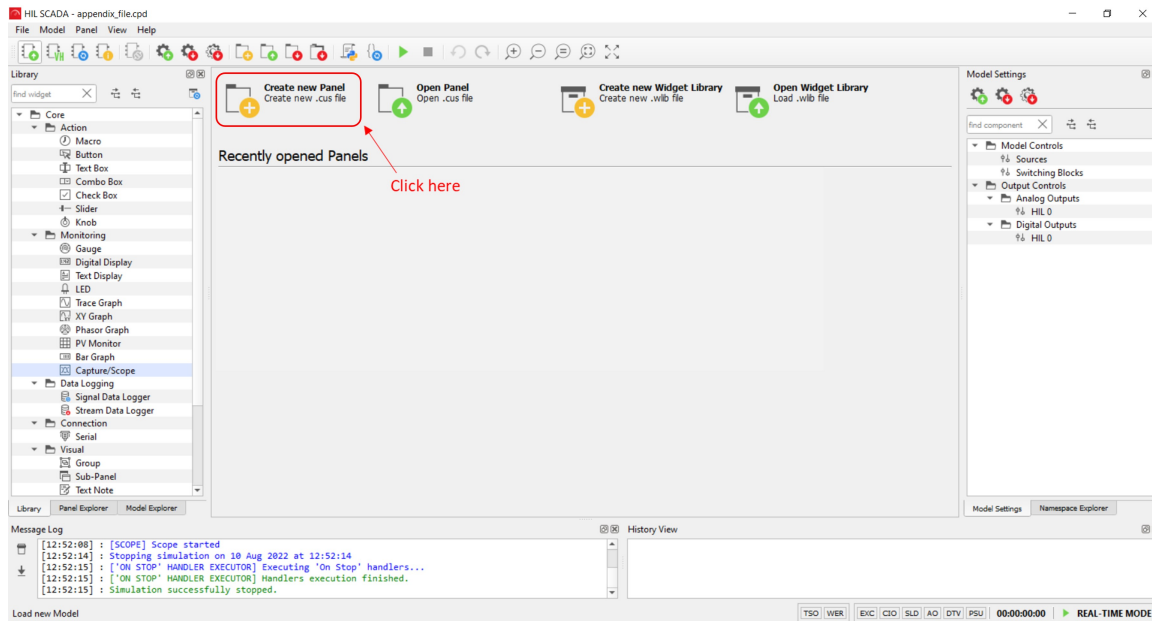


Figure A.9: HIL SCADA user interface

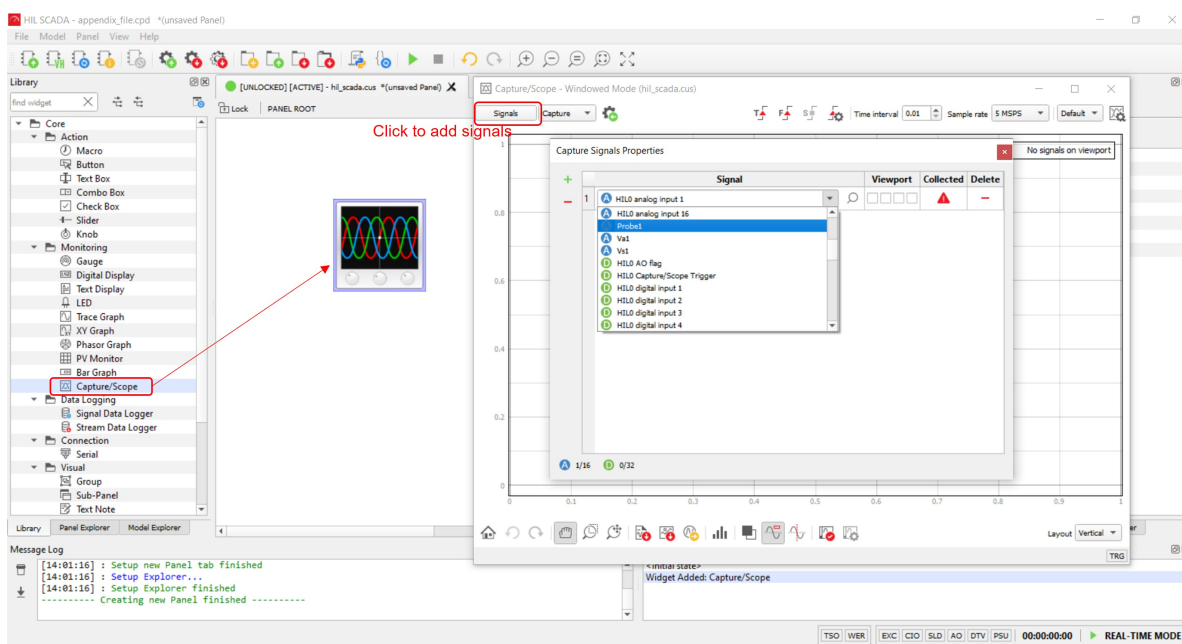


Figure A.10: Capture/scope widget

- Now click on the trigger option and click on the green prompt to run the simulation. The output voltage will be captured and displayed on the screen. To observe the FFT plot, select the FFT analysis option shown in figure A.12.

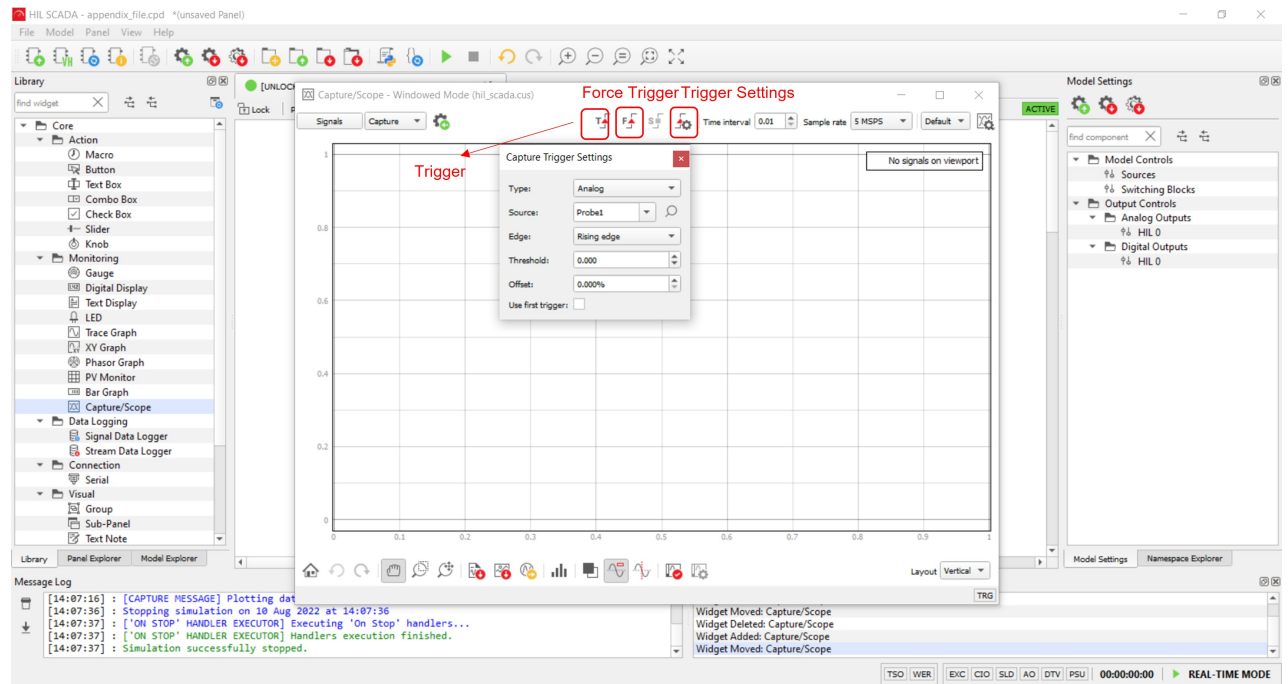


Figure A.11: Trigger settings for scope

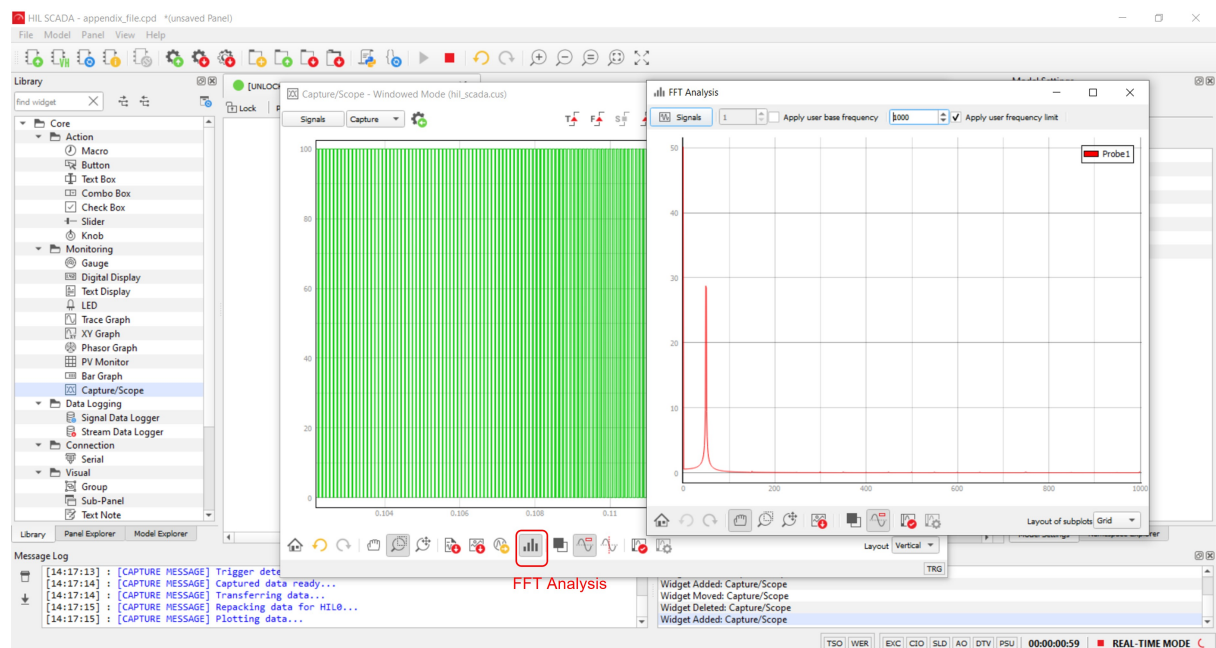


Figure A.12: 2 level IGBT leg output voltage across resistor

A.3. Exporting signal data from Typhoon HIL

The data points from a signal can be exported from typhoon using the signal streaming or logging widget in HIL SCADA. Signal streaming is recommended if a lower execution rate is

needed to store data, whereas signal logging can be used to store data with a much slower rate. The illustration here shows the use of the signal streaming widget. The output voltage across the resistor from the previous model was streamed. The following steps can be used:

1. Double click on the probe 1 signal to be streamed and click on the signal streaming option as shown in the figure A.13. A Wifi like a symbol will appear on the probe indicating that signal streaming is enabled.

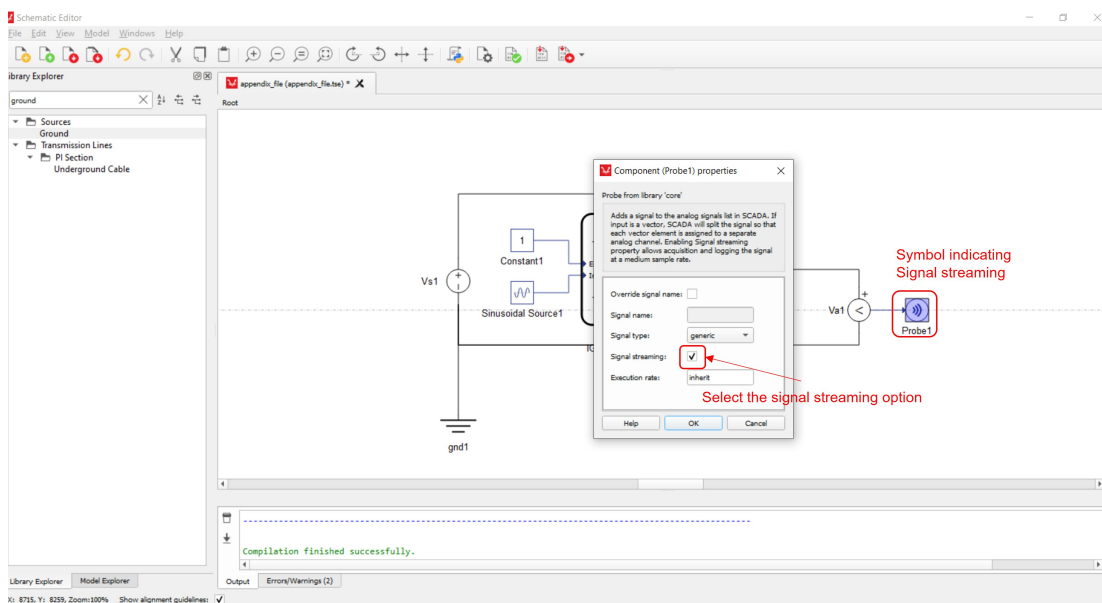


Figure A.13: Enabling Signal streaming

2. Run and compile the model
3. Once HIL SCADA is launched, add a signal stream widget in the panel file
4. Double click on the streaming widget to open the properties, and select the desired file location. For illustration, .csv format is selected .
5. Set the execution rate to $2 \mu\text{s}$ and add Probe 1 signal to analog signal list as shown in figure A.14.
6. Run the simulation, the streaming will start and continue to store data until the simulation is stopped.
7. Data gets stored at the desired location in csv format.

A.4. Changing the configuration of the device

The following steps can be used to change the configuration of the HIL device:

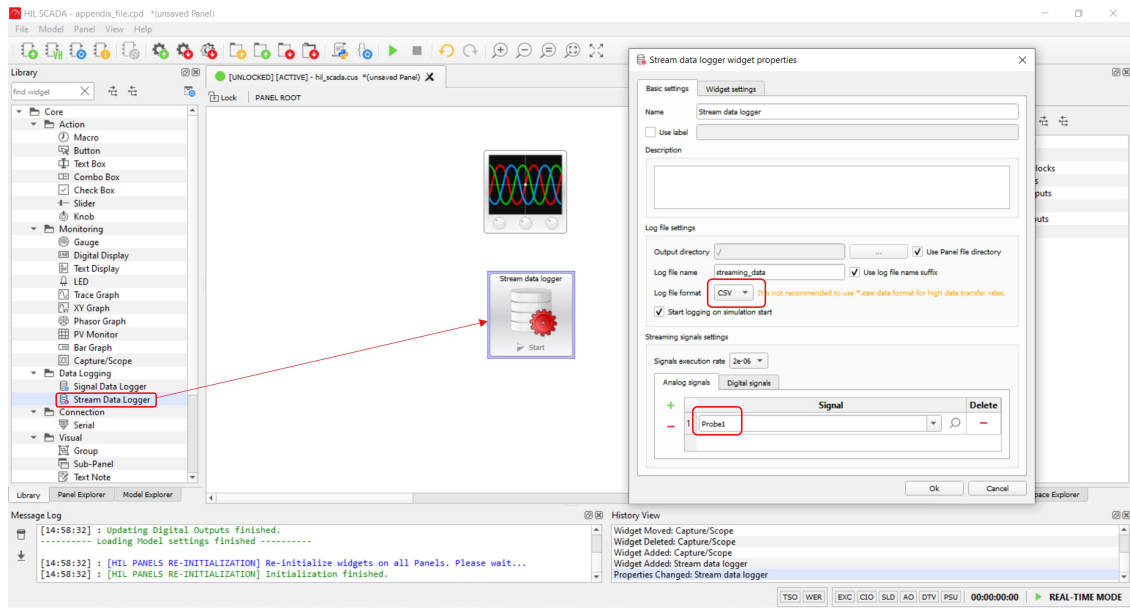


Figure A.14: Signal streaming widget settings

1. First make sure you are connected to your HIL device either through a USB or Ethernet port.
2. Open Typhoon HIL control center
3. Click on additional tools
4. Select the Firmware manager prompt as shown in figure A.15.

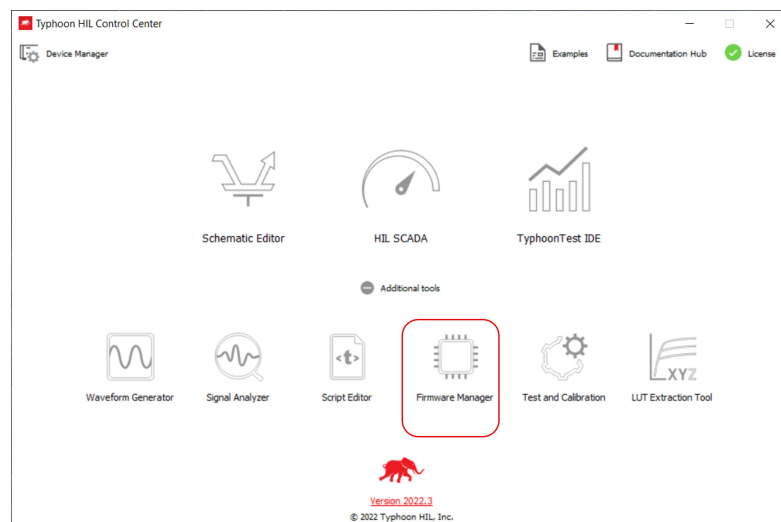


Figure A.15: Firmware Manager

- Next, click on the change configuration tab and select the new configuration. Click on change configuration as shown in figure A.16.

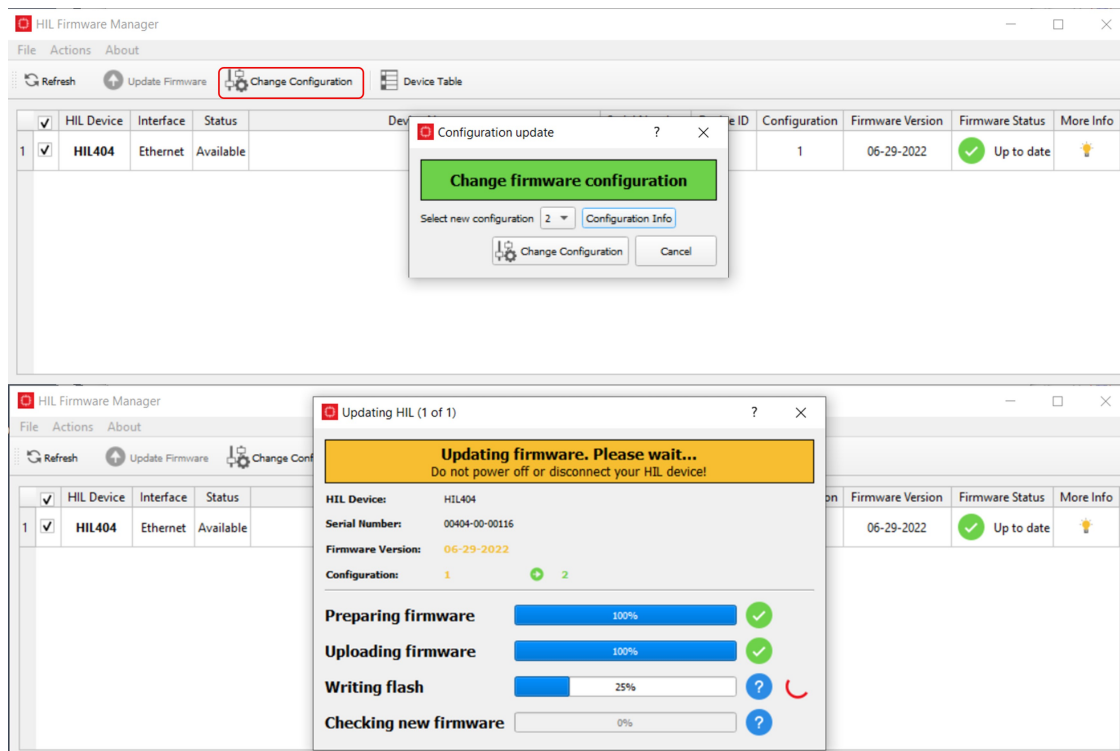


Figure A.16: Changing the device configuration

- Restart the HIL device

B

MMC Integrated Hybrid

B.1. Design of wave-shaping network

This section includes the MATLAB script to design the values of R_f and R_h based on values of load capacitance, additional capacitor, blocking condenser and MMC parameters.

```
%%-----  
mreq = 0.9; %Modulation Index  
freq = 50; %Frequency of the reference  
Vdc = 150; % Half of DC voltage  
No_submodules =2;  
  
Submodule_cap = 75e-6;  
L_arm_4 = 6e-3; % Arm Inductor  
R_arm_4 = 90; % Arm Resistor  
C_dc = 220e-6;%500e-9; % DC source capacitance  
  
C_load = 100e-9; %6.8*10^-6; %Load Capacitor  
R_load = 238;  
  
Rs_snubber = inf;  
Cs_snubber = inf;  
Ron = 1e-6;  
  
Vc_max = 1.2*((2*Vdc)/No_submodules);  
Vc_min = 0.8*((2*Vdc)/No_submodules);  
  
fPWM=50004; %Switching frequency  
TPWM = 1/fPWM;
```

Figure B.1: MMC parameter initialization

```

% Initialization of Impulse Generator
alpha1 = 14662.76;%3521.12; % %%%
alpha2 = 2.4691e6;%2.6246e6; % %%%
C11 = 220e-6;%220e-6;
C12= 500e-9; % Additional Condenser
C1= C11*C12/(C11+C12);
%C2 = 6.8e-6;
a = alpha1+alpha2;
b = alpha1*alpha2;

Cb = 1e-6; % Blocking condenser
C2= C_load*Cb/(Cb+C_load);
%C2=C_load;
Div =C2/C1;

ratio = a/b;
p = alpha1/alpha2;
q = alpha2-alpha1;

R1 = (1/(2*C1))*(ratio-sqrt(ratio^2-((4*(C2+C1))/(b*C2)))); %FR
R2 = (1/(2*(C1+C2)))*(ratio+sqrt(ratio^2-((4*(C2+C1))/(b*C2)))); % TR

```

Figure B.2: Design of R_f and R_h

B.2. Curve fitting using Polyfit command

The polyfit command in the thesis was used to obtain the coefficients of the polynomial of single degree to find the relation between the frequency information about the capacitor voltages in the input pulses to the HIL device.

```

%%-----
V =[50:25:300]; % Applied DC voltage
F =[104.539,103.491,102.476,101.412,100.386,99.341,98.296,97.249,96.212,95.158,94.103]; % Frequency of input pulse
n = 1; % degree of polynomial
p = polyfit(V,F,n);

```

Figure B.3: Polyfit command