High Voltage Wireless Power Transfer

Design and Prototyping of a DC Power Supply Based on Inductive Power Transfer

ET4300 : Master Thesis (5472482)

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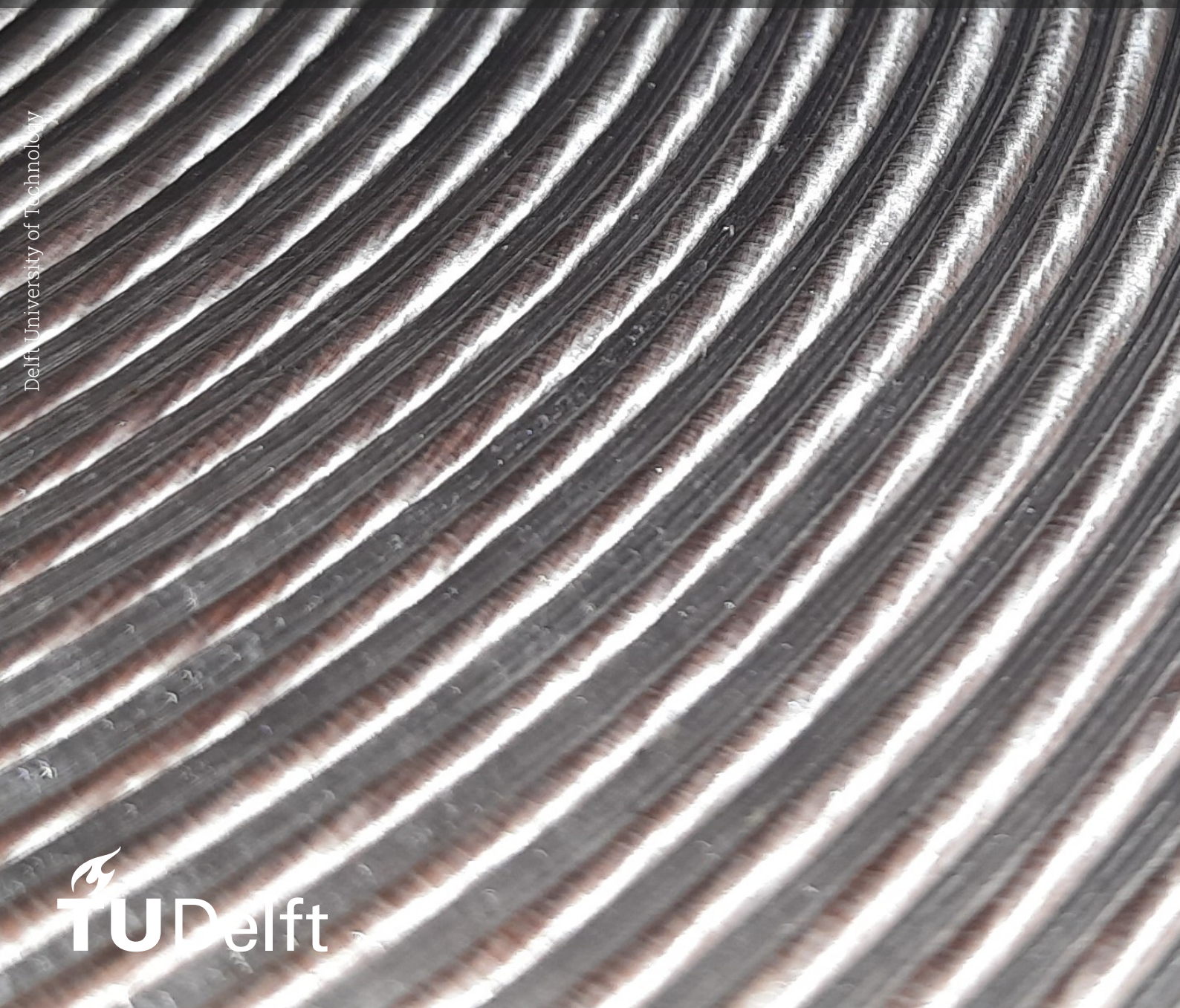

Delft University of Technology

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Design and Prototyping of a DC Power Supply Based on Inductive Power Transfer

by

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No man should escape our universities
without knowing how little he knows.

J. Robert Oppenheimer

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Suraj Jagannath Manur
Delft, August 2023

Abstract

The integration of renewable energy systems into the grid brings new and unique propositions involving the integration of power electronic inverter based solutions into the High Voltage (HV) grid. Thus a need arises to test the HV components with unconventional waveforms which can be satisfied by the Arbitrary Waveshape Generator (AWG). Two such topologies have been shortlisted for the AWG, ie: Modular Multilevel Converter (MMC) & Cascaded H Bridge (CHB). The MMC requires a single insulated DC source while the CHB requires multiple insulated DC sources with isolation.

Developing insulated DC sources using traditional transformers requires oil, epoxy or other complex insulation materials. The insulation requirements are further exacerbated when HV > 5 kV is required at power levels greater than 1 kW. For this reason, Wireless Power Transfer (WPT) methods are studied in this thesis to develop a DC Power Supply based on Inductive Power Transfer (IPT). The developed supply is capable of conducting DC breakdown tests and high frequency (>100 kHz) AC discharge tests on dielectrics.

The key requirements for developing such a system are Load Invariant Voltage, High Voltage Gain and Soft Switching. Considering these requirements the Series Parallel (S-P) topology is chosen to deliver 1.5 kW at a DC voltage of 5 kV from a 350 V input, with a diode rectifier. Using the Greinacher rectifier, 10 kV DC output is obtained. Different parameters of the developed resonant converter such as coupling coefficient, switching frequency, deadtime and overcurrent protection are analysed to find a suitable configuration for the DC Power Supply. An efficiency of 88% at rated load and load regulation of 18% is achieved for the developed power supply.

For the CHB, a multi-receiver IPT system is desirable to provide multiple isolated DC outputs. A 2-receiver and a 3-receiver IPT system is constructed and their coupling behaviour is studied. A conclusion is drawn that an ”n” receiver system has a coupling coefficient $k_n = \sqrt{n}k_1$ and accordingly a S-P IPT system can be developed to obtain multiple (n) isolated DC voltage sources.

Suraj Jagannath Manur
Delft, August 2023

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List of Abbreviations

AWG Arbitrary Waveshape Generator

MMC Modular Multilevel Converter

CHB Cascaded H Bridge

HV High Voltage

EMI Electromagnetic Interference

EMC Electromagnetic Compatibility

WPT Wireless Power Transfer

HVIPT High Voltage Inductive Power Transfer

DC Direct Current

IPT Inductive Power Transfer

CPT Capacitive Power Transfer

S-S Series Series

S-P Series Parallel

P-S Parallel Series

P-P Parallel Parallel

ZPA Zero Phase Angle

ZVS Zero Voltage Switching

ZCS Zero Current Switching

LIV Load Invariant Voltage

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Introduction

This chapter provides the motivation for designing a DC test source with Wireless Power Transfer. It begins with a brief regarding why different HV test sources are needed in an increasingly renewable energy based power electronic inverter dominated grid. Thereafter, the technologies of WPT and in particular IPT are discussed along with applications where they are used in research and industry. The amalgamation of the DC test source and IPT is what this thesis delves into. This chapter culminates by mentioning the goals, objectives and outline of this thesis.

1.1. Test Sources for a Power Electronic Dominated Grid

Shortage of resources, global warming, fossil fuel dependency are the buzzwords when it comes to any discussion regarding the energy system today. Around a century or two ago, the industrial revolution fueled the rise of engines and generators. Along with it came access to cheap fuel which eventually led to the growth of the AC grid. However, in the previous two decades, society has come to realise that a sustainable energy consumption pattern and better use of the available resources is the way to go forward. The prevailing situation has meant that electric power is viewed as the means of transition from a fossil-fuel-based society to a renewable-based one. This can be clearly seen in TenneT's Target Grid for 2045 where around 250 GW of electricity is expected to be used in the Netherlands and Northern Germany, which is more than double the energy use of today. [1]

Therefore, with the ever-increasing capacity of the grid along with the electrification of the energy mix and increase in renewable sources of energy, there is a need to make the present electric network more robust and interconnected [2]. A steady increase in power electronics based solutions in the grid is observed with the latest projects on offshore wind [3] and large solar parks [4] around the world. It is thus imperative to have the HV assets installed in the grid capable of handling the

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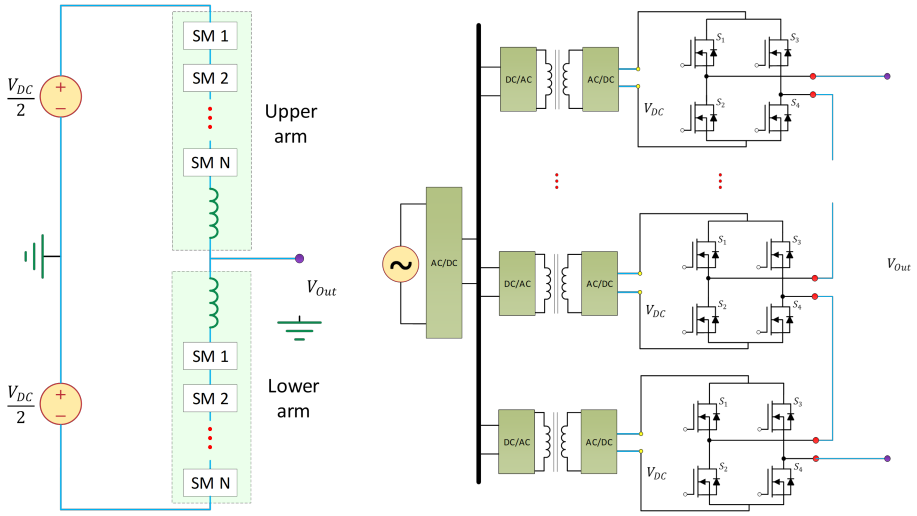
stresses arising from non-conventional sources of energy. These stresses can be in the form of DC, AC at 50 Hz, AC at higher frequencies and non-sinusoidal stresses. Therefore, the HV components must be tested for these conditions before being installed in the grid.



(a) Modular Multilevel Converter **(b)** Cascaded H Bridge

Figure 1.1: Topologies for the Arbitrary Waveform Generator (AWG)

The High Voltage Technologies Laboratory, at the TU Delft is developing an AWG for generating arbitrary waveshapes to test HV components. Two suitable topologies have been shortlisted for developing the AWG, ie: MMC and CHB. Fig 1.1a highlights that the MMC requires a single isolated DC source while Fig 1.1b shows that the CHB with n stages requires n isolated DC sources. It is important for the DC source to have insulation from the grid as the transients and distortions during tests must not affect the grid. Moreover, having multiple isolated DC sources are a must for the CHB. The DC sources currently used in the lab provide low power (< 500 W) at voltages of 20 kV and 40 kV [5]. These sources are large and can not be used to provide floating voltages. It is desirable to have these DC sources to provide HV at considerable powers higher than 1 kW. Therefore, the goal of this thesis is to develop a prototype test source with single and multiple isolated DC outputs for the MMC and the CHB respectively, capable of providing power higher than 1 kW at high voltages of 5 kV - 10 kV. With WPT the galvanic isolation required for the AWG is provided.

Alternatively, the single output of the HV WPT provides an AC voltage at high frequencies (> 50 kHz) which can be used to test surface discharge on dielectrics and other AC breakdown mechanisms at high frequencies. The single output of the HV WPT can also be used as a DC source to test the breakdown of air and other dielectrics.

1.2. Wireless Power Transfer

Dating back to the 1880's, coming from pioneers such as Hertz and Tesla [6], Wireless Power Transfer (WPT) is a technology that enables the transmission of electrical energy without the need for physical connections, which leads to galvanic isolation. These are broadly classified into 2 categories: ie: Near Field and Far Field power transfer [7]. As one might understand from the name, far-field power transfer refers to distances in the range of kilometres at high frequencies (10 MHz) and can only operate at very low powers due to ICNIRP exposure and safety limits [8]. Far-field power transfer is therefore usually used in microwave energy generation.

Near-field power transfer, on the other hand, refers to lower frequencies and the immediate space around the transmitter. This category of power transfer requires a study on the distance between the transmitter and receiver as the power transfer is dependent on the coupling between the transmitter and receiver [9]. Transmission distances in the near field power transfer are in the range of centimetres to a few meters. Near-field power transfer can be further divided into Capacitive Power Transfer (CPT) and Inductive Power Transfer (IPT) which can be seen as duals of each other [10].

CPT is the process of electrically coupling two metallic plates to transfer power. CPT as a technology is still premature and for the application of this thesis is not feasible as the high electric fields could have unintended consequences such as the breakdown of the medium between the metallic plates. CPT also requires higher switching frequencies and till now has been used majorly in low-power and short-range applications such as IoT devices, smart wearables and biomedical applications as seen in [11]. Another consideration is that CPT has lower power density than IPT when the air gap is in order of centimetres and is recommended to be used for smaller airgaps in the order of millimetres [12]. Therefore in this thesis, IPT will be used to transfer power.

1.3. Inductive Power Transfer

IPT involves magnetically coupling inductors to transfer power. An alternating magnetic field is created when alternating current passes through a coil. This alternating magnetic field is linked to any additional coil when placed close to the initial coil. Magnetic coupling between the coils is inversely proportional to the distance between them and is highly dependent on the alignment between the coils. The coupling coefficient described by the letter 'k' is indicative of the coupling between the two coils. Strong coupling is usually referred to when k is approaching 1 and is observed when a core is used to couple the coils or when the separation between the coil is very small (few millimetres) [10]. However, in an IPT system, the inductors are said to be "loosely coupled" as the core material is air and here a low coupling coefficient (k<0.5) is observed. As a result the WPT systems have a large leakage inductance and a relatively smaller mutual inductance. To improve the coupling and mitigate the effect of the leakage inductance, a compensation circuit primarily consisting of capacitors is designed. This configuration ends up forming a resonant circuit, which is known as magnetic resonant coupling. [13]

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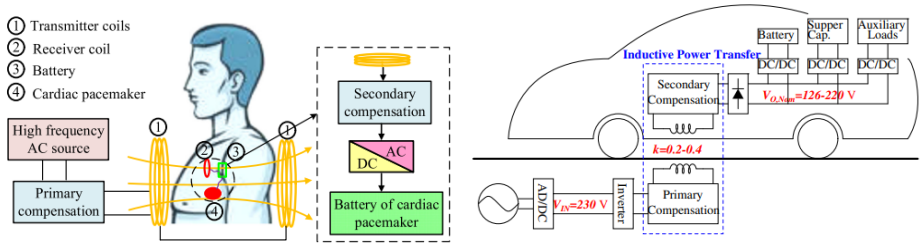
Magnetic resonant coupling circuits are therefore used to compensate for the leakages introduced by the low coupling coefficient. This magnetic resonance involves a multitude of methods of compensation which will be seen in Chapter 2. With this resonance, the IPT is able to operate at high efficiencies and provide design flexibility when it comes to the distance between coils and alignment. IPT with compensation behaves as a resonant converter and is thus used to transfer high powers efficiently in the orders of kilowatts [14] [15]. IPT is a mature technology [16] and has seen widespread adoption in a broad spectrum of domains. In [17], [18] magnetically coupled resonant circuits are used to power artificial hearts. For shorter distances, in the case of electronics charging [19],[20] highlights the use of strong magnetic coupling circuits. For longer distances and higher powers such as electric vehicle charging, compensation networks are used to enable high efficiency and flexibility [21], [22]. As seen from these examples [Fig 1.2], the use of WPT and specifically IPT is that air insulation makes a product very user-friendly.



(a) Biomedical Application [23] **(b)** EV charging Application [24]

Figure 1.2: Applications of IPT

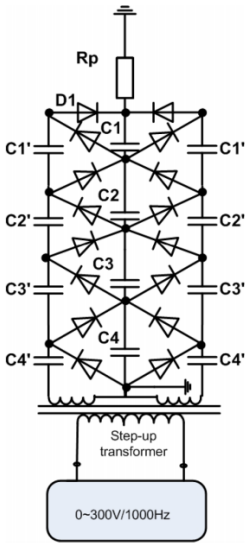
However, for a test source, insulation is a key requirement and IPT enables insulation. Using this as the premise and in a bid to eliminate the requirement of complex insulation for DC test sources, in this thesis, the IPT is investigated to create a high voltage gain suitable for powering the AWG and for testing applications.

1.4. An HV-based IPT system

High-voltage supplies are used for a variety of applications ranging from HV component testing, capacitor charging and hipot testing along with other general high-voltage applications [25] [26] [27]. Current DC power supplies (higher than 5kV) are moulded in silicon resin, dipped in oil or coated with epoxy to provide insulation between HV and the LV grid connection. The supplies also tend to be heavy, bulky and usually have a string of doubler stages which can be slow and sluggish in response as they operate at low switching frequencies. [28] [29].

Using IPT systems which come with inherent insulation across the coils, there is a possibility to create HV from the LV grid. The key requirement for such a system is to have high voltage gain across the coupling coils. Generally, IPT systems have similar primary and secondary inductances (1:1) where the input and output voltages are

(a) 17 stage HV multiplier - No insulation [28]



(b) HV supply with complex insulation [29]

Figure 1.3: DC test sources

in the same range. However, with a higher turn ratio, in this thesis the development of a **High Voltage Inductive Power Transfer (HVIPT)** is explored.

Narrowing down the scope and combining the motivation in Section 1.1 and Section 1.3, in this thesis a 10 kV DC power supply with Inductive Power Transfer (IPT) is developed. Considering input from the AC grid and an active PFC stage as a prerequisite, a 200-400 V DC Bus will be considered as the DC input for the HVIPT [Fig 2.1]. Accordingly, a feasible topology considering several factors in an IPT such as voltage gain, turns ratio, efficiency, coupling coefficient and power rating will be studied, simulated and developed as a test prototype. The AC output of the IPT system will then be rectified to provide the required DC output voltage. The supply thus developed can provide power to the MMC based AWG and also be used to conduct dielectric tests at high-frequency AC and DC.

However, for the CHB topology of the AWG, multiple isolated outputs from a single input are expected from the IPT system. For this application, in this thesis, a multiple receiver coils setup for the IPT is constructed and the coupling behaviour across these coils is studied.

1.5. Thesis Goals & Objectives

The aim of this thesis is to design a DC IPT system capable of powering the AWG while being capable of conducting AC and DC tests on dielectrics. The challenge involved in developing such a system is to obtain a high-voltage gain with sufficient

load regulation to operate efficiently at no-load and rated loads. Additionally, the supply must be capable of detecting short-circuit conditions during tests and turn itself off. Considering the above, the goal of this thesis is set to develop a 10 kV DC Power Supply using IPT which can be used to provide power up to 1.5 kW. Alternatively, a feasibility study of the IPT system, to provide multiple isolated DC outputs is also conducted in this thesis.

Accordingly, the following are the questions this thesis aims to answer

1. What are the possible topologies of IPT to achieve a high voltage gain suitable for the HVIPT?
2. What are the parametric tradeoffs involved in achieving a high voltage gain for the selected topology?
3. What are the design, prototype and testing considerations for such a supply?
4. What is the feasibility of a multi-coil output for the CHB AWG application?

1.6. Thesis Outline

The thesis addresses each of these research questions. The chapters of this thesis are summarised here.

- In Chapter **1**, an introduction to this thesis is provided where the motivation for the thesis is highlighted along with the thesis goals, objective and outline.
- In Chapter **2**, the IPT topology analysis is done based on the parametric requirements and a feasible topology is chosen for this thesis.
- In Chapter **3**, the selected topology is studied by developing a mathematical model which is then verified through simulations considering several test conditions that the supply is expected to face.
- In Chapter **4**, the process of developing the prototype is highlighted along with all the components involved in it.
- In Chapter **5**, the testing processes and results for the developed prototype are shown and their implications for an HVIPT are discussed.
- In Chapter **6**, the behaviour of multiple receivers for isolated DC outputs will be studied and an overview for designing multiple isolated outputs is provided.
- In Chapter **7**, the conclusions from the thesis are mentioned and certain recommendations are provided to make the HVIPT more suitable for testing applications.

2

Topology Analysis

This chapter provides a comprehensive analysis of the IPT topologies available for creating a high voltage gain and their suitability for the HVIPT. Several important parameters are initially listed, after which topologies from the literature are studied to see if they match the requirements for the desired supply. Finally, the use of the diode rectifier vis-à-vis the voltage multiplier for rectifying the HV AC to a HV DC output is studied. At the end of this chapter, a particular topology is chosen as the preferred topology for this thesis.

An IPT system comprises of an inverter, primary side compensation, primary coil, secondary coil, secondary side compensation, rectifier, output filter and the load [Fig **2.1**]. Typically, the input high-frequency inverter and the output HV high-frequency rectifier of the WPT system are full-bridge topologies. In this thesis, the load is the HV component intended to be tested.

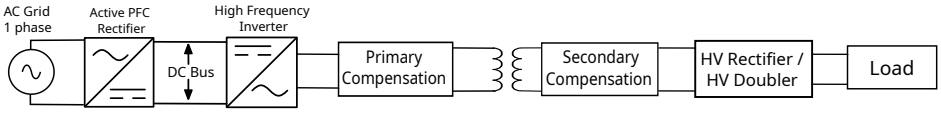


Figure 2.1: HVPS Layout

The main focus when it comes to an IPT is to design the compensation such that the required goals of a particular project are met. In this thesis, an air gap between the primary and secondary is imperative to provide HV insulation. The large air gap between the coils naturally brings with it galvanic isolation. Accompanying this isolation is a high leakage inductance and a considerably diminished magnetising inductance. Therefore, compensation networks are used on both sides of the magnetic coupling. These networks are connected in tandem with the respective coils and designed in such a way that the system resonates at the switching frequency

of the full bridge inverter while counteracting the reactive current induced by the leakage inductance, thereby providing a system with high efficiency.

The resulting topologies as a combination of different compensations are discussed in this chapter. They include single capacitor compensation shown in Section 2.2 or multiple component compensation shown in Section 2.3. The tradeoffs of each compensation topology with respect to designing and developing an HVIPT from a lower 200–400V DC input are studied. It must be noted that the DC input comes from an active boost PFC that is connected to the AC grid [Fig 2.1]. To simplify the prototype development and study the compensation topologies in this thesis, the DC input to the inverter is considered as the input supply.

2.1. Parameters Evaluation

Before delving into the compensation topologies and their impact on the IPT systems, it is imperative to know the several parameters based on which the compensation topologies are evaluated and the parameters that are crucial for the HVIPT. Knowing these parameters beforehand will help in evaluating each compensation topology for the development of the HVIPT. It is to be noted that the points mentioned below are not in any order of importance.

- **Load Invariant Voltage (LIV) :** As a power supply, it is desired to have a constant voltage as per the user's requirements, irrespective of the connected load. However, a maximum current limit exists for any supply, beyond which the system ceases to operate. The compensation topology must provide a voltage irrespective of the output load until a particular power level after which the system must switch off. In some IPT systems, using feedback, the switching frequency is varied to obtain the same output voltage at different loads [30]–[32]. This does not seem convenient especially when the secondary is at high voltage and such a feedback system can be complicated and expensive due to isolation requirements. Therefore, LIV is preferred as the output of the HVIPT.

- **Soft Switching :** In a power electronic inverter used for IPT applications, it is essential to have soft switching for the MOSFET's of the inverter [33]. Zero Phase Angle (ZPA) highlights the operating point where the current from the inverter and the voltage across the inverter have no phase difference; this indicates maximum power transfer as the input impedance seen from the inverter is totally resistive. For ZVS, however, a lag in input current is required for the following reason. For ZVS to occur in a MOSFET, the body diode of the blocking MOSFET must conduct before the junction of the MOSFET does. The reason is to discharge the drain-source capacitance of the blocking MOSFET and thereby prevent the turn-on losses of the MOSFET. The implication of operating in ZVS for a full-bridge inverter is that the input impedance of the resonant network should be inductive, albeit slightly. For the HVIPT, it must be ensured that the input current lags the input voltage, forming the essential ZVS soft switching condition for all MOSFET's in the inverter. If the

compensation topology does not accommodate ZVS, then severe reverse recovery losses in the MOSFET diode will occur, leading to high turn-on losses. This will lead to high switching losses and Electromagnetic Interference (EMI) problems [33].

Zero Current Switching (ZCS) is possible in IPT but from [33], it's shown that implementing the zero crossing of current is not straightforward. Moreover, the MOSFET's drain-source capacitors are not discharged in ZCS, again leading to high turn-on losses of the MOSFETs. On the other hand, ZVS occurs when the voltage across the switch is zero during the switching transition when a certain dead time is used to discharge the drain-source capacitor. Applying this dead time is straightforward in an open-loop setup. For the above reasons, ZCS is not preferred over ZVS for soft switching in the HVIPT to obtain higher efficiency and lower EMI.

- **High voltage gain :** As shown in Fig 2.1, the DC Bus for the IPT is around 200-400 V DC which is the result of the active PFC rectification from the grid. The goal of the HVIPT is to achieve 10 kV DC from the low voltage bus. There are two ways of achieving this in an IPT. Firstly, by just having a high turn ratio. Alternatively, a compensation topology could be there that provides a high gain as a result of the resonant circuit thus formed. This high gain must be in consideration with other parameters as well (ie: A high gain with low efficiency is not acceptable for the HVIPT). Usually, for HV component testing applications, a high voltage of >50 kV is expected. However, considering the scope of this thesis and the prototype being a proof of concept to also power the AWG, the goal is adjusted to providing a 10 kV DC output. Therefore, a gain of around 10-20 from the IPT is targeted in this thesis. This gain will provide around 4 kV - 6 kV as the AC output of the IPT, after which a Greinacher voltage multiplier is used to provide the desired DC output voltage. [34]

- **Minimal HV components:** The secondary side of the HVIPT will be operating at an AC HV above 5 kV. Therefore, the secondary compensation should have minimal components, as designing components for such high voltages is complex. For this reason, having an inductor for filtering or as part of the resonant circuit on the secondary is ruled out. Accordingly, the number of capacitors on the secondary side must be as minimal as possible.

- **Coupling Coefficient :** Also known as 'k' as shown in Eq.2.3, coupling coefficient is inversely proportional to the distance between the coils. Coupling coefficient indicates the strength with which the primary and secondary coils link with each other. Knowing the parameter gives information regarding the leakage and mutual inductances involved in the IPT setup. This parameter has no dependency on the topology chosen, but topologies behave differently in different coupling coefficient ranges and therefore it is an important parameter while evaluating topologies for the HVIPT. In the broader sense, in an IPT the coupling coefficient is usually in the range of 0.1-0.4. Generally, a

ferrite core is used to improve k of the air-cored coil systems [35]. However, with good compensation structures in certain topologies and use cases, there might not be a need to improve the coupling coefficient. Having a compensation topology that does not necessitate the ferrite core is an advantage from a cost and system point of view.

- **Efficiency :** Standard HV supplies usually operate at >85% efficiency at optimal load points. However, at non-optimal points, several supplies do drop their efficiency point to as low as 40% [5]. The HVIPT must also reach these efficiency points at least at optimal points to be seen as a feasible alternative. In IPT, the maximum theoretical efficiency depends on the coupling coefficient and the quality factor of the coils. However, to reach those efficiency points, the switching devices and the compensation topology must accommodate soft switching. In this thesis, the broader goal is to achieve an efficiency of >80%.

- **Operational Frequency :** IPT supply usually has a limit on the switching frequency which is based on the standards set by [8] for all purposes and SAE J2954, IEC 61980 for EV's. For the HVIPT, it is permitted to exploit the advantages of higher frequencies on the chosen topology. In a real-life implementation, this product can be encased, and therefore the Electromagnetic Compatibility (EMC) will be met for the surrounding environment. These supplies are used in safety cages where humans are considerably away from the supply. However, magnetic field studies for human exposure levels must be done on such systems to decide on the level of enclosure for the HVIPT.

- **No-load characteristics :** There are potential conditions where breakdown tests and corona-based tests are done with the HVIPT. In these tests, the load moves from a no load to a rated load condition. For these situations, the voltage must have good no-load characteristics such that the voltage remains the same even when no load is connected.

- **Short Circuit Protection :** Usually in power supplies, there are current limits that must be adhered to, above which the system provides the maximum current it can (aka CC mode). However, in the case of a short circuit, the supply must switch off and cease to send any power. The inverter intended to be used in an HVIPT must have these capabilities, where the inverter must switch off above the current limit set for that supply. The time taken to switch off the supply of power is also an important parameter that must be studied and noted, especially when tests involving a short circuit current are performed.

- **Feedback and Controllability :** Having LIV implies that variable current will be delivered by the supply to the load. Depending on the load point, the efficiency could vary based on the compensation topology used. There might be situations of air-gap variation and misalignment of the coils. Upon such parameters varying, the operating condition of the converter might change and this has to be detected and changes in the converter must be made to

manage the parametric variation. The compensation capacitors and coupling coils are usually fixed and therefore the system parameters such as switching frequency could be varied during situations such as misalignment or movement of the system. The IPT are usually tuned at a particular frequency and to control them there are in general 2 main methods frequency control and impedance matching [36] [37]. These control systems are put in place to maximise efficiency and enable a stable operating point at edge cases.

However, it must be considered that unlike dynamic charging applications [38] the HVIPT will be a static setup and is thus less prone to physical movements and variability in coil alignment and airgap variation. Thus with the HVIPT being a stationary system, feedback and control from the HV secondary is not considered in the thesis. Moreover, the peak efficiency of the system will be at an optimal load, apart from that load, the system will still operate at LIV albeit at a reduced efficiency. The goal of this thesis is to see if it is feasible to get a high voltage at a particular power level using IPT systems. The HVIPT is an open loop system which is why having good voltage controllability (LIV) is important. Therefore, the IPT must behave as a voltage source.

Several compensation topologies existing in the literature are studied in this chapter. Initially, the basic capacitive compensation topologies are introduced, and then the multi-component compensation topologies are explored for the HVIPT.

2.2. One component compensation

There are four basic network topologies which are implemented by placing capacitors in series or parallel to either of the primary and secondary coils as shown in Fig 2.2, with R_{ac} being the AC load. As the system is driven at resonant frequency, the primary compensation capacitor C_p minimizes the reactive power provided by the power supply, whereas the secondary compensation capacitor C_s maximizes the power transfer. This means that C_s is designed to resonate with the secondary inductor L_s which leads to Eq 2.1, that is irrespective of the compensation topology chosen for the IPT.

$$C_s = \frac{1}{\omega_0 L_s} \tag{2.1}$$

where ω_0 is the resonant frequency of the IPT system which also is the switching frequency of the inverter. C_p is obtained by minimising the equivalent input reactance for a particular topology which is shown in Table 2.1 [39]. Compensation at the primary influences the reactive power of the circuit, the VA rating of the input power source and the realization of soft switching [40]. The primary and secondary resonant frequencies are defined in Eq 2.2 which are irrespective of the compensation topology.

$$\omega_P = \frac{1}{\sqrt{L_P C_P}} \text{ and } \omega_S = \frac{1}{\sqrt{L_S C_S}} \tag{2.2}$$

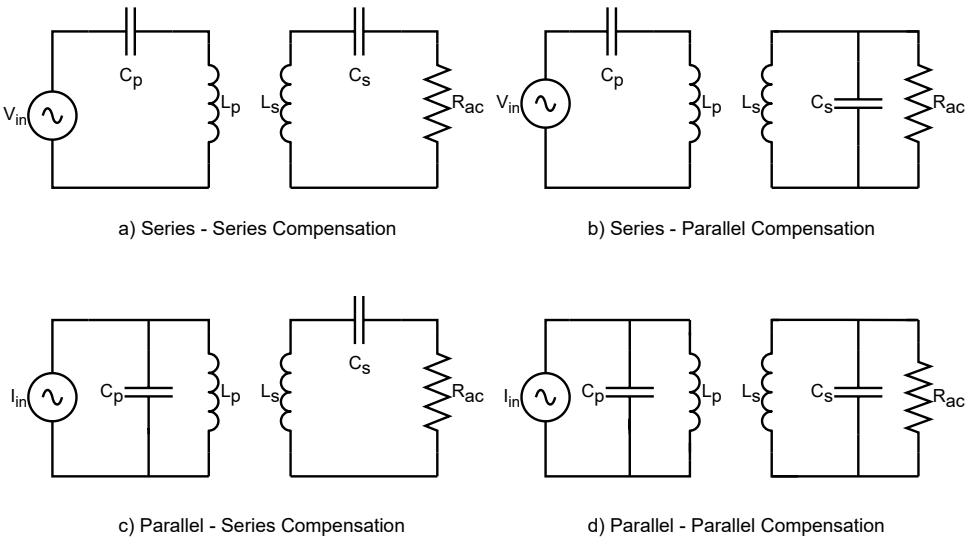


Figure 2.2: One Component Compensation Topologies

$$M = k\sqrt{L_p L_s} \tag{2.3}$$

The mutual inductance is given by Eq 2.3 where k is the coupling coefficient between L_p and L_s, which are the primary and secondary inductances respectively. As expected the increase in distance between the coils leads to the reduction of the coupling coefficient.

Table 2.1: Primary Compensation Capacitor

Topology	C_p
Series Series (S-S)	$\frac{1}{\omega_0^2 L_p}$
Series Parallel (S-P)	$\frac{1}{\omega_0^2 L_p - \frac{\omega_0^2 M^2}{L_s}}$
Parallel Series (P-S)	$\frac{L_p}{\omega_0^2 L_p^2 + \left(\frac{\omega_0^2 M^2}{R_{ac}}\right)^2}$
Parallel Parallel (P-P)	$\frac{L_p - \frac{M^2}{L_s}}{\omega_0^2\left(L_p - \frac{M^2}{L_s}\right)^2 + \left(\frac{R_{ac} M^2}{L_s^2}\right)^2}$

2.2.1. Primary Parallel Compensation

For the primary parallel resonant compensated topologies, an equivalent input current source is needed [Fig 2.2] [14]. The primary parallel compensation capacitor can not be directly connected to the output of a voltage source H-bridge inverter. Due to the difficulty of a power source in the form of a simple current source inverter, an extra inductor will be needed to transfer energy from a voltage source, incurring an extra component and complication in design and control. As shown in Table 2.1, primary compensation capacitor (C_p) depends on the load [39] [40]. Variation of load as expected in HVIPT will make tuning the primary parallel topologies impossible in an open loop setup. Therefore, primary series compensation will be used in this thesis and the P-S and P-P topologies are eliminated and will not be discussed further in this thesis.

2.2.2. Primary Series Compensation (S-S) & (S-P)

In a primary series compensated setup, a voltage source inverter must be used which is ideal for implementation. Having a series or parallel secondary compensation gives us different behaviour and their evaluation will be based on the parameters declared in Section 2.1.

In this section, the resistance of the coils will be ignored to avoid complexity. However, the quality factor of the coil is a key parameter for the efficiency of the IPT system and will be discussed later in this thesis. Both the S-S and S-P topologies are said to have high efficiencies of around 95% at the optimised load points [14].

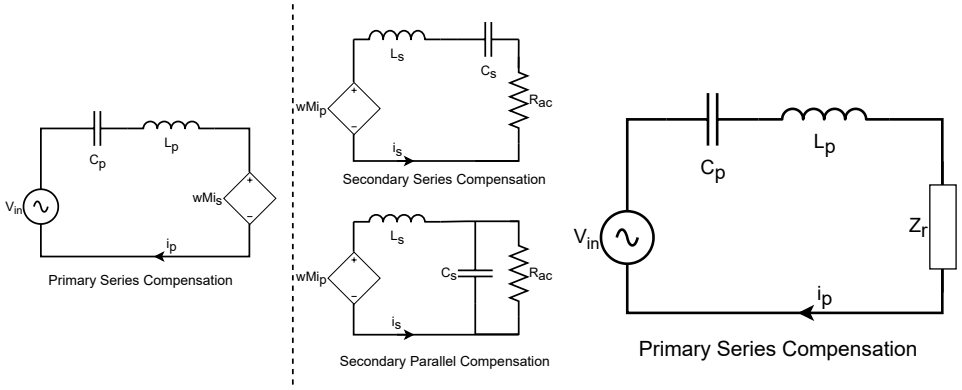
In Eq 2.4 the secondary impedances developed in S-S and S-P topologies are shown. The secondary impedance is then referred to the primary side following Eq 2.6. The secondary series compensation acts as a current source while the secondary parallel compensation behaves as a voltage source and this character of the topologies is shown in Eq 2.5 [41] [42].

$$Z_2 = \begin{cases} j\left(\omega L_s - \frac{1}{\omega C_s}\right) + R_{ac} & \text{secondary series compensation} \\ j\omega L_s + \frac{R_{ac}}{1+j\omega C_s R_{ac}} & \text{secondary parallel compensation} \end{cases} \tag{2.4}$$

$$R_{ac} = \begin{cases} \frac{8}{\pi^2} R_L = \frac{\frac{4}{\pi} V_{out}}{\frac{\pi}{2} I_{out}} & \text{secondary series compensation} \\ \frac{\pi^2}{8} R_L = \frac{\frac{\pi}{2} V_{out}}{\frac{4}{\pi} I_{out}} & \text{secondary parallel compensation} \end{cases} \tag{2.5}$$

The equivalent circuit with current dependent sources linking the primary and secondary of the IPT is shown in Fig 2.3a. For an easier understanding of input impedance, the circuit is converted into an equivalent impedance shown in Fig 2.3b. Eq 2.6 gives the relation between the two circuit diagrams in Fig 2.3.

$$Z_r = R_r + jX_r = \frac{\omega^2 M^2}{Z_2} \tag{2.6}$$



(a) Current Dependent Sources **(b)** Referred Impedance Z_r

Figure 2.3: Primary Series Compensation

Therefore, Eq 2.7 is the input impedance (load) for a primary series compensated IPT.

$$Z_{in} = \frac{1}{j\omega C_p} + j\omega L_p + Z_r \tag{2.7}$$

Table 2.2 has the referred resistance R_r and reactance X_r as seen by the high-frequency inverter. The S-P topology has considerable X_r, which is to be compensated by the primary capacitor. Since the S-S topology has zero X_r, the primary capacitor in this topology only compensates the primary inductance. Meanwhile, the secondary capacitor only compensates the secondary inductor in any primary series compensated system. Q_1 and Q_2 refer to the primary and secondary circuit quality factors [39].

Table 2.2: Referred Impedance (Eq 2.6) & Circuit Quality Factor [43]

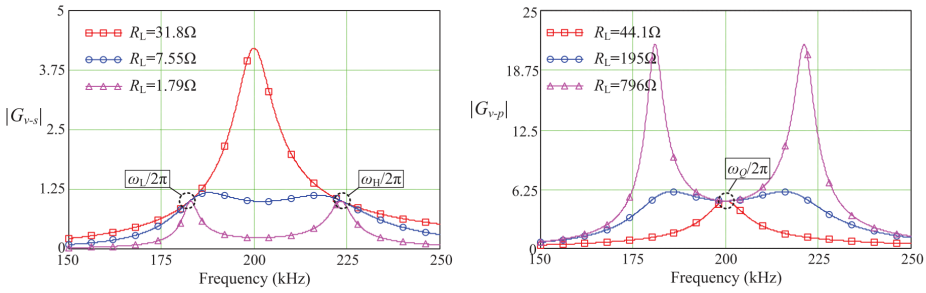
Secondary Compensation	R_r	X_r	Q_1	Q_2
Series	$\frac{\omega_0^2 M^2}{R_{ac}}$	0	$\frac{L_p R_{ac}}{\omega_0 M^2}$	$\frac{\omega_0 L_s}{R_{ac}}$
Parallel	$\frac{M^2 R_{ac}}{L_p^2}$	$-\frac{\omega_0 M^2}{L_s}$	$\frac{\omega_0 L_p L_s^2}{M^2 R_{ac}}$	$\frac{R_{ac}}{\omega_0 L_s}$

To compare the two topologies with the given parameters, operating points where the system can achieve both **load-invariant voltage** and **soft switching** are studied. The topology must also operate at **high efficiency** at least for the optimal load point. Moreover, obtaining a **high voltage gain** by virtue of the compensation topology will be highly beneficial for a HVIPT.

From Fig 2.4, the gain (V_o/V_{in}) bode plots for both primary series compensated

topologies are shown. In Fig 2.4a and 2.4b the switching frequency is 200 kHz while coupling coefficient is 0.2. The primary and secondary inductances are same with a value of 30 µH. As highlighted in Eq 2.1 and Table 2.1, the primary and secondary frequencies ω_P & ω_S are compensated accordingly. Based on the gain plot, it can be said that operating on ω_l or ω_h for S-S and ω_q for S-P will lead to load invariant voltage where the IPT shall behave as a voltage source. Therefore, for the secondary series compensation, the converter has two operating frequencies to realize the load-invariant voltage transfer ratio. For secondary parallel compensation, it has one operating frequency to realize the load-invariant voltage transfer ratio [44].

Another interesting observation is that for secondary parallel compensation, the voltage gain is around 5 while for secondary series compensation, the gain is unity for the conditions in [44]. Using these observations, the further 2 subsections will delve into the operating characteristics of the two secondary compensation topologies to analyse their feasibility for HVIPT.



(a) Series Series **(b)** Series Parallel

Figure 2.4: Bode Plots for Primary Series Compensation [44]

2.2.2.1. Series - Series Compensation

The S-S compensation behaves as a constant current source at the unique operating frequency ω_o [14]. It can be shown from Table 2.1 that C_p is independent of mutual inductance. From Table 2.1 and Eq 2.2 the following can be understood for S-S.

$$\omega_P = \omega_S = \omega_o \tag{2.8}$$

When the S-S topology is operating at Eq 2.8, ZPA occurs, where the input impedance seen by the voltage source inverter is resistive. Operating with ZVS, at this point the system provides the highest efficiency which is dependent on the resistances of the coil. The system efficiency is unity in an ideal case where the primary and secondary coil resistances (R_P & R_S) are ignored [45].

$$\eta_P = \frac{\Re\left(Z_r\right)}{R_P + \Re\left(Z_r\right)} \tag{2.9}$$

$$\eta_S = \frac{R_{ac}}{R_{ac} + R_S} \tag{2.10}$$

The transfer efficiency η_T is therefore given as

$$\eta_T = \eta_P \eta_S \tag{2.11}$$

The real component of the referred impedance is as stated below.

$$\Re\,(Z_r) = \frac{\omega^2 M^2 R}{R^2 + {X_S}^2} = \frac{\omega^2 k^2 L_P L_S R}{R^2 + {X_S}^2} \tag{2.12}$$

where $R = R_S + R_{ac}$ and $X_S = \omega L_S - \frac{1}{\omega C_S}$ [45]. However, the S-S provides a constant current as shown in Fig 2.5 where based on the load resistance, the system provides constant current and the voltage shoots up as we move to lighter loads (higher values of R_{ac}) which is expected for the HVIPT. During the no-load condition, the input impedance is zero and the input current does not reduce. This can be understood by studying equations 2.7, 2.8 and 2.12, that as R_{ac} tends to infinite (no load condition), Z_r and Z_{in} become zero in a perfectly compensated system. When input impedance Z_{in} is zero, then the input current will shoot up without any limit. Therefore, it is concluded that the S-S topology at ZPA behaves as a current source and is not suitable for the HVIPT.

From the gain equation (Eq 2.15) at the maximum efficiency point as shown by Eq.2.8, the gain ends up being $(R_{ac}/\omega_o M)$. It can therefore be concluded that for a particular input voltage, the voltage at the output increases as R_{ac} moves to the no-load condition. Therefore, operating the S-S topology at Eq 2.8 is not the suitable condition for the HVIPT. The G_v is directly proportional to R_{ac}, making it difficult to have good voltage regulation [36].

From Fig 2.4 there are 2 points where voltage controllability is good ie: ω_L and ω_H. Equations 2.13, 2.14 and 2.15 give an idea regarding the operating points in S-S topology with good voltage controllability. The gain of the system is derived using Fig 2.3. The output voltage is obtained in Eq 2.13. The input current is found by dividing the input voltage and input impedance of the S-S system in Eq 2.14. The input current is then substituted to find voltage gain in Eq 2.15 [46].

$$V_{\text{out}} = j\omega M \frac{R_{ac}}{Z_2} i_P = j\omega M i_P \frac{R_{ac}}{j\omega L_s - \frac{1}{j\omega C_s} + R_{ac}} \tag{2.13}$$

$$i_P = \frac{V_{\text{in}}}{Z_{in}} = \frac{V_{\text{in}}}{\frac{1}{j\omega C_p} + j\omega L_p + \frac{\omega^2 M^2}{Z_2}} = \frac{V_{\text{in}}}{\frac{1}{j\omega C_p} + j\omega L_p + \frac{\omega^2 M^2}{j\omega L_s - \frac{1}{j\omega C_s} + R_{ac}}} \tag{2.14}$$

$$G_v = \frac{V_{out}}{V_{in}} = \frac{j\omega M R_{ac}}{\left(j\omega L_p + \frac{1}{j\omega C_p}\right) Z_2 + \omega^2 M^2} \tag{2.15}$$

Upon eliminating R_{ac} from the gain Eq 2.15 we see two possible operating frequencies ω_l and ω_h as shown below. Further simplification is done with the assumption that primary and secondary resonant frequencies are the same ($\omega_p = \omega_s$) [31].

$$\omega_L = \sqrt{\frac{\omega_P^2 + \omega_S^2 - \sqrt{\left(\omega_P^2 + \omega_S^2\right)^2 - 4\left(1-k^2\right)\omega_P^2\omega_S^2}}{2\left(1-k^2\right)}} = \frac{\omega_s}{\sqrt{(1+k)}} \tag{2.16}$$

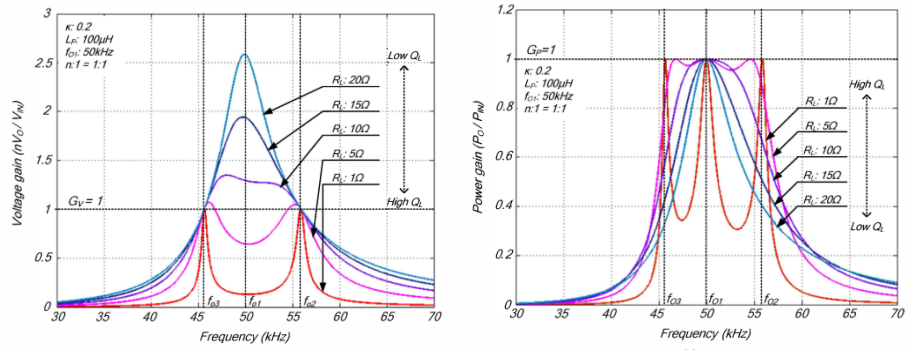
$$\omega_H = \sqrt{\frac{\omega_P^2 + \omega_S^2 + \sqrt{\left(\omega_P^2 + \omega_S^2\right)^2 - 4\left(1-k^2\right)\omega_P^2\omega_S^2}}{2\left(1-k^2\right)}} = \frac{\omega_s}{\sqrt{(1-k)}} \tag{2.17}$$

In either of the cases, the load invariant gain is shown in Eq 2.18 where n is the turns ratio between the primary and secondary coils. Therefore, a high turns ratio between the primary and secondary coils is the only way to obtain a high voltage gain in S-S topology.

$$G_v = \frac{V_{out}}{V_{in}} = \frac{\omega M}{\omega L_p - \frac{1}{\omega C_p}} = \sqrt{\frac{L_s}{L_p}} = n \tag{2.18}$$

Now it is known that at switching frequencies ω_l and ω_h the S-S system provides load invariant voltage. Operating at ω_h is suitable for H-bridge converters for its inductive input phase angle which allows the inverter to operate in ZVS [45].

It is shown in Fig 2.5b that upon varying the load quality factor to low values (high R_{ac}) the efficiency drops considerably from when compared to a high load quality factor where R_{ac} is very low [Table 2.2]. Also observable is the fact that while the quality factor improves, the unity efficiency point moves from a single sharp peak to a blunt peak and thereafter to a triple peak at ω_l, ω_o and ω_h [46]. Thus for high resistance (low load) applications, this mode of operation is not suitable as efficiency is heavily reliant on the load quality factor.



(a) Gain Plot **(b)** Efficiency Plot

Figure 2.5: Behaviour of S-S IPT system [46]

In Fig 2.5 the coupling coefficient is 0.2, the primary inductor L1 = 100 μH, unity turns ratio and inverter switching at 50 kHz. The conclusion drawn from this section is that the S-S topology does provide a switching frequency where the output voltage is constant and with soft switching (ZVS). However, this switching frequency does not have ZPA, the efficiency is load-dependent and the voltage gain is limited to the turns ratio n.

2.2.2.2. Series - Parallel Compensation

The S-P compensation is designed to have a constant voltage and the operating frequency is unique [Fig 2.4b]. From Table 2.2 the S-P does not have zero referred impedance, therefore the expression of C_p is different from the S-S topology as shown in Table 2.1. Upon further simplification, the below Eq 2.8 holds good for this topology.

$$\frac{\omega_P}{\sqrt{1-k^2}} = \omega_S = \omega_o \tag{2.19}$$

It is shown from Table 2.1 that C_p is dependent on mutual inductance, implying that variation of the coupling coefficient changes C_p. This is a disadvantage during dynamic situations such as coil movement and misalignment, however, in the HVIPT the coils will be stationary at a particular distance and with perfect alignment. This dependence is also an advantage when the secondary coil is absent, or the light load condition occurs, the primary side gets detuned and the total impedance seen by the source is high and not zero, unlike the S-S topology. Therefore, the primary current does not increase to a high value limited by source capability and resistances of the coil and the inverter, on the other hand, it reduces to a minimum circulating current as shown in Fig 2.4b. Thus, SP topology is safer than SS topology in no-load conditions, while providing load-invariant voltage.

$$V_{\text{out}} = j\omega M i_P \frac{\frac{R_{ac}}{1+j\omega C_s R_{ac}}}{Z_2} = \omega M i_P \frac{\frac{R_{ac}}{1+j\omega C_s R_{ac}}}{j\omega L_s + \frac{R_{ac}}{1+j\omega C_s R_{ac}}} \tag{2.20}$$

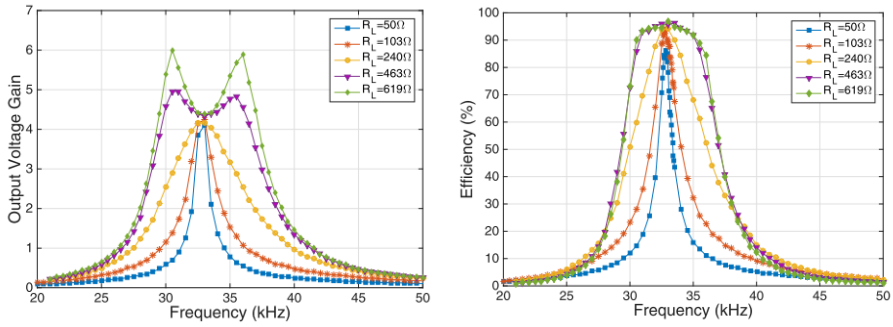
$$i_P = \frac{V_{\text{in}}}{Z_{in}} = \frac{V_{\text{in}}}{\frac{1}{j\omega C_p} + j\omega L_p + \frac{\omega^2 M^2}{Z_2}} = \frac{V_{\text{in}}}{\frac{1}{j\omega C_p} + j\omega L_p + \frac{\omega^2 M^2}{j\omega L_s + \frac{R_{ac}}{1+j\omega C_S R_{ac}}}} \tag{2.21}$$

$$G_v = \frac{V_{out}}{V_{in}} = \frac{j\omega M \frac{R_{ac}}{1+j\omega C_s R_{ac}}}{\left(j\omega L_p + \frac{1}{j\omega C_p}\right) Z_2 + \omega^2 M^2} \tag{2.22}$$

Similar to the previous section, the voltage gain Eq 2.22 is derived from Eq 2.21 and Eq 2.20. Plugging in Eq 2.19 into Eq 2.22 leads to the voltage gain highlighted in Eq 2.23 [44]. This is promising for the HVIPT because, with longer distances between the coil, the coupling coefficient does reduce and therefore combining this with the additional turns ratio between the primary and secondary coil, one can achieve a high voltage gain in the order of 10-20 as stated in Section 2.1. This also means in general cases for a particular output voltage the S-P topology requires lesser dc-link voltage compared with the S-S topology. The tradeoff for obtaining a high voltage gain is the increase in circulating current in the secondary coil and capacitor as the coupling coefficient is reduced. This tradeoff will be studied later in this thesis.

$$G_v = \frac{1}{k}\sqrt{\frac{L_s}{L_p}} = \frac{n}{k} \tag{2.23}$$

In Fig 2.6 the operating conditions are k = 0.2, L1 = 500 µH, turns ratio 0.8 and 33 kHz switching frequency [47]. A constant voltage irrespective of the load is shown in Fig 2.6a with efficiencies to the north of 90% in Fig 2.6b. However, as the voltage gain is constant, the output power is determined by load resistance, which means output power fluctuates when the load resistance is varied [47].



(a) Gain **(b)** Efficiency

Figure 2.6: Behaviour of S-P IPT system [47]

Operating at the switching frequency shown in Eq 2.19 gives the best efficiency and is unity in the ideal case. In a realistic scenario where the coils have a particular coil resistance, the system efficiency is dependent on parameters shown in Eq 2.24, Eq 2.25 and Eq 2.26.

$$\eta_P = \frac{\Re\left(Z_{in}\right)}{R_P + \Re\left(Z_{in}\right)} \tag{2.24}$$

$$\eta_S = \frac{\Re\left(\frac{R_{ac}}{1+j\omega C_S R_{ac}}\right)}{\Re\left(\frac{R_{ac}}{1+j\omega C_S R_{ac}}\right) + R_S} \tag{2.25}$$

$$\eta_T = \eta_P \cdot \eta_S \tag{2.26}$$

From the equations above and Fig 2.6 it can be concluded that the S-P is a suitable prospective topology and therefore it will be explored in detail in the upcoming chapters.

2.3. Multiple component compensation

The need to explore multiple component compensation techniques arises from the fact that neither of the basic one component compensation topologies have freedom of design from the mutual inductance. This implies that upon varying the distance between the coils, the coupling coefficient and the mutual inductance vary. Therefore, the compensation capacitors or frequencies have to be changed to obtain resonance. WPT systems offer high spatial freedom of the coils, meaning the air-gap variation and misalignment of the transmitting and receiving coils are possible. Usually, the resonant frequency of the primary and secondary resonant tanks change when the coupling coefficient change. With traditional one-order compensation topologies, to achieve high efficiency, a tuning method is needed to maintain the resonance when the air gap changes or misalignment happens. The load-invariant voltage output with ZPA input is required for the HVIPT for expected performance, but this is reliant on the parameters of the loosely coupled transformer, which are fixed in one component compensation topologies [48]. Therefore, this section explores the multiple component compensation topologies in literature which give more design flexibility. Their feasibility for the HVIPT will be studied and in the end, a conclusion will be drawn if any of the listed topologies are suitable for the HVIPT based on the parameters mentioned in Section 2.1.

2.3.1. LC Compensation

In the previous section, the primary parallel compensated topology was discarded as it requires a current source input. To eliminate this requirement, an inductor can be used in series to the high-frequency resonant circuit leading to LC compensation. The converter with the LC compensation topology is called the LCL converter with the second L being the coupling inductor. The LC compensation topology is usually double-sided, symmetrical and thus suitable for bidirectional power transfer. The

LCL converter is robust as the input current is independent of load [49]. However, the converter has no flexibility on the parameters selected based on the coils and their orientation. Here are two advantages for the LCL converter when the system operates at the resonant frequency. Firstly, only the active power required by the load is supplied by the inverter; secondly, the input current is independent of the load condition. However, the compensation inductor has a value in the order of coupling coils [50]. This can be complex to design for HV and the whole purpose of the HVIPT with well insulated coils and inductors is lost in this case.

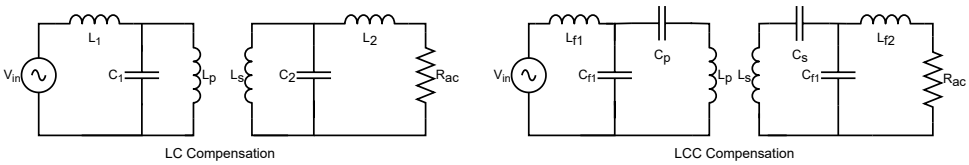


Figure 2.7: LC & LCC compensation topologies

2.3.2. LCC Compensation

The LC compensation topology has an input current dependency on the mutual inductance of the coupling coils. To eliminate this dependency, the LCC compensation topology exists in the literature. There are single-sided LCC compensation networks but their voltage gain is dependent on the coupling coefficient and on the inductors involved, not giving a significant advantage over the single-order compensation topologies. On the other hand, double-sided LCC networks provide significant freedom of input current with respect to coil coupling [51]. The resonant frequency in this compensation topology is independent of the coupling coefficient and the load condition. When LCC compensation network is adopted at the secondary, reactive power at the secondary is compensated to form a unit input power factor. The so-formed IPT system can work at a constant frequency, which eases the control required. The LCC compensation topology is designed for a WPT system with multiple loads and dynamic coil conditions [13]. For the whole range of coupling and load conditions, high efficiency for the IPT system is achieved. This topology is suitable and designed for an environment where the coupling coefficient keeps changing, such as the electric vehicle charging application. Due to the symmetrical structure, the double-sided LCC can be used in a bidirectional system [13].

To attain ZVS however, a complex design of the secondary coil and the secondary inductor is required. This is the HV side for the HVIPT and the inductor design is therefore undesired for the HV side. Also, the gain is still equivalent to the turns ratio and not any more as opposed to the S-P. Moreover, the HVIPT is operating in a static environment and power flows unidirectionally. Therefore the advantages of the double-sided LCC compensation do not really match the requirements of the HVIPT.

2.3.3. S-SP Compensation

The load-invariant voltage gain and input current of the S-S and the S-P IPT converter are dependent on transformer parameters and can get affected considerably due to misalignment and variation in coupling coefficient. The LC and LCC topologies use extra inductors to obtain the flexibility of the coil parameters and achieve the desired output. However, the extra inductor is not preferred from a HV insulation and efficiency point of view.

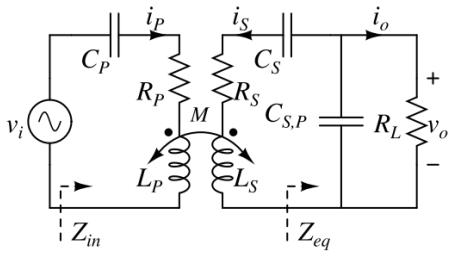


Figure 2.8: Series Series/Parallel Topology

In [52],[53] a new topology called the series series/parallel has been introduced as shown in Fig 2.8, where the goal is to compensate the leakage inductances by the series capacitors on either side and to compensate the magnetising inductance with the parallel capacitor leading to the following equation.

$$\frac{1}{(1-k)L_P C_P} = \frac{1}{(1-k)L_S C_S} = \frac{1}{n^2 k L_P C_{S,P}} = \omega_o^2 \tag{2.27}$$

This leads to the output gain at this resonant frequency being equal to the transformer turns ratio 'n' which is independent of load change and the transformer's coupling coefficient. Also, ZPA is achieved which allows the system to operate at soft switching with ZVS. The input impedance at ω_o is R_L/n^2 and is free of all transformer parameters. It must be noted that the circulating current will increase for the same terminal parameters as the coupling coefficient or mutual inductance reduces. Output gain at the resonant frequency ω_o is equal to the transformer's turn ratio (n) which is independent of load change and coupling coefficient [48]. For the HVIPT however, this mode of the S/SP is not sufficient as the gain is turns ratio (n) while in S-P there is a significant advantage in voltage gain with the reduction in coupling coefficient. Moreover, the output gain can not be varied unless the coils themselves are changed in this topology.

In [48] there is a promising solution with the same series series/parallel compensation topology where a single design factor **μ** is introduced [Eq 2.28]. The idea primarily comes by having different resonant frequencies for the primary and secondary circuit. The operational switching frequency (ω_H) of the inverter is seen in Eq 2.32.

$$\mu = \frac{\omega_P}{\omega_S} \tag{2.28}$$

This configuration of the series series/parallel topology gives a higher gain which can be controlled by the factor μ, shown in Eq 2.29.

$$E = \frac{v_o}{v_i} = \frac{jX_M}{jX_P + \frac{X_M^2 - X_P X_S}{Z_{\text{eq}}}} \tag{2.29}$$

where $X_P = \omega L_P - \frac{1}{\omega C_P}, X_S = \omega L_S - \frac{1}{\omega C_S}, X_M = \omega M$ and $Z_{\text{eq}} = \frac{1}{j\omega C_{S,P} + \frac{1}{R_L}}$ are the impedances shown in Eq. 2.29. The condition to obtain LIV output is shown in Eq 2.30.

$$\omega^2 M^2 - X_P X_S = 0. \tag{2.30}$$

Solving the above two equations, the E_{LIV} and its operating frequency ω_H are given by Eq 2.31 and Eq 2.32 respectively

$$E_{\text{LIV}} = \sqrt{\frac{L_S}{L_P}} \frac{k\left(\mu^2 + 1 + \Delta\right)}{\left(2k^2 - 1\right)\mu^2 + 1 + \Delta}, \tag{2.31}$$

$$\omega_H = \omega_S \sqrt{\frac{\mu^2 + 1 + \Delta}{2\left(1 - k^2\right)}} \approx \frac{\mu}{\sqrt{1 - k^2}} \omega_S, \text{ when } \left(\mu^2 - 1\right)^2 \gg 4k^2\mu^2 \tag{2.32}$$

here, ω_L is ignored due to a lack of an inductive phase angle and ZVS. To find $C_{S,P}$ the input impedance (Z_{in}) must be made purely resistive.

$$Z_{\text{in}} = jX_P + \frac{\omega^2 M^2}{jX_S + Z_{\text{eq}}} \tag{2.33}$$

which is satisfied by

$$C_{S,P} = \frac{C_S}{\frac{\omega_H^2}{\omega_S^2} - 1} \tag{2.34}$$

Varying k and μ gives varying gain points and combining with it the high turns ratio, a desirable high gain can be achieved as shown in Fig 2.9. Therefore, the μ factor-based S-SP topology is a promising solution which gives more design flexibility with respect to voltage gain (E_{LIV}) than the S-P topology, this obviously comes with a tradeoff that increasing the gain by just varying μ and reducing k would lead to increased amounts of circulating currents and reduced efficiency. Moreover, an extra HV capacitor is being introduced in this topology as compared to the S-P topology.

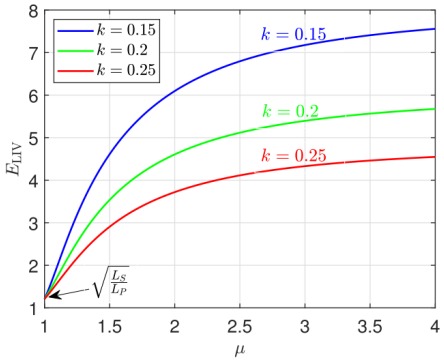


Figure 2.9: Gain of the μ factor-based S-S/P topology [48]

2.4. Diode Rectifier and Voltage Multiplier

After choosing a particular compensation topology for the HVIPT, an HV AC output is obtained at the output of the IPT. Now a suitable rectifying setup must be chosen to rectify this AC output and obtain a constant DC output.

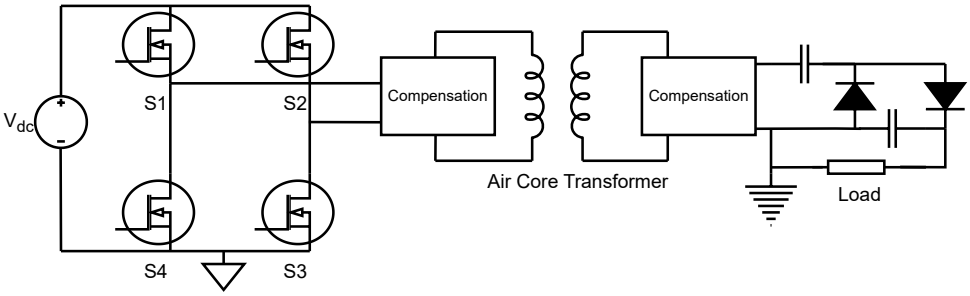


Figure 2.10: IPT Layout - Doubler

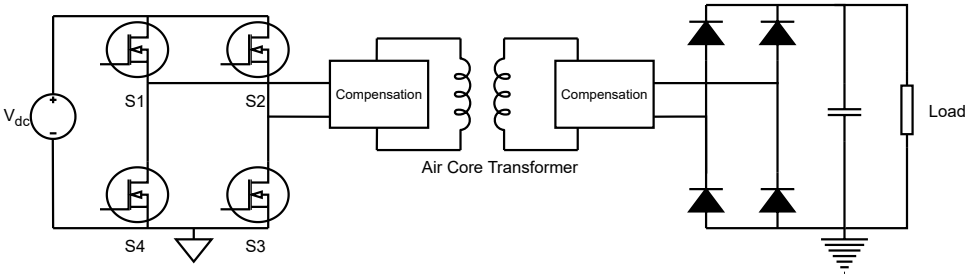


Figure 2.11: IPT Layout - Rectifier

Generally, a diode rectifier as shown in Fig 2.11 is used in EV or biomedical

applications. For the HVIPT, high voltages are desired albeit at low power levels and for such conditions using the Greinacher voltage multiplier [34] as shown in Fig 2.10 is an option. This gives a higher DC output voltage at the same power level which is ideal for a DC test supply. Multiple stages of the doubler can get bulky, slow and have a large voltage ripple. However, multipliers in current HV sources operate at much lower frequencies [29] while here in the HVIPT the switching frequency will be in the order of several 100's of kHz. Nevertheless, to prove the working of a high-voltage gain with greater than unity turn ratio, in this thesis, both the diode rectifier and the voltage doubler will be developed and tested. The compensation topology which is suitable for this application must behave as a constant voltage source providing input to the multiplier circuit or diode rectifier [34]. To obtain 10 kV with a gain of 10-20 from the 200-400V DC Bus input there is a need for a multiplier stage. Therefore an output AC voltage of around 4-6kV is expected from the compensation topology.

2.5. Suitable Topology

Going through various single and multi component compensation topologies, the suitable topology for this thesis is the S-P or the μ factor-based S-SP. The parallel primary single-order circuits are eliminated due to a current source requirement. Multi-order topologies involving a secondary inductor are not an option considering the HV across the inductor and the design complexity involved with them. The S-S does not offer the most efficient point as a voltage source output and while there are operating frequencies where it behaves as a voltage source, they are load quality factor dependent. Moreover, they do not provide the high-voltage gain as an inverse relation to the coupling coefficient that the S-P or the μ factor-based S-SP provides.

Table 2.3: Parametric qualification of topologies

Parameters	**S-S**	**S-P**	**P-S**	**P-P**	**LC**	**LCC**	**S-SP**
Load Invariant Voltage	✓	✓	✗	✗	✓	✓	✓
High Voltage Gain	✗	✓	✗	✗	✗	✓	✓
ZVS	✓	✓	✗	✗	✓	✓	✓
No load condition	✗	✓	✗	✗	✓	✓	✓
Minimal HV components	✓	✓	✓	✓	✗	✗	✗
Coupling Coefficient	Independent of topology						
Switching Frequency	Independent of topology						
Efficiency	✗	✓	✗	✗	✓	✓	✓
Short Circuit Protection	Provided by the H-Bridge Inverter						
Feedback & Controllability	Open Loop System						

While both S-P or the μ factor-based S-SP topologies are suitable for the HVIPT in this thesis it is chosen to go with the S-P for 2 main reasons. Firstly, S-SP has an extra component at the HV side. Secondly, μ factor-based S-SP offers additional advantages by varying μ such as obtaining different voltage gains which help in dy-

namic situations, providing easier control strategies. For the HVIPT, a static setup with a particular operating point, a fixed coupling coefficient and gain is preferred with the goal being to get a constant DC output that can be easily controlled by choosing the required input voltage based on a fixed gain for the overall system.

In this chapter the parameters suitable for the HVIPT are highlighted of which Load Invariant Voltage, High Voltage Gain and Soft Switching are of higher weight. Upon analysing several compensation topologies, the S-P and the μ factor-based S-SP seem suitable. However, considering the simplicity required in designing a fixed supply the S-P topology is the chosen topology for this thesis.

3

Series - Parallel Topology

This chapter highlights the suitable characteristics of the Series Parallel Topology for the HVIPT. Further evaluation and analysis of the S-P topology is done using simulations and a mathematical model. Parametric evaluation of the topology for obtaining a high gain with a non-unity turns ratio is done in this chapter, which is followed by a study on the existence of zero phase angle for all operating conditions along with efficiency analysis. The chapter ends with simulations of the system with a diode rectifier and a voltage multiplier.

3.1. Introduction

As concluded in the previous chapter, the Series Parallel topology meets most of the requirements for the HVIPT and is the topology going to be used in this thesis. Amongst the parameters mentioned Table 2.3 the **Load Invariant Voltage**, **Soft Switching**, **High Voltage Gain**, **No Load Characteristics** are met by the S-P topology while maintaining high **efficiency** [47] [54]. In this chapter, characteristics of this compensation topology will be studied and the parametric considerations of using this topology for the HVIPT will be discussed.

For studying any IPT system, the most important components are the primary and secondary coils. There are multiple ways of modelling them but here the focus is on the two general methods, the T model and M model as seen in Fig 3.1 and Fig 3.2 respectively.

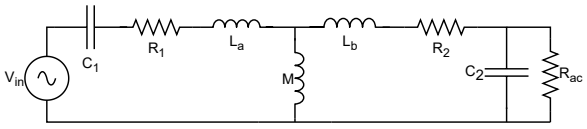


Figure 3.1: T Model

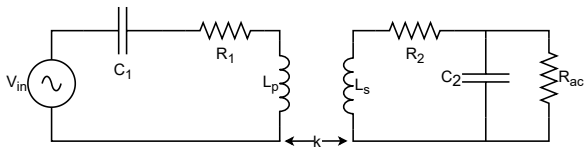


Figure 3.2: M Model

Here R_1 and R_2 are the parasitic resistances of the primary and secondary coils respectively. The M model can be converted to the T model with the following equations :

$$L_s = n^2 L_p \tag{3.1}$$

$$M = k\sqrt{L_p L_s} = nkL_p \tag{3.2}$$

$$L_a = L_p - M = L_p - nkL_p = L_p(1 - nk) \tag{3.3}$$

$$L_b = L_s - M = L_s - kL_s/n = L_s(1 - k/n) \tag{3.4}$$

To achieve resonance with the highest efficiency and have zero component of the reactive input impedance with perfect compensation, these values of C_p and C_s from the following equations must be used :

$$C_p = \frac{1}{\omega_o^2(L_p - M^2/L_s)} = \frac{1}{\omega_o^2 L_p(1 - k^2)} \tag{3.5}$$

$$C_s = \frac{1}{\omega_o^2 L_s} \tag{3.6}$$

3.2. Load Invariant Voltage

To derive and understand this characteristic property of the S-P topology, the circuit must be analysed using current-controlled voltage sources linking the primary and secondary coils as seen in Fig 3.3.

$$Z_p = R_p + j\omega L_p + \frac{1}{j\omega C_p} \tag{3.7}$$

$$Z_s = R_s + j\omega L_s + R_{ac} // \left(\frac{1}{j\omega C_s}\right) = R_s + j\omega L_s + Z_{eq} \tag{3.8}$$

$$Z_{eq} = R_{ac} // \left(\frac{1}{j\omega C_s}\right) = \frac{R_{ac}}{1 + j\omega C_s R_{ac}} \tag{3.9}$$

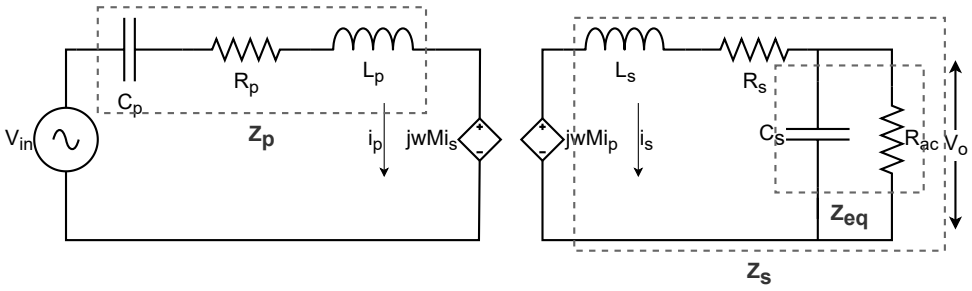


Figure 3.3: S-P with current controlled voltage sources

Equations 3.7, 3.8 and 3.9 refer to the impedances shown in Fig 3.3. These impedances will be used to derive the voltage gain shown in Eq 3.17. It can be seen that no-load regulation is possible as the gain is load independent and the system behaves as a voltage source.

The output voltage and input voltages are obtained using Kirchhoff's Voltage Law and their ratio is the voltage gain of the IPT.

$$V_{\mathrm{o}} = j\omega M i_P \frac{Z_{eq}}{Z_s} \tag{3.10}$$

$$V_{\mathrm{in}} = i_P(Z_p + j\omega M\frac{i_s}{i_p}) = i_P(Z_p + j\frac{\omega^2 M^2}{Z_s}) = i_P\frac{Z_p Z_s + \omega^2 M^2}{Z_s} \tag{3.11}$$

$$i_s Z_s = j i_p \omega M \tag{3.12}$$

$$\frac{V_o}{V_{in}} = \frac{j\omega M Z_{eq}}{Z_p Z_s + \omega^2 M^2} = \frac{j\omega M Z_{eq}}{Z_p(j\omega L_s + Z_{eq}) + \omega^2 M^2} = \frac{j\omega M}{Z_p + \frac{Z_p j\omega L_s + \omega^2 M^2}{Z_{eq}}} \tag{3.13}$$

The second term in the denominator of Eq 3.13 is the only term involving the load resistance (Z_{eq}) and on eliminating Z_{eq}, the gain transfer function is independent of the load.

$$(\omega L_p - \frac{1}{\omega C_p})(\omega L_s) = -Z_p j\omega L_s = \omega^2 M^2 = \omega^2 k^2 L_p L_s \tag{3.14}$$

$$\omega L_p(1 - k^2) = \frac{1}{\omega C_p} \tag{3.15}$$

Which gives the below operating frequency ω_o

$$\omega_0 = \frac{\omega_p}{\sqrt{1 - k^2}} = \omega_s \tag{3.16}$$

Therefore upon eliminating the load-dependent term, the gain of the system reduces to Eq 3.17.

$$G(\omega_0) = \frac{V_o}{V_{in}} = \frac{j\omega_0 M}{Z_p} = \frac{\omega_0 M}{\omega_0 L_p - \frac{1}{\omega_0 C_p}} = \frac{1}{k}\sqrt{\frac{L_s}{L_p}} = \frac{n}{k} \tag{3.17}$$

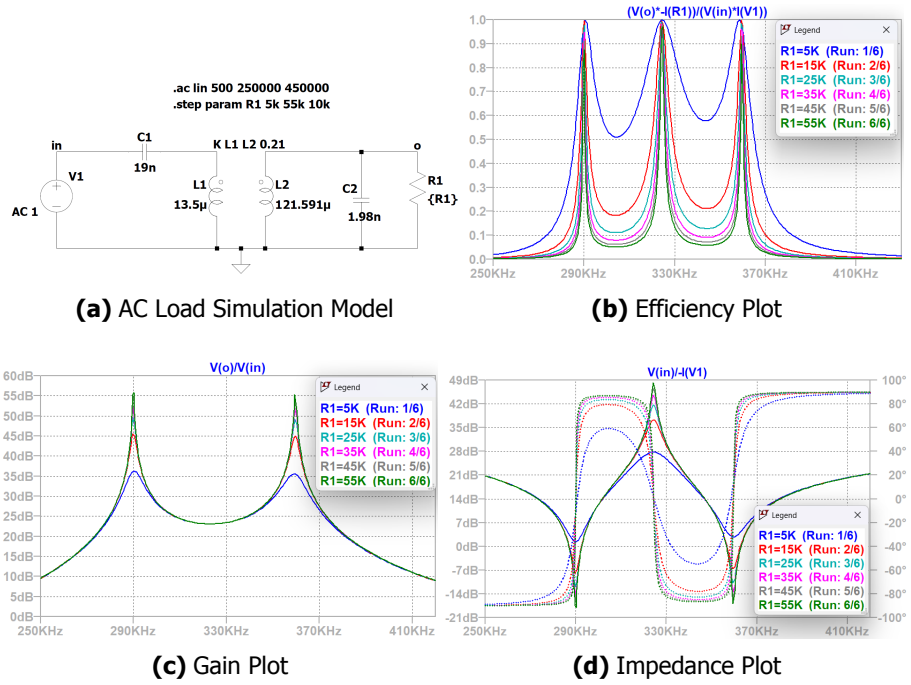
It is to be noted that the above derivation (Eq 3.14) ignores the parasitic resistances of the coils and it can be seen from [55] that they do not make a difference with respect to the fundamental operation of the IPT. High voltage gain which is load independent is the prime motive behind selecting the S-P IPT for the design of the HVIPT and this is proven from Eq 3.17.

Now, it can be seen that the output voltage is load-independent and is also inversely proportional to the coupling coefficient. This means that as the distance between the coils is increased, the output AC voltage at the secondary increases. The tradeoff, however, is the circulating current increases leading to a higher input current and lower efficiency. To analyse system efficiency it is important to know the input impedance of this topology. From the previous Eq 3.11 we can find Z_{in}. To operate the system at ZVS, it is imperative that this input impedance is slightly inductive in nature.

$$Z_{in} = \frac{V_{in}}{I_p} = Z_p + j\frac{\omega^2 M^2}{Z_s} = R_p + j\omega L_p + \frac{1}{j\omega C_p} + \frac{\omega^2 M^2}{R_s + j\omega L_s + \frac{R_L}{1+j\omega C_s R_L}} \tag{3.18}$$

From the M model in Eq 3.1 and the above input impedance, it can be seen that ωM has to be as high as possible to enable an inductive impedance for a wide range of load resistance while minimising the circulating current. This can be done by having a high switching frequency, high coil inductance or a high coupling coefficient. The latter two are bounded by the size constraints of the coil and the space between the coils respectively. Moreover, having a lower coupling coefficient is beneficial to obtain HV required for the HVIPT. High switching frequency is limited by the switching capability of the inverter's MOSFET, HV rectifier and litz wire of the coils. A detailed explanation regarding parametric selection will be discussed in Chapter 4 as well as later in this chapter in Section 3.9. However, in general, the design process is as follows: the primary, secondary coils and coupling coefficient are fixed at first. A suitable operation frequency is then selected. The compensation capacitors are then determined at the desired operation frequency according to Eq 3.16 [47]. Important to note is that the primary compensation capacitor is dependent on the coupling coefficient in this topology.

A simulation with an equivalent AC load is shown in Fig 3.4 in order to understand the gain, efficiency and input impedance of this topology.



(a) AC Load Simulation Model **(b)** Efficiency Plot

(c) Gain Plot **(d)** Impedance Plot

Figure 3.4: Frequency sweep of S-P topology with a variable AC load

In Fig 3.4, the S-P topology is tuned at 320 kHz. The following observations can be made from Fig 3.4. Theoretically, operating at the resonant frequency will provide unity efficiency for the entire load range [Fig 3.4b]. Accordingly, the gain remains high (around 25 dB) for all loads at the resonant frequency [Fig 3.4c]. An inductive input impedance is shown in Fig 3.4d for all simulated loads at a frequency slightly below the resonant frequency, allowing the HVIPT to ignore the bifurcation concept as discussed in [43] [56]. However, this assumption is only possible when the S-P topology is operating at a fixed frequency slightly below the resonant frequency, providing the inductive input impedance required for ZVS.

3.3. Mathematical Model

In any resonant converter, First Harmonic Analysis (FHA) is not enough to analytically understand the topology. In these resonant circuits, higher harmonic voltages and currents are seen across the impedances and these have to be analysed in order to obtain the exact behaviour of the system. By using the equivalent circuit shown in Fig 3.3 for each harmonic component, one can calculate the currents, voltages, and other electrical quantities across the components of the S-P IPT. By adding all the harmonics components of the respective electrical quantities, accurate results as compared to FHA can be obtained. The output of the H bridge inverter itself is a square wave, which means it has considerable higher-order harmonics. Therefore

in this section, a mathematical model for this topology is developed as similar to [57] considering the load to be an AC load (R_{ac}) as shown in 3.3. Since the output of the H bridge is a square wave, the even harmonics are zero. Accordingly, the voltages and currents of every odd^{th} harmonic are calculated as per Table 3.2 and plotted in Fig 3.5 using Matlab till the 29th fourier harmonic.

Table 3.1: Harmonic breakdown of impedances

Parameter	h^{th} harmonic Value
Primary Impedance (Z_P)	$R_P + j\left(h\omega L_P - \frac{1}{h\omega C_P}\right)$
Secondary Impedance (Z_S)	$R_S + jh\omega L_S + \left(\frac{R_{ac}}{1+jh\omega C_S R_{ac}}\right)$
Referred Impedance (Z_r)	$\frac{(h\omega M)^2}{R_S+jh\omega L_S+\left(\frac{R_{ac}}{1+jh\omega C_S R_{ac}}\right)}$
Total Impedance (Z_T)	$R_P + j\left(h\omega L_P - \frac{1}{h\omega C_P}\right) + \frac{(h\omega M)^2}{R_S+jh\omega L_S+\left(\frac{R_{ac}}{1+jh\omega C_S R_{ac}}\right)}$

The voltages are derived using the currents flowing through the components and multiplying them with their respective impedances. The currents are derived from the voltage across a particular component and dividing them with the respective impedance. An impedance table [Table 3.1] is shown for reference. The respective phase angles of the system are shown below. These phase angles refer to the shifts with respect to the input sinusoidal fourier harmonic. The Matlab script in Appendix A can be varied to find the behaviour of the IPT at different parameters ie: **Switching Frequency**, **Load**, **Coupling Coils**, **Input Voltage** and **Compensation Capacitors**. These parameters will also be discussed in Section 3.9.

The following phase angles mentioned in Table 3.2 are described below :

$$\varphi_p = \tan^{-1}(Z_{in}) \qquad \varphi_{C_P} = \tan^{-1}\left(\frac{1}{j\omega h C_P}\right) \qquad \varphi_{L_P} = \varphi_{C_P} - \varphi_p$$

$$\varphi_s = \tan^{-1}(Z_S) \qquad \varphi_{\mathrm{Cs}} = \tan^{-1}\left(\frac{R_{ac}}{R_{ac}+\frac{1}{j\omega h C_S}}\right) \qquad \varphi_{\mathrm{R}_{ac}} = \tan^{-1}\left(\frac{\frac{1}{j\omega h C_S}}{R_{ac}+\frac{1}{j\omega h C_S}}\right)$$

$$\varphi_{v_o} = \tan^{-1}\left(\frac{1}{j\omega h C_S}\right)$$

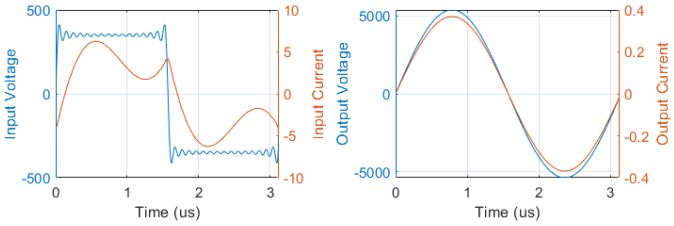
In Fig 3.5 the results of the mathematical model are shown for the parameters as mentioned in Table 3.3. Input current along with all the other component currents and voltages are shown as well as the Fourier decomposition of the input voltage and current. From Fig 3.5, it can be seen that the input current and the input voltage have considerable 3^{rd} & 5^{th} order harmonics. Moreover, neither the primary capacitor voltage nor the primary inductor voltages are sinusoidal in nature. However, the secondary side voltages are all completely sinusoidal and this can be explained by the fact that the secondary capacitor and load are parallel to the secondary coil which is practically a parallel RC load.

Table 3.2: Mathematical Model of S-P topology

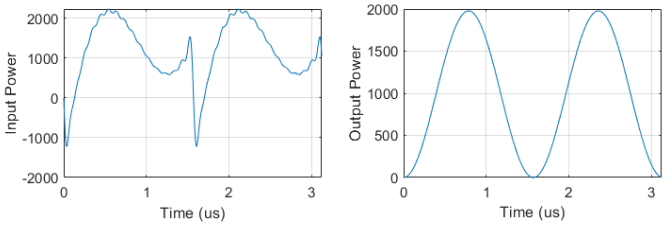
Parameter	Maximum h^{th} harmonic - Magnitude	Angle
H Bridge Voltage	$\sum_{h=1,3,5..}^{\infty} \frac{4V_{in}}{h\pi}$	$h\omega t$
Input Primary Current	$\sum_{h=1,3,5.}^{\infty} \frac{4V_{in}}{\pi h\lvert Z_{in}\rvert}$	$h\omega t$ - φ_p
1º Capacitor Voltage	$\sum_{h=1,3,5.}^{\infty} \left\lvert \frac{1}{j\omega hC_P} \right\rvert \frac{4V_{in}}{\pi h\lvert Z_{in}\rvert}$	$h\omega t$ - φ_p + φ_{C_P}
1º Coil Voltage	$\sum_{h=1,3,5..}^{\infty} \sqrt{\left(\frac{4V_{in}}{\pi h}\right)^2 + \left(\left\lvert \frac{1}{j\omega hC_P} \right\rvert \frac{4V_{in}}{\pi h\lvert Z_{in}\rvert}\right)^2}$	$h(\omega t + \pi/2) + \varphi_{L_P}$
2º Coil Voltage	$\sum_{h=1,3,5.}^{\infty} \omega M \frac{4V_{in}}{\pi h\lvert Z_{in}\rvert}$	$h(\omega t + \pi/2)$
2º Coil Current	$\sum_{h=1,3,5.}^{\infty} \omega M \frac{4V_{in}}{\pi h\lvert Z_{in}\rvert\lvert Z_S\rvert}$	$h(\omega t + \pi/2)$ - φ_s
2º Capacitor Current	$\sum_{h=1,3,5..}^{\infty} \left\lvert \frac{R_{ac}}{R_{ac}+\frac{1}{j\omega hC_S}} \right\rvert \omega M \frac{4V_{in}}{\pi h\lvert Z_{in}\rvert\lvert Z_S\rvert}$	$h(\omega t + \pi/2)$ - φ_s + φ_{C_s}
2º Load Current	$\sum_{h=1,3,5..}^{\infty} \left\lvert \frac{\frac{1}{j\omega hC_S}}{R_{ac}+\frac{1}{j\omega hC_S}} \right\rvert \omega M \frac{4V_{in}}{\pi h\lvert Z_{in}\rvert\lvert Z_S\rvert}$	$h(\omega t + \pi/2)$ - φ_s + $\varphi_{R_{ac}}$
2º Capacitor Voltage	$\sum_{h=1,3,5..}^{\infty} \frac{\left\lvert \frac{R_{ac}}{R_{ac}+\frac{1}{j\omega hC_S}} \right\rvert \omega M \frac{4V_{in}}{\pi h\lvert Z_{in}\rvert\lvert Z_S\rvert}}{\omega hC_S}$	$h(\omega t + \pi/2)$ - φ_s + φ_{d_1} + φ_{v_o}

Table 3.3: Parameters for the Mathematical Model

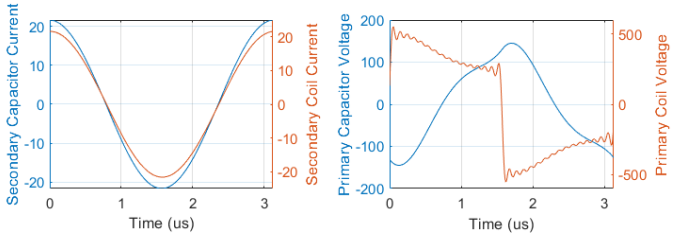
Parameters	Value
Primary Inductance	13 µH
Secondary Inductance	125 µH
Primary Capacitor	19 nF
Secondary Capacitor	1.96 nF
Coupling Coefficient	0.21
Switching Frequency	320 kHz
Input voltage	300 V
AC Resistance Load (Rac)	20 kΩ



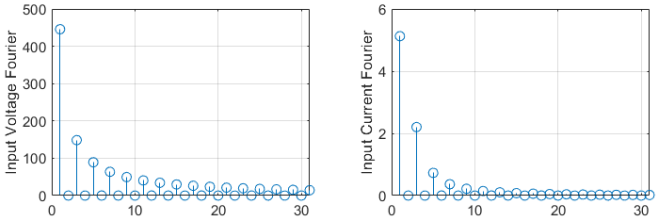
(a) Input Voltage & Current



(b) Input and Output Power for an AC Load



(c) Voltage & Current waveforms across components of S-P topology



(d) Fourier Decomposition of Input Voltage & Current

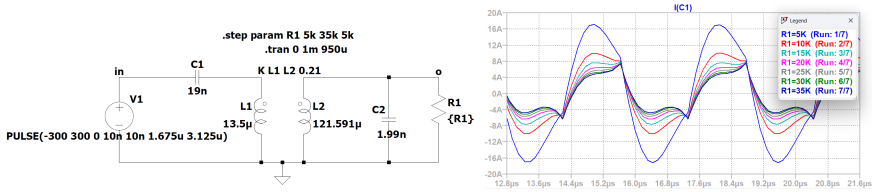
Figure 3.5: Results of the Mathematical Model

3.4. Simulation

The mathematical analysis enables us to understand the fourier decomposition of the IPT. However, this analysis gives minimal insight into the behaviour of the inverter and HV rectifier. Moreover, the mathematical analysis assumes an equival-

ent AC load which is not the case in reality. With simulations, the high-frequency inverter and HV rectifier can be implemented, thereby giving a better insight into system behaviour while enabling analysis of different parameters affecting the IPT behaviour. In Figures 3.6, 3.8, 3.10, 3.12 are the SPICE simulations of the S-P topology. With each progressive simulation, the complexity of the system is increased and the system behaviour is evaluated.

For the HVIPT it is crucial that the system operates efficiently at all load values above a particular value dictated by the power level of the supply. Therefore the behaviour of the HVIPT must be evaluated from rated loads to light loads. To analyse this behaviour, it is imperative to study the input current characteristics across all load values to understand the converter behaviour.

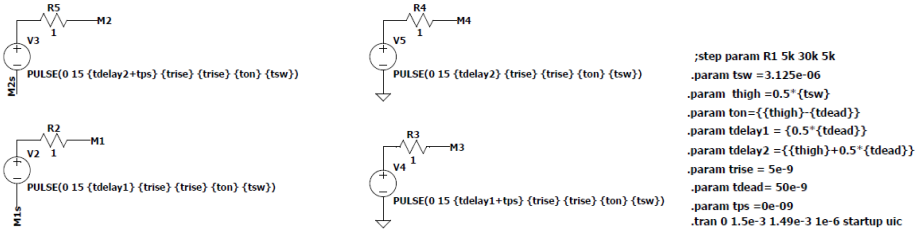


(a) Spice Simulation **(b)** Input current at various loads

Figure 3.6: Load sweep of the S-P IPT

From Fig 3.6, it is concluded that as the load resistance increases, input current decreases which indicates that the HVIPT operates efficiently in the given load range. However, as the load moves towards an (open circuit) no-load condition the effective power delivery reduces and the input current is fed only to facilitate the circulation current in the secondary inductor and capacitor.

3.5. ZVS Operation



(a) Gate Drive for Simulation **(b)** Parameters

Figure 3.7: Driving conditions for SPICE simulation

In Fig 3.6a the input was DC square pulses while in reality there is an inverter providing these pulses from the DC source. To understand the switching device behaviour and whether the MOSFETs operate with ZVS, simulations on SPICE are

done using the C2M0160120D Mosfet by CREE for the inverter as it provides an accurate Level 3 LTSpice model. With an AC resistive load, the operation of the switch with variation in deadtime and circuit parameters such as output load can be observed. The gate drive and simulation parameters for SPICE simulations is shown in Fig 3.7.

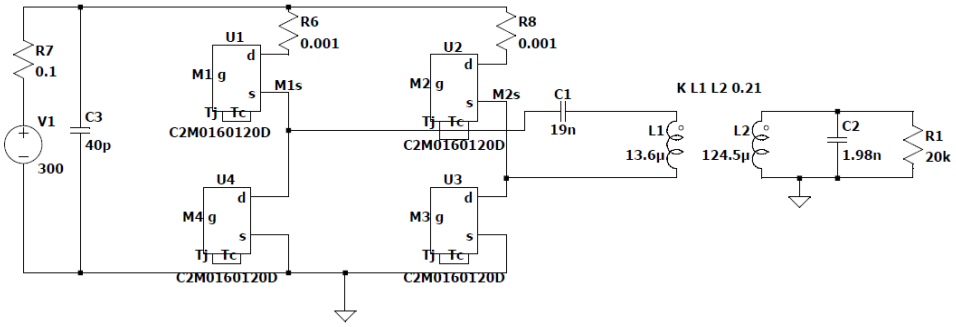


Figure 3.8: SPICE Model to analyse ZVS

Soft switching, in this case, ZVS is done to discharge the C_{ds} of the switch and prevent charge energy dissipation in the switch, during turn-on. To enable this behaviour a certain dead time between the switching cycles must be introduced to achieve the discharge of the drain-source capacitor. Eq 3.19 [33] [58] indicates that the dead time applied decides the minimum negative current required to discharge the drain-source capacitor before the conduction cycle of the other leg begins. The losses saved from the ZVS in an IPT system, are more than the extra input power arising by a lack of ZPA. However, the turn-off current of the MOSFET (I_{off}) must not be too high and should be around the minimum current indicated in Eq 3.19. This condition must be followed to prevent extra turn-off losses of the other 2 switches involved in the H bridge inverter. In Fig 3.8 a deadtime of $50\,\text{ns}$ is implemented and lagging input current with ZVS is shown in Fig 3.9. Additionally from Fig 3.4d it is shown that the S-P provides ZVS at all load points provided a sufficient deadtime is applied.

From Eq 3.19, it is concluded that the dead time has to be above a particular value to obtain soft switching. The limit on increasing the dead time is dependent on the switching frequency and the rate at which C_{ds} of the MOSFET discharges. If the deadtime is above a certain duration, then the resonant converter will see the system as a phase-shifted setup. Alternatively, if the dead time is much larger than the time required to discharge the C_{ds} capacitor, then the inverter will provide no voltage to the IPT till the opposite leg is turned on.

$$I_{OFF} > \frac{2C_{ds}V_{in,\max}}{t_{dead}} \tag{3.19}$$

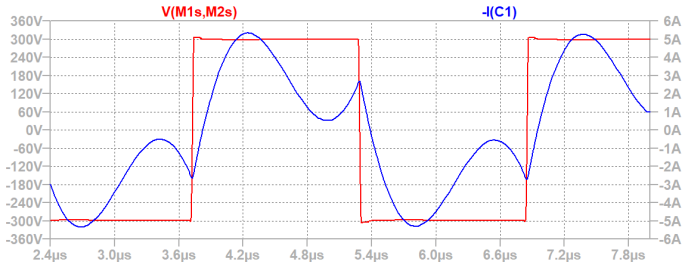


Figure 3.9: ZVS analysis from lagging input current

3.6. Diode Rectifier

In the previous section, the simulation involves an AC resistive load. A DC output is needed for the HVIPT and one of the options is the diode rectifier. The output of an S-P IPT is a constant voltage source which gives current as needed by the load. The rectification transfers this current while rectifying the AC voltage to DC. A filter capacitor is added to maintain the DC voltage and the value of this capacitance decides the voltage ripple.

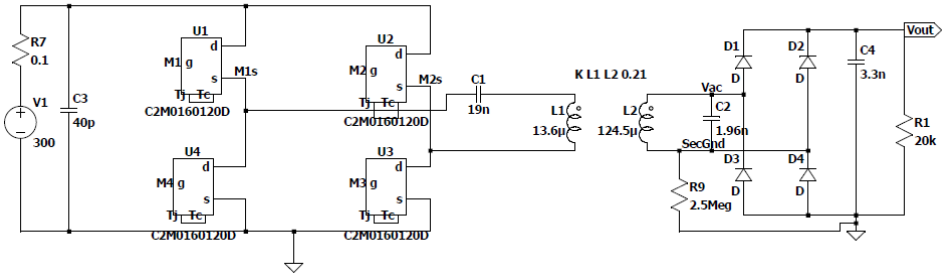
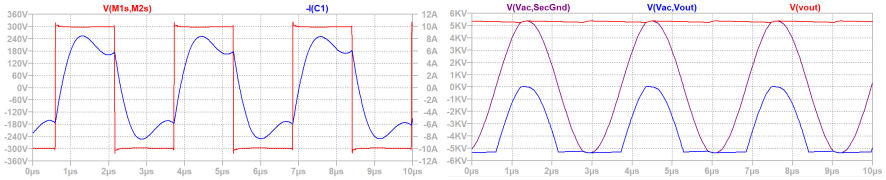


Figure 3.10: SPICE model of Diode Rectifier

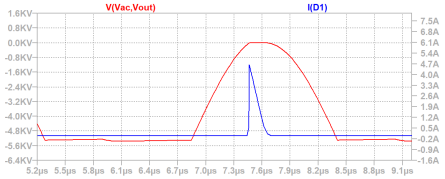
In Fig 3.10 the spice simulation of the HVIPT with a diode rectifier is shown. An interesting observation is that there is a floating point on the secondary inductor which has no reference to any ground. For this reason, a large resistance is added to the secondary ground to enable the simulation. Accordingly, during realisation, it must be considered that a point on the secondary inductor can not be connected to the common ground of either the primary side or the secondary diode rectified side. This leads to a floating point and could lead to an issue during testing of the AC output from the IPT. The grounds of the primary and secondary have to be different, however, in this setup, the secondary inductor is floating which is undesirable, especially for measuring and from a safety point of view.

Another factor to be considered is the ripple capacitor value as it determines the current spike the diode undertakes to charge the capacitor. Higher capacitance for filtering means a lower output voltage ripple and higher diode spike currents.

A higher switching frequency also implies that the time available to charge the capacitor is lower and therefore the current spike is higher. In Fig 3.10 the operating frequency is 320 kHz and the filter capacitor is 3.3 nF.



(a) Input Voltage & Current **(b)** Output AC, DC & Diode Voltages



(c) Diode Voltage & Current

Figure 3.11: Simulated waveforms of Diode Rectifier

In Fig 3.11 the simulation results of the S-P IPT with the diode rectifier are shown. An output AC and DC voltage of around 5 kV is shown in Fig 3.11b and the DC ripple is around 150 V. The behaviour of a single diode in the diode rectifier is shown in Fig 3.11c. Reverse recovery currents of the diode are not shown in the simulations as an ideal diode is used, however in Chapter 5, diode reverse recovery currents are observed in the LV tests.

3.7. Voltage Multiplier

For a given AC output voltage from the IPT, the diode rectifier only provides an equivalent DC voltage. For HV sources a higher voltage is desired albeit at the same power rating. A convenient solution to the multiplication of DC voltage when rectifying AC is known as the Greinacher or Cockcroft & Walton rectifier [34] mentioned simply as the voltage multiplier in this thesis. In this thesis, a single-stage multiplier is used to get 10 kV from the 5 kV AC output at a power level of maximum 1.25 kW.

In Fig 3.12, a 10 kV DC output is expected and the capacitor is varied for the DC rectifier according to the desired ripple [Eq 3.20] [34]. The advantage of the multiplier is that the ground of the secondary inductor is the same as the load ground which can be seen by resistor R1 in Fig 3.12. In a typical multiplier circuit, the operational frequency is 50 Hz or a few kHz [29]. However, here the system is operating at 320 kHz. This helps the capacitor and the entire multiplier to be smaller, faster and observe lesser ripple than the conventional multiplier circuits.

For an n-stage voltage multiplier, the output DC voltage is 2*n times the AC

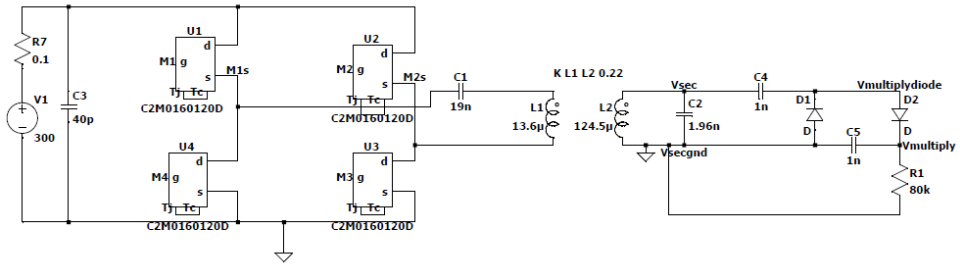
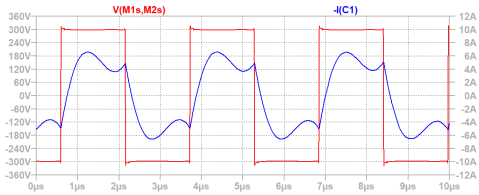
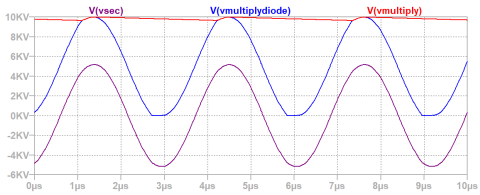


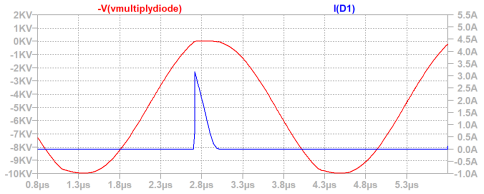
Figure 3.12: SPICE Model of a One stage Multiplier



(a) Input Voltage & Current



(b) Output AC, DC & Diode Voltages



(c) Diode Voltage & Current

Figure 3.13: Simulated waveforms of One Stage Multiplier

voltage across the secondary capacitor. The DC voltage ripple at the output of the multiplier is dependent on the n-stage multiplier as highlighted in Eq 3.20, where i_o is the output current of the HVIPT. The value of the multiplier capacitors can be made higher to obtain a small ripple. However, higher capacitance values lead to an increase in the diode spike currents, which have to be within the manageable values for the diodes being used [Fig 3.13c]. The diode provides current to the capacitor only when the capacitor is depleted of charge. Therefore, a higher capacitor indicates a larger diode peak current while obtaining a smaller output DC ripple. In Fig 3.12 a filter capacitor of $1\,\text{nF}$ is used at a switching frequency of $320\,\text{kHz}$. This operating condition gives a ripple of $300\,\text{V}$ for the single-stage multiplier as shown in Fig 3.13b where the blocking voltages across the diode and the AC voltage across the secondary parallel capacitor are also shown.

$$V_r = \frac{q}{C} = \frac{i_0}{fC}(1 + 2 + 3 \ldots n) \tag{3.20}$$

3.8. Efficiency Analysis

Generally, test sources operate at higher efficiencies for optimal loads and at other points they follow a decreasing trend and at no load, they have very minimal input currents. In an IPT however, the resonant circuit as shown in Fig 3.1 has a certain circulating current operating through the resonant circuit [Fig 3.6b], even at no load. This allows the system to operate as a constant voltage source that provides the required current as per the load connected at the HV side. In Fig 3.6b the system still operates with ZVS even at no load, which is ideal for the operation of the MOSFET and thus the inverter.

Sources of losses in the IPT include the litz wire conduction loss which involves R_{ac} at the operational frequency. The ESR of the primary and secondary capacitors also contribute to power loss. The former is easy to evaluate using R_{ac} and knowing the currents through the coils. The latter contributes minimally to the overall loss. Therefore power loss across the capacitor can be ignored. The final sources of power loss come from the inverter and HV rectifier. These are basically the conduction loss, turn-off losses of the MOSFET in the inverter and the diode conduction and reverse recovery loss in the HV rectifier.

To increase efficiency for a given load, the mutual inductance (M) or switching frequency (ω) can be increased [59]. This increase basically limits the input current by minimising the circulating current in the S-P IPT. However, any increase in either (M or ω) is limited by the switching device of the inverter and the size constraints of the coils. Further analysis of efficiency will be explained with the test results in Chapter 5. However, to understand how different parameters affect the operation and efficiency of the S-P topology, the next section delves into parametric evaluation of the HVIPT.

3.9. Parametric evaluation

The simulations in this chapter have assumed certain parameters such as a switching frequency of 320 kHz, the coupling coefficient of around 0.2-0.25 and primary and secondary inductances of 13 µH, 125 µH respectively. However, it is important is know how these parameters have been chosen and what are the trade-offs in deciding these parameters. In this section, the parametric evaluation of the S-P topology for the HVIPT is conducted. Using the analysis from this section the prototype will be developed in Chapter 4.

- **Switching frequency :** Switching frequencies in EV and biomedical implants are limited by IEC, IEEE and other standards. These limits are basically pertaining to the surrounding magnetic field at a particular power transfer level. However, for the HVIPT, the switching frequency is allowed to be much higher. This is because this supply will be used in a laboratory environment

and not in sensitive domestic surroundings. Therefore, the switching frequency is limited by the capability of the switching devices used in the HVIPT. SiC MOSFETs can go up to 500 kHz with rise times being as small as 5-10ns and their body diode reverse recovery times being in the order of 50-100ns for obtaining ZVS [60]. However, the HV rectifier must operate at these frequencies which is also possible with the SiC diode available in the market today which has minimal reverse recovery times of around 50 ns [61]. The last bottleneck for having any particular switching frequency is the litz wire and its skin depth which is given by the Eq 3.21 where f: frequency (Hz), μ : permeability (H/m), σ : electric conductivity (S/m)

$$\delta = \frac{1}{\sqrt{\pi \cdot f \cdot \mu \cdot \sigma}} \tag{3.21}$$

Table 3.4: Skin Depth of Copper

Frequency	Skin Depth
10 kHz	0.65 mm
50 kHz	0.29 mm
100 kHz	0.21 mm
200 kHz	0.15 mm
400 kHz	0.10 mm
800 kHz	0.07 mm

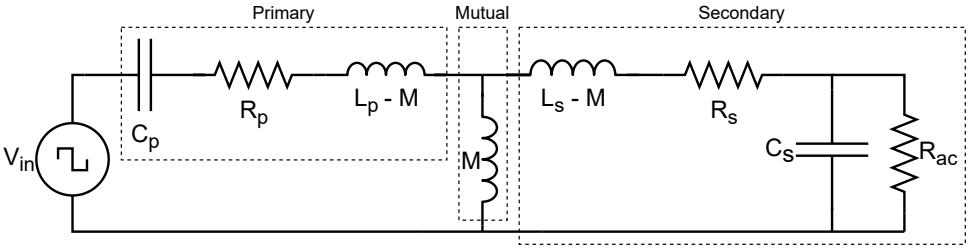


Figure 3.14: Mutual Inductance Model

As much as physically possible, a high product of ωM is required for the S-P topology to limit the amount of input current for the same operating conditions. This can be understood from the M model in Fig 3.14 where the secondary capacitance is parallel to the load resistor and therefore the circuit behaves as a parallel RLC circuit with the inductor controlling the input current from the inverter. The graph [Fig 3.15] from the mathmematical model shows the variation of the input current for different frequencies keeping other parameters constant as shown in the Table 3.5. Upon increasing the switching frequency, the input current gets more sinusoidal for the same load. This means the higher mutual inductance involved in coupling the coils takes a

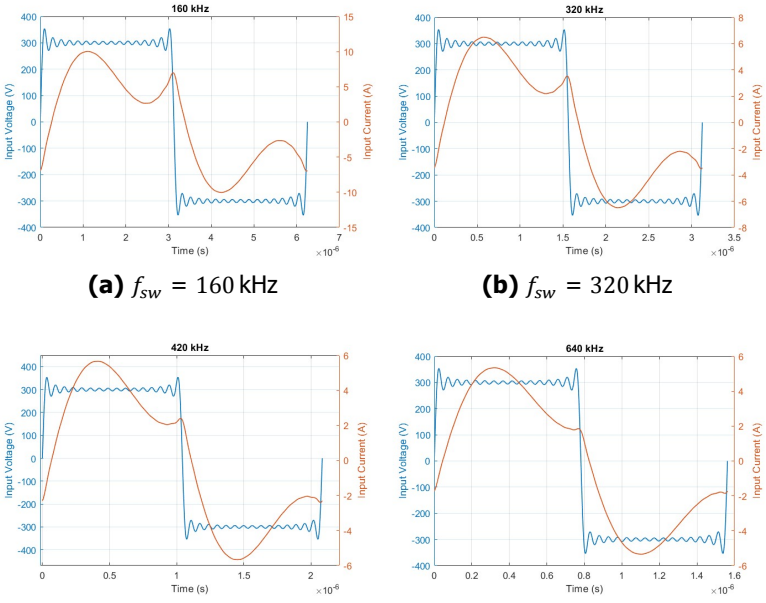
Table 3.5: Parameters of HVIPT to analyse f_{sw}

Parameters	Value
Primary Inductance	13 µH
Secondary Inductance	125 µH
Coupling Coefficient	0.21
Input voltage	300 V
AC Resistance Load (Rac)	20 kΩ
Output Voltage (peak)	5 kV
Output Power	1.25 kW

Table 3.6: Input Current at different switching frequencies

Frequency	Input Current (rms)
80 kHz	13.76 A
160 kHz	6.37 A
320 kHz	4.24 A
640 kHz	3.64 A

lower current and more of the input power is transferred to the output and thereby efficiency is increased. Lower input current also reduces the parasitic loss caused by the resistance of the litz wire.



(a) f_{sw} = 160 kHz **(b)** f_{sw} = 320 kHz

(c) f_{sw} = 420 kHz **(d)** f_{sw} = 640 kHz

Figure 3.15: Input behaviour of the HVIPT based on switching frequency (f_{sw})

- **Primary and Secondary Coil Inductances:** While developing the IPT, the primary, secondary inductances along with the coupling coefficient must be decided simultaneously. The coupling coefficient is a function of the geometry, size of the coils and then the distance between them. The goal is to get the maximum inductance in a smaller area and keep the two coils at least 5cm away in this thesis, to enable insulation with respect to high voltage. The smaller size requirement arises from the fact that usually DC test sources in the range of 10 kV are usually compact albeit with some kind of insulation material which is eliminated in the HVIPT. Therefore, no coil in this thesis will be bigger than 15 cm in radius which provides a limitation on the maximum inductance possible for the secondary coil.

  Generally, it can be seen that for bigger coils and larger inductances a higher coupling coefficient can be obtained for the same distance separation [62]. A high gain (around 15) is desired in this system which can be obtained from having a larger secondary coil. However, the additional gain is provided by the low coupling coefficient (0.2-0.4) as shown in Eq 3.17. Therefore, a turns ratio of around 3 is considered for the HVIPT.

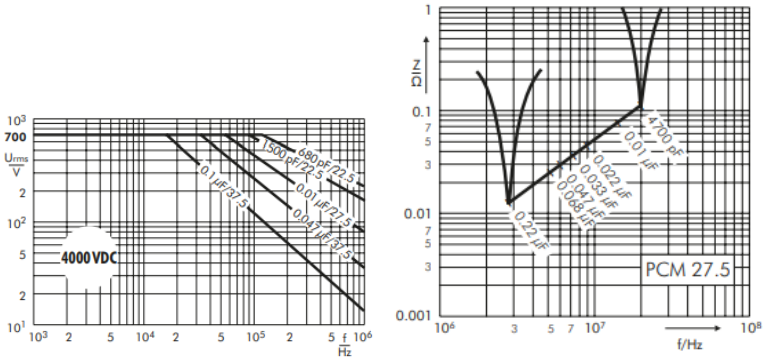
  A coupling coefficient lower than 0.15 is not considered in this thesis because as highlighted in Fig 3.14 in an IPT system, the mutual inductance must be kept as high as possible to reduce the circulating current in the secondary coil and capacitor. Considering that the primary inductances are not high when compared to EV charging [15], it is imperative to not have a very low coupling coefficient so as to maintain the mutual inductance required for a more efficient operation of the so-formed resonant converter.

- **Input Voltage :** Considering input from the AC grid through an active pfc rectifier, a maximum DC input of 400 V can be considered. For testing purposes, a DC source with controllable voltage is used to provide the DC Bus. Alternatively, in certain cases, a boost DC-DC converter could be used to provide a higher DC square wave input voltage and then achieve a higher output DC voltage. However, another converter for this application will take up additional space, costs and complexity. Therefore in this thesis a maximum of 400 V DC is considered as the input for the H bridge inverter.

- **Load :** Considering a high voltage and low power (1.5 kW) application of the HVIPT, high resistances ($> 20\,\text{k}\Omega$) must be used to test the designed converter at different load points. Also, the system as seen before must be capable of providing HV output at no load conditions and during capacitive load applications. Therefore, the HVIPT must be tested for all $R_l > V^2/P$ and when these loads vary instantaneously. This means for testing corona, partial discharges and breakdowns there is a need to have a damping resistor to limit the flow of current and make the impedance as seen by the resonant converter bigger than the particular load resistance R_l.

- **Compensation Capacitor :** Based on the coupling coefficient, coupling coils and switching frequency the compensation capacitors are found as per Equa-

tions 3.5 and 3.6. The voltages across these capacitors are AC voltages and those ratings must be considered while selecting the capacitors for the prototype. A factor to consider is that the secondary capacitance is very sensitive for obtaining resonance. In Fig 3.11a and Fig 3.9, the secondary capacitance has only been varied 1% (50 pF) and yet the input current seen in their respective simulations are considerably different. Therefore for the HV secondary parallel capacitor, a capacitor bank with many capacitors in series and parallel must be constructed to meet the HV requirement and obtain the exact required capacitance. Moreover, these capacitors must handle high frequencies without loss of performance due to their ESR and parasitics. Polypropylene film ceramic capacitors from WIMA meet these requirements. Generally, it is seen that lower values of capacitances can operate at higher frequencies [Fig 3.16b]. It must be noted that PCM 27.5 indicates the distance between the leads to be 27.5 mm. High blocking voltages are also observed at higher frequencies when the value of the capacitances is lower [Fig 3.16a]. Therefore, it is beneficial to make the secondary high-voltage capacitor using multiple smaller polypropylene film capacitors in series and parallel. The constructed secondary capacitor is shown in Fig 4.9, in the next chapter where the HVIPT prototype will be developed.



(a) Voltage blocking characteristic **(b)** Impedance characteristic

Figure 3.16: WIMA PCM 27.5 capacitor behaviour across frequencies [63]

This chapter provides a detailed evaluation of the S-P topology for its use in the HVIPT. The topology's additional gain and load invariant property makes it feasible in the HVIPT. The mathematical model thus developed provides the harmonic behaviour of the input current of the resonant converter. In low-load conditions, the higher harmonics of the input current dominate over the fundamental component. Simulation results of the S-P topology provide insight into prototype development considering aspects such as ZVS operation and HV rectifier. Finally, a parametric evaluation of the topology is done to choose a switching frequency of 320 kHz, *coupling coefficient of 0.25 and primary and secondary inductances of* 13 µH *and* 125 µH *for the prototype.*

4

Prototype Setup

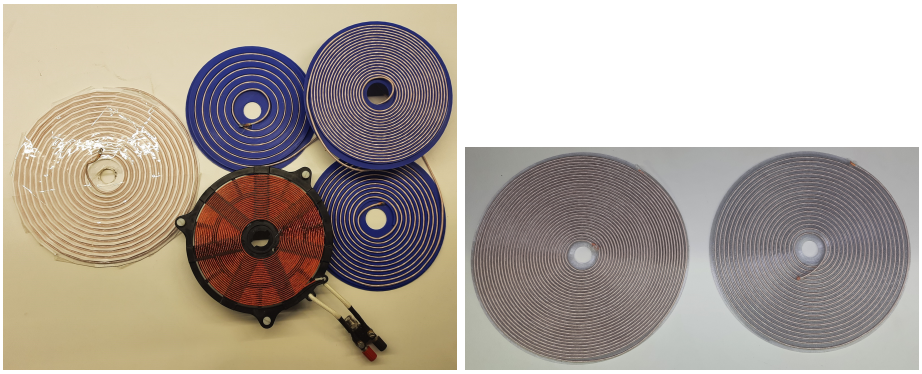
This chapter provides a detailed description of prototype development which involves the selection of the coils, compensation capacitor, test loads, high-frequency inverter, HV rectifier and HV multiplier. The reasoning behind several decisions and constraints during prototype development are also provided in this chapter. As highlighted earlier the goal is to get around 5 kV *DC output for the diode rectifier and* 10 kV *with a single-stage voltage multiplier from a* 300 V - 400 V *DC input.*

4.1. Coils

The coils in an IPT system enable the transfer of power in an WPT which makes it a crucial component in the design of the HVIPT. The transfer of power basically occurs through flux linkage as directed by the Amperes and Faradays law [64] [65]. Several coil configurations are available for this application, which are discussed below.

The fundamental coil shapes are Circular, Square and Rectangular which are unipolar in nature [66] [67]. These shapes have single current flow paths and are convenient to design and develop [68]. Alternatively, several complex shapes are also present in the literature [69] [35]. These include DD, DDQ etc which are bipolar in nature, meaning each of the primary and secondary is split into 2 coils to achieve the required coupling magnetic field. These configurations of coils are typically used for interoperability, misalignment, and bidirectional amongst other reasons [70]. However, for the HVIPT the goal is to obtain maximum inductance in a minimal area and a suitable coupling coefficient above a particular distance between the coils. Additionally, the coils must have good HV insulation to avoid inter-winding breakdown. Therefore based on these requirements, the planar circular (spiral) coil seems appropriate and is the chosen option for this thesis.

The key priority in designing these coils is to maximise the quality factor which is defined in Equations 4.1, 4.2 and 4.3. The higher the quality factor is, the closer the coil behaves to an ideal inductor [68]. To get a high-quality factor, the aim is for each



(a) Smaller Coils (Diameter < 20 cm) **(b)** Bigger Coils (Diameter < 30 cm)

Figure 4.1: Designed Coils for HVIPT [Table 4.1]

coil to have high self-inductance and minimal parasitic resistance. Another factor to consider is the parasitic winding capacitance which dictates the self-resonant frequency (SRF) of the coil [Eq 4.4]. Operating at this resonant frequency is to be prevented as the coil is seen as an open circuit due to the parasitic capacitance compensating with the self-inductance of the coil. It is thus recommended to have the self-resonant frequency of the coil much higher than the operating switching frequency.

$$Q_{pri} = \frac{\omega_0 L_{pri}}{R_{pri}} \tag{4.1}$$

$$Q_{sec} = \frac{\omega_0 L_{sec}}{R_{sec}} \tag{4.2}$$

$$Q = \sqrt{Q_{pri} * Q_{sec}} \tag{4.3}$$

$$f_{SRF} = \frac{1}{2 * \pi * \sqrt{C_{coil} * L_{coil}}} \tag{4.4}$$

To achieve a particular gain in the S-P topology, the coupling coefficient and the self-inductances of the primary and secondary coils need to be known. These parameters are found using analytical, finite element modelling methods and then verified through practical measurements using the Bode 100 Vector Network Analyser (VNA). The analytical calculation was done according to the planar spiral coils equation for self and mutual inductances in [67], [71] & [72]. In Eq 4.5, N refers to the number of turns in the planar spiral inductor, while d_{out} and d_{in} relate to the outer and inner diameter of the coil.

$$L = \frac{\mu_0 N^2 d_{\text{avg}}}{2} \left[\ln\left(\frac{2.46}{\gamma}\right) + 0.20\gamma^2 \right] \tag{4.5}$$

where

$$\gamma = \frac{d_{\text{out}} - d_{\text{in}}}{d_{\text{out}} + d_{\text{in}}}$$

and

$$d_{\text{avg}} = \frac{d_{\text{out}} + d_{\text{in}}}{2}$$

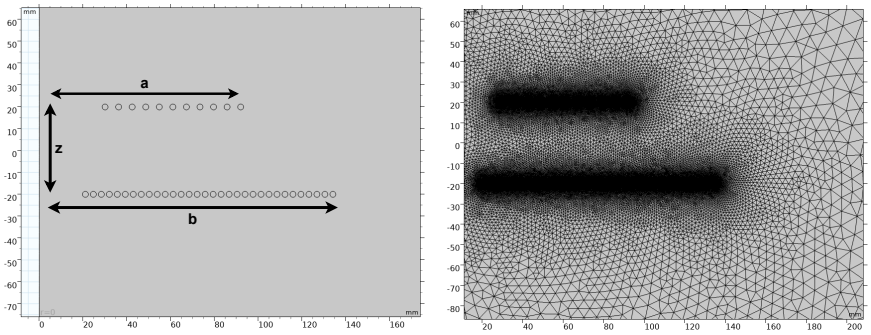
Meanwhile, the process of determining the mutual inductance involves calculating the mutual inductance between every single turn in the primary to a corresponding turn in the secondary as per Eq 4.6. Thereafter, these mutual inductances must be added to obtain the final mutual inductance between the coils. In Eq 4.6 a and b refer to the lateral distance of the respective coils from the coil centre while z refer to the vertical distance between the coils.

$$M = \frac{\mu_0 \pi a^2 b^2}{2\left(a^2 + b^2 + z^2\right)^{3/2}} \left(1 + \frac{15}{32}\gamma^2 + \frac{315}{1024}\gamma^4\right). \tag{4.6}$$

where

$$\gamma = 2ab/\left(a^2 + b^2 + z^2\right)$$

COMSOL Multiphysics is then used in the 2D axis symmetry mode to develop the 2 coils and find their self and mutual inductances for different separation distances. The developed model is shown in Fig 4.2. Using magnetic field physics, a unit current excitation is provided to either of the coils modelled as a single conductor. Thereafter, in derived values under global evaluation, the self and mutual inductances are found. Self inductance is obtained by dividing the developed voltage by $j\omega$. Mutual inductance is obtained by dividing the induced voltage by $j\omega$. Knowing the self-inductances of both the coils and their mutual inductance, the coupling coefficient can be found. Results obtained from the FEM Modelling are highlighted in Fig 4.5



(a) Layout of Coils **(b)** Meshing of the Model

Figure 4.2: FEM Modelling of the Coils

After obtaining the results analytically and through FEM, the Bode 100 VNA was used to obtain the self-inductances, parasitic resistance and winding capacitance

of the individual coils. Thereafter, the mutual inductance in the Bode VNA was obtained as per the procedure in the application note [73]. The process of determining the mutual inductance involved connecting the primary and secondary coils in a way such that their fields cancel [Fig 4.3]. From the series inductance, the mutual inductance can be found using Eq 4.7.

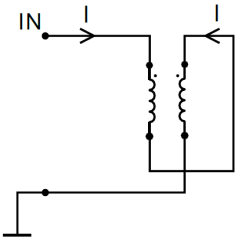
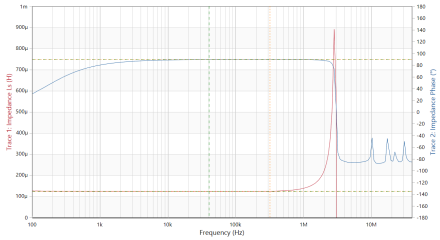


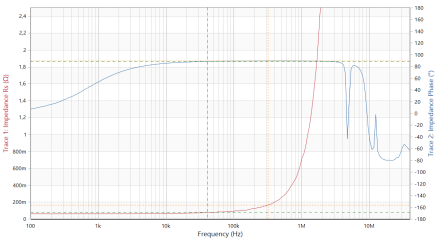
Figure 4.3: Series inductance (L_{series}) to measure M

$$M = \frac{L_{pri} + L_{sec} - L_{series}}{2} \tag{4.7}$$

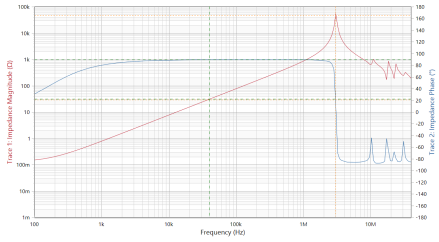
The results obtained from the Bode 100 VNA of the characteristics of the coil are shown in Fig 4.4.



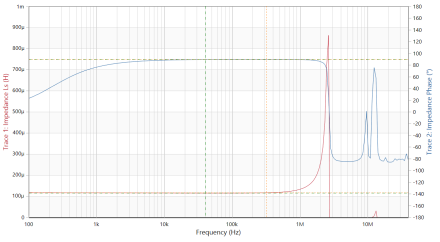
(a) Inductance Plot



(b) Resistance Plot



(c) Capacitance and SRF Plot



(d) Mutual (Series) Inductance Plot

Figure 4.4: Results from Bode100 VNA

The comparison of the 3 methods of coil evaluation is given below in Fig 4.5. The coils used for Fig 4.5 are Coil 4 and Coil 5 from Table 4.1.

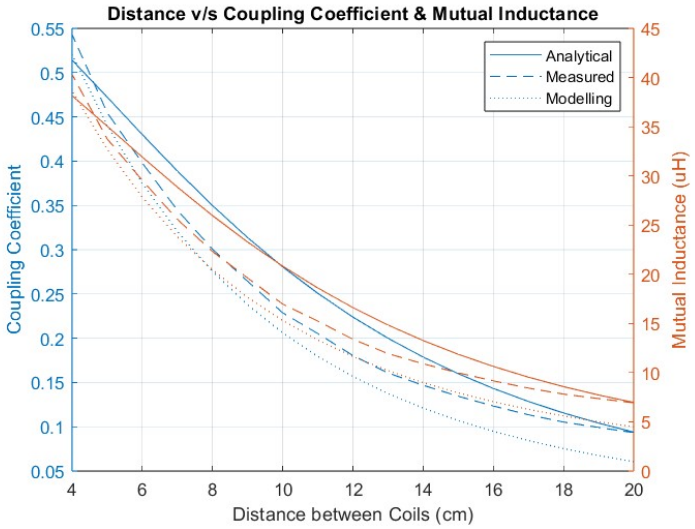


Figure 4.5: Mutual Inductance from the 3 methods of evaluation

Table 4.1: Specifications of 3D Printed Spiral Coils

Parameters	Coil 1	Coil 2	Coil 3	Coil 4	Coil 5
Coil Inductance	4.5 µH	13.6 µH	38.9 µH	45.3 µH	124.6 µH
Coil Resistance (50 kHz)	0.12 Ω	0.14 Ω	0.23 Ω	0.24 Ω	0.29 Ω
Coil Resistance (250 kHz)	0.17 Ω	0.20 Ω	0.32 Ω	0.33 Ω	0.66 Ω
Coil Resistance (1.25 MHz)	0.49 Ω	0.91 Ω	2 Ω	5.4 Ω	9.8 Ω
Parasitic Capacitance	14 pF	15 pF	28 pF	42 pF	22 pF
Self Resonant Frequency	19.3 MHz	10.7 MHz	4.7 MHz	3.6 MHz	2.2 MHz
Inner Diameter	65 mm	53 mm	43 mm	46 mm	46 mm
Outer Diameter	158 mm	180 mm	186 mm	262 mm	262 mm
Wire Diameter	2.7 mm	2.7 mm	2.7 mm	2.7 mm	2.7 mm
Distance between turns	10 mm	6.5 mm	3.5 mm	6 mm	3.6 mm
Number of Turns	5	10	18	18	30

Choosing the switching frequency suitable for the HVIPT is dictated by the input current for the rated load as shown in Fig 3.15. Accordingly, the current of the primary and secondary coils can be studied from simulations and the mathematical model. Considering a safety factor on the current and switching frequency, the litz wire is designed for the primary and secondary coils. The switching MOSFETs used in the H Bridge Inverter must be capable of operating at the chosen frequency.

Generally in biomedical applications and in electric vehicles there is a limit on switching frequency based on the maximum possible magnetic field in the application environment. This limit is 85 kHz for wireless charging of electric vehicles at powers in the range of 5 kW [35] and 10 MHz for Biomedical due to low power

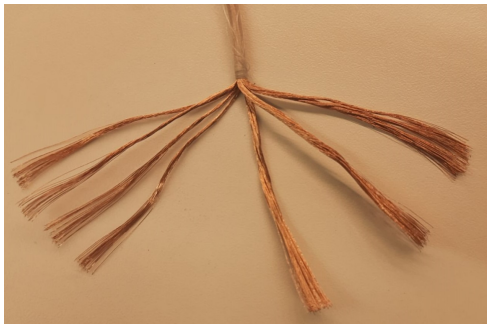


Figure 4.6: Litzwire subbundle

transfer in the range of 10 mW [74]. For HV testing applications, no personnel will be nearby the test source and moreover, there can be an encasing to prevent the magnetic fields at high switching frequencies in the surrounding environment. Therefore higher switching frequencies for power transfer level of around 1 kW are attainable and litz wire is used accordingly [75]. Considering the small size of the coils (maximum 15 cm radius) an operating frequency of 320 kHz is preferred. Having a high switching frequency provides a better quality factor, thereby increasing efficiency. Moreover, operating at a high frequency of 320 kHz reduces the circulating current in the secondary coil and the secondary capacitor, making it feasible to operate with low coupling coefficients since the reduction in magnetic coupling "k" can to some extent be compensated by the higher coil quality factor Q. In the S-P topology, the low coupling coefficient is beneficial as it gives a higher gain ratio for the same setup.

Table 4.2: Parameters of the chosen Litz Wire

Parameters	**Value**
No of Strands	400
Diameter of each Strand	0.1 mm
Wire Diameter	2.7 mm
No of Bundles	4
No of Sub Bundles	4
Maximum Frequency	425 kHz
Insulation Wrapping	1x52 Natural Silk

Litz wire is used to reduce the skin effect caused by eddy currents at high switching frequencies. Moreover, they are grouped in bundles and subbundles to eliminate the proximity effect across strands. The litz wire ends up in a configuration where each subbundle and bundle is twisted to achieve maximum copper area for a given diameter of the litz wire while eliminating the proximity effect [Fig 4.6]. This type of Litz wire is also known as a Type 2 litz wire. The details of the Litz wire used for the HVIPT are highlighted in Table 4.2. The maximum operating frequency is

considered when the skin depth is equal to the diameter of the strand. This basically is a sufficient rule of thumb while considering frequencies at which litz wire can be operated. However, theoretically, the AC resistance is still minimal when skin depth is equal to the radius of the copper strand. [76]

Several coils were made to analyse the high voltage gain possible at different conditions of coupling coefficients, frequencies and loads. The different coils designed are shown in Fig 4.1 and their details are in Table 4.1. Finally, the chosen coils are described in Table 4.3 and the setup is shown in Fig 4.7.

Table 4.3: Coil Parameters at 320 kHz

Parameters	Value
Primary Inductance	13.6 µH
Secondary Inductance	124.5 µH
Primary Resistance	0.22 Ω
Secondary Resistance	0.73 Ω
Primary Quality Factor	163
Secondary Quality Factor	387

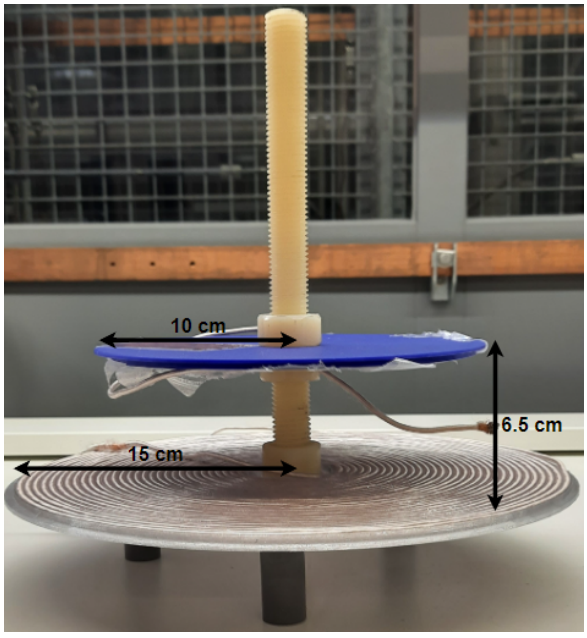


Figure 4.7: Primary & Secondary Inductors

4.2. Compensation Capacitors

The primary series capacitor is a variable polystyrene decade capacitor box which is rated upto 500 V [Fig 4.8]. It is good to know that the capacitor in Fig 4.8b has more flexibility in choosing the capacitance value which is used in a series of low-voltage tests as the secondary parallel capacitor. For the secondary parallel HV capacitor, a capacitor bank using WIMA capacitors (700 V AC rated and 2 kV DC rated) is developed. 3 parallel paths of 10 capacitors are connected to achieve the required capacitance of 1.91 nF operating at 320 kHz [Fig 4.9]. This capacitor bank developed on the secondary is rated for up to 7 kV AC and 2 MHz as highlighted in Fig 3.16.

(a) GRC Polystyrene **(b)** THoogspanning

Figure 4.8: Variable Capacitor Banks

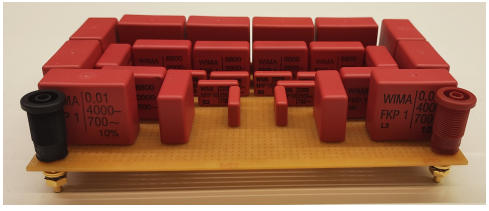


Figure 4.9: Secondary Parallel Compensation Capacitor

4.3. H-Bridge Inverter

In the HV lab, a full bridge PCB is used to realise the inverter needed for the IPT. This inverter has been previously designed, built and tested for the MMC AWG project as highlighted in [77]. For the MMC AWG application, multiple of these boards are used in tandem to create an MMC which can create arbitrary waveforms as controlled by the gate drivers of the individual MOSFETs. The board thus has the additional capability of operating in a closed-loop system and can take switching inputs from both Arduino and Typhoon HIL (optical inputs). The inverter is made of two boards which are the gate driver board and the power board. These boards are detachable from each other. The gate driver board has optical communication through Typhoon HIL which provides the switching information for the full bridge. Alternatively, pulses can be provided by arduino on the power board directly. In this situation, it is necessary to implement the dead time and the phase shift on the arduino itself.

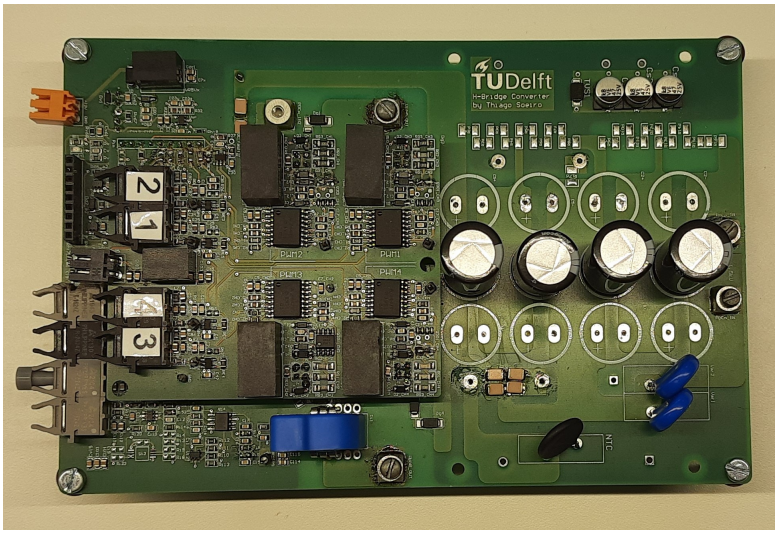
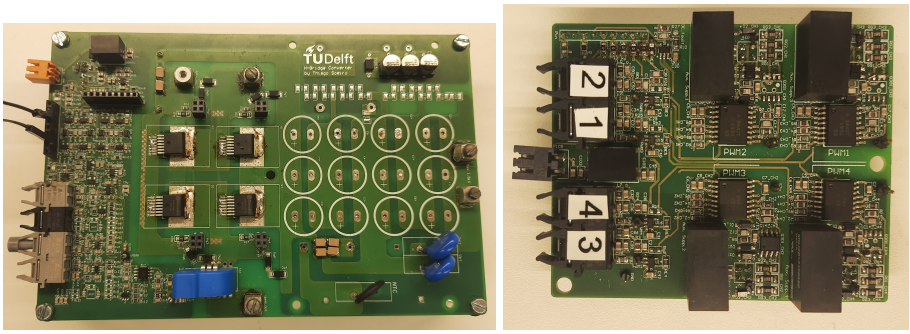


Figure 4.10: H Bridge Inverter

For the HVIPT, the system is operated in an open loop configuration considering that the S-P topology provides a constant voltage at all loads. Moreover, feedback from the HV output side requires optical and grounding isolation which as discussed in Section 2.1 is not addressed in this thesis. The inverter as seen in Fig 4.10 has the Silicon Carbide MOSFET G3R450MT17J [60]. Having rise times and fall times in 10's of nanoseconds makes it suitable for operation at high switching frequencies up to 500 kHz. A high value of the DC Bus capacitance for the HVIPT is not needed as the resonant converter is always operational and there is no considerable need for these capacitors to store charge for pumping into the circuit. Thus, only 4 electrolytic capacitors are kept for the inverter.

An auxiliary supply of 12 V must be provided for the operation of the gate drive

and all the peripherals involved in the board. A separate power supply PE 1536 from Philips is used for providing the voltage needed for the auxiliaries. The clear pin must be pulled to the ground at the input bus to allow the power board to function as intended. However, the clear signal is a result of the fault signal input on a D Flip-Flop. Thus, the clear-to-ground short in the input bus must be removed after the inverter is turned on. Not following the above procedure causes the clear signal to bypass the fault signal and any fault detected by the inverter will not turn the HVIPT off. The fault LED not glowing and the enable pin glowing indicates that the system is functional. However, it is recommended to verify the gate pulses before and after the gate driver.



(a) Power Board **(b)** Gate Drive Board

Figure 4.11: Two boards of the Inverter

The GeneSiC MOSFET has a $15\,\mathrm{V}/-5\,\mathrm{V}$ gate-source driver requirement and the gate driver provides this using an MGJ2D121505SC DC-DC converter which comes with the isolation as required by the power board for the HVIPT. The isolation is also required in a full bridge, as there is the requirement to isolate the gate drivers with different reference points. This requirement is essential as the source of the lower legs is attached to the ground while the source of the upper legs is connected to the output of the full bridge and the drain of the lower legs.

To protect the H-Bridge inverter from high currents which may occur due to faults, a LEM current transducer is used with an overcurrent detection circuit, whose output goes to the gate driver circuit and disables the entire gate driver. This is an essential requirement for a system such as the HVIPT where fault on the load's side can lead to higher input current which could potentially destroy the MOSFET. Therefore, before using the inverter in this setup, it is required to ensure the overcurrent detection circuit is fully functional.

In the current configuration, the current transducer is set to an $5\,\mathrm{A}$ while the MOSFET is rated for $9\,\mathrm{A}$. To use the board for higher currents for the HVIPT, similar T0-263-7 package MOSFETs must be found with a higher current rating and the resistor divider from the LEM transducer must be changed to attain the required current limit. It is also recommended to isolate the kelvin source (KS) from the power source (S) to protect the gate drive circuit from the current surges that can

be expected during the operation of the HVIPT [Fig 4.12]. However, the current inverter used for the HVIPT has the Kelvin and Power source shorted.

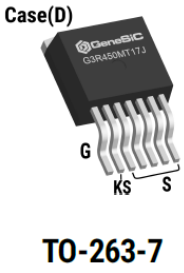
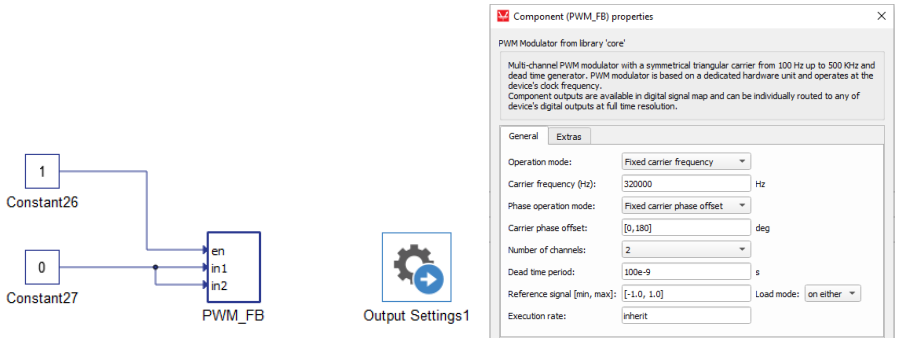


Figure 4.12: Kelvin Source and Power Source in the SiC MOSFET

4.4. Typhoon HIL & Providing Pulses

Typhoon HIL is a control centre environment which is a vertically integrated system engineering toolkit catered for various power engineering needs. Targeted for high-speed hardware in loop applications, this setup also has multiple alternative functions such as software in loop and provides engineers with a way to test their control strategies. Rapid control prototyping is one of the ways it helps engineers to verify and develop better control algorithms [78].

The Typhoon HIL (TIL 402) system in the HV lab provides 32 Digital Outputs (DO) which are provided optically. This is of prime importance for the HVIPT. Using optical methods for communicating signals, there is low latency and easy controllability of parameters as opposed to wired communication such as the ATmega328P in the Arduino. Therefore 4 DO pins are used to provide high-frequency gating pulses (320 kHz) from TIL402.



(a) PWM Input to Full Bridge **(b)** PWM Modulator Settings

Figure 4.13: Typhoon HIL settings for the HVIPT

These pulses are provided using the PWM modulator block where there are

several options for different PWM techniques for power electronic converters [Fig 4.13]. A fixed frequency setup with zero offset is used. There must be a significant dead time to ensure the MOSFET drain-source capacitor discharges, thus enabling ZVS. Considering the values of the capacitance of the MOSFET in the board, a dead time in the range of 25-150 ns can be used. Therefore, it is possible to tune both the frequency and dead time of the inverter with Typhoon HIL making it convenient for prototyping the HVIPT.

4.5. Diode Rectifier

The S-P topology behaves as a voltage source on the output, providing an AC output across the secondary parallel compensation capacitor. A rectifier provides a DC output by filtering the AC component. Operating at 320 kHz the diode rectifier will have short surges of current every cycle to recharge the capacitor, therefore there is a need to have a diode of higher current rating. The SiC diode used for the rectifier is the STTH812DI by ST Microelectronics. This is rated for 8 A current and the goal is to limit the spike current to below 6 A. A spike current during every cycle at 320 kHz means that the SiC diode observes almost rated current flowing through it every cycle which necessitates the use of a heatsink as shown in Fig 4.14. Multiple diodes are used in series to meet the voltage blocking levels of 5.5 kV. The parasitic capacitances of the diodes are connected in series, as shown in Fig 4.14, which is advantageous as the overall parasitic capacitance is reduced [79].

(a) Top View **(b)** Side View

Figure 4.14: Diode Rectifier

The filter capacitor used is 3.3 nF which is formed by connecting three 0.01 µF's in series to achieve the DC blocking voltage capability. Higher capacitor values can be chosen to limit the output voltage ripple, that however comes at a cost ie: higher peak currents through the diode. This is shown in Fig 4.16 where the blue waveform is the diode peak current while the red waveform is the output voltage with a ripple. The purple waveform is the diode blocking voltage.

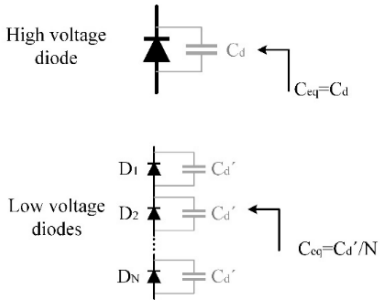
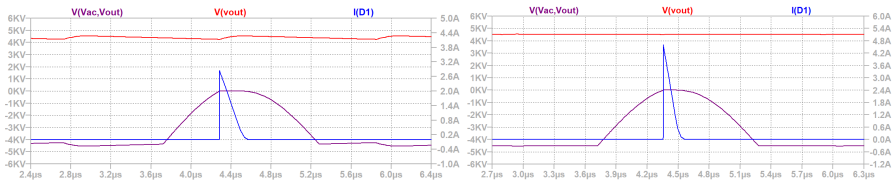


Figure 4.15: Multiple Diodes for the rectifier [79]

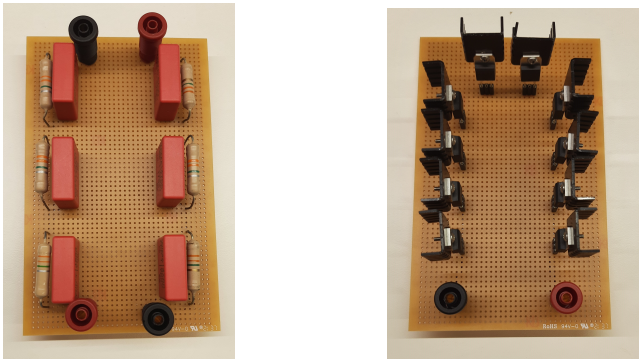


(a) 1 nF Filter Capacitor **(b)** 10 nF Filter Capacitor

Figure 4.16: Diode peak current and Output ripple voltage - Diode Rectifier

4.6. Voltage Multiplier

The 5 kV AC across the secondary compensation capacitor is used as an input for the one-stage multiplier to obtain 10 kV. Similar to the diode rectifier, 10 diodes each rated for 1.2 kV are connected in series to obtain a single diode for the multiplier. Fig 4.17 shows the capacitors and diodes designed for the HV multiplier.

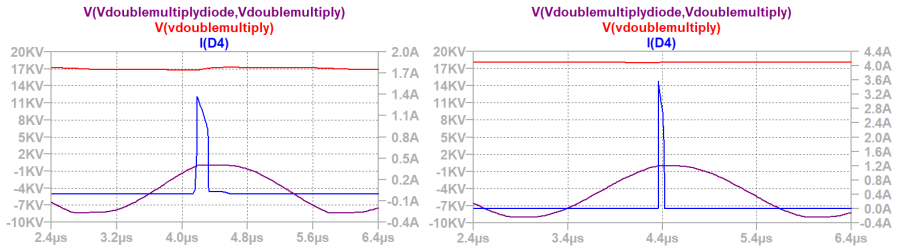


(a) Capacitor **(b)** Diode

Figure 4.17: Voltage Multiplier Components

Similar to the case of the diode rectifier, there is a need to manage the diode

spike currents that charge the capacitors. The filter capacitor for the multiplier is 1.56 nF which is obtained by connecting 3 4.7 nF's in series to achieve the DC blocking voltage capability. Again, higher capacitor values could have been chosen to limit the output voltage ripple, that however comes at a cost ie: higher peak currents through the diode. This is shown in Fig 4.18 where the blue waveform indicates the diode peak current and the red waveform is the output voltage which has a certain ripple. The purple waveform is the diode blocking voltage.

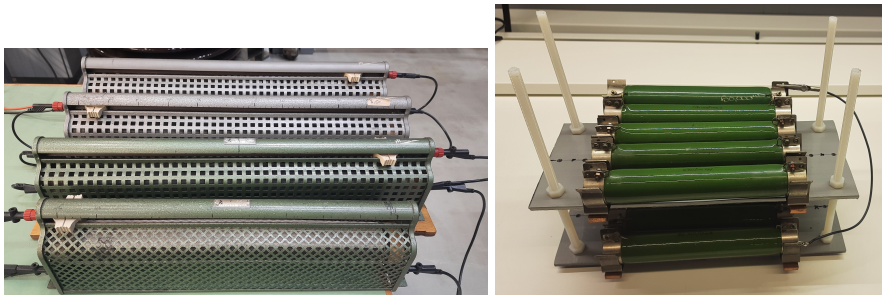


(a) 1 nF Filter Capacitor **(b)** 10 nF Filter Capacitor

Figure 4.18: Diode peak current and Output Ripple voltage - Voltage Multiplier

4.7. Source, Load & Measuring HV

A DC source is used to power the inverter for the HVIPT. The supply used for this purpose is the delta electronics bidirectional power supply SM 1500-CP-30 [80], which is capable of providing the required voltages and currents. Power limit of 1.5 kW is kept and voltage is not risen to more than 400 V. For low-voltage testing (below 30 V) in the initial phases, the BaseTech BT-305 supply is used as the power supply.



(a) Variable Resistor **(b)** Resistor Bank

Figure 4.19: Available Loads at HV Lab

A bank of high-power adjustable resistors as shown in Fig 4.19a is used to obtain a maximum of 20 kΩ required for testing the HVIPT. These resistors can be varied to obtain the required resistance for testing at different loads. For loads greater

than $20\,k\Omega$, a resistor bank as shown in Fig 4.19b is used for testing.

To measure the voltages on the primary low voltage side, the differential probes TA057 of pico technology are used and the current probe N2783B by keysight is used, however, configuring it to oscilloscopes requires the keysight N2779A power supply. For voltages on the HV side the Tektronix probe P6015A is used as shown in Fig 4.20. All the voltages measured with this probe are with respect to ground, therefore it must be noted that this HV probe is not a differential probe. For rated load tests, the HV probe must be connected across the rheostat. For no-load tests, the connectors are left open and the probe is connected across the open points to detect the no-load voltage.

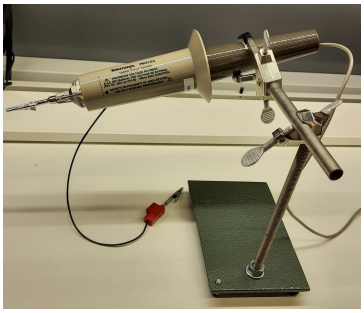
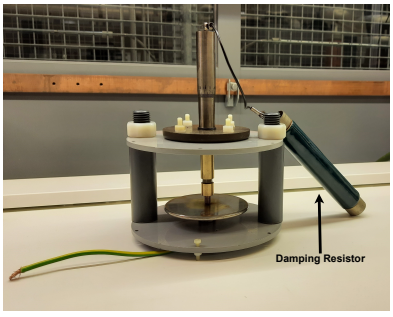
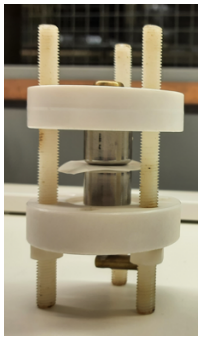


Figure 4.20: HV Probe

For DC tests regarding on breakdown of air, the HV probe is connected outside the dampening resistor with the other end at the ground as shown in Fig 4.21a. The damping resistor is required to limit the sudden current increase when the load moves from a no load to a short circuit condition. The setup in Fig 4.21b can be connected parallel to the secondary capacitor to conduct high-frequency AC surface discharges on the dielectric.



(a) DC Breakdown of Air



(b) AC Discharge Test on Teflon

Figure 4.21: Setup for Dielectric Tests

In Fig 4.22 the test setup is shown with all the components mentioned above in

this chapter. Fig 4.23 highlights the way these components are connected to form the HVIPT. The testing process and results will be discussed in the next chapter.

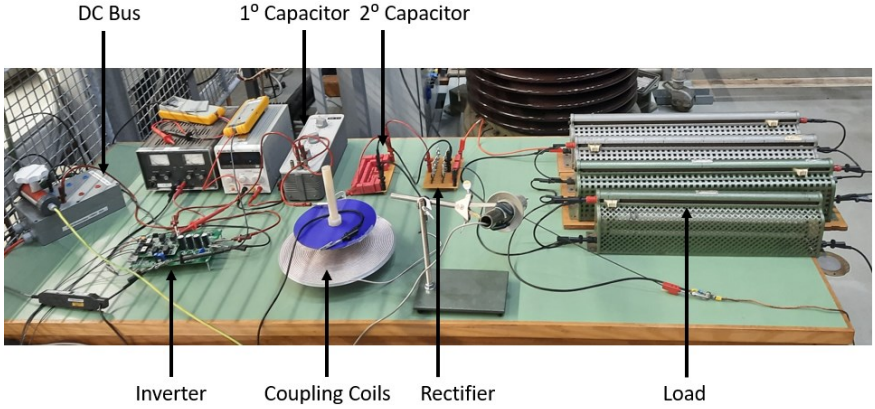


Figure 4.22: Setup of the HVIPT Prototype

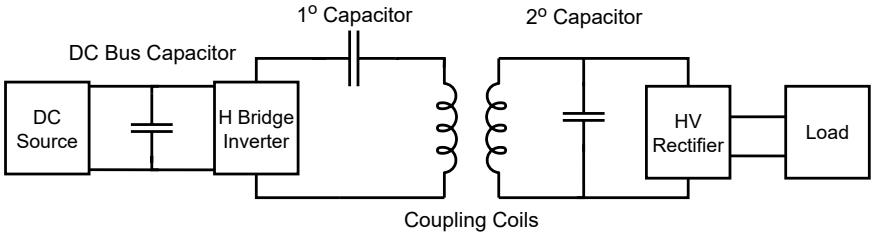


Figure 4.23: Circuit Diagram of the HVIPT Prototype

*In this chapter, the development of the prototype is highlighted. A 400*0.1mm diameter litz wire is used to design primary and secondary coils with a high-quality factor. The variable capacitor banks are used to tune the resonant converter to operate in ZVS. The inverter used for the HVIPT is capable of short-circuit protection with an overcurrent transducer. Typhoon HIL is used to provide the required frequency and deadtime. Finally, the HV rectifier is developed using filter capacitor as* 3.3 nF *and the HV multiplier with the capacitor as* 1.56 nF*. The setup of the HVIPT is highlighted in Fig 4.22.*

5

Testing

This chapter provides the methodology of the testing process followed by the results of the tests done on the HVIPT. These results are then compared with simulations. With these comparisons, conclusions are then drawn on the built prototype. Since the setup involves dealing with HV there are certain safety processes followed, which will be highlighted. Based on the results of the IPT testing, several conclusions will be drawn which can be found in the final chapter of this thesis.

5.1. Introduction

The components involved in the testing are all described in the previous chapter. In this chapter initially, a series of Low Voltage (LV) tests are done to understand the behaviour of the S-P IPT. After deciding the component parameters, the HV tests are done to obtain the desired $5.5\,\text{kV}$ with the rectifier and $10\,\text{kV}$ with the multiplier. Thereafter, tests such as the rated load, no load and breakdown tests are performed with the HVIPT to understand its behaviour as a DC test source.

5.2. LV Testing

The goal of this set of tests is to understand and evaluate the working of the chosen topology with various parameters and how they affect the operation of the power supply. Eventually, a particular setup is chosen and finalised for the HVIPT. At these lower voltages, the variable capacitor box in Fig 4.8b is used as the secondary parallel capacitor with the output AC voltage at the secondary being lower than $500\,\text{V}$. Unless otherwise mentioned the following parameters in Table 5.1 are used for the LV tests. The LV tests are done with the diode rectifier on the secondary side.

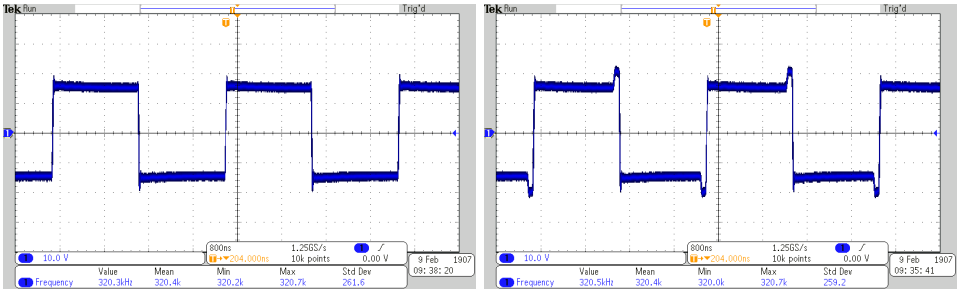
5.2.1. H Bridge inverter test

Firstly, the working of the H Bridge has to be verified at a no-load condition. For this, the pulses are provided from typhoon HIL and the no-load output voltage of

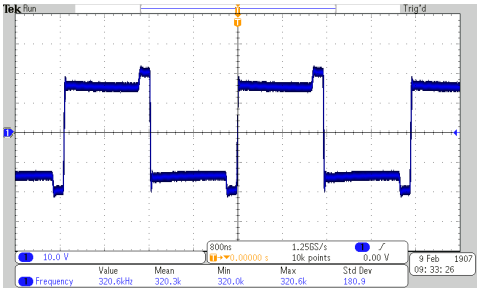
Table 5.1: Parameters for Low Voltage tests

Parameters	Value
Primary Inductance	13 µH
Secondary Inductance	125 µH
Coupling Coefficient	0.25
Switching Frequency	320 kHz
Distance between Coils	65 mm
Input voltage	15 V
Load Resistance (Rac)	20 kΩ
Filter Capacitor	3.3 nF

the inverter is measured at different deadtimes [Fig 5.1]. The overshoot of the output voltage during the deadtime is attributed to the forward voltage drop of the body diode in the conducting SiC MOSFET's. The H-Bridge, therefore, performs as expected, providing a 15 V high-frequency square wave output for a 15 V DC Bus.



(a) 0 ns deadtime **(b)** 100 ns deadtime



(c) 200 ns deadtime

Figure 5.1: No load test of the inverter

5.2.2. Overcurrent Test

Before conducting any tests on the H-Bridge inverter, there is a need to study the reaction time of the overcurrent protection. This is done to protect the MOSFETs in case of over-current conditions in the HVIPT. The design of this protection is shown with the schematics in Appendix B. A diagram highlighting the test circuit is shown in Fig 5.2. A relay is controlled by an Arduino to detect the time instant when over current is applied through the LEM transducer. The overcurrent limit set for the transducer is 5 A. A $0.22\,\Omega$ series resistor is connected to detect the current. The Hall effect-based LEM transducer provides a particular voltage which is then compared with reference voltages in the overcurrent detection circuitry. Finally, based on detecting an overcurrent situation, a fault signal is sent gate driver to prevent the generation of gate pulses and switch off the HVIPT. The clear signal however must not be shorted to ground, enabling the fault signal to operate as explained above.

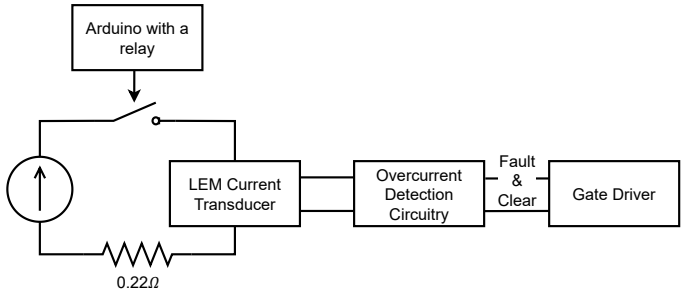
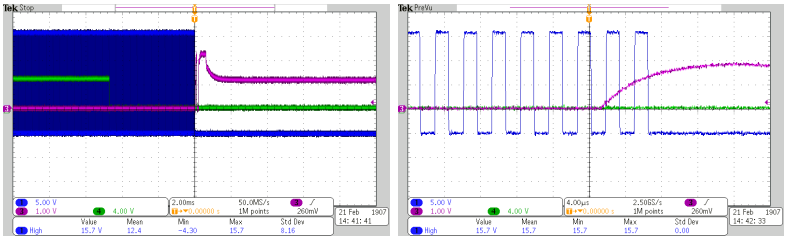


Figure 5.2: Overcurrent Test Schematic

In Fig 5.3, the switching off of gate pulses is observed when an overcurrent of 5.5 A is pushed by the current source. The green waveform in Fig 5.3a is the arduino signal which triggers the relay. The purple waveform is the relay response to the trigger which has a considerable delay of 5 ms. However, in Fig 5.3b an extremely fast response time of maximum 1 µs is observed for the gate pulses to switch off when the current crosses 5 A.



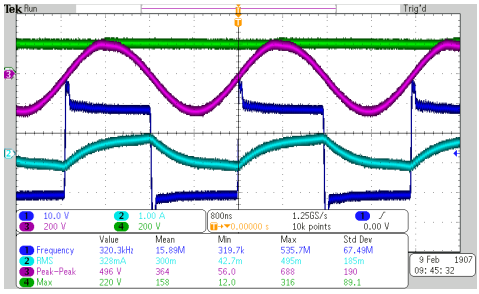
(a) Response of Gate Driver **(b)** Response Time of 1 µs

Figure 5.3: Overcurrent Test

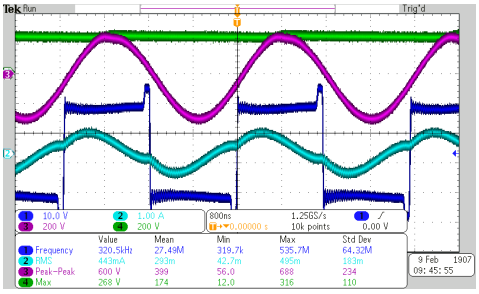
5.2.3. ZVS tests

The condition for obtaining ZVS in an IPT is that the input impedance must be inductive. This corresponds to the input current lagging the input voltage from the H bridge. The way to detect ZVS during testing is to obtain the output voltage and current from the H Bridge. If the input current is inductive, no offset is seen in the H Bridge output voltage before the transition to the other leg during the dead time. This is so because the drain-source capacitor of the non-conductive leg's MOSFET is discharging itself with the inductive current. However, if the input impedance is not inductive then the current can only flow through the MOSFETs of the conductive leg during the deadtime. This leads to the additional voltage equivalent to the body diode drop of the MOSFET at the H-Bridge output voltage for the duration of the dead time. Additionally, a lagging current highlights ZVS while a leading current indicates a lack of ZVS.

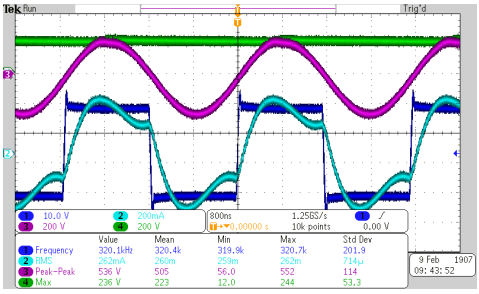
The following colour codes must be followed for the LV tests. The dark blue waveform is the input voltage for the IPT which is seen as the output of the high-frequency H Bridge inverter. The light blue waveform is the input current into the IPT which is again coming from the inverter. Finally, the pink and green waveforms are the AC output across the secondary capacitor and rectified DC output respectively.



(a) 1.7 nF - ZVS



(b) 1.8 nF - No ZVS



(c) 1.75 nF - ZVS

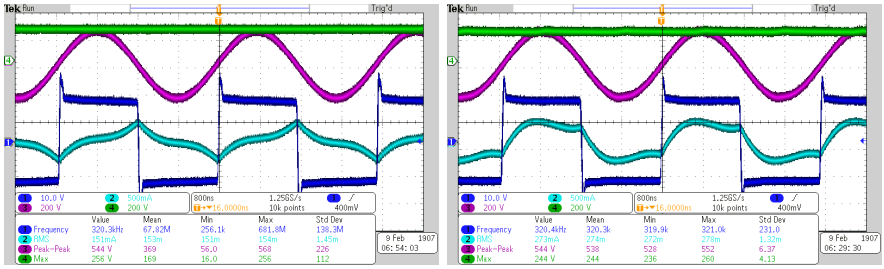
Figure 5.4: ZVS by tuning secondary parallel capacitor C_s

As observed from Fig 5.4, obtaining ZVS for the HVIPT is highly sensitive and

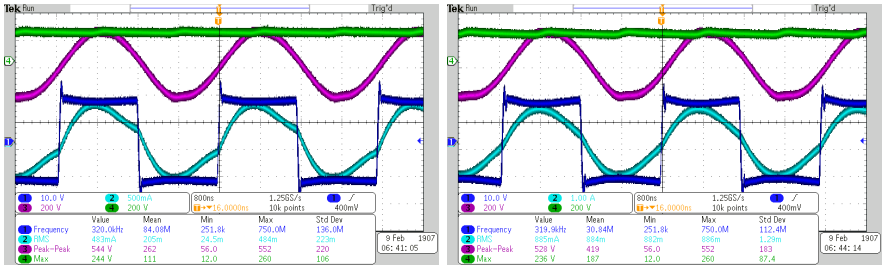
dependent on the exact value of the secondary compensation capacitor (C_s). In Fig 5.4b the MOSFETs do not have ZVS as the input current is leading the inverter voltage. However, slightly changing C_s to $1.75\,\text{nF}$ offers resonance with perfect compensation and ZVS with much lower lagging input current of $262\,\text{mA}$ [Fig 5.4c]. Reducing the C_s even more to $1.7\,\text{nF}$ in Fig 5.4a causes the system to have a much larger inductive input impedance which is seen by the increase in lagging input current to $326\,\text{mA}$ for the same output load and output voltage. However, interesting to note is that the MOSFETs still operate with ZVS in Fig 5.4a, as the input current is still inductive.

5.2.4. Load tests

In Fig 3.6b the input currents are simulated for varying AC output loads. As the resistive load for the HVIPT moves from a heavier load ($5\,\text{k}\Omega$) to a lighter load ($30\,\text{k}\Omega$), the input currents get more inductive as the mutual coupling inductor dominates over the connected load [Fig 3.14]. Eventually, at no load, a $90°$ phase shift can be seen between the H bridge voltage and input current.



(a) No Load **(b)** $20\,\text{k}\Omega$ Load



(c) $10\,\text{k}\Omega$ Load **(d)** $5\,\text{k}\Omega$ Load

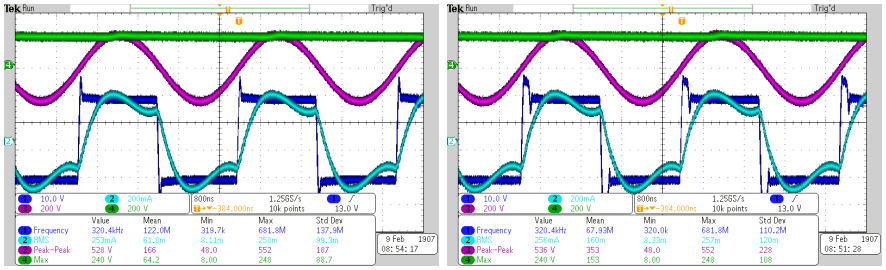
Figure 5.5: Load tests on the HVIPT

Results similar to simulation are seen in the LV tests where, as the load resistance is increased, the input current starts lagging further, with the input impedance getting increasingly inductive. This also means that more of the input current is lost as circulation currents when load resistance is increased. Eventually in the case of no load in Fig 5.5a all the input current is used as the circulation current in

the S-P IPT. Interestingly this IPT topology also works without the HV rectifier and similar load test results can be seen with an AC resistive load.

5.2.5. Deadtime tests

In Eq 3.19 there is a minimum dead time required to meet the ZVS requirement of the IPT. Having a longer dead time would lead to the complete discharge of the drain-source capacitor of the MOSFET. Therefore, it is interesting to have some information regarding the behaviour of the HVIPT at different deadtimes.



(a) 100 ns **(b)** 200 ns

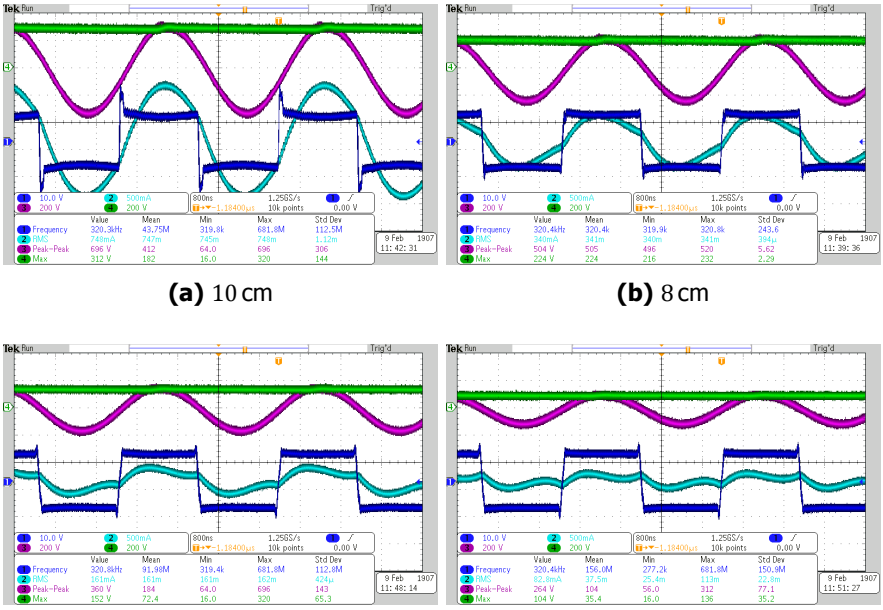
Figure 5.6: LV tests of the HVIPT at different deadtimes

In Fig 5.6 the behaviour of the IPT can be seen at deadtimes of 100 ns and at 200 ns. The overshoot in either case during the deadtime is due to the reverse body diode drop of the conducting MOSFET's. Upon the end of the deadtime, these MOSFETs begin conducting normally and therefore the offset ceases to exist past the deadtime. In Fig 5.6b a small dip in the inverter voltage is observed at the end of the deadtime, indicating that the drain-source capacitor of the MOSFET has totally discharged before the deadtime has ended. It is also observable that the input current of the inverter has switched polarities before the deadtime has ended. This means that the body diode of the blocking MOSFETs can no longer conduct current and the MOSFET must be switched on to enable the flow of current into the IPT. Increasing deadtime beyond this value leads to no benefit for the HVIPT and therefore this is the maximum deadtime the system can operate at.

5.2.6. Coupling coefficient tests

In the S-P topology, the load invaraint gain is inversely proportional to the coupling coefficient [Eq 3.17]. Therefore, upon varying the distance between the primary and secondary coils the output voltage varies and thus a particular distance (coupling coefficient) can be set to obtain the desired output voltage. However, it must be noted that below a particular coupling coefficient, the mutual inductance gets minimized to the extent where the circulation current increases considerably, after which there is no benefit in obtaining a higher voltage from an efficiency point of view.

In Fig 5.7 as the distance between the coils reduces, the coupling coefficient increases and the output voltage of the S-P topology decreases. The input voltage



(a) 10 cm **(b)** 8 cm

(c) 6 cm **(d)** 4 cm

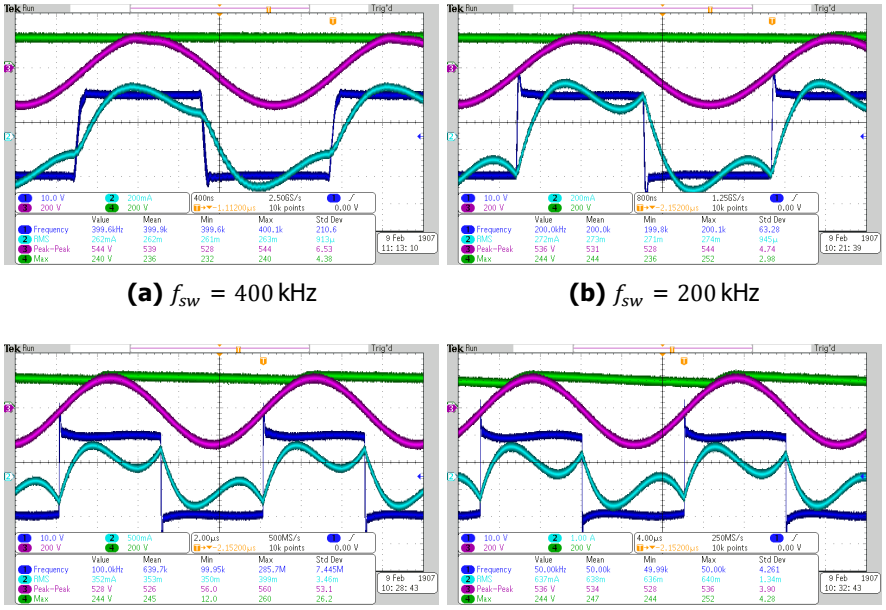
Figure 5.7: Change in coupling coefficient

for this analysis has been reduced to 10 V. An interesting thing to note is that as the voltage increases by a factor of 2 between Fig 5.7c and Fig 5.7a the input current increases by a factor of 4.5, proving the above hypothesis that as the coupling coefficient reduces, the circulation current increases leading to an increase in input current. This increase in input current however leads to a reduction in efficiency of the IPT. Therefore, distance between the coils can not be increased infinitely and for the HVIPT a lateral distance of 6.5 cm is considered.

5.2.7. Frequency tests

In Fig 3.15, it can be shown that upon increasing the switching frequency for a particular load, the input current reduces as the system sees a higher load with an increase in mutual inductance. Correlating with Fig 3.14, a conclusion can be drawn that an increased frequency reduces the circulating current entering the mutual inductance, thereby reducing input current.

In Fig 5.8, the HVIPT is tested at various switching frequencies at the given load of 20 kΩ and input voltage of 15 V. The compensation capacitors are varied accordingly for the different frequencies. In Table 5.2 the input currents at these frequencies are shown. From Table 5.2, it can be safely concluded that an increase in switching frequency improves efficiency, especially at lighter loads of 20 kΩ. However, this improvement is not that significant as we move from 200 kHz to 400 kHz. Thus, considering the lifetime and SOA of switching MOSFETs, diodes



(a) f_{sw} = 400 kHz **(b)** f_{sw} = 200 kHz

(c) f_{sw} = 100 kHz **(d)** f_{sw} = 50 kHz

Figure 5.8: Switching frequency test

and litz wire, a switching frequency of 320 kHz is chosen for the HVIPT.

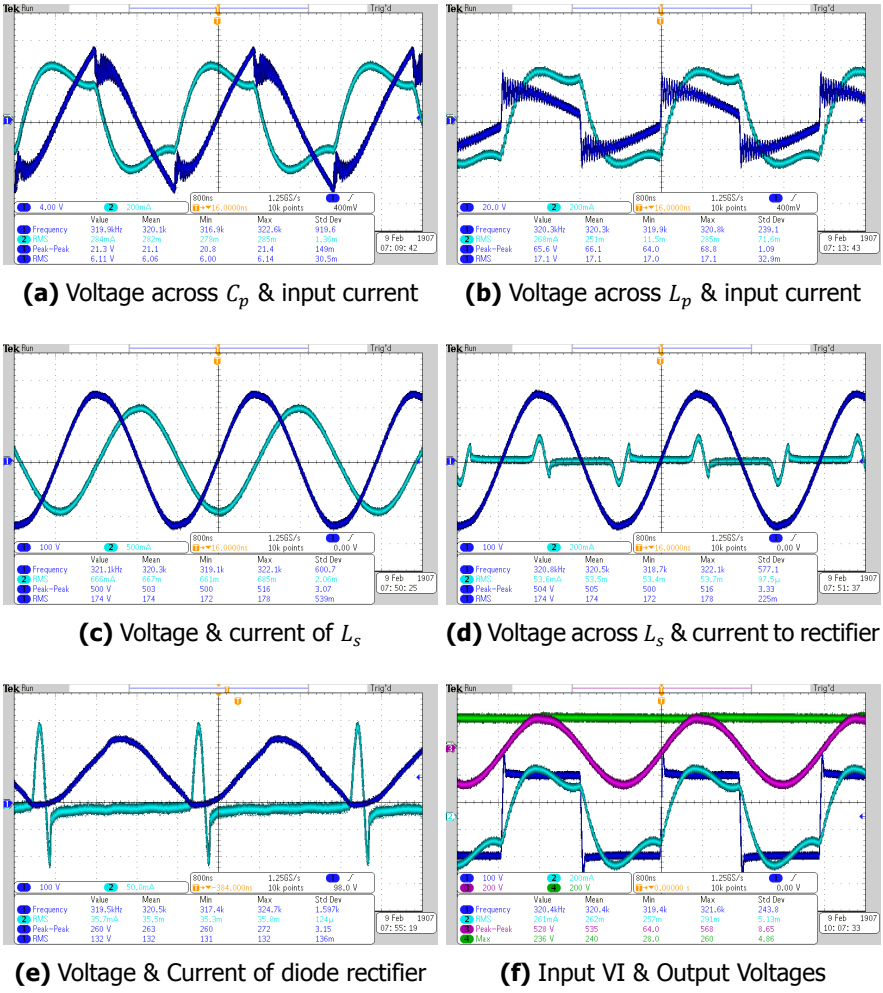
Table 5.2: Input Current v/s Switching frequency - LV Test

Frequency	Input Current (rms)
50 kHz	0.637 A
100 kHz	0.352 A
200 kHz	0.272 A
400 kHz	0.262 A

5.2.8. Final test results at 15 V input

Considering the results obtained from theory, simulation, mathematical model and finally the LV tests, Table 5.3 indicate the final parameters for the HVIPT prototype. In Fig 5.9 waveforms across all the components involved in the S-P topology are shown. These waveforms are similar to the waveforms obtained with the mathematical model [Fig 3.5].

With these results [Fig 5.9], the HV tests can be done. It must be noted that each of the profiles shown above will be 20x when the input voltage is increased 20 times from 15 V to 300 V. Apart from the output voltage, input voltage and input current, waveform across the other components cannot be measured during the HV tests as the probes are not rated for measurement at those conditions.



(a) Voltage across C_p & input current

(b) Voltage across L_p & input current

(c) Voltage & current of L_s

(d) Voltage across L_s & current to rectifier

(e) Voltage & Current of diode rectifier

(f) Input VI & Output Voltages

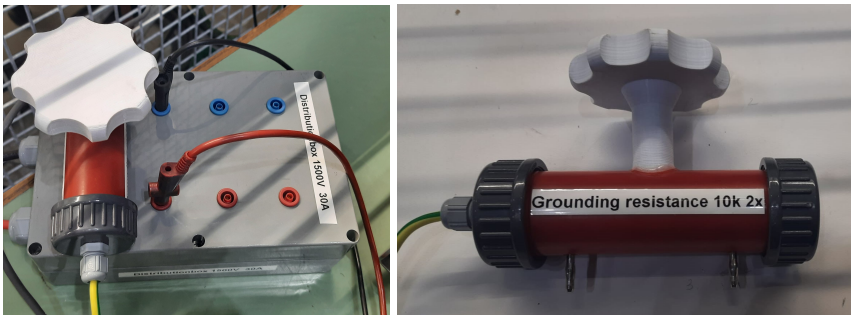
Figure 5.9: Final LV tests

Voltages across the primary capacitor C_p and primary inductor L_p are not sinusoidal as shown by Fig 5.9a and Fig 5.9b. This however has no bearing on the output voltage across the secondary inductor L_s which is purely sinusoidal. This voltage serves as the AC output voltage of the IPT because the secondary capacitor C_s and the load is parallel to L_s. Accordingly, a sinusoidal output AC and a flat DC voltage are observed from the pink and green waveforms in Fig 5.9f respectively, The light blue waveform is the input current. In Fig 5.9d and Fig 5.9e the current into the diode rectifier is shown. As opposed to simulation results in Fig 3.11, a negative spike in diode current is observed. This is attributed to the parasitic capacitances in the diode are not modelled in simulation. The use of SiC diode with minimal reverse recovery time and charge is therefore justified for the HVIPT.

Table 5.3: Parameters for HV tests

Parameters	Value
Primary Inductance	13 µH
Secondary Inductance	125 µH
Coupling Coefficient	0.25
Distance between Coils	6.5 mm
Switching Frequency	320 kHz
Primary Capacitance	19 nF
Secondary Capacitance	1.9 nF
Filter Capacitance	3.3 nF
Rated Load	18 kΩ
Rated Power	1.25 kW
Deadtime	100 ns

5.3. Safety Consideration



(a) Distribution Box **(b)** Grounding Resistor

Figure 5.10: Safety setup for the SM 1500-CP-30

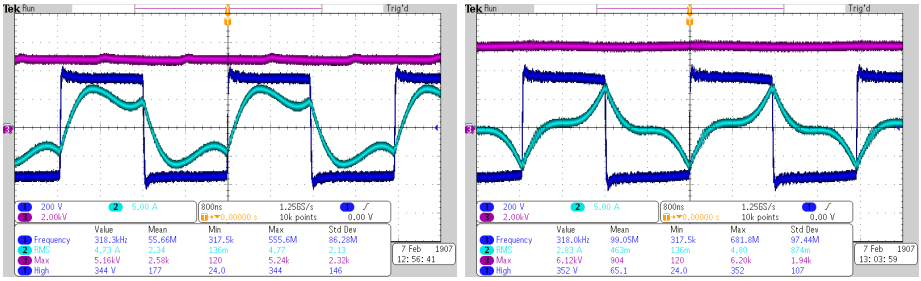
Operating with HV comes with certain safety requirements for the personnel and equipment. A grounding stick is necessary with the damping resistor to tap all the exposed HV points such as to prevent the existence of any space charges as the system generates DC power. Secondly, a distribution box is used for the delta electronic supply for a neat and clean connection to the input of the inverter. To remove any residual currents built up in the box or the inverter, a high grounding resistor of 20 kΩ is connected across the positive and negative terminals coming out of the distribution box as shown in Fig 5.10.

Finally, the setup is used in a cage with the interlock connected to the delta electronic (SM 1500-CP-30) supply. A setup to activate the interlock manually is also built. Therefore opening the cage to access the HVIPT, automatically shuts down the power to the HVIPT. However, the system must be accessed only after connecting the grounding resistor to the distribution box and after tapping all the exposed points with the grounding stick.

5.4. HV Tests

The HV tests are done on the S-P IPT based on the parameters in Table 5.3. As the input voltage is increased from 15 V to 350 V the output voltage increases from 244 V to 5.2 kV respectively. This indicates the working of the HVIPT with S-P topology at the rated load as desired. The results as shown in Fig 5.11 match the waveforms seen from the simulation and the mathematical model mentioned in Fig 3.11 and Fig 3.5.

In Fig 5.11a the input voltage of 350 V is provided at a rated load of 18 kΩ. The dark blue waveform indicates the input voltage to the IPT and the light blue waveform indicates the primary input current from the high-frequency inverter. The pink waveform shows the DC output of the HV rectifier. Considering an input current of 4.73 A, the input and output powers are 1655 W and 1469 W respectively [Fig 5.11b], leading to an efficiency of 88%.



(a) Rated Load **(b)** No Load

Figure 5.11: HVIPT test at 350 V input

In Fig 5.11b, a no-load test is conducted with an input voltage of 350 V. A phase shift of 90° between the input voltage and input current can be seen, highlighting the load as seen by the inverter is completely inductive in nature. Therefore, the input current in this situation facilitates the circulating current requirement in the resonant converter. The input current has fallen to 2.83 A which is the current required at no load to achieve a high DC output. Input power at no load is around 160 W which is almost equivalent to the power lost at rated load. An output voltage of 6.12 kV is seen, giving a load regulation of around 18% between no load and rated load.

An important aspect to be measured is the magnetic field in the surrounding environment. For this, the Narda LT-400 exposure level tester [81] is used with the magnetic field probe as shown in Fig 5.12. The results of the surrounding magnetic field at different distances from the central axis of the coils are shown in Table 5.4. The major component of the magnetic field is in the z-axis between the coils, as all the flux sent by the primary coil is captured by the secondary coil.

The general public exposure limit to time-varying magnetic fields as per the ICNIRP guidelines at this frequency range is around 27 µT [8]. Therefore, it is recommended to be at least 30 cm away from the centre of the coils.

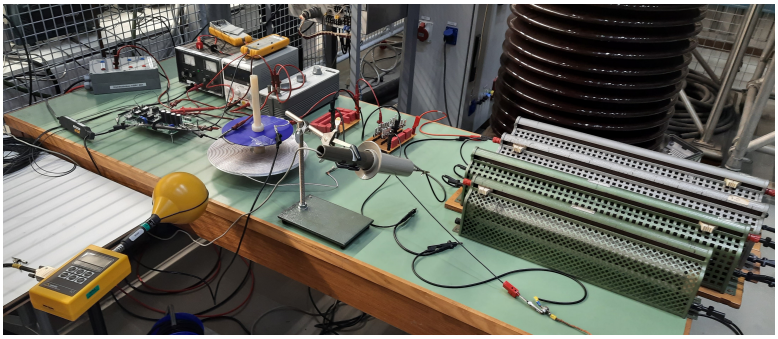


Figure 5.12: Magnetic Field Testing of the HVIPT

Table 5.4: Magnetic Field Measurements

Distance	Magnetic Field
20 cm	78.7 µT
25 cm	36.2 µT
30 cm	23.6 µT
35 cm	15.2 µT
40 cm	11.4 µT
45 cm	7.5 µT
50 cm	6.1 µT

5.5. Efficiency analysis

In the HVIPT, there are primarily 3 sources of power loss. These are the litz wire conduction loss of the coils, the diode rectifier loss and the inverter MOSFETs loss. Loss arising due to the ESR of the compensation capacitors is minimal compared to these 3 sources and is thus ignored for efficiency analysis. In the previous section, a total loss of 180 W is observed when the HVIPT operates at a load of 18 kΩ with an efficiency of 88%. In this section, power loss will be split into three sources.

The conduction losses of the primary and secondary coils are evaluated by multiplying the AC resistance of each harmonic with the square of the rms current at that harmonic [Eq 5.1]. The AC resistance of the primary and secondary coils are 0.16 Ω and 0.73 Ω respectively at 320 kHz.

$$P_{coil} = \sum_{h=1,3,5..}^{\infty} I_h^2 \times R_{ac(h)} \tag{5.1}$$

The losses of the diode rectifier are obtained by the following formula shown in Eq 5.2 [61]. It is important to note that this loss considers only the conduction loss and not the reverse recovery loss which is minimal in a SiC diode.

$$P_{diode} = 1.5 \times I_{F(AV)} + 0.05 \times I_{F(RMS)}^2 \tag{5.2}$$

Finally, the turn-off losses of the inverter MOSFET's are estimated by multiplying energy dissipated during switching [60] with the switching frequency. The conduction losses are obtained by multiplying the square of rms current with the on-state resistance. The sum of these losses is multiplied by 4 to obtain the overall loss of the switches in the H Bridge inverter as shown in Eq 5.3.

$$P_{MOSFET} = 4 \times (I^2_{F(\mathrm{RMS})} R_{on} + (E_{off} - E_{oss}) f_{sw}) \tag{5.3}$$

The overall losses in the HVIPT are shown in Table 5.5. The circulating current flowing through the secondary coil and secondary compensation capacitor is the major source of loss in the HVIPT, taking upto 79% of all the losses [Fig 5.13].

Table 5.5: Power Loss in the HVIPT

Loss Component	Loss
Diode Rectifier	9 W
Primary Coil Conduction	6 W
Secondary Coil Conduction	125 W
MOSFET Conduction	12.5 W
MOSFET Turnoff	5 W
Total Loss	157.5 W

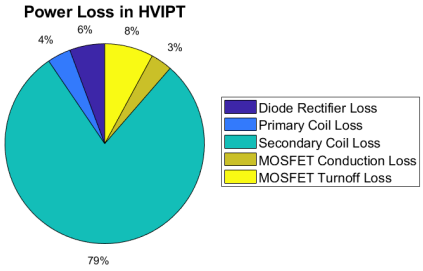


Figure 5.13: Power Loss Distribution in the HVIPT

5.6. DC Testing with discharges - no load to rated load

The setup shown in Fig 4.21a is used with the HVIPT to produce breakdown of air and create discharges across the air gap present. A damping resistor of $20\,\mathrm{k}\Omega$ is used. From a load point of view, the setup undergoes variation from a no load to a rated load ($20\,\mathrm{k}\Omega$) condition. This is better understood from Fig 5.14 where the air is the medium between the electrodes and when air breaks the test object begins to conduct with a damping load resistor of $20\,\mathrm{k}\Omega$. The results from tests on the HVIPT is shown in Fig 5.15a and is verified by simulations in Fig 5.15b. The drop in

output voltage during the switchover from no load to rated load explains the load regulation of the HVIPT which is found to be around 18%.

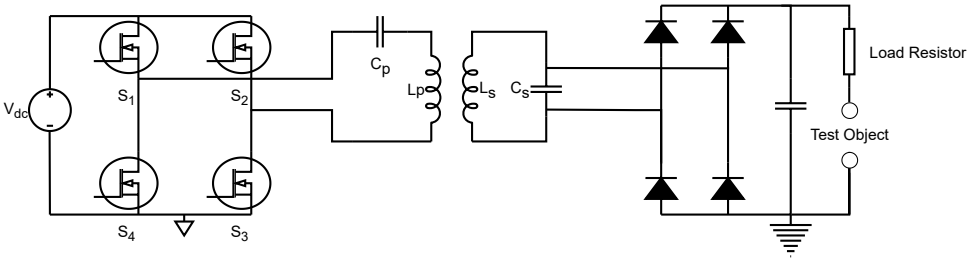
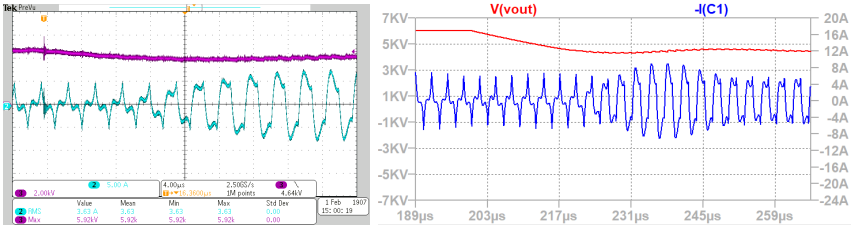


Figure 5.14: Circuit Diagram for Breakdown of Air



(a) Test **(b)** Simulation

Figure 5.15: Breakdown test

5.7. AC Testing with discharges - capacitive load

The setup shown in Fig 4.21b is used with the HVIPT to produce surface discharges on Teflon . From a circuit point of view, this load is viewed as a capacitor as shown in Fig 5.16. The discharges conducted on the dielectric are at a high frequency of 320 kHz.

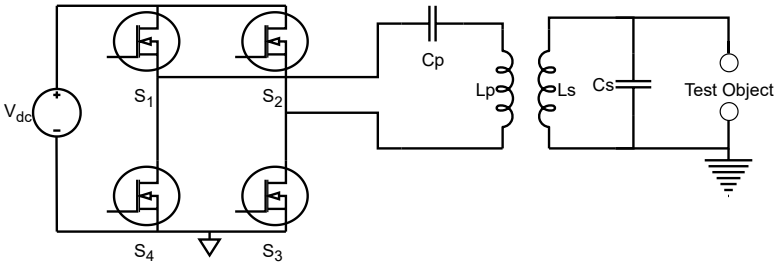


Figure 5.16: Circuit Diagram for Surface Discharges

In Fig 5.17, surface discharges are produced with the HVIPT on Teflon at an

input DC voltage of 200 V and an output AC voltage of 4 kV. The difference in the input current to the HVIPT is shown in Fig 5.18. This change in input current is explained by modelling the test object as a parallel capacitor to the secondary compensation capacitor C_s. Therefore, the test object changes the operating point of the resonant converter. A simple rule of thumb for testing dielectrics with the HVIPT is that the capacitance of the test object must be lesser than 10% of the secondary compensation capacitor C_s, to prevent the resonant converter from going off-resonance and out of ZVS. The pink waveform in Fig 5.18 shows the AC voltage across the test object.

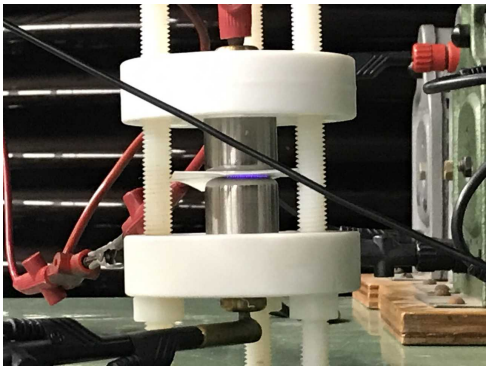
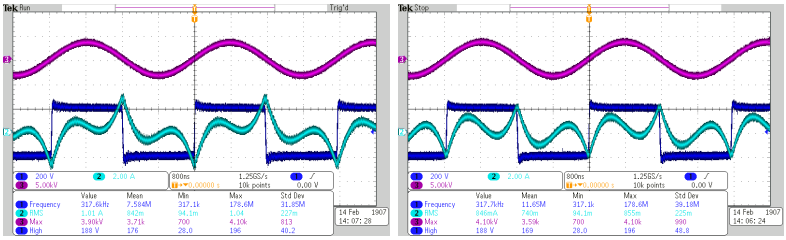


Figure 5.17: Surface Discharges on Teflon



(a) Without Discharge **(b)** During Discharge

Figure 5.18: AC Discharges Waveform

5.8. Voltage Multiplier Test

The HV tests until here were with the diode rectifier. However, it is desirable to obtain a higher DC voltage during rectification. Using the Greinacher rectifier highlighted in [34] the AC voltage across the secondary capacitor is rectified to a higher DC voltage. In Fig 5.19 a one-stage multiplier is shown, which provides a rectified DC voltage of two times the AC voltage. Having an n-stage multiplier gives 2*n times the AC voltage as the DC rectified voltage. Thus, in this section, the HVIPT is tested with a one-stage multiplier to obtain 10 kV, from a 350 V input.

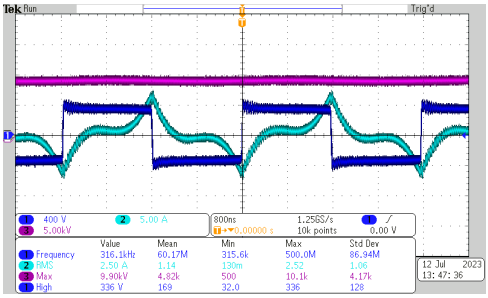


Figure 5.19: HVIPT Test with the Greinacher multiplier

These tests are done at no load, as the high ohmic ($>100\,\mathrm{k\Omega}$) resistors to dissipate powers north of $1\,\mathrm{kW}$ do not exist in the HV lab. The input rms current of around $2.5\,\mathrm{A}$ is observed, which is similar to the no-load test for the diode rectifier in Fig 5.11b. An input current profile similar to Fig 5.11a is expected when a rated load is connected across the HVIPT with the multiplier.

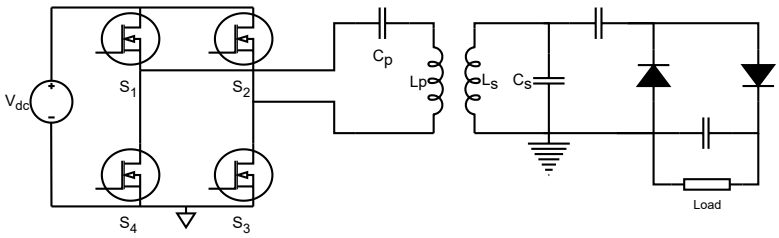


Figure 5.20: One Stage Multiplier

In this chapter, the process of tuning the secondary capacitor using the variable capacitor bank is shown. The secondary capacitor must be within $250\,\mathrm{pF}$ *of the calculated value to operate at the highest efficiency with ZVS. A deadtime of* $100\,\mathrm{ns}$ *is chosen for this topology to allow ZVS. A distance of* $6.5\,\mathrm{cm}$ *is chosen between the coils to enable high voltage gain while keeping efficiency greater than 80%. A significant reduction of 2.5 times in input current is observed as the switching frequency is increased from* $50\,\mathrm{kHz}$ *to* $400\,\mathrm{kHz}$ *for the same load. Therefore, a switching frequency of* $320\,\mathrm{kHz}$ *is used for the HVIPT. The developed HVIPT performs well to provide* $1.5\,\mathrm{kW}$ *at* $5.2\,\mathrm{kV}$ *DC. Load regulation of around 18% is observed with the system providing* $6.12\,\mathrm{kV}$ *at no load with the diode rectifier. The efficiency of the formed supply is 88% with the major loss component being the secondary inductor conduction loss. The setup is also used to perform DC breakdown tests and high-frequency AC tests with surface discharges on dielectrics.*

6

Multiple Output

This chapter provides an introduction of modelling a multi-receiver S-P IPT for the CHB AWG. Coils for the multi-receivers are developed and tested to verify the coupling behaviour across the multi-receiver IPT. A 2-receiver and 3-receiver model is developed in this chapter.

For the CHB AWG there is a requirement to have multiple isolated DC sources. With a multiple receiver based IPT system, isolated DC sources can be obtained from a single transmitter. Using the S-P topology for this setup provides a high voltage gain with load invariant voltage, which is sufficient for the CHB AWG. In this chapter, three receiver coils are constructed to understand the operation of a multi-receiver IPT. In Fig 6.1, the primary and secondary coils are shown and the specifications of these coils are shown in Table 6.1

Figure 6.1: Secondary and Primary Coils

Modelling these receiver coils is not straightforward as they have mutual inductances across them. Therefore, it is necessary to prove that the coupling coefficient between the receiver coils is negligible compared to their coupling coefficients with

Table 6.1: Inductances in the Multi Coil IPT

Coil	Inductance	Resistance	SRF	Cparasitic
Primary (L_p)	45.3 µH	0.233 Ω	3.6 MHz	42 pF
Secondary 1 (L_{s1})	175 µH	1.22 Ω	2.3 MHz	26 pF
Secondary 2 (L_{s2})	153 µH	1.07 Ω	2.5 MHz	26 pF
Secondary 3 (L_{s3})	144 µH	0.97 Ω	2.6 MHz	25 pF

the primary single transmitter. This can be visualised in Fig 6.2 where it is necessary to prove M_{12}, M_{23} and M_{31} are considerably negligible to M_{p1}, M_{p2} and M_{p3}. Table 6.2 shows that the coupling coefficients of the secondary coils with the primary transmitter are around 30x higher than the coupling coefficients of the secondary coils amongst each other.

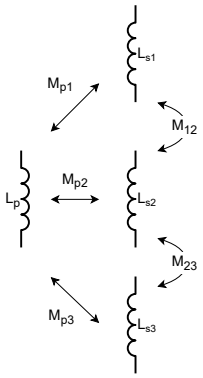


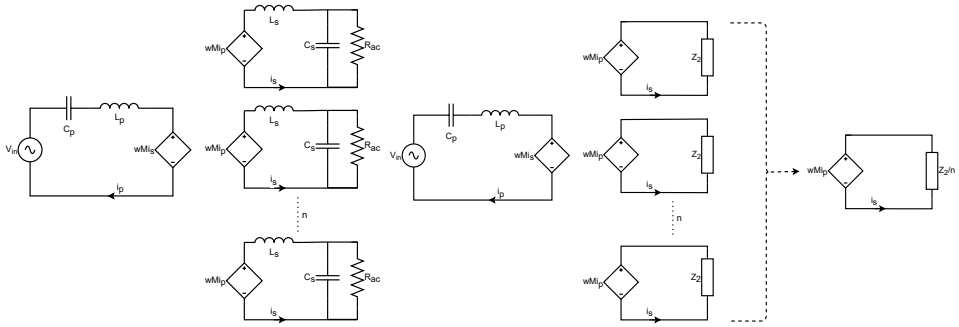
Figure 6.2: 3 isolated receivers

Table 6.2: Mutual Inductances at 5 cm between primary and secondary coils

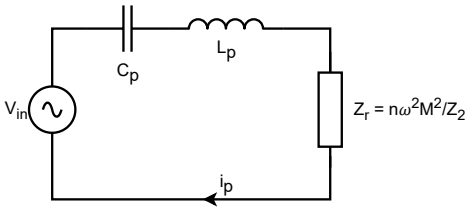
Inductance	M	k
M_{p1}	7.15 µH	0.081
M_{p2}	7.85 µH	0.089
M_{p3}	7.25 µH	0.086
M_{12}	0.3 µH	0.0025
M_{23}	0.3 µH	0.0027
M_{31}	0.3 µH	0.0029

An assumption drawn while modelling the multi-receiver IPT is that all the secondary inductances and their mutual inductances with the primary are equivalent. With this assumption an n receiver based IPT can be modelled according to Fig 6.3. In Fig 6.3a n receivers connected with current-dependent voltage sources are highlighted in a S-P topology. In Fig 6.3b the multi-coil secondaries are simplified to a secondary impedance Z_2. These secondary circuits with equivalent impedance

connected to equivalent voltage sources are simplified into a single voltage source with n parallel impedances [Fig 6.6]. Therefore, the secondary impedance seen by the primary transmitter is Z_2/n. Thus, the n receiver IPT system with S-P topology can be simplified to a referred impedance of Z_r as shown in Fig 6.3c. It is to be noted that the above conclusion is only possible when the mutual inductance formed in an n receiver IPT system is similar to a single receiver IPT system, which has been highlighted in [82].



(a) n receivers in a S-P IPT **(b)** Secondary impedance with n receivers



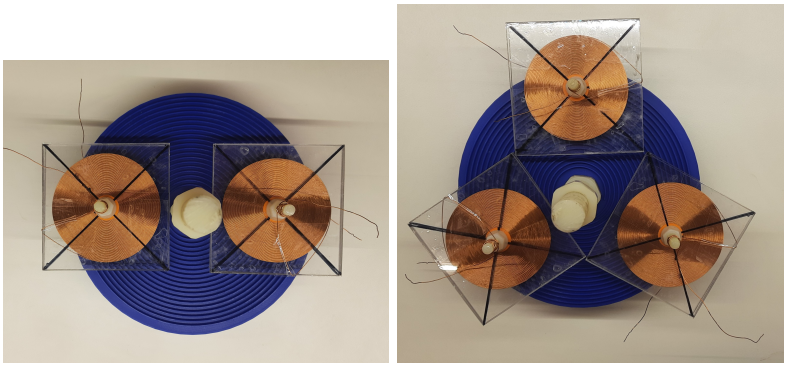
(c) referred impedance with n receivers

Figure 6.3: Modelling of multiple receivers in S-P IPT

$$M = k\sqrt{L_p L_s} = \sqrt{n}k\sqrt{\frac{L_p L_s}{n}} \tag{6.1}$$

$$k_{multicoil} = \sqrt{n}k_{singlecoil} \tag{6.2}$$

Given that the mutual inductances are equivalent in an n receiver and a single receiver IPT, a conclusion is drawn that the n receivers are theoretically connected in parallel as shown in Fig 6.6. Therefore, Eq 6.1 and Eq 6.2 are obtained to understand and develop compensation for the multi-receiver S-P IPT. To test the above conclusion, the Bode VNA is used to obtain the mutual inductances and coupling coefficients in a two-receiver and three-receiver system as shown in Fig 6.4. As highlighted in Fig 6.5, the coupling between the coils is found when the primary inductor is 5 cm away from the plane of the multiple secondary receivers.



(a) Two receiver **(b)** Three receiver

Figure 6.4: Multi Receiver Setup

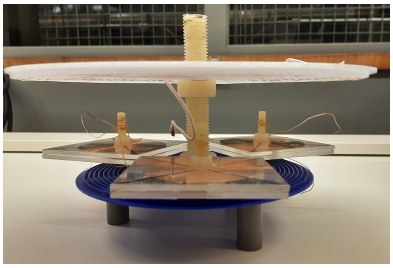


Figure 6.5: Multi-receiver setup at 5 cm between primary and secondary planes

To test the multi-receiver IPT setup, the secondary coils are connected in parallel as shown in Fig 6.6 and the Bode VNA is used to find the equivalent mutual inductance and coupling coefficient. These tests are done on the two-receiver coil and the three-receiver coil setup. The results from the Bode VNA tests are highlighted in Table 6.3.

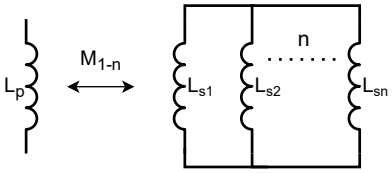


Figure 6.6: Testing n isolated equivalent receivers

M_{12} indicates that only the secondary coils L_{s1} and L_{s2} exist on the secondary plane as a two-receiver coil setup. Similarly, M_{123} highlights that L_{s1}, L_{s2} and L_{s3} exist on the secondary plane as a three-receiver coil setup. The coils in the secondary planes are connected according to Fig 6.6 for testing with the Bode 100

VNA. Comparing the coupling coefficients from Table 6.2 and Table 6.3, a conclusion can be drawn that the k_{2coil} and k_{3coil} is around 1.41 and 1.73 times $k_{singlecoil}$ respectively, thereby proving the Eq 6.2 to be true for the S-P IPT.

Table 6.3: Multi-receiver Mutual Inductances at 5 cm between coils

Inductance	M	k
M_{12}	7.7 µH	0.126
M_{23}	7.5 µH	0.123
M_{31}	7.65 µH	0.125
M_{123}	7.25 µH	0.147

Therefore to develop an IPT for a multi-coil setup, the primary compensation capacitor C_p has to be calculated assuming n receivers are connected in parallel as shown in Fig 6.6. However, each of the receiver coils has to be compensated with a parallel secondary capacitor C_s assuming a single receiver setup as highlighted in Table 6.2. An important consideration while designing the IPT for multiple receivers is that the secondary coil wires have a lower diameter of 0.5 mm and therefore the switching frequency can not be higher than 50 kHz accounting to skin depth.

In this chapter, a two-coil and three-coil multi-receiver based IPT is developed. Their coupling behaviour in these configurations is studied and a conclusion of $k_n = \sqrt{n} * k$ is obtained for a n-receiver IPT. This result has been verified by measurements on the Bode 100 VNA. Insights and potential considerations for developing such a system are provided for the CHB AWG.

7

Conclusion & Recommendations

7.1. Conclusion

The objectives of the master thesis, to develop the HVIPT, a DC IPT based power supply with HV gain have been met, apart from the rated load test at 10 kV DC.

- **Chapter 1** introduced the research topic and provided context as to the need for the HVIPT.
- **Chapter 2** explored the various IPT topologies available based on the required parameters for the HVIPT.
- **Chapter 3** described the working principles with parametric evaluation of S-P topology to match the requirements for the HVIPT.
- **Chapter 4** discussed the prototype development procedure, highlighting the tradeoffs involved in the process.
- **Chapter 5** dealt with the testing of the developed HVIPT prototype.
- **Chapter 6** gave an explanation regarding the development of a multi-receiver IPT system.

This thesis aimed at answering the following research questions which are discussed below :

1. **What are the possible topologies of IPT to achieve a high voltage gain suitable for the HVIPT?**

   The parameters suitable for the HVIPT are highlighted of which Load Invariant Voltage, High Voltage Gain and Soft Switching are of higher weight. Upon

analysing several single-component and multiple-component compensation topologies, the S-P and the μ factor-based S-SP seem suitable. However, considering the simplicity required in designing a fixed supply the S-P topology is the chosen topology for this thesis.

2. **What are the parametric tradeoffs involved in achieving a high voltage gain for the selected topology**

   The parametric tradeoffs between switching frequency, coupling coefficient, primary and secondary inductances are analysed through simulations and a mathematical model. Considering the harmonic behaviour of the input current, ZVS and HV rectifier a switching frequency of 320 kHz, a coupling coefficient of 0.25 and primary and secondary inductances of 13 μH and 125 μH are chosen for the prototype.

3. **What are the design, prototype and testing considerations for such a supply**

   A 400*0.1mm diameter litz wire is used to design primary and secondary coils with a high-quality factor. The variable capacitor banks are used to tune the resonant converter to operate in ZVS. The secondary capacitor must be within 250 pF of the calculated value to operate at the highest efficiency with ZVS. A deadtime of 100 ns is chosen for this topology to allow ZVS. Typhoon HIL is used to provide the required frequency and deadtime. The HV rectifier is developed using filter capacitor as 3.3 nF and the HV multiplier with the capacitor as 1.56 nF. A distance of 6.5 cm is chosen between the coils to enable high voltage gain while keeping efficiency greater than 80%. A significant reduction of 2.5 times in input current is observed as the switching frequency is increased from 50 kHz to 400 kHz for the same load. The developed HVIPT performs well to provide 1.5 kW at 5.2 kV DC. Load regulation of around 18% is observed with the system providing 6.12 kV at no load with the diode rectifier. The efficiency of the developed supply is 88% with the major loss component being the secondary inductor conduction loss. The setup also performs DC breakdown tests and high-frequency AC tests with surface discharges on dielectrics.

4. **What is the feasibility of a multi-coil output for the CHB AWG application?**

   Coupling coefficient for a 2-receiver and a 3-receiver multi-receiver based IPT is studied and a conclusion of $k_n = \sqrt{n} * k_1$ is obtained for a n-receiver IPT. Insights into developing a load invariant, high voltage gain, efficient multiple DC output system is provided using the S-P topology. Potential considerations such as switching frequency for developing such a system are highlighted.

7.2. Recommedations

The conducted research has few areas of improvement regarding the development and testing of the HVIPT, along with suggestions for the multi-receiver IPT system.

The power loss in the secondary winding contributes to around 80% of the overall losses in the HVIPT. A litz wire with a lower strand diameter can be used to reduce the AC resistance, thereby reducing the power loss in the coil. However, a cost analysis must be conducted because lower-diameter strands of litz wire are expensive. Alternatively, the proximity effect of these strands must be analyzed for a Type 2 litz wire, using a FEM tool such as COMSOL. An optimum litz wire configuration must be chosen for the HVIPT, based on cost analysis and loss simulations.

There are a series of developments that can be done on the H-Bridge inverter to optimise the board design, making it more suitable for the HVIPT.

- The kelvin-source and power-source of the SiC MOSFETs must not be shorted on the PCB [Fig 4.12].
- Operating at frequencies around 500 kHz requires the gate drive to be close to the driver MOSFETs, a design change from a two board to a one board setup can be explored for this reason.
- The main hindrance to testing at higher currents and transferring higher powers for the HVIPT are the SiC MOSFETs of the H Bridge. Higher current MOSFETs from the same family and packages are available, these MOSFETs could be used instead of the SiC MOSFET [60] being used now.
- The track width of the PCB power line must be considered before pushing more current. Minor changes to the overcurrent protection scheme must also be made before pushing more current [Appendix B].
- The clear pin must be removed from ground once power is applied in order to enable overcurrent protection and protect the MOSFETs.
- The heatsink on the rear of the power board must be attached to protect the MOSFETs from thermal effects.

A more robust, reliable board must be developed for the HV rectifier. The current board is made using a general purpose board with off-the-shelf and makeshift heatsinks. Alternative designs for a 10 kV diode and a 10 kV blocking DC capacitor must be developed. For developing a 'n' stage multiplier, the capacitors must be increased to increase the load capacitance.

Typhoon HIL is an expensive setup to be used for the HVIPT. The inverter board has the capability to run with the ATMega chip of arduino. For the purpose of prototyping with different frequencies and deadtimes, Typhoon HIL was used. Once a particular frequency and deadtime are decided, arduino can be used to provide pulses for the H Bridge.

The DC breakdown test uses a damping resistor of $20\,\text{k}\Omega$, however, lower resistors could be used to verify the working of the overcurrent protection.

For developing the multi-output IPT system, the proximity effect and skin effect of the secondary windings have to be thoroughly evaluated. This is so because a single-strand isolated wire of 0.5 mm is used with very minimal spacing between them. The use of FEM modelling on COMSOL is recommended for the analysis of proximity, skin effect and coupling coefficient.

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A

MATLAB Code

```
%% Define Inductances (dont vary much with frequency) (from Bode100)

Lp = 13.63e-6;
Ls = 124.25e-6;
Rp = 0.16;      %(80m at 40KHz and 200m at 400kHz - Skin effect)
Rs = 0.73;      %(210m at 40KHz and 915m at 400kHz - Skin effect)
resfreq1 = 9.076e1; %3,46 k
parcap1 = 1/(4*pi*pi*resfreq1*resfreq1*Lp);
resfreq2 = 3.06e6; %46,88 k
parcap2 = 1/(4*pi*pi*resfreq2*resfreq2*Ls);

%%  Mutual Inductance (Analytical)

Mcoil_analytic = 0;
z = 65e-3; %distance between coil
u = 4*pi*1e-7;
ur = 1; %relative permittivity

innradn = 30; % inner radius primary (mm)
innradm = 21; % inner radius secondary (mm)
N = 10; % no of primary turns
M = 31; % no of secondary turns
sn = 6.2; % distance between concentric coil primary (mm)
sm = 3.65; % distance between concentric coil secondary (mm)

for ii = 0:N-1
    a = (innradn+(sn*ii))*1e-3;
    for j = 0:M-1
        b = (innradm+(sm*j))*1e-3;
        g = 2*a*b/(a*a+b*b+z*z);
        M_modified = u*pi*a*a*b*b/((a*a+b*b+z*z)^1.5);
        M_iter = 0.625*M_modified*(1+(15*g*g/32)+(315*g*g*g*g/1024));
        Mcoil_analytic = Mcoil_analytic + M_iter;
    end
end

k_analytic = Mcoil_analytic/sqrt(Lp*Ls);
%% Mutual Inductance (Bode100)

SumInductance = 120.2e-6; % match with the z distance between coil
Mcoil_Meas = (-SumInductance+Lp+Ls)*0.5;
k_Meas = Mcoil_Meas/sqrt(Lp*Ls);

%% Frequencies and Compensation caps

k = 0.25;
freq = 310e3;
omega = 2*pi*freq;
period = 1/freq;
ontime = period/2;

w_sec = omega;
w_pri = w_sec*sqrt(1-k^2);

Cp = (w_pri*w_pri*Lp)^-1;
Cs = (w_sec*w_sec*Ls)^-1;
%Cs = 2e-9;

%% Self Inductance Analytical

%primary coil details
N1 = 10;
Douter1 = 2*95e-3;
Dinner1 = 2*30e-3;
w1 = 2.7e-3;
p1 = 3.86-3;
davg1 = (Dinner1+Douter1)/2;
gamma1 = (Douter1-Dinner1)/(Douter1+Dinner1);

%secondary coil details
N2 = 31;
Douter2 = 2*134.15e-3;
Dinner2 = 2*21e-3;
w2 = 2.7e-3;
p2 = 0.95e-3;
davg2 = (Dinner2 + Douter2)/2;
gamma2 = (Douter2-Dinner2)/(Douter2+Dinner2);

Lp_analytic = u*N1*N1*davg1*0.5*(0.2*gamma1*gamma1+log(2.46/gamma1));
Ls_analytic = u*N2*N2*davg2*0.5*(0.2*gamma2*gamma2+log(2.46/gamma2));
```

(a) Compensation

```
%%  Inductances and Coil Related

Lp_leak = (1-k)*Lp;
Ls_leak = (1-k)*Ls;
Lp_mag = k*Lp;
Ls_mag = k*Ls;
M = k*sqrt(Lp*Ls);

sigma = 5.96e7;
skindepth = 1/sqrt(pi*freq*u*sigma);

length1 = N1*pi*davg1;              % coil length primary
length2 = N2*pi*davg2;              % coil length secondary
dia = 0.1;
effdia = sqrt(0.25*pi*2.7*2.7/(400*0.25*pi));
porosityfactor = sqrt(0.25*pi)*dia/effdia; %d/t*sqrt(0.25*pi)

R1 = 8*(0.0025*4*N1*pi*davg1/(sigma*pi*1e-4*1e-4)); % 8*DCresistance
% primary    %around 5.5ohm/km is DC resistance
R2 = 8*(0.0025*4*N2*pi*davg2/(sigma*pi*1e-4*1e-4)); % 8*DCresistance
% secondary  %does not match with real life find skin effect formula for
% litz wire
Q1 = 2*pi*freq*Lp/R1; % Q factor coil 1
Q2 = 2*pi*freq*Ls/R2; % Q factor coil 2

E_LIV = sqrt(Ls/Lp)/k;
%% Mathematical Analysis (Primary Side) 1st Harmonic

Vin = 350;
RL = 10e3;
Rac= 8*RL/pi^2;

for h = 1:2:31
% Harmonic
Zin(h) = R1 + h*omega*Lp*1i + (h*omega*Cp*1i)^-1 + ((h^2*omega^2*M^2)/ ...
    (R2 + h*omega*Ls*1i + (Rac/(1+(omega*h*Cs*Rac*1i)))));
Zin_real(h) = real(Zin(h));
Zin_mag(h) = abs(Zin(h));
Zin_imag(h) = imag(Zin(h));

% Reflected impedance
Zr(h) =  h^2*omega^2*M^2/(R2 + h*omega*Ls*1i + ...
    (Rac/(1+(omega*h*Cs*Rac*1i))));
Zr_real(h) = real(Zr(h));
Zr_mag(h) = abs(Zr(h));
Zr_imag(h) = imag(Zr(h));

% H bridge input V-I
Vhmax(h) = 4*Vin/(h*pi);
Vhrms(h) = 4*Vin/(h*pi*sqrt(2));
Ihmax(h) = 4*Vin/(h*pi*abs(Zin(h)));
Ihrms(h) = 4*Vin/(h*pi*sqrt(2)*abs(Zin(h)));
Impedanceangle(h) = angle(Zin(h));

% primary cap V
Xcp(h) = (omega*h*Cp*1i)^-1;
Vcpmax(h) = abs(Xcp(h))*Ihmax(h);
Vcprms(h) = abs(Xcp(h))*Ihrms(h);
Capacitanceangle(h) = angle(Xcp(h));

% primary coil V
Inductanceangle(h) = Capacitanceangle(h) - Impedanceangle(h);
Vlprms(h) = sqrt((Vhmax(h))^2+(abs(Xcp(h))*abs(Ihmax(h)))^2)/sqrt(2);

% power primary
P_instant(h) = Vhrms(h)*Ihrms(h);

skindepth(h) = 1/sqrt(pi*h*freq*u*sigma);
end
```

(b) Mathematical Model

Figure A.1: MATLAB Code - 1

A

```
%% Mathematical analysis (Secondary Side)
Vin = 0;
Iin = 0;
Vout = 0;
Iout = 0;
Icoil = 0;
Ics = 0;
Vcp = 0;

for h = 1:2:31 %harmonic

% load impedance
Zsload(h) = (Rac/(1+(omega*h*Cs*Rac*1i)));
Zsload_real(h) = real(Zsload(h));
Zsload_mag(h) = abs(Zsload(h));
Zsload_imag(h) = imag(Zsload(h));

% secondary side impedance
Zs(h) = (R2 + h*omega*Ls*1i + (Rac/(1+(omega*h*Cs*Rac*1i))));
Zs_real(h) = real(Zs(h));
Zs_mag(h) = abs(Zs(h));
Zs_imag(h) = imag(Zs(h));
SecImpedanceangle(h) = angle(Zs(h));

% induced voltage and secondary current at coil
Vindmax(h) = omega*M*Ihmax(h);
Vindrms(h) = omega*M*Ihmax(h)/sqrt(2);
Ismax(h) = omega*M*Ihmax(h)/Zs_mag(h);
Isrms(h) = omega*M*Ihrms(h)/Zs_mag(h);

% secondary cap current
impdivision_cap(h) = (Rac/(Rac+(omega*h*Cs*1i)^-1));
Zcapdiv_mag(h) = abs(impdivision_cap(h));
Capdivangle(h) = angle(impdivision_cap(h));
Icsmax(h) = Zcapdiv_mag(h)*abs(Ismax(h));
Icsrms(h) = Zcapdiv_mag(h)*abs(Isrms(h));

% secondary load current
impdivision_load(h) = (((omega*h*Cs*1i)^-1)/(Rac+(omega*h*Cs*1i)^-1));
Zloaddiv_mag(h) = abs(impdivision_load(h));
Loaddivangle(h) = angle(impdivision_load(h));
Iloadmax(h) = Zloaddiv_mag(h)*abs(Ismax(h));
Iloadrms(h) = Zloaddiv_mag(h)*abs(Isrms(h));

% secondary output voltage
Vsmax(h) = Zcapdiv_mag(h)*abs(Ismax(h))/(omega*h*Cs);
Vsrms(h) = Zcapdiv_mag(h)*abs(Isrms(h))/(omega*h*Cs);
Voltagesecangle(h) = angle((omega*h*Cs*1i)^-1);

% power primary
P_instant_sec(h) = Vsrms(h)*Iloadrms(h);

% declare parameters
t = 0:1e-12:0.9375e-5/3;
Vin = Vin + Vhmax(h)*sin(h*omega*t);
Iin = Iin + Ihmax(h)*sin(h*omega*t-Impedanceangle(h));
Vout = Vout + Vsmax(h)*sin(h*(omega*t+(0.5*pi))-SecImpedanceangle(h)+Capdiv
    angle(h)+Voltagesecangle(h));
Iout = Iout + Iloadmax(h)*sin(h*(omega*t+(0.5*pi))-SecImpedanceangle(h)+ ..
    Loaddivangle(h));
Icoil = Icoil + Ismax(h)*sin(h*(omega*t+(0.5*pi))-SecImpedanceangle(h));
Ics = Ics + Icsmax(h)*sin(h*(omega*t+(0.5*pi))-SecImpedanceangle(h)+Capdiv
    angle(h));
Vcp = Vcp + Vcpmax(h)*sin(h*omega*t-Impedanceangle(h)+Capacitanceangle(h));

end
```

(a) Mathematical Model

```
%% plotting waveforms


Pin = Vin.*Iin;
InputV = rms(Vin);
InputI = rms(Iin);
InputP = rms(Pin);

subplot(3,3,1)
yyaxis left
plot(t,Vin);
ylabel('Input Voltage')
yyaxis right
plot(t,Iin);
ylabel('Input Current')
grid on

subplot(3,3,3)
plot(t,Vin.*Iin)
ylabel('Input Power')
grid on

Pout = Vout.*Iout;
OutputV = rms(Vout);
OutputI = rms(Iout);
OutputP = rms(Pout);

subplot(3,3,2)
yyaxis left
plot(t,Vout);
ylabel('Output Voltage')
yyaxis right
plot(t,Iout);
ylabel('Output Current')
grid on

subplot(3,3,4)
plot(t,Vout.*Iout)
ylabel('Output Power')
grid on

subplot(3,3,5)
yyaxis left
plot(t,Ics);
ylabel('Secondary Capacitor Current')
yyaxis right
plot(t,Icoil);
ylabel('Secondary Coil Current')
grid on

Vlp = Vin - Vcp;
subplot(3,3,6)
yyaxis left
plot(t,Vcp);
ylabel('Primary Capacitor Voltage')
yyaxis right
plot(t,Vlp);
ylabel('Primary Coil Voltage')
grid on

subplot(3,3,7)
stem(Vhmax)
ylabel('InputVoltage Decompose')
subplot(3,3,8)
stem(Ihmax)
ylabel('InputCurrent Decompose')

subplot(3,3,9)
yyaxis left
stem(Zin_real)
ylabel('InputRealImpedance Decompose')
yyaxis right
stem(Zin_imag)
ylabel('InputImagImpedance Decompose')
```

(b) Plotting waveforms

Figure A.2: MATLAB Code - 2

B

Over Current Protection

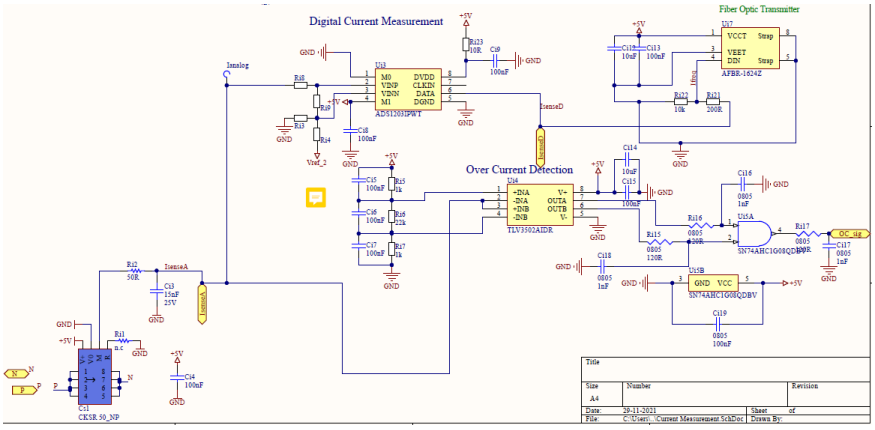

Figure B.1: Over Current Detection

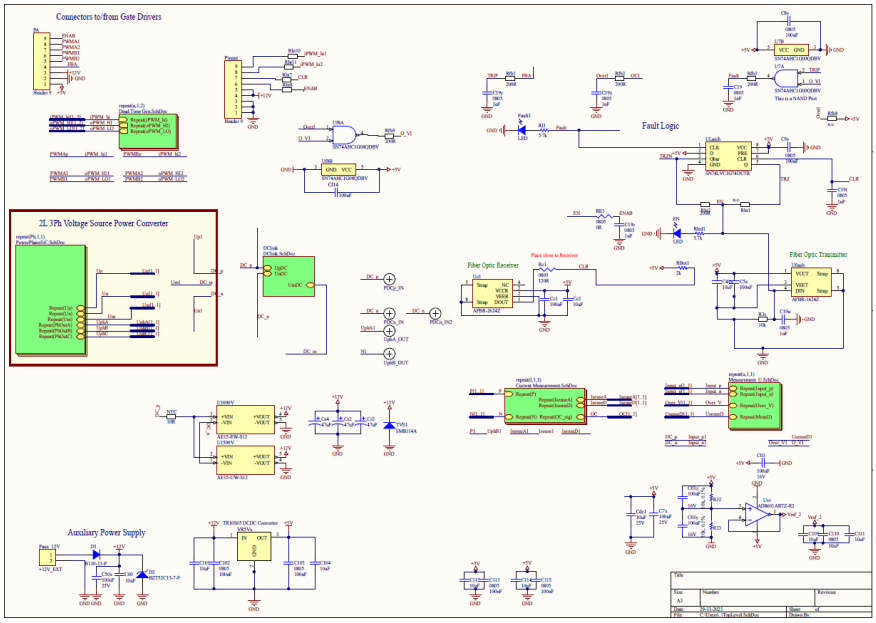

Figure B.2: Fault Condition Circuit