

An Energy-Efficient Reconfigurable Interface for Resonant Sensors Based On Ring-Down Measurement

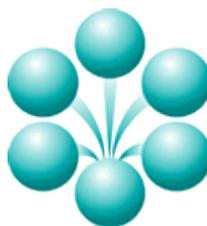
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Abstract

This thesis discusses the theory, architecture design, circuit design and measurements of an ultra-low-energy reconfigurable interface circuit for resonant gas sensors.

This interface circuit employs a transient measurement method. The resonant sensor is driven at a frequency close to its resonance frequency by an excitation source that is intermittently disconnected, causing the sensor to oscillate at its resonance frequency with an exponentially-decaying amplitude. From the associated ring-down signal, the frequency of the freely-oscillating sensor and its quality factor are obtained by means of a counting technique. A prototype readout circuit that senses the ring-down signal and performs the required level-crossing detection has been fabricated in a standard 0.35- μm CMOS technology. The experimental results obtained using this prototype in combination with samples of micro-machined clamped-clamped beam resonators show good consistency with the resonance frequency and quality factor obtained using conventional impedance analysis. Compared to prior implementations, the realized prototype is less sensitive to leakage currents, enabling a shorter measurement time, and provides a reconfigurable front-end circuit that allows it to be connected to resonators with different parameters. The circuit consumes an energy of 207.9nJ per measurement.

Key words: Energy-efficiency, Sensor interfacing, Resonant sensors, Reconfigurability

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Chapter 1

Introduction

At Holst Centre, micromachined resonant sensors have been developed for the measurement of gas concentration [1]. These sensors consist of a high aspect (length/thickness) ratio doubly-clamped silicon nitride beam with integrated piezoelectric (aluminum nitride) transducers, which can be used to achieve high sensitivity and ultra low power consumption. After coating with special material, it can be sensitive to gas concentration and applied to biochemical sensing. The compound concentration can be derived by measuring the shift of the resonance frequency (f_{res}) and quality factor (Q). These characteristics make it become a very promising candidate for the application in wireless autonomous sensor systems. However, an energy-efficient interface circuit is required to fulfill this promising sensor system. The goal of this thesis is to illustrate how to design such a readout circuit and to evaluate its performance.

At the beginning of this chapter, a brief explanation of the operating principle is given as well as a description of the electrical model of resonant sensor. That is followed by a short discussion of different readout approaches in section 1.2, including a comparison between the prior art and our work. Finally, the outline of the whole thesis is shown in section 1.3.

1.1 Micromechanical resonant sensors

1.1.1 Operating principle

The micromechanical resonant sensors studied in our work consist of a silicon nitride beam with integrated piezoelectric (aluminum nitride) transducers, as shown in Figure 1-1(a). When the sensor is excited with an electrical signal, the beam starts oscillating because of the transducer. After coating with a suitable polymer, these sensors are sensitive to gas compounds and can be used to detect gas concentration. When the sensor is exposed to the target volatile gas, if the gas concentration varies, the polymer swells and the swelling induces stress. This stress will cause a shift in resonance frequency and quality factor. By measuring the shift of resonance frequency and quality factor, gas concentration can be obtained.

The typical number for the resonance frequency in our work is hundreds of kilohertz. A typical number for the relative sensitivity of the resonance frequency to absorption of ethanol has been

reported to be 3.6×10^{-6} /ppm [1].

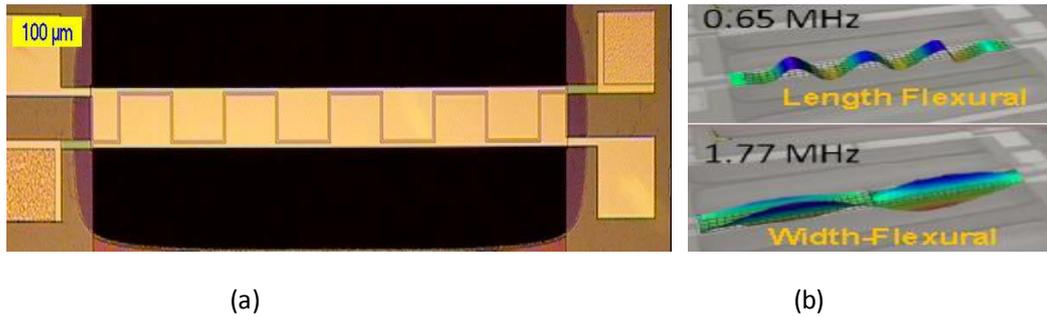


Figure 1-1: (a) Closed-up view of mechanical resonant sensor (b) images illustrating the length-flexural and width-flexural modes

1.1.2 Electrical model

In general, the resonant sensor has several resonance modes for sensing, and each of them has a different resonance frequency and vibration shapes, for instance, the length-flexural mode at lower frequency and the width-flexural mode at higher frequency as shown in Figure 1-1(b). Furthermore, different modes also have their own equivalent electrical parameters (L_m , C_m , R_m in the equivalent electrical model). In this work, we focus on the length-flexural mode in series resonance because the sensor has higher sensitivity at this mode. The electrical model is illustrated in Figure 1-2. The two terminals in Figure 1-2 represent the pins of the resonator used for connecting with the interface.

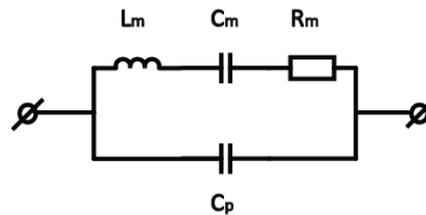


Figure 1-2: Electrical model of resonant sensor

This electrical model is composed of two parts: one is a RLC circuit consisting of a resistor (R_m), an inductor (L_m), and a capacitor (C_m), connected in series. The other is a parallel parasitic capacitance (C_p). The parallel capacitor (C_p) is an indication of the actual parasitic capacitance of the piezoelectric patch. The inductor L_m and the capacitor C_m act as an electrical resonator. The energy oscillates back and forth between the capacitor's electric field (E) and the inductor's magnetic field (B). Charge flows back and forth between the capacitor and the inductance. However, due to the presence of the resistor R_m , the oscillating current decays with time to zero if it is not kept going by an excitation source.

One important property of this circuit is its capability to resonate at a specific frequency, the resonance frequency. The resonance frequency is defined as the frequency at which the impedance of the circuit is at its minimum. Equivalently, it can be defined as the frequency at which the impedance is purely real (that is, purely resistive). This occurs because the impedances of the inductor and capacitor at resonance are equal but of opposite sign and cancel out.

$$j\omega L_m = -\frac{1}{j\omega C_m}$$

Hence, the resonance frequency can be derived by:

$$f_{res} = \frac{1}{2\pi\sqrt{L_m C_m}} \quad (1-1)$$

The other important property of this circuit is the quality factor. It is defined as the peak frequency in the circuit divided by the bandwidth between two frequencies at which the power stored on the RLC tank has fallen to half the value passed at resonance. One of the half-power frequencies is above, and the other is below the resonance frequency [2].

$$Q = \frac{\omega_0}{\Delta\omega} = \frac{\omega_0}{2\alpha} \quad (1-2)$$

In this formula, α is damping attenuation, which can be obtained by the following equation.

$$\alpha = \frac{R_m}{2L_m}$$

As a result, the quality factor is given by:

$$Q = \frac{1}{R_m} \sqrt{\frac{L_m}{C_m}} \quad (1-3)$$

Two other factors are also commonly used for indicating the power loss-rate of oscillation: the damping factor (ζ) and the dissipation factor (D). The damping factor is calculated by:

$$\zeta = \frac{1}{2Q} \quad (1-4)$$

The dissipation factor is the reciprocal of quality factor,

$$D = \frac{1}{Q} \quad (1-5)$$

1.2 Readout approaches and prior art

There are three main approaches applied to the measurement of resonance frequency and

quality factor of resonant sensors: impedance analysis, oscillator-based readout, and ring-down measurement [9] [10] [11].

Using an impedance analyzer is the most commonly used technique in the laboratory. The impedance of the resonator over a range of frequencies is measured by sweeping the frequency of the driving voltage. Based on the curve of the measured impedance, parameters of the electrical model can be derived, e.g. by means of curve-fitting. Then the value of resonance frequency and quality factor can be derived by Equation (1-1) and (1-3) respectively. Disadvantages of this method are the fact that it is time-consuming, energy-consuming and computationally intensive. And the large and complex equipment needed during the measurement also lead to high cost and poor integration. Hence, the impedance analysis method is not readily applicable to wireless autonomous sensor applications.

The oscillator-based readout approach is implemented by using a feedback loop circuit to maintain the resonator oscillating. As a result, the output of the feedback loop is a sustained oscillation signal with a frequency equal to the resonance frequency. Therefore, the resonance frequency can be measured. However, information about the quality factor cannot be obtained in this approach. Even though this method is compatible with integration technology, it consumes energy to sustain the oscillation. Moreover, the circuit is difficult to work with in the presence of large parasitic capacitance C_p [3].

To apply the resonant sensor to wireless autonomous sensor systems, we need to design an energy-efficient integrated readout circuit. The ring-down measurement is exactly the approach we are looking for.

1.2.1 Basic principle of ring-down measurement

In the ring-down measurement approach, basically, two operating phases are involved. The block diagram of ring-down measurement is shown in Figure 1-3.

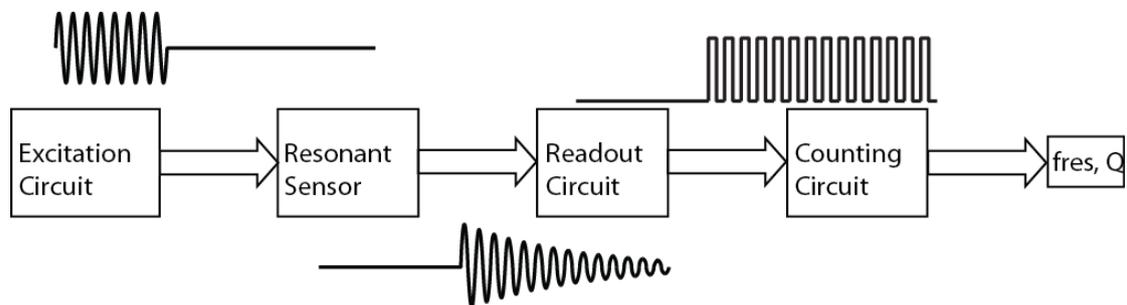


Figure 1-3: Block diagram of the ring-down measurement

In the excitation phase, the resonant sensor is connected to an excitation circuit. This excitation source has a frequency close (but not necessarily equal) to the resonance frequency of resonator. As a consequence, the resonator gets enough energy and starts oscillating at the driving frequency. In the next ring-down phase, the driving source is terminated and the resonant sensor is connected to the readout circuit. Due to the absence of the excitation source, the resonance starts to decay at the resonance frequency. Then, an exponentially-decayed sinusoidal signal is obtained. Based on the zero-crossing technique and threshold-crossing technique (Chapter 2, section 2.2.2), the information of the resonance frequency and quality factor can be extracted.

1.2.2 Prior art

Several studies and PCB implementations of the ring-down measurement technique can be found in the literature [5] [6] [7] [8]. An integrated implementation of this technique has also been reported [9]. Figure 1-4 demonstrates the circuit diagram of the resonant-sensor interface reported in [9].

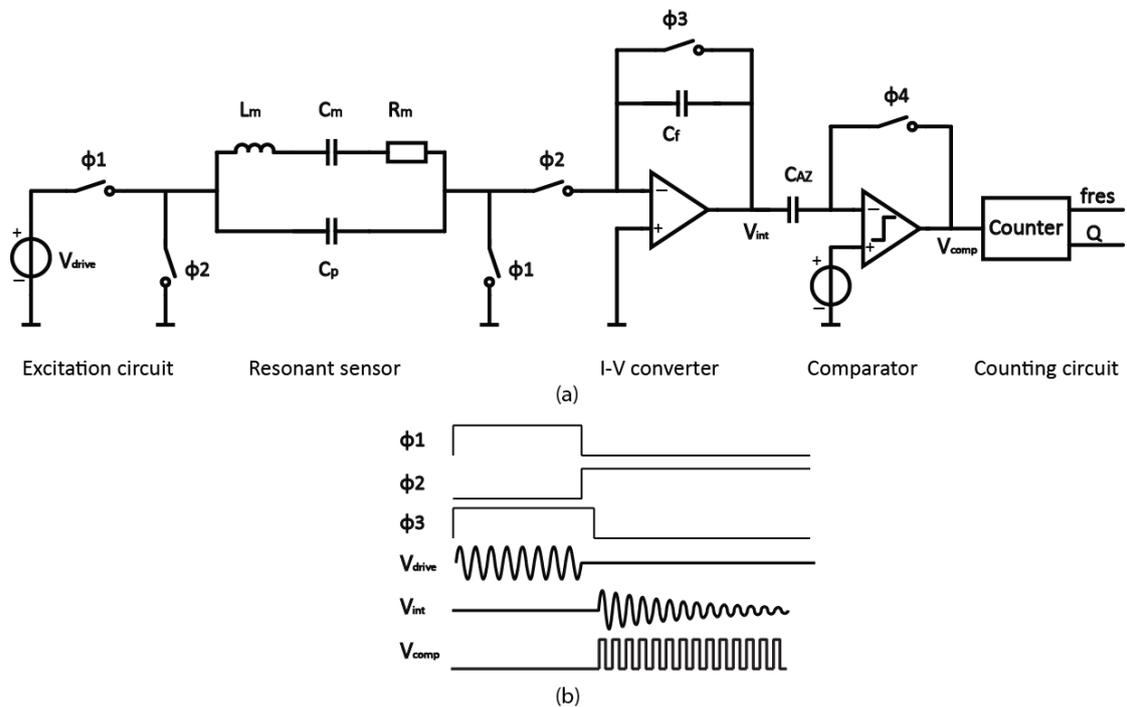


Figure 1-4: (a) Circuit diagram of the resonant-sensor interface (b) timing diagram and important signals for the resonance frequency measurement

As shown in Figure 1-4, this resonant-sensor interface is composed of a switched excitation source, a switched-capacitor current-to-voltage (I-V) converter, a comparator, and a digital counter. During the excitation phase ϕ_1 , the resonator is driven by the excitation source (V_{drive}) at a frequency close to its resonance frequency. The rest of the circuit is powered down to save energy. At the end of phase ϕ_1 , the excitation source is switched off. At the beginning of phase

ϕ_2 , the integrator is briefly kept in unity-gain configuration to dissipate the charge stored in C_p and cancel the effect of C_p . During the subsequent phase ϕ_2 , the resonator is connected to the readout circuit. The damped sinusoidal ring-down current is integrated to a ring-down voltage (V_{int}) by the integrator that acts as a current-to-voltage converter. Then at the output of the comparator, a square wave (V_{comp}) is obtained. Prior work has demonstrated this approach with a few advantages discussed below [9].

Advantages

- Both resonance frequency and quality factor can be extracted easily using zero-crossings and threshold-counting technique.
- The energy-efficient circuit consumes energy of 237nJ per measurement, which is relatively-low consumption [9].
- Effect of C_p is cancelled by keeping the integrator in unity-gain configuration at the beginning of the ring-down phase to dissipate the charge on C_p .

Disadvantages

However, there are still some shortcomings in the prior work. In the previous work, a capacitive feedback current-to-voltage converter was chosen because the feedback impedance is proportional to the resistance of the resonator. Large feedback impedance is required due to the large resistance of the resonator. To reduce the die area, the capacitive feedback was chosen.

One of problems caused by capacitive feedback is the influence of leakage currents. As shown in Figure 1-5, if there is a leakage current at the input of the OTA, this current is integrated by the feedback capacitor during the ring-down phase. This integrated voltage causes the DC operating point at the output of OTA to increase over time, which has a negative influence on the zero-crossing detection.

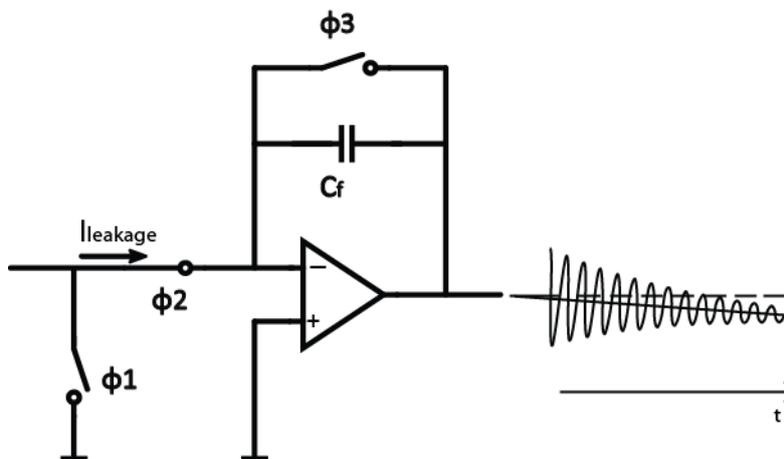


Figure 1-5: Influence of the leakage current

An offset is also induced by using the integrator. For instance, one of extreme cases is shown in Figure 1-6. The ring-down signal in the left represents the ring-down current that flows into the integrator, and the ring-down signal in the right represents the integrated output voltage. When switch 3 is switched on at zero level of the ring-down current, after integration, a 90 degree phase shift is generated at the output due to the feedback capacitor. Therefore, the output starts to ring down at the peak level, and then an offset occurs (V_{os} in Figure 1-6). In this case, we have the maximum offset, which equals the initial ring-down amplitude. When switch 3 is switched on at the peak of the ring-down current, no offset is introduced. Since the switching moment decides the starting point of charge integration, the value of the offset depends on the switching moment of switch 3. Hence, the auto-zeroing technique is needed to cancel this offset for one excitation & ring-down step before the measurement of resonance frequency and quality factor.

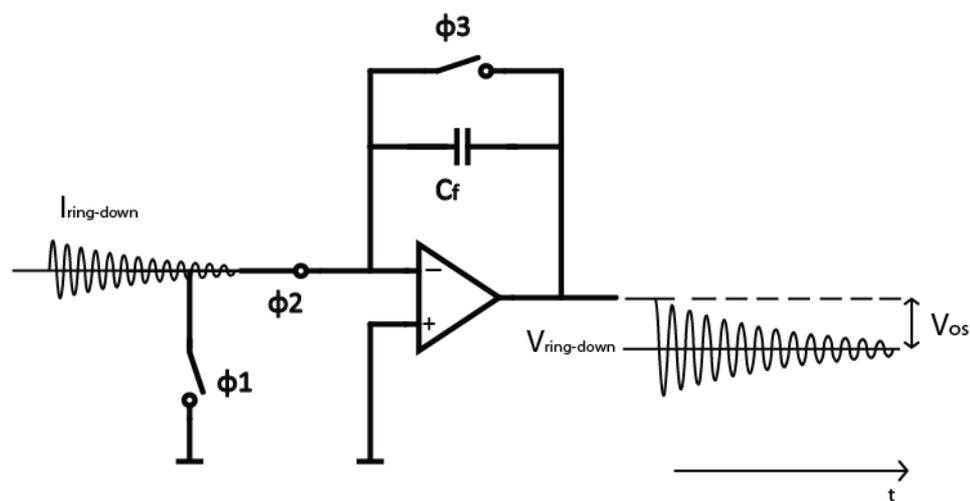


Figure 1-6: switching at the zero level of the ring-down current

Moreover, prior work is only applied to one sensor. It is not proved to be qualified for various different sensors.

Therefore, our work intends to address these shortcomings. Compared with prior work, our work is not sensitive to the leakage current. The auto-zeroing technique is only needed to cancel the DC offset for a short time before the main ring-down measurement, thus significantly reducing the measurement time. Another important improvement of our work is its configurability to be applied to various different sensors. The details of the solution will be developed later in the thesis.

1.3 Outline of the thesis

This thesis presents the basic principles and circuit implementation of a readout circuit for micromechanical resonant sensors, which can be applied for energy-efficient sensing applications.

Apart from this introductory chapter, the rest of this thesis is divided into four chapters.

Chapter 2 discusses the target specifications and the operating principles of the different sub-blocks (front-end circuit, comparator and counting circuitry). This chapter also provides a detailed analysis of the architecture-level design of the proposed readout approach, including sub-block design requirements and error analysis of each sub-block.

Chapter 3 contains the circuit-level analysis and design of the resonator interface. The proposed circuit will be discussed in several sub-sections, describing a programmable feedback network, the front-end amplifier, switches, and the auto-zeroed comparator. Simulation results are also presented in this chapter. Apart from the analog design and the simulation results, the design of the counting circuitry is also introduced.

In Chapter 4, the details of the measurement results are given. A brief introduction describing the fabricated chip and the measurement setup is also included.

Finally, Chapter 5 summarizes the contributions of the thesis. Furthermore, potential directions in future work are highlighted.

References

- [1] D.M. Karabacak, S.H. Brongersma, and M. Crego-Calama, "Enhanced sensitivity volatile detection with low power integrated micromechanical resonators," *Lab on a Chip*, 2010, no. 10, pp. 1976–1982.
- [2] RLC circuit, Wikipedia, http://en.wikipedia.org/wiki/RLC_circuit
- [3] L. Sieben-Xu, J. Pettine, V. Petrescu, M. Vandecasteele, D. M. Karabacak, "System Optimization Methodology for Integrated Piezoelectric MEMS Resonator Biochemical Sensors," *Procedia Engineering*, Proceedings of Eurosensors XXVI, 47, 635-638, 2012.
- [4] G. Torri, X. Rottenberg, D. M. Karabacak, M. Vandecasteele, C. van Hoof, R. Puers, and H. Tilmans, "Optimized design and placement of piezoelectric transducers for micromechanical structures subject to membrane stress", *The Proceedings of the 13th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, 1-8, 2012.
- [5] M. Rodahl, F. Höök, A. Krozer, P. Brzezinski, and B. Kasemo, "Quartz crystal microbalance setup for frequency and Q-factor measurements in gaseous and liquid environments," *Rev. Sci. Instrum.*, vol. 66, no. 7, pp. 3924-3930, July 1995.
- [6] M. Rodahl and B. Kasemo, "A simple setup to simultaneously measure the resonant frequency and the absolute dissipation factor of a quartz crystal microbalance," *Rev. Sci. Instrum.*, vol. 67, no. 9, pp.3238-3241, Sept. 1996.
- [7] K. Zeng, K.G. Ong, C. Mungle, and C.A. Grimes, "Time domain characterization of oscillating sensors: Application of frequency counting to resonance frequency determination," *Rev. Sci. Instrum.*, vol. 73, no. 12, pp. 4375-4380, Dec. 2002.
- [8] K. Zeng and C.A. Grimes, "Threshold-crossing counting technique for damping factor determination of resonator sensors," *Rev. Sci. Instrum.*, vol. 75, no. 12, pp. 5257-5261, Dec. 2004.
- [9] Z. Zeng, M. A. P. Pertijs and D. M. Karabacak, "An Energy-Efficient Readout Circuit for Resonant Sensors Based on Ring-Down Measurement," *Review of Scientific Instruments*, 84, 025005, Jan. 2013.
- [10] M. Patrascu, J. Pettine, D.M. Karabacak, M. Vandecasteele, S.H. Brongersma, M. Crego-Calama "Oscillator-based volatile detection system using doubly-clamped micromechanical resonators" *Procedia Engineering*, 25 (2011), pp. 1533–1536
- [11] B. Jakoby, "A novel analog readout electronics for microacoustic thickness shear-mode sensors", *IEEE Sensors Journal*, vol. 5, pp. 1106-1111, Oct. 2005.

Chapter 2

Architecture-Level Analysis and Design

In this chapter, the architecture-level analysis and design of the proposed ring-down approach are presented. It starts with target specifications; followed by the operating principles of the different sub-blocks, including the front-end circuit, comparator and counting circuitry. Then design requirements of each sub-block are discussed. An error analysis is also included. Finally, simulation results and conclusions are given.

2.1 Target specifications

The target specifications will be explained in the following three aspects: detection limit, configurability and energy consumption.

Detection limit

In this project, we measure the resonance frequency and the quality factor of the resonator. Based on this information, the concentration of volatile compounds can be derived. The sensitivity of the chosen sensors is expected to have a similar sensitivity for ethanol concentration as reported in [1], i.e. 3.6×10^{-6} /ppm. Hence, to achieve a detection limit in terms of ethanol concentration of at least 25ppm, we derive a minimum requirement (0.9×10^{-4}) on the detection limit for the frequency measurement. As a consequence, the detection limit for the interface circuit is given by:

$$\frac{\Delta f_{\text{res}}}{f_{\text{res}}} < 10^{-4} \quad (2-1)$$

In addition to the detection limit for the resonance frequency, a detection limit for the quality factor is also defined:

$$\frac{\Delta Q}{Q} < 1\% \quad (2-2)$$

This detection limit will not be explicitly considered in our design phase to simplify the analysis.

Configurability

The interface is made programmable to cover a certain range of resonators. Resonant sensors designed by Holst Centre can be divided into two different types. One of them is called Type A. The other is named Type C. Type A is fully covered with the piezoelectric transducer while Type C is 50% covered with the piezoelectric transducer. Table 2-1 gives an example with typical values of the model parameters in Type A and Type C [2].

| Model parameter | Type A | Type C |
|-----------------|-----------------|-----------------|
| R_m | 390.9k Ω | 1.391M Ω |
| L_m | 51.07H | 240.7H |
| C_m | 1731aF | 460aF |
| C_p | 4.199pF | 9.758pF |
| f_{res} | 535.2kHz | 478.3kHz |
| Q | 439.4 | 520.1 |

Table 2-1: Model parameters for Type A and Type C

The resistance (R_m) of Type A is much smaller than that of Type C. A rough calculation is given below to estimate the effect of R_m .

If we assume the excitation frequency (f_{dr}) is equal to the resonance frequency (f_{res}) and the amplitude of the excitation signal is expressed by V_{dr} , the initial ring-down current (i_0) through the RLC tank can be calculated by V_{dr}/R_m (section 2.3). This current is amplified by the I-V converter by a factor of the feedback impedance (R_f). Hence, the initial amplitude of the ring-down voltage (A_0) after I-V conversion is approximately equal to:

$$A_0 = V_{dr} \cdot \frac{R_f}{R_m}$$

According to this equation, the value of the feedback impedance should be proportional to the value of R_m . In our work, V_{dr} is about 100mV and A_0 is 500mV to be readable. Then R_f is five times larger than R_m , which means large values of R_m results in large die area on chip [8]. Therefore, we prefer to use Type A for our design.

To be able to read out a reasonable subset of the Type A resonators, we choose to make the readout circuit reconfigurable. It should be able to handle the following ranges of parameters:

- f_{res} : 300kHz ~ 800 kHz
- C_p : 5~15pF
- Q : >300
- R_m : 100k~500k Ω

Energy consumption

Resonant sensors are promising energy-efficient resonant if the readout circuit is also energy-efficient. So we need to make energy per measurement as low possible while maintaining detection limits for $\Delta Q/Q$ and $\Delta f_{res}/f_{res}$. As reported in [8], power consumption is 236.9nJ per measurement. For our work, the energy consumption is expected to be at least as good as the previous work.

2.2 Operating principles

The operating principles of the proposed architecture for the interface circuit (Figure 2-1) are described in this section. Resistive feedback for the I-V converter is chosen because capacitive feedback is sensitive to the leakage current (proved in the prior art) [8], and the parallel capacitor is added to reduce the noise (section 2.4.3). The interface system includes a front-end circuit, an auto-zeroed comparator and counting circuitry. The front-end circuit consists of a switched excitation source, the resonator with parasitic, and a current-to-voltage converter (I-V converter). According to their different function, the operation of the read-out circuit will be introduced in three aspects: front-end operation, comparator operation and counting circuitry operation.

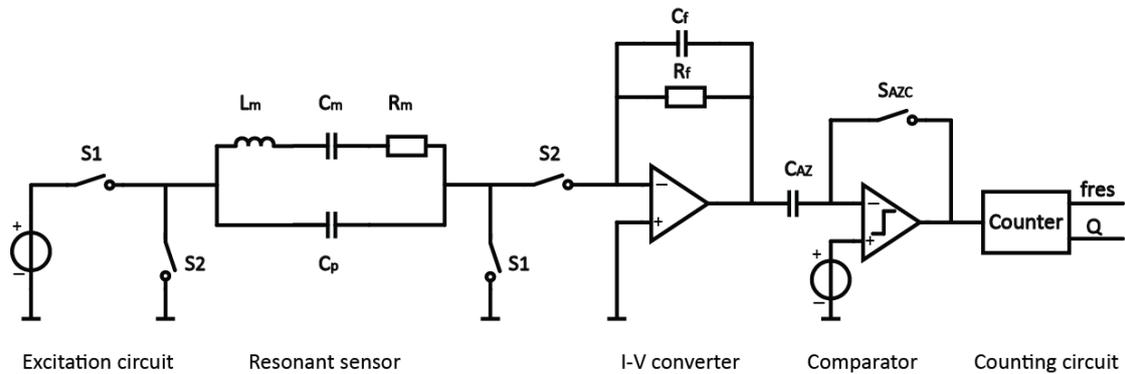


Figure 2-1: Proposed architecture

2.2.1 Front-end circuit operation

In the front-end circuit, firstly, we have a resonant sensor to be applied for gas sensing. A switched excitation source is used for driving the resonators, after which the I-V converter amplifies the ring-down current. The details of their operating principles will be discussed in two phases: excitation phase and ring-down phase.

Excitation phase

During the excitation phase, the resonator is energized. As shown in Figure 2-2, switches S1 are

closed and switches S2 are open. One side of the resonator is connected to the excitation source. The other side is shorted to ground. The excitation time needs to be long enough and the frequency of the excitation signal needs to be close to the resonant frequency to make sure the energy stored in the resonator is high enough. The remaining circuit can be powered down to save energy.

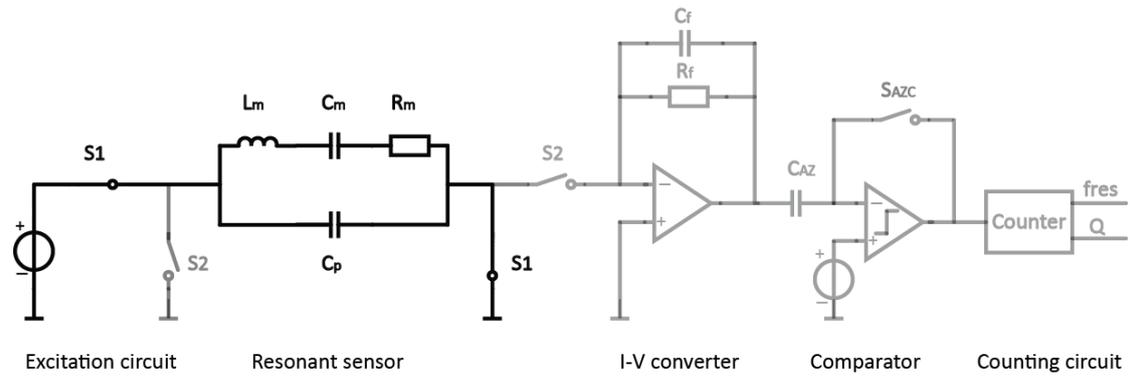


Figure 2-2: Operation during the excitation phase

Ring-down phase

During the ring-down phase, as shown in Figure 2-3, switches S1 are switched off while switches S2 are switched on. The resonator is connected to the I-V converter. Because the ring-down signal is a very small current, the I-V converter is needed to amplify this current to a readable voltage before zero-crossing detection.

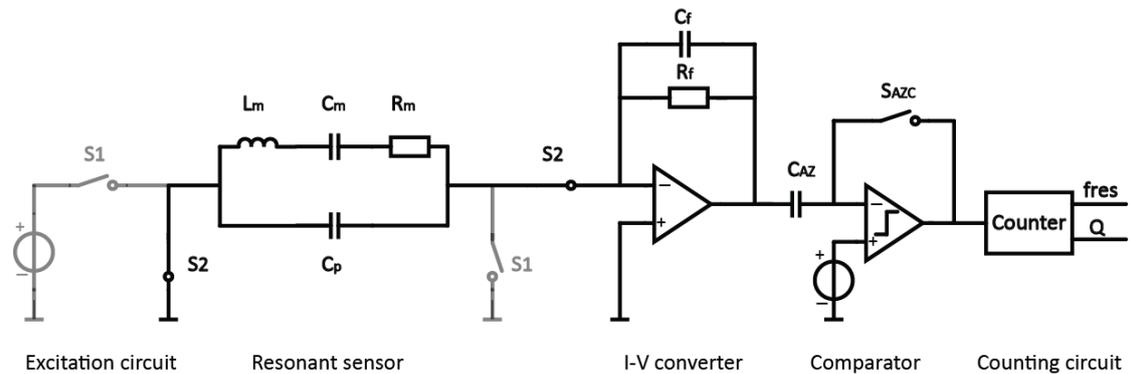


Figure 2-3: Operation in the ring-down phase

2.2.2 Comparator and counting circuitry operation

Another important part of the whole system is the comparator, which plays a role in the zero-crossing and threshold-crossing technique. By using the zero-crossing technique, the resonance frequency can be determined. Threshold-crossing detection is needed to acquire information about the quality factor. To get the final measurement result of the resonance frequency and quality factor, counting circuitry is needed to calculate both of them.

Resonance frequency measurement: zero-crossing detection

To measure the resonance frequency, the threshold voltage at one input of the comparator is set to zero. As a result, a digital signal that has the same frequency as the ring-down signal is generated at the output of the comparator as shown in Figure 2-4.

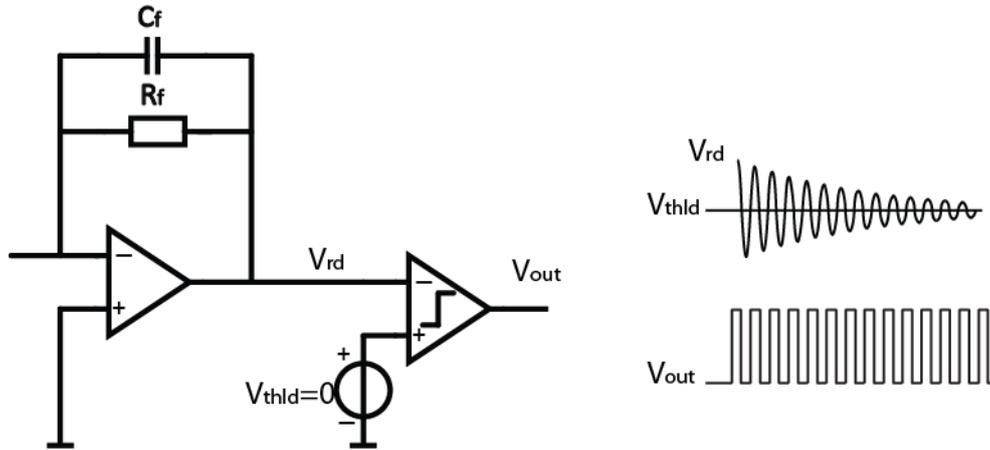


Figure 2-4: Zero-crossing for resonance frequency measurement

Figure 2-5 displays the counting process for calculating the resonance frequency.

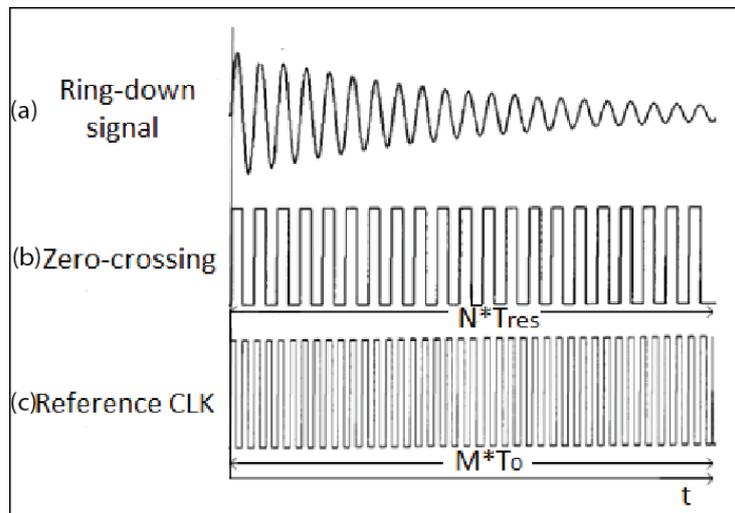


Figure 2-5: Frequency counting process for calculating the resonance frequency. (a) Ring-down signal generated by the I-V converter (b) Digital signal generated by the comparator (c) Reference clock signal [8]

In order to calculate f_{res} , we need to know both the number of the ring-down cycles measured (N) and the measurement time (t) according to the following equation:

$$f_{res} = \frac{1}{T_{res}} = \frac{N}{t} \quad (2-3)$$

To know the measurement time, a reference clock, with a certain known frequency f_0 is applied. The relation between f_{res} and f_0 is indicated:

$$f_{res} = \frac{N}{t} = \frac{N}{M} \cdot f_0 \quad (2-4)$$

where N is the number of ring-down cycles, t is the measurement time, M is the number of reference clock cycles and f_0 is reference clock frequency.

Among these parameters, M and N are the parameters that need to be measured while f_0 is known before counting. There are two measurement methods [8]:

- Method A: measuring the number of reference clock period (M) for a specified number of zero-crossing cycles (N)
- Method B: measuring the number of zero-crossing cycles (N) for a specified number of reference clock cycles (M)

For these two methods, the frequency determined by Equation (2-4) is exact only when the measurement time (t) is an integer multiple of both the ring-down signal period and the reference clock period. When this is not the case, a quantization error is introduced. To reduce the quantization error, we chose method A (section 2.6).

Quality factor measurement: threshold-crossing detection

As displayed in Figure 2-6, to measure the resonance frequency, we apply two different threshold-levels, a_1 and a_2 , to the comparator. As a consequence, two different square-waves are generated at the output of the comparator after threshold-crossing.

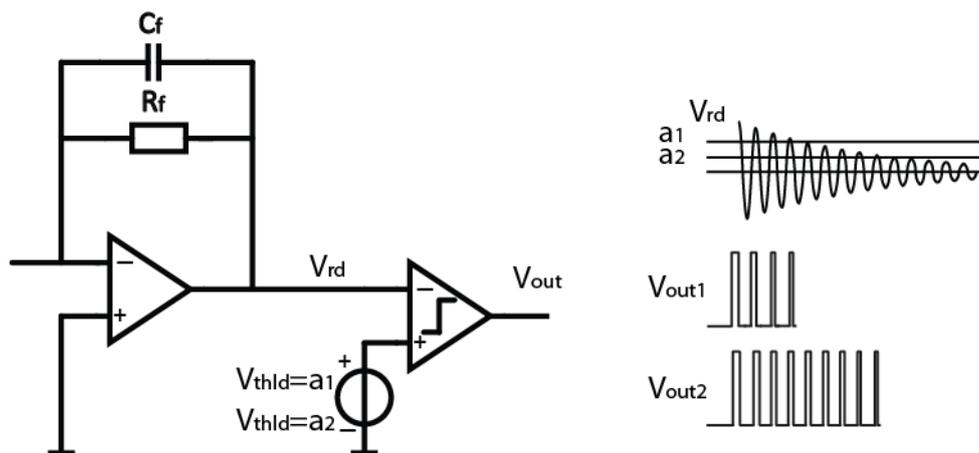


Figure 2-6: Threshold-crossing for quality factor measurement

Figure 2-7 displays the counting process for calculating the quality factor.

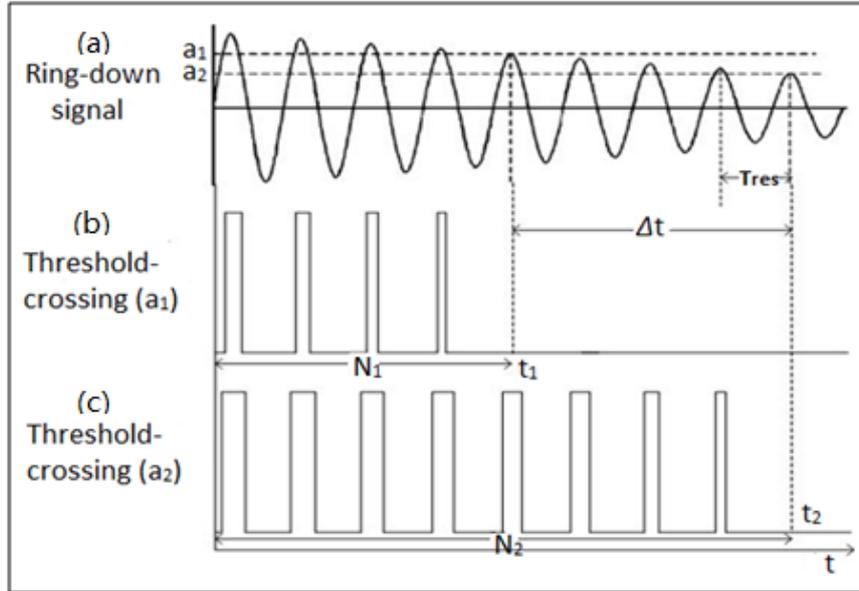


Figure 2-7: Threshold-crossing counting process for calculating the quality factor (a) Ring-down signal generated by I-V converter (b) square-wave generated by the threshold-level (a_1) crossings of the ring-down signal (c) square-wave generated by the threshold-level (a_2) crossings of the ring-down signal [8]

During threshold-crossing detection, the threshold voltage is set to a_1 and a_2 , respectively. As a result, two series of square-waves are generated. The number of cycles obtained by threshold-level a_1 is N_1 , and the number of cycles obtained by a_2 is N_2 . As shown in Figure 2-7, the time t_1 and t_2 can be roughly calculated by the following equation.

$$t_1 \approx N_1 \cdot T_{res} = \frac{N_1}{f_{res}}$$

$$t_2 \approx N_2 \cdot T_{res} = \frac{N_2}{f_{res}}$$

Also according to [3], the relation between a_1 , a_2 and t_1 , t_2 can be expressed by Equation (2-5) and (2-6).

$$a_1 = A_0 \exp(-\alpha \cdot t_1) \quad (2-5)$$

$$a_2 = A_0 \exp(-\alpha \cdot t_2) \quad (2-6)$$

The expression of α can be obtained by dividing Equation (2-5) by Equation (2-6).

$$\alpha = \frac{\ln(a_1/a_2)}{t_2 - t_1} \quad (2-7)$$

Combined with Equation (1-2) (section 1.1.2), the quality factor can be calculated by the following equation.

$$Q = \frac{\pi \cdot \Delta N}{\ln(a_1/a_2)} \quad (2-8)$$

where ΔN is the difference between N_1 and N_2 equal to $N_2 - N_1$. a_1 and a_2 present two different threshold voltages.

2.3 Excitation circuit analysis

An electrical signal is needed to excite the mechanical resonant sensor before measuring the ring-down signal. Hence, we will assume a sinusoidal excitation voltage is utilized. In the following, the requirement on its frequency and amplitude will be analyzed.

Excitation signal frequency

For a specified resonator, the amplitude of the ring-down current that flows through RLC tank depends on the driving frequency.

If the driving frequency is exactly equal to the resonance frequency, the impedance (reactance) of the inductor and capacitor is equivalent but of opposite sign and cancel out [4]. As a result, the impedance of the RLC tank is at minimum with a purely real value equal to R_m . Therefore, the amplitude of ring-down current through the RLC tank is at maximum.

$$i_{RLC} = \frac{V_{dr}}{R_m} \quad (2-9)$$

Where V_{dr} is the amplitude of the driving source and R_m is the resistor of the electrical model.

However, in general, the driving frequency always has a minor difference from the resonance frequency. In this case, the impedance of capacitor and inductor are not equal anymore, so the impedance RLC circuit has an imaginary part. The absolute value of the impedance equals:

$$R_{RLC} = \sqrt{R_m^2 + \left(2\pi f_{dr} \cdot L_m - \frac{1}{2\pi f_{dr} \cdot C_m}\right)^2} \quad (2-10)$$

According to Equation (1-1) and (1-3), L_m and C_m can be also expressed as:

$$L_m = \frac{R_m \cdot Q}{2\pi \cdot f_{res}} \quad (2-11)$$

$$C_m = \frac{1}{2\pi \cdot f_{res} \cdot R_m \cdot Q} \quad (2-12)$$

Substituting Equation (2-11) and (2-12) into Equation (2-10), a formula for R_{RLC} is obtained with

the representation of f_{res} and Q .

$$R_{RLC} = R_m \cdot \sqrt{1 + \left(\frac{f_{dr}}{f_{res}} \cdot Q - \frac{f_{res}}{f_{dr}} \cdot Q\right)^2} \approx R_m \cdot \sqrt{1 + \left(\frac{2\Delta f}{f_{res}} \cdot Q\right)^2} \quad (2-13)$$

where Δf is the difference between driving frequency and resonance frequency equal to $f_{dr} - f_{res}$.

Consequently, when there is a difference between driving frequency and resonance frequency, the current through RLC tank is equal to

$$i_{RLC} = \frac{V_{dr}}{R_m \cdot \sqrt{1 + \left(\frac{2\Delta f}{f_{res}} \cdot Q\right)^2}} \quad (2-14)$$

As indicated in the above equation and shown in Figure 2-8, the further the driving frequency is away from the resonance frequency, the smaller the RLC current will be. Hence, in order to get large amplitude of ring-down current through RLC tank, the driving frequency should be as close as possible to the resonance frequency.

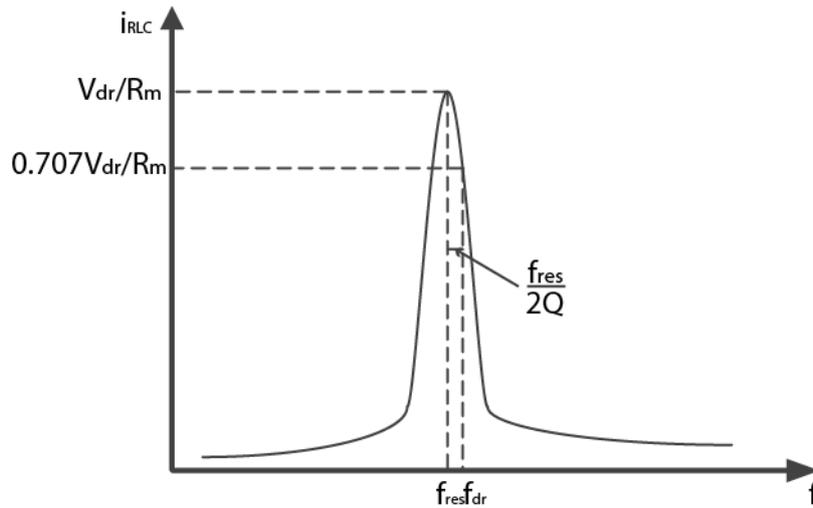


Figure 2-8: Y-axis: current through RLC tank; X-axis: driving frequency

Excitation signal amplitude

In addition to excitation signal frequency, excitation signal amplitude is also a consideration. Due to the property of resonators, the amplitude should be kept within a specified value. Otherwise, the resonator operates in a non-linearity region [2]. So the requirement of excitation signal amplitude is:

$$V_{p-p} = 200mV \quad (2-15)$$

In conclusion, the excitation source is a sine-wave with 200mV amplitude, the frequency of which is as close as possible to the resonance frequency.

2.4 Front-end circuit analysis

At the beginning of this section, based on an introduction of timing jitter, a requirement for signal-to-noise ratio (SNR) is derived to achieve the detection limit. This is followed by a noise analysis and output signal amplitude analysis, respectively. In the end, a trans-conductance requirement for the amplifier is given.

2.4.1 Timing Jitter

In this sub-section, the relation between timing jitter and noise in the circuit is introduced. In Figure 2-9, when there is a noise voltage (ΔV) at the output of the amplifier (or the input of the comparator), this noise will result in the ring-down voltage reaching the threshold voltage earlier or later. Therefore, a timing jitter (Δt) is caused by noise [5].

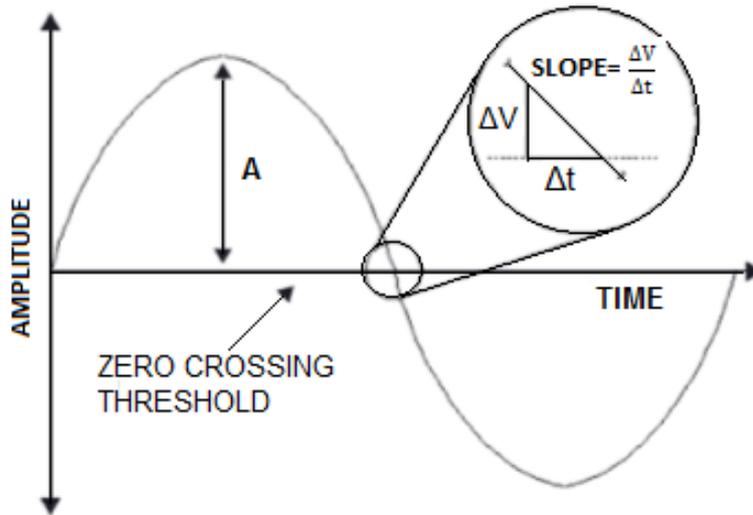


Figure 2-9: Timing jitter caused by noise voltage [8]

In order to get the mathematical relation of ΔV and Δt , the slope of the ring-down curve at the zero-crossing point is calculated first. According to [3], the sinusoid ring-down voltage with exponentially decaying amplitude can be expressed mathematically by:

$$V(t) = A_0 \cdot e^{-\alpha t} \cdot \sin(2\pi f_{res} \cdot t) \quad (2-16)$$

Together with the condition at zero-crossing point,

$$\sin(2\pi f_{res} \cdot t) = 0$$

$$\cos(2\pi f_{res} \cdot t) = -1$$

The slope of the sine-wave at its zero crossings is derived by the derivative of Equation (2-16).

$$\left| \frac{\Delta V}{\Delta t} \right| = 2\pi f_{\text{res}} \cdot A_0 \cdot e^{-\alpha t} \quad (2-17)$$

According to Equation (1-2), the attenuation parameter α can be expressed as:

$$\alpha = \frac{\omega}{2 \cdot Q} = \frac{2\pi \cdot f_{\text{res}}}{2 \cdot Q} \quad (2-18)$$

In the meantime, the measurement time t can be estimated by:

$$t = \frac{N}{f_{\text{res}}} \quad (2-19)$$

By substituting the RMS noise voltage ($V_{n,\text{RMS}}$) for ΔV , the expression for the RMS timing jitter (Δt) in terms of the initial ring-down signal amplitude (A_0), the RMS noise voltage and the ratio of N and Q is obtained as:

$$\Delta t = \frac{V_{n,\text{RMS}}}{2 \cdot \pi \cdot f_{\text{res}} \cdot A_0 \cdot e^{-\frac{\pi \cdot N}{Q}}}$$

As indicated by this equation, the timing jitter corresponding to the last zero crossing in the measurement time is the most critical one. As to the number of zero-crossing measured (N), it depends on the value of the quality factor (Q). by assuming $N=Q$, we get the expression for the maximum timing jitter with respect to the initial ring-down signal amplitude (A_0), the RMS noise voltage ($V_{n,\text{RMS}}$):

$$\Delta t = \frac{V_{n,\text{RMS}}}{2 \cdot \pi \cdot f_{\text{res}} \cdot A_0 \cdot e^{-\pi}} \quad (2-20)$$

2.4.2 Signal-to-Noise ratio requirement

In this part, the signal-to-noise ratio requirement is discussed. Firstly, to obtain the signal-to noise ratio requirement, the relation between timing jitter and detection limit is analyzed. Based on Equation (2-4) (section 2.2.2), the resonance frequency can be expressed by:

$$f_{\text{res}} = \frac{N}{t} = \frac{N}{M} \cdot f_0$$

When there is timing jitter caused by noise voltage, the shift of the frequency can be calculated as:

$$\Delta f_{\text{res}} = \frac{N}{t} - \frac{N}{t + \Delta t} \approx \frac{N \cdot \Delta t}{t^2}$$

where Δt is the timing jitter and t is the measurement time equal to N/f_{res} .

Consequently, the requirement on the detection limit given by Equation (2-1),

$$\frac{\Delta f_{\text{res}}}{f_{\text{res}}} = \frac{\Delta t}{t} < 10^{-4} \quad (2-21)$$

Combined with Equation (2-20) results in:

$$\frac{\Delta f_{\text{res}}}{f_{\text{res}}} = \frac{\Delta t}{t} = \frac{V_{n,\text{RMS}}}{2 \cdot \pi \cdot N \cdot A_0 \cdot e^{-\pi}} < 10^{-4} \quad (2-22)$$

Equation (2-22) implies that for a given N, the resonance frequency detection limit defines a SNR requirement, where we define SNR $A_0/V_{n,\text{RMS}}$. If we again assume $N=Q=300$, we obtain the maximum requirement for signal-to- noise ratio:

$$\text{SNR} = \frac{A_0}{V_{n,\text{RMS}}} > 130 \quad (2-23)$$

If Q is bigger than 300, the requirement for signal-to-noise ratio is lower than that of our assumption as shown in Figure 2-10. Therefore, the maximum requirement for signal-to-noise ratio is 130.

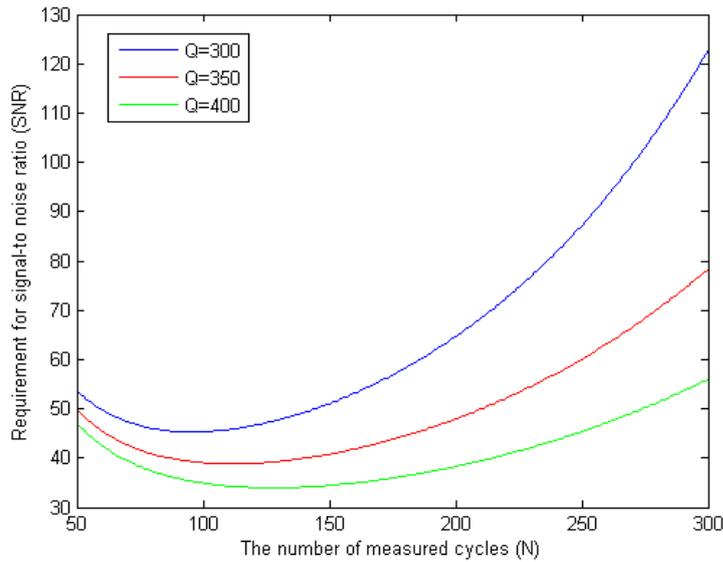


Figure 2-10: Requirement for SNR vs. Q

2.4.3 Noise analysis

In this subsection, in order to understand how thermal noise limits the detection limit in detail, and derive the trans-conductance (g_m) requirement of the amplifier, the noise in the front-end circuit is analyzed to get an expression for the signal-to-noise ratio.

As shown in Figure 2-11, three noise sources are analyzed for the front-end circuit: the noise

generated by R_m ($V_{n,m}$), the noise generated by feedback resistor ($V_{n,f}$) and the noise of the OTA ($V_{n,a}$). The noise generated by R_m can be negligible because it is filtered by the RLC tank. The noise generated by the feedback resistors is added to the output of the amplifier directly. The noise of the OTA is amplified by a factor of $g_m \cdot R_f$ at high frequencies (see Figure 2-11). Therefore, the noise in the front-end circuit is dominated by the noise of the OTA.

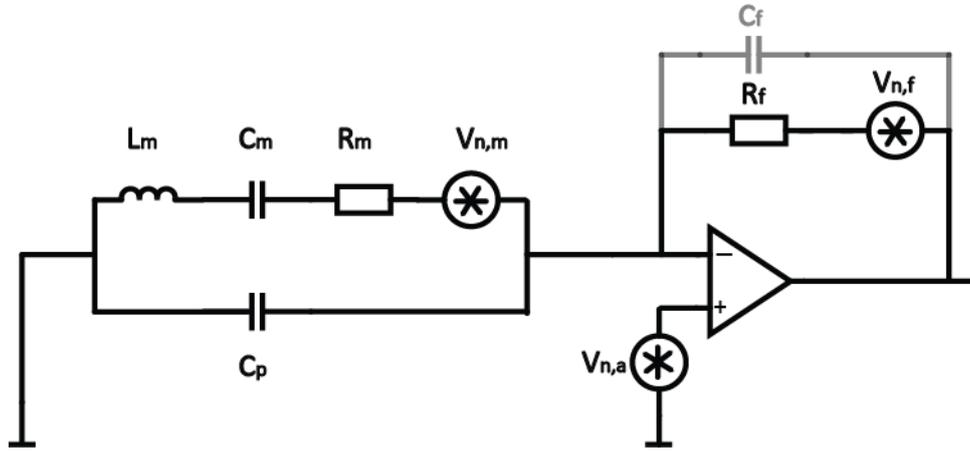


Figure 2-11: Noise sources in the front-end circuit

In our work, a resistive feedback for the I-V converter is applied to cancel the leakage current problems caused by capacitive feedback (Chapter 1, section 1.2.2). However, the integrated output noise in this architecture is excessively large (theoretically infinite if the OTA would have infinite bandwidth) without adding a parallel capacitor. The noise spectrum without shaping by such a capacitor is shown in Figure 2-12.

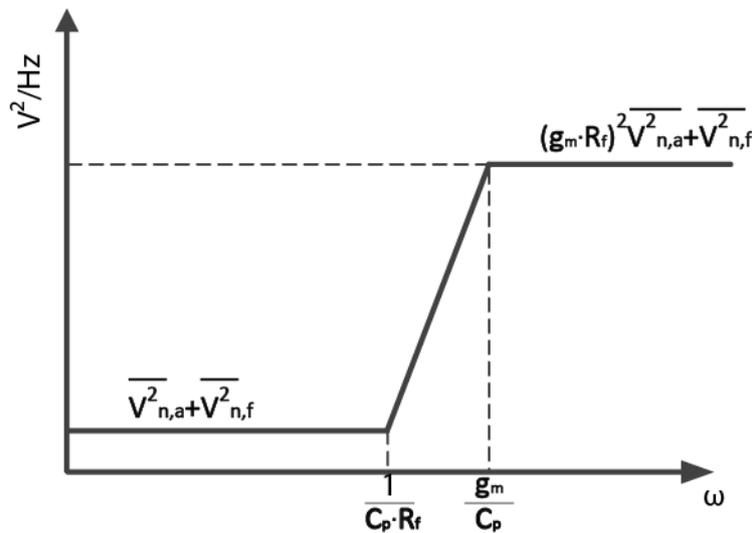


Figure 2-12: Noise spectrum without parallel capacitor

The feedback resistor results in a zero ($1/R_f \cdot C_p$) while the OTA causes a pole (g_m/C_p). At lower

frequency, the noise is dominated by $V_{n,a}$ and $V_{n,f}$. At higher frequency, the noise is dominated by the amplified $V_{n,a}$ and $V_{n,f}$. Hence, the integrated noise will be increasing with frequency. To limit this noise, a small capacitor is added to introduce a pole at $1/R_f \cdot C_f$. After adding a capacitor in parallel with the feedback resistor, the noise at higher frequency is filtered by this capacitor. The noise spectrum shaping by the parallel capacitor is shown in Figure 2-13. Here, we assume the pole introduced by the parallel capacitor is higher than the pole generated by the OTA. In this case, the signal is not influenced by C_f , because the bandwidth of the OTA is $g_m/2\pi C_p$. If the pole introduced by C_f is lower than the pole of the OTA, the signal is also reduced by C_f .

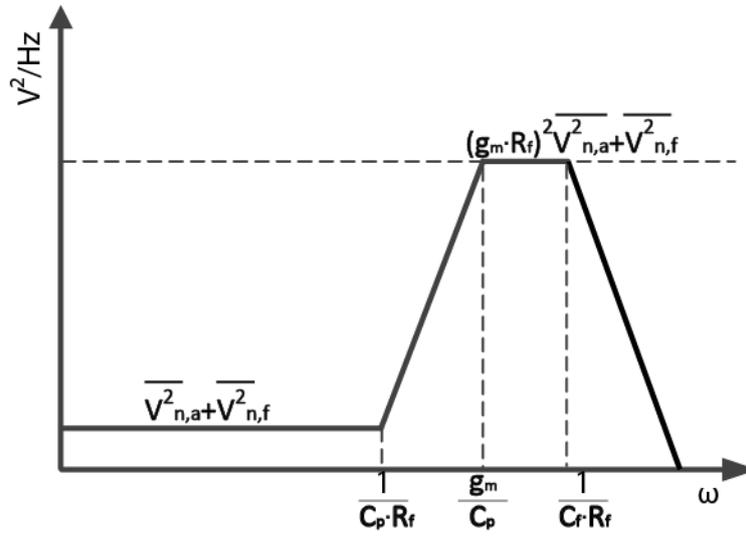


Figure 2-13: Noise spectrum shaping by a parallel capacitor

The integrated noise is calculated after adding a capacitor and the process is shown in Appendix I. All the calculations assume the amplifier is an ideal voltage-controlled current source with infinite DC gain. In order to calculate $V_{n,a}$, thermal noise for a MOSFET can be modeled by a current source in parallel with the channel. The noise currents of the input device can be represented by an equivalent noise voltage source at its gate terminal, with a power spectral density (PSD) of $(8/3)kT/g_m$ [6]. The final equation is shown as the following equation:

$$V_{n,RMS} = \sqrt{\frac{k \cdot T \cdot (5 \cdot C_p + 2 \cdot C_f)}{3 \cdot C_f \cdot C_p} - \frac{2 \cdot k \cdot T \cdot C_p}{3 \cdot g_m \cdot C_f \cdot R_f \cdot (C_p + C_f)}} \quad (2-24)$$

This equation is obtained by assuming the pole introduced by feedback capacitor is between the zero caused by the feedback resistor and the pole generated by the OTA.

2.4.4 Output signal amplitude analysis

In order to get the signal-to-noise ratio, in addition to analyzing the noise, it is also necessary to

analyze the initial amplitude of the output signal A_0 . The calculation of A_0 is explained in three steps: calculation of the ring-down current through the RLC tank (i_{RLC}), calculation of the ring-down current flowing into the amplifier (i_0) and calculation of ring-down voltage after amplification by the I-V converter (A_0).

Firstly, we compute the ring-down current through the RLC tank (i_{RLC}). For simplicity, we assume the excitation frequency is exactly equal to the resonance frequency. As discussed in section 2.3, this current can be calculated by Equation (2-9) (section 2.3).

Secondly, the ring-down current flowing into the amplifier (i_0) is calculated. In order to calculate i_0 , the I-V converter can be modeled as a resistor with a value of $1/g_m$ (input impedance of the I-V converter), where g_m is the trans-conductance of the OTA. Hence, as shown in Figure 2-14, we have a current divider model.

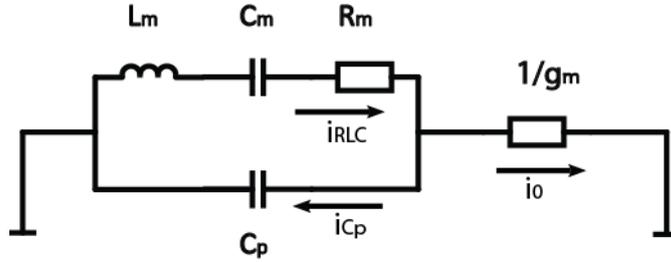


Figure 2-14: Current divider model

It can be seen from the figure that the current through RLC tank is divided into two parts. One part (i_0) flows into the amplifier while the other part (i_{Cp}) is dissipated by the parasitic capacitor. According to the impedance ratio of these two parts, the current flowing into the amplifier can be calculated as:

$$i_0 = i_{RLC} \cdot \frac{g_m}{\sqrt{g_m^2 + (2 \cdot \pi \cdot f_{res} \cdot C_p)^2}}$$

Combining with Equation (2-9) results in:

$$i_0 = \frac{V_{dr}}{R_m} \cdot \frac{g_m}{\sqrt{g_m^2 + (2 \cdot \pi \cdot f_{res} \cdot C_p)^2}} \quad (2-25)$$

Finally, i_0 is amplified into a ring-down voltage by the feedback resistor. Due to the parallel capacitor, the ring-down signal is also filtered by this capacitor. The ring-down is converted into a ring-down voltage by a factor of feedback impedance. The feedback impedance is:

$$R_o = R_f \parallel \frac{1}{j \cdot 2 \cdot \pi \cdot f_{res} \cdot C_f}$$

Consequently, the initial amplitude of ring-down voltage A_0 is:

$$A_0 = \frac{V_{dr}}{R_m} \cdot \frac{g_m}{\sqrt{g_m^2 + (2 \cdot \pi \cdot f_{res} \cdot C_p)^2}} \cdot \frac{R_f}{\sqrt{1 + (2 \cdot \pi \cdot f_{res} \cdot C_f \cdot R_f)^2}} \quad (2-26)$$

2.4.5 Trans-conductance requirement

Base on the discussion in two previous subsections, we know the expression for the noise voltage and the initial amplitude of ring-down voltage. In this subsection, the trans-conductance requirement is given by the analysis of SNR and the initial ring-down voltage.

- Analysis of the trans-conductance requirement based on SNR

Firstly, we analyze the choice of C_f . As shown in Equation (2-24) and Figure 2-15, the noise decreases with an increasing C_f . In the meantime, if the bandwidth is reduced to less than the resonance frequency by the introduction of C_f , the amplitude of the ring-down signal will be reduced. So there is an optimum value for the C_f with a given R_f for the largest SNR, which will correspond to a bandwidth a bit less than the resonance frequency. Using the expressions for $V_{n,RMS}$ and A_0 , and, and assuming $C_p \gg C_f$, SNR can be calculated by:

$$SNR = \frac{V_{dr}}{R_m} \cdot \frac{1}{\sqrt{1 + \left(\frac{2\pi f_{res} C_p}{g_m}\right)^2}} \cdot \frac{R_f}{\sqrt{1 + (2\pi f_{res} C_f R_f)^2}} \cdot \sqrt{\frac{kT}{3C_f} \left(5 - \frac{2}{g_m \cdot R_f}\right) + \frac{5kT}{3C_p}} \quad (2-27)$$

Since the calculation is complex, the optimization is done by simulation.

As for g_m , the input equivalent noise reduces with increasing g_m , but the gain of the noise increases with an increasing g_m . As a consequence, the noise still increases with a bigger g_m . At the same time, with a bigger g_m , more current will flow into the amplifier, so that A_0 will be larger. As a result, SNR increases with an increasing g_m . Hence, for a given bandwidth (i.e. for a given value of C_f) we can find a minimum g_m that supports the required SNR.

We use the resonator used in the preceding work as an example to make a comparison. The parameters for this resonator are as follows [8]:

- $R_m = 126k\Omega$, $L_m = 3.01H$, $C_m = 2.16fF$, $C_p = 5.48pF$
- $f_{res} = 1.977MHz$, $Q = 297$

We assume the feedback resistor is about five times R_m , i.e. $630k\Omega$. The simulated SNR as a function of bandwidth for different value of g_m are shown in Figure 2-15. It can be seen from the

graph that there is an optimum value of bandwidth for a given g_m , and this optimum value decreases when g_m increases.

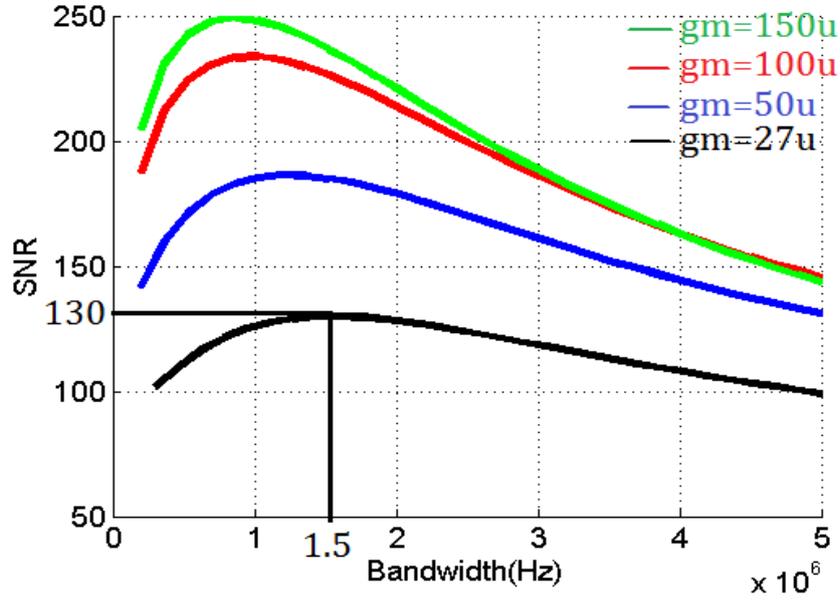


Figure 2-15: Optimum value of bandwidth with different g_m

Based on the simulation result, we have the requirement for g_m equal to $27\mu S$ with an optimum bandwidth of 1.5MHz. However, since this optimum bandwidth is smaller than the resonance frequency, and since at this g_m a significant fraction of the ring-down current flows into the parasitic capacitance C_p , it leads to very small initial amplitude of the ring-down signal of only 57mV.

➤ Analysis of the trans-conductance requirement based on A_0

Since our ring-down signal has exponentially decaying amplitude, after N cycles, the amplitude will be much smaller than the initial value. As mentioned in section 2.4.1, the amplitude after N cycles should be:

$$A_N = A_0 \cdot e^{-\frac{\pi \cdot N}{Q}}$$

In order to make the amplitude after N cycles still readable, the initial amplitude should be more than 500mV. With initial amplitude of 500mV, after 300 cycles, we have amplitude of 20mV left, which is necessary for our design. We know the expression for A_0 as shown in Equation (2-26).

$$A_0 = \frac{V_{dr}}{R_m} \cdot \frac{g_m}{\sqrt{g_m^2 + (2 \cdot \pi \cdot f_{res} \cdot C_p)^2}} \cdot \frac{R_f}{\sqrt{1 + (2 \cdot \pi \cdot f_{res} \cdot C_f \cdot R_f)^2}}$$

As shown in above equation, there are three ways to increase A_0 . Firstly, A_0 can be increased by

increasing the bandwidth introduced by feedback capacitor. This method is not a good choice since it will increase the noise at the same time. Secondly, we can increase g_m , to make more current though RLC tank flow into the amplifier. However, larger g_m will consume more energy, which leads to high energy consumption. Therefore, to make our circuit more energy-efficient, we choose the third method. By applying larger feedback resistor to enlarge the gain of the amplifier, then even the current flowing into the feedback resistor is small due to small g_m , the initial amplitude is still amplified to a large value. By only increasing R_f , we get the requirement for R_f as follows:

$$R_f = 5.42\text{M}\Omega = 43 \cdot R_m$$

The range of R_m is from 100k Ω to 500k Ω , and then the range of the feedback resistor can be estimated from 4.3M Ω to 21.5M Ω . However, this will lead to a large die area and not practical. So we set the bandwidth around the resonance frequency and increase g_m a bit to make most current flowing into the I-V converter and to get a reasonable value of the feedback resistor.

Finally, we get the requirement for g_m is 81 μS . And the feedback resistor is 2.3M Ω with a feedback capacitor of 35fF. According to [8], the requirement for g_m in prior work is 300 μS , which is bigger than 81 μS that we get from our architecture design. Hence, our design is potentially more energy efficient than prior art.

To make a reconfigurable circuit, the simplest way is to make the feedback capacitor and resistor programmable to measure different resonators. The configurability of the design is described in detail in Chapter 3, section 3.1. Based on simulation, to meet the requirement for all the resonators we want to measure (see the parameter range of the resonators in section 2.1), the requirement for g_m is 200 μS .

2.5 Comparator analysis

In addition to the front-end circuit, the comparator is also an important part in the system. In this section, two requirements on the comparator are analyzed: propagation delay and input offset.

Propagation delay

The comparator delay has an influence on the detection limit. A delay in the comparator results in an error in the measurement. Figure 2-16 demonstrates the influence of the propagation delay.

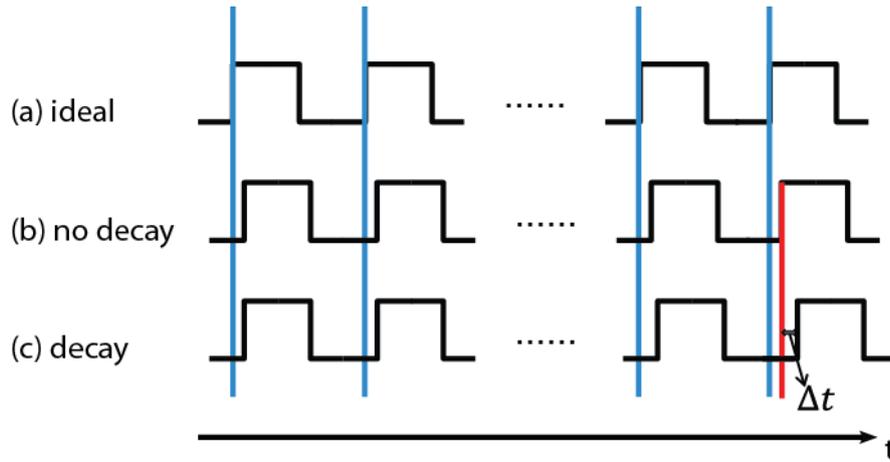


Figure 2-16: Influence of propagation delay: (a) ideal situation without delay (b) the situation when ring-down voltage is not a decaying signal (c) the situation when ring-down voltage is a decaying signal

If the comparator doesn't generate any delay time, an exact zero-crossing result will be achieved at the output of the comparator (Figure 2-16(a)). Otherwise, propagation delay will cause an error during zero-crossing detection as shown in Figure 2-16(b) and (c). As long as the first and last ring-down cycles experience the same time delay as shown in (b), no error occurs in the measurement time. However, the ring-down voltage has exponentially decaying amplitude. Since the propagation delay depends on the overdrive applied to the input of the comparator [7], the delay time for the first and last cycle is distinct because of different overdrive. The delay of the last cycle is the longest one due to its smallest overdrive voltage. Therefore, detection limit is influenced by the difference between the delay of the first cycle and the delay of the last cycle (Δt). The relation between them is:

$$\frac{\Delta f_{\text{res}}}{f_{\text{res}}} = \frac{\Delta t}{t} = \frac{\Delta t \cdot f_{\text{res}}}{N} < 10^{-4} \quad (2-28)$$

where f_{res} is from 300kHz to 800kHz and Q is from 300 to 400.

Substituting the parameters into Equation (2-28), we get:

$$\Delta t < 37.5\text{ns}$$

As long as the delay time corresponding to the last sine-wave meets this requirement, the difference in delay between the first cycle and the last cycle meets the requirement as well. Hence, the requirement for the comparator is:

$$\Delta t_{\text{p-last}} < 37.5\text{ns} \quad (2-29)$$

Input offset

A constant input offset of the comparator only reduces the number of cycles measured. It

doesn't have an impact on the resonant frequency measured. To make sure enough cycles can be detected, the offset should be smaller than the ring-down voltage of the last cycle. As a result, the requirement for input offset is:

$$V_{\text{offset}} < 20mV \quad (2-30)$$

This DC input offset can be compensated by auto-zeroing the comparator at the beginning of the measurement time. There are two operating phase of the comparator involved:

- Comparator auto-zeroing phase

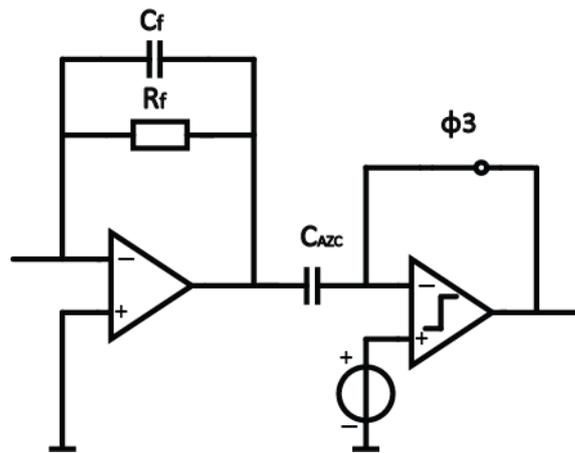


Figure 2-17: Comparator working at auto-zeroing phase

In this step, switch 3 is closed. The comparator is configured as unity-gain buffer (Figure 2-17). The offset is sampled and stored on C_{AZC} .

- Zero-crossing detection phase

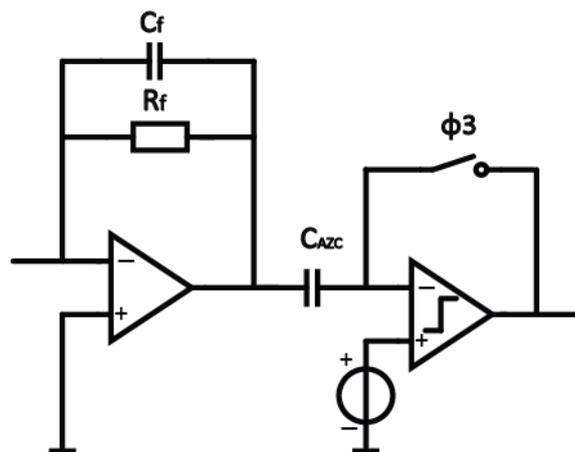


Figure 2-18: Comparator working at zero-crossing phase

In this step, switch 3 is open. The comparator is open loop and used as a zero-crossing detector. Both excitation phase and ring-down phase happen during this zero-crossing phase.

In conclusion, until now, we have three operating phases for the measurement: comparator auto-zeroing phase, excitation phase and ring-down phase.

2.6 Counting circuitry analysis

In this section, the quantization error introduced by counting circuitry is analyzed. After zero-crossing detection, a counting circuitry is applied off-chip to extract the information of the resonance frequency and quality factor. As discussed in section 2.2.2, two measurement methods are mentioned. And both of them result in a frequency uncertainty Δf_{res} , which will be explained as follows:

- Method A: measuring the number of reference clock periods (M) for a specified number of zero-crossing cycles (N)

In the time interval of N ring-down cycles, there could be M or M+1 clock ticks ($M \gg 1$). The frequency uncertainty Δf_{res} is:

$$\Delta f_{res} = \frac{N}{M} \cdot f_0 - \frac{N}{M+1} \cdot f_0 = \frac{N}{M \cdot (M+1)} \cdot f_0 \approx \frac{N}{M^2} \cdot f_0 = \frac{f_{res}^2}{N \cdot f_0} \quad (2-31)$$

Dividing Equation (2-31) by f_{res} , we get the detection limit:

$$\frac{\Delta f_{res}}{f_{res}} = \frac{f_{res}}{N \cdot f_0} < 10^{-4} \quad (2-32)$$

Where f_{res} is from 300kHz to 800kHz and Q is from 300 to 400.

Based on the Equation (2-32) and the values of the parameters, as long as the frequency of the reference clock is bigger than 25MHz, the detection limit will be realized.

- Method B: measuring the number of zero-crossing cycles (N) for a specified number of reference clock cycles (M)

In the time interval of M reference clock cycles, there could be N or N+1 zero-crossing ticks ($M \gg 1$). The frequency uncertainty Δf_{res} is:

$$\Delta f_{res} = \frac{N+1}{M} \cdot f_0 - \frac{N}{M} \cdot f_0 = \frac{1}{M} \cdot f_0 = \frac{f_{res}}{N} \quad (2-33)$$

Dividing Equation (2-33) by f_{res} , we get the detection limit:

$$\frac{\Delta f_{res}}{f_{res}} = \frac{1}{N} < 10^{-4}$$

Based on the above equation, the number of zero-crossing cycles measured should be more than ten thousand, which is not feasible in our work.

Therefore, method A is chosen in our work. And in order to reduce the quantization error and fulfill the detection limit, the reference frequency should be at least 25MHz.

2.7 Simulation results

To do the architecture-level simulation, we choose one of the samples we have as an example.

The parameters for this resonator are:

- $R_m = 390.9\text{k}\Omega$, $L_m = 51.07\text{H}$, $C_m = 1731\text{aF}$, $C_p = 4.199\text{pF}$
- $f_{\text{res}} = 535.2\text{kHz}$, $Q = 439.3$

The parameters for the feedback network are:

- $C_f = 75\text{fF}$
- $R_f = 3.7\text{M}\Omega$

We use a voltage-controlled-current-source (vccs) with a trans-conductance of $200\mu\text{S}$ as an ideal OTA; and a voltage-controlled-voltage-source (vcvs) with a high voltage gain and a 3.3V output voltage range as an ideal comparator. We apply a sine-wave with 100mV amplitude, and 535.2kHz frequency as the excitation source. All the switches are ideal, with the control signals shown in Figure 2-19.

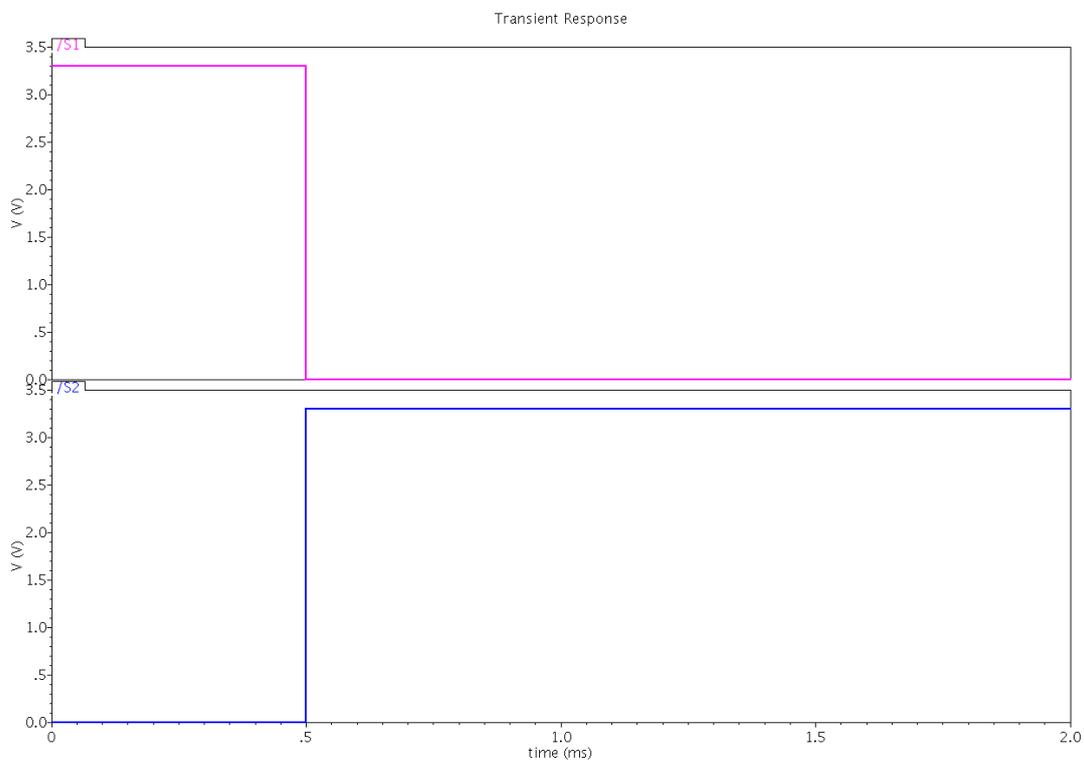


Figure 2-19: Timing of the control signals

The simulation results are shown in Figure 2-20. Since all the models we use in the architecture design are ideal, the auto-zeroing of the comparator is not applied in this simulation. In the excitation phase, the resonator is energized by the excitation signal (switched excitation signal in Figure 2-20). In the integration phase, the ring-down signal is generated (Out_ivconverter in Figure 2-20), and the comparator starts to detect the zero-crossings, producing square waves at the output (Out_comparator in Figure 2-20).

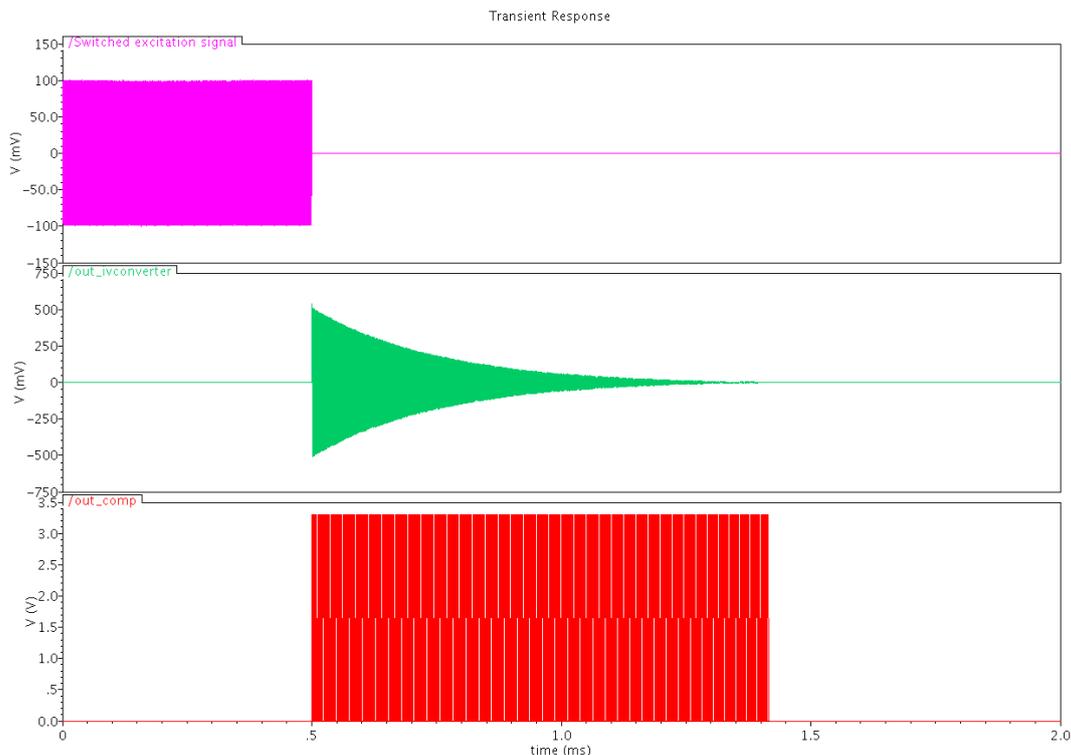


Figure 2-20: Simulation results

It can be seen from the graph that the initial amplitude of the ring-down signal is about 500mV. And the energy consumption can be estimated to be lower than prior art owing to the lower trans-conductance.

2.8 Conclusions

In this chapter, the architecture-level analysis and design of the readout circuit have been presented. The target specifications including detection limit, configurability and energy consumption have been introduced. The operating principles of different sub-blocks, including front-end circuit, comparator and counting circuitry have been explained. Then each sub-block has been analyzed separately. For the front-end circuit, the signal-to-noise ratio requirement has been derived by analyzing the timing jitter. And the resulting trans-conductance requirement has been obtained by analyzing the thermal noise and signal amplitude. In terms of the comparator,

two chief requirements, propagation delay and input offset, have been analyzed. And the minimum reference frequency for the counting circuitry has been derived. The requirements are concluded in Table 2-2.

| Architecture | Requirements |
|--------------------|--|
| Excitation circuit | $V_{p-p}=200\text{mV}$ |
| | f_{dr} as close as possible to f_{res} |
| I-V converter | $g_m=200\mu\text{S}$ |
| Comparator | $t_{p-last}<37.5\text{ns}$ |
| | $V_{off}<21\text{mV}$ |
| Counting circuitry | Reference frequency $> 25\text{MHz}$ |

Table 2-2: Requirements for each block

References

- [1] D. M. Karabacak, "Enhanced sensitivity volatile detection with low power integrated micromechanical resonators", *Lab on a Chip*, vol. 10, pp. 1976-1982, Apr. 2010.
- [2] D. M. Karabacak, Z. Zeng, Private Communication
- [3] K. Zeng, "Threshold-crossing counting technique for damping factor determination of resonator sensors", *Rev. Sci. Instrum*, vol. 75, pp. 5257-5261, Dec. 2004.
- [4] RLC circuit, Wikipedia, http://en.wikipedia.org/wiki/RLC_circuit
- [5] "Random Noise Contribution to Timing Jitter—Theory and Practice", Maxim Integrated Products, Application Note, June 2007
- [6] R. Schreier, J. Silva, J. Steensgaard, G. C. Temes, "Design-oriented estimation of thermal noise in switched-capacitor circuits", *IEEE Transaction Circuits and System*, vol. 52, no. 11, Nov. 2005.
- [7] P.E.Allen, "Characterization of comparators", lecture note, lecture 360, http://users.ece.gatech.edu/pallen/Academic/ECE_6412/Spring_2003/L360-Char_Comparators-2UP.pdf, 2002.
- [8] Z.Zeng, "Energy-efficient Readout of Resonant Sensors", Master thesis, October 2011.

Chapter 3

Circuit-level Analysis and Design

In this chapter, the circuit-level analysis and design for the readout circuit are presented. The design of the front-end circuit is analyzed in several aspects, including programmable feedback network, the I-V converter, and the associated switches. This is followed by the design of the auto-zeroed comparator and counting circuitry. After that, an overview of the simulation results is given, with a conclusion in the end.

3.1 Programmable feedback network

In order to implement the target of configurability, the feedback network should be made programmable to enable the measurement of various sensors. In this subsection, we firstly introduce the T-type feedback network used and then give the design for the switchable feedback resistors and capacitors.

3.1.1 T-type feedback resistor network

As explained in section 2.4.5, to be energy-efficient, the feedback resistance should be large, which result in large die area. To solve this problem, a T-type resistor network (Figure 3-1) is used.

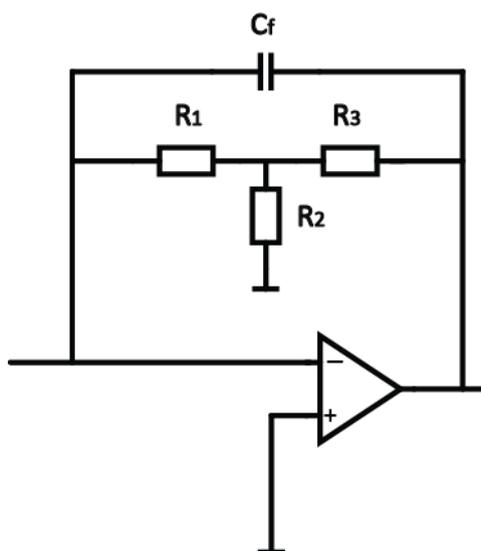


Figure 3-1: Front-end circuit with T-type resistor network

According to [1], the effective resistance of this T-type network can be expressed as:

$$R_{\text{eff}} = R_1 + R_3 + \frac{R_1 \cdot R_3}{R_2} \quad (3-1)$$

Therefore, by using relatively small resistances, a large effective resistance can be achieved, which reduce the cost of the die area.

3.1.2 Switchable feedback resistors and capacitors

In this subsection, the design of switchable feedback resistors and capacitors is introduced to make the circuit applicable to different resonators.

Switchable feedback resistors

As discussed in section 2.1, the resistance of resonators ranges from 100kΩ to 500kΩ. Hence, to enable the circuit to operate with different resonators, the T-type feedback network has been designed as shown in Figure 3-2.

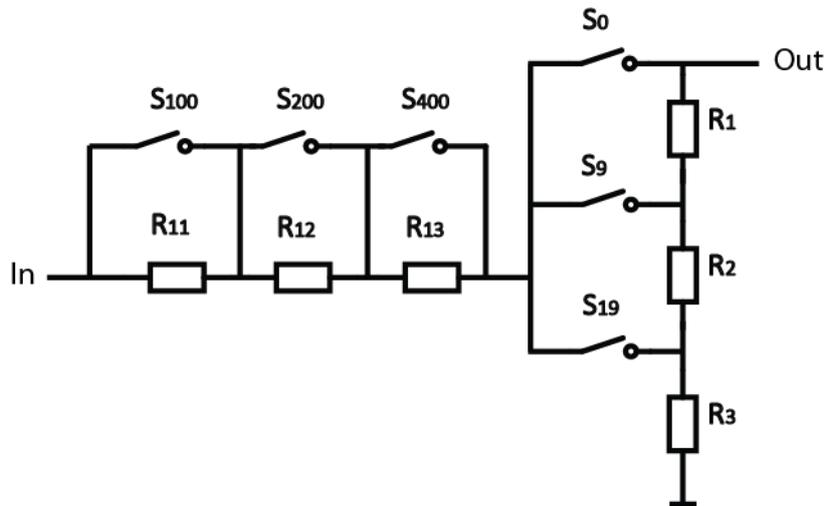


Figure 3-2: Switchable feedback resistors

Based on the simulation results presented in Chapter 2, section 2.7, we know that we need a feedback resistor equal to 3.7MΩ when R_m equals 390kΩ. We can roughly estimate that the values of the feedback resistor should be from 950kΩ to 4.75MΩ. Hence, the following values are chosen for the resistors:

- $R_{11} = 100\text{k}\Omega$, $R_{12} = 200\text{k}\Omega$, $R_{13} = 400\text{k}\Omega$
- $R_1 = 900\text{k}\Omega$, $R_2 = 50\text{k}\Omega$, $R_3 = 50\text{k}\Omega$

With the series resistance of 100kΩ, 200kΩ and 400kΩ, by controlling the switches (S_{100} , S_{200} and

S_{400}), we can get eight combinations from 100k Ω to 700k Ω . And by tuning the switches (S_0 , S_9 and S_{19}), we can get multiplication factors of 1, 9 or 19.

Switchable feedback capacitors

The feedback capacitor is used for limiting the noise. To make the circuit programmable, the feedback capacitors have been designed as shown in Figure 3-3.

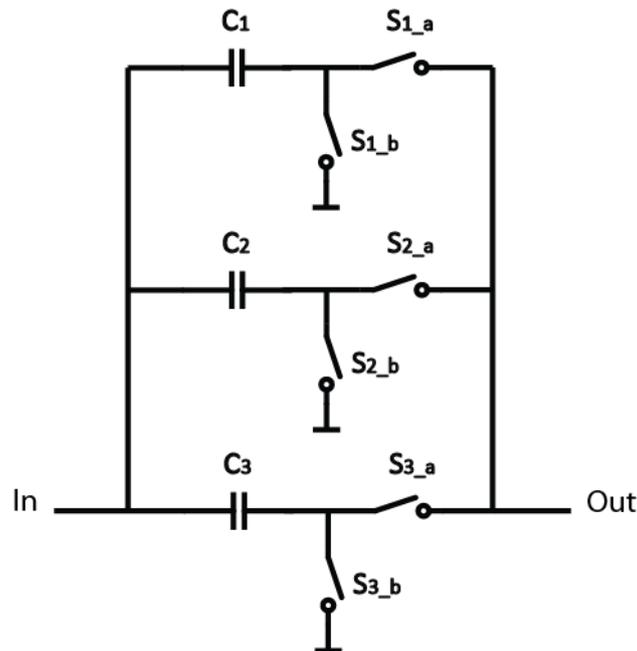


Figure 3-3: Switchable feedback capacitors

Based on the simulation result, the following values are selected for the capacitors:

- $C_1 = 25\text{fF}$
- $C_2 = 50\text{fF}$
- $C_3 = 100\text{fF}$

Consequently, we have eight combinations of feedback capacitance, from 25fF to 175fF. Two switches with complementary control signals (S_{j_a} and S_{j_b} , with $1 \leq j \leq 3$) have been employed to connect or disconnect the capacitor in each path. The switches are at the output side of the I-V converter (“Out” in Figure 3-3). Hence, when the capacitors are not selected, they are connected with the input node of the I-V converter (“In” in Figure 3-3). Then they are added to the parasitic capacitance C_p without changing the output capacitance.

3.2 I-V converter

In this subsection, the design of the I-V converter is discussed. We start with a design using one single transistor, and then improve the circuit by implementing an auto-zeroing technique and adding a cascode stage and an output stage. Finally, the stability of the amplifier is considered.

3.2.1 A single transistor

The function of the I-V converter is to convert the small ring-down current into a readable output ring-down voltage. With a single transistor, this can be realized. Therefore, to make energy consumption as low as possible, we start with a simple single-transistor design. Initially, we use ideal switches and an ideal biasing circuit as shown in Figure 3-4. And also one side of R_2 is connected with a common-mode voltage to set the DC operating voltage at the output.

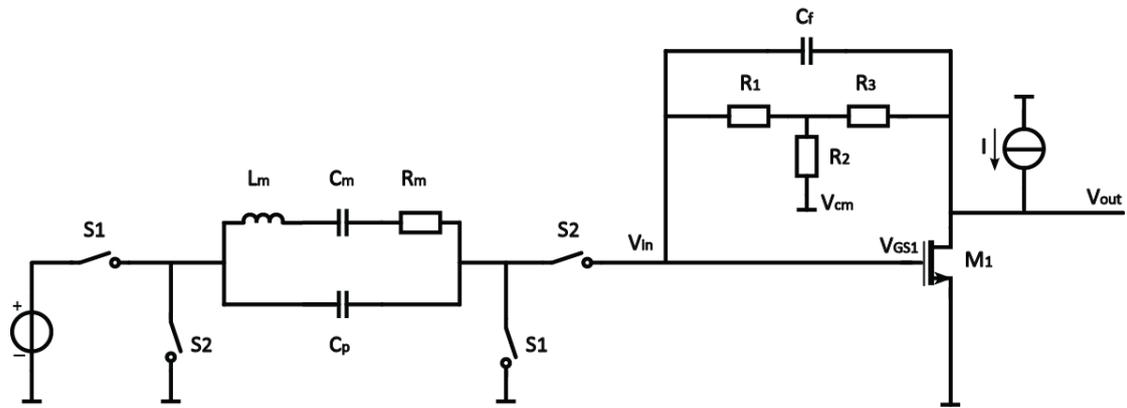


Figure 3-4: I-V converter with a single transistor

In order to make an energy-efficient interface, we make this single transistor work in its weak-inversion region to maximize the trans-conductance-to-current ratio: $g_m/I_D \approx 20$. Therefore, to achieve the g_m requirement ($g_m = 200 \mu S$, Chapter 2, section 2.4.5), a bias current (I in Figure 3-4) of $10 \mu A$ is required.

Due to our feedback resistor network, there is a DC path from the input of the I-V converter to the output V_{out} , which influences the DC operating voltage at V_{out} . During the ring-down phase, this voltage can be expressed by the following equation:

$$V_{out} = V_{cm} + (V_{in} - V_{cm}) \cdot \frac{R_2 + R_3}{R_2} \quad (3-2)$$

where V_{in} is equal to the gate-source voltage of the transistor (around 600mV) and V_{cm} is the common-mode voltage for the biasing.

This shows that the output DC operating point can be set to a desired value (e.g. halfway between the supplies to maximize the output swing) by choosing an appropriate value for V_{cm} . However, the value of feedback resistors varies with different resonators, which causes the DC

operating point to change, and influences the headroom at the output. To solve this problem, the DC bias point at the input will be made independent of the gate-source voltage by adopting auto-zeroing.

3.2.2 I-V converter auto-zeroing

To solve the problem mentioned above, the I-V converter is auto-zeroed.

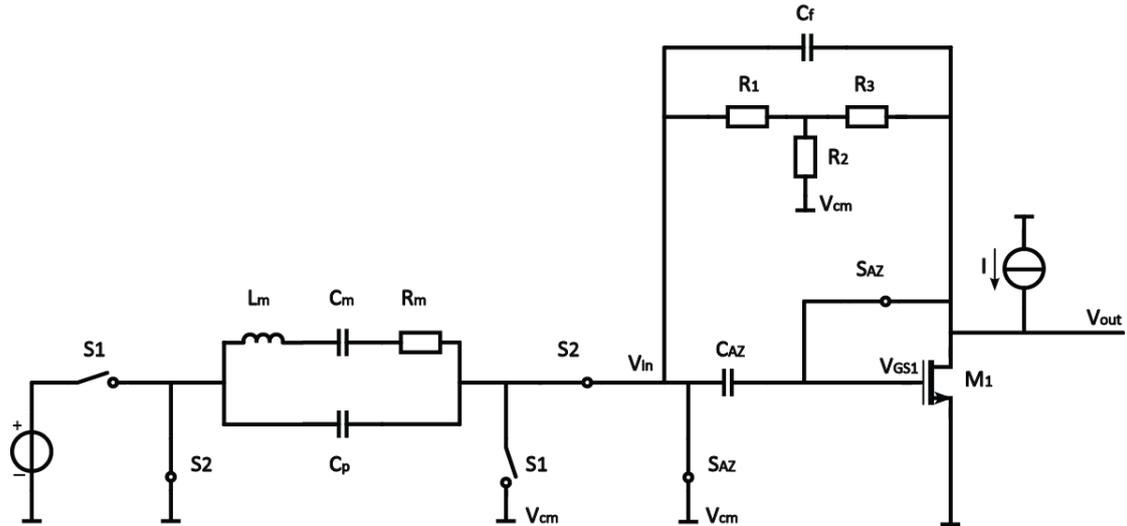


Figure 3-5: I-V converter during auto-zeroing phase

During the auto-zeroing phase, the switch S_{AZ} is closed as shown in Figure 3-5. The I-V converter works as a unity gain amplifier while the input of the I-V converter is connected to the common-mode voltage ($V_{in} = V_{cm}$). As a consequence, the difference between V_{cm} and V_{GS1} is stored on C_{AZ} .

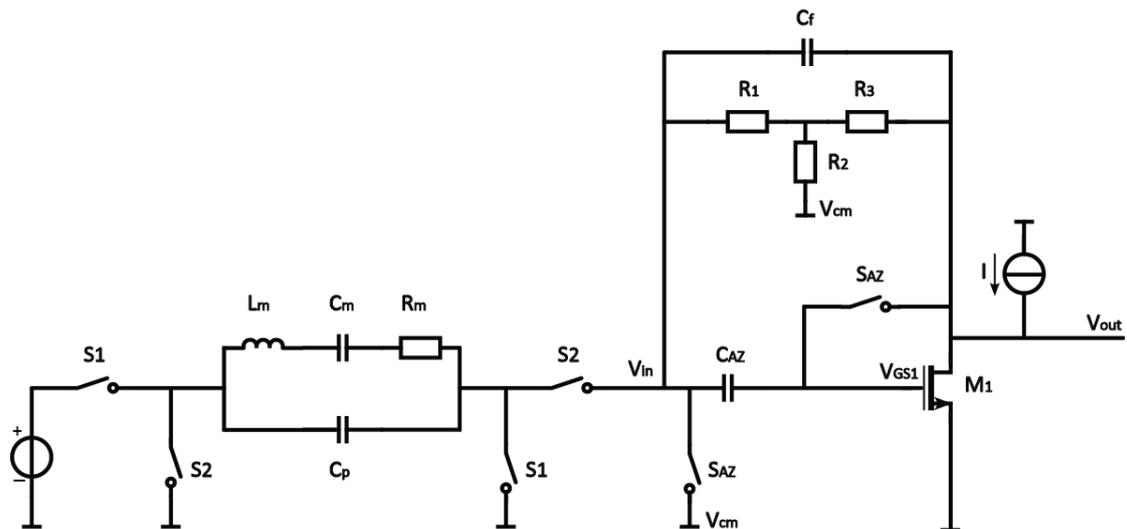


Figure 3-6: I-V converter during the other phases

During the other phases (Figure 3-6), S_{AZ} is open. The charge stored on C_{AZ} keeps the voltage at the input of the I-V converter equal to the common-mode voltage. Therefore, the second item in Equation (3-2) disappears, and then the DC biasing point at the output will be exactly equal to the common-mode voltage. At the same time, by tuning the level of the common-mode voltage, the output headroom of the amplifier can be maximized. For instance, the supply voltage of the circuit is 3.3V, if we have the common-mode voltage at 1.65V, the best output swing in both directions will be obtained.

As to the choice of C_{AZC} and C_{AZ} , the ring-down signal generated by the I-V converter is attenuated by the factor $C_{AZC} / (C_{AZC} + C_{in})$, where $C_{in} = C_{GS}$, is the input capacitance of the comparator. In order to reduce this signal attenuation and the charge-injection offset ($Q / (C_{AZC} + C_{in})$), C_{AZC} is chosen much bigger than C_{in} . Since the value of input capacitance is few tens of fF, the C_{AZC} is chosen to be 300fF. In the meantime, C_{AZ} is also chosen to 300fF, which is much bigger than C_{in} to store the big offset of the I-V converter.

With the addition of auto-zeroing, we have four different operating phases in one measurement period. To clarify, these four operating phases are demonstrated as follows:

- Phase 1: auto-zeroing the amplifier

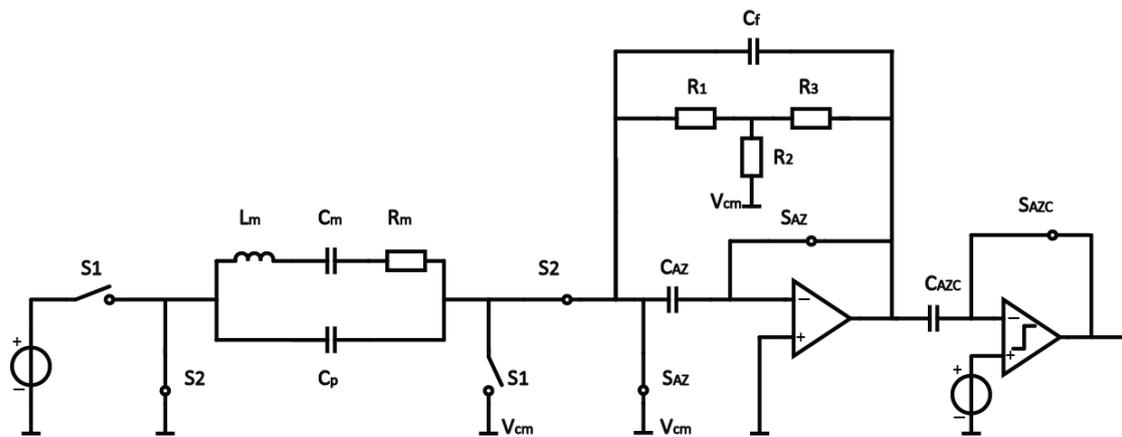


Figure 3-7: Phase1: auto-zeroing the amplifier

During the amplifier auto-zeroing phase, S_{AZ} , S_{AZC} and $S2$ are closed while $S1$ is open. The offset of the amplifier is stored on C_{AZ} as discussed in this subsection.

➤ Phase 2: auto-zeroing the comparator

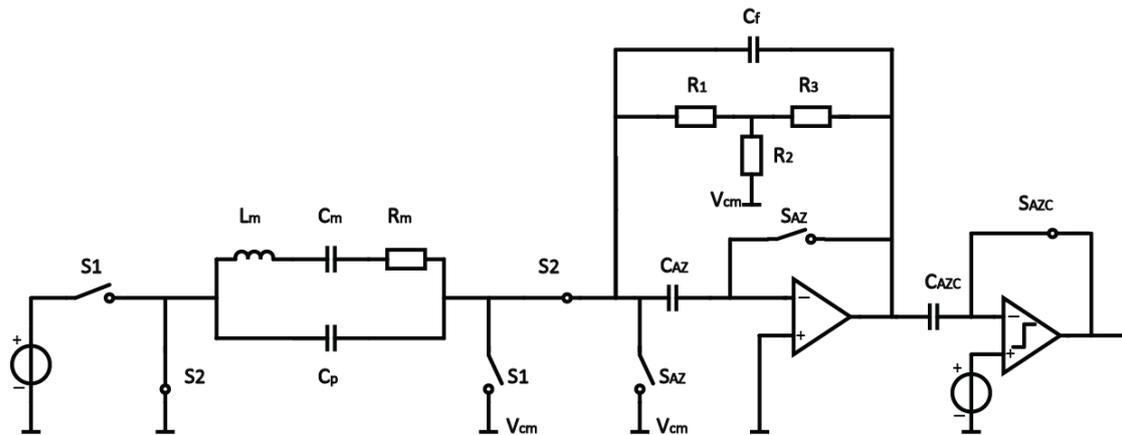


Figure 3-8: Phase2: auto-zeroing the comparator

During the comparator auto-zeroing phase, S_{AZC} and S_2 are closed while S_1 and S_{AZ} are open. The offset of the front-end circuit and the comparator is stored on C_{AZC} .

➤ Phase 3: excitation phase

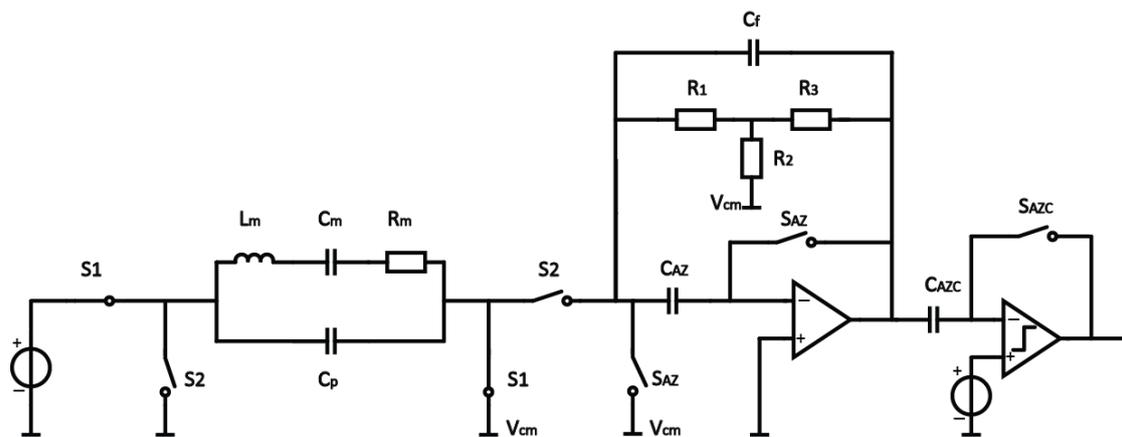


Figure 3-9: Phase3: excitation phase

During the excitation phase, S_1 is closed while S_{AZC} , S_{AZ} and S_2 are open. The circuit operates in the excitation phase introduced in section 2.2.1.

➤ Phase 4: ring-down phase

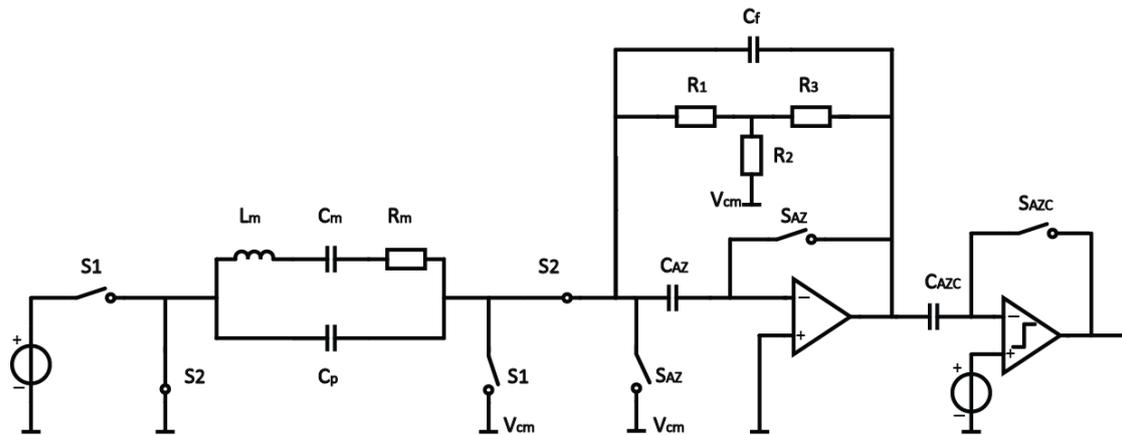


Figure 3-10: Phase4: ring-down phase

During the ring-down phase, S2 is closed while SAZC, SAZ and S1 are open. The circuit operates in the ring-down phase introduced in section 2.2.1.

3.2.3 Cascode stage and output stage

In this subsection, the circuit is improved by adding a cascode stage and an output stage. Until now, the amplifier is only implemented by a single transistor. However, this simple architecture results in some problems. Two main problems will be discussed in detail.

➤ Problem 1: residual offset caused by the finite DC gain

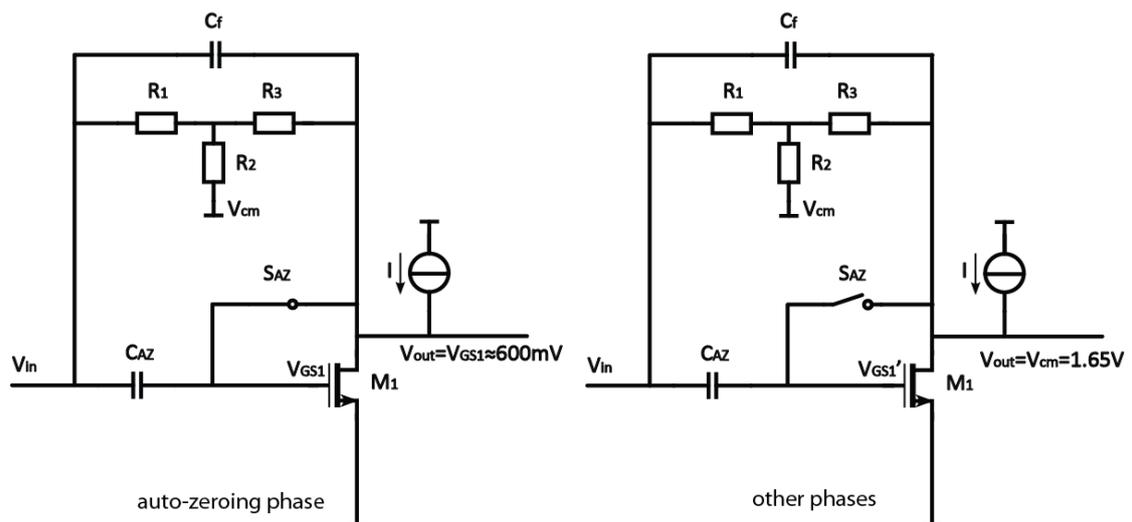


Figure 3-11: The variation of V_{GS1} caused by the variation of V_{DS} during different phases

During the amplifier auto-zeroing phase, the I-V converter operates in unity-gain. As a result, the voltage at the output of the amplifier (V_{out}) is equal to the gate-source voltage of the transistor

(V_{GS1}) of approximately 600mV. During the ring-down phase, the I-V converter is biased by the common-mode voltage. Consequently, the voltage at the output of the amplifier is approximately equal to the common-mode voltage, which is assumed to be 1.65V to get the biggest headroom.

Hence, the drain-source voltage (V_{DS}) of the transistor increases from 0.6V to 1.65V. Due to the finite DC gain of the transistor, this increase will lead to a reduction in the overdrive and hence in gate-source voltage. The charge sampled on the auto-zeroing capacitor is constant. Due to the reduction of V_{GS1} , the voltage at the input of the amplifier during the ring-down phase will be different from that during auto-zeroing phase (V_{cm}). As a consequence, the DC operating voltage at V_{out} will be shifted to an uncertain value unequal to V_{cm} , effectively introducing a residual offset at the output. To solve this problem, a cascode stage is used to increase the DC gain and thus reduce this offset as shown in Figure 3-12. The biasing circuit for the cascode stage will be introduced later in section 3.3.

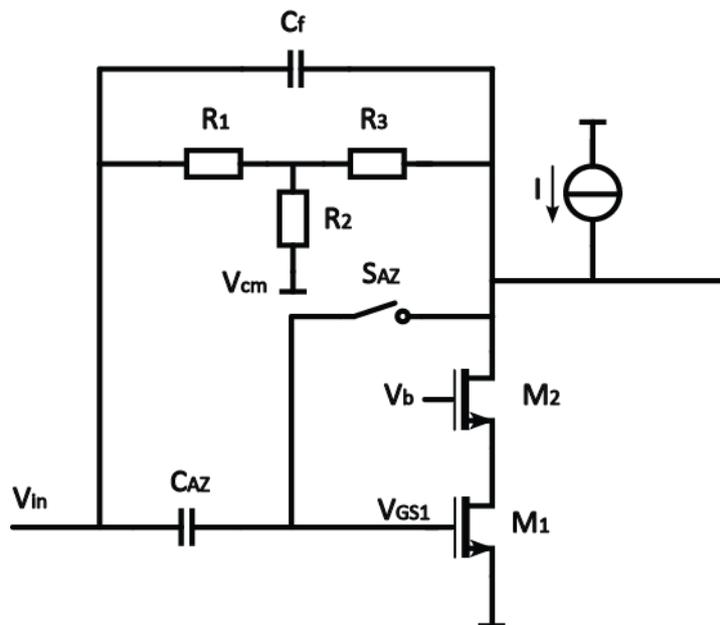


Figure 3-12: Front-end circuit with a cascode stage

- Problem 2: gain reduced by load of R_2 and R_3

Due to the special feedback resistor architecture, R_2 and R_3 act as a load of the amplifier. This load is in parallel with the output impedance of the amplifier, which leads to a reduction of the voltage gain of the amplifier. To solve this problem, a source follower has been added as an output stage to drive the load resistor R_2+R_3 (Figure 3-13).

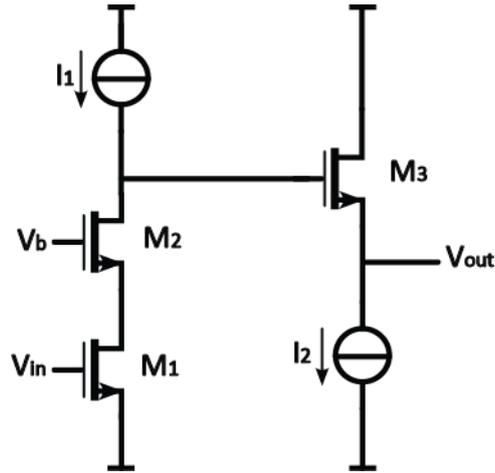


Figure 3-13: Front-end circuit with an output stage

The minimum bias current I_2 of this output stage is decided by the output swing (V_{p-p}) and the load resistance as expressed in Equation (3-3).

$$I_{\min} = \frac{V_{p-p}}{R_2 + R_3} \quad (3-3)$$

In our work, the V_{p-p} is about 1V and the load resistance is $1M\Omega$ (sum of the R_1 , R_2 and R_3 in section 3.1.2). Therefore, the minimum current for the second stage is $1\mu A$.

After adding the source follower, the value of the common-mode voltage should be adjusted to get the proper headroom in both directions. The upper limitation voltage at the output can be expressed by Equation (3-4) while the lower limitation is shown in Equation (3-5).

$$V_{\max} = V_{DD} - V_{DSSAT} - V_{GS} \approx 2V \quad (3-4)$$

$$V_{\min} = V_{DSSAT} \approx 0.5V \quad (3-5)$$

In order to get enough headroom in both directions, the common-mode voltage is designed to be 1.3V.

3.2.4 Stability

After the output stage is used in the front-end circuit, the front-end circuit becomes a two-stage amplifier. The internal point between two stages introduces an extra pole, which will have an impact on the stability of the amplifier. To make the circuit stable, enough phase margins in both the auto-zeroing phase and the ring-down phase are required. This requirement will make our design more complex. This problem is solved by only auto-zeroing the first stage during the auto-zeroing phase as shown in Figure 3-14.

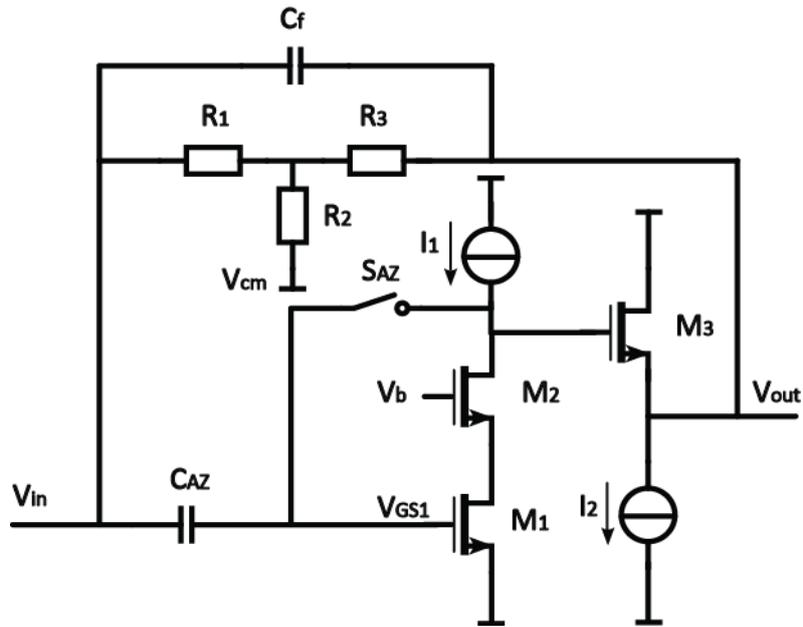


Figure 3-14: Auto-zeroing the first stage during auto-zeroing phase

Thus, only the stability during the ring-down phase needs to be considered. Based on the simulation, to keep the circuit stable the current for the second stage should be $3\mu\text{A}$.

3.3 Switches

So far, all switches have been assumed to be ideal with infinite off-resistance and zero on-resistance. However, this is not the truth in the real chip. In this subsection, the implementation of the switches is discussed. All switches have been implemented using NMOS transistors. Three problems caused by these switches and the corresponding solutions are presented: leakage current (off-resistance), finite on resistance and charge injection.

Leakage current (off-resistance)

There is always some leakage current flowing through the switches due to their finite off-resistance. In our circuit, the leakage current flowing through S_{AZ} and S_{AZC} will have an effect on the performance of the circuit, which is illustrated respectively in the following discussion.

- Design for the switch S_{AZ}

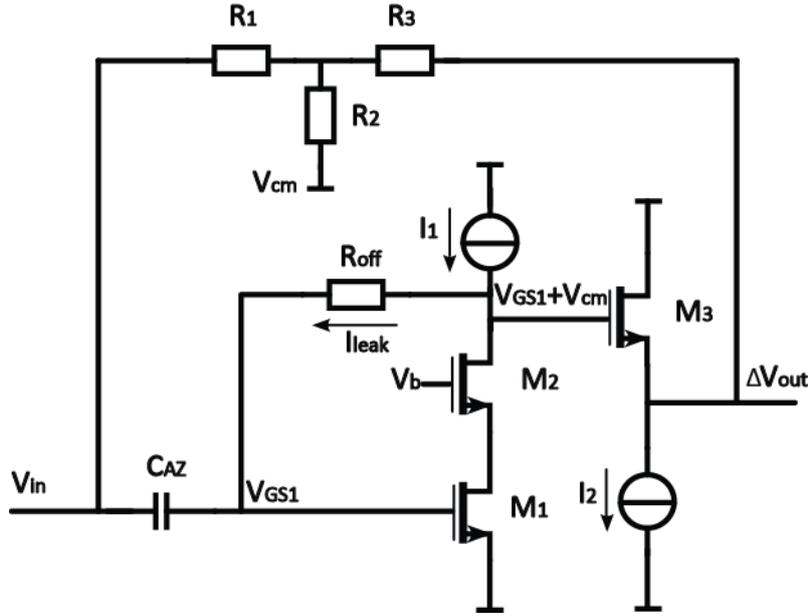


Figure 3-15: Influence of the leakage current caused by S_{AZ} during ring-down phase

As shown in Figure 3-15, S_{AZ} is switched off during the ring-down phase. Since there is a voltage V_{saz} across the switch, there is a leakage current I_{leak} flowing through S_{AZ} because of its finite off-resistance:

$$i_{leak} = \frac{V_{saz}}{R_{off}} \quad (3-6)$$

This current will be integrated by the auto-zeroing capacitor C_{AZ} , which leads to an offset ΔV at the input of the amplifier:

$$\Delta V = \frac{1}{C_{AZ}} \int_0^t i_{leak}(\tau) d\tau \quad (3-7)$$

This input offset is amplified by R_3 and R_2 into an output offset. For instance, the voltage across the switch is around 0.7V during the ring-down phase, and the off-resistance is typically a few $G\Omega$. Then a leakage of a few nA is achieved. Together with a measurement time of about 1ms, the offset is approximately a few volts. This large offset strongly decreases the number of zero-crossing cycles detected.

In order to solve this problem, according to the Equation (3-6) and (3-7), we have three options. The first choice is enlarging C_{AZ} to reduce the offset voltage integrated from the leakage current. The second and third methods are reducing the leakage current by increasing the R_{off} or decreasing the voltage across the switch. The third solution is chosen due to its simplicity. We reduce the voltage across the switch by applying the architecture shown in Figure 3-16.

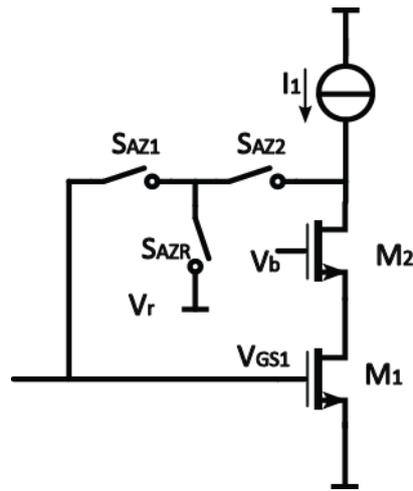


Figure 3-16: Low leakage implementation of the switch S_{AZ}

A voltage source (V_r) to replicate the gate-source voltage of the main NMOS is generated while an additional switch S_{AZR} is applied. S_{AZR} is operated complementary to S_{AZ} , and the switch S_{AZ} is split into two identical switches S_{AZ1} and S_{AZ2} . This implementation makes the voltage across the switch S_{AZ1} become zero; hence it significantly reduces the leakage current.

To generate this replica voltage (V_r), we apply a diode connected cascode transistors with a W/L proportional to the main cascode stage (10 times less). In the meantime, to obtain the same current density, the supply current (I_r) is also 10 times less, with a value of $1\mu A$. Moreover, the cascode transistor needs to be biased properly. To generate the biasing voltage V_b (see Figure 3-12), we use a transistor (M3) with a large L to leave more headroom for M6, and the supply current (I_b) is also 10 times less with a value of $1\mu A$. The circuit is shown in Figure 3-17.

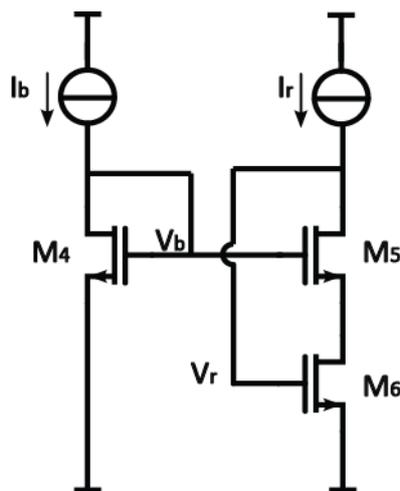


Figure 3-17: Generation of V_b and V_r

➤ Design for the switch S_{AZC}

Similarly, the finite off-resistance of the switch S_{AZC} also causes a droop at the input of the

comparator resulting in an impact on the number of ring-down cycles that can be detected. The difference is that the voltage at the input of the comparator is not identical during the excitation phase and the ring-down phase.

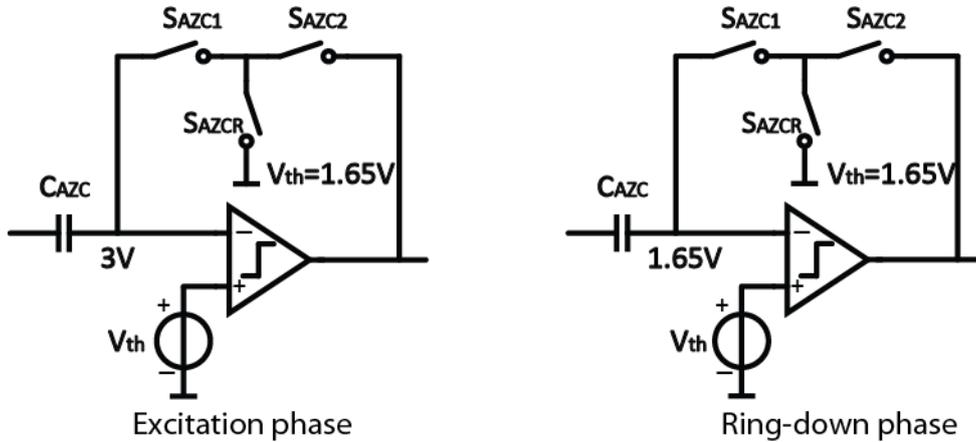


Figure 3-18: Difference between excitation phase and ring-down phase

As shown in Figure 3-18, in excitation phase, the voltage at the input of the comparator (V_{in_comp}) is about the sum of the offset sampled on the S_{AZC} and the open-loop operating voltage at the output of the I-V converter, which is about 3V. However, in the ring-down phase, the DC biasing voltage of V_{in_comp} is approximately equal to the threshold voltage ($V_{th}=1.65V$).

To address the impact of this difference on the leakage of the switches, the switches are implemented as displayed in Figure 3-19.

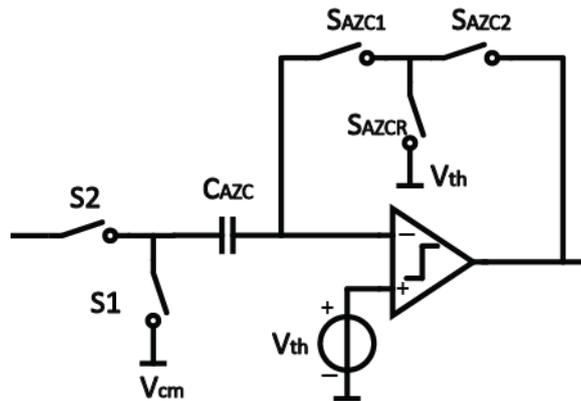


Figure 3-19: Low leakage implementation of the switch S_{AZC}

Two extra switches S1 and S2 are added to solve this problem. One side of S1 is connected to the common-mode voltage. The switch S_{AZC} is implemented the same as the switch S_{AZ} with a replica voltage of the threshold voltage. During excitation phase, S1 is closed while S2 is open. As a result, V_{in_comp} is about equal to the V_{th} , and then the voltage across the S_{AZC1} is zero. The leakage current is cancelled.

Finite on resistance

In addition to the finite off-resistance, the switches have a finite on-resistance [2]. We assume the transistor operating in non-saturation region ($V_{DS} < V_{GS} - V_{TH}$) when working as a closed switch. The current flowing through the switch is the drain current of the transistor (I_D). In the meantime, the voltage across the switch is the drain-source voltage of the transistor (V_{DS}). In non-saturation region, we have:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) - \frac{V_{DS}}{2} \right] \cdot V_{DS} \quad (3-8)$$

By calculating the derivative of Equation (3-8), the on-resistance can be found:

$$R_{on} = \frac{1}{\frac{\partial I_D}{\partial V_{DS}}} = \frac{1}{\frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH} - V_{DS})} \quad (3-9)$$

Hence, we reduce the on-resistance by increasing the size of the transistor. There are several switches of which the on-resistance needs to be considered. The first one is the switch located between the resonator and the amplifier. During the ring-down phase, the on-resistance will be in series with the resistance of the resonator, which effectively increases the value of R_m . To cancel the effect of R_{on} , we split the S2 into two switches as shown in Figure 3-20, so that the finite on-resistances of these switches are within the feedback loop and no longer add to R_m .

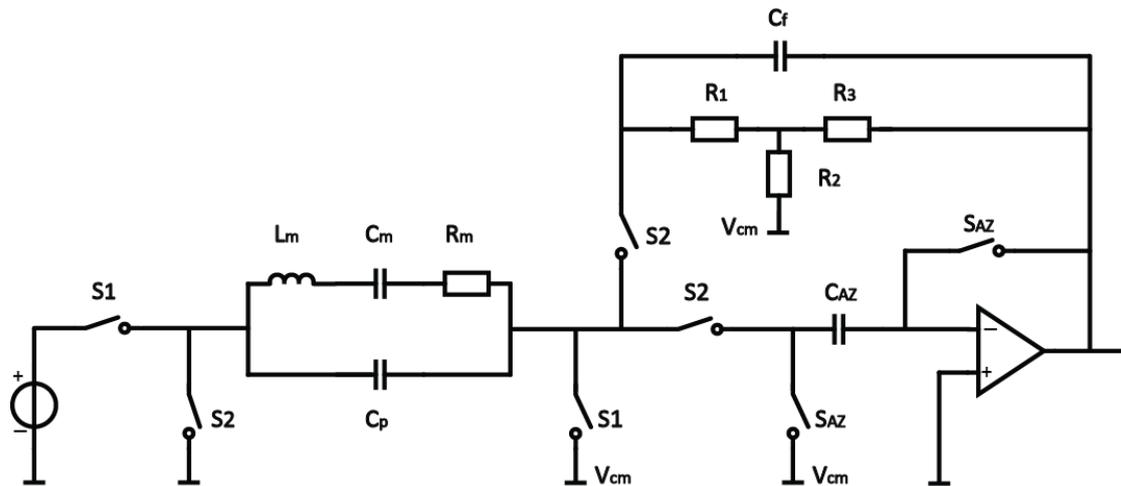


Figure 3-20: Implementation of S2 to cancel the effect of R_{on}

The second one is the switch S1 located at the right side of the resonator. During the excitation phase, the on-resistance is in series with the resistance of the resonator. R_{on} and the resonator act as a voltage divider. With a big R_{on} , the voltage across the resonator will be reduced. As a result, the ring-down current decreases. To make R_{on} lower, we enlarge the size of the transistor instead of utilizing minimize size.

The last ones are the switches in parallel with the feedback resistor $R_{11} \sim R_{13}$. These feedback resistors are hundreds of kilohms. To reduce the influence of R_{on} , we adjust the size of transistors to make their R_{on} smaller than one percentage of the feedback resistances.

Charge injection

The charge injection caused by the MOSFET switches has an influence on the charge sampled on the auto-zeroing capacitors C_{AZ} and C_{AZC} . For instance, as to C_{AZ} , when S_{AZ1} and S_{AZ2} are on, due to small V_{DS} there is small charge in the channel. When S_{AZ1} and S_{AZ2} switch off (Figure 3-21), this charge is distributed on both sides through the source and drain i.e. towards the C_{AZ} at the left side and to the C_{AZC} at the right side. We assume the charge is equally distributed on both sides of the switch. The charge towards C_{AZ} will increase the charge stored on C_{AZ} , which changes the offset voltage sampled and leads to an error. However, the charge injection of S_{AZ} (S_{AZ1} and S_{AZ2}) can be cancelled by the following comparator auto-zeroing phase. The charge injection of S_{AZC} (S_{AZC1} and S_{AZC2}) should be minimized to reduce the error on the charge stored on C_{AZC} . This is done by using a minimum size transistor for this switch.

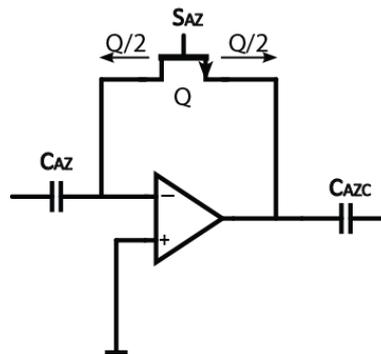


Figure 3-21: Charge injection caused by S_{AZ} (S_{AZ1} and S_{AZ2})

For clarity, after the design of the switches, the new architecture is presented in Figure 3-22.

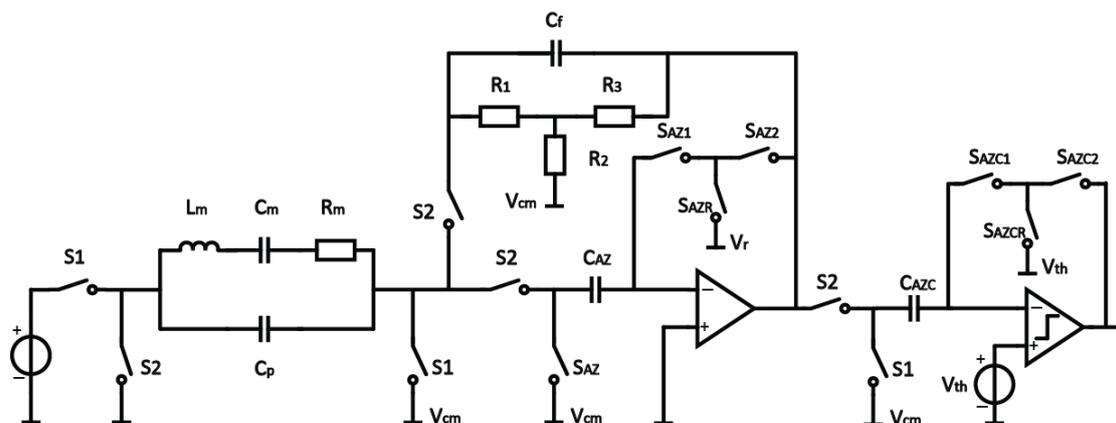


Figure 3-22: The architecture in the readout chip

All the bias-currents (I_r and I_b in Figure 3-17, I_1 and I_2 in Figure 3-13) for the I-V converter are generated from on-chip current mirrors while the current sources are provided off-chip on the PCB board. I_1 , I_r and I_b are generated from current mirrors from the same current source ($10\mu\text{A}$, $I_{\text{ref_1st}}$, see Appendix III, Figure III-5) while I_2 is generated by a current mirror from another current source ($10\mu\text{A}$, $I_{\text{ref_2nd}}$, see Appendix III, Figure III-5).

3.4 Comparator design

As described in Chapter 2 (section 2.5), the main design requirement of the comparator is the delay time. The propagation delay of the last ring-down cycle should be smaller than 37.5ns (for a minimum overdrive). For simplicity, we use the comparator designed by prior art directly as shown in Figure 3-23 [3] [4], which achieves a delay of less than 15ns. The current consumption of the comparator is $36\mu\text{A}$. The same as the I-V converter, the bias-currents for the comparator are all generated from on-chip current mirrors by an off-chip current source with a value of $1\mu\text{A}$ ($I_{\text{ref_comp}}$, see Appendix III, Figure III-5).

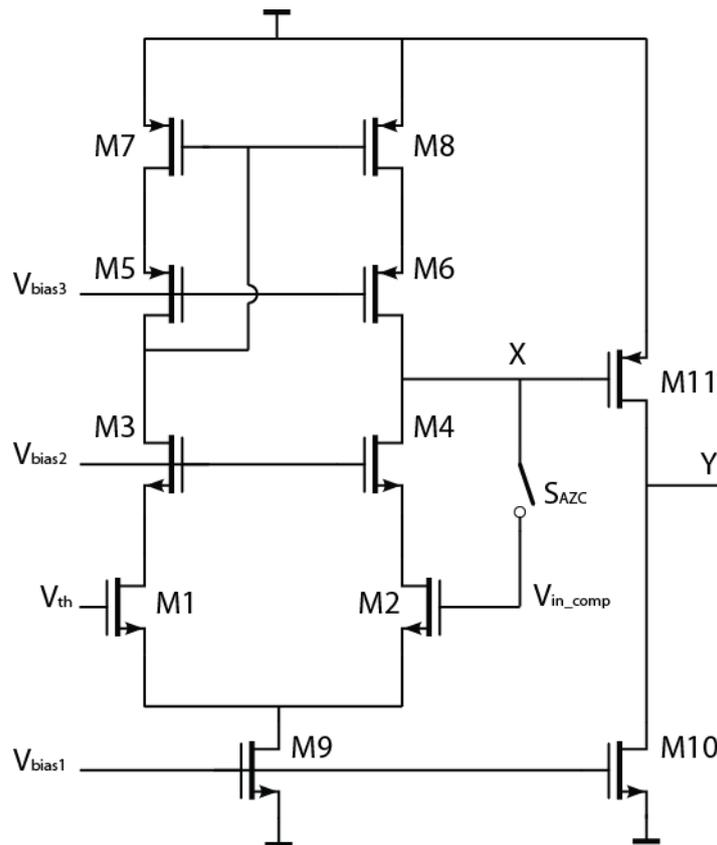


Figure 3-23: Two-stage auto-zeroed comparator circuit

3.5 Design for testability

Several circuits have been included in the prototype design to make the chip sufficiently tunable and observable during the measurement. These will be discussed in this subsection.

Shift register

The nine signals are needed to control the feedback network to implement the configurability, which increases the number of I/O pins needed. To solve this problem, a serial-in, parallel-out shift-register with output registers (Figure 3-24(a)) is used for the start-up configuration of the prototype chip. This is an I/O-efficient approach which needs only three extra digital I/O pins: a serial input (feedback_control), a clock (control_clk) and a configuration enable trigger (feedback_en). The length of the shift-register equals to that of the configuration command word, which is nine here.

Figure 3-24 (b) shows the operation timing diagram of the proposed circuit. Before the core circuits are started up, a 9-bit configuration command word, which is generated by data acquisition board (DAQ), is serially written into the shift-register in pace with the external clock control_clk, which is also generated by DAQ. Upon completion, the contents of the shift-register are transferred to the separated registers on the rising edge of feedback_en. The outputs of these registers (CMD1n) are then available for the configuration of the feedback network.

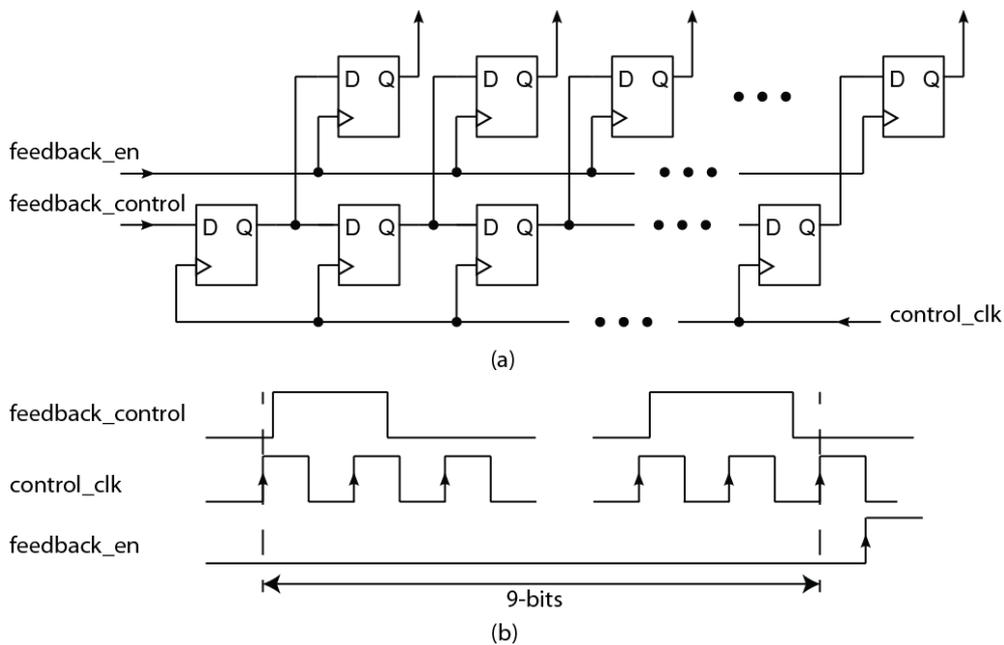


Figure 3-24: (a) Schematic of the shift-register (b) the operation timing diagram

Source follower

To be able to observe the voltage waveform at the output of the I-V converter without disturbing the normal circuit operation, an on-chip analog output buffer is utilized. As illustrated in Figure

3-25, such an analog out put buffer is a PMOS source-follower (M_{SF}), which is driven by a constant current source (I_{SF}) off-chip on the PCB test board.

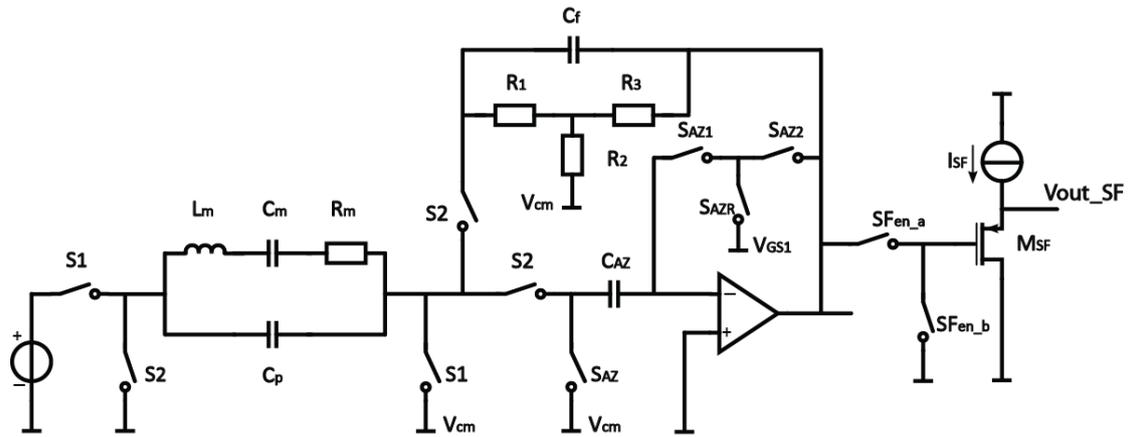


Figure 3-25: The implementation of the source follower

The source of M_{SF} is directly connected to a test I/O pad without any electrostatic discharge (ESD) protective devices. Therefore, the voltage waveform on the gate of M_{SF} can be reproduced with a level-shift equal to V_{GS} at the test I/O pad. Moreover, to make our circuit flexible, we apply two complementary switches to select this buffer stage.

3.6 Counting circuitry design

To extract the resonance frequency and quality factor from the output signal of the readout chip, an off-chip counting circuitry has been implemented on a FPGA. The block diagram of the counting circuitry (including control signals) is shown in Figure 3-26.

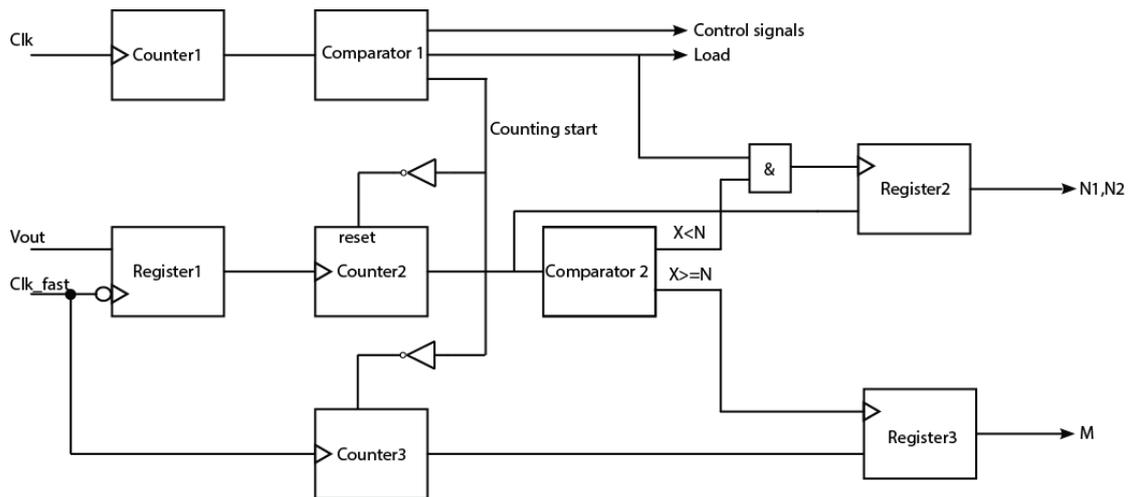


Figure 3-26: Block diagram of the counting circuitry

‘Clk’ is an internal clock generated by the FPGA development board with a frequency of 10MHz,

which is counted by 'Counter1'. 'Clk' is applied to generate the control signals. 'Clk_fast' is the reference clock used for counting process. 'Vout' is the output square-wave from the chip used for counting. 'Counter2' counts the output square wave while 'Counter3' counts the reference clock. Both counters are reset by signal 'counting start', which is active in the ring-down phase. When the result obtained by 'Counter2' is more than N cycles, the final output is the cycles of reference clock M. When the result obtained by 'Counter2' is less than N cycles and the load signal is high, the final output is the counted cycles of 'Vout' (N1, N2 used in Equation (2-8), Chapter 2, and section 2.2.2). The verilog code for counting circuitry can be found in Appendix II.

3.7 Simulation results

In this subsection, some simulation results are given to prove the circuit working correctly. Firstly, the parameters of sensors simulated are presented as well as the simulation test bench. Secondly, the simulation results, consisting of ring-down amplitude, noise and stability, are given. Finally, the energy consumption is calculated based on the simulation results.

3.7.1 Simulated sensors and simulation test bench

To simulate the circuit-level design, we use the parameters for the resonator the same as that used in architecture-level design. In addition to this resonator, to prove the programmability, all the resonators have been simulated. For simplicity, we demonstrate one of them as an example.

The parameters for the resonator are:

SH0_AF71314:

- $R_m = 390.9\text{k}\Omega$, $L_m = 51.07\text{H}$, $C_m = 1731\text{aF}$, $C_p = 4.199\text{pF}$
- $f_{\text{res}} = 535.2\text{kHz}$, $Q = 439.3$

S71_B770910:

- $R_m = 309.3\text{k}\Omega$, $L_m = 40.52\text{H}$, $C_m = 4389\text{aF}$, $C_p = 3.256\text{pF}$
- $f_{\text{res}} = 377.4\text{kHz}$, $Q = 310.6$

And the parameters for the feedback network are:

SH0_AF71314:

- $C_f = C_1 + C_2 = 75\text{fF}$
- $R_1 = R_{13} = 400\text{k}\Omega$, $R_2 = 100\text{k}\Omega$, $R_3 = 900\text{k}\Omega$

S71_B770910

- $C_f = C_2 + C_3 = 150\text{fF}$
- $R_1 = R_{11} + R_{12} = 300\text{k}\Omega$, $R_2 = 100\text{k}\Omega$, $R_3 = 900\text{k}\Omega$

We apply a sine-wave with amplitude of 100mV, and a frequency equal to the resonance frequency as the excitation source. We set the common-mode voltage level (V_{cm}) at 1.3V, and the threshold-level (V_{thld}) is 1.65V to detect the resonance frequency. In addition to the control signals shown in Chapter 2, section 2.7, three extra signals are added to bias the circuit and cancel the leakage current. Figure 3-27 plots all the control signals, with a total measurement time of 2ms.

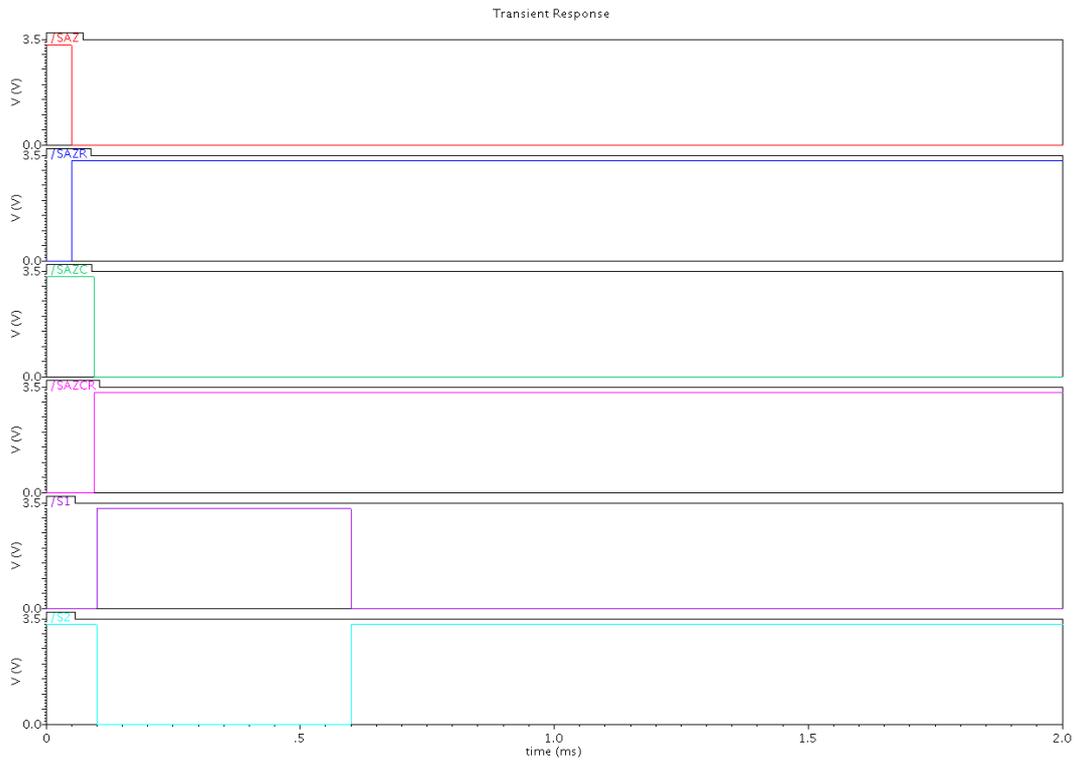


Figure 3-27: Timing of control signals

3.7.2 Simulation results

Firstly, simulation results for the resonator SH0_AF71314 are shown in Figure 3-28: the switched excitation signal with an amplitude of 100mV and a frequency of 535.2kHz (Fig. 3-28 top), the ring-down signal at the output of the integrator and the ring-down signal at the input of the comparator (Fig. 3-28 middle), and the comparator output signal for frequency counting (Fig. 3-28 bottom). In the meantime, the simulation results for the resonator S71_B770910 are also demonstrated in Figure 3-29 in the same way.

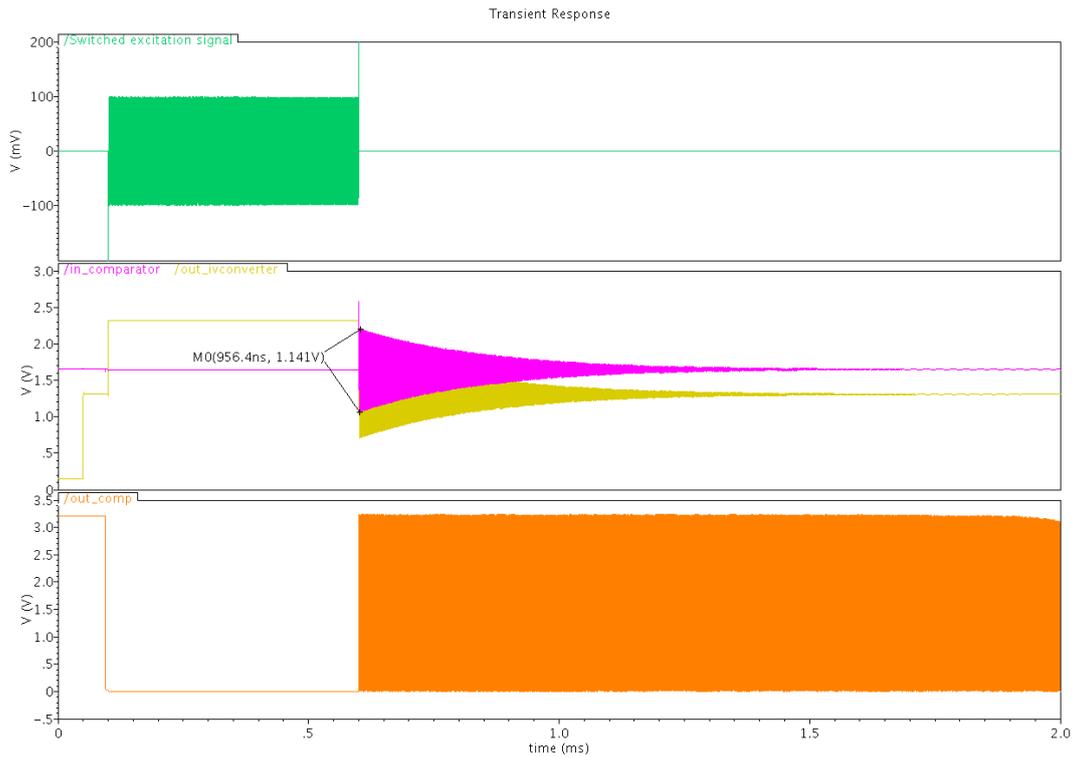


Figure 3-28: Simulation results of SH0_AF71314

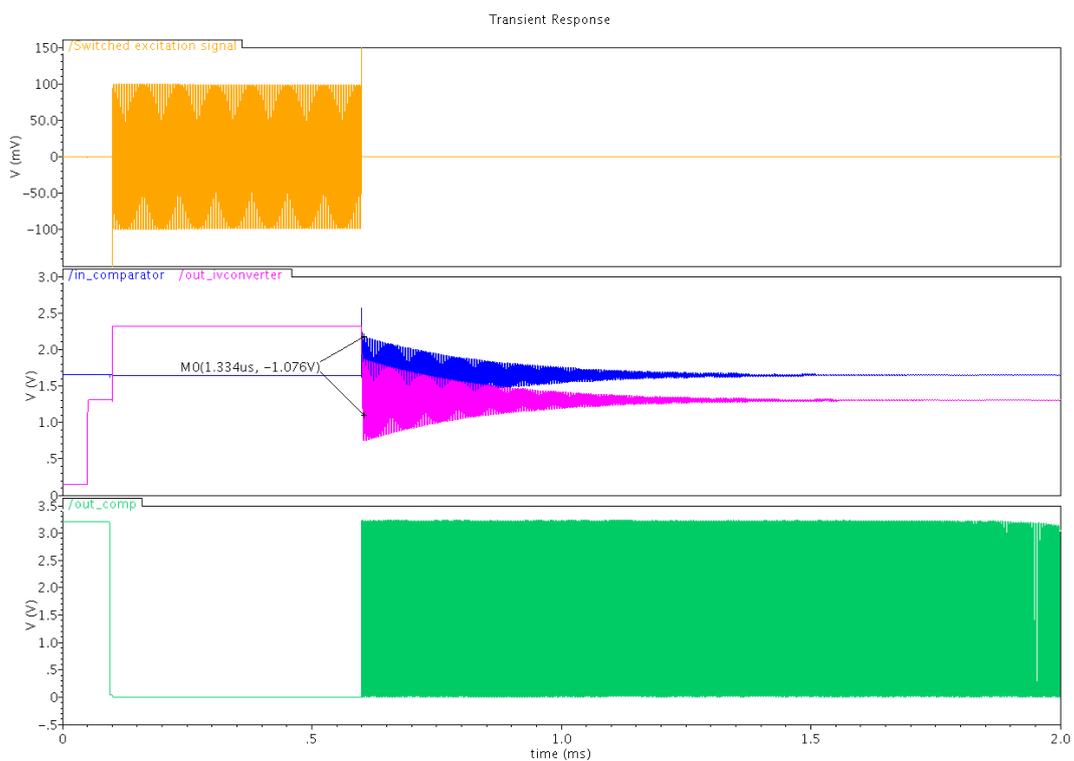


Figure 3-29: Simulation results of S71_B770910

In the following description, the simulation results of the resonator SH0_AF71314 are analyzed in comparison with S71_B770910 in three aspects: initial ring-down amplitude, noise and stability.

Initial ring-down amplitude

The peak-to-peak amplitude of the first ring-down cycle in both Figures 3-28 and 3-29 is bigger than 1V. This has been achieved by selecting a larger feedback resistance for SH0_AF71314 than for S71_B770910, to compensate for the larger resistance R_m of resonator SH0_AF71314.

We will now compare the simulated initial amplitude of resonator SH0_AF71314 with the value predicted by Equation (2-26) (Chapter 2, section 2.4.4). For the feedback resistors, we assume it is equal to the effective value as shown in Equation (3-1).

$$R_f = 400k + 900k + \frac{400k \cdot 900k}{100k} = 4.9M\Omega$$

And with other parameters shown below:

- $R_m = 390.9k\Omega$
- $f_{res} = 535.2kHz$
- $V_{dr} = 0.1V$
- $g_m = 200\mu S$

We obtain the peak-to-peak ring-down amplitude:

$$A_{0(p-p)} = 1.47V$$

This value is much bigger than the simulation result (1.14V). One obvious reason is that Equation (2-26) has been obtained by assuming only one feedback resistor instead of the T-type network. After using the T-type architecture, the input impedance is reduced by a factor of $R_1 / (R_1 + R_2)$ (Figure 3-1). As a result, less current will flow into the I-V converter. The other reason is our actual amplifier has a finite DC gain, but we assume the amplifier has an infinite DC gain in Equation (2-26). Hence, the DC gain of the I-V converter is:

$$G_0 = \frac{1}{\beta + 1/A} = \frac{1}{\beta}$$

where β is the feedback factor, and A is the DC gain of the amplifier.

While in reality, after adding a feedback capacitor, the bandwidth of the I-V converter is reduced. The gain at the resonance frequency is also reduced. As a consequence, the finite DC gain (A) of the amplifier causes $G_0 \ll 1/\beta$ reducing the output amplitude.

Noise and stability

In this section, we check the thermal noise and stability for both resonators. The small-signal noise during the ring-down phase has been simulated. While this simulation does not include noise sampling, this simplification is justified, since the kT/C noise sampled on C_{AZ} is not

significant in our circuit. The simulation results are shown in Figure 3-30 (SH0_AF71314) and Figure 3-31 (S71_B770910), respectively.

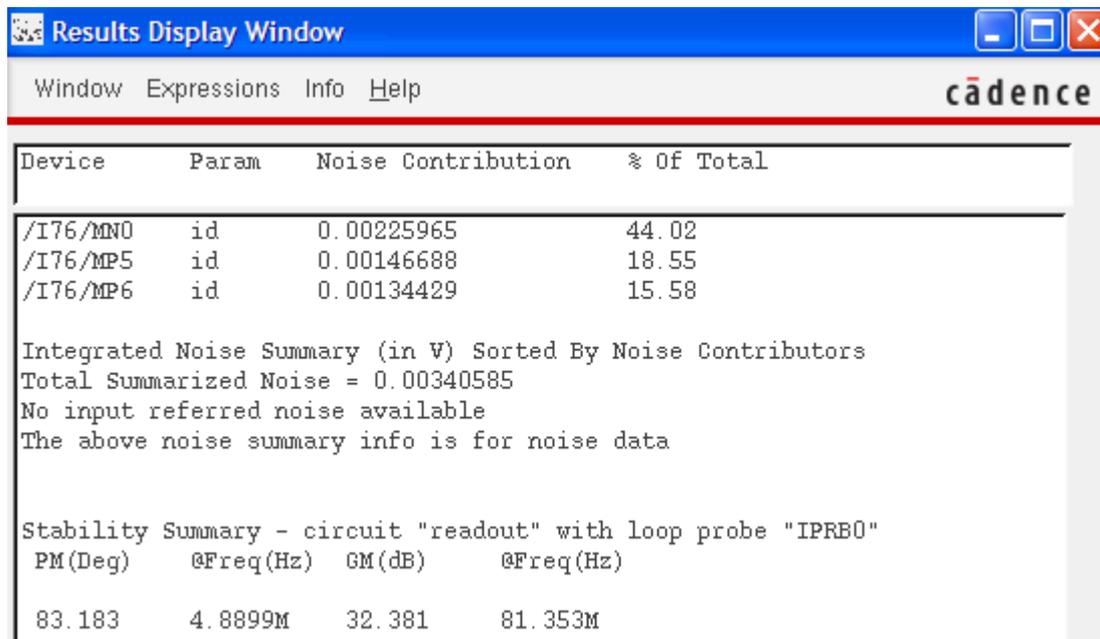


Figure 3-30: RMS noise summary and stability summary of the resonator SH0_AF71314

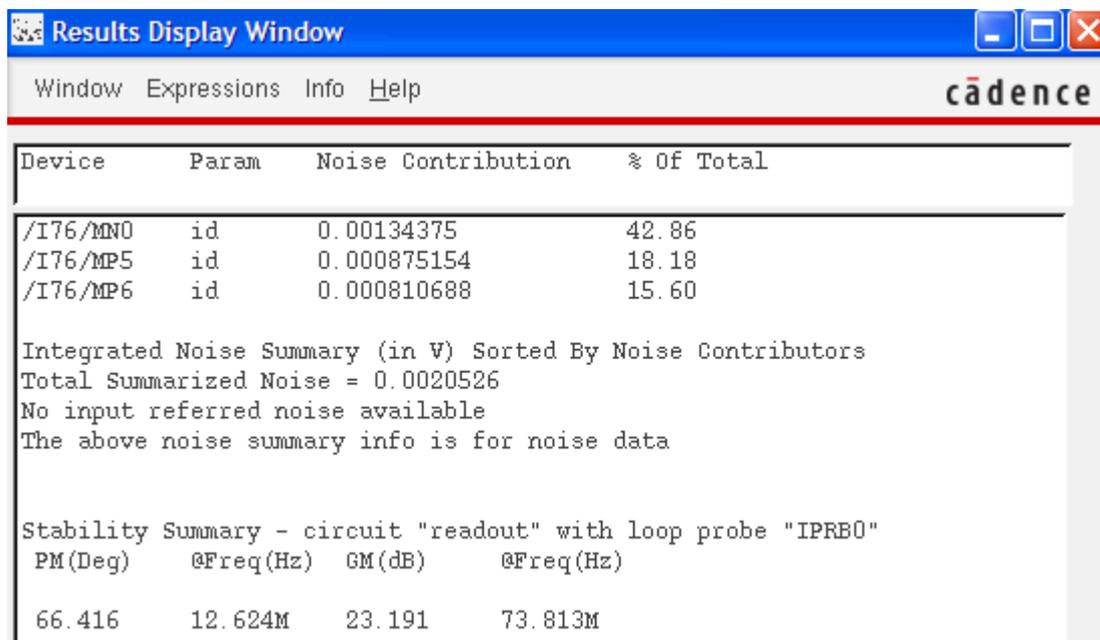


Figure 3-31: RMS noise summary and stability summary of the resonator S71_B770910

Since the resonance frequency of the S71_B770910 is smaller than that of the SH0_AF71314, the feedback capacitance chosen for S71_B770910 can be bigger, which helps to reduce the noise. As a result, the RMS noise for S71_B770910 is about 2mV while the RMS noise for SH0_AF71314 is around 3.4mV. According to these results, the SNR for both of them meets the requirement. In the meanwhile, the stability for both of resonators can fulfill the requirements:

- Phase margin > 60 degrees
- Gain margin > 14dB

3.7.3 Energy consumption

We summarize the energy consumption in Table 3-1:

| Components | Supply voltage | Supply current | Time | Energy consumption |
|---------------|----------------|----------------|-------|--------------------|
| I-V converter | 3.3V | 15uA | 1.5ms | 74.25nJ |
| Comparator | 3.3V | 36μA | 1.5ms | 178.2nJ |

Table 3-1: Summary of the energy consumption in simulation

During the excitation phase, the I-V converter and comparator are not connected with the resonator. They consume no energy. Hence, we have a total energy consumption of 252.45nJ per measurement. If we check the ring-down signals (Figure 3-28 and 3-29), the signal rings down approaching its steady state at about 1.5ms. Thus, we can make the measurement time shorter to save energy. If we apply a measurement time of 1.5ms, we have the total energy consumption reduced to 168.3nJ per measurement).

3.8 Conclusions

In this chapter, the circuit-level analysis and design of the interface circuit have been introduced. In the front-end circuit design, we have mainly discussed the programmable feedback network with feedback resistors using a T-type architecture, the core amplifier implementation using an auto-zeroed two-stage amplifier with a cascode stage and an output stage, the implementation of the switches and the design for testability using shift register and source follower. For the auto-zeroed comparator, we use a simple two-stage configuration as the same as the prior work. Also, the counting circuitry design has been briefly discussed. Furthermore, we have analyzed the simulation results in several aspects: ring-down amplitude, thermal noise. Finally, we have calculated the total energy consumption of 363nJ (which can be further reduced to 244nJ by applying a shorter measurement time).

Reference

- [1] R. Wu, F. J. Lidgey, K. Hayatleh, "Using the 'T' feedback network with the current feedback operational amplifier" International Journal of Electronics, vol.91, Issue 11, 2004
- [3] P. E. Allen, D. R. Holdberg, CMOS Analog Circuit Design. Oxford University Press, 2002
- [4] P. E. Allen, "Open-loop comparators", lecture note, lecture 310.
http://www.aicdesign.org/SCNOTES/2010notes/Lect2UP310_%28100328%29.pdf
- [5] Z. Zeng, M. A. P. Pertijs and D. M. Karabacak, "An Energy-Efficient Readout Circuit for Resonant Sensors Based on Ring-Down Measurement," Review of Scientific Instruments, 84, 025005, Jan. 2013.

Chapter 4

Measurement Results

In this chapter, measurement results of our resonant sensor interface are presented. We start with a brief introduction to the fabricated chip. After that, the measurement setup including the PCB test board design and the equipment setup are presented. Finally, measurement results obtained by using both a conventional impedance analyzer and the ring-down technique are given.

4.1 Fabricated chip

At the beginning of this section, the layout of the prototype chip is introduced. Then, a micrograph of the fabricated chip is presented.

4.1.1 Layout

To enable fabrication of a prototype chip in a standard 0.35- μm CMOS technology, a physical layout of the design presented in the previous chapter has been drawn. Figure 4-1 displays the complete chip layout, including pad ring. The active area occupies 0.0625mm² (0.25mm \times 0.25mm). 22 I/O pins are used, of which 8 are digital, 12 are analog and 2 are metal pads without ESD protections for the analog output buffers 'Vout_SF' (pin3 in Figure 4-1) and 'V_sensor_right' node of the resonator (pin8 in Figure 4-1). As shown in Figure 4-1, I/O pins are also labeled with different numbers. The names of the I/O are listed in the Table III-1, Appendix III.

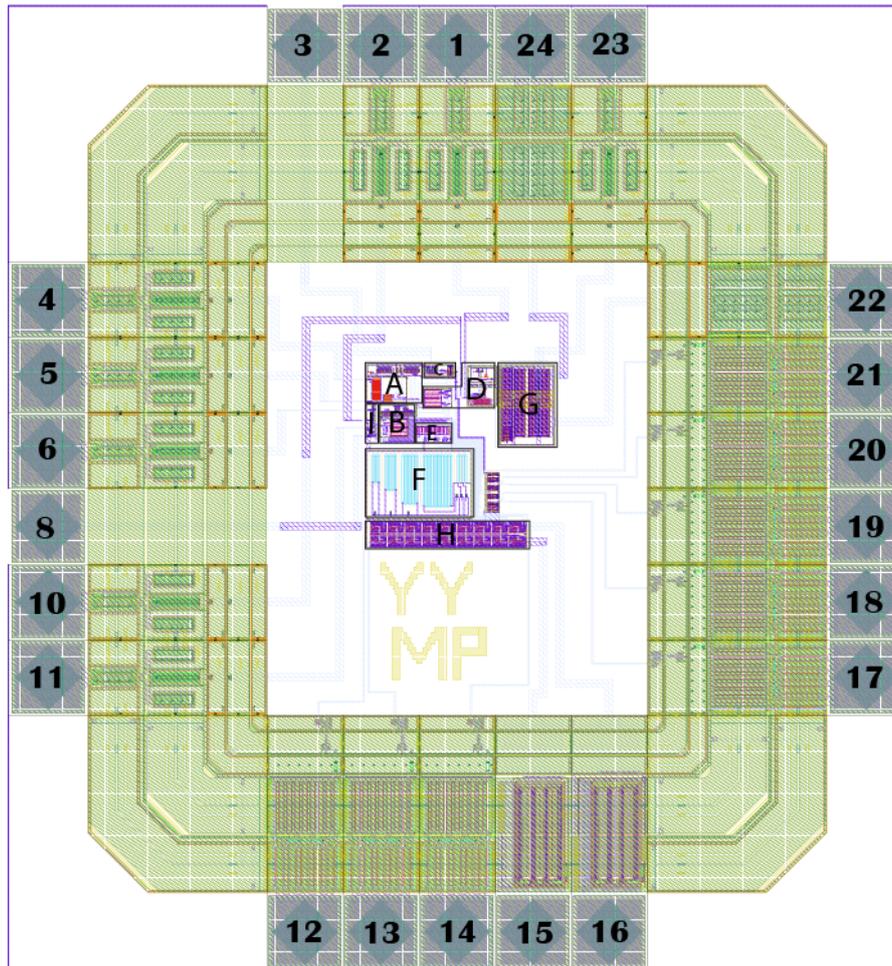


Figure 4-1: Layout with pad ring

As shown in Figure 4-1, critical sub-blocks are labeled. Functionality of each block is listed below:

- A. Biasing circuit
- B. Auto-zeroed I-V converter
- C. Source follower
- D. Auto-zeroed comparator
- E. Switchable feedback capacitors
- F. Switchable feedback resistors
- G. Inverter-bank circuit
- H. Shift register
- I. Analog switches

4.1.2 Chip micrograph

The design is implemented in a 0.35- μm CMOS process, and the chip micrograph is shown in Figure 4-2. The chip area is 1.2mm \times 1.3mm.

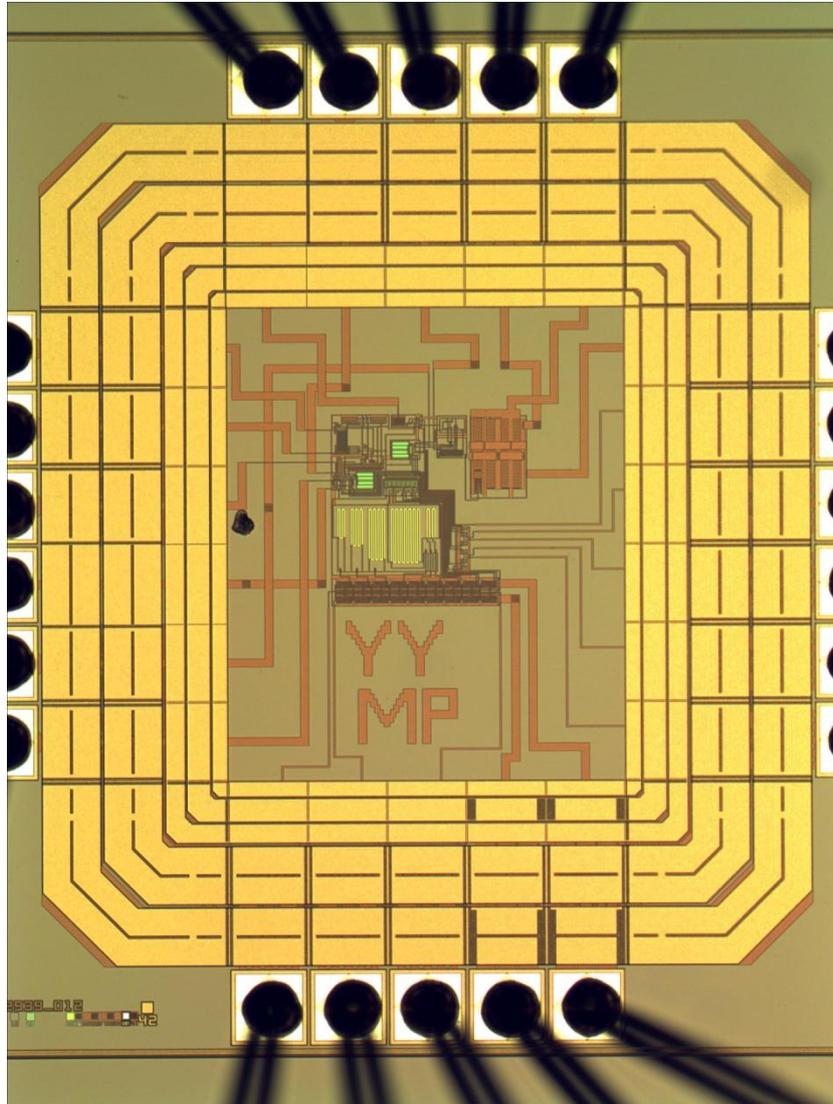


Figure 4-2: Chip micrograph

4.2 Measurement setup

To test our chip, we have built a measurement setup. The main part of this setup is a printed circuit board (PCB), which has been designed and fabricated as a test board for the measurement. Firstly, we give an introduction to the equipment for the measurement setup. After that, the design of the PCB board is described.

4.2.1 Equipment

An overview of the equipment setup is depicted in Figure 4-3.

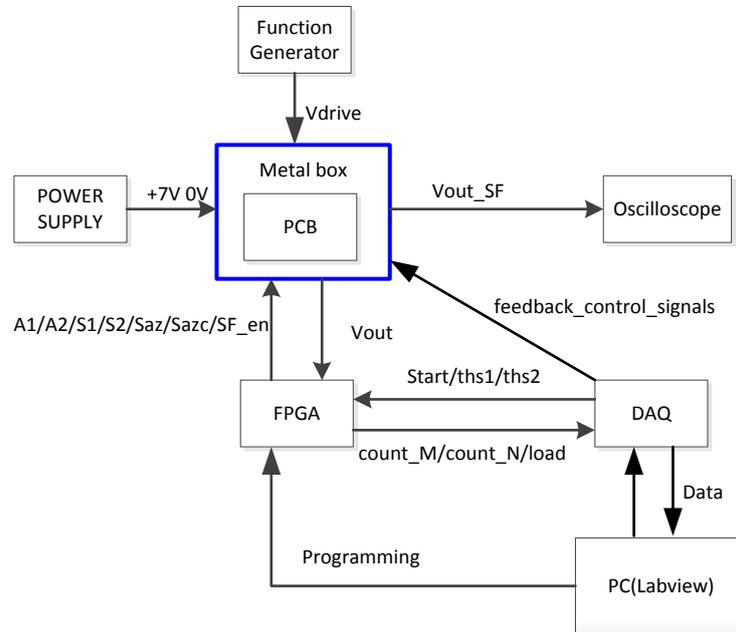


Figure 4-3: Overview of the measurement equipment setup

In the measurement, several equipments have been used (Figure 4-3):

1. Power supply

It provides positive supply (+7V) and ground (gnd) for the test board (Figure 4-6).

2. Function generator

It provides an external excitation signal (a 200mVp-p sine-wave with a frequency close to f_{res}) for the test board (Chapter 2, section 2.3). In order to minimize cross-talk from the output of the function generator to the readout circuit, we operate it in burst-mode, in which it only generates an excitation signal during the excitation phase, as shown in Figure 4-4.

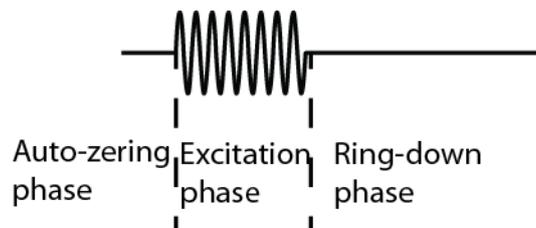


Figure 4-4: Excitation signal generated by function generator

3. Oscilloscope

The oscilloscope displays the level-shifted ring-down signal (read-out using the source follower) and the output signal of the comparator.

4. Metal box

The metal box is used for shielding of the test board during measurement.

5. FPGA development board

The FPGA development board provides the control signals ($S1$, $S2$, S_{AZ} , S_{AZC} , SF_en , A_1 and A_2 in Figure 4-3) and performs the frequency counting (Chapter 3, section 3.6). The verilog code is shown in Appendix III. $S1$, $S2$, S_{AZ} and S_{AZC} are the control signals for the switches in the ring-down chip. SF_en is the control signal for selecting the source follower. A_1 and A_2 are the control signals for selecting the multiplexer.

6. Data acquisition board (DAQ)

DAQ provides the control signals ($Start$, $ths1$ and $ths2$ in Figure 4-3) to the FPGA development board, generates the control signals for the feedback network to the test board and reads-out the results from the FPGA board ($count_M$, $count_N$ and $load$ in Figure 4-3) and transfers them to the PC. 'Start' is the control signal generated by DAQ given to FPGA to reset the measurement. 'ths1' and 'ths2' are the signals used to control the selection of threshold voltages.

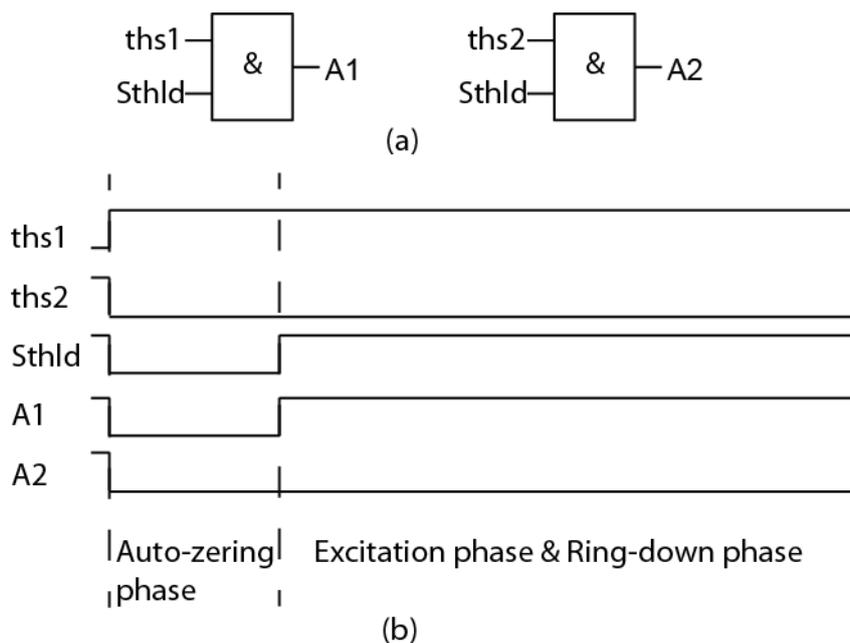


Figure 4-5: Timing diagram for the control signals of the multiplexer

Since the threshold voltage during auto-zeroing phase should always be equal to 1.65V, 'ths1' and 'ths2' are gated by FPGA, as shown in Figure 4-5(a), to ensure that a threshold voltage of 1.65V is selected during the auto-zeroing phase. During the ring-down phase, the selection signals provided by the DAQ are passed to the multiplexer as shown in Figure 4-5(b). 'A1' and 'A2' are the final signal applied to the multiplexer to select the threshold voltage.

7. Computer

The PC controls the data acquisition board and processes the measurement results and provides final f_{res} and Q values.

4.2.2 Test PCB

The PCB design is described in detail in Appendix III. An overview of the test board is displayed in Figure 4-6.

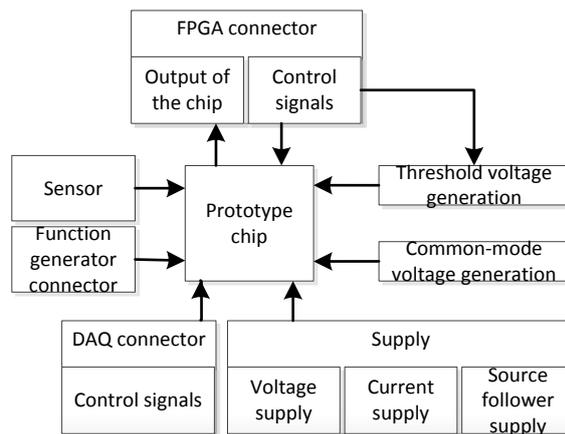


Figure 4-6: Block diagram of the PCB board

The functionality of each part is introduced as follows:

1. FPGA development board connector

An FPGA (mention type) is used to generate the clock signals for the chip (such as S1 and S2) and to implement the counting process. We use an FPGA development board which is connected to the PCB via a flat cable.

2. Function generator connector

The excitation signal is generated by a function generator. Hence, a connector is used for connecting the function generator with the PCB board.

3. DAQ connector

A National Instruments Data Acquisition (DAQ) Board is used to generate the control signals for the programmable feedback network. In addition, the signal for controlling the multiplexer (ths1, ths2 in Figure 4-3) is also generated by DAQ. The use of the DAQ allows these control signals to be easily changed without reprogramming the FPGA.

4. Threshold-level (V_{thld}) generation

At least two threshold-levels are needed for the quality factor detection (Chapter 2, section 2.2.2), and one voltage level is required for the resonance frequency detection. In order to provide flexibility, we use a 4-channel multiplexer to provide four choices for V_{thld} . In this way, we can switch the threshold-levels easily by programming the multiplexer. To generate these voltage levels (V_{thld1} , V_{thld2} , V_{thld3} and V_{thld4}), we implement resistive dividers with potentiometers.

5. Common-mode voltage (V_{cm}) generation

A resistive divider implemented with potentiometer between the 3.3V supply and ground is used to generate the common-mode voltage.

6. Supply

- Positive DC voltage supply
- Bias-current source for the front-end amplifier and the comparator
- Bias-current source for the source follower (Chapter3, section 3.5)

4.3 Impedance analysis

We use the impedance analysis approach (Chapter1, section 1.2) to measure the resonance frequency and the quality factor of a sample resonator (SH0_AF70910) in this section. The samples have been measured at Holst Centre. The measured results are shown below:

- $R_m = 396.3k\Omega$
- $C_m = 1.904fF$
- $L_m = 46.35H$
- $C_p = 4.197pF$

With Equation (1-1) and (1-3), we conclude:

$$f_{res} = 535.8 \text{ kHz} \quad (4-1)$$

$$Q = 393.7 \quad (4-2)$$

Thus, we obtain a resonance frequency and quality factor value that will be used as a benchmark to compare the results obtained with ring-down based measurements.

According to [1], DC voltage biasing of the resonator leads to a resonance frequency shift. To check the bias dependence of the resonator, we repeat the above measurement with different DC bias voltages (V_{DC}).

We apply the same excitation (100mV), and calculate the resonance frequency under different bias (from -1.5V to +2V). The results are shown in Table 4-1 and Figure 4-7.

| $V_{DC}(V)$ | -1.5 | -1 | -0.5 | 0 | 0.5 | 1 | 1.5 | 2 |
|----------------|---------|---------|---------|---------|---------|---------|---------|---------|
| $f_{res}(kHz)$ | 535.983 | 535.817 | 535.733 | 535.533 | 535.333 | 535.150 | 534.983 | 534.833 |

Table 4-1: Biasing voltage dependency

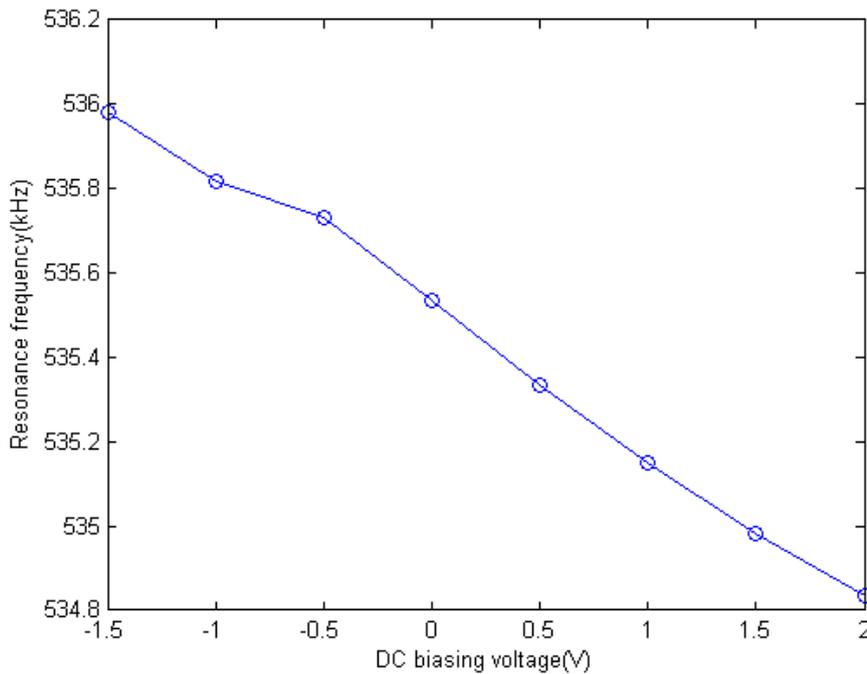


Figure 4-7: Biasing voltage dependency

Hence, we obtain the DC bias dependency of the resonator is 0.053%/V. This result will also be compared to ring-down based measurements in the next section.

4.4 Measurement results

In this section, an overview of the results obtained using the ring-down measurement approach is described in two parts: resonance frequency measurement and quality factor measurement.

4.4.1 Resonance frequency

The sensor we measured as example is also SH0_AF70910. We apply an excitation signal with 100mV amplitude and a frequency of 536 kHz (generated by a function generator) for the ring-down measurement. Feedback capacitors are selected with a total capacitance of 100fF while R_1 is selected to be 400k Ω and the amplification factor is 9 ($R_3= 900k\Omega$, $R_2=100k\Omega$). The threshold voltage is 1.65V, and the common-mode voltage is 1.1V. We obtain the results shown in Figure 4-8.

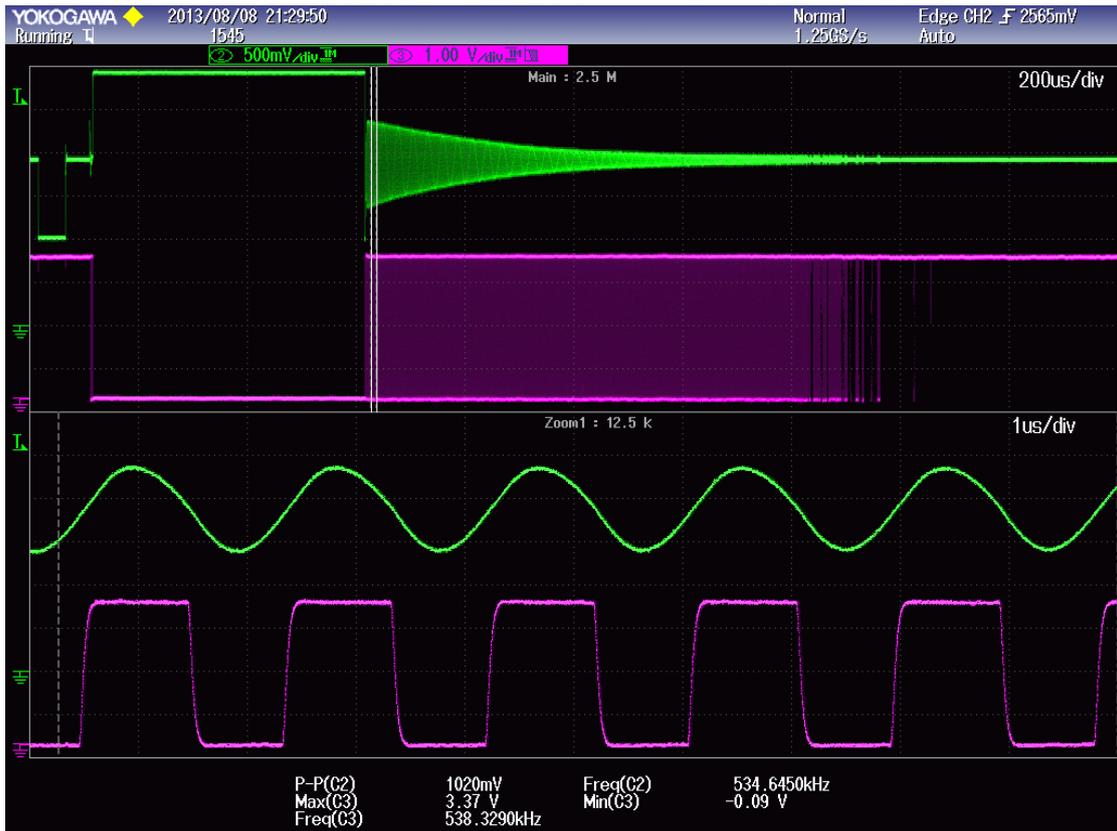


Figure 4-8: Measurement results shown on the oscilloscope

Figure 4-8 shows a frequency counting measurement lasting 2ms. The lower half side is the close-up view of the initial ring-down signal of the measurement, where a clear square wave around 535 kHz can be seen.

The resonance frequency can be calculated using Equation (2-4) (Chapter 2, section 2.2.2). We rewrite the equation here:

$$f_{res} = \frac{N}{t} = \frac{N}{M} \cdot f_0 \tag{4-3}$$

In the measurement, the FPGA counts $N=300$ ring-down cycles, with $f_0=25\text{MHz}$ (see Appendix II for the code). Figure 4-9 displays the calculated values of f_{res} for 1000 successive measurements (iterations).

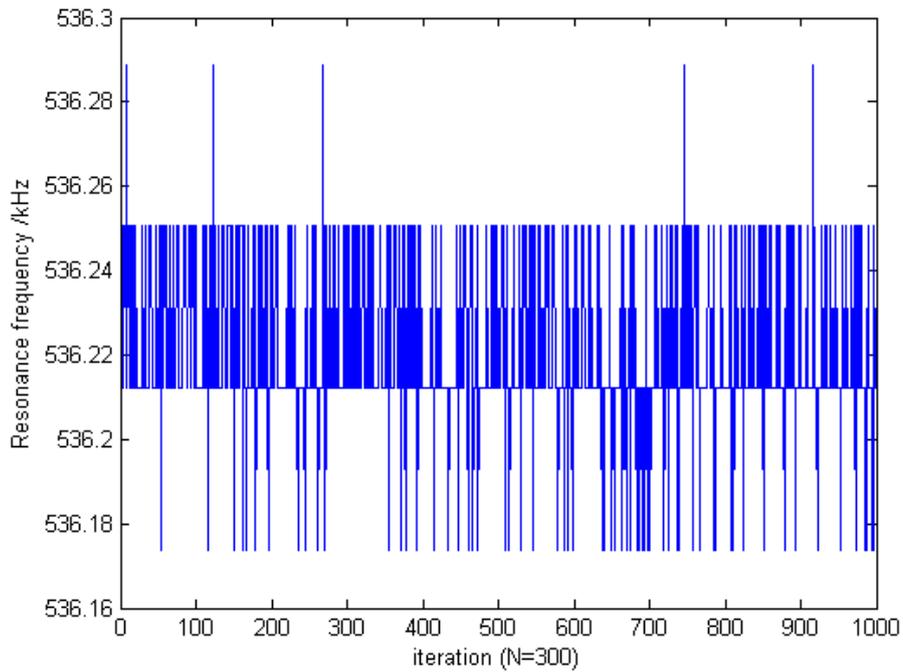


Figure 4-9: Measured resonance frequency

The average of these 1000 results is:

$$f_{res} = 536.220\text{kHz}$$

Compared with Equation (4-1) (f_{res} obtained by impedance measurement), this result is off by 0.07%, this is partially because with ring-down measurement, the resonator is actually biased at a voltage around -1.1V during the ring-down phase, since the input of the I-V converter is biased at the common-mode voltage, and thus produces a bit bigger f_{res} value.

4.4.1.1 Initial amplitude versus the value of the feedback resistor

In this sub-section, we demonstrate the programmability of the feedback network of I-V converter by reporting the measured initial amplitude of the ring-down signal for different values of R_1 (Chapter 3, Figure 3-1), while the other conditions remain the same. Firstly, the gain of I-V converter has been simulated for seven distinct combinations of R_1 , from 100k Ω to 700k Ω . The simulated results are normalized to the gain for 400k Ω . The normalized results are shown in Table 4-2 and Figure 4-10 ('o' line).

| R_1 (k Ω) | 100 | 200 | 300 | 400 | 500 | 600 | 700 |
|---------------------|------|------|------|-----|------|------|------|
| Normalized gain | 0.52 | 0.74 | 0.93 | 1 | 1.15 | 1.23 | 1.31 |

Table 4-2: Normalized gain of I-V converter vs. R_1

In this measurement, we also take seven distinct combinations of R_1 , from 100k Ω to 700k Ω . The results are shown in Table 4-3 and Figure 4-10 (' Δ ' line).

| R_1 (k Ω) | 100 | 200 | 300 | 400 | 500 | 600 | 700 |
|-----------------------|------|------|------|------|------|------|------|
| A_{0p-p} (V) | 0.38 | 0.78 | 0.83 | 1.02 | 1.16 | 1.28 | 1.34 |
| Normalized A_{0p-p} | 0.37 | 0.76 | 0.81 | 1 | 1.14 | 1.25 | 1.31 |

Table 4-3: Initial amplitude vs. R_1

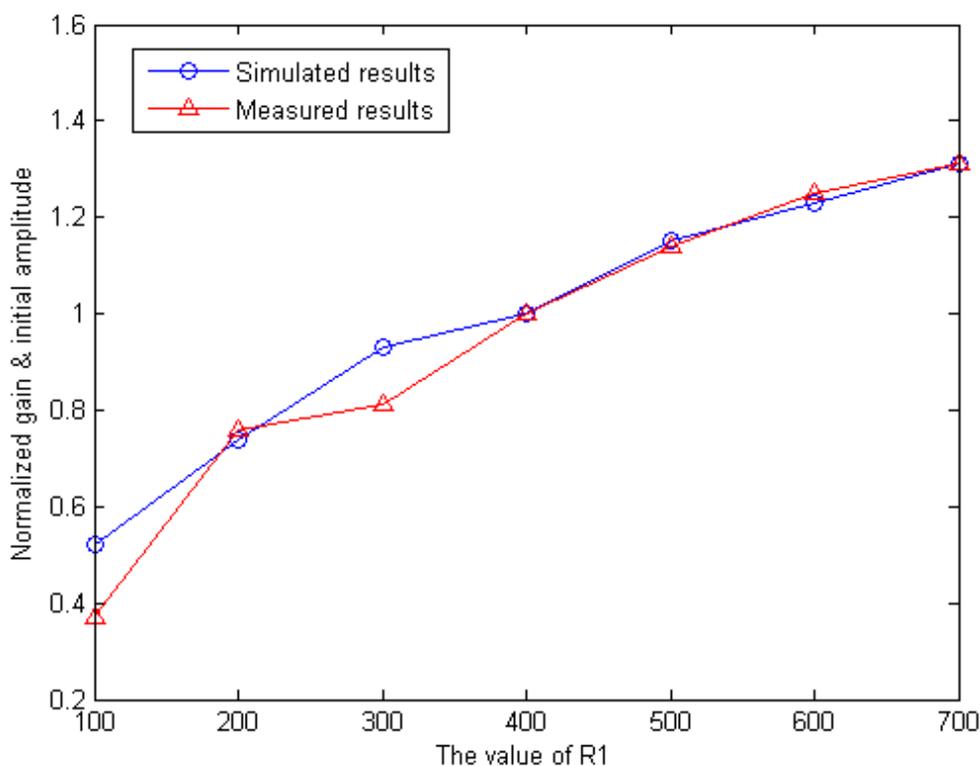


Figure 4-10: Simulated results & measured results vs. R_1

It can be seen from the Figure 4-10 that the measured results basically agree with the simulated results.

4.4.1.2 Resonance frequency versus number of ring-down cycles

In this sub-section, we report the resonance frequency calculated from different numbers of ring-down cycles, while the other conditions remain the same. There are two aspects that decide the detection limit ($\sigma (\Delta f_{res}/f_{res})$): noise and quantization error. By analyzing the results, we can determine whether the circuit is limited by thermal noise or quantization error.

The detection limit caused by thermal noise can be calculated by Equation (2-22) (Chapter 2,

section 2.4.2). For clarity, we rewrite the equation here:

$$\sigma\left(\frac{\Delta f_{\text{res}}}{f_{\text{res}}}\right) = \frac{V_{n,\text{RMS}}}{2 \cdot \pi \cdot N \cdot A_0 \cdot e^{-\frac{\pi \cdot N}{Q}}} < 10^{-4} \quad (4-4)$$

We use the SNR obtained from the simulation results with a value of 172, with a quality factor of around 390, according to Equation (4-4), we have the detection limit with different number of ring-down cycles based on thermal noise in Table 4-4.

| N | 50 | 100 | 150 | 200 | 250 | 300 |
|--|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|
| $\sigma(\Delta f_{\text{res}}/f_{\text{res}})$ | 0.276×10^{-4} | 0.207×10^{-4} | 0.206×10^{-4} | 0.231×10^{-4} | 0.277×10^{-4} | 0.345×10^{-4} |

Table 4-4: Detection limit vs. N based on thermal noise

The quantization step is equal to $f_{\text{res}}/N/f_0$, which is represented by the symbol ‘ Δ ’. According to [3], the squared standard deviation (σ^2) caused by quantization noise is equal to $\Delta^2/12$. Since we have two quantization noises at the first cycle and the last cycle, which is uncorrelated, the squared standard deviation (σ^2) caused by quantization noises is $\Delta^2/6$. Therefore, the detection limit (σ) caused by quantization noise can be calculated by Equation (4-5).

$$\sigma\left(\frac{\Delta f_{\text{res}}}{f_{\text{res}}}\right) = \frac{f_{\text{res}}}{N \cdot f_0} / \sqrt{6} \quad (4-5)$$

We use the reference clock with a frequency of 25MHz. With a resonance frequency of around 536kHz, we have the detection limit with different number of ring-down cycles based on quantization noise in Table 4-5.

| N | 50 | 100 | 150 | 200 | 250 | 300 |
|--|-----------------------|------------------------|------------------------|------------------------|------------------------|------------------------|
| $\sigma(\Delta f_{\text{res}}/f_{\text{res}})$ | 1.75×10^{-4} | 0.875×10^{-4} | 0.584×10^{-4} | 0.438×10^{-4} | 0.350×10^{-4} | 0.292×10^{-4} |

Table 4-5: Detection limit vs. N based on quantization noise

Combined with Table 4-4, the detection limit caused by the total noise can be calculated by adding these two uncorrelated noise together. The results are shown in Table 4-6 and Figure 4-11 (‘ σ' line).

| N | 50 | 100 | 150 | 200 | 250 | 300 |
|--|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|
| $\sigma(\Delta f_{\text{res}}/f_{\text{res}})$ | 1.771×10^{-4} | 0.915×10^{-4} | 0.619×10^{-4} | 0.495×10^{-4} | 0.446×10^{-4} | 0.452×10^{-4} |

Table 4-6: Detection limit (simulated) vs. N

In the measurement, we repeat the measurement 1000 iterations. To calculate the detection limit for the measurement results, we calculate the standard derivation of the f_{res} divided by the

average value of the f_{res} . The detection limit obtained by measurement results is shown in Table 4-7 and Figure 4-11 ('Δ' line).

| N | 50 | 100 | 150 | 200 | 250 | 300 |
|----------------------------------|-----------------------|------------------------|------------------------|------------------------|------------------------|------------------------|
| $\sigma(\Delta f_{res}/f_{res})$ | 1.97×10^{-4} | 1.072×10^{-4} | 0.661×10^{-4} | 0.547×10^{-4} | 0.490×10^{-4} | 0.500×10^{-4} |

Table 4-7: Detection limit vs. N based on measurement results

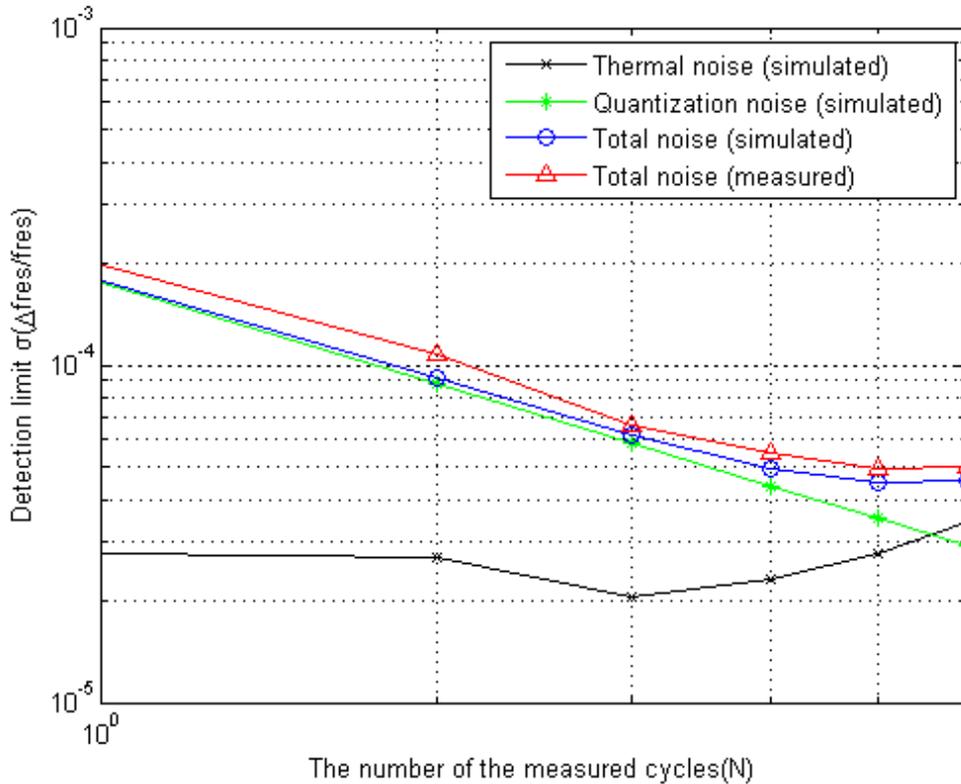


Figure 4-11: Detection limit vs. N (log-log scale)

This shows that when N is small with a value of 50 or 100, the detection limit is limited by the quantization error. By measuring more cycles, the error caused by quantization is reduced while the error caused by the thermal noise increases. Hence, our detection limit is 0.5×10^{-4} .

According to Equation (4-4), the signal-to-noise ratio for N=300 is:

$$SNR = \frac{A_0}{V_{n,RMS}} = \frac{1}{0.500 \times 10^{-4} \cdot 2 \cdot \pi \cdot 300 \cdot e^{-\frac{300\pi}{390}}} = 118.8$$

This result is smaller than the simulated result (172.4) because this result includes both the thermal noise and the quantization noise. However, the simulation result only includes the thermal noise.

4.4.1.3 Resonance frequency versus DC biasing

In this subsection, we report the measured resonance frequency for different DC biasing voltage. Firstly, we illustrate how we apply different DC biasing conditions to the resonator. This requires a small modification to the setup, as shown in Figure 4-12, since the DC biasing in the original design is determined by the common-mode voltage at the input of the front-end amplifier, which cannot be changed over a significant voltage range.

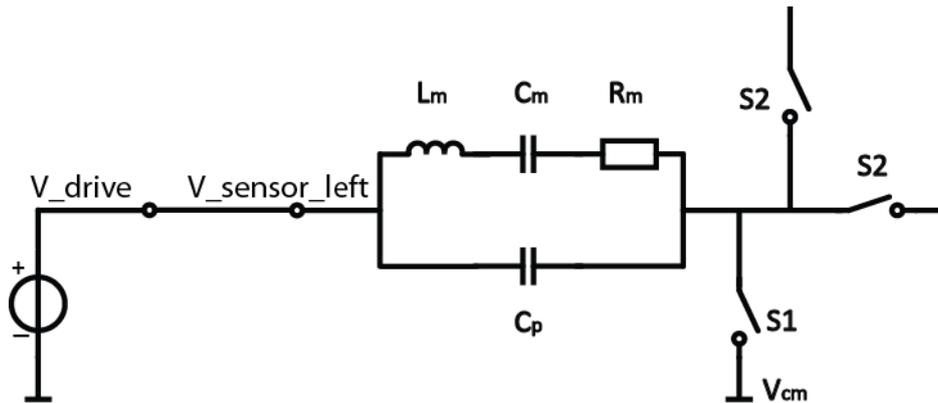


Figure 4-12: The modified setup to measure the DC biasing voltage

We connect the V_drive and V_sensor_left together to bypass the switches between them. By changing the DC offset of the excitation signal, we can bias the resonator at different DC voltages. Since we have already biased the resonator with a common-mode voltage of 1.1V, the DC offset of the excitation signal is from -0.4V to 3.1V to achieve a biasing voltage from -1.5V to 2V. With the new measurement setup, we obtain the measurement results of the resonance frequency versus DC biasing shown in Table 4-8 and Figure 4-13.

| | | | | | | | | |
|----------------|---------|---------|---------|---------|---------|---------|---------|---------|
| $V_{DC}(V)$ | -1.5 | -1 | -0.5 | 0 | 0.5 | 1 | 1.5 | 2 |
| $f_{res}(kHz)$ | 536.366 | 536.136 | 536.040 | 535.904 | 535.660 | 535.510 | 535.387 | 535.230 |

Table 4-8: f_{res} vs. V_{DC}

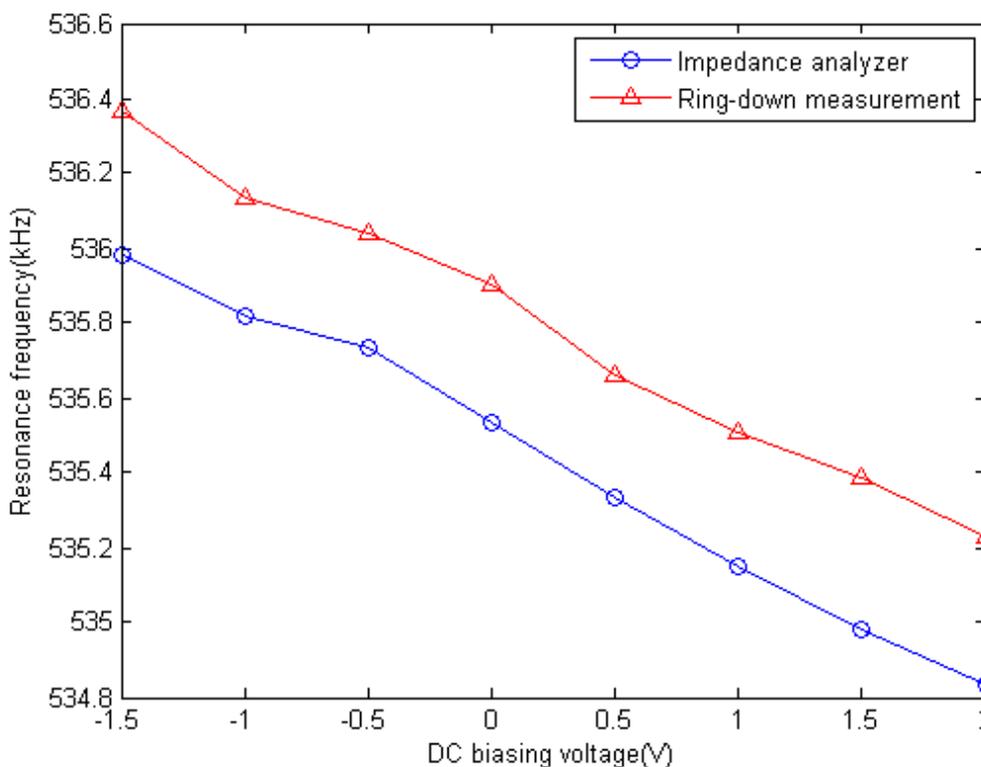


Figure 4-13: Impedance analyzer vs. Ring-down measurement

After simple calculations based on Figure 4-13('Δ' line), we conclude that the DC biasing dependency of the resonator is around 0.06%/V. This result nicely agrees with what we obtained using impedance measurement (Figure 4-13 'o' line). It is clear that the slope is identical. The offset between the curves could be caused by changes in the environmental conditions between the measurements.

4.4.1.4 Expose to water vapor

According to [2], in the resonance frequency measurements, when we breathe on the sensor gently during continuous monitoring, even though uncoated, we can still see some frequency shift in the measurement results. This experiment leads to the measurement results as shown in Figure 4-14.

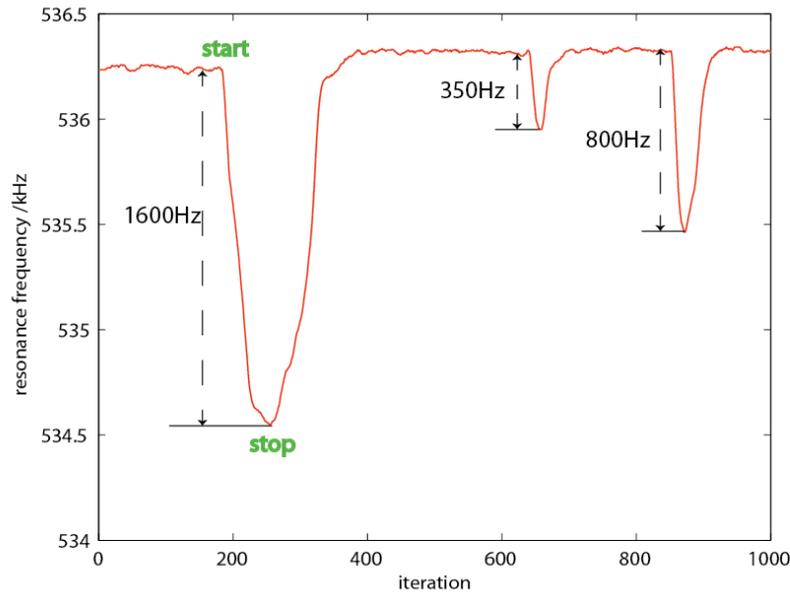


Figure 4-14: Resonance frequency shift measured while breathing on the sensor

To have sufficient time to see the changes of f_{res} , we take 1000 repeated measurements, which is around 2s measurement time in total. We apply a 10-point moving-average filter to improve the resolution. Due to different breath levels, we achieve different shifts as shown in Figure 4-14. We breathe strongly in the first time; consequently, the shift is bigger with a value of around 1600Hz. Conversely, we breathe slightly in the second time, and then the shift is smaller with a value of only 350Hz.

As a result, we conclude that f_{res} decreases while blowing over the sensor and eventually comes back to the original value after the blowing has stopped. A similar behavior of the sensor response to humidity can be found in [2].

4.4.2 Quality factor

Two threshold voltages need to be applied to measure the quality factor (Chapter 2, section 2.2.2). For each threshold voltage, the total number of ring-down cycles needs to be recorded.

Similar with the measurement of f_{res} , we apply an excitation signal with an amplitude of 100mV, a frequency of 536 kHz; and a common-mode voltage equal to 1.1V. Again, for each threshold voltage, we repeat 1000 measurements. In these 1000 results, a few values appear that are far away from the average value due to noise or other uncertainties; hence, we take the median value among the 1000 results to represent Q.

Although two threshold-levels are enough for quality factor measurement, we take three voltage levels to make more combinations and take an average value to reduce the influence of the noise and other uncertainties. We use symbol ' ΔV_{thld} ' to represent the applied threshold-level (V_{thld})

relative to the output DC-level (1.65V), and 'N' for measured number of ring-down cycles. The measurement results are listed in Table 4-9.

| Point | V_{thld} | $\Delta V_{thld} (V_{thld}-1.65V)$ | N |
|-----------|------------|------------------------------------|-----|
| P1(a1,N1) | 1.75 | 0.1 | 261 |
| P2(a2,N2) | 1.85 | 0.2 | 172 |
| P3(a3,N3) | 1.95 | 0.3 | 124 |

Table 4-9: Quality factor measurement results

The quality factor can be calculated by the following equation:

$$Q = \frac{\pi \cdot \Delta N}{\ln(a_1/a_2)} \quad (4-6)$$

Thus, we obtain the results shown in Table 4-10.

| Points | P1,P2 | P2,P3 | P1,P3 |
|------------|-------|-------|-------|
| ΔN | 89 | 48 | 137 |
| Q | 403 | 372 | 392 |

Table 4-10: Results of quality factor

The three results we obtained (Table 4-10) provide an average value to represent Q; hence, we have:

$$Q = 389 \quad (4-7)$$

This result nicely matches what we obtained by impedance measurement (Equation (4-2)).

4.4.3 Energy consumption

To calculate the energy consumption, we measure the total DC current consumed by the chip through the pin 'vdd' (voltage supply for the I-V converter and the comparator, see Appendix III, Table III-1). The total measurement time is 2ms. The final results are listed in Table 4-11.

| Supply voltage | Supply current | Time | Energy consumption |
|----------------|----------------|------|--------------------|
| 3.3V | 31.5 μ A | 2ms | 207.9nJ |

Table 4-11: Energy consumption

The reference currents ('I_2nd' and 'I_comp', see Appendix III, Table III-1) we apply are a bit less than what have been applied in the simulation; hence, the total DC current consumption is less than what we expected (Chapter 3, Table 3-1).

Thus, we obtain the final energy consumption of 207.9nJ per measurement, less than what we derived in the simulation (252.45nJ per measurement, see section 3.7.3). As mentioned before (Chapter 3, section 3.7.3), by reducing the measurement time, we expect to achieve an energy consumption of around 156nJ per measurement.

4.5 Conclusions

In this chapter, we have reported the resonance frequency and quality factor of the resonator measured using two methods: ring-down measurement and, for comparison, impedance measurement. We summarize the results in Table 4-12:

| Method | f_{res} | Q |
|-----------------------|-----------|-----|
| Impedance measurement | 535.8kHz | 393 |
| Ring-down measurement | 536.2kHz | 389 |

Table 4-12: Summary of results

Both resonance frequency and quality factor of these two methods are nicely in agreement. The resonance frequency shift due to DC biasing (0.06%/V) is also in nicely agreement with what we obtained with impedance measurement (0.053%/V). The measured detection limit shows, as expected, a quantization-noise-dominated behavior at for small numbers of ring-down cycles, and a thermal-noise-dominated behavior at larger numbers of cycles. The measured values are in good agreement with the detection limit predicted by the analysis presented in this thesis. The measurement of breath on the sensor shows the resonance frequency responds to humidity in breath.

References

- [1] D. M. Karabacak, "Enhanced sensitivity volatile detection with low power integrated," Lab on a Chip, vol. 10, pp. 1976-1982, Apr. 2010
- [2] Z.Zeng, "Energy-efficient Readout of Resonant Sensors", Master thesis, October 2011.
- [3] Quantization (signal processing), Wikipedia,
[https://en.wikipedia.org/wiki/Quantization_\(signal_processing\)](https://en.wikipedia.org/wiki/Quantization_(signal_processing))

Chapter 5

Conclusions and Future Work

5.1 Conclusions

Micromachined resonant sensors have been developed at Holst Centre for the measurement of gas concentration [1]. These sensors consist of a high aspect (length/thickness) ratio doubly-clamped silicon nitride beam with integrated piezoelectric (aluminum nitride) transducers, which can be used to achieve high sensitivity and ultra low power consumption. By applying appropriate coatings to these resonators, they can be utilized to sense concentration of volatile organic compounds like ethanol, benzene etc, by measuring shifts in resonance frequency f_{res} and quality factor Q . These characteristics make them a very promising candidate for application in wireless autonomous sensor systems. However, an energy-efficient interface circuit is required to fulfill this promise. This thesis describes the design and performance of such a sensor interface.

There are three main approaches for the measurement of resonance frequency and quality factor of resonant sensors: impedance analysis, oscillator-based readout, and ring-down measurement [1] [2] [3]. In this work, we apply the ring-down measurement technique. Several studies and PCB implementations of the ring-down measurement technique have been reported in the literature [4] [5] [6] [7]. An integrated implementation of this technique has also been reported [1]. Compared with the previous integrated implementation, our implementation is less sensitive to the leakage current, allowing more ring-down cycles to be detected. Moreover, the measurement time has been significantly reduced by applying a more efficient implementation of the auto-zeroing technique that only requires a single excitation of the sensor to cancel DC offset, rather than the two excitations required previously. Another significant improvement of our work is its configurability, allowing the interface to be applied to various different sensors.

The interface system is composed of four main parts: a switched excitation source that excites the resonator at a frequency close (not necessarily equal) to its resonance frequency, an auto-zeroed I-V converter that amplifies the ring-down current to a readable ring-down voltage, an auto-zeroed comparator that detects the zero-crossings of the ring-down voltage, and finally a counting circuit that extract the frequency of the zero-crossings. Moreover, in our implementation, the quality factor can be measured easily by applying non-zero threshold levels for the comparator.

Studies and analysis have been made at the architecture level design. For the front-end circuit, the signal-to-noise ratio requirement has been derived by analyzing the timing jitter. And the resulting trans-conductance of at least $200\mu\text{S}$ has been obtained by analyzing the thermal noise and signal amplitude. In terms of the comparator, the delay time of the comparator is 37.5ns while the input offset is cancelled by auto-zeroing technique. And the minimum reference frequency for the counting circuitry is 27MHz .

In the circuit level design, we use an auto-zeroed two-stage amplifier and an auto-zeroed two-stage comparator to achieve the required performance. We have applied low-leakage switches to improve the performance and programmable feedback network to achieve the configurability. And shift register and source follower are applied for the testability. Simulation results of the circuit-level design have been analyzed (see section 3.3) in terms of signal amplitude, noise, offset and energy consumption.

After the layout design, a prototype chip has been fabricated in $0.35\text{-}\mu\text{m}$ CMOS technology. Together with a test PCB, a FPGA development board and a DAQ board on which the digital part of the readout circuit has been implemented, a fully-functional interface based readout approach has been realized.

The same resonator has been measured by using two different methods: the proposed ring-down measurement using our prototype chip, and, for comparison, impedance analysis using a bench-top impedance analyzer. The measured resonance frequencies and quality factors (Chapter 4, Table 4-9), show good consistency. The initial amplitude of the ring-down signal varies with different feedback resistors. The measured resonance frequency shifts with changing DC biasing in both methods are also in good agreement. Moreover, measurements have been shown that demonstrate the transient response of the sensor to humidity.

With a total current consumption of $31.5\mu\text{A}$ in a measurement time of 2ms , we have a low energy consumption of 207.9nJ per measurement (which is expected to be reduced to 156nJ per measurement by applying a shorter measurement time of 1.5ms , section 4.4.3). The energy consumption is lower than the previous work with a power consumption of 236.9nJ .

5.2 Future Work

Beyond the prototype chip, the proposed sensor interface could be further improved. A summary of several potential improvements is provided below.

- Develop an optimized low-power excitation circuit, which can be applied when the

approximate resonance frequency is unknown. For instance, this can be implemented by developing an optimized frequency-searching algorithm based on the readout circuit we have now.

- Optimize the design of the comparator by adding hysteresis to make the zero-crossing detection less sensitive to noise. Moreover, the energy consumption of the comparator can be reduced by redesigning it with a longer propagation delay since the comparator currently used is somewhat over-designed.
- Optimize the layout design to reduce the parasitic problem
Separate the excitation signal and the output of the source follower to cancel the coupling effect from the excitation signal to the output of the source follower. And use a digital I/O pad for the digital output of the readout interface to reduce the parasitic coupling effect from the digital output to the input of the front-end amplifier.
- Do measurements in a gas chamber to check how the readout circuit in combination with a functionalized resonator responds to actual changing concentrations of a suitable volatile organic compound.

References

- [1] Z. Zeng, M. A. P. Pertijs and D. M. Karabacak, "An Energy-Efficient Readout Circuit for Resonant Sensors Based on Ring-Down Measurement," *Review of Scientific Instruments*, 84, 025005, Jan. 2013.
- [2] M. Patrascu, J. Pettine, D.M. Karabacak, M. Vandecasteele, S.H. Brongersma, M. Crego-Calama "Oscillator-based volatile detection system using doubly-clamped micromechanical resonators" *Procedia Engineering*, 25 (2011), pp. 1533–1536
- [3] B. Jakoby, "A novel analog readout electronics for microacoustic thickness shear-mode sensors", *IEEE Sensors Journal*, vol. 5, pp. 1106-1111, Oct. 2005.
- [4] M. Rodahl, F. Höök, A. Krozer, P. Brzezinski, and B. Kasemo, "Quartz crystal microbalance setup for frequency and Q-factor measurements in gaseous and liquid environments," *Rev. Sci. Instrum.*, vol. 66, no. 7, pp. 3924-3930, July 1995.
- [5] M. Rodahl and B. Kasemo, "A simple setup to simultaneously measure the resonant frequency and the absolute dissipation factor of a quartz crystal microbalance," *Rev. Sci. Instrum.*, vol. 67, no. 9, pp.3238-3241, Sept. 1996.
- [6] K. Zeng, K.G. Ong, C. Mungle, and C.A. Grimes, "Time domain characterization of oscillating sensors: Application of frequency counting to resonance frequency determination," *Rev. Sci. Instrum.*, vol. 73, no. 12, pp. 4375-4380, Dec. 2002.
- [7] K. Zeng and C.A. Grimes, "Threshold-crossing counting technique for damping factor determination of resonator sensors," *Rev. Sci. Instrum.*, vol. 75, no. 12, pp. 5257-5261, Dec. 2004.

Appendix I Noise calculation

The output root-mean-square (RMS) noise of the I-V converter can be calculated as:

$$V_{n,RMS} = \sqrt{\int_0^{\infty} S_Y(f) df} \quad (1)$$

where $S_Y(f)$ is the I-V converter's output noise power spectral density (PSD). This can be obtained by:

$$S_Y(f) = S_X(f) \cdot |H(f)|^2 \quad (2)$$

where $S_X(f)$ is the input-referred noise PSD of the I-V converter and $H(f)$ is the transfer function of the I-V converter.

Three noise sources (Figure 2-11) are uncorrelated. The noise generated by R_m tends to be negligible, so we only consider the noise generated by feedback resistors ($V_{n,f}$) and the noise of the OTA ($V_{n,a}$). We calculate them separately, and then add them together to get the total RMS noise.

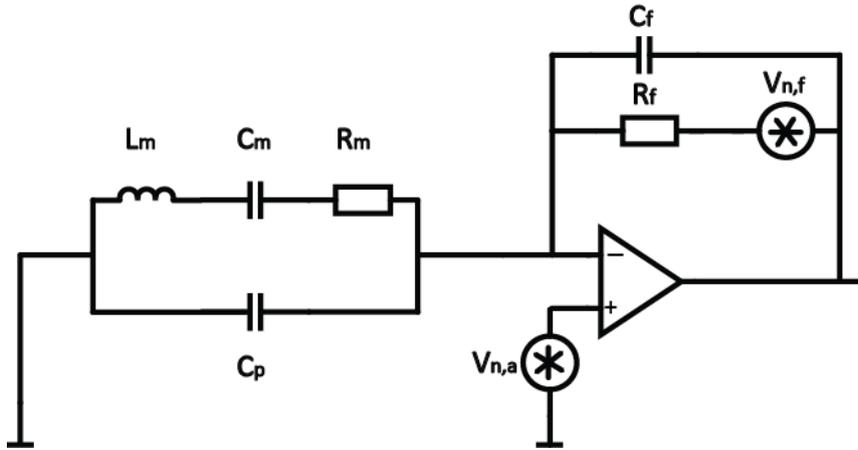


Figure I-1: circuit used for noise analysis

Noise of the OTA ($V_{n,a}$)

Figure I-1 demonstrates the circuit used for noise analysis. $V_{n,a}$ represents the equivalent input noise PSD of the OTA, with a value of $(8/3)kT/g_m$ (section 2.4.3). With the assumption we made in section 2.4.3 (modeling the OTA as a voltage-controlled current source with infinite DC gain), we compute the transfer function $H(f)$ from $V_{n,a}$ to V_{out} :

$$H(f) = \frac{g_m \cdot [R_f \cdot (C_p + C_f) \cdot 2 \cdot \pi \cdot f \cdot j + 1]}{(g_m + C_p \cdot 2 \cdot \pi \cdot f \cdot j) \cdot (R_f \cdot C_f \cdot 2 \cdot \pi \cdot f \cdot j + 1)} \quad (3)$$

Based on the above equation, we know there are two poles and one zero in the circuit at:

$$f_{p,1} = \frac{g_m}{2 \cdot \pi \cdot C_p}$$

$$f_{p,2} = \frac{1}{2 \cdot \pi \cdot R_f \cdot C_f}$$

$$f_{z,1} = \frac{1}{2 \cdot \pi \cdot R_f \cdot (C_p + C_f)}$$

Moreover, the gain at low frequencies is equal to unity gain. The gain at high frequencies can be calculated as:

$$\lim_{f \rightarrow \infty} |H(f)| = \frac{g_m \cdot (C_p + C_f)}{C_p \cdot C_f \cdot 2 \cdot \pi \cdot f}$$

If we assume $f_{p,2}$ is lower than $f_{p,1}$ and higher than $f_{z,1}$, the gain at $f_{p,1}$ is equal to

$$|H(f_{p,1})| = \frac{C_p + C_f}{C_f}$$

Therefore, the noise spectrum at the output of the amplifier can be approximated by the sketch shown in Figure I-2.

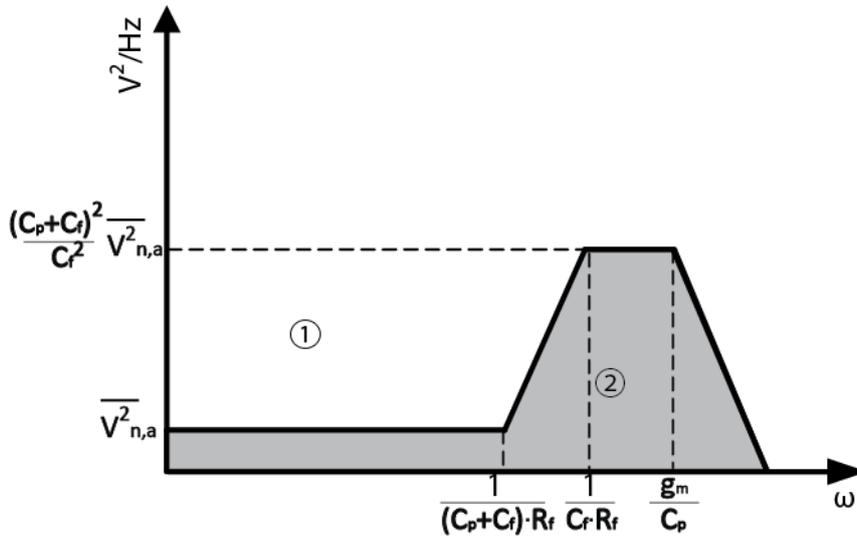


Figure I-2: noise spectrum shaping by a parallel capacitor

In order to calculate the output root-mean-square (RMS) noise, one straightforward method is applying Equation (1) directly. A simpler approach, however, is to calculate the sum of the shaded areas in Figure II-2, which equals the integrated output noise. Then, after applying the square root, the output root-mean-square (RMS) noise is obtained. The shaded area labeled by ② and a blank area labeled by ① are defined for convenience of calculation.

Firstly, the sum of ① and ② is computed. This part can be considered as a first-order filter with a DC gain of $V_{n,a}$ multiplied by $(C_p+C_f)/C_f$ and the corner frequency of $g_m/2\pi C_p$. Hence, the area is:

$$V_{n,sum}^2 = \frac{2 \cdot k \cdot T \cdot (C_p + C_f)}{3 \cdot C_f \cdot C_p} \quad (4)$$

Secondly, we calculate the area of ① by considering it as a first-order filter with a DC gain of $V_{n,a}$ multiplied by C_p/C_f and the corner frequency of $1/2\pi R_f(C_p+C_f)$. As a result, the area is:

$$V_{n,1}^2 = \frac{2 \cdot k \cdot T \cdot C_p}{3 \cdot g_m \cdot C_f \cdot R_f \cdot (C_p + C_f)} \quad (5)$$

Finally, the area of ② ($V_{n,a,out}^2$) is achieved by subtracting Equation (5) from (4),

$$V_{n,a,out}^2 = \frac{2 \cdot k \cdot T \cdot (C_p + C_f)}{3 \cdot C_f \cdot C_p} - \frac{2 \cdot k \cdot T \cdot C_p}{3 \cdot g_m \cdot C_f \cdot R_f \cdot (C_p + C_f)} \quad (6)$$

Noise generated by feedback resistors ($V_{n,f}$)

Without filtering capacitor, the noise generated by the feedback resistors $V_{n,f}$ is added to the output of the amplifier directly. After adding this capacitor, this noise is filtered by the parallel capacitor. Therefore, the calculation of this noise can be simply regarded as the noise generated by a low-pass RC filter. According to [II.1], this noise can be calculated by Equation (7).

$$V_{n,f,out}^2 = \frac{k \cdot T}{C_f} \quad (7)$$

Hence, in total, the output root-mean-square (RMS) noise is:

$$V_{n,RMS} = \sqrt{\frac{k \cdot T \cdot (5 \cdot C_p + 2 \cdot C_f)}{3 \cdot C_f \cdot C_p} - \frac{2 \cdot k \cdot T \cdot C_f}{3 \cdot g_m \cdot C_p \cdot R_f \cdot (C_p + C_f)}} \quad (8)$$

This expression has been cross-checked against the simulation results.

Reference

[II.1] B. Razavi, Design of Analog CMOS Integrated Circuits. Boston: McGraw-Hill, 2001.

Appendix II Verilog code

```
module digital ( Vout, clk, clkfast, start, thlds1, thlds2, A1, A2, S1, S2, Saz, Sazc, SF_en, load,
count_M, count_N);

input Vout, clk, clkfast, start, thlds1, thlds2;
output S1, S2, Saz, Sazc, SF_en, load, A1, A2, count_M, count_N;

reg[15:1]clk_reg;//measurement time=2ms 15bits 10MHzclock
reg[9:1]Vout_reg;//counting N N=300 9bits
reg[9:1]count_N;//output for measured N
reg[15:1]clkfast_reg;//counting M 16bits 25MHz clock
reg[15:1]count_M;//output for measured M
reg S1;
reg S2;
reg Saz;
reg Sazc;
reg Sthld;
reg Vout_sync;//read Vout from output of chip
reg counting_start;//start
reg load;//start to piso
wire SF_en;
wire A1;
wire A2;

assign SF_en = 1'b1;
assign A1 = thlds1 & Sthld;
assign A2 = thlds2 & Sthld;

// FPGA is triggered by start signal from DAQ,begin to count when start==1
always @ (posedge clk)
begin
if(start == 1'b0)
begin
clk_reg <= 15'b000000000000000;
end
else
begin
```

```
    clk_reg <= clk_reg+1'b1;
    if(clk_reg == 15'b100111000100000) //start a new measurement when t=2ms
        begin
            clk_reg <= 15'b000000000000000;
        end
    end
end

// generate control signal S1
always @ (posedge clk)
begin
    if(clk_reg >= 15'b000001111101000 && clk_reg < 15'b001011101110000)
        begin
            S1 <= 1'b1;//1
        end
    else
        begin
            S1 <= 1'b0;//0
        end
    end

// generate control signal S2
always @ (posedge clk)
begin
    if(clk_reg >= 15'b000001111101000 && clk_reg < 15'b001011101110000)
        begin
            S2 <= 1'b0;//0
        end
    else
        begin
            S2 <= 1'b1;//1
        end
    end

// generate control signal Saz
always @ (posedge clk)
begin
    if(clk_reg > 15'b000000000000000 && clk_reg < 15'b000000111110100)
        begin
```

```
Saz <= 1'b1;//1
end
else
begin
Saz <= 1'b0;//0
end
end

// generate control signal Sazc
always @ (posedge clk)
begin
if(clk_reg > 15'b0000000000000000 && clk_reg < 15'b000001110110110)
begin
Sazc <= 1'b1;//1
end
else
begin
Sazc <= 1'b0;//0
end
end

// generate threshold voltage control auto-zeroing
always @ (posedge clk)
begin
if(clk_reg > 15'b0000000000000000 && clk_reg < 15'b000001111101000)
begin
Sthld <= 1'b0;
end
else
begin
Sthld <= 1'b1;
end
end

// define the staring time of counting
always @ (posedge clk)
begin
if(clk_reg >= 15'b001011110100010)//begin to count when t=605us
begin
```

```
        counting_start <= 1'b1;
    end
else
    begin
        counting_start <= 1'b0;
    end
end

// define the starting time of loading
always @ (posedge clk)
begin
    if(clk_reg >= 15'b100011010110100)//begin to load when t=1.81ms
        begin
            load <= 1'b1;
        end
    else
        begin
            load <= 1'b0;
        end
    end

//read Vout from output of the chip at the negative edge of clkfast
always @ (negedge clkfast)
begin
    Vout_sync <= Vout;
end

// counting Vout
always @ (posedge Vout_sync)
begin
    if(counting_start == 1'b0)
        begin
            Vout_reg <= 9'b000000000;
        end
    else
        begin
            if(Vout_reg < 9'b111111111)
                begin
                    Vout_reg <= Vout_reg + 1'b1;
                end
            else
                Vout_reg <= 9'b111111111;
            end
        end
    end
end
```

```
        end
    end
end

// counting clkfast
always @ (posedge clkfast)
begin
if(Vout_reg == 9'b000000000 || counting_start == 1'b0)
    begin
        clkfast_reg <= 15'b00000000000000000; //start to count when Vout is counted
        count_M <= 15'b00000000000000000;
        count_N <= 9'b000000000;
    end
else
    begin
        if(Vout_reg > 9'b100101100) //stop to count when N=300
            begin
                count_M <= clkfast_reg;
            end
        else if(clk_reg > 15'b100011001010000) //load N when t=1.8ms if N<300
            begin
                count_N <= Vout_reg;
            end
        else
            begin
                clkfast_reg <= clkfast_reg + 1'b1;
            end
    end
end

end

endmodule
```

Appendix III PCB design

We describe the PCB design in nine parts: the prototype chip, sensor chip, voltage supply, current supply, source follower supply, threshold voltage generation, common-mode voltage generation, buffer stage, FPGA board and DAQ board connector, level shifter.

III.1 The prototype Chip ‘Ring-down chip’

Figure III-1 shows the pin-out of the ring-down chip.

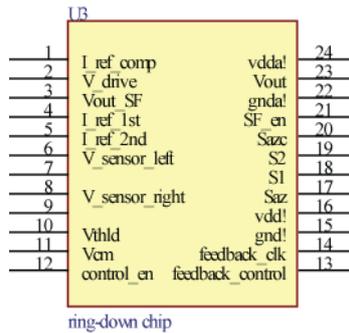


Figure III-1: schematic of the ring-down chip

The ring-down chip is packaged in a 24-pin DIL package, of which two pins remain unconnected. The ‘V_sense_left’ and ‘V_sense_right’ pin of the chip are designed to connect both sides of the resonator. The unconnected pins have been placed on both sides of V_sensor_right (the right side of the resonator). On the PCB board, these two pins are connected to ground to reduce interference. Table III-1 describes the function of each pin.

| Pin number | Name | description |
|------------|--|---|
| 1 | I_ref_comp | DC current supply of the comparator |
| 2 | V_drive | Excitation source |
| 3 | Vout_SF | The level shifted output signal of the I-V converter |
| 4 | I_ref_1st | DC current supply for the first stage of the I-V converter |
| 5 | I_ref_2nd | DC current supply for the second stage of the I-V converter |
| 6 | V_sensor_left | Connect the resonator to the excitation source |
| 8 | V_sensor_right | Connect the resonator to the I-V converter |
| 10 | Vthld | Threshold voltage (programmable) |
| 11 | Vcm | Common-mode voltage (tunable) |
| 12,13,14 | control_en, feedback_clk, feedback_control | Control signals to select the feedback resistors and capacitors |
| 15,16 | vdd!, gnd! | 3.3V supply and ground for the analog circuit |

| | | |
|-------------|----------------|--|
| 17,18,19,20 | Saz,S1,S2,Sazc | Control signals for switch S1, S2, S _{AZ} , S _{AZR} , S _{AZC} , S _{AZCR} |
| 21 | SF_en | Control signal to select the source follower |
| 22,24 | vdda!,gnda! | 3.3V supply and ground for the inverter bank |
| 23 | Vout | The output signal of the comparator |

Table III-1: Pin description

III.2 Sensor chip

The resonator chips, which contain several resonators, are bonded onto a custom-designed PCB adapter, which plugs into a DIL socket on the test PCB. The layout of this adapter is shown in Figure III-2.

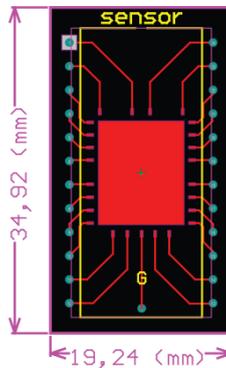


Figure III-2: layout of the adapter

Several of the available resonators are bonded, each to two adjacent pins, for instance, pin1 and pin2 are connected with the left and right side of a resonator, respectively. In the meantime, on the main PCB board, there are two connections sensor_left and sensor_right (Figure III-3) connected to the V_sensor_left and V_sensor_right pins of the readout chip. With this arrangement, different resonators can be selected by moving the position of the adapter in the socket. In addition to the holes for connection, we put four extra holes on the main PCB board for mechanical stability of the adapter.

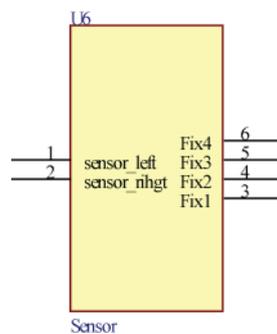


Figure III-3: schematic for the adapter

III.3 Voltage supply circuit

The voltage supply circuit generates two voltage levels: 3.3V and 5V. The ring-down chip is operated at a 3.3V supply voltage, while 5V provides the supply voltage for the other components on the PCB board. We use two voltage regulators to generate these two voltage levels, as shown in Figure III-4.

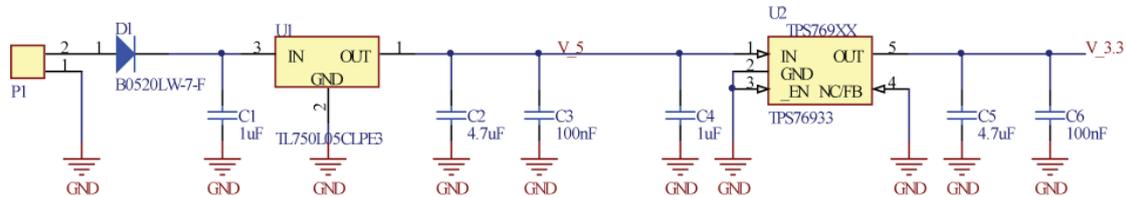


Figure III-4: schematic of supply voltage

The screw termination P1 is connected with external power supply (+7V and 0V) to provide positive supply and ground. The diode is used here to make sure the current flow in the correct direction for PCB protection purpose. To generate the 5V supply voltage, a TL750L regulator is utilized. A 1µF input bypass capacitor, connected between IN and GND and located close to the regulator, is added to improve transient response and noise rejection. Also, two output bypass capacitors with the value of 4.7µF and 100nF are used between OUT and GND to decouple both low frequency and high frequency AC signal from the power supply. In the meantime, regular TPS76933 is applied to generate 3.3V supply voltage. For the same reason, C4, C5 and C6 are used.

III.4 Current supply circuit

Three current supplies are implemented to provide the current for the first and the second stage of the I-V converter and the comparator. The circuit is depicted in Figure III-5.

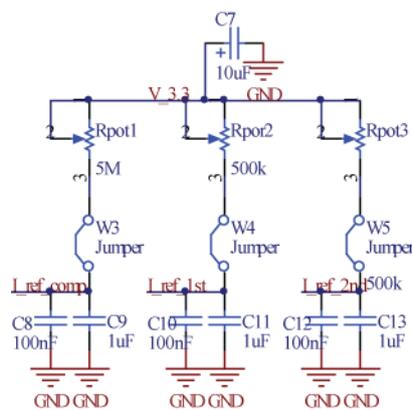


Figure III-5: current supply circuit

To generate a 10µA DC current, a 3.3V DC supply voltage is applied across a 330kΩ resistance. In order to tune the current during the measurement, a 500kΩ potentiometer is chosen for the resistor. As a consequence, two 500kΩ potentiometers are used for generating two DC current

supply of the I-V converter while a 5MΩ potentiometer is used for generating the DC current for the comparator. Furthermore, a 10uF bypass capacitor is added at 3.3V voltage port to filter the signal. And C8~C13 are implemented for decoupling. To detect the current, three jumpers are applied.

III.5 Source follower supply

In order to read the ring-down signal at the output of the I-V converter, a source follower is designed. The bias-current source for this source follower is implemented as Figure III-6.

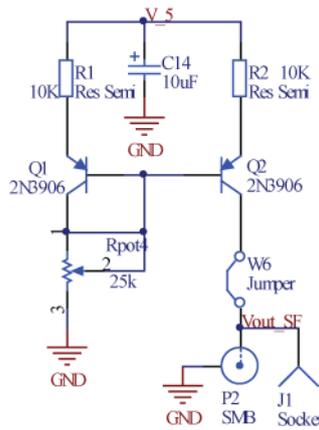


Figure III-6: source follower supply circuit

A PNP current mirror is used to implement the circuit. 5V supply with a decoupling capacitor C14 is applied to obtain sufficient output swing for the ring-down signal. Since the minimum current needed is around 120μA, we choose 10kΩ resistor together with a 25kΩ potentiometer to give a flexible current. We assume the current is 120μA. With a 5V supply voltage, the voltage across the potentiometer is about:

$$V = 5V - 10k\Omega \times 120\mu A - 0.7V = 3.1V$$

So the potentiometer should be around 25kΩ to offer a minimum current of 120μA. The most commonly used component '2N3906' for both PNP transistors is chosen. A jumper is also used for measuring the current. A SMB connector is implemented to see the output of the source follower by oscilloscope. A socket is also applied for flexibility.

III.6 Threshold voltage generation

As described before, to improve the flexibility, a multiplexer is applied to select the different threshold voltages to measure both the resonance frequency and quality factor. The circuit for threshold-level generation is shown in Figure III-7. Our choice for the multiplexer is the most commonly used chip 'HEF4052BT'. 'A1' and 'A2' are control signals, which generated by the FPGA development board. Four threshold voltages are implemented with potentiometer to make them

tunable. Also some decoupling capacitors are used at the input and the output.

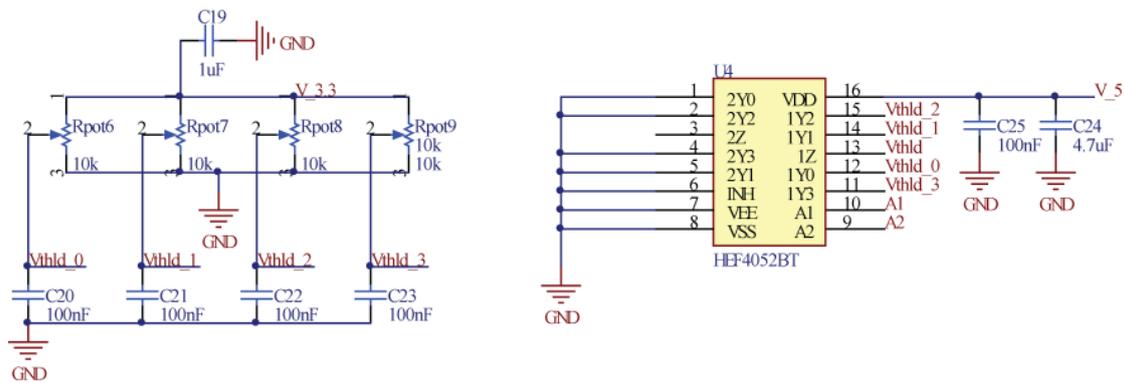


Figure III-7 circuit for threshold voltage generation

III.7 Common-mode voltage generation

During the corner analysis, we find that the common-mode voltage should be tunable in case the technology is not the typical one. So we implement the circuit for the common-mode voltage generation as follows. A potentiometer with a value of 2k is used as a voltage divider. Decoupling capacitors are also applied here.

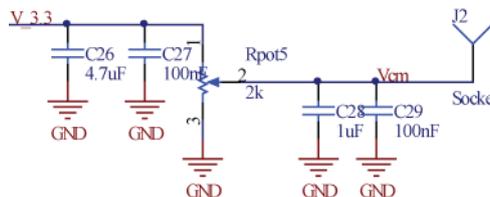


Figure III-8: circuit for common-mode voltage generation

III.8 Buffer stage

A buffer stage is used between the digital signal at the output of the ring-down chip and signal given into the FPGA for counting. We choose most commonly used chip 'SN74LVC1G17' to provide buffers with Schmitt-trigger action and transform the slowly changing signals into sharply defined signals. Two decoupling capacitors are added to the 3.3V supply voltage.

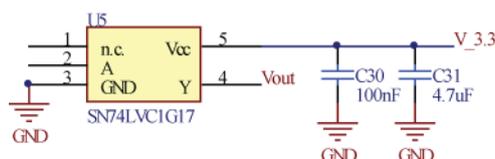


Figure III-9: Buffer stage

III.9 FPGA board connector

The FPGA development board provides two, 40-pin expansion headers. For convenience, we use the same 40-pin header on the PCB board (Figure III-10). All the signals generated by FPGA board have 3.3V DC level, which can be directly applied to the ‘ring-down’ chip.

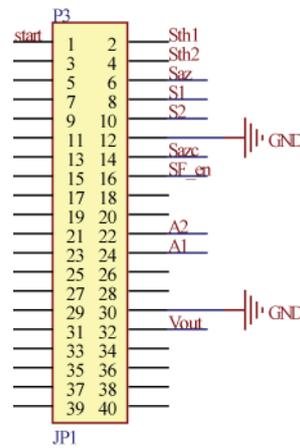


Figure III-10: schematic of the FPGA board connector

III.10 DAQ board connector and level shifter

Screw terminations P4 and P6 are used on the PCB board to connect the DAC with the PCB. All the signals generated by DAQ are 5V DC level, which cannot be directly applied to the ‘ring-down’ chip and FPGA. In order to solve this problem, two MAX3392 level shifters are applied between DAC and FPGA and prototype chip to shift 5V signals to 3.3V signals. A SMB connector is applied to provide the excitation signal from the function generator to the PCB board.

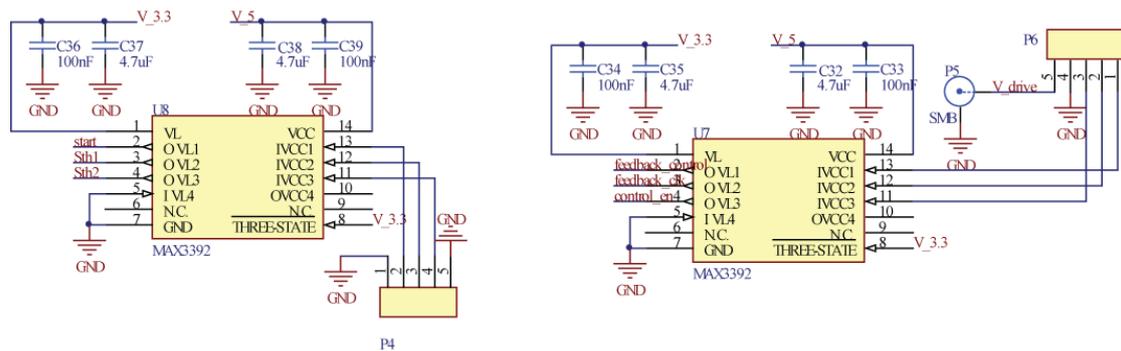


Figure III-11: schematic of level shifter and DAC connector

III.11 Whole system

Figure III-12 demonstrates the complete schematic of the PCB design.

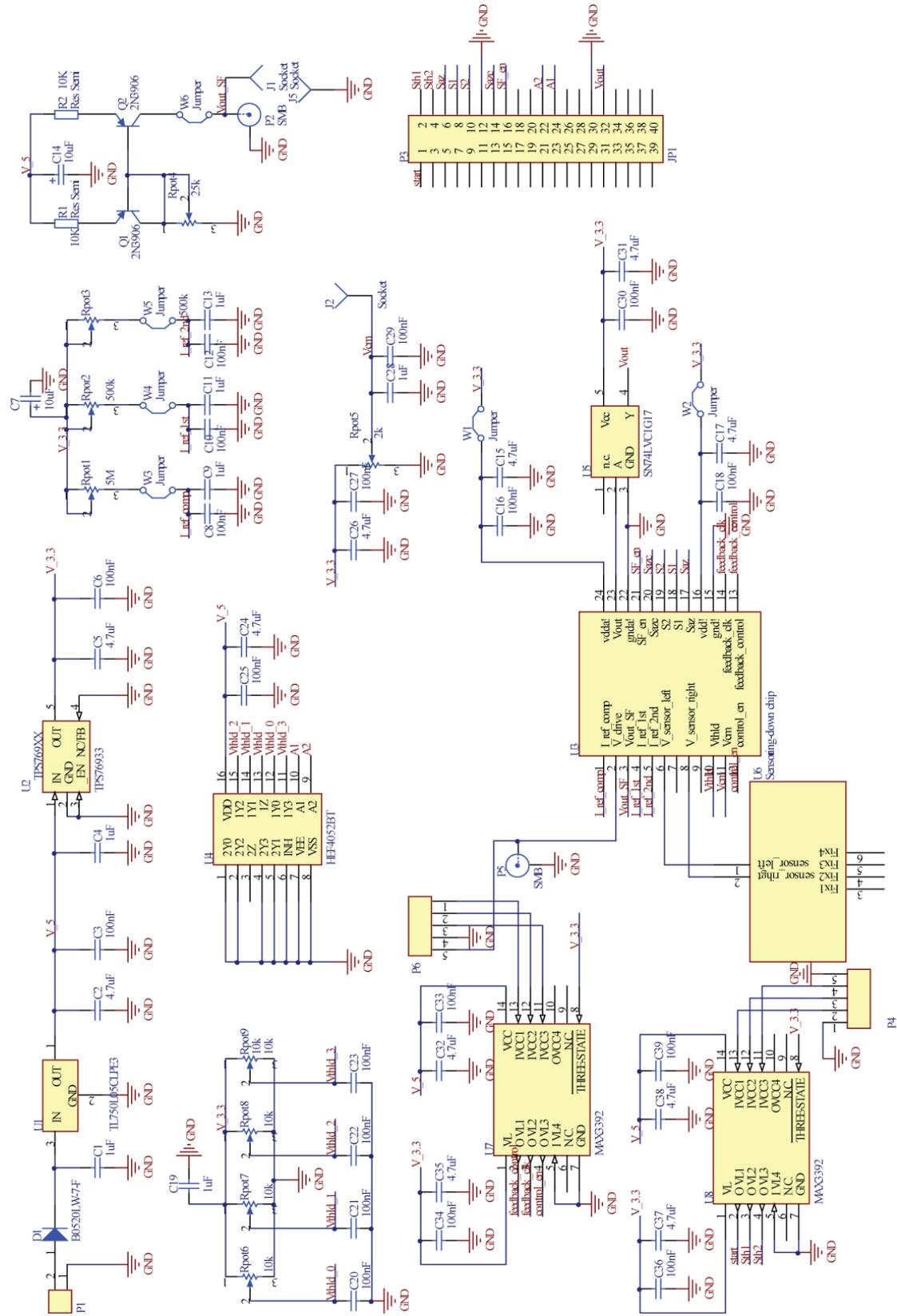


Figure III-12: the complete PCB schematic

Figure III-13 demonstrates the complete layout of the PCB design.

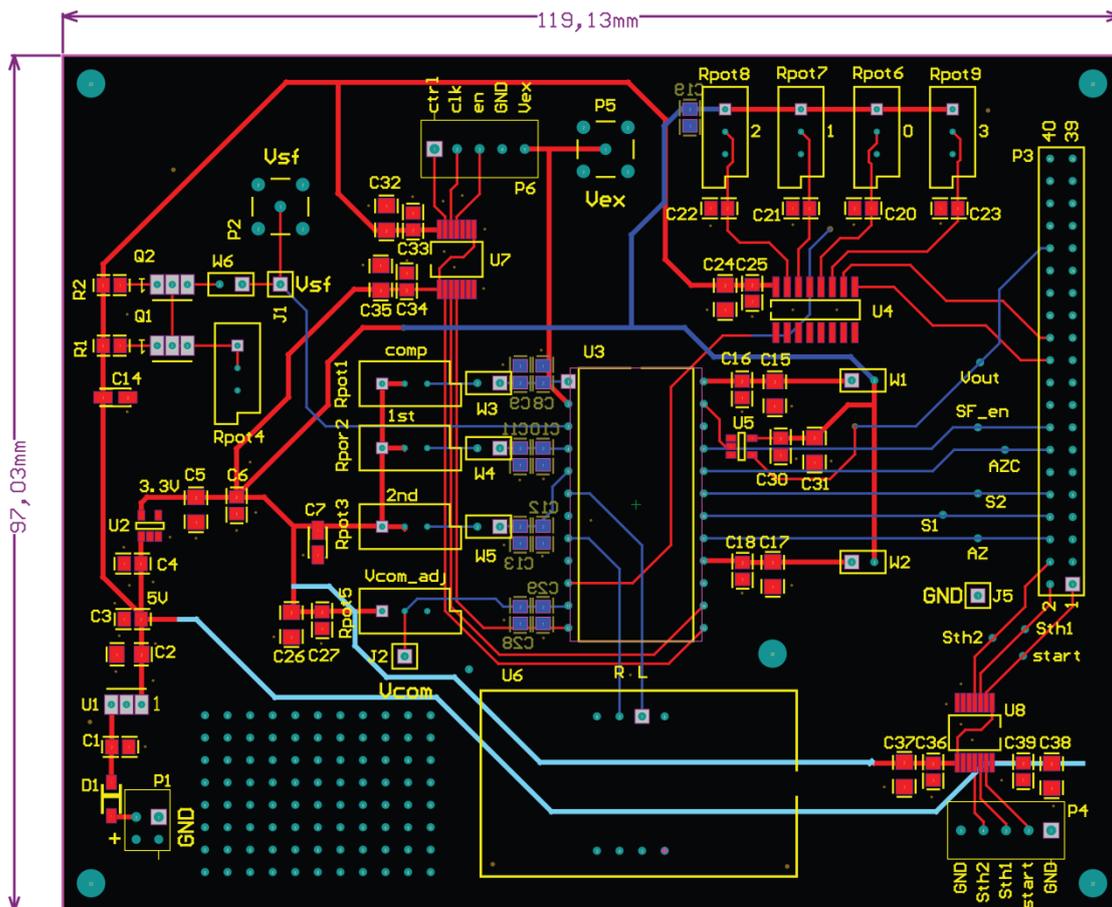


Figure III-13: the complete PCB layout