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Metallic Nanoparticle Sintering for High Density Interconnect

Metallic Nanoparticle Sintering for High Density Interconnect

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology
by the authority of the Rector Magnificus,
prof. dr. ir. T.H.J.J. van der Hagen,
chair of the Board for Doctorates
to be defended publicly on
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Keywords: metallic nanoparticles, high-density interconnect, lithographic stencil printing, microbump, Cu-Cu direct bonding, nanoparticles sintering

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To my parents and grandparents

Xinrui

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Summary

As integrated circuits (ICs) become increasingly miniaturized, traditional solder-based interconnects face challenges related to their thermal and mechanical performance, limiting their reliability in high-density applications. This thesis addresses the growing demands of the microelectronics industry, particularly in advanced semiconductor packaging technologies, by focusing on the development of innovative interconnect methods using metallic nanoparticles, specifically copper (Cu). The research aims to overcome these limitations by utilizing copper nanoparticle (CuNP) paste to achieve direct copper-to-copper (Cu-to-Cu) bonding through nanoparticle sintering. This technique is essential for enabling next-generation 2.5D and 3D IC architectures, which require dense interconnects for improved performance.

A significant contribution of this thesis is the development and optimization of the Lithographic Stencil Printing (LSP) technique, which enables the precise patterning and transfer of Cu nanoparticles (CuNPs). The LSP method integrates traditional stencil printing with photolithography to create high-resolution patterns using copper nanoparticles, addressing the need for fine-pitch interconnects in semiconductor packaging. This technique aims to replace solder-based interconnects, which cannot meet strict requirements because of their low melting points and the possibility of electromigration (EM) issues. The research demonstrates the use of CuNP sintering to produce reliable, high-density interconnects for advanced packaging applications.

The experimental section of the thesis delves deeply into optimizing nanoparticle patterning techniques. Various experiments were conducted to investigate the influence of lift-off processes and printing parameters on the quality of CuNP patterns. A key focus of the research was to improve the uniformity and structural integrity of the nanoparticle patterns pre- and post-sintering, as well as to enhance the mechanical and electrical performance of the resulting

interconnects. The research highlights the importance of precise control over the lift-off process through systematic experimentation, demonstrating how temperature, agitation, and chemical treatments affect the successful removal of photoresist, thereby improving the patterning of CuNPs.

In addition to the LSP technique, this thesis explores innovative nanoparticle patterning methods, including the use of Cu nanoparticles for sintering in flip-chip interconnects and the integration of photopatternable underfill films. The research also investigates new methods for generating nanoparticles through spark ablation to pattern various metal nanoparticles, demonstrating the flexibility of the LSP method in transferring nanoparticle patterns.

Further experimental work was conducted to characterize the mechanical and electrical properties of the sintered Cu bumps. Nanoindentation testing was employed to assess the mechanical strength of the bumps, while conductivity measurements were used to evaluate their electrical performance. The results established a correlation between the properties of the sintered Cu bumps and the sintering parameters, providing a benchmark for future experimental conditions.

The thesis also presents the development and testing of 20 μm pitch Cu-to-Cu direct bonding using nanoparticle sintering technology. Detailed experiments were conducted to fabricate fine-pitch interconnects and evaluate their mechanical reliability through shear strength tests. The successful implementation of fine-pitch Cu-to-Cu bonding demonstrated its suitability for high-density IC integration, addressing the challenges of miniaturization and performance in advanced electronics.

In summary, this research provides a comprehensive study of metallic nanoparticle sintering as a method for achieving high-density interconnects in advanced IC applications. The work successfully demonstrates the feasibility and advantages of using CuNPs for Cu-to-Cu bonding, offering a cost-effective and reliable alternative to traditional solder-based interconnects. The findings of this thesis not only present a proof of concept but also provide a pathway toward overcoming the limitations of Moore's Law and enabling the continued miniaturization and performance enhancement of electronic devices. Future work is recommended to

further refine CuNP sintering techniques, focusing on challenges related to mass production, long-term reliability, and potential applications in emerging electronic devices such as 5G communication systems, artificial intelligence (AI), and high-performance computing.

Samenvatting

Naarmate geïntegreerde schakelingen (IC's) steeds verder worden geminiaturiseerd, krijgen traditionele op soldeer gebaseerde interconnecties te maken met uitdagingen op het gebied van thermische en mechanische prestaties, wat hun betrouwbaarheid in hoogdichtheidstoepassingen beperkt. Dit proefschrift adresseert de groeiende eisen van de micro-elektronica-industrie, met name in geavanceerde halfgeleiderverpakings-technologieën, door zich te richten op de ontwikkeling van innovatieve interconnectiemethoden met behulp van metallische nanodeeltjes, specifiek koper (Cu). Het onderzoek heeft als doel deze beperkingen te overwinnen door gebruik te maken van een koper-nanodeeltjespasta om directe koper-tot-koper (Cu-tot-Cu) verbindingen te realiseren via nanodeeltjes sintering. Deze techniek is essentieel voor het mogelijk maken van de volgende generatie 2.5D- en 3D-IC-architecturen die dichte interconnecties vereisen voor verbeterde prestaties.

Een belangrijke bijdrage van dit proefschrift is de ontwikkeling en optimalisatie van de Lithografisch Stencilprinten (LSP)-techniek, die het mogelijk maakt om nauwkeurige patronen te creëren en koper-nanodeeltjes (CuNPs) over te dragen. De LSP-methode combineert traditionele stencilprinting met fotolithografie om hoogresolutiepatronen te maken met koper-nanodeeltjes, waardoor wordt voldaan aan de behoefte aan fijnmazige interconnecties in halfgeleiderverpakkingen. Deze techniek is bedoeld om op soldeer gebaseerde interconnecties te vervangen, die niet aan strenge eisen kunnen voldoen vanwege hun lage smeltpunten en gevoeligheid voor elektromigratieproblemen. Het onderzoek toont het gebruik van CuNP-sintering aan voor de productie van betrouwbare, hoge dichtheid interconnecties voor geavanceerde verpakkingapplicaties.

Het experimentele deel van het proefschrift gaat dieper in op het optimaliseren van nanodeeltjespatroneringstechnieken. Er zijn verschillende experimenten uitgevoerd om de invloed van lift-off-processen en printparameters op de kwaliteit van

CuNPs-patronen te onderzoeken. Een belangrijk aandachtspunt van het onderzoek was het verbeteren van de uniformiteit en structurele integriteit van de nanodeeltjespatronen, zowel vóór als na het sinteren, evenals het verbeteren van de mechanische en elektrische prestaties van de resulterende interconnecties. Het onderzoek benadrukt het belang van nauwkeurige controle over het lift-off-proces door middel van systematische experimenten. Het laat zien hoe factoren zoals temperatuur, agitatie en chemische behandelingen de succesvolle verwijdering van de fotoresist beïnvloeden, waardoor de patronering van CuNPs wordt verbeterd.

Naast de LSP-techniek onderzoekt dit proefschrift innovatieve methoden voor het maken van patronen van nanodeeltjes, waaronder het gebruik van koper-nanodeeltjes voor sinteren in flip-chip-interconnecties en de integratie van fotopatteerbare onderlaagfilms. Het onderzoek bestudeert ook nieuwe methoden voor het genereren van nanodeeltjes via vonkablatie om patronen van nanodeeltjes te maken, wat de flexibiliteit van de LSP-methode aantoonst bij het overdragen van nanodeeltjespatronen.

Verdere experimentele werkzaamheden zijn uitgevoerd om de mechanische en elektrische eigenschappen van de gesinterde koperbumps te karakteriseren. Nano-indentatietests werden gebruikt om de mechanische sterkte van de bumps te beoordelen, terwijl geleidingsmetingen werden gebruikt om hun elektrische prestaties te evalueren. De resultaten toonden een verband aan tussen de eigenschappen van de gesinterde koperbumps en de sinterparameters, wat een benchmark biedt voor toekomstige experimenten.

Het proefschrift presenteert ook de ontwikkeling en testen van 20 μm pitch Cu-Cu-directe verbindingen met behulp van nanodeeltjessintertechnologie. Gedetailleerde experimenten werden uitgevoerd om fijnmazige interconnecties te fabriceren en hun mechanische betrouwbaarheid te evalueren via afschuifsterktetests. De succesvolle implementatie van fijnmazige Cu-Cu-verbindingen toonde de geschiktheid aan voor hoge dichtheid IC-integratie, waardoor de uitdagingen van miniaturisatie en prestaties in geavanceerde elektronica worden aangepakt.

Samenvattend biedt dit onderzoek een uitgebreide studie van het sinteren van metallische nanodeeltjes als methode voor het bereiken

van hoogdichte interconnecties in geavanceerde IC-toepassingen. Het werk toont met succes de haalbaarheid en voordelen aan van het gebruik van CuNPs voor Cu-Cu-verbindingen, wat een kosteneffectief en betrouwbaar alternatief biedt voor traditionele op soldeer gebaseerde interconnecties. De bevindingen van dit proefschrift presenteren niet alleen een bewijs van het concept, maar bieden ook een weg naar het overkomen van de beperkingen van de wet van Moore, waardoor verdere miniaturisatie en prestatieverbetering van elektronische apparaten mogelijk worden. Voor toekomstig werk wordt aanbevolen om de CuNPs-sinter technieken verder te verfijnen, met aandacht voor uitdagingen op het gebied van massaproductie, het waarborgen van langdurige betrouwbaarheid en het verkennen van mogelijke toepassingen in opkomende elektronische apparaten zoals 5G-communicatiesystemen, kunstmatige intelligentie (AI) en high-performance computing.

Acronyms

Acronyms and Abbreviations

2.5D IC Two-and-a-Half-Dimensional Integrated Circuit

3D IC Three-Dimensional Integrated Circuit

AI Artificial Intelligence

Au Gold

B-Cu Bulk Copper

BEOL Back End of Line

C2C Chip-to-Chip

C2S Chip-to-Substrate

C2W Chip-to-Wafer

C2 chip-connection

C4 Controlled Collapse Chip Connection

CBKS Cross-Bridge Kelvin Structure

CMP Chemical Mechanical Polishing

CSM Continuous Stiffness Measurement

CIS CMOS image sensors

CTE Coefficient of Thermal Expansion

Cu Copper

Cu-Cu Copper-to-Copper

CuNP Copper Nanoparticle

CuNP paste Copper nanopaste

CuNPs Copper Nanoparticles

Cu-Sn Copper-Tin

DBI Direct Bond Interconnect

DI Deionized (Water)

D2D Die-to-Die

D2W Die-to-Wafer

DoE Design of Experiment

EM Electromigration

FCCSP Flip Chip Chip Scale Package

FCBGA Flip Chip Ball Grid Array

FCR Flip-chip Reflow

FIB Focused Ion Beam

FIB/SEM Focused Ion Beam/Scanning Electron Microscope

HI Heterogeneous Integration

HPC High-Performance Computing

IC Integrated Circuit

ICs Integrated Circuits

IMS Injection Molded Solder

IoT Internet of Things

IR Infrared

LPCVD Low-Pressure Chemical Vapor Deposition

LSP	Lithographic Stencil Printing
MEMS	Micro-Electro-Mechanical Systems
MUF	Molded Underfill
N-Cu	Nanocopper
NMP	N-Methyl-2-pyrrolidone
NP	Nanoparticle
NPs	Nanoparticles
PCB	Printed Circuit Board
RDL	Redistribution Layer
SAB	Surface-Activated Bonding
SAM	Self-Assembled Monolayer
SEM	Scanning Electron Microscope
SiNx	Silicon Nitride
SiOx	Silicon Oxide
SiP	System in Package
SoIC	System on Integrated Chips
TaN	Tantalum Nitride
TCB	Thermal Compression Bonding
Ti	Titanium
TiN	Titanium Nitride
TiO₂	Titanium Dioxide
TIM	Thermal Interface Materials
TSV	Through-Silicon Vias

UBM Under Bump Metallization

VDP Van Der Pauw

W2W Wafer-to-Wafer

μbump Microbump

1

Introduction

1.1. Background

Microelectronics packaging involves encasing and protecting semiconductor devices, such as ICs and power electronics, while providing electrical connections to external circuits. It serves key functions, including shielding the device from environmental damage, offering mechanical support, ensuring signal integrity, and managing heat dissipation [1]. Recently, microelectronics packaging has encompassed various technologies aimed at integrating dies or chips into electronic systems [2]. Moreover, microelectronic packaging can combine chips from different manufacturing technologies into a single package, such as photonic and mechanical components, to enhance the versatility and functionality of electronic systems [3], [4]. Progress in this field, often referred to as advanced packaging, is crucial for the continued development of smaller, faster, and more powerful electronic devices [5]–[8].

With the continuous advancement of microelectronic manufacturing processes, the size of transistors has been miniaturized, driving further research into interconnects and integration. Traditional Moore's Law is no longer fully compatible with the growing needs of the microelectronics industry [9]. As a result, the 'More than Moore' concept has emerged [10], where high-end system-in-package (SiP) and heterogeneous integration (HI) are global solutions for "More than Moore" applications [11], [12]. Furthermore, advanced integration technologies such as chip-to-chip (C2C) and chip-to-wafer (C2W) are being adopted to miniaturize multi-functional integrated applications [13], [14]. The rapid innovation in 2.5D and 3D integration technologies is driving the development of novel materials and processes [15].

Flip-chip and wire bonding are two commonly used interconnection technologies in SiP and HI applications [16]. Flip-chip packaging technology establishes interconnections by flipping the chip so that the input/output (I/O) on the active side faces the substrate, creating a chip-to-substrate (C2S) bond [17]. An underfill material is then used to secure the chip to the substrate, ensuring reliable interconnections (Fig. 1.1a). Flip-chip bonding technology for C2C and C2W is widely utilized as the basic building block of 2D, 2.5D, and 3D stacking architectures for ICs. This approach aims to achieve high-density integration, signal integrity,

and environmental protection, enabling the creation of compact, advanced microelectronic systems [18].

Wire bonding, the oldest chip-to-package interconnection technology, connects the die to the substrate using thin wires for low power and thick wires for high power. It provides a reliable and straightforward connection, as shown in Fig. 1.1b. First, the chip is attached to the substrate using a die-attach material, which can be electrically conductive or nonconductive. Next, wires made of Al, Au, or Cu are bonded to create electrical connections from the chip to the substrate. When combined with the die-attach process, wire bonding is widely employed in power electronics packaging [19]–[22].

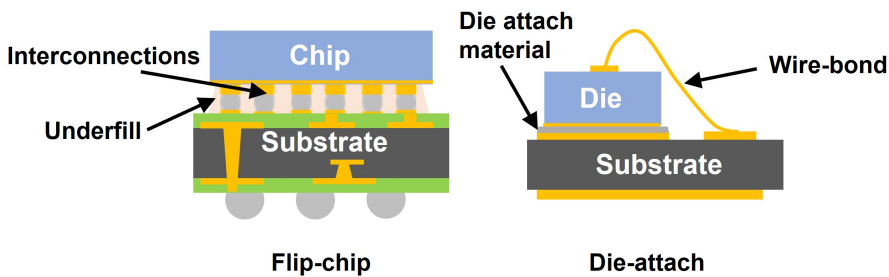


Figure 1.1: Schematics of flip-chip packaging (left) and power device packaging (right).

1.2. Advanced Packaging for Semiconductor Manufacturing

The semiconductor industry is driving advancements across five major application domains [23]: (1) mobile devices such as smartphones and computers, (2) high-performance computing (HPC), (3) electric vehicles, (4) the Internet of Things (IoT) with AI integration, and (5) big data and instant data. Advanced packaging technologies are continuously evolving to support and accelerate progress in these areas, moving from 2D to 3D integration. To enhance chip integration and overcome the limitations of Moore's Law, chiplet design and HI packaging offer alternative solutions, particularly for advanced nodes [24].

This broadens the application spectrum of flip-chip technology,

which utilizes bumpless 3D integration instead of conventional bump processes to improve the performance of high-density ICs, will be introduced and discussed in detail. In addition, techniques such as flip-chip mass reflow, thermo-compression bonding (TCB), and bumpless hybrid bonding play critical roles in the current landscape of advanced packaging and its applications. This section discusses the development of various bonding technologies critical for achieving high-density integration, focusing on bump technologies in 3D packaging, which are essential for semiconductor manufacturing.

1.2.1. Interconnects for 2D to 3D architectures

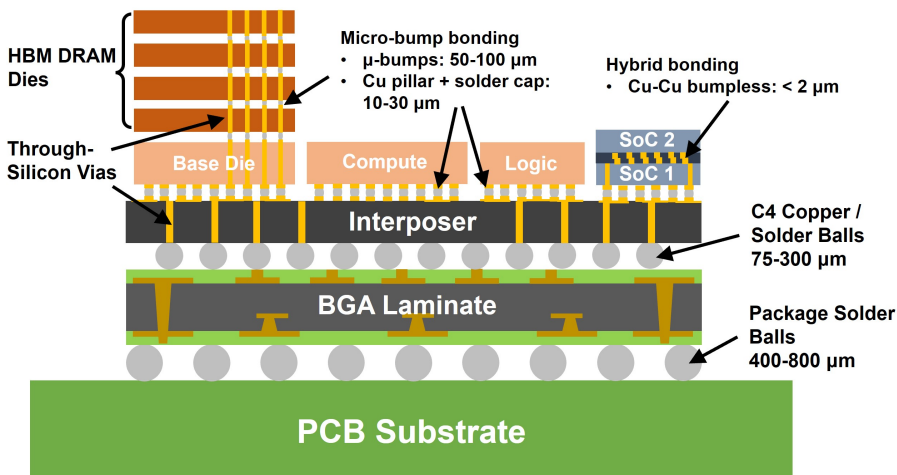


Figure 1.2: An overview of bonding technologies employed in 3D interconnections for high-density IC integration [25]–[27]

Advanced semiconductor technologies have led to significant advancements in interconnection technologies, which are crucial for 2D, 2.5D, and 3D IC architectures. In order to achieve higher density and improved electrical performance in 2D to 3D interconnects, it is possible to stack multiple dies vertically instead of horizontally, like in traditional wire bonding designs. The approach to 2D integration involves arranging circuits on a single plane, resulting in longer interconnects and increased signal delay. In contrast, 2.5D and 3D interconnection involves stacking chiplets vertically and using

through-silicon vias (TSVs) to connect the stacked dies [28], [29]. The schematic of the 3D interconnection architecture is shown in Fig. 1.2. 3D interconnects are essential in modern high-performance computing (HPC) and data centers, enabling the integration of multiple dies into a single package [27], [30], [31]. This method decreases the overall I/O footprint and shortens signal paths, enhancing performance and energy efficiency. However, it also presents challenges such as thermal management and increased manufacturing complexity [32].

Flip chip technology and TSVs are essential in advancing 3D integration and enhancing performance. Initially, flip-chip technology used solder balls as interconnects, connecting the chip directly to the packaging substrate. Microbump (μ bump) technology emerged as advancements progressed, with finer solder bumps interconnecting with smaller Cu bumps, resulting in improved flip chip designs that are more compact and efficient. Bumpless technologies like hybrid bonding were introduced to improve performance and reliability further. These advanced methods eliminate the need for solder, enabling direct Cu-to-Cu bonding or all-Cu interconnects, which offer superior electrical and thermal conductivity. The transition from conventional solder interconnects to Cu bump interconnects, and eventually all-Cu interconnects, helps maintain miniaturization and improved performance in various applications.

1.2.2. Flip-chip development

Flip-chip technology, introduced by IBM in the 1960s [33], [34], aligns the contact pads on the device with corresponding pads on the substrate, using solder bumps, Cu pillars, and gold studs for electrical interconnections [27]. The evolution of flip-chip technology can be divided into three generations [35]: Controlled Collapse Chip Connection (C4) bumps, Cu pillar bumps, and 3DIC assembly. Fig. 1.3 illustrates the scope of bumping technology for flip-chip bonding.

The first generation, C4 bumps, typically features bump pitches exceeding 130 μm . These bumps can be created by melting Sn-based solders using a standard reflow process, where the molten solder displays self-alignment properties due to surface tension, ensuring precise alignment during bonding. The solder is then bonded to

ceramic or organic substrates, as shown in Fig. 1.2. The C4 joint technology produces two traditional package types: Flip Chip Ball Grid Array (FCBGA) and Flip Chip Chip Scale Package (FCCSP).

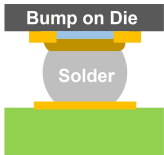
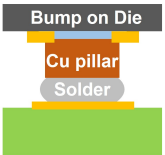
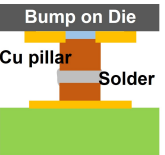
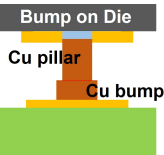
Bonding Method	C4 Flip Chip	C2 Flip Chip	Thermal Compression (Local Reflow) Flip Chip	Thermal Compression Flip Chip
Structure				
Major Bump Pitch Range	> 130 μm	140 μm ~ 60 μm	80 μm ~ 20 μm	< 30 μm
Bonding Method	Conventional Reflow	Reflow with Cu pillar	Thermal Compression with Cu pillar	Cu Thermal Compression
Bump Metallurgy	Solder (SnAg or SnAgCu)	Cu + Solder (SnAg or Sn)	Cu + Solder (SnAg or Sn) Cap	Cu

Figure 1.3: Development of flip chip interconnects [36]

Table 1.1: C4 bumps vs. C2 bumps [27], [37]

Structure	Thermal conductivity (W/m · K)	Electrical resistivity $\mu\Omega \cdot \text{m}$	Bump pitch	Self-alignment
Cu	400	0.0172	-	-
C4 Bump (solder)	55-60	0.12-0.14	$\geq 50\mu\text{m}$	Very good
C2 Bump (Cu Pillar + Solder Cap)	300 (Effective)	0.025 (Effective)	$< 50\mu\text{m}$	Very poor

The second generation, known as Cu pillar bumps or microbumps (μ bumps), primarily provides a reduced bump pitch ranging from 20 to 140 μm . Copper pillar bumps can be bonded using two main techniques: flip-chip reflow (FCR) and TCB [38]. FCR involves aligning the top and bottom chips and placing them in a reflow furnace, where the solder caps melt to create electrical connections.

TCB uses heat and pressure directly to bond the chips, making it ideal for finer-pitch applications and providing better bonding control. C2 (chip-connection) bump technology utilizes solder-capped Cu pillar bumps through a solder reflow process to connect fine-pitch flip-chips economically and cost-effectively [36]. Due to the decrease in solder volume compared to C4 bumps, C2 bumps technology cannot self-align, so we refer to them as chip-connection bumps [39]. C2 bumps are capable of interconnections of C2C and C2W with smaller pitch dimensions and provide improved thermal and electrical performance compared to the C4 bumps, as shown in Table 1.1 [27], [37]. To achieve more precise chip-to-chip interconnection, a finer-pitch copper pillar with a solder cap was developed using TCB technology, enabling ultra-fine pitches ranging from 20 to 80 μm for C2C integration. This method requires improved alignment accuracy, which can enhance the reliability and performance of high-density 3D ICs. μ bumps are becoming more popular in flip-chip packaging, making it possible to create fine-pitch flip-chip packages, SiP, 2.5D and 3D packages to enable advanced heterogeneous integration [39].

The latest generation of 3DIC assembly has reduced bump pitch to below 30 μm . 3D integration is becoming more popular as devices evolve and expand in applications due to its superior bandwidth, power efficiency, performance, and compact size compared to traditional packaging. The key to achieving 3D technology is having high-density interconnects and a reliable, high-throughput stacking and bonding process. Traditional solder bump technology is not feasible for high current density applications due to its low melting temperatures, poor high-temperature resistance, and inferior thermal conductivity [40]. These limitations lead to issues such as joule heating, which undermines the reliability of solder joints. Furthermore, the resistance to EM of Cu-Cu bumps is significantly higher than that of solder joint interconnects [41]–[43]. Consequently, Cu-Cu direct bonding has emerged as a superior alternative, offering enhanced performance and reliability [44].

1.2.3. Cu-to-Cu direct bonding

The development of direct Cu-Cu direct bonding, which can be formed with both Cu bumps and Cu nanopaste (CuNP paste), is

aimed at solving issues related to pitch, EM, and reliability [45]. Cu-Cu bonding can be categorized into two primary types: TCB and low-temperature direct bond interconnect.

Cu-Cu TCB

Direct Cu-Cu bonding is achieved through atomic interdiffusion between two Cu bumps interfaces. However, this process is challenging to accomplish at room temperature and atmospheric pressure due to the slow diffusion rate of Cu at low temperatures. Therefore, Cu-Cu bonding usually requires high temperature and high pressure. This process is called TCB, typically performed at 300-400 °C in a vacuum or protective gas environment [46]. After Cu-Cu TCB, the integration process is completed by introducing underfill material into the gap as depicted in Fig. 1.4. The key factors affecting Cu-Cu bonding are bonding temperature, pressure, and time. Higher temperatures or extended annealing times can improve bonding quality by enhancing Cu diffusion and grain growth [46]–[48]. However, high processing temperatures can lead to significant thermal expansion and mechanical stress, potentially leading to reliability issues and even damaging components sensitive to thermal and mechanical loads.

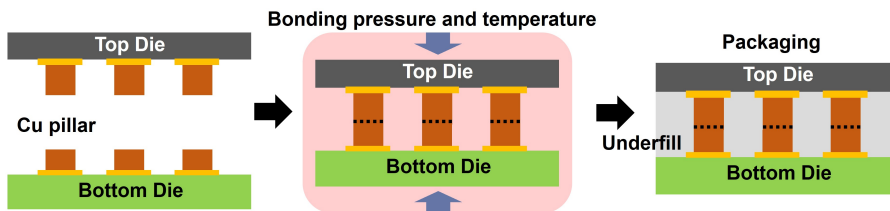


Figure 1.4: Schematic process flow of Cu-Cu TCB

At the same time, Cu quickly reacts with oxygen, creating an oxide layer that prevents atomic diffusion. Therefore, removing the copper oxide and activating the Cu surface is essential. To address this issue, bonding pressure is applied to disrupt the oxide layer [44]. In addition, compression pressure is mainly influenced by surface topography and roughness. The pressure ranges from 100 to 150 MPa for electroplated Cu pads and pillars. In contrast, for smooth Cu surfaces, the pressure is less than 2.5 MPa [49]. Consequently, the TCB

process requires high surface flatness, typically achieved through chemical mechanical polishing (CMP). By using this technique, surface roughness can be reduced to a few nanometers, ensuring optimal contact between the two surfaces. Moreover, careful pressure control is necessary to prevent mechanical damage to the dies during the bonding process.

Cu-Cu hybrid bonding

Hybrid bonding, which combines dielectric materials, such as SiO_2 , SiN_x and SiCN , and metal bonding to create interconnections, is a significant advancement in 3D packaging technology and is also referred to as bumpless bonding [50]–[52]. This hybrid bonding process is called low-temperature direct bond interconnect (DBI) in the industry for its ability to activate at room temperature and then anneal at temperatures ranging from 150 to 300 °C [53]. This method has a significant advantage in decreasing the thermal stress on devices compared to the high-temperature requirements of TCB. The historical development of DBI technology began with its commercialization by Ziptronix [54]. A significant breakthrough occurred in 2016 when Sony pioneered the use of wafer-level hybrid bonding in CMOS image sensors (CIS), enhancing performance by integrating memory with image-sensors logic [55], [56]. In 2020, TSMC introduced a multifunctional integration of stacked multi-layer DRAM and logic devices, announcing the System on Integrated Chips (SoIC) Bumpless Chiplets 3D IC Integration technology [57], [58].

An essential requirement for successful Cu-Cu hybrid bonding is achieving an extremely flat surface through CMP, which reduces surface roughness and creates a slight recess in the metal areas relative to the dielectric surface. This flatness is critical to maximizing contact between the Cu surfaces to ensure a quality bonding. The fabrication of Cu-Cu hybrid bonding typically involves several key steps: surface cleaning, surface activation, and bonding, as shown in Fig. 1.5 [53]. First, surface cleaning is essential to remove contaminants or oxides from the copper surface, as even the smallest particles can disrupt the bonding interface, reducing bond strength and reliability. After cleaning, the dielectric surfaces are activated by plasma treatment to enhance chemical bonds, followed by the actual bonding process. At room temperature, a bond is established between

the dielectric materials of both surfaces and then the temperature is raised to close the dishing gap and create a metal-to-metal bond. This process establishes a direct, low-resistance connection, crucial for 3D integration in advanced electronic devices. After bonding, the wafers are annealed. During this process, the metal expands to fill any gaps because its coefficient of thermal expansion is much higher than that of the dielectric materials. This process enhances mechanical strength and improves the interconnects' overall reliability and electrical performance by promoting further atomic diffusion.

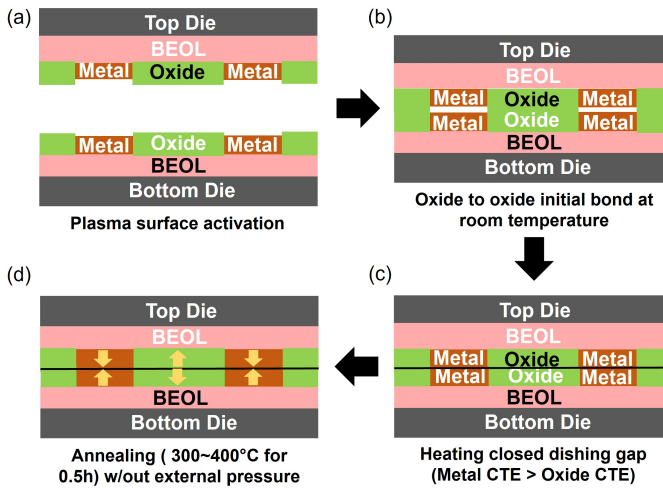


Figure 1.5: Schematic process flow of Cu-Cu hybrid bonding

Cu-Cu hybrid bonding is a promising method for achieving high aspect ratios in fine-pitch interconnections by providing low resistance, high signal integrity, and strong current density capacity. This process is prone to surface roughness and contamination, affecting electrical performance. Efforts to overcome challenges such as surface roughness, contamination, and residual stress require optimizing processes and developing robust technologies to achieve successful applications in 3D packaging.

1.3. Metallic Nanoparticles Sintering Technology in Advanced Packaging

1

1.3.1. Metallic nanoparticles materials

Metallic NPs have become a highly effective alternative material, driving advancements in microelectronics. As microelectronic devices continue to be miniaturized and energy-efficient, metallic NPs are increasingly utilized. Their nanoscale efficiency makes them highly compatible with various applications, such as thermal management in power electronics, printable electronics, high-performance sensors, interconnects in ICs, and energy storage systems [59]–[64]. Typically composed of metals such as Cu, silver (Ag), and gold (Au), these NPs improve the electrical, thermal, and mechanical performance of microelectronic devices and packaging modules, making them crucial components in many electronic applications [60], [61], [65]–[67]. In recent research and applications, metallic NP materials are usually classified into three forms: nanoporous metal materials, metallic NPs ink, and metallic NP paste [59], [62], [66], [68]. Among these, mixed organic materials and solvent additives are incorporated with metallic NPs to formulate conductive inks and pastes, enhancing their transport, storage, and usability [68], [69].

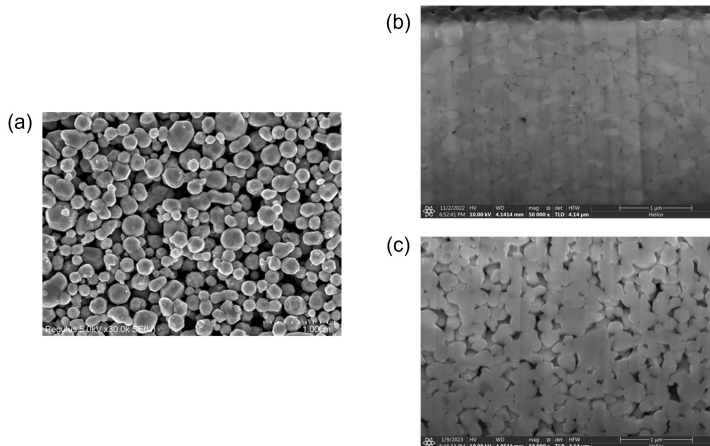


Figure 1.6: (a) CuNPs sintered in (b) low porosity polycrystalline materials and (c) nanoporous materials

Recent research on metallic NPs has focused on optimizing their synthesis and integration into microelectronic systems by refining the NPs' size, shape, and composition to enhance performance. Among these materials, Cu- and Ag NPs stand out as ideal choices for high-performance interconnection applications due to their excellent electrical and thermal conductivities. However, the processing temperatures in semiconductor manufacturing and packaging must remain low, driving increased interest in low-temperature packaging technologies. metallic NPs can be sintered under certain temperatures and pressure to create nanoporous materials or ultra-low porosity polycrystalline materials close to bulk materials, as illustrated in Fig. 1.6 [62], [70]. Their high surface area and nanoscale features enable the sintering temperature to be lower than their bulk melting points. Sintering temperatures can be kept below 300 °C, meeting the requirements for bonding in microelectronic assembly and packaging at relative low temperatures. Studies have shown that as the size of NPs decreases, the sintering temperature is significantly reduced, far below the melting points of Cu and Ag [71]. Nanoporous Au has been investigated for use in wafer-level packaging interconnects, providing a new interconnect technology for future applications that require Au interconnects in chip integration [63], [72], [73].

1.3.2. Potential applications in ICs packaging

One application of metallic NPs in the domain of ICs is in the interconnecting line for redistribution layers (RDLs). RDLs reroute a chip's input/output (I/O) connections to align with the layout of a printed circuit board (PCB) or package. Conductive inks can be utilized in RDLs applied for flexible substrates to provide versatility in design [74]–[76].

Another critical application area is flip-chip bonding, which shortens electrical paths, reduces signal delay, and improves thermal dissipation, making it especially valuable in demanding environments such as data centers, high-performance computing, and telecommunications equipment [77], [78]. The metallic NPs bridge the gap between the Cu pillar and the substrate to form an interconnect, replacing the conventional TCB method in Fig. 1.7. Liu *et al.* utilized the Ag NPs suspension to inject into the gap between

pillar and carrier. Capillary bridges form the electrical necks with increasing NP concentration after solvent evaporation. The sintering process establishes a stable interconnect at the low temperature[79]. Zürcher *et al.* reported a method for all-Cu flip-chip interconnects by dip-coating Cu ink on the Cu pillar and transferring it to the substrate[80]. Aoki *et al.* has published a fine pitch flip-chip technique using CuNP paste sintering to achieve plating-free bumps [81]. After the sintering process, the Cu pillar is formed. Then, the injection-molded solder (IMS) is injected at 250 °C as a buffer layer for C2C bonding. The manufactured sample has a 60 μm pitch pattern.

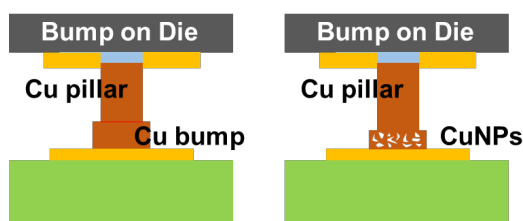


Figure 1.7: Schematics of the development of direct Cu to Cu bonding from using Cu-Cu TCB (left) to using CuNP joint (right)

1.3.3. Application in power electronics

One of the most promising applications of metallic NPs is in power electronics. Specifically, die attachment using nanopaste, applied through stencil printing followed by sintering, as illustrated in Fig. 1.8 [70], ensures a strong connection between the device and its substrate, providing high electrical and thermal conductivity. Compared to solder, nanomaterials can still function effectively at temperatures expected to exceed 250 °C in harsh environments. The excellent thermal conductivity can improve thermal management in power electronic components for large-area interconnections in power electronics [82], [83]. Efficient heat dissipation is critical to preventing overheating and ensuring the long-term reliability of power devices. By using metallic NPs as thermal interface materials (TIM), heat transfer can be enhanced from high-temperature components to cooling configurations [84]. metallic NPs applications are precious because overheating can hurt high-power applications like electric vehicles, industrial automation, and renewable energy systems.

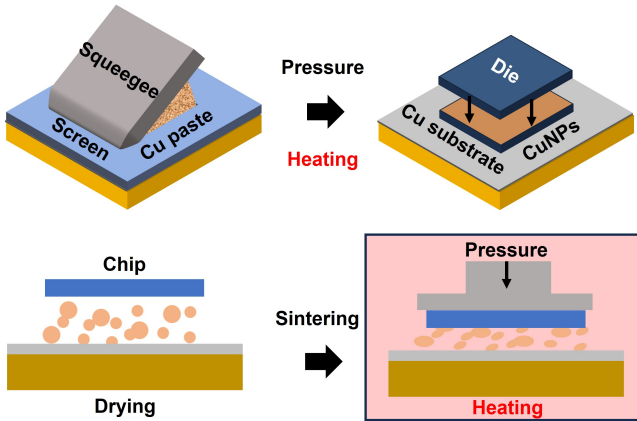


Figure 1.8: Schematics of die-attachment technology for power electronics packaging using nanopaste [70]

1.4. Challenges and Gaps

The key challenge of this thesis is using CuNP paste to replace traditional solder-based interconnects in high-density applications. Developing an efficient and scalable process for Cu-Cu direct bonding that can create high-resolution, fine-pitch interconnects.

For conventional Cu-Cu TCB, high pressure and temperatures of 300-400 °C are typically required to form interconnects through the Cu atomic diffusion. Plated Cu films or pillars generally require 100-150 MPa pressures, while CMP pre-treated Cu films require pressures below 2.5 MPa [49]. However, the high temperatures and pressures can lead to coefficient of thermal expansion (CTE) mismatches and introduce significant mechanical stress, potentially damaging components during the bonding process.

Hybrid bonding, another low-temperature method explored for fine-pitch interconnects, also offers the potential for sub-30 μm pitch interconnects by combining dielectric and metal bonding. However, this method faces challenges such as the need for near-perfect planarity, the high cost of advanced equipment, and the complexity of the process. Reliable bonding requires a specific ratio of dielectric to metal surface area, which limits the effective metal bonding area. Furthermore, surface contamination and roughness can significantly impact bonding quality, leading to inconsistent electrical

performance. It is necessary to align accurately and control parameters such as temperature, pressure, and time, which requires advanced equipment and materials, which increases costs. Considering these complexities, CuNP paste is a simpler and more scalable alternative that eliminates many difficulties associated with hybrid bonding while allowing for reliable interconnects through low-temperature sintering.

Although nanopaste and other metallic NPs have not yet become mainstream in high-density integration, Cu and Ag nanopaste are gaining increasing attention in power electronics packaging. They are being considered as replacements for traditional solder to enhance interconnect reliability. The increase in emphasis on improving interconnect performance is reflected in this change. Despite some progress made in achieving fine-pitch Cu-Cu bonding using CuNPs, significant challenges remain [79]–[81], [85], [86]. CuNPs have shown promise as an alternative, but there is still a requirement for developing a high-throughput and flexible method for transferring CuNP patterns, as well as further investigation into the properties and reliability of CuNP interconnects.

1.5. Outline of the Thesis

1.5.1. Scope of thesis

The work aims to develop and optimize a novel technique that utilizes metallic NPs, particularly CuNP paste, to create high-density interconnects in advanced semiconductor packaging technologies. Through NP sintering, direct Cu-to-Cu bonding can be achieved, which overcomes the limitations of traditional solder-based interconnects and provides a cost-effective and more straightforward alternative to Cu-Cu hybrid bonding. This method is intended for advanced 2.5D and 3D ICs.

The scope of this research involves developing and optimizing the LSP technique. The study examines novel NPs patterning methods and includes a fundamental mechanical and electrical performance evaluation of the resulting interconnects. In addition, the investigation focuses on fine-pitch bulk-Cu (B-Cu) to nanoporous-Cu bonding, aiming to establish a proof of concept and evaluate the reliability of novel Cu-Cu interconnects for high-density applications.

1.5.2. Thesis outline

The outline of this thesis is as follows:

Chapter 2: This chapter introduces an innovative LSP technique developed to address the limitations of conventional solder-based interconnects. The LSP process combines photolithography and stencil printing to transfer CuNPs with high precision, forming the basis for high-density μ bumps in 3D ICs. The chapter outlines the detailed process flow of LSP, including critical parameters such as photoresist thickness, printing cycles, and lift-off conditions. It also describes the experimental setup used to optimize the process to achieve uniform and high-resolution CuNP patterns. The chapter concludes by discussing the results of various optimization strategies applied to enhance NP patterning quality, highlighting the LSP technique's effectiveness in achieving reliable all-Cu interconnects.

Chapter 3: In this chapter, the focus shifts to exploring various applications of novel NP patterning methods to demonstrate the flexibility of this approach further. The chapter begins by discussing using sapphire-to-silicon flip-chip interconnects, where CuNPs are sintered to achieve robust and reliable bonds. It then examines the integration of photopatternable underfill films with fine-pitch Cu-to-Cu direct bonding, demonstrating how this combination can enhance interconnects' mechanical and electrical properties. Additionally, the chapter investigates the use of thin nanoporous films synthesized by spark ablation for fine-feature patterning, offering insights into advanced material applications in microelectronics. The chapter concludes with a synthesis of findings from these innovative approaches, emphasizing their potential to replace conventional methods in semiconductor manufacturing.

Chapter 4: This chapter is dedicated to the mechanical and electrical characterization of sintered CuNP bumps, which are critical for the performance of high-density ICs. It begins by outlining the experimental procedures for fabricating and testing the CuNP bumps, including detailed descriptions of the nanoindentation and electrical conductivity tests. The chapter presents the results of these tests, offering a comprehensive analysis of the mechanical strength, microstructural properties, and electrical performance of the sintered CuNP bumps. It discusses the implications of these findings for the reliability and effectiveness of CuNP interconnects, providing

evidence that supports their use in high-performance electronic devices. The chapter concludes with a summary of the key results, highlighting CuNP sintering interconnects' micro- and nano-mechanical properties.

Chapter 5: This chapter presents the experimental development and characterization of 20 μm fine-pitch Cu-to-Cu direct bonding using NP sintering technology. It begins by introducing the design of the interconnect test samples, followed by a detailed explanation of the photolithographic techniques employed to pattern the CuNPs. The chapter then describes the formation of fine-pitch interconnects through a carefully controlled sintering process, along with the mechanical testing conducted to assess the shear strength of the bonded dies. The results section provides an in-depth analysis of the microstructural properties of the sintered CuNP interconnects, demonstrating their suitability for high-density IC applications. The chapter summarizes the successful implementation of fine-pitch Cu-to-Cu bonding, highlighting its potential to meet the demands of next-generation semiconductor devices.

Chapter 6: Conclusion The final chapter summarizes the research outcomes and advancements in CuNP sintering for high-density IC applications. It highlights the significant impact of these findings on the semiconductor industry, particularly in addressing the limitations of conventional interconnection technologies. Additionally, this chapter explores future research directions, proposes strategies to further optimize CuNPs-based interconnections, and identifies key reliability challenges that require further investigation.

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2

Lithography Stencil Printed Nanoparticle Transfer Technology for High Density Microbumps

This chapter presents an innovative LSP technique for the fabrication of high-density metallic interconnects, addressing the critical demands of advanced semiconductor packaging in 3D ICs. The LSP method utilizes lithographically patterned photoresist to ensure precise transfer of CuNPs onto substrates, followed by a lift-off process to produce high-resolution patterns. Optimizing process parameters, such as stencil material selection, printing pressure, and photoresist thickness, is key to ensuring optimal pattern quality. According to the study, the LSP technique is capable of producing uniform and well-defined CuNP bumps with varying sizes (20 μm to 100 μm) and pitches, making it suitable for fine-pitch interconnects. The optimized lift-off process, conducted at 60 °C with agitation, significantly improves the integrity of the transferred patterns, minimizing residues and ensuring clean substrate surfaces. Furthermore, the influence of printing repetitions and photoresist thickness on pattern transfer is investigated, revealing that double printing is essential for thicker photoresists, while single printing suffices for thinner photoresists to avoid short-circuiting in fine-pitch applications.

2.1. Introduction

In recent years, the trend to integrate more microelectronic functions per unit area is not solely supported by Moore's law anymore [1]. Heterogeneous and 3D integration are now the key enablers to drive further integration, which will put chip assembly technologies more in the center of system creations. Moreover, not only the SiPs but also HI can broaden the spectrum of applications beyond conventional microelectronic applications, which drives the need for novel packaging solutions. With the high demand for more multi-functionalization and "more-than-Moore" application, the 3D stack integration can be the approach at C2W and C2C [2]. Flip chip technology plays an important role in 3D integration and is recognized as an essential building block that can support more complex C2W and C2C assemblies [3].

The conventional approach for C2W and C2C integration is solder-based flip-chip intermetallics technology. However, this approach has several disadvantages, including restricted height, susceptibility to EM, and re-melting at high temperatures. As a result, solder cannot meet the demands of advanced electronic devices and packaging technologies [4]. To address these issues, silver and copper nanometallic materials have been proposed as replacements for solder. Metallic nanoparticles have garnered significant attention from researchers as interconnecting materials due to their non-melting properties and higher thermal conductivity [5]. Compared to silver, Cu offers higher electrical conductivity and is more cost-effective [6]. CuNP sintering occurs at low temperatures, does not reflow during the assembly process, and, once sintered, the material remains stable at high temperatures. CuNP joint integration technology is considered a promising solution to replace solder in advanced packaging applications [7].

CuNP joint bonding technology is investigated due to its good thermal dissipation ability, mechanical property and electrical conductivity. Recent studies have been undertaken to employ and transfer copper nanoparticles to establish interconnection. Zürcher [8], [9] and Carro *et al.* [10], [11] presented a dip-based method for transferring the copper nanopaste as the interconnects between Cu pillar and pad, reducing the sintering temperature below 200 °C. Sosa *et al.* [12], [13] investigated the nanoporous-Cu caps to integrate the

Cu-pillar interconnects with nanoporous-Cu caps using thermal compression bonding process. Wang *et al.* [14] used a pulsed laser deposition method to deposit Cu nanoparticles onto a hole-patterned photoresist and subsequently stripped the photoresist to form an all-Cu interconnect. Aoki *et al.* [15] used Cu nanopaste, applied through a photoresist mask, to transfer the nanopaste onto the substrate. Following this, Cu pillars were formed through a sintering process, which were then integrated into conventional solder-based interconnect technologies.

This chapter presents novel methods for transferring CuNPs to achieve metallic interconnects, which facilitate device interconnection. Utilizing lithographically patterned photoresist as a stencil enables the precise transfer of nanopaste during the lift-off process, resulting in accurate patterns. The lift-off process is widely employed in microfabrication for patterning thin films, offering significant advantages in achieving high-resolution patterns. Using photoresist as a mask for material transfer, this method ensures precise patterning, which makes it essential for applications in semiconductor device fabrication and nanotechnology [16].

The lift-off process is a commonly used method for defining complex structures, which is a crucial step in the research of the LSP process. Moreover, lift-off is presented to be an advantageous technique for patterning materials that are difficult to etch. CuNP paste is a material made by mixing diluted nanoparticles with reactants and stabilizers. As a paste, it is typically deposited using conventional paste dispense techniques such as injection or stencil printing with a squeegee. Due to the complex structure of the material, once deposited it is hard to etch using conventional methods. Therefore, we need to investigate the application of lift-off in CuNP patterning process. The lift-off process is a viable solution for advanced semiconductor packaging applications, and this approach provides a solution for fabricating high-density interconnects. Bellaredj *et al.* [17] demonstrated the application of a lift-off process for thick copper films in advanced packaging for RDL, highlighting the potential of this technique for use in the semiconductor field.

The combined process of stencil printing with lift-off is referred to as the LSP process, which has the potential for high throughput and high resolution [7]. The primary objective is to investigate the transfer

of CuNPs through stencil printing using CuNP paste, combined with the optimization of the lift-off and printing processes.

2

2.2. The Approach of Lithographic Stencil Printing

Both lift-off and stencil printing methodologies are essential factors in determining the quality of the patterning results. These two methods are commonly employed for transferring metal. It is usually used for sputtered or evaporated thin metal films. Stencil printing, utilized for applying paste materials, has already found applications in flip-chip interconnect [18]. The LSP process integrates these two technologies to achieve precise metal patterning.

2.2.1. Flow of lithographic stencil printing

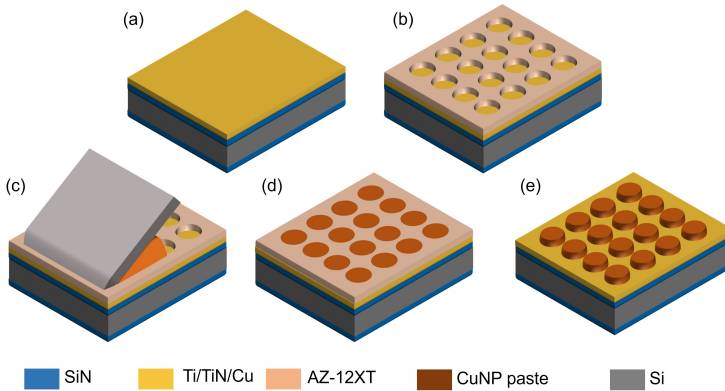


Figure 2.1: A overview of the patterns transferring process for all-Cu interconnects using LSP. (a) Insulation and adhesion layer deposition. (b) Photolithography. (c) CuNP paste spread process. (d) Dry process. (e) Lift-off process.

The process flow of LSP for transferring CuNP paste is depicted in Fig. 2.1. The first step was to grow 300 nm of low-stress silicon nitride (SiNx) as an insulating barrier layer on a silicon wafer by low-pressure chemical vapor deposition (LPCVD), followed by sputter coating of a 25/2 nm Ti/TiN adhesive layer along with a 300 nm Cu interconnect layer, as illustrated in Fig. 2.1a. Subsequently, a positive photoresist layer was spin-coated on the wafer, then was exposed and developed

with a contact opening mask, as demonstrated in Fig. 2.1b. The CuNP paste is then manually distributed using a silicon squeegee to fill the gaps between the photoresist. The CuNPs on the photoresist surface should be removed as much as possible to minimize the residue on the photoresist surface. This step is referred to as the spreading process, as shown in Fig. 2.1c. The next step was the drying process, where the CuNPs spread wafer was dried in an oven at 80 °C to 110 °C for 10 min to 15 min (Fig. 2.1d). Finally, The lift-off process was applied by N-Methyl-2-pyrrolidone (NMP) to strip the photoresist, as depicted in Fig. 2.1e. This LSP process was completed after rinsing by deionized (DI) water.

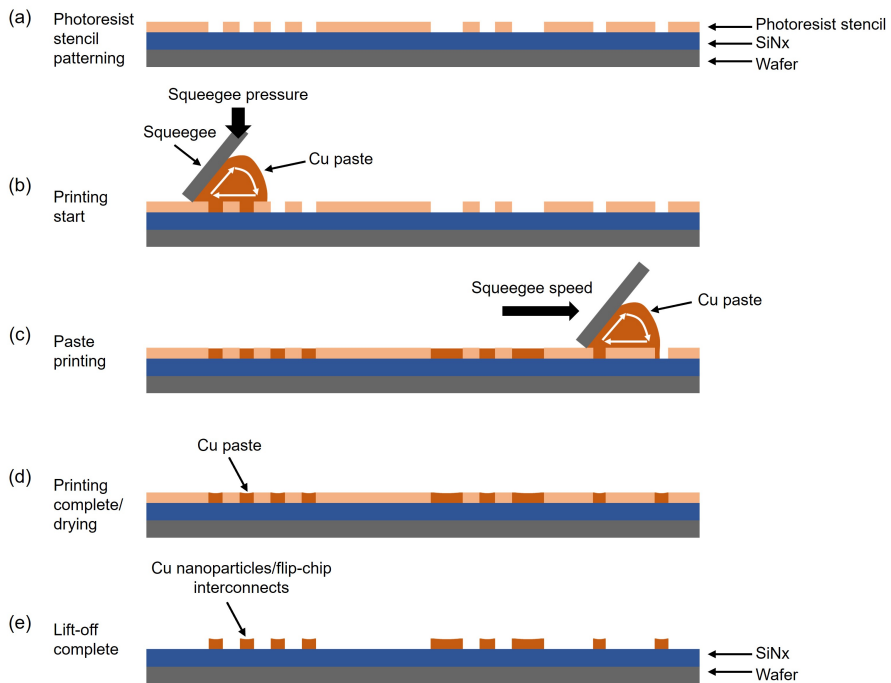


Figure 2.2: A cross-sectional sketch of LSP. (a) Insulation and adhesion layer deposition. (b) Photo lithography. (c) CuNP paste spread process. (d) Dry process. (e) Lift-off process.

The schematic of the LSP process, comprising two main procedures, is illustrated in Fig. 2.2, highlighting the details and key parameters for discussion. The initial step is the printing process,

which is similar to conventional stencil printing, where metallic materials are applied to the substrate. The lift-off process is the second step that ensures precise patterning by removing any excess deposited metal materials.

The factors that influence conventional stencil printing have been investigated and discussed in previous studies [19]. In this research, we utilized photoresist as the stencil material. The process has been optimized by selecting key parameters that are relevant to our applications, with the aim of improving the integrity of the patterned results. The critical parameters that are necessary for both printing and lift-off processes are listed below.

Fig. 2.2b and c show that stencil printing is a dynamic and multifaceted process. The process commences with the placement of a wafer or substrate, then a squeegee is used to move the CuNP paste through the stencil apertures under controlled pressure and speed. Excessive pressure from the squeegee is not appropriate because the stencil is made of soft photoresist and not conventional stainless steel. After printing, the wafer is removed from the vacuum chuck and CuNP paste is deposited onto the SiNx substrate. The process involves the transportation, transfer, and drying of CuNP paste, and a process map is created to provide a reference for various circumstances. In applications demanding fine pitch, the properties of CuNP paste, aperture size, and photoresist mask thickness are crucial parameters. The uniformity of CuNP paste deposition depends on factors such as paste formulation, number of printing and squeegee type. Since we cannot alter the formulation of the CuNP paste, this factor will not be taken into consideration in this section.

In the lift-off process, the sacrificial photoresist layer serves as the mask pattern. The formation of CuNP patterns is achieved through squeegee printing of nanopaste onto the photoresist pattern, followed by the dissolution of the sacrificial layer to remove the excess deposited materials. For the LSP technique, it is necessary to enhance the lift-off process, and factors such as the photoresist thickness and the lift-off process temperature can significantly influence the results of this process. The assessment of the integrity and topography of patterned CuNPs after the lift-off process will be examined in the Sec. 2.3.

If required, the spreading and drying processes need to be repeated

twice to improve the uniformity of the CuNP pattern heights in certain situations. Following the first CuNPs spreading process, the processing wafer should be dried at 80 °C for 10 min. Subsequently, to repeat the steps shown in Fig. 2.1c and d, the second CuNP paste spread wafer is dried at 110 °C for 15 min. The resulting CuNP patterns for both single and double spreading processes, along with the situations in which they should be applied, will be discussed in the Sec. 2.3.2.

2.2.2. Experimental Setup

Fig. 2.3a displays the stencil printer setup, which includes a vacuum chuck platform to clamp the process wafer that has already been coated with photoresist patterns. Fig. 2.3b shows the squeegee used for the application of spreading CuNPs. Typically, stencil printing squeegees are made of rubber or stainless steel. For managing substrates between 2 and 4 inches in size, a rigid squeegee is necessary for the LSP application. Commercially available squeegees, typically made of polymers, are not suitable for this purpose. For transferring fine-pitch and ultra-fine-pitch CuNP paste, the flatness of the squeegee is crucial, as it significantly influences the uniformity of CuNP paste deposition. To achieve a highly flat squeegee, we cleaved a 4-inch Si wafer along the crystalline direction of Si into 15–20 mm wide strips. The resulting fracture surface displayed the expected flatness. To handle the silicon strips as a squeegee, we designed and 3D-printed a squeegee holder. A rounded squeegee edge was formed by wrapping a 150 μm thick Kapton tape around the edge of the silicon strip.

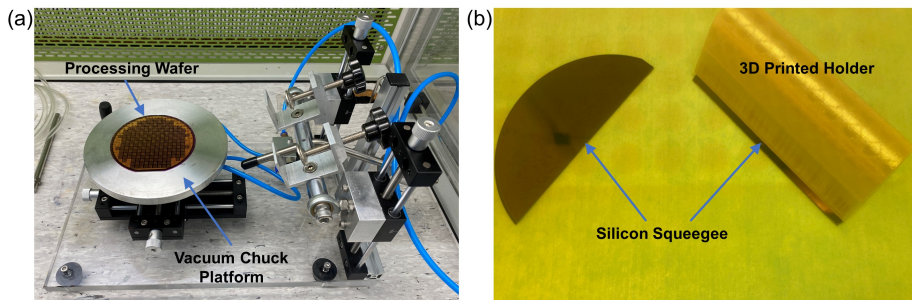


Figure 2.3: (a) Manual stencil printer with vacuum chuck platform and (b) wafer-scale LSP set-up with silicon wafer made squeegee.

2.3. Experimental Optimization of LSP Procedure on NP Patterning

As mentioned in the previous section, the factors affecting the results of both stencil printing and the lift-off process need to be investigated, as they are interrelated. The equipment utilized for the lift-off process, temperature conditions during lift-off, photoresist thickness, and number of printing cycles are discussed in this section. The outcome of the LSP process is influenced by the coupling of all of these parameters. The lift-off process was improved first before optimizing the printing procedure.

2.3.1. The influence of lift-off procedure on patterning results

This subsection investigates the effects of different experimental conditions and equipment on the results of patterning CuNPs using the lift-off process. The test silicon wafers were first coated with 300 nm of SiNx, followed by the sputtering of a Ti/TiN layer. To optimize the transfer process of CuNP paste using the LSP method, we utilized test wafers coated with a 10 μm thick photoresist (AZ 12-XT). The test pattern consisted of holes ranging in size from 20 μm to 100 μm , with a pitch of 250 μm . The mask details are provided in the Appendix A. The corresponding process flow is illustrated in Fig. 2.1, with steps Fig. 2.1c and d repeated once to achieve double printing of CuNPs. The initial discussion revolved around improving the integrity of CuNP patterns through the lift-off process at room temperature, and then we expanded the investigation to higher lift-off temperatures.

Room temperature lift-off process

In a previous study, Bellaredj *et al.* have successfully achieved ultra-fine pitch interconnects of the evaporated Ti/Cu film, using the lift-off technique in a heated ultrasonic bath at 60 °C with a dedicated organic solvent [17]. Initially, lift-off steps were performed at room temperature to prevent the dissolution of patterned CuNPs in the NMP solution. Following the design of experiments (DOE) in Table 2.1, we labeled the test wafers as Wafer A to D and tested the CuNPs results under different process conditions. In Fig. 2.4a, wafer A was placed downwards into a rectangular glass container, which was

then placed in an ultrasonic bath for 10 seconds. Following that, the wafer was set aside for one minute, then the wafer was taken out and rinsed with DI water.

Table 2.1: DOE for Lift-off Process at Room Temperature

Parameters	Wafer A	Wafer B	Wafer C	Wafer D
Agitation	0	2 min 210 rpm	2 min 210 rpm	2 min 210 rpm
Ultrasonic	10 s	0	0	0
Bumps Size	100 μm	100 μm	100 μm	20 μm
Wafer Placement	downward	downward	upside down	upside down

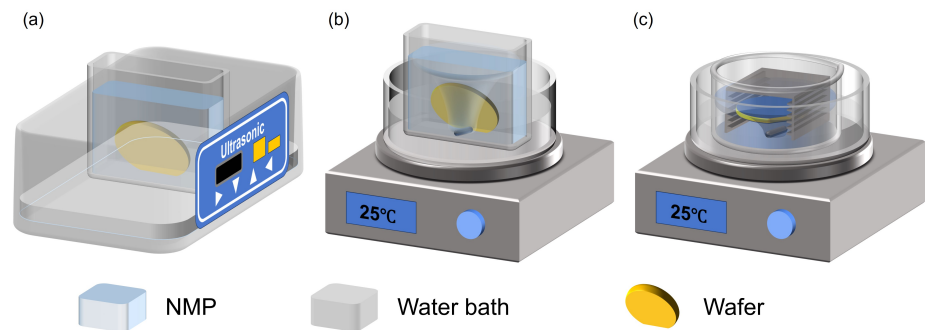


Figure 2.4: The schematic diagram of the hardware and equipment used in the lift-off process at room temperature. (a) Ultrasonic-bath setup, (b) agitation setup, and (c) wafer upside down with agitation.

After drying, we obtained images of the wafer surface, as shown in Fig. 2.5a and b. It can be seen that no intact CuNP bumps remain on the substrate. However, there are some obvious traces in the form of CuNP patterns in Fig. 2.5a, which are derived from the peeled-off CuNP bumps, as indicated by the green arrows. Moreover, a large amount of residual CuNPs stayed on the substrate, as highlighted by purple and yellow arrows, which could not be completely removed during the described process.

Therefore, we modified the lift-off tool and process conditions for Wafer B to further investigate and enhance the integrity of the transferred CuNP patterns. Instead of using the ultrasonic bath for

the lift-off process, we used a hotplate stirrer at the room temperature. The glass container was placed on the hotplate, and magnetic stirring was utilized to agitate the lift-off process at 210 rpm for 2 min, as illustrated in Fig. 2.4b.

The optical and SEM images of the Wafer B after rinsing with DI water are shown in Fig. 2.5c and d, respectively. There has been a significant improvement in the quality of the patterned CuNPs array. It is apparent that the patterns match the opening area of the photoresist stencil. The CuNPs residual were attached at the edge of CuNP bumps in the form of a small triangle, as indicated by the purple arrow. A large number of CuNP bumps peeled off (green arrow), leaving noticeable traces on the substrate. The CuNPs residue can be seen as a thin layer on the substrate in Fig. 2.5d, which is highlighted by the yellow arrow. The adjacent CuNPs exhibited a well-defined shape corresponding to the opening in the photoresist stencil, and there were only a few residues remaining in the areas covered by the photoresist. It seems that this method can effectively remove the CuNPs that was deposited on top of the photoresist. Despite the processing conditions, the CuNP bumps were not effectively maintained on the substrate, and some residual material fell onto the substrate during agitation, leading to the formation of a triangular thin layer residue.

We maintained the same surrounding conditions for the lift-off process and improved the lift-off tool to address the issue of re-deposited CuNPs residues. In this optimization, we used a 4-inch wafer carrier to accommodate the entire wafer. In Fig. 2.4c, Wafer C was facing down and placed inside the carrier, with magnetic stirring applied below the wafer to dissolve the photoresist for 2 min. Fig. 2.5e and f show the inspection results of the CuNP patterns in size of 100 μm . It can be observed that both the problem of re-deposition of CuNPs residues and the integrity of patterns have significantly improved. There has been a noticeable decrease in the amount of CuNPs residue attaching to the bump edge, and the surface has no residues in the areas covered by photoresist. Despite efforts, the issue of bumps peeling off remained, as shown by the green and yellow arrows. It is observed that the bumps are peeling off and moving to different positions on the wafer substrate. It is possible for the peeling off phenomenon to happen during both the lift-off process and the

rinsing step, as indicated by this observation. It can be attributed that the patterning integrity was not maintained due to the processing time being too long or Cu to substrate adhesion is not adequate.

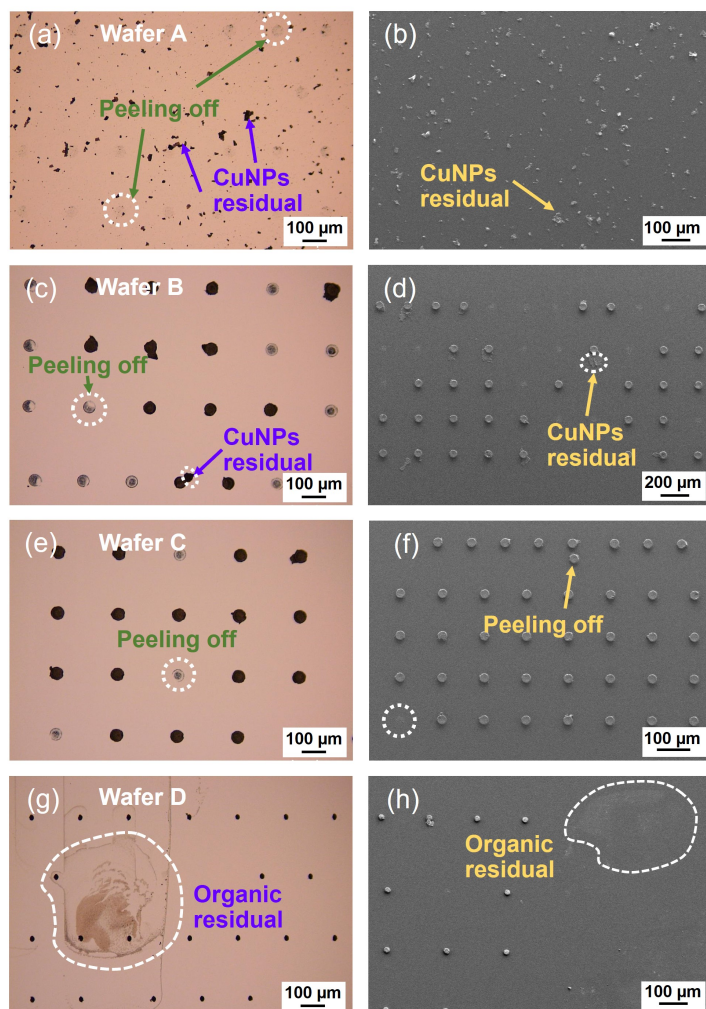


Figure 2.5: Optical (left) and SEM (right) images of the resulting Wafer A to Wafer D after the lift-off process depict the surface of the processing wafer using the tool in Fig. 2.4, respectively.

We inspected the Wafer D with an array of CuNP bumps sized at 20 μm , following the same process flow as that of the 100 μm sample, using the lift-off processing conditions (in Fig. 2.4c) for 2 min. The

results are depicted in Fig. 2.5g and h. Pattern integrity in the 20 μm size has also been improved. The SEM image in Fig. 2.5h shows that only one bump has moved to another bump, much like the observation made in Fig. 2.5f regarding the 100 μm sample. It is worth mentioning that the problem with CuNP paste residues has been greatly reduced in this sample, which was not apparent in Fig. 2.5g. However, there were issues with organic residue, as labelled by the white dashed circle with purple and yellow markers. It reveals that 2 mins processing time was not sufficient for this sample.

Based on the observation, although agitating the wafer face-down for 2 min at room temperature has better the lift-off results, it is not the ideal processing condition for the LSP technique. It causes larger-sized bumps (100 μm) to peel off from the substrate, and it also leads to organic residue issues observed on the wafer with smaller-sized bumps (20 μm). To address these issues, a lift-off process with shorter process times and higher bath temperatures was investigated.

High temperature lift-off process

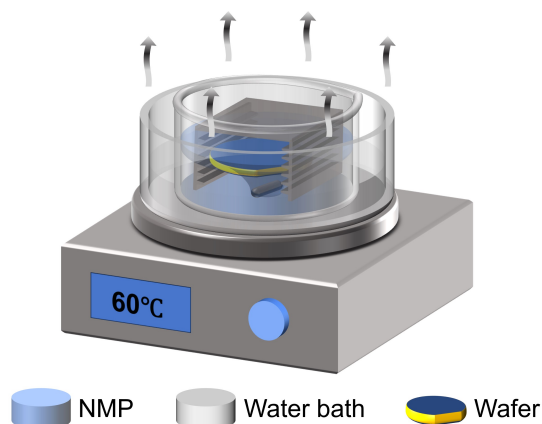


Figure 2.6: The schematic diagram of set-up used in the lift-off process at high temperature of 60 °C.

As discussed in the previous part, the 2-minute processing time at room temperature was found to be too long for larger-sized CuNP bumps, which have a higher area ratio of bumps to photoresist, while being too short for smaller-sized CuNP bumps, which have a lower

area ratio. The lift-off results in this study could not be consistently improved by just adjusting the lift-off time. We raised the lift-off temperature to 60 °C, which accelerated the dissolution of the epoxy-based photoresist to strip the excess CuNP paste without affecting the transferred CuNP paste. By reducing processing time, it is possible to keep the CuNPs in larger sizes. Consequently, we made the decision to place the wafer coated with CuNP paste in the 4-inch wafer carrier and process it with agitation for 90 seconds, as depicted in Fig. 2.6.

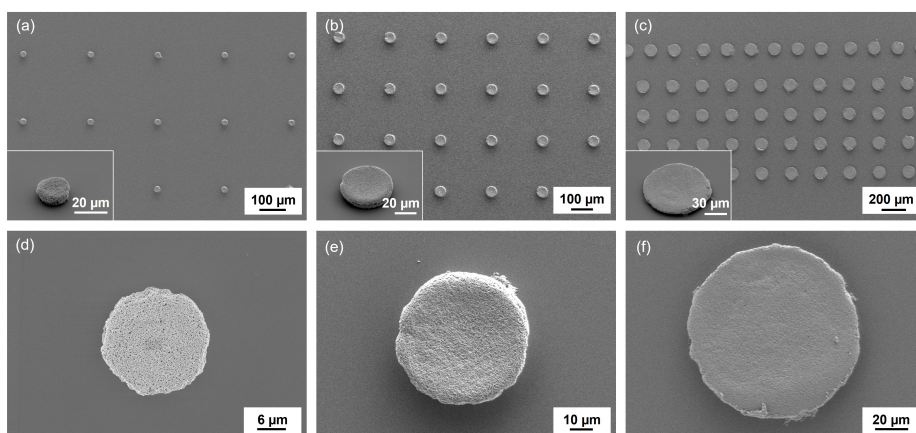


Figure 2.7: SEM images of CuNP bumps with different diameters using optimized lift-off processing conditions, applied with the same thickness of photoresist stencil for LSP process, showing various aspect ratio bumps.

Fig. 2.7 shows the SEM images of the resulting wafer after enhancing the lift-off process, indicating the integrity of the CuNP bump array. Three different sizes of CuNP bumps, measuring 20 μm , 50 μm , and 100 μm , were characterized to demonstrate patterns at long range scales, as illustrated in Fig. 2.7a-c. The inset images depict a single CuNP bump in a top view. It is evident that both the photoresist and CuNP paste on its top surface were totally removed from the substrate, leaving the surface below the photoresist covered remarkably clean without any CuNPs, comparing to Fig. 2.5. The bumps have distinct edges and maintain a consistent, rounded shape across all sizes, forming an array of bumps with integrity.

Fig. 2.7d-f depict the CuNP bumps, sized at 20 μm , 50 μm , and 100 μm , tilted at a 45 degree angle. The transfer process using LSP for

each sample used the same thickness of the photoresist and performed double printing. Different aspect ratios were observed in bumps with different aperture openings during the LSP process due to variations in the aperture opening of the photoresist. It can be seen that the surfaces of all sizes of bumps are smooth, while the edge areas are slightly higher than the central part. This can be attributed to the evaporation of organic solvents in the drying steps of the LSP process, leading to some shrinkage of the CuNPs. In addition, their appearance is mushroom-like, with wider tops and narrower bottoms, which is more obvious for bumps with a high aspect ratio, attributed to the overcut profile obtained by the positive photoresist [20].

Fig. 2.8a-c show 3D images of bumps with dimensions of 100 μm , 50 μm , and 20 μm , respectively. It can be observed that these bumps of various sizes have sharp edges, relatively flat surfaces and sufficient heights to facilitate the formation of all-Cu interconnects, especially for the interconnects without electroplating Cu pillars.

The height profile was measured on one arbitrary bump from each array of CuNP bumps with different sizes, as shown in blue, black, and red dashed boxes in Fig. 2.8a-c. The sum of the height profile is indicated in Fig. 2.8d with the corresponding color curves. It shows that the 100 μm and 50 μm bumps exhibit a bowl-like shape, with estimated lowest and highest positions of 10 μm and 14 μm for the 100 μm bump (by blue curve), and 11 μm and 13.5 μm for the 50 μm bump (by black curve), respectively. This reveals that shrinkage of the volume of CuNP bumps inevitably occurs with the LSP method, which heavily influences the central part of the bumps. Furthermore, CuNPs are prone to maintaining and accumulate next to the photoresist wall, resulting in more CuNPs at the edges of the bumps. Right and left edges differ in height levels in both 100 μm and 50 μm bumps, with a noticeable directionality being caused by the printing direction of the CuNP paste. The 20 μm bump was identified by the 3D profilometer as cylindrical with a round top (represented by the red curve), but this is not the bowl-shaped surface that was observed in the previous SEM image (Fig. 2.7d). The profilometer cannot accurately detect the surface morphology at this scale, and we can only obtain an approximate height of the bump estimated to be 9.5 μm .

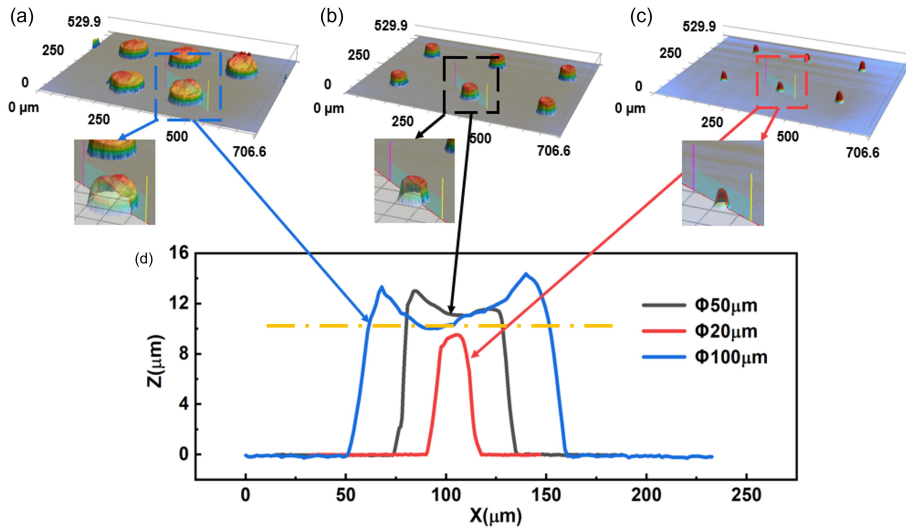


Figure 2.8: Profiles images of transferred CuNP bumps using the optimized lift-off process are depicted in (a), (b), and (c), representing the 3D profiles of measured substrates with CuNP bumps sized 100 μm , 50 μm , and 20 μm , respectively. (d) illustrates the topography of measured bumps, with the 100 μm , 50 μm , and 20 μm sizes indicated by blue, black, and red marks in (a), (b), and (c), respectively. The yellow dashed line represents the height of applied photoresist.

Based on observations, the extent of CuNPs height shrinkage decreases with higher aspect ratios of bumps. The larger the bumps are, the greater the difference between the lowest and highest points. For this sample, the changes in aspect ratios are between 0.5 and 0.1. The thickness of the photoresist is the primary factor in determining the height of bumps, and the height of larger bumps is typically slightly higher. Despite not being perfectly flat, the surfaces display relative flatness. The surface profile of the bumps indicates that the LSP has clear printing directionality. Because the nanoporous material can be compressed during the TCB process, the non-uniformity is not a barrier for stacked dies integration.

We determined that the lift-off process is performed at a temperature of 60 $^{\circ}\text{C}$ with 2 min agitation when the printed wafer is flipped downward, as the optimized process conditions. The formation of actual CuNP joint interconnects will be achieved in subsequent research using this method. The next subsection will address the additional LSP factors to provide more comprehensive

instruction for further applications.

2.3.2. The influence of printing procedure on patterning results

In the previous subsection, we established a photoresist thickness of 10 μm to optimize the lift-off process for the LSP technique. Throughout that study, we consistently applied the CuNP paste twice during the printing process, as double printing was found to be essential for achieving uniform and reliable pattern transfer.

In this subsection, we systematically investigated how the interplay between photoresist thickness and printing repetitions influences the quality of CuNP pattern transfer. By varying the photoresist thickness and evaluating the impact of single versus double printing, we aimed to adapt the process to different aperture sizes and application requirements. The optimized lift-off parameters from the previous subsection were utilized to ensure consistency and reliability in this evaluation.

Process optimization applying thick photoresist

We consistently applied thick photoresists to test wafers coated with Ti/TiN layers and implemented a double-printing process during the paste printing step in Sec.2.3.1. As the next step in this research, we first investigated the influence of thick photoresists as stencil masks in the LSP printing procedure, focusing on the number of printings during the paste printing step. The photoresist mask was created by spin-coating AZ-12XT at 6 μm on the substrate of the dummy sample and featured a hole-patterned array with a diameter of 50 μm . Subsequently, the numbers of printing was tested on the prepared dummy samples in the paste printing procedure, as indicated in Fig. 2.1c. Continuously, the following steps were carried out, based on the optimized lift-off process at 60 $^{\circ}\text{C}$ with agitation in an NMP solution.

The patterning results using LSP process are illustrated in Fig. 2.9. The height profile of the CuNP bumps are characterized by measuring a single bump on each sample. Black and red dashed boxes were used to highlight selected bumps during both single and double printing procedures in the paste printing process. The black and red curves were used to show the corresponding height profiles. It can be

observed that these bumps with different numbers of printing have sharp edges and show a height difference between the right and left side walls, which indicates the obvious printing direction. It is worth noting that the height of bump from single printing is significantly lower than that from double printing. Furthermore, the bump produced by double printing have surfaces that is relatively flat, while that produced by single printing has more surface roughness. It reveals that for thicker photoresist exceeding $6\text{ }\mu\text{m}$, double printing during the LSP procedure is necessary. This approach ensures the transfer of uniform CuNP bumps with sufficient height, thereby facilitating the sintering process for die integration.

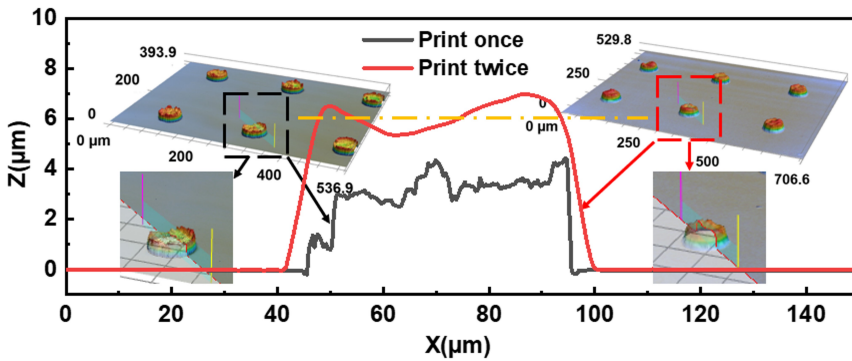


Figure 2.9: Comparison of CuNP bump profiles: printed once (black) vs. printed twice (red) using $6\text{ }\mu\text{m}$ photoresist. The yellow dashed line represents the height of applied photoresist. The inset shows 3D images of CuNP bumps, with black and red markings signifying single and double printing accordingly.

Process optimization applying thin photoresist

The test Si wafer was sputtered Ti/TiN/Cu layer to examine the effect of using thin photoresist on the transfer of CuNP patterns. This investigation considered various sizes of photoresist opening areas and different numbers of printing. We prepared other dummy samples to examine the transfer results when using thin photoresist. The photoresist (AZ 10-XT) mask was applied with an thickness of $3.1\text{ }\mu\text{m}$, and the holes were sized between 20 and $50\text{ }\mu\text{m}$, in the pitch of 40 and $100\text{ }\mu\text{m}$. The Appendix A contains information about the mask.

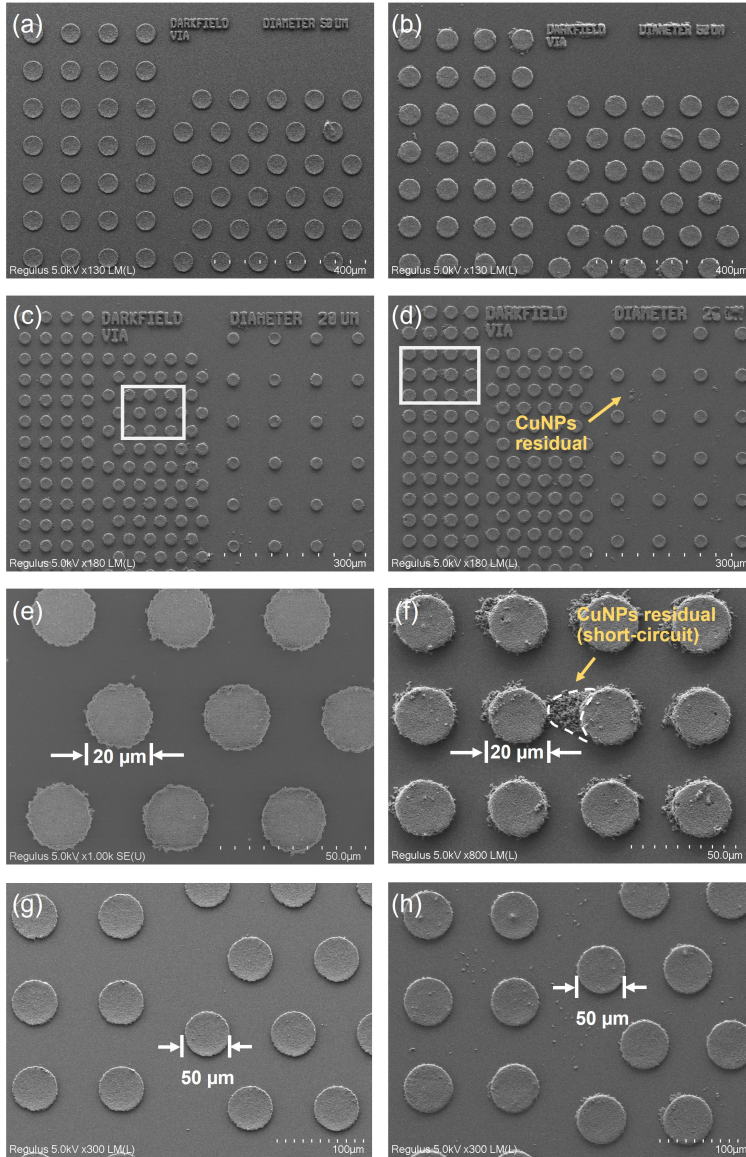


Figure 2.10: SEM images of CuNP bumps with different diameters on the same dummy sample using optimized lift-off processing conditions, applied with a thin thickness ($3.1 \mu\text{m}$) of photoresist with different numbers of printing: (a)(c)(e) and (g) single printing; (b)(d)(f) and (h) double printing.

The SEM images of the dummy sample with a thin photoresist mask applied after lift-off are displayed in Fig. 2.10, which reveal the

details of the CuNP bump array in different diameters and the substrate surface. Fig. 2.10a, c, e, and g illustrate the resulting samples obtained by printing CuNP paste once, while Fig. 2.10b, d, f and h depict the resulting samples obtained by printing the paste twice. For 20 μm -sized CuNP bumps, Fig. 2.10c and d represent zoomed-in images of the areas marked with white boxes in Fig. 2.10a and b, respectively. The integrity of the CuNP bump pattern was ensured through both single- and double printing processes. Moreover, there were noticeable differences in those two processes. In single printing, the substrate remained clean outside the CuNPs patterned area, while in double printing, there was a significant residue on the substrate in the photoresist-covered region, as indicated by yellow arrow. It was evident that for the fine pitch of 40 μm bumps array, more CuNPs residues accumulated on the substrate and between adjacent bumps, leading to short circuits when integrated in 3D IC applications, as marked by white dashed circle in Fig. 2.10d.

Fig. 2.11a and b illustrate single CuNP bumps with a diameter of 20 μm following single and double printing processes, respectively. Both bumps have clear edges that correspond to the opening area in the photoresist mask. When the CuNP paste is applied twice, it is observed that there are still NPs surrounding the bumps and adhering to the substrate (in Fig. 2.11b), whereas this issue is not observed when the paste is applied only once (in Fig. 2.11a). Fig. 2.11c shows a significantly cleaner background following single printing compared to double printing shown in Fig. 2.11d. The height profiles of the measured CuNP bump arrays that were influenced by different printing numbers are depicted in Fig. 2.11g. The black line and red line were the measured bumps depicted in Fig. 2.11e and f. It is obvious that the height profile when using a single printing process is slightly lower than when using a double printing process. Both profiles have a bowl-like shape and the degree of collapse in the central area is not significantly different.

When considering a larger pitch of 100 μm in a CuNP bump array with a diameter of 50 μm , Fig. 2.10g and h depict higher magnification images from Fig. 2.10e and f. The integrity of the transferred bump arrays after both single and double printing processes is revealed in these images. The removal of CuNPs residue from the photoresist-covered area was improved when using LSP with a larger

hole size of 50 μm , as shown in Fig. 2.10f. This is in contrast to the process applied with a hole size of 20 μm (Fig. 2.10d), where double printing is particularly evident. As depicted in Fig. 2.10h, there are still some individual NPs cluster attached to the substrate. However, there are no connections between adjacent bumps, indicating that these isolated NPs will not affect the electrical properties after die-to-die bonding.

In comparison to the 50 μm single CuNP bump after single printing in Fig. 2.12a, the bump of the same size after double printing in Fig. 2.12b has a more rounded surface with remaining CuNPs surrounding it. Similar to the bump array in Fig. 2.11, the substrate was cleaner after single printing compared to after double printing, as shown in Fig. 2.12c and d. When the size of the transfer bumps increases to 50 μm , the number of prints has a more significant effect on the height profile, as shown in Fig. 2.12g. The black and red lines represent the bumps after single and double printing that were characterized in Fig. 2.12e and f. It has been observed that the height profile of CuNP bumps produced by the single-printing process is significantly lower than that created by the double-printing process. The profile of single printing possesses a bowl-like shape, and the collapse in the central area is attributed to shrinkage during the dry process in LSP procedure. In contrast, bumps produced with double printing exhibit a uniform height of approximately 3.1 μm , consistent with the thickness of the photoresist.

Based on the observations, when we applied a thin photoresist with a thickness of 3.1 μm to a test wafer containing CuNP bumps of various sizes and pitches, both the size of the opening apertures and the number of printings had an impact on the transfer results. Considering the cleanliness of the substrate, single printing consistently proved more effective in enhancing lift-off by removing CuNPs residue from the sample within the photoresist-covered area. The height profiles of the 20 μm and 50 μm size bumps produced by a single print are at the same level, with a height of approximately 2.7 μm . This observation demonstrates that the LSP method can transfer CuNP patterns of different sizes to the same height. The advantage is evident when compared to electroplated Cu bumps, which require the same size opening area to achieve the same height.

The height of transferred patterns is not significantly different

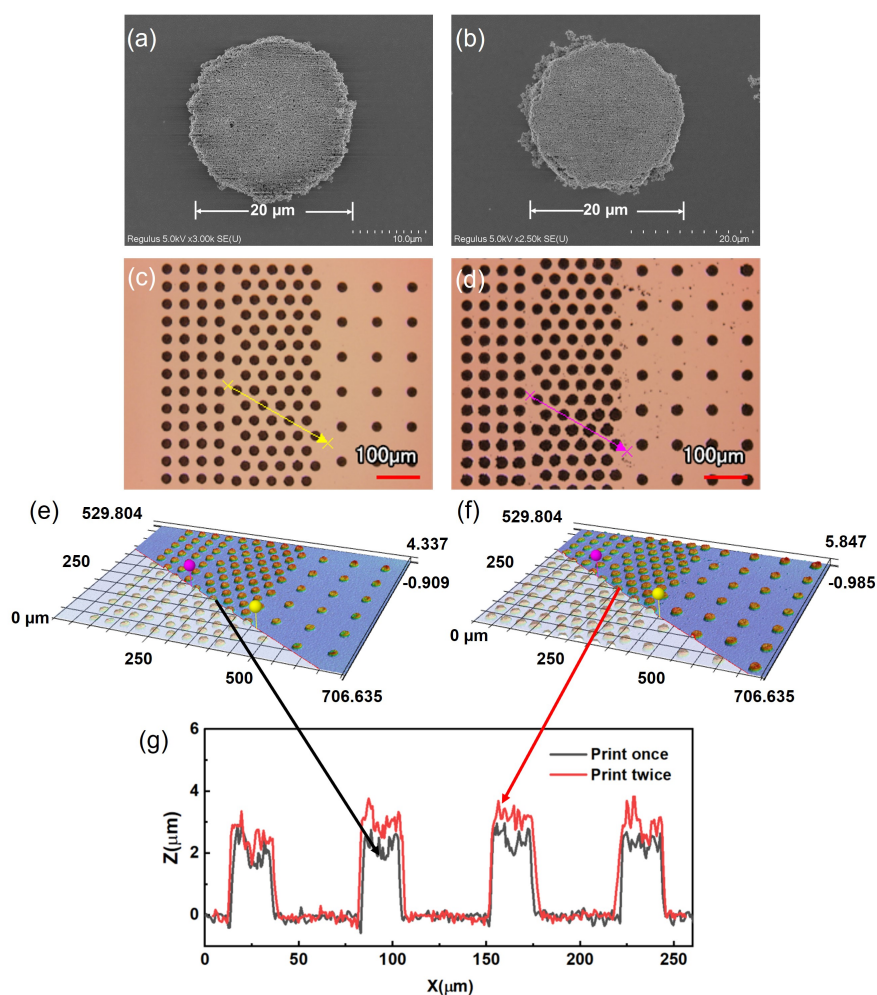


Figure 2.11: SEM images of a single CuNP bump with a 20 μm diameter by (a) single printing and (b) double printing. Optical images of transferred CuNP bumps array in 40 μm pitch by (c) single printing and (d) double printing. (e) and (f) represent the 3D image of the surface profile corresponding to (c) and (d), respectively. And (g) shows the height profile of the surface of measured CuNP bumps along the yellow and pink lines in (c) and (d), indicated by the black curve and red curve in (e) and (f).

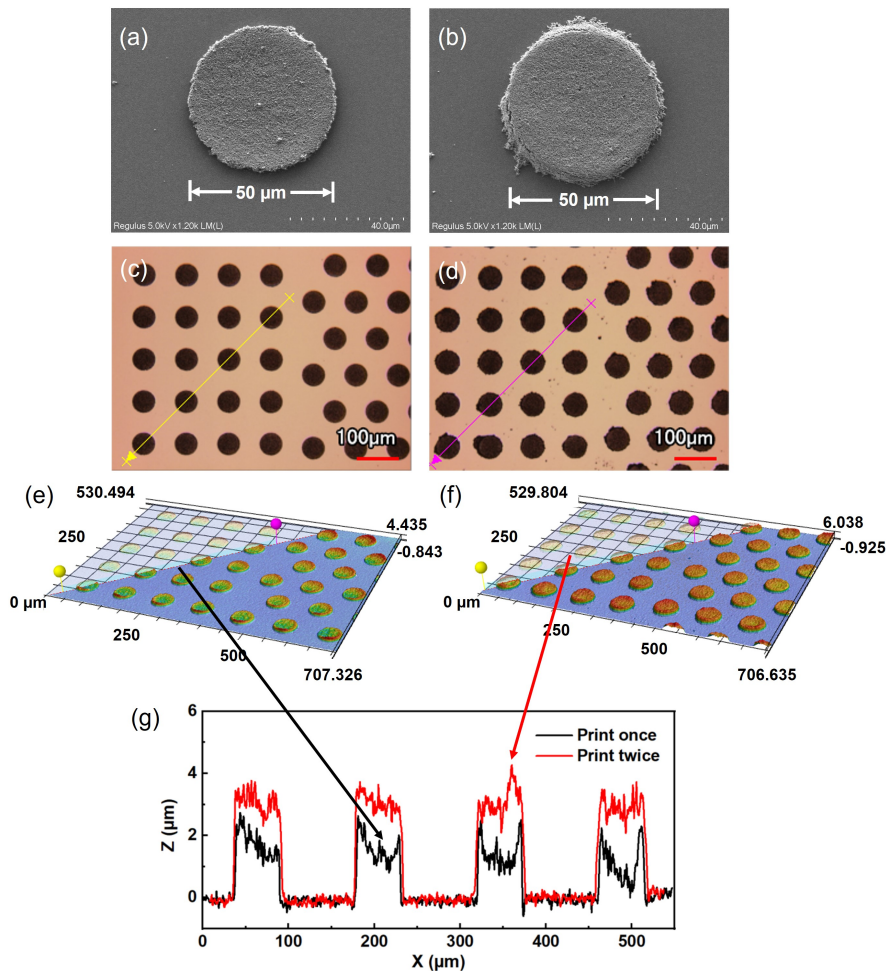


Figure 2.12: SEM images of a single CuNP bump with a 50 μm diameter by (a) single printing and (b) double printing. Optical images of transferred CuNP bumps array in 100 μm pitch by (c) single printing and (d) double printing. (e) and (f) represent the 3D image of the surface profile corresponding to (c) and (d), respectively. And (g) shows the height profile of the surface of measured CuNP bumps along the yellow and pink lines in (c) and (d), indicated by the black curve and red curve in (e) and (f).

between single and double printing for smaller opening areas, such as 20 μm , using thin photoresist. Single printing produces a cleaner substrate and prevents short-circuiting. Therefore, we recommend single printing for low-height and small-sized CuNP bumps. When working with a larger opening area of 50 μm , printing twice improves the evenness of patterned bumps and results in higher quality bumps for chip integration. In this situation, bumps can be produced by both single and double printing processes, and the decision should be made based on the specific requirements of the application.

2.4. Conclusion

This chapter explores innovative methods for transferring CuNPs in the fabrication of high-density metallic interconnects that are essential for IC integration. This exploration focuses on the LSP process, which involves using lithographically patterned photoresist as a stencil. This method played a significant role in facilitating the precise and efficient transfer of CuNPs during lift-off, leading to the creation of metallic interconnect patterns with high throughput and accuracy. The versatility of LSP in microelectronic fabrication was demonstrated by the consistent and reliable nanoparticle patterning achieved through careful optimization of both the lift-off and printing processes using CuNP paste.

By leveraging NP technology and the inherent precision of lithographic stencil masks, the optimized LSP process has demonstrated significant potential for fabricating high-quality metallic interconnects. The integration of lithography with stencil printing marks a substantial improvement over conventional methods, offering enhanced accuracy, cost-efficiency, and throughput. Furthermore, LSP provides greater flexibility in layout design, as height differences are not a critical issue due to the compressable of CuNP pillars. This compatibility with general IC manufacturing processes makes LSP a promising candidate for widespread adoption in the semiconductor industry.

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3

Lithography Stencil Printed Nanoparticle Transfer Approaches for Microbump Applications

Building on the exploration of LSP technology in interconnects fabrication, the focus is now on bonding and integration of metallic NP bumps after patterns transferring. The aim is to apply LSP method in different applications. The study investigates practical applications such as sapphire-to-silicon flip-chip interconnection and the Cu-Cu integration combined with photopatternable underfill films. Furthermore, a new approach to patterning fine details in nanoporous films produced by spark ablation is introduced, introducing new possibilities for the transfer of metallic NPs films. These developments present a promising solution for chip integration technologies in the future.

Section 3.2 has been published in: X. Ji *et al.*, IEEE ESTC Conference, 2022 [1].
Section 3.3 has been published in: X. Ji *et al.*, IEEE ECTC Conference, 2023 [2].
Section 3.4 has been published in: X. Ji *et al.*, IEEE NANO Conference, 2022 [3].

3.1. Introduction

The continuous advancement of semiconductor technologies demands new strategies to improve device performance, particularly regarding high-density μ bumps and interconnects [4]. Traditional solder-based flip-chip technology faces growing limitations related to thermal and mechanical reliability [5]. As a result, exploring alternative materials and innovative methodologies is crucial to meet the rigorous requirements of modern electronic packaging. Recent developments have underscored the potential of various interconnect materials and techniques, which offer promising improvements in performance and reliability.

This chapter will cover the LSP nanoparticle patterning technology, which is a cutting-edge approach that enables the precise transfer of metallic NPs to create fine pitch flip chip interconnects. Continuing on from Chapter 2, which centered on nanoparticle transfer technology for high-density μ bumps, this chapter explores the particular utilization of LSP in establishing fine-pitch Cu-to-Cu direct bonding. In addition to LSP, this chapter introduces an cutting-edge method for transferring metallic nanoporous films, which employs a spark ablation process followed by a lift-off technique [3]. The nanometallic transfer technique can now utilize a wider range of materials due to the precise fabrication of nanoporous metallic films through this novel approach.

During the lift-off process, well-defined nanoparticle patterns can be created using the precision of lithographically patterned photoresists as stencils in the LSP process. This method, which combines the benefits of stencil printing and lift-off techniques, addresses the critical need for improved interconnect density in 3D SiP and heterogeneous integration technologies. With nanoparticle sintering processes through TCB procedure, this technique presents a promising pathway to achieve reliable and high-performance interconnects [6][7].

In this chapter, we study various applications of LSP technology, beginning with its use in sapphire-to-silicon flip-chip interconnects, where copper nanoparticle sintering is employed to create conductive interconnects [1]. We then explore the integration of photopatternable underfill films with fine-pitch Cu-to-Cu bonding. A detailed discussion of the experimental setup and DOE highlights the

key parameters affecting the quality of the patterned interconnects, demonstrating the feasibility and effectiveness of this approach.

This chapter also presents the combination of LSP and spark ablation technology. Spark ablation allows precise deposition of nanoporous metallic films by better controlling their morphology and composition [8]. When combined with the LSP process, this method can create conductive nanoporous structures for the interconnects, especially in applications that require nanoscale metallic particles and precise feature patterning in thin films.

3.2. Sapphire to Silicon Flip Chip Interconnects by Copper Nanoparticle Sintering

Motivation

Currently, flip chip technologies rely on lead-free solder joints on copper micro bumps. The lead-free solder has a reflow temperature of 220–280 °C, which is challenging applications in a harsh environment, such as power electronics and aerospace applications. In addition, the solder joints are restricted by dimensions and height. To investigate the 3D heterogeneous integration for the state of art devices, such as silicon carbide and sapphire-based devices, the conventional solder joints may not be suitable. CuNP joint bonding technology is investigated due to its good thermal dissipation ability, mechanical property and electrical conductivity [9]–[11].

In this study, we used CuNP paste as the bonding materials. The lithographically patterned photoresist was defined as a stencil mask, combined with stencil printing, to obtain CuNP paste joints after the lift-off process. Sapphire chips were applied as the top chip, which had the advantages of higher temperature operation and UV light photonics applications, to be used in harsh environments [12]. The sintering process of CuNPs was applied at 280 °C at low pressure of 9 MPa and was performed to obtain the interconnect between the top chip and bottom substrate.

Fabrication

To implement the interconnects, two types of the wafers are prepared. One was a single side polished 525 μm silicon substrate and the other was a 650 μm sapphire wafer. The Si wafer was first insulated with 300

nm thermal oxide on both sides, and then both the Si wafer as well as the sapphire wafer were patterned with 10/100 nm Cr/Au by photolithography and lift-off. To fabricate the stacked integration sample, the Si substrate and sapphire chip were designed as 20×20 mm² dies and 10×10 mm² dies with measurement pads and interconnect patterns, respectively. As shown in Fig. 3.1a, the bottom Si substrate has fan-out interconnects measurement pads consisting of four blocks of 12 parallel Cr/Au (10/100 nm) lines with a length of 5.6 mm, and a width of 300 μm. For interconnecting, four interconnecting corners of 12 Cr/Au lines with a width of 300 μm were patterned on the topside of a sapphire chip (Fig. 3.1c) to connect the Si substrate through CuNPs. Finally, alignment pads are deposited on the backside of the sapphire chip (Fig. 3.1b) [13]. The process flow of LSP to transfer the CuNPs is depicted in Fig. 3.2.

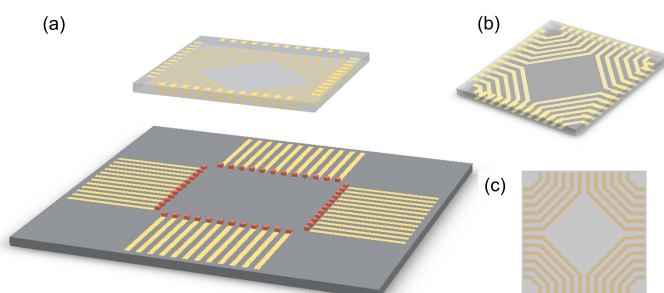


Figure 3.1: Schematic illustration of (a) 3D stacked structure of sapphire chip to Si substrate CuNP joints flip chip, (b) flipped sapphire chip with Au deposition patterns and (c) the front side of sapphire chip with the Au interconnect lines.

For the flip chip bonding process, the test Si wafer was cut into four quarters and the sapphire wafer was diced into 10×10 mm² dies. Fig. 3.1a illustrates the structure schematic of the resulting stacked flip chip. The top sapphire die was flipped and aligned under optical microscopy to stack onto the patterned Si substrate. The CuNPs were applied as squares of 260×260 μm² on the overlapping area between the upper and lower interconnect lines using the previously mentioned patterning method. After alignment, the sapphire to Si flip chip was transferred to a AML waferbonder for CuNP sintering. That bonding tool provided a high vacuum environment ($\sim 1 \times 10^{-3}$ mbar)

to prevent Cu nanoparticles from oxidation. The specimen was bonded with a pressure of 9 MPa at 280 °C for 60 min.

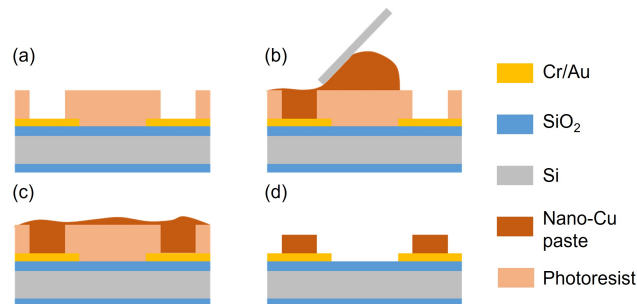


Figure 3.2: An overview of the patterns transferring process using LSP on photoresist mask and sequential lift-off process.

Inspection

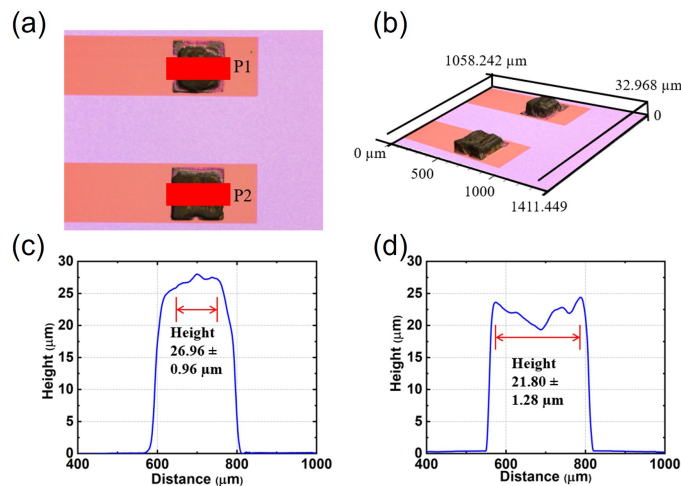


Figure 3.3: (a) Top view of microscopy image for the specimen after lift-off process, (b) 3D image of CuNP bumps after lift-off, (c) the profile of the CuNP bump indicated at P1 in (a) and (d) the profile of the CuNP bump indicated at P2 in (a).

To inspect the CuNP bump after LSP, two CuNP patterns were characterized by optical profiling and microscopy (Keyence VK-X250). Fig. 3.3a and b show 2D and 3D optical images of the CuNP bumps after lift-off. In the 2D image, due to the weak adhesion during the

lift-off process, the sides of the CuNP bump was partially lost, but the edge of the CuNP pattern on the substrate was clear, corresponding to the open area of the photoresist mask. The surface topography of the CuNP bump was observed in the 3D image, showing slight unevenness due to manual stencil printing. To estimate the average height of the CuNP bumps, 50 profile lines at intervals of 1.5 μm on P1 and P2 were characterized and averaged, represented by the red box in Fig. 3.3a. The average surface topographic profiles of P1 and P2 are shown in Fig. 3.3c and d, respectively. The border of the side-well and the top surface is selected as the boundary for calculating the average height of the CuNP bumps. The average heights of P1 and P2 are estimated to be $26.96 \pm 0.96 \mu\text{m}$ and $21.80 \pm 1.28 \mu\text{m}$, respectively. It can be observed on these shape profiles that the tops of the CuNP bumps are slightly smaller than the bottoms due to the shrinkage of CuNP paste during drying (Fig. 3.2c).

The final sapphire to Si flip chip is shown in Fig. 3.4a. The SEM images in Fig. 3.4 illustrate the bonding edge between the sapphire die and Si substrate at a 45° tilt angle. The gap between the top die and substrate was attributed to the CuNP bumps. The alignment inspection of the sapphire chip and Si surface is indicated in Fig. 3.4c, showing bare overlaying on the flip chip.

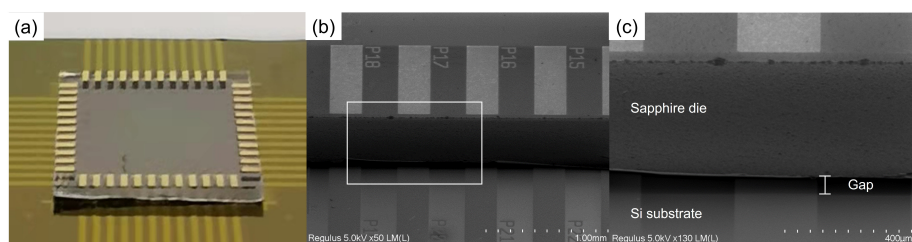


Figure 3.4: (a) Resulting specimens after bonding, image at tilted. (b) SEM image of the bonding edge at a 45° tilt angle. (c) Close-up view of the side-edge, indicated by the white box in (b), showing the alignment result and the gap due to Cu bumps.

To estimate the height of the copper bumps after the bonding process, the stacked die profile was measured at various locations on the edge of the sapphire die using Keyence. It is known that the sapphire wafer is 650 μm , hence, the CuNP bumps can be derived from the difference between the thickness of the sapphire wafer and

the measured data using Keyence. Fig. 3.5 demonstrates the distribution of CuNP bump height after measurement and calculation. The mean height and standard deviation were $21.17\text{ }\mu\text{m}$ and $2.36\text{ }\mu\text{m}$, respectively. Compared with the height information of the Cu bump before bonding ($26.96\text{ }\mu\text{m}$ and $21.80\text{ }\mu\text{m}$), the height of the Cu bump lowered to the shrinkage of the CuNP paste during sintering and the compression during bonding under pressure. After stencil printing and the sintering process, the height of the CuNP bumps was higher than that of the spin-coated photoresist ($10\text{ }\mu\text{m}$) in the first step. It was assumed that the spread amount of the CuNP paste was larger than the required amount, and there was excess coverage on the photoresist mask. Therefore, the actual thickness of CuNP bumps was not the estimated $10\text{ }\mu\text{m}$ after lift-off.

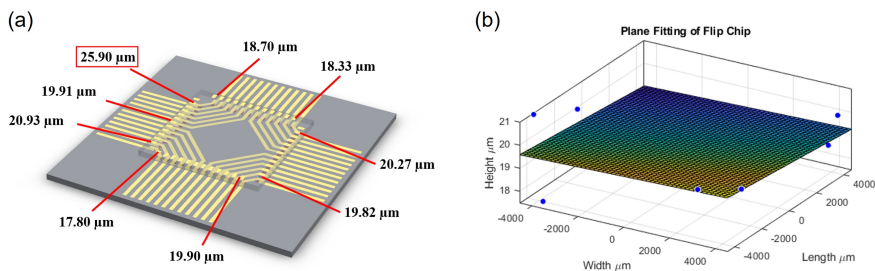


Figure 3.5: (a) Schematic of Cu bumps height distribution and the red box representing an outlier and (b) Fit plane of flip chip according to the height distribution.

In addition, the uniformity of the bonded flip chip can also be detected according to the schematic of CuNP bumps height distribution, as shown in Fig. 3.5a. It can be observed that there is only one outlier of $25.90\text{ }\mu\text{m}$ in the upper left corner, which will be calculated exclusively. The height outlier location is assumed to be an unevenness of the sapphire die and there are no other locations with a height above $20\text{ }\mu\text{m}$ nearby. The mean height and the standard deviation are estimated to be $19.46\text{ }\mu\text{m}$ and $1.07\text{ }\mu\text{m}$ without this outlier. Compared with the two adjacent CuNP bumps of $26.96\text{ }\mu\text{m}$ and $21.80\text{ }\mu\text{m}$ after the lift-off process, as indicated in Fig. 3.3, the height difference between the two CuNP bumps at different positions after bonding is much smaller. The metallic NP material is supposed

to be compressible leading to an uniform standard height after bonding. As illustrated in Fig. 3.5b, the plane fitting of this flip chip was simulated using the measured data, showing the sapphire plane was relatively flat after bonding, indicating that CuNP paste can be beneficial as a bonding material to planarize the flip chip.

3

Electrical Characterization

This specimen was designed to be interconnected by CuNP bumps through the top and bottom Au patterns, hence, the electrical resistivity is important for evaluating the 3D interconnects. The schematic of the electrical measurement setup is shown in Fig. 3.6a, indicating in the top right box, that it was a simplified four-point measurement method using four-probes to inspect the electrical contacts between the top die and bottom substrate. A forced current was applied through needle 1 and needle 2, and the voltage differences were measured by needle 3 and needle 4, the interconnection path following the red arrow. To induce the forced current, a DC voltage sweep was performed from -2 V to 2 V.

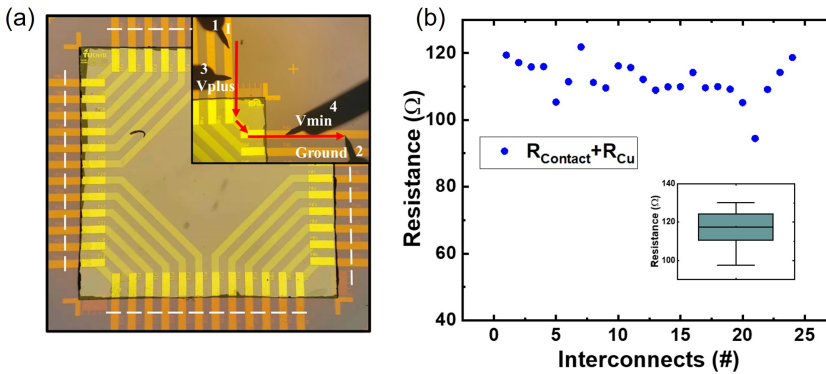


Figure 3.6: (a) Schematic of Cu bumps height distribution and the red box representing an outlier and (b) Fit plane of flip chip according the height distribution.

The Cu interconnects resistances, consisting of contact resistance between Au patterns and CuNP bumps as well as the resistance of CuNP bumps, can be estimated as:

$$R_{Cu} = \frac{V_{plus} - V_{min}}{I_{Force}} - \rho_{Au} \frac{l_{line}}{A} \quad (3.1)$$

Where ρ_{Au} is the gold electrical resistivity, which is approximately $2.44 \times 10^{-8} \Omega \cdot m^{-1}$ at room temperature, and A is the cross-sectional area of the Au line, calculated as $3 \times 10^{-8} m^2$. The Cu interconnects resistances will be derived by subtracting the total resistance of each interconnecting Au line from the resistance measured using the four-points method. Following the white dashed line, we placed needle 3 and needle 4 in the same position on each interconnect to ensure repeatability of measurements, and then obtained V_{plus} and V_{min} , respectively. The distance between needle 3 and needle 4 that current flows through the Au line, denoted by l_{line} , can be estimated in the design layout. Fig. 3.6b represents the Cu interconnects resistances of each of the 24 interconnects, each consisting of two CuNP bumps. The interconnects yield was measured to be 24 out of 24 interconnects, and the mean and standard deviation of the 24 measured Cu interconnects resistances were 117.45Ω and 6.84Ω , respectively. The mean interconnects resistances of one CuNP bump was 58.73Ω . The measured resistance of CuNP bumps is more significant than that of a bulk Cu. It can be attributed that the drying was performed in air leading to oxidation and subsequent incomplete sintering.

Conclusion

In summary, a novel method to bond sapphire to silicon was developed by applying CuNP paste joints at low temperature. The CuNP paste was stencil-printed using a lithographic defined photoresist mask. The metallic NPs enable the 3D integration of sapphire and silicon bonding. The metallic NP sintering process for bonding occurred at a low temperature of $280^\circ C$ and low pressure of $9 MPa$. The Cu nanopaste had a porous structure that was compressible after bonding, enabling the uniformity of the height of the flip chip. For one 3D interconnect structure consisting of four contact resistances between CuNP bumps and Au lines and two CuNP bumps resistances, the Cu interconnects resistances were estimated to be $117.45 \pm 6.84 \Omega$. The flip chip interconnects were repeatable, with all 24 interconnects being valid after CuNPs patterning and specimen bonding.

3.3. Fine Pitch Cu-to-Cu Direct Bonding Combining Photopatternable Underfill Films

The work on "Photopatternable Underfill Combined All-Cu Interconnects" was performed by Weiping Jiao as part of his thesis work under supervision of the author and Henk van Zeijl [2].

3

Motivation

In current studies, Cu-Cu direct bonding technology is combined with underfill technology, because it can significantly reduce the CTE mismatch and enhance the reliability of solder joint [14]. Furthermore, underfill has the advantages of improving the adhesion between chip-to-substrate (C2S) and redistributing the thermal stress to reduce the solder strain and enhance the solder joint lifetime [15]. Conventionally, capillary underfill technology is applied after the solder bonding by injecting the underfill materials in the cavity between the chip and the substrate [16]. A no-flow underfill was invented by Wong *et al.* to simplify the conventional underfill technology, when applying specific underfill materials with the properties of reaction latency and flux-ability [17]. Gilleo *et al.* proposed the molded underfill (MUF) to encapsulate the flip-chip and molding compound at the same time [18]. However, the underfill process reduce throughput and requires specialized equipment.

This report presents a novel wafer-scale all-Cu interconnecting approach using the LSP process for CuNPs patterning combined with photopatternable polymer underfill. Sample A was fabricated using regular LSP process to demonstrate the normal LSP printing capable of pattern 20 μm pitch copper nanoparticle-paste interconnects for heterogeneous integration. For improved integration reliability, sample B proof a concept that an epoxy-based photoresist was applied not only as a lithography stencil mask but also as a permanent underfill material self-aligned with patterned CuNP interconnects to combine precise patterning and underfill together.

Design and Materials

Fig. 3.7a shows a overview of the test vehicle in this experiments. We fabricated two types Si wafers, one designed as 10x10 mm² dies as

bottom wafer, and another one designed as $6 \times 6 \text{ mm}^2$ dies as top wafer, both first following the procedure for "substrate wafers" described in the previous section. Then, the substrate wafers were deposited with 300 nm Cu though sputtering and then patterned through lithography and wet etching process. The etchant solution ($\text{Na}_2\text{S}_2\text{O}_8$ (1 wt%) H_2SO_4 (0.25 wt%) H_2O) was mixed for bulk Cu etching. After CuNPs patterning procedure, the $6 \times 6 \text{ mm}^2$ chips were flipped and aligned onto $10 \times 10 \text{ mm}^2$ bottom chips to form the test vehicle containing Cu pads, redistribution layer (RDL) and CuNP interconnects.

The test vehicle is consisting of daisy chain, cross-bridge kelvin structure (CBKS) and sheet resistance with pressure and without pressure. The patterns of Cu pads are symmetrical on the top and bottom dies. For the Daisy chain and CBKS structure, the CuNP bumps form rectangles and circles with diameters of 10, 20, 40, 50, 100 μm , and the pitches of Daisy chains are 20, 40, 80, 100 and 200 μm . The sheet resistance can be measured by the Greek cross, a special Van Der Pauw (VDP) structure, in cross area of $50 \mu\text{m}^2$. To compare the sheet resistance between the pressureless and pressure-assisted sintering processes, two Greek cross structures were located outside and inside the top chip area, respectively.

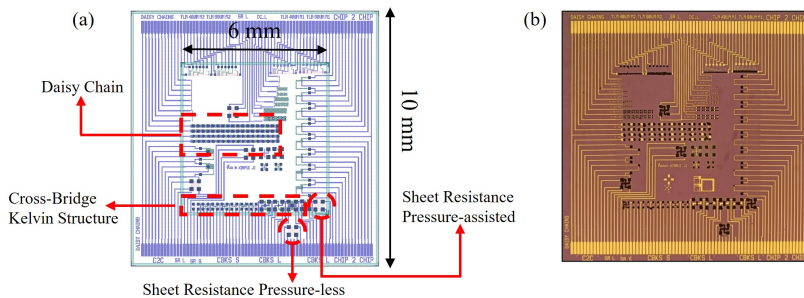


Figure 3.7: Layout of test vehicle for (a) screen shot and (b) microscopy image of CuNP patterns

Fabrication: Free-standing CuNP Joint All-Cu Interconnects

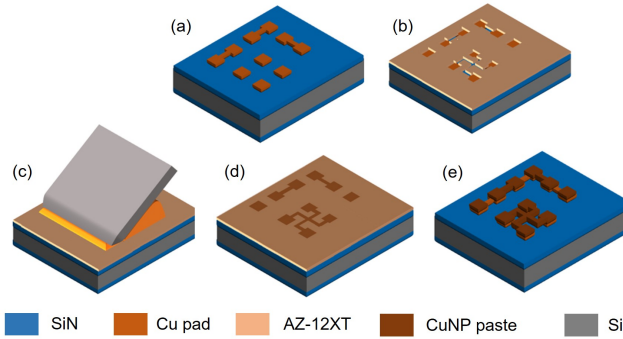


Figure 3.8: An overview of the patterns transferring process using LSP for sample B.

To investigate the LSP process on test vehicle structure, free-standing CuNP bumps were first formed on the test bottom wafer, as sample A, and the process flow is illustrated in Fig. 3.8. The photoresist was spin-coated on the test bottom wafer with the test vehicle pattern and exposed to open the areas on the Cu pads for contact with CuNPs, as shown in Fig. 3.8b. As in the LSP process described previously, on the resulting chip, CuNP patterns were in contact with the Cu pad to provide interconnections (Fig. 3.8e). Fig. 3.9a demonstrated the resulting test bottom wafer after CuNP pattern formation.

The CuNP pattern were defined by the photoresist stencil mask being derived from lithographic reticle. The patterned Greek cross sheet resistance structure is shown in Fig. 3.9b and the finest pitch approach using this method was 20 μm for both rectangular and circular CuNP interconnects, as illustrated in Fig. 3.9c and d showing 2D and 3D optical images using a 3D profilometer (Keyence VK-X250), respectively. The height of pattern was resulted from the thickness of the applied photoresist. The surface profile of 20 μm Daisy chain structure with CuNP interconnects was observed by a 3D profilometer, as shown in Fig. 3.9e, where the yellow and purple dashed line represent the horizontal height of Cu pads and wafer substrate, respectively. The height of the CuNP pillars was estimated from the height difference between the highest point of the profile and the substrate to be $8.06 \pm 0.22 \mu\text{m}$.

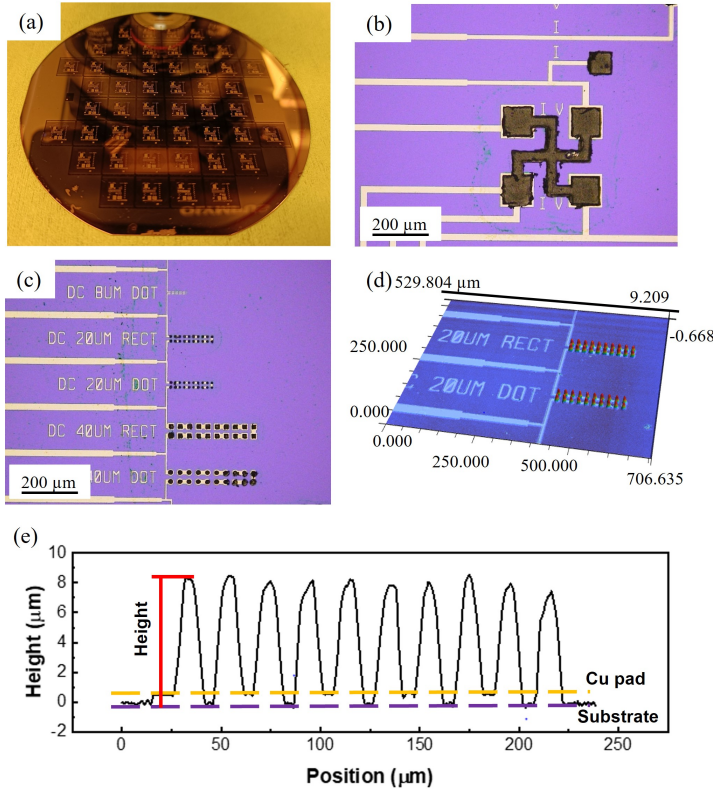


Figure 3.9: Test bottom pattern obtained after LSP process. (a) Wafer-scale CuNP pattern shown in the dark non-reflected area, (b) Greek cross CuNP pattern used for sheet resistance measurements, (c) and (d) representing the resulting 2D and 3D information, and (e) surface profile of the CuNP bumps.

Fabrication: Photopatternable Underfill Combined All-Cu Interconnects

Underfill is widely used in packaging technology, and the process is usually performed after the flip-chip pick-and-place step. To alternate the conventional underfill process, we use PermiNex® 2015 purchased from Microresist Technology, which is an epoxy-based photo-patternable photoresist, to combine the interconnect and underfill process. The PermiNex® 2015 is a negative photoresist, hence, its lithography reticle for opening contact area of CuNP pattern is inverted from the previous section. According to the previous process, we can estimate the compressed thickness of CuNPs after sintering and determine the thickness of the

photoimageable underfill layer and photolithographic stencil mask thickness.

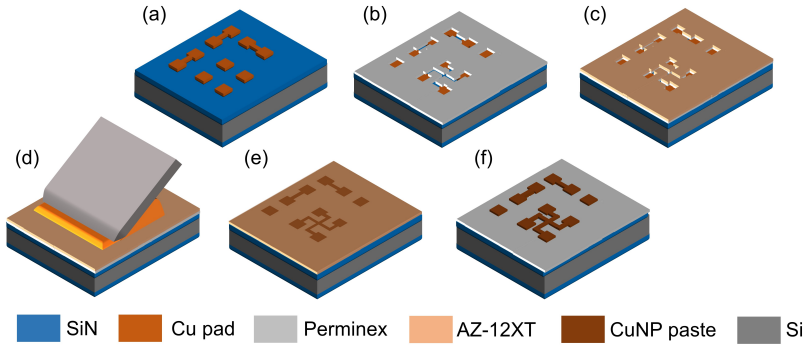


Figure 3.10: An overview of the patterns transferring process using LSP and Perminex as underfill

The process flow combines LSP and photoimageable underfill, as shown in Fig. 3.10. After the Cu pad fabrication step (Fig. 3.10a), the prepared test bottom wafer, containing the $10 \times 10 \text{ mm}^2$ chips, was first spin-coated with PermiNex® at 8000 rpm, followed by photolithography/exposure to obtain the self-aligned underfill layer (Fig. 3.10b), which can be observed under microscopy, as shown in Fig. 3.11a in viewing of $10 \times 10 \text{ mm}^2$. The laser and optical image of the Greek cross on this chip is illustrated in Fig. 3.11c, where the red arrow indicates the profile of underfill layer in Fig. 3.11e, approximately $12.8 \text{ }\mu\text{m}$. Sequentially, photoresist AZ-12XT was applied to achieve a second layer as a stencil mask layer on the underfill layer (Fig. 3.10c). Fig. 3.11b demonstrated the optical image of resulting chip after bi-layer photoresist process, where the Greek cross structure is characterized by profilometer, as shown in Fig. 3.11d. Fig. 3.11f depicts the opening contact profile of bi-layer photoresist, indicated by blue arrow in Fig. 3.11d. The depth of opening contact area for bi-layer process is approximately $19.0 \text{ }\mu\text{m}$. For the wafer with bi-layer photoresist, designated as sample B, the steps in the LSP process were repeated in this modified process (Fig. 3.10d-f).

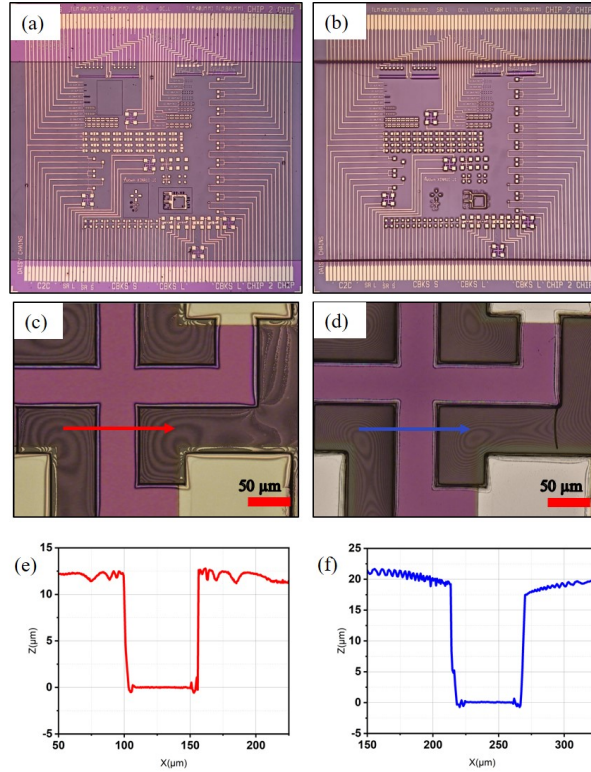


Figure 3.11: Microscopy images of (a) and (c) self-aligned underfill patterning process, (b) and (d) bi-layer photoresist patterning. (e) The profile of the thickness of PermiNex® layer indicated at the red arrow in (c) and (f) the profile of the bi-layer thickness indicated at the blue arrow in (d).

Fig. 3.12 indicates the defined CuNP patterns retained on the resulting wafer using the Perminex® underfill for sequential bonding process. Fig. 3.12a and b show the optical and laser images of specific area of the fine pitch Daisy chain structure and CBKS structure, respectively. It can be observed that the background photoresist protrudes at the area of Cu pattern. It is attributed to weak adhesion between bulk-Cu and PermiNex®. Furthermore, there is a corrugated optical reflection outside the dark CuNPs area under laser inspection due to the transparent photoresist. Hence, Keyence profilometer cannot measure the profile of CuNP bumps. We use Dektak surface Profiler to characterize the surface topography of CuNP bumps and underfill. The height between surface of underfill and the surface of CuNP patterns can be measured and indicated in Fig. 3.12c. It can be

observed that the side well is higher than the middle of the CuNPs due the shrinkage of CuNP paste during drying. The highest points between the surface of underfill and CuNP pillar are ranging from 5.47 to 7.75 μm , hence, the height of CuNP pillar using LSP combined with Perminex[®] is estimated to be $19.41 \pm 1.14 \mu\text{m}$.

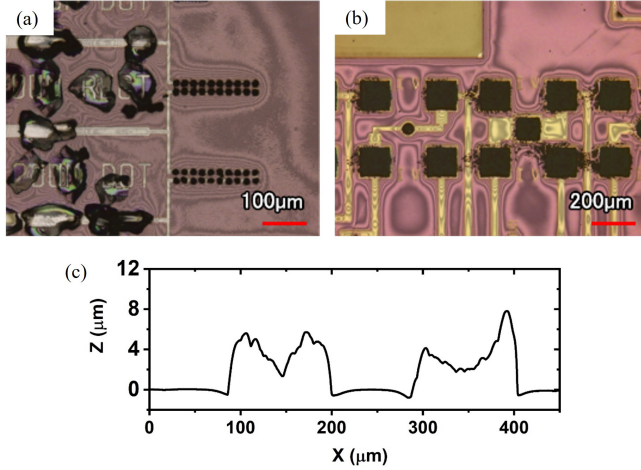


Figure 3.12: Optical and laser microscopy images of (a) Daisy chains with 20 μm pitch and (b) the CKBS structure after LSP process with PermiNex[®], and (c) the surface profile of the patterned CuNPs and underfill layer.

Sintering and Integration

Tresky die-Bonder (T-3000-PRO) was applied to align the chip-level flip-chip, and due to the limited pressure available, 1.5 MPa was applied during the bonding process with nitrogen flow. AML waferbonder was used for wafer-level bonding and provide a vacuum environment (below 10^{-3} mbar) to prevent CuNPs from oxidation.

The sintering parameters of this experiment are demonstrated in Table 3.1. First, the top wafers with Cu pad patterned $6 \times 6 \text{ mm}^2$ sized of chip were flipped and aligned with samples A and B using AML-Bonder and Tresky die-Bonder. The sample A without underfill layer was treated at the temperature of 280 $^{\circ}\text{C}$ under 1.5 MPa for 1 hour. And the stacked sample B with CuNP pattern combining with Perminex[®] layer was bonded with a pressure of 1.5 MPa at 220 $^{\circ}\text{C}$ and 280 $^{\circ}\text{C}$ for 1 hour, as illustrated in Fig. 3.13a and c. The bonded dies is depicted in Fig. 3.13b.

Table 3.1: Sintering process parameter

Parameter	Sample A	Sample B	
Pressure (MPa)	1.5	1.5	1.5
Temperature (°C)	280	220	300
Time (min)	60	60	60

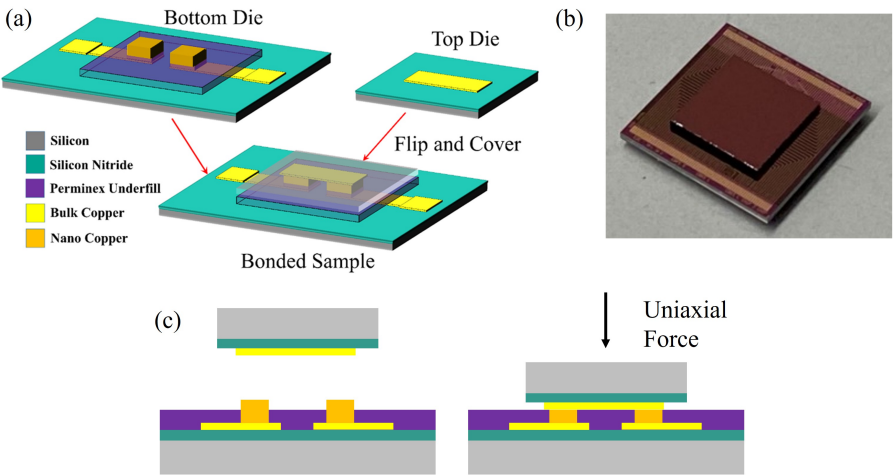


Figure 3.13: (a) A schematic of Cu NP joint integration, illustrating a bottom die with photoimageable underfill and patterned CuNP interconnect as well as a top die with Cu pad. (b) The stacked dies with underfill. (c) Sketch of cross-section, showing the top- and bottom-dies were aligned and bonded using thermal-compression bonding.

Measurement

The electrical property plays an important role in CuNP joint interconnects. As previous sections described, the contact resistance is the key parameter to CuNP joint integration interconnects. In this experiment, the resistance of the sintered CuNPs was measured by a Cascade Microtech probestation. The contact resistance is measured on the sample C coated with Perminex[®] and bonded at 1.5 MPa at 220 °C and 300 °C. After LSP process, the CBKS's were formed to characterize bulk-Cu on the bottom substrate, CuNPs film and bulk-Cu on the top substrate contact resistances using four-point measurement. The specific contact resistances were calculated by measuring the contact resistance for contact area sizes of 50×50 μm²

and $100 \times 100 \mu\text{m}^2$, as depicted in Fig. 3.14a. The test CBKS structure is indicated in Fig. 3.12b. With the increase of sintering temperature from 220°C to 300°C , the specific contact resistances of $50 \times 50 \mu\text{m}^2$ and $100 \times 100 \mu\text{m}^2$ decreased rapidly from $1.4 \times 10^{-5} \Omega \cdot \text{cm}^2$ to $4.6 \times 10^{-6} \Omega \cdot \text{cm}^2$ and $4.6 \times 10^{-5} \Omega \cdot \text{cm}^2$ to $1.0 \times 10^{-5} \Omega \cdot \text{cm}^2$, respectively. For low pressure sintering process, the sintering temperature plays an important role to determine the specific contact resistance.

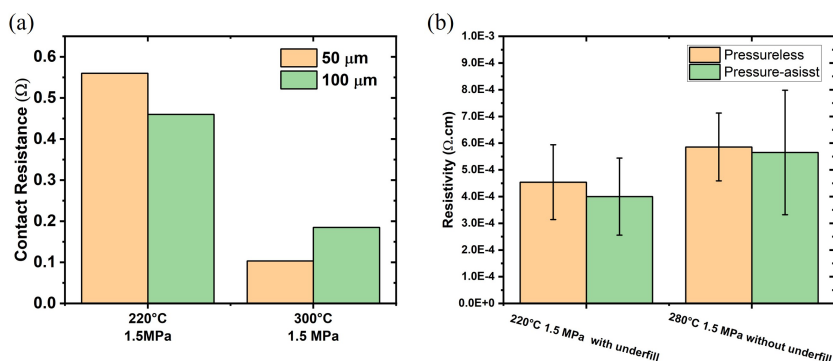


Figure 3.14: (a) Specific contact resistance of bulk-Cu/CuNP/bulk-Cu sandwich structures at different sintering temperature at bonded pressure of 1.5 MPa. (b) The resistivity of different process with and without underfill under different sintering parameters

Greek cross structures were to characterize the sheet resistance and resistivity of sintered Cu nanoporous patterns using LSP methods with underfill and without underfill. The width of Greek cross is designed as $50 \times 50 \mu\text{m}^2$ and the CuNPs thickness of bonded samples with and without underfill were measured to be approximately 8.06 and 19.41 μm , as mentioned in previous sections. There were two Greek crosses on the test structure, one in the area covered by the top die, providing pressure-assisted sintering, and the other in the area without the top die applying pressure, which was pressure-free sintering, as mentioned in Fig. 3.7a.

Fig. 3.14b illustrates the average resistivity illustrates the average resistivity during pressure-less and pressure-assisted processes, indicated by orange and green columns. For the experiments with and without underfill, the resistivity of CuNPs in the pressure-assisted sintering process is significantly lower than that in the pressure-free process, and the pressure aids the sintering process. It can be

observed that when sintered at 1.5 MPa, the resistivity of the bonded sample with underfill sintered at 220 °C is $4.54 \times 10^{-4} \Omega \cdot \text{cm}$, which is lower than the resistivity of $5.86 \times 10^{-4} \Omega \cdot \text{cm}$ for the bonded sample without underfill at 280 °C. It is attributed to the underfill layer is benefit to planarize the top and bottom substrates and assists in sintering during bonding at lower temperature and pressure. Compared to the resistivity of bulk-Cu of $1.7 \times 10^{-6} \Omega \cdot \text{cm}$, the sintered CuNPs with underfill is more than 200 times larger.

Conclusion

In this work, the CuNPs were applied for the interconnects the patterning process was investigated to enhance the flip chip integration applying for 3D integration. The heights of interconnects are determined by the thickness of applied photoresist. It is feasible to combine epoxy-based photoresist film and LSP process for precise patterning, controllable interconnect height and underfill. The LSP process can provide uniform interconnect heights with different joint sizes.

The specific resistance of sintered CuNPs using photoimageable underfill process depends on the sintering temperature, when characterizing sample B. Low specific resistance of bulk-Cu/CuNPs/bulk-Cu sandwich structure are obtained at sintering temperature 220 °C and 300 °C. The higher sintering temperature results in lower specific resistance at sintering pressure of 1.5 MPa.

The electrical resistivity of sintered CuNPs is two order larger than that of bulk-Cu, due to oxidation issues and porous structure of sintered CuNPs. Comparing sample A and B at a sintering temperature of 220-280 °C at a bonding pressure of 1.5 MPa, the underfill combination process facilitates the sintering process to reduce the resistivity. And the resistivity of pressure-less sintered CuNPs is higher than that of pressure-assisted sintered CuNPs. The bonding pressure is also a key parameter of sintering process.

3.4. Patterning of Fine-features in Thin Nanoporous Films Synthesized by Spark Ablation

Motivation

In this study, we fabricated nanoporous structures using the lift-off method. The generation of the nanoporous film relies on the synthesis of nanoparticles through spark ablation between two opposing electrodes [8][19]. Unlike wet chemical methods for nanoparticle synthesis, this approach requires no additional chemicals beyond the metallic electrodes and carrier gas. Notably, it offers high flexibility in material selection by allowing different electrode metals. Spark ablation can be applied to pure metals, alloys, and certain semiconducting materials.

To deposit the generated aerosol, we employed an inertial impaction printer developed by VSPARTICLE B.V. This printer enables contactless, chemical-free, maskless, and local deposition [13]. The thickness of the nanoporous film and the size of the nanoparticles can be tuned by adjusting synthesis or printing parameters [19]. By combining the strengths of both methods, lift-off of directly written nanoparticles achieves fine resolution, sharp edges, minimal metal waste, and enables wafer-level printing of complex nanostructured deposits.

In our specific work, we patterned Au and ZnO nanoparticle deposits using the lift-off technique. The lithographically defined patterns were tested down to a resolution of 2 μm . We investigated their microstructure and compatibility with different substrates, as well as measured their conductivity.

Experimental Setup

Fig.3.15 illustrates a schematic diagram of our nanomaterial direct-write system, which exhibits high accuracy and consistency. The system comprises a VSP G1 spark discharge generator and a Proto-0 Nanomaterial Printer, both developed by VSParticle B.V. We utilized pure N_2 (99.999%) gas as the carrier gas, flowing at a rate of 1.5 L/min. To achieve adequate production rates, we set the spark conditions to 8 mA and 1 kV for Au and 4 mA and 1 kV for ZnO.

Two opposing electrodes, consisting of Au (99.99%) and doped Zn (99.95% Zn, 0.05% Al), were ablated to generate a nanoparticle aerosol. This aerosol was then transported to a printing chamber operating at a vacuum pressure of less than 1 mbar. The pressure difference across the nozzle accelerated the gas, causing the

nanoparticle aerosol to impact the substrate. By combining this process with an xyz-orientable stage, we achieved the capability to directly write nanoporous structures in three dimensions. For this study, we utilized a nozzle with a flow rate of 0.99 L/min. It is important to note that the clean surface of these nanoparticles renders them highly sensitive to oxidation. When exposed to oxygen, the Zn component rapidly oxidizes, forming ZnO. We deposited rectangular patterns by printing several parallel lines approximately 1 mm in width, with a spacing of 0.1 mm, resulting in an overlap between adjacent lines.

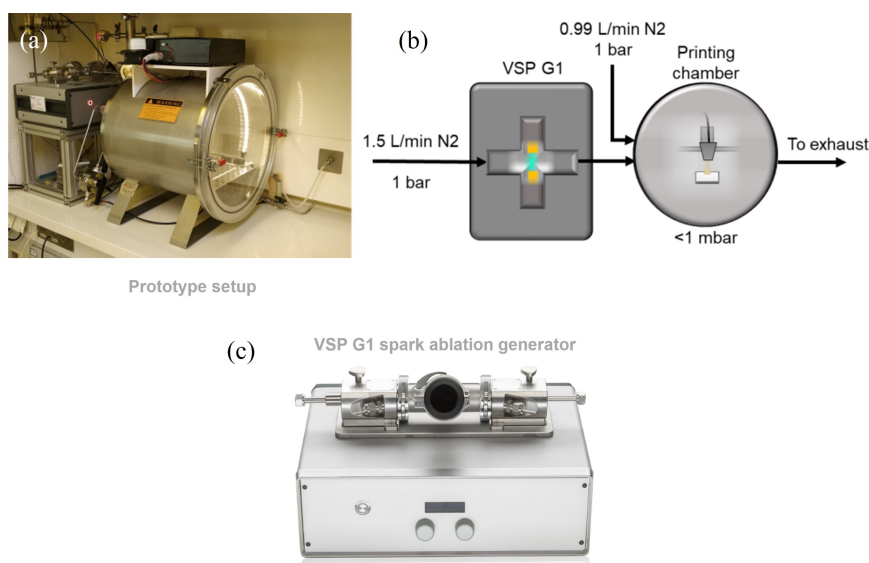


Figure 3.15: (a) Photograph of the nanomaterials printer. (b) A schematic diagram showing the major components and gas flow. (c) VSP G1 spark ablation generator

Fabrication

Photolithography was utilized to define patterns for wafer-level processing. The fabrication process for fine nanoporous patterns on a 525 μm p-type Si wafer is depicted in Fig.3.16. Initially, a 190 nm low-stress silicon oxide (SiO_2) layer was deposited using LPCVD, followed by sputtering a 25 nm thin Titanium (Ti) layer for adhesion, which oxidizes fully in ambient air to form TiO_2 . Subsequently, an 8.5 μm 12XT-20PL series photoresist was spin-coated onto the surface, as shown in Fig.3.16a. After exposure and development of the

photoresist, a patterned surface structure was obtained.

The cured photoresist then served as the mask for the lift-off process. As illustrated in Fig.3.16b, a nanoporous film was directly written on the surface. Following this, the wafers with printed films, shown in Fig.3.16c, were immersed in a beaker filled with NMP for photoresist stripping in an ultrasonic bath at room temperature for 30 seconds. Finally, the fabrication process was completed with DI water rinse and drying, as depicted in Fig. 3.16d.

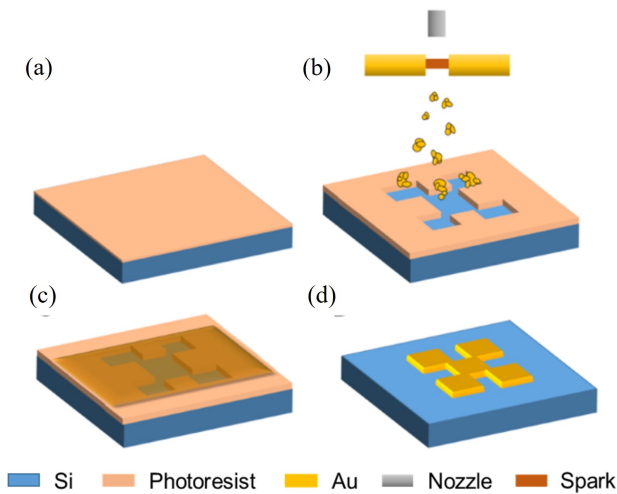


Figure 3.16: An overview of fabrication process: (a) Photolithography; (b) NPs synthesis using spark ablation; (c) Nanoporous film formation and (d) Lift-off process.

Inspection

The test structure in this experiment can be seen in Fig. 3.7a and b where the photoresist mask with patterns created by photolithography. We selected a VDP structure to analyze the patterned photoresist mask, which is estimated at $8.5\ \mu\text{m}$ in thickness as demonstrated in Fig. 3.7d. Because the photoresist is positive, it exhibits top-cut walls.

The printed surfaces of the Au nanoporous films are depicted in Fig.3.18a through a series of pitch resolution check patterns. The photoresist and NPs were removed by the lift-off process, leaving only the patterns on the Ti substrate. Fig.3.18b displays the resulting patterns, the resulting patterns after lift-off process, indicating

successful photoresist removal and an absence of remarkable residues on the surface. Fig.3.20 depicts the Au nanoporous patterns before and after lift-off in various sizes of VDP structures.

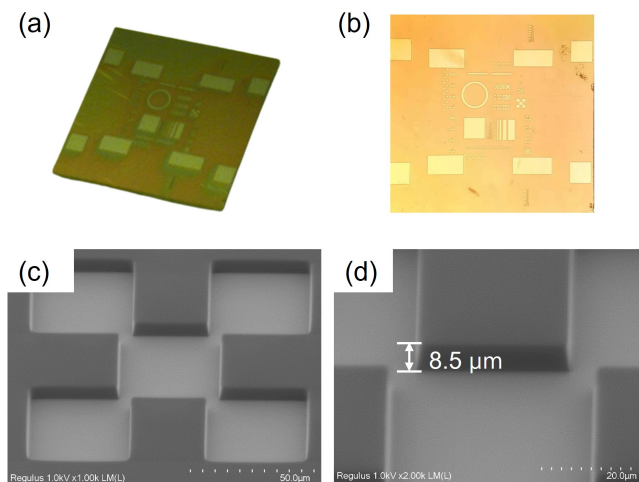


Figure 3.17: Photoresist mask design

The printed surfaces of the Au and ZnO nanoporous films are depicted in Fig.3.18a and Fig.3.19a through a series of pitch resolution check patterns, respectively. The photoresist and NPs were removed by the lift-off process, leaving only the patterns on the Ti substrate. Fig.3.18b and Fig.3.19b displays the resulting patterns, the resulting patterns after lift-off process, indicating successful photoresist removal and an absence of remarkable residues on the surface. Fig.3.20 and Fig.3.21 depict the Au and ZnO nanoporous patterns before and after lift-off in various sizes of VDP structures.

Fig.3.18c and d display close-up views of regions indicated by the blue and green boxes in Fig.3.18b, respectively, showing the achieved resolution for nanoporous film strips with high and low length-to-width ratios. For high aspect ratio patterns, the NPs film remained in the gap between the two strips when the gap distance exceeds 5 μm , while the strips rolled inward when the gap being below 5 μm . However, for patterns with low length-to-width ratios, a resolution of 5 μm for the gap and 4 μm for the strip width can be achieved. This phenomenon is attributed to the large accumulation of NPs stuck on the sidewall of the photoresist pattern. Nanomaterials

are able to connect between two fine strips over the photoresist mask due to the top-cut wall, which makes it hard to remove during the lift-off process, especially for long and fine structures.

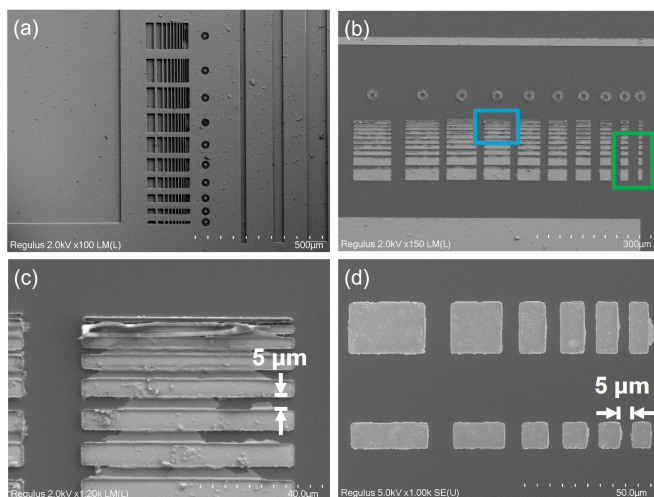


Figure 3.18: SEM images showing the pitch resolution of nanoporous Au patterns: (a) before lift-off, and (b)-(c) after lift-off. (c) Close-up view of the achieved resolution, marked by the blue box in (b). (d) Closed-up view of achieved resolution marked by the green box in (b).

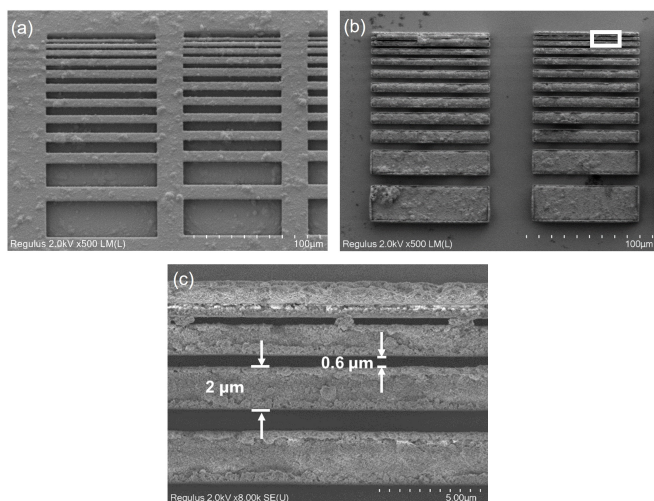


Figure 3.19: SEM images showing the pitch resolution of nanoporous ZnO patterns: (a) before lift-off, and (b)-(c) after lift-off. (c) Close-up view of the achieved resolution, marked by the white box in (b).

Zooming in on the area marked by white box in Fig.3.19b, Fig.3.19c reveals that the resolution limitation by lithography used to pattern the photoresist, with the finest gap measuring $0.6\ \mu\text{m}$ and the finest film strip measuring $2\ \mu\text{m}$.

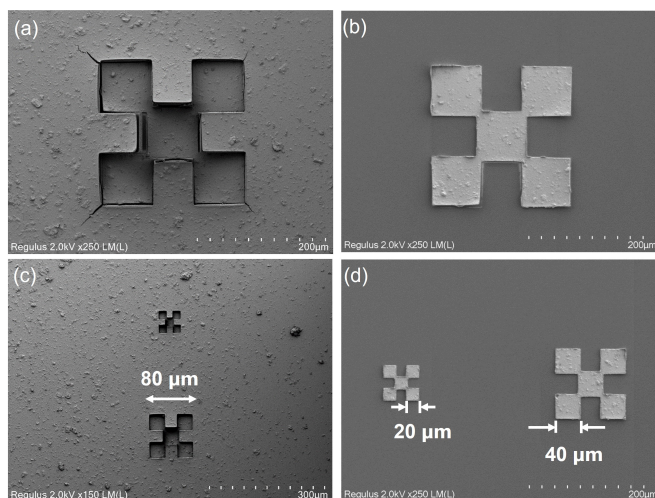


Figure 3.20: SEM images of VDP structure patterned by Au NPs in various size for electrical conductivity measurement: (a)(b) before lift-off; (c)(d) after lift-off.

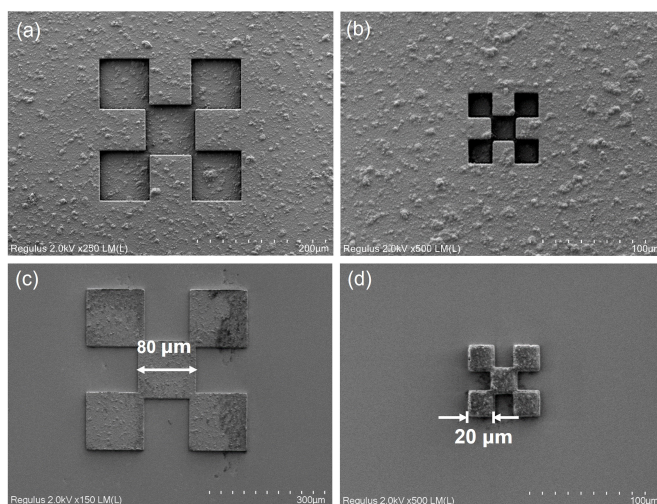


Figure 3.21: SEM images of VDP structure patterned by ZnO NPs in various size for electrical conductivity measurement: (a)(b) before lift-off; (c)(d) after lift-off.

Measurement

The VDP structures, serving as functional patterns and characterized in Fig. 3.22, display distinct edges in both the Au nanoporous films. Dark regions visible in Fig. 3.22a of the optical image indicate the presence of large nanoparticle aggregates, significantly exceeding the film thickness. In order to determine the average height of the nanoporous film, we measured and averaged 100 lines at intervals of $0.5\ \mu\text{m}$, as shown in the red area on Fig. 3.22a. The height profiles reveal a relatively flat surface for both samples, with the Au nanoporous film averaging a thickness of $1.24\ \mu\text{m}$.

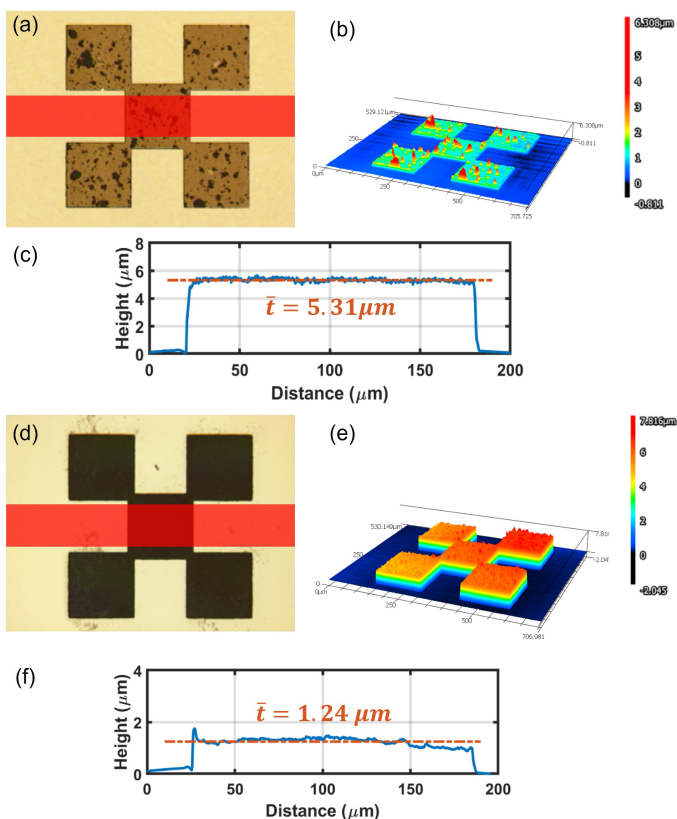


Figure 3.22: VDP structures and height profiles are illustrated for both Au (top) and ZnO (bottom): (a)(d) Top views; (b)(e) 3D views; (c)(f) The height profiles of the VDP structures, along with corresponding profiles of the red areas, represent the averages of 100 lines spaced $0.5\ \mu\text{m}$ apart.

The VDP structures, serving as functional patterns and characterized in Fig. 3.22, display distinct edges in both the Au and ZnO nanoporous films. Dark regions visible in Fig. 3.22a of the optical image indicate the presence of large nanoparticle aggregates, significantly exceeding the film thickness. In order to determine the average height of the nanoporous film, we measured and averaged 100 lines at intervals of $0.5\ \mu\text{m}$, as shown in the red area on Fig. 3.22a and d. The height profiles reveal a relatively flat surface for both samples, with the Au nanoporous film averaging a thickness of $1.24\ \mu\text{m}$ and the ZnO film thicker at $5.31\ \mu\text{m}$.

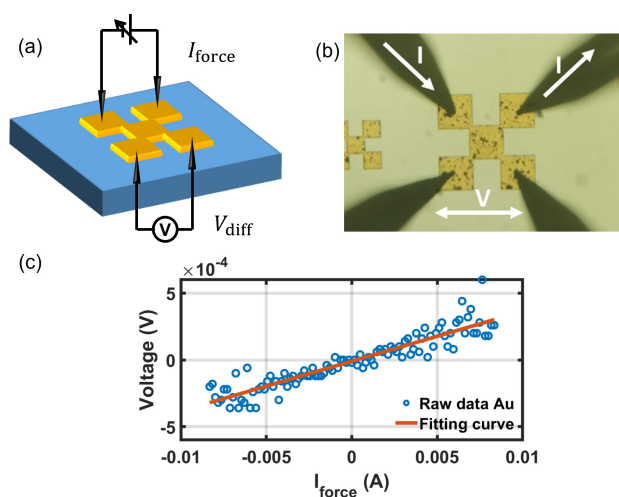


Figure 3.23: (a) Schematic of a VDP measurement, (b) measurement setup observed under microscopy and (c) the I-V response.

In this study, patterned square Van der Pauw structures were employed to determine the resistivity of the nanoporous film. This section only shows the resistivity of Au nanoporous films. The measurement schematic is depicted in Fig. 3.23a and b. Contact resistance was eliminated by measuring the voltage difference and current across the bottom contacts, which were applied to the adjacent topside contacts. A current was generated by applying a voltage sweep that ranged from -0.5V to 0.5V to the Au nanoporous film. The resulting I-V curve demonstrates good linearity, as shown in Fig. 3.23c. The slope of the linearly fitted line was used to determine

the resistance. Finally, the resistivity of the fabricated nanoporous film was calculated using the following equation:

$$\rho = 4.532 \cdot t \cdot R \quad (3.2)$$

Where t is the film thickness and R is the resistance measured.

Considering the measured thickness of 1.24 μm , the Au nanoporous sample exhibits a resistivity of $2.07 \times 10^{-5} \Omega \cdot \text{cm}^{-1}$. This value is approximately 8.52 times higher than the bulk resistivity of Au ($2.44 \times 10^{-6} \Omega \cdot \text{cm}^{-1}$), which can be primarily attributed to its porous structure. Their application can be varied based on their material characteristics. The nanoporous films resistivity can be improved with additional thermal treatment to enhance the degree of sintering. As a result, we developed a nanofabrication process flow that is a viable approach for producing nanoporous films, allowing for significant flexibility in material selection.

Conclusion

We developed a novel nanofabrication method for fabricating a nanoporous film using lithography stencil printing method. Au and ZnO nanoporous films were synthesized by using spark ablation and locally written on photoresist patterned Ti/TiO₂ substrate. Subsequently, a lift-off process was applied to pattern nanoporous films. The fabricated nanoporous film exhibited heights of 1.24 μm for Au and 5.31 μm for ZnO, with ZnO achieving the finest patterned gap width of 0.6 μm and a line width of 2 μm . Furthermore, the resistivity of the resulting Au nanoporous film was measured to be $2.07 \times 10^{-5} \Omega \cdot \text{cm}^{-1}$, which is 8.5 times its bulk state. As a result, We have been able to produce precisely defined Au and ZnO nanoporous films. This achievement provides a promising approach for the mass production of nanoporous film-based structures using various materials.

3.5. Conclusion

The novel methods for transferring metallic NPs were developed to achieve metallic interconnects that facilitate device interconnection. Utilizing lithographically patterned photoresist as a stencil enabled the precise transfer of metallic NPs during the lift-off process,

resulting in accurate patterns. This innovative technique is referred to as the LSP process, which has the potential for high throughput and high resolution.

In this chapter, several applications were presented to validate the feasibility of the LSP process for metallic NP joint interconnects. A method to bond sapphire to silicon using CuNP paste joints at low temperature was developed. The CuNP paste was stencil-printed using a lithographically defined photoresist mask. The metallic NPs enable the 3D integration of sapphire and silicon bonding.

A novel wafer-scale all-Cu interconnecting approach using the LSP process for CuNPs patterning was also combined with photopatternable polymer underfill. The epoxy-based photoresist was applied not only as a lithography stencil mask but also as a permanent underfill material self-aligned with the patterned CuNP interconnects. This approach combined precise patterning and underfill together.

Furthermore, a novel nanofabrication method was developed for fabricating nanoporous films using spark ablation and the lift-off technique. Au and ZnO nanoporous films were synthesized and locally written on photoresist patterned Ti/TiO₂ substrates. However, due to the oxidation of metal particles during the process, ZnO formation is caused by the oxidation of metal particles during the process, resulting in Zn spark ablation. To achieve pure metallic nanoporous structures, it is recommended to use a nitrogen gas environment in the chamber. The lift-off process was applied to pattern the nanoporous films, achieving fine resolution down to 2 μm . The fabricated nanoporous films exhibited resistivities of $2.07 \times 10^{-5} \Omega \cdot \text{cm}^{-1}$ for Au and $1.54 \times 10^{-4} \Omega \cdot \text{cm}^{-1}$ for ZnO, demonstrating the capability of this method for producing precisely defined nanoporous structures. This novel approach enables the precise production of nanoporous metallic films, broadening the applicability of these materials in various high-technology domains, including sensor technologies and advanced electronics. The spark ablation method serves as a complementary technique to stencil printing, providing additional flexibility in fabricating structures with desirable nanoporous characteristics.

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4

Mechanical and Electrical Performance Characterization of Sintered Cu Bumps

CuNPs sintering for flip-chip interconnects is a promising solution for 3D and heterogeneous integration to overcome the limitation of solder materials. To this end, we perform the LSP method to pattern CuNPs, and the form of flip-chip interconnects is completed after CuNP sintering process. This paper aims to study the effect of sintering processing parameters (time, pressure, temperature) on the mechanical properties of CuNP bumps when applying the novel method to approach the Cu interconnects. We fabricated seven groups of specimens of sintered CuNP bumps, built with a diameter of 100 μm and sintered. The nanoindentation tests assessed the mechanical property to get Young's modulus and hardness. Results clarify that Young's modulus is strongly affected by pressure. An suggested combination of parameters (the 25 MPa and 260 °C for 15 minutes) give the highest modulus of 126 GPa and the hardness of 1.76 GPa. Moreover, the observations by SEM reveal the microstructure and porosity evolution versus different processing parameters.

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4.1. Introduction

Recently, CuNP sintering technology has been developed for flip-chip packaging but has been widely used in die-attach technology. For nanosilver sintering, shear strength is commonly used to characterize the mechanical properties [2]–[4]. Similarly, Zhang *et al.* [5] studied the effect of the process parameter on the in-air sintering CuNP paste in high-power electronics. Maximum shear strength is obtained at in-air sintering parameters of 240 °C, 25 MPa, and 3 min, being 41.63 ± 4.35 MPa. Liu *et al.* [6] also investigated the influence of sintering parameters in the N₂ atmosphere, and the best die shear strength was 116 MPa when the die was sintered at a temperature of 250 °C and a pressure of 30 MPa for 3 min. The sintered CuNPs are mainly used as the die-attach materials in high-power devices. In the last decade, a few works investigated the mechanical reliability of CuNP joint flip-chip through shear tests [7]–[9]. Moreover, the microstructure-related mechanical properties of sintered CuNPs are crucial for studying interconnects reliability in flip-chip integration.

Nanoindentation is commonly used to investigate the mechanical properties of nanoscale materials. Some valuable information can be derived from the load-displacement curve, such as elastic modulus and hardness. As reported in [10], elastic modulus, yield stress and hardness are crucial in terms of mechanical reliability. Nanoindentation can be used as a measurement technique to assess all of these properties. The mechanical properties of nanoporous materials were characterized through the load-displacement curve by the nanoindentation test [11]–[14]. Fan *et al.* [15] reported the high-temperature deformation behaviors of sintered CuNPs using the nanoindentation test. The continuous stiffness measurement (CSM) technique has recently significantly improved the conventional nanoindentation test, which can directly measure the dynamic contact stiffness and accurately observe the micro/nanoscale deformation during indentation loading [16]. Fakiri *et al.* [17] proposed that the mechanical properties of porous materials at micro- and nanoscale can be determined through nanoindentation using the CSM method. The nanoindentation test enables multi-point testing of different CuNP bumps on a sample with a specific sintering parameter to characterize the mechanical properties of the nanostructure. Once sintered at relatively low

temperatures, the sintered material properties approach that of the bulk materials, enabling the integration of high melting materials into chip assembly.

In this chapter, nanoindentation tests are performed to investigate the mechanical properties of CuNP bumps. Seven groups of specimens under different processing parameters, including sintering time, pressure and temperature, are fabricated. An optimal combination of processing parameters related to Young's modulus and hardness is proposed. Based on the SEM observation and analysis of porosity, the relationship between microstructure evolution and processing parameters is revealed and discussed.

4

4.2. Experimental Section

4.2.1. CuNPs

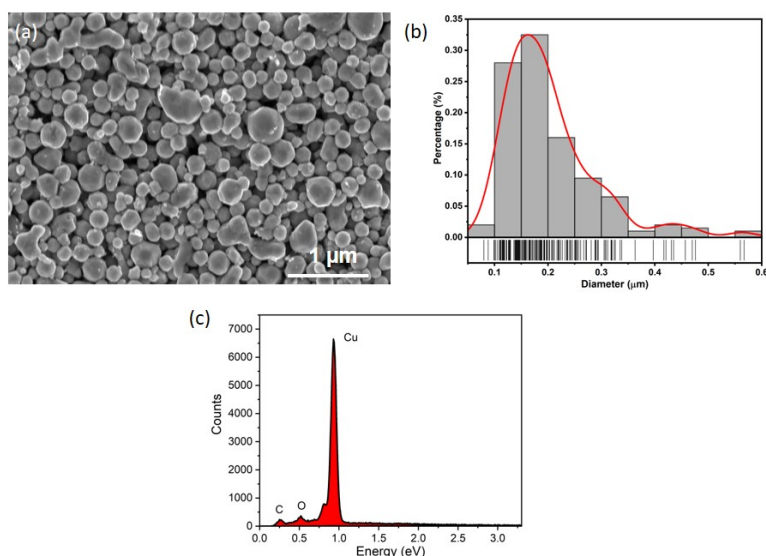


Figure 4.1: A SEM image of CuNPs before sintering.

In this study, an in-house produced CuNP paste was applied to fabricate CuNP bumps for flip chip integration. To characterize the CuNPs before sintering process, a thin layer of the CuNP paste was first spread on the substrate and then dried for 15 min at 110 °C in air.

The morphology of CuNPs was observed by scanning electron microscopy (SEM, FEI Helios G4 CX), as shown in Fig. 5.1(a). The size distribution of as-treated CuNPs was counted on the SEM images using image processing software (ImageJ), as illustrated in Fig. 5.1(b). The majority of CuNPs have a diameter of about 100 nm to 300 nm with a spherical shape. The composition of the CuNP was investigated using EDX (AMETEX) to show the detailed information of the CuNP paste. Fig. 5.1(c) shows the EDX result at the position indicated in the corresponding Fig. 5.1(a), observing the NPs are predominantly copper and have not been oxidized during preservation and pretreatment.

4

4.2.2. Test CuNP Bumps Fabrication

It is well known that stainless steel foils are commonly used as stencil masks to pattern paste-based materials in the industry. The pattern size of the conventional stencil is limited by the product technique, therefore, LSP enables the patterning and definition of CuNP patterns at the wafer level, with the advantages of high throughput and high resolution. During LSP process, the photoresist acts as the stencil mask and a photoresist lift-off process is applied to remove the photoresist stencil and excess CuNP paste.

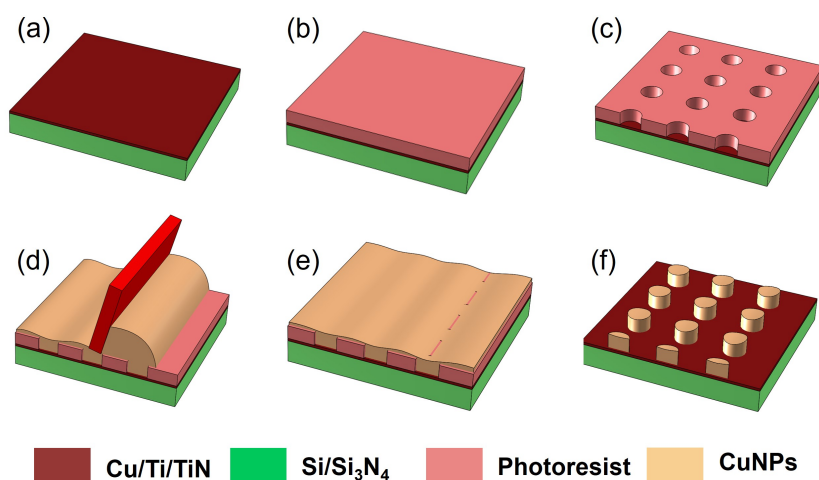


Figure 4.2: Fabrication process of test CuNP bumps.

To implement the flip chip interconnects, we designed an array of 200 μm pitch CuNP interconnects with the diameter of 100 μm on $10\times 10\text{ mm}^2$ dies. We prepared a double side polished 500 μm silicon (Si) wafer and the sample fabrication process is illustrated in Fig. 4.2(a). The Si wafer was first insulated with 300 nm low-pressure silicon nitride (SiNx) by LPCVD to protect the Si substrate from copper diffusion. Then, a 300 nm Cu conductive layer and a 2/25 nm Ti/TiN adhesion layer were deposited on the prepared Si wafer using sputtering deposition (Trikon Sigma 204 Dealer). Subsequently, a 10 μm positive photoresist (AZ[®] 12XT-20PL) was spin-coated on the substrate. The photoresist was exposure (ASML PAS 5500/80 waferstepper) and developed to obtain an array of opening holes with a diameter of 100 μm , as shown in Fig. 4.2(c). Then, a small quantity of CuNP paste was dispensed and manually distributed by a silicon squeegee on the test wafer. The test wafer was dried in an oven at 80 °C for 10 minutes for the next step. The step in Fig. 4.2(d) and (e) was repeated to improve the uniformity of patterned CuNPs, a small additional amount of CuNP paste was evenly applied again on the test wafer to dry at 110 °C for 15 min.

In the subsequent photoresist lift-off process, the prepared wafer was immersed in N-methyl-2-pyrrolidone (NMP) and stirred at room temperature to strip the photoresist. After rinsing with DI water and drying steps, the 100 μm CuNP bumps array remained on the substrate of the process wafer. The resulting wafer after LSP process was diced into $10\times 10\text{ mm}^2$ chips, and the remaining CuNP bumps were observed and estimated using the 3D profilometer (Keyence VK-X250).

4.2.3. Sintering of CuNP Bump

To fabricate the stack integrated sample for sintering process investigation, the bare Si wafer was diced into $6\times 6\text{ mm}^2$ dies, which were then flipped and placed onto $10\times 10\text{ mm}^2$ chips with CuNP patterns. The pressure-assisted sintering process was performed by a wafer bonder (AML-AWB-04 waferbonder) in a high vacuum environment ($<1\times 10^{-3}$ mbar) to prevent oxidation of CuNPs. Fig. 4.3(a) depicts a schematic of the cross-section of the flip chip bonding setup for CuNP interconnects. The top and bottom bonding plates applied temperature (220-300 °C), time (15-60 min) and pressure (20-30 MPa) to the stacking chips. The DOE for the

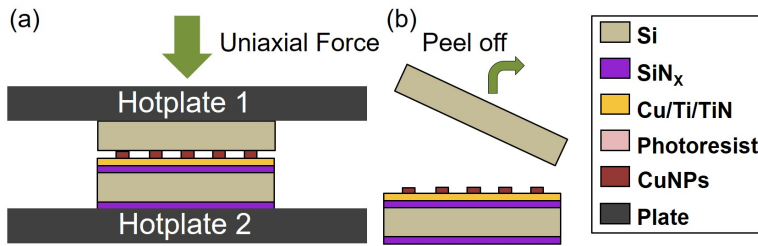


Figure 4.3: Schematic of CuNP pressure-assisted sintering bonding process and the samples fabrication for nanoindentation test.

4

pressure-assisted sintering process in this study is shown in Table 4.1. After sintering process, the top Si die was easily peeled off from the bottom die and the CuNP bumps were retained, as illustrated in Fig. 4.3(b). Finally, the resulting samples with sintered CuNP bumps were used for the nanoindentation test.

Table 4.1: DOE for sintering process parameter study

NO.	Pressure/MPa	Temperature/°C	Time/min
1	20	300	60
2	20	300	30
3	20	300	15
4	20	260	15
5	15	260	15
6	25	260	15
7	20	220	15

4.2.4. Nanoindentation Test

The conventional nanoindentation test displays a typical load-displacement curve, as in Fig. 4.4(a), with the load and unload performance. The diamond tip is pressed into the surface of a sample; meanwhile, plastic and elastic deformation occurs. During loading, the shape of the tip and indentation depth determines the contact area to calculate the hardness of materials. When unloading the tip, the elastic deformation is recovered. The hardness and the elastic modulus are the mechanical properties measured using nanoindentation. According to the load-displacement curve, the

hardness can be derived from the peak load P_{max} :

$$H = \frac{P_{max}}{A} \quad (4.1)$$

where A is the projected area of the contact surface as a function of the contact depth h_c and the shape of tip as:

$$A = f(h_c) \quad (4.2)$$

$$h_c = h_{max} - S(h_{max} - h_r) \quad (4.3)$$

where h_{max} and h_r are the maximum indentation depth and the final depth after complete unloading, as shown in Fig. 4.4(b). S represents the contact stiffness at the initial unloading, which is defined as the slope of the initial unloading curve. The elastic modulus can be derived from the contact stiffness as follows

$$S = 2\beta \sqrt{\frac{A}{\pi}} E_r \quad (4.4)$$

where β is the geometric constant of the indenter [18] and E_r is the reduced elastic modulus, which is related to elastic modulus E and Poisson's ratio ν , as the following relationship:

$$E_r = \frac{1 - \nu^2}{E} + \frac{1 - \nu_i^2}{E_i} \quad (4.5)$$

For the diamond Berkovich indenter, $E_i = 1141$ GPa, $\nu_i = 0.07$ and $\beta = 1.034$ [19], as well as the projected area A is given by $24.56h_c^2$.

Compared to the conventional method of determining stiffness from the slope at the top of the unloading curve, the advantage of the CSM mode is that the contact stiffness can be measured continuously in one loading experiment without the need for an unloading process. And the time constant of CSM is at least three orders of magnitude lower than conventional methods [16]. The CSM is conducted by applying harmonic forces to the nominally increasing load on the indenter, as illustrated in Fig. 4.4(c).

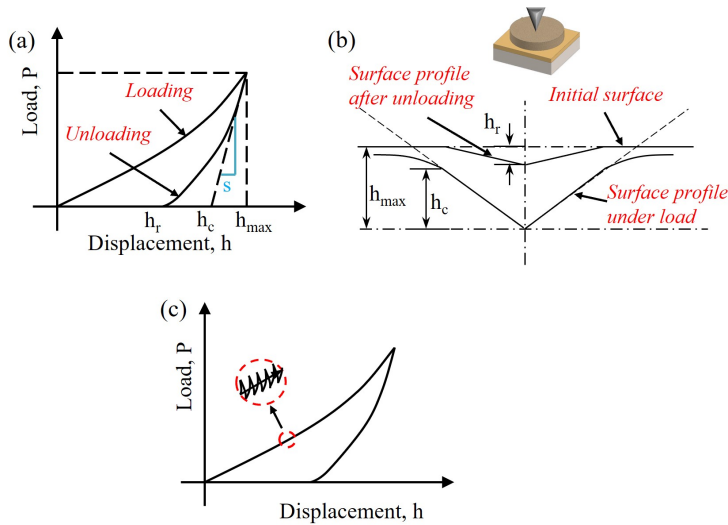


Figure 4.4: (a) A typical load-displacement curve, (b) schematic of the deformation of the sample during and after indentation [18] and (c) A sketch of the CSM loading cycle.

To study the sintering process parameters, nanoindentation test were performed on the surface of sintered CuNP bumps under different sintering conditions using the same process. In this study, the nanoindentation test were conducted in the Nano indenter G200, which is equipped with a diamond Berkovich tip indenter at a room temperature. For each sintering process parameter according to DOE, three CuNP bumps were selected, indented and measured at one position of each bump. For the characterization the surface nanocopper materials to achieve the improved nanoindentation test results, the CSM mode was applied during measurement and the indentation distance was set from 0 μm to 2 μm into the surface, using a surface approach velocity of 10 nm/s, a harmonic displacement of 2 nm and a frequency of 45 Hz. Finally, the effect of the sintering process parameters on the nanoindentation performance was investigated and analyzed by the load-displacement curve and the measured hardness, contact stiffness, and Young's modulus.

4.3. Results and Discussion

4.3.1. Test sample inspection

To inspect and compare the morphologies of CuNP bumps after LSP and sintering processes, a 3D optical and laser profiling analyzer combined with a 3D profilometer (Keyence VK-X250) were used to characterize the as-printed and sintered CuNP bumps. Fig. 4.5(a) and (b) show the 2D optical images and 3D laser image of the as-printed CuNP bumps. It has been observed that the majority of the CuNP bumps exhibit a circular shape and maintain uniform pitch, although some CuNP clusters are still attached to them. The success of the subsequent sintering process relies on achieving well-defined patterns following the LSP process. To determine the average height of the CuNP bumps, we created ten profile lines at intervals of $1.5\ \mu\text{m}$ for a row of both non-sintered and sintered CuNP bumps, respectively. These lines are indicated by the blue lines in Fig. 4.5(a) and (d). Fig. 4.5(c) shows the height distribution measured from 3D profilometer of the as-printed CuNP bumps indicated by the blue line in Fig. 4.5(a). It is observed that almost all the as-printed bumps present a valley shape. On the one hand, the solvent was evaporated due to the drying progress under $110\ ^\circ\text{C}$ (Fig. 4.2(e)), which caused the shrinkage of the CuNP bump. On the other hand, the boundary of the CuNP bumps was squeezed by the thermal expansion of the photoresist. Fig. 4.5(d) and e show the surface morphologies of the CuNP bumps sintered at $260\ ^\circ\text{C}$ with a pressure of 15 MPa for 15 min (sample 5). It is seen from Fig. 4.5(e) that the surface of the sintered CuNP bumps is more smooth than the as-printed CuNP bumps in Fig. 4.5(b).

Fig. 4.5(c) shows the height distribution of the CuNP bumps after the sintering process, where the blue lines represent the profile of non-sintered and sintered CuNP bumps, respectively. Obviously, the CuNP bumps show almost the same height after the sintering process, which is caused by the compressive stress during the sintering process. For as-printed bumps, the highest height point on the top surface is selected to calculate the average height of the CuNP bumps. The average heights of as-printed and sintered CuNP bumps are around $15.18\ \mu\text{m}$ and $6.19\ \mu\text{m}$ and the height deviation is $1.65\ \mu\text{m}$ and $0.18\ \mu\text{m}$, respectively. The height of sintered CuNP bumps is only

59.22% of the height of as-printed CuNP bumps. Fig. 4.5(f) compares the average height profile of the CuNP bumps (sample 6, sintered at 260 °C, 25 MPa, 15 min) with sample 5. It is observed that as the pressure increase to 25 MPa, the average height of as-printed and sintered CuNP bumps are around $14.63 \pm 1.54 \mu\text{m}$ and $5.55 \pm 0.16 \mu\text{m}$, respectively. The height of the CuNP bumps is reduced by 62.08% after sintering. It can be seen that the higher sintering pressure leads to higher compressibility.

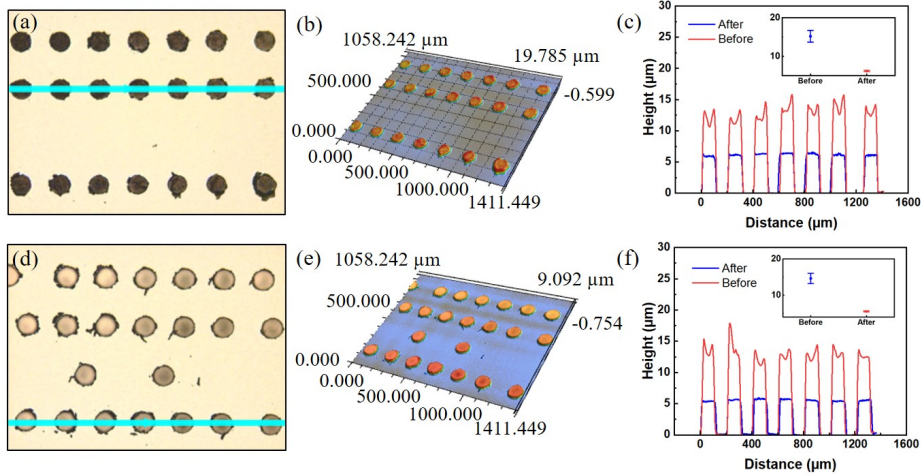


Figure 4.5: Inspection of CuNP bump sintered at 260 °C for 15 min with different pressure of (a)-(e) 15 MPa and (f) 25 MPa. (a) and (b) represent the top view of microscopy image for the sample before and after sintering, (b) and (e) represent 3D image of CuNP bumps before and after sintering, (c) and (f) represent the profile of the CuNP bumps sintered at 15 and 25 MPa, showing the profile before and after sintering in red and blue lines.

4.3.2. Nanomechanical analysis of sintered CuNPs

To investigate the micro-scale mechanical properties of the CuNPs bumps, the CSM nanoindentation tests were performed under different maximum indented depths. Fig. 4.6 shows the stiffness-displacement curves of CuNP bumps with different sintering parameters. Three groups of CSM nanoindentation tests were repeated for each sintering parameter. Fig. 4.6a-c presents the effects of sintering time, temperature, and pressure on the contact stiffness,

respectively. For each group, a clearly aligned contact stiffness curve is selected to indicate the micro-scale mechanical properties of the sintered CuNP material. Fig. 4.6d-f show the performance of Young's modulus as a function of indented depth for the sintered CuNP bumps. As reported by Li and Bhushan [16], the uniform material shows a linear relationship between indented depth and contact stiffness. This means that as the material becomes progressively harder, the contact stiffness increases with an ascending slope when the contact depth increases. On the contrary, for a progressively softer material, the contact stiffness rises with a decreasing slope with increasing contact depth.

Fig. 4.6a shows the contact stiffness of sintered CuNP bumps with different sintering time (15, 30, 60 min) under 20 MPa and 300 °C. For the samples sintered for 60 min, the slope of the contact stiffness decreases rapidly, while Young's modulus decreases with the contact depth, as shown in Fig. 4.6d, which indicates that the sintered CuNPs become softer from the surface to the deep location. In the cases of the samples sintered for 15 min and 30 min, the contact stiffness slope increases slightly with the contact depth, and Young's modulus has the same trend shown in Fig. 4.6d. It can be concluded that the samples sintered for 15 and 30 min present better homogeneity compared to the sample sintered for 60 min. To study the effect of sintering pressure and temperature on contact stiffness and Young's modulus, some samples were sintered at 260 °C for 15 min with different pressure (15, 20, and 25 MPa), and the other samples were sintered for 15 min with 20 MPa at different temperatures (220, 260, and 300 °C). Fig. 4.6b shows the relationship between contact stiffness and indented depth under 15, 20, and 25 MPa. It is shown that both the contact stiffness and Young's modulus increase when the sintering pressure increases from 15 MPa to 25 MPa. However, when the sintering temperature increased from 220 °C to 300 °C, the contact stiffness and Young's Modulus did not show a dependence on temperature.

Fig. 4.7 shows Young's modulus (black) and hardness (red) of the sintered CuNP bumps under different process parameters. Fig. 4.7a illustrates the effect of sintering time (15, 30, 60min) on modulus and hardness. First, Young's modulus remains at the same level of 116 GPa when the sintering time increases from 15 to 30 min; meanwhile, the

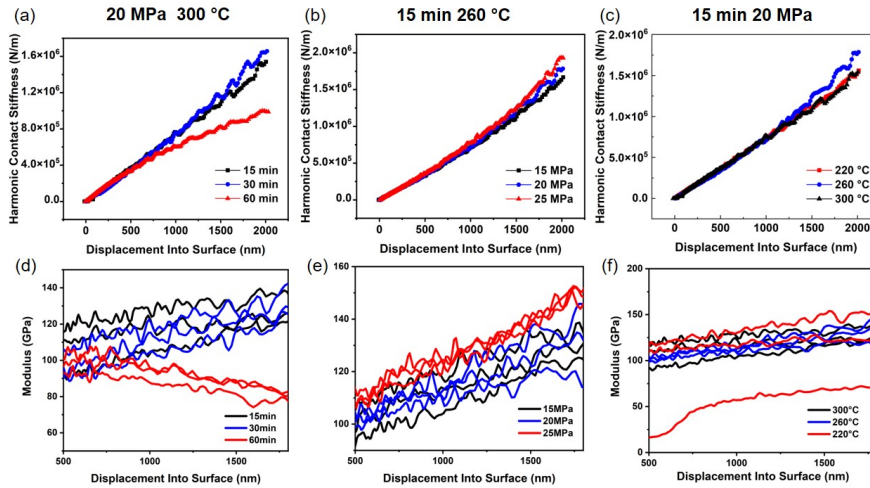


Figure 4.6: Contact stiffness and modulus as a function displacement into the surface of CuNP bumps with different (a) and (d) sintering temperatures of 15, 30, 60 min, (b) and (e) sintering pressure of 15, 20, 25 MPa, (c) and (f) sintering temperature of 220, 260, 300 °C.

hardness drops from 1.74 GPa to 1.59 GPa. Then, when the sintering time increases to 60 min, Young's modulus drops to 92 GPa, and the hardness increases to 1.77 GPa. It is reported that the modulus decreases continually when the sintering temperature is set at 300 °C, which is attributed to the softening behavior between 200-300 °C [20]. As reported, the hardness of pure copper remains unchanged under annealing at 200 °C, however, it reduces significantly after 300 °C annealing. The longer annealing time causes a more significant decrease in hardness. Young's modulus and hardness are to some extent coupled, so Young's modulus for the sample sintered with 60 min is lower than other samples. However, there is an increase in hardness for the sample sintered with 60 min.

Fig. 4.7b displays the effect of sintering temperature on Young's modulus and hardness of sintered CuNPs. The evolution of modulus and hardness exhibits a similar trend under different temperatures. When the sample was sintered at 220 °C, it presented that the average values of the modulus and hardness are 101 GPa and 1.59 GPa, respectively. When the sintering temperature increases to 260 °C, the modulus significantly improves, reaching 114 GPa with a 14.0% increase rate, and the hardness is measured to be from 1.59 GPa to

1.65 GPa. With further increasing the sintering temperature to 300 °C, the result does not improve substantially in both modulus and hardness. At 300 °C, the modulus only slightly increases to 116 GPa, representing an increase rate of 1.8%, while the hardness reaches 1.74 GPa, indicating a 5.5% increase rate. Based on the above results, we selected the sintering temperature of 260 °C to investigate the effect of different pressures.

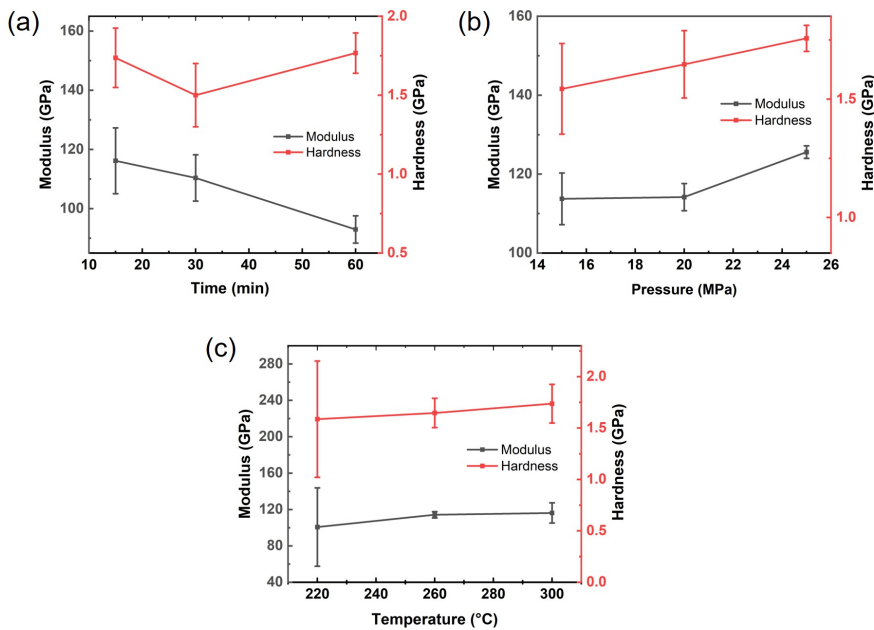


Figure 4.7: The effect of sintering time of (a) 15, 30, 60 min, sintering temperature of (b) 220, 260, 300 °C and sintering pressure of (c) 15, 20, 25 MPa on the modulus and hardness.

Fig. 4.7c shows the relationship among sintering pressure, Young's modulus and hardness. As the sintering pressure increases from 15 MPa to 20 MPa, Young's modulus remains constant at 114 GPa. Simultaneously, the hardness of the material increases from 1.54 GPa to 1.65 GPa. When a higher pressure of 25 MPa is applied, the modulus significantly increases to 126 GPa, corresponding to a 10.5% increase. Compared to 128 GPa for bulk Cu, the sample sintered at 25 MPa is reasonable and approaches the ideal situation [21]. Additionally, the hardness at this pressure reaches 1.76 GPa. As

discussed above, we achieved the highest modulus with 25 MPa pressure-assisted sintering at 260 °C for 15 min, based on the average value of modulus.

Actually, Young's modulus is highly determined by the microstructure of the sintered CuNPs. In this study, the sintering parameters (260°C, 25MPa) is recommended for this novel processing as sintered CuNPs under such temperature and pressure give stable and high Young's modulus and hardness. Meanwhile, the sintering time of 15 min is recommended for this processing. On the one hand, Young's modulus remains almost the same with the sintering time of 15 and 30 min. On the other hand, the less time will help to enhance the high throughput of packaging based on this processing.

4.3.3. Micro- and nanostructural analysis of sintered CuNPs

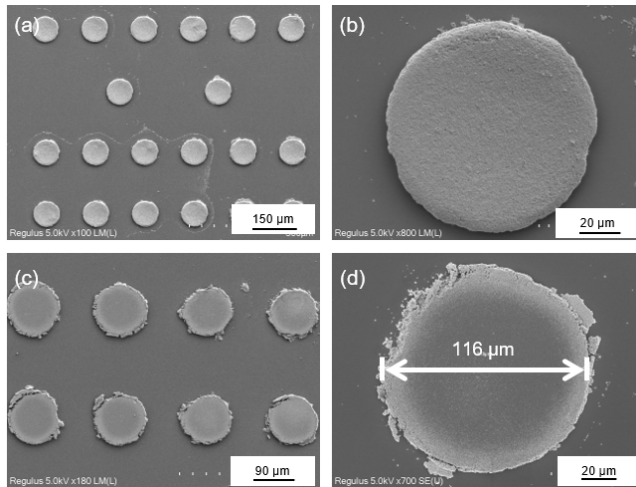


Figure 4.8: (a) and (b) the SEM image of CuNP bumps before sintering, (c) and (e) the SEM image of CuNPs sintered at 15 MPa and 260°C for 15 min

A Hitachi Regulus 8230 scanning electron microscope (SEM) was used to observe the micro- and nanostructure of CuNPs. Fig. 4.8a and Fig. 4.8b shows the SEM images of the non-sintered CuNPs array at different magnifications. It can be observed that the patterned CuNP bumps have regular round shapes and smooth edges, corresponding to the photoresist mask after photolithography, as indicated in

Fig. 4.2c. There are only a few bright CuNPs on the substrate, which is due to the fact that the organic residue (NMP) with dissolved nanoparticles was not rinsed clean enough by deionized water after the lift-off process. These remaining CuNPs are bare; hence, there are no interconnects between neighboring CuNP bumps. Consequently, the patterning process is completed successfully.

Fig. 4.8c and Fig. 4.8d show the top view of sintered CuNP bumps on a sample sintered at 15 MPa and 260 °C for 15 min (sample 5) after the dummy die peeled off from the substrate chip. Since the top dummy die is bare silicon, the CuNPs cannot be sintered on the silicon interface and can be detached easily. Peeling off the top die does not influence the CuNP bump substrate. It can be observed from Fig 4.8d that a central relatively dark area and a brighter edge area refer to the sintered and unsintered areas of CuNPs, respectively, which is caused by the compression of the uneven surface during sintering process.

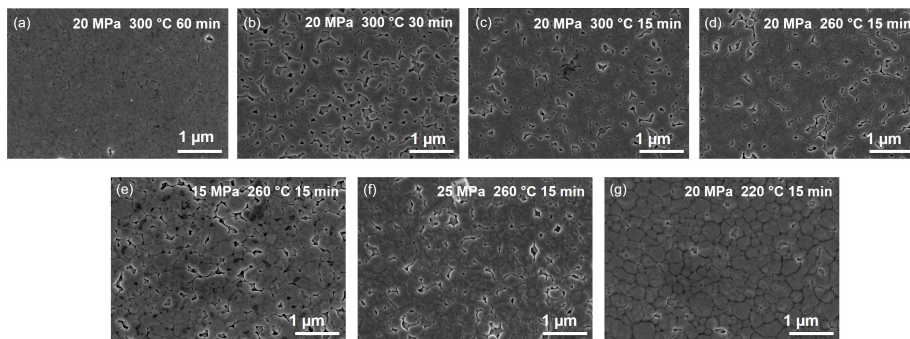


Figure 4.9: SEM image of the top surface of a sintered CuNP bump, with sintering parameters marked on top of each image.

Surface images of sintered CuNPs under different sintering parameters, on which an indenter was imprinted to measure CSM nanoindentation, are shown at higher magnification in Fig. 4.9. It can be observed that the CuNPs on the upper surface are still quasi-spherical and constitute a porous network structure with the formation of sintering necks between adjacent CuNPs. The SEM image of the indentation spot on the test samples is shown in Fig. 4.10. As reported [17], a rapid change occurs at the beginning of the indentation measurement due to the observed compaction

phenomenon until about 200 nm of penetration. The measurement data of nanoindentation were not stable near the surface of the CuNP bumps, so we used the average data of the mechanical properties of CuNP bumps from 0.2 μm of penetration of the indenter to the depth.

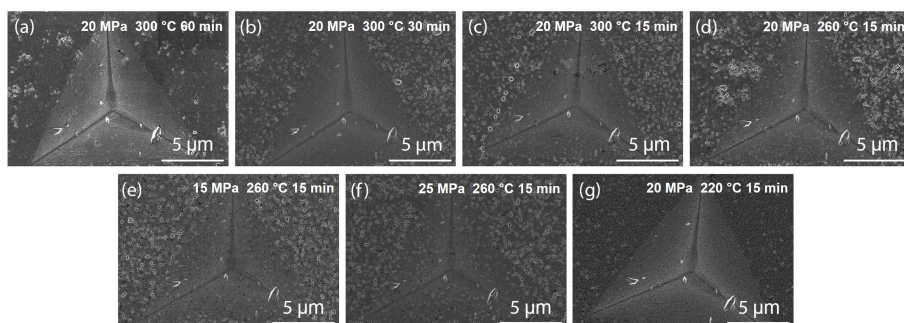


Figure 4.10: The SEM images of the indentation imprints with different sintering parameters marked on top of each image.

The cross-section of the sintered CuNP bump on sample 5 (15 MPa, 260 °C, 15 min) was obtained by using focused ion beam milling (SEM-FIB, FEI Helios G4 CX), as illustrated in Fig. 4.11a. It is observed that sintered CuNPs is a porous structure and the formation of the sintering neck establishes a network on the cross-section. Nanoparticles were compressed in the vertical direction. The composition of the sintered CuNPs was analyzed using EDX to evaluate the oxygen content of the sintered CuNP bump on sample 5. Fig. 4.11b shows the EDX result at the position indicated in the corresponding location in Fig. 4.11a. It is observed that there is only a small amount of oxygen, which is attributed not only to the residual organic additives but also to a slight surface oxidation on individual CuNP at the vacuum atmosphere. As a result, oxidation is not significantly detrimental to the sintering process, and vacuum sintering conditions are feasible for flip-chip interconnects.

Fig. 4.11c shows the SEM-FIB image of the cross-section for sample 1, which was sintered at 20 MPa, 300 °C for 60 min, leading highly sintered structures and extremely low porosity. It is observed that the CuNPs are almost a polycrystalline copper material. This sintering parameter combination can promote densification and reduce porosity in the sintered material. However, as discussed in the

previous section, copper will present softening effect at the temperature of 300 °C, and the hardness has been enhanced when the sintering time increases from 15 to 30 min. As indicated by the red curve in Fig. 4.7a, the hardness of this sample was higher than those samples sintered for 15 and 30 min.

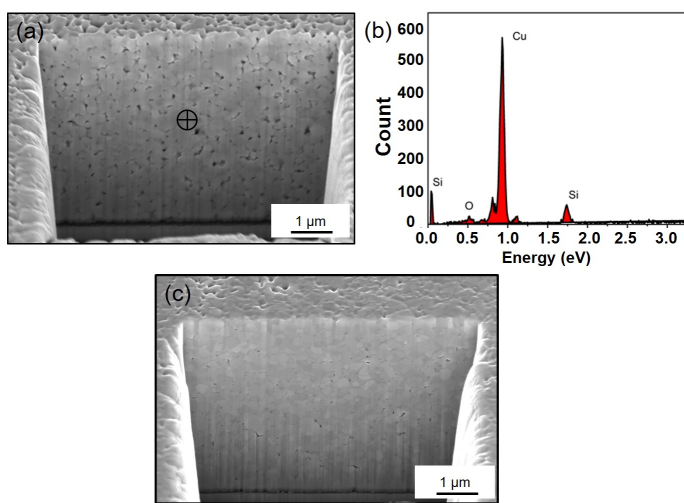


Figure 4.11: (a) and (c) represent FIB/SEM images of the cross-section of the CuNP bumps sintered at 15 MPa, 260 °C, 15 min and 20 MPa, 300 °C, 60 min, respectively.

4.3.4. Electrical conductivity of sintered CuNPs

Electrical conductivity is essential for interconnect application of sintered CuNPs. An individual CuNP bump on sample 5 (15 MPa, 260 °C, 15 min) was characterized in this study to measure the resistivity. The schematic of the four-point measurement setup is shown in Fig. 4.12a. Voltage was applied to the top left and right edge of the bump. Meanwhile, the voltage difference can be measured by landing the probes on the bottom left and right edge of the bump, and the current on the top-side contact can be characterized to eliminate contact resistance. A force voltage was applied to the CuNP bumps sweeping from -0.5 to 0.5 V. The I-V characteristics are plotted in Fig. 4.12b, where the measurement data are fitted as a lineal relationship between voltage difference and force current. The

measured resistance was extracted as 3.28 mΩ. Then, the resistivity of sintered CuNP bump was derived from:

$$\rho = 4.532 \cdot t \cdot R \quad (4.6)$$

where t is the thickness of sintered bump, combined with the previously mentioned thickness of the bumps on sample 5 as 6.19 μm. R presents the measured resistance as 3.28 mΩ, extracted from the I-V curve. The resistivity of sample 5 is $9.2 \times 10^{-6} \Omega \cdot \text{cm}$, which is 5 times of the bulk Cu of $1.7 \times 10^{-6} \Omega \cdot \text{cm}$ due to its porous structure and slight oxidation. The resistivity of sintered CuNPs is related to their porosity and indicates the sintering quality. As a result, it can be concluded that the sintering parameter of sample 5 is feasible for the flip-chip interconnects in the aspect of electrical conductivity.

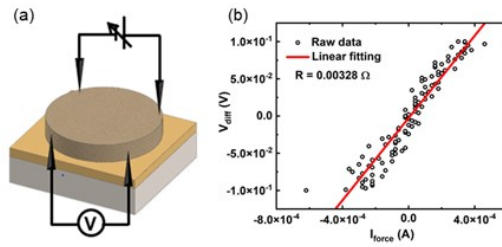


Figure 4.12: (a) A sketch of a four-point measurement and (b) the I-V characteristics.

4.4. Conclusions

In this study, firstly, we developed a novel CuNPs patterning method for flip chip integration fabrication. The thickness of CuNP interconnects bumps was determined by the photoresist thickness during the LSP process and the sintering parameter. The higher applied sintering pressure induced the higher compression of sintered bumps. The LSP process enables more freedom in the form of factor and thickness for CuNP interconnects, which will contribute to the fabrication of dedicated stress relive structures. Then, the mechanical properties of CuNP material under different sintering parameters were evaluated by using CSM nanoindentation. Young's modulus and hardness were utilized to assess the homogeneity and the strength of sintered material. The less sintering time was

beneficial to achieve a homogenous material and increased the productivity in the industry. The sintering temperature was adjusted to reach a suitable temperature of 260 °C. The increasing sintering pressure improved the sintering neck formation to strengthen the hardness of sintered CuNP material. The combination of sintering parameters at 260 °C, 15 minutes, and 25 MPa is recommended, not only because it yields the highest Young's modulus of 126 GPa but also due to its high throughput during fabrication. Moreover, the sintered CuNPs have a nanoporous structure with slight oxidation. Therefore, they are more ductile than bulk Cu. In addition, the resistivity of sintered CuNPs was $9.2 \times 10^{-6} \Omega \cdot \text{cm}$, which is 5 times of the bulk state. Therefore, these experiments revealed the optimal sintering parameter for CuNPs as an interconnect material and provided a high-throughput solution for CuNP bumps patterning in the flip chip integration application.

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5

20 μm Pitch Cu-to-Cu Direct Bonding through NP Sintering Technology for High Density Integration

A 20 μm pitch Cu-to-Cu direct bonding method is proposed in this study using CuNP sintering technology, which provides a viable alternative to conventional solder-based interconnects for high-density integration in next-generation semiconductor packaging. The LSP technique was employed for precise CuNP patterning, followed by TCB to achieve reliable Cu-to-Cu interconnects. The effects of sintering temperature and pressure on bonding quality were systematically investigated, revealing that optimal conditions of 280 °C and 75 MPa yield a shear strength of 38 MPa, comparable to that of Cu-Sn interconnects reported in this study. Compared to bulk Cu-to-Cu interconnects, CuNP-based joints require lower annealing temperatures and pressures while achieving higher shear strength. Microstructural analysis confirms the formation of well-defined sintering necks and fracture characteristics, demonstrating the bonding quality and mechanical reliability of CuNP-based interconnects.

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5.1. Introduction

Chiplet technology, as a modular design approach, has become integral to fulfilling the concept of 'More than Moore'. Microbump interconnects play a key role in Chiplet-based architectures to realize 3D structures and must withstand higher current densities and temperatures, especially in high-performance computing systems. Due to the low melting temperature of solder, conventional Sn-based interconnects in 3D integration may lead to issues such as remelting and electromigration failure under high current densities [2]. To overcome these limitations, Cu-Cu direct bonding has been identified as a promising solution for 3D integration.

In bonding technology, several bonding materials and approaches exist. According to research, 3D integration is achieved through metal-to-metal bonding, polymer-to-polymer bonding, oxide-to-oxide bonding, and hybrid bonding [3]–[5]. Among these, metal-to-metal bonding offers the advantage of superior electrical performance in 3D stacking structures. With increasing transistor density, the continuous decrease in power supply voltage, and advancements in 3D integration, current density continues to rise [6]. When a sufficiently high current density flows through integrated circuits, EM occurs, leading to device failure. Cu exhibits superior EM resistance and holds great potential for 3D packaging [7]. Therefore, further investigation into all-Cu interconnect technology is essential to enhance reliability.

Cu-Cu TCB is a preferred interconnect technique for fabricating all-Cu interconnects. The fundamental mechanism of Cu-Cu bonding relies on Cu atom interdiffusion and Cu grain growth at the interface under applied pressure and temperature [8]. However, Cu is an active material that oxidizes easily, and the presence of an oxide layer hinders Cu atom interdiffusion. Although high temperature and pressure can improve bond strength, excessive process conditions can degrade IC interconnect performance due to damage to Cu interconnects. Hence, low-temperature and low-pressure Cu-Cu bonding has been investigated [9].

Cu-Cu surface-activated bonding (SAB) was first applied by Takagi *et al.* at room temperature [10]. In this approach, an argon ion beam is used to remove the Cu surface oxide layer. However, the drawbacks of SAB include Cu surface damage and increased surface roughness.

Consequently, a CMP step is necessary after SAB [11]. Additionally, Cu-Cu bonding through a self-assembled monolayer (SAM) passivation layer is another technique to achieve low-temperature, low-pressure all-Cu bonding [12]. An alkane-thiol SAM layer forms on the Cu surface under ambient conditions, as demonstrated by Whelan *et al.* [13].

CuNP paste offers an alternative to solder-based interconnects due to its superior EM resistance and high melting temperature [14]. Unlike B-Cu (bulk Cu), CuNPs can form interconnects through a sintering technique at temperatures below their bulk melting point (1083 °C), reducing thermal stress during bonding. In addition, CuNPs are compressible, eliminating the need for CMP before bonding. They are particularly suitable for fine-pitch Cu-to-Cu bonding applications that require high precision, uniformity, and low-temperature processing [15]. CuNP sintering enables a more reliable and efficient bonding process, particularly in harsh environments such as data centers and high-performance computing systems.

In this study, we employed LSP to fabricate an array of 20 μm pitch CuNP bumps [16], [17]. A thin layer of photoresist served as the stencil mask during CuNP paste printing and was subsequently removed by a lift-off process. Then, the TCB process was utilized to integrate the CuNP bumps with electroplated Cu μ bumps, achieving Cu-to-Cu direct bonding. We developed the sintering parameters for the TCB process and investigated the mechanical properties as well as the microstructural evolution.

5.2. Experimental Section

5.2.1. Design of interconnect test sample

Two chips were prepared to implement the 20 μm pitch 3D-stacked dies. One die served as the bottom substrate, featuring a cavity array to define the CuNP bumps, while the other die had electroplated Cu bumps. Fig 5.1a illustrates the design definitions for the interconnect test sample. In the first stage, we designed and fabricated the bottom substrate with a photoresist stencil mask intended for the subsequent LSP process, as shown in Fig. 5.1c. To begin, a 1 μm -thick dielectric layer (SiO_x) was deposited on a 12-inch wafer, followed by lithography

and plasma etching to create 660 nm-deep cavities. The cavity array had a diameter of 14 μm (Φ_1) and a pitch of 20 μm . Next, the prepared wafer was sputter-coated with a TaN/Cu adhesive layer (10 nm/150 nm). Subsequently, the CMP process removed the TaN/Cu layer from the surface of the dielectric layer, leaving it inside the cavities. Then, a 1.6 μm -thick photoresist layer was coated onto the wafer, followed by photolithography to pattern a hole array with a 16 μm diameter (Φ_2) and a 20 μm pitch. The wafer was then diced into test coupons measuring $35.1 \times 33.6 \text{ mm}^2$, each consisting of a 3×3 chip array, as shown in Fig. 5.2a.

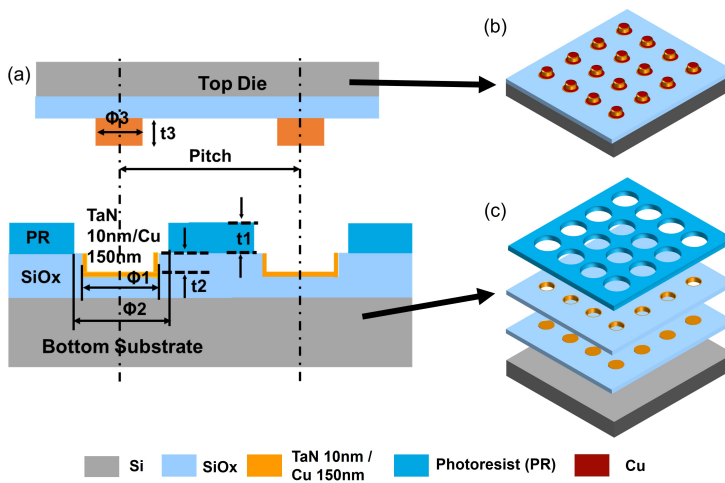


Figure 5.1: (a) Schematic diagram of the interconnect test sample, showing the prepared bottom substrate fabricated via photolithography and the top die with Cu μ bumps. (b) 3D illustration of the bottom substrate. (c) Schematic illustration of the top die.

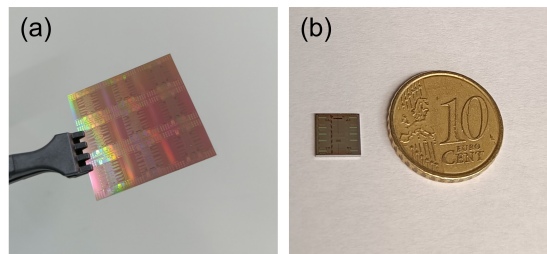


Figure 5.2: (a) The test coupon serving as the bottom substrate with a photolithographic stencil mask. (b) Top die with electroplated Cu μ bumps.

In addition, we fabricated top chips featuring electroplated Cu μ bumps with a 20 μ m pitch, each measuring 2 μ m in height and 7 μ m in diameter (Φ_3), on 12-inch wafers. Figure 5.1b presents a sketch of the Cu μ bumps on the top die. The processed wafer was then diced into 7.2×7.2 mm² chips to facilitate chip-to-substrate bonding in the subsequent step, as illustrated in Fig. 5.2b.

5.2.2. Photolithographic approach to CuNP patterning

We conducted LSP experiments to transfer the CuNP patterns onto the test coupon, as illustrated in Fig. 5.3. As discussed in Sec. 2.3.2, LSP was performed when a thin 1.6 μ m layer of photoresist was applied. Therefore, the CuNP paste was applied once using a silicon squeegee on the coupon and then dried in an oven at 110 $^{\circ}$ C for 15 min, as shown in Fig. 5.3a and b.

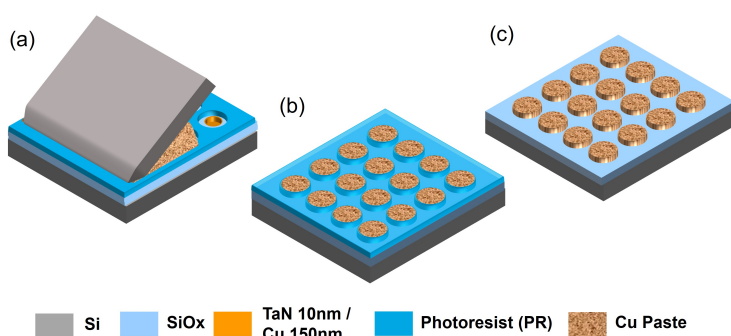


Figure 5.3: Overview of the pattern transfer process using LSP.

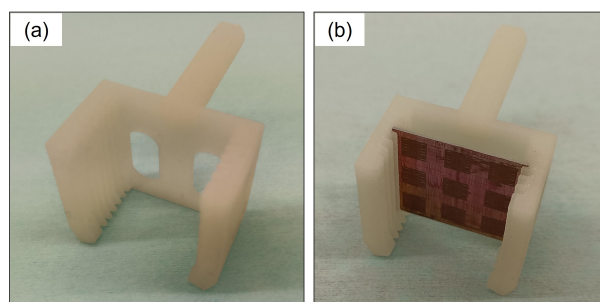


Figure 5.4: (a) A specially designed and manufactured lift-off carrier fabricated via 3D printing. (b) Insertion of the nanopaste-spread test coupon into the carrier for lift-off.

We designed a special test coupon carrier for the lift-off process in Fig. 5.3c, which was manufactured using Polypropylene by 3D printing. The coupon carrier is depicted in Fig. 5.4a, which has the property of resisting dissolution in organic solutions. The test coupon was properly inserted and positioned in this carrier (Fig. 5.4b) and then was upside-down immersed in N-Methyl-2-pyrrolidone under agitation under 60 °C to strip the photoresist (Fig. 5.3c). The sketch of the lift-process is shown in Fig. 5.5.

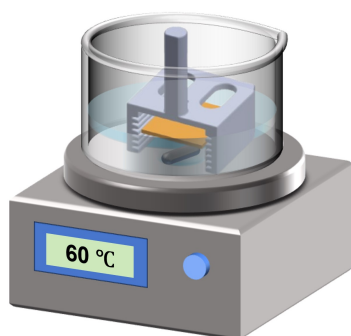


Figure 5.5: A schematic of lift-off process. The carrier was specially designed and fabricated using 3D printing.

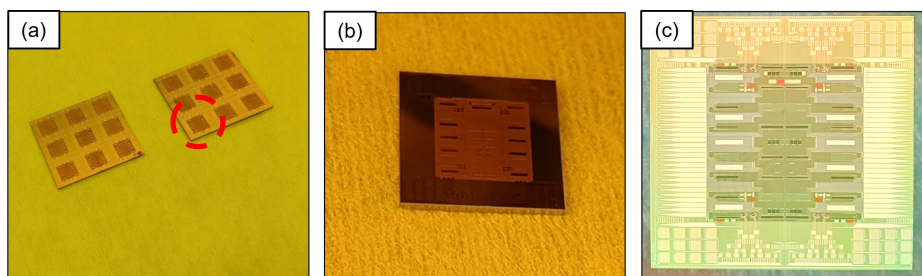


Figure 5.6: (a) Test coupon with CuNP patterns after the lift-off process. (b) Single chip after dicing. (c) Top view of a well-defined die with CuNP patterns transferred via the LSP method.

The resultant coupons following the lift-off process were depicted in Fig. 5.6a. These coupons were subsequently diced into individual chips measuring $11.7 \times 11.2 \text{ mm}^2$ using the wafer dicing Disco DAD321, as illustrated in Fig. 5.6b. These diced chips served as the bottom substrate for the integration process in the subsequent step.

Fig. 5.6c shows the entire bottom chip with CuNP pattern under the microscope, the characterization details of which will be discussed in the next section.

5.2.3. Formation of fine pitch interconnects

We employed the TCB process to sinter the CuNP interconnects. This involved aligning the flipped top chip with the bottom substrate using an FC150 flip-chip bonder (Karl Suss). The FC150 bonder is capable of performing only pressure-assisted sintering in an ambient environment to integrate the top chip and bottom substrate. Fig. 5.7 illustrates the heating platform, which can reach temperatures up to 450 °C while simultaneously applying a bonding force.

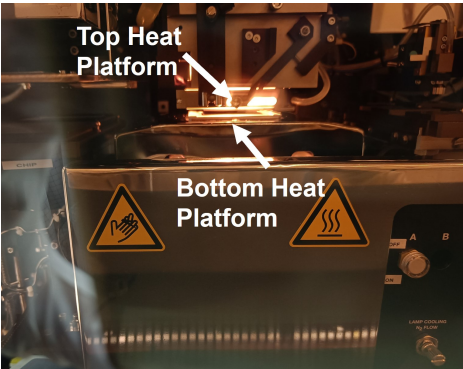


Figure 5.7: (a) Flip chip bonder tool and (b) thermal compression bonding platform

Table 5.1: DOE for sintering process parameter study (B-Cu: bulk Cu, N-Cu: CuNPs, Cu-Sn: solder interconnects).

Materials	Pressure/MPa	Temperature/°C	Time/min
B-Cu to N-Cu	75	180	15
B-Cu to N-Cu	75	210	15
B-Cu to N-Cu	75	240	15
B-Cu to N-Cu	75	280	15
B-Cu to N-Cu	40	240	15
B-Cu to N-Cu	100	240	15
B-Cu to N-Cu	35	340	15
B-Cu to B-Cu	300	240	15
B-Cu to Cu-Sn	6	250	2

The DOE for the study of 20 μm pitch integration is shown in Table 5.1. Based on the study in Chapter 4, we achieved good results even with a sintering time of only 15 min in a vacuum environment. In this chapter, due to the limitations of the flip-chip bonding tool, the TCB process had to be performed in air. CuNPs are more prone to oxidation during in-air sintering, so the sintering time in this chapter was set to the minimum sintering time (15 min) used in the vacuum sintering experiments. Initially, we studied the impact of process parameters on the integration of CuNPs (N-Cu) with B-Cu and aimed to establish a calibration for subsequent investigations. To assess the key properties in comparison with conventional flip-chip integration methods, we conducted tests involving B-Cu to B-Cu and B-Cu to solder (Cu-Sn) integration, which served as references for evaluating the novel CuNP joint technology.

Formation of Cu-to-Cu Interconnects Using NP Sintering Technology

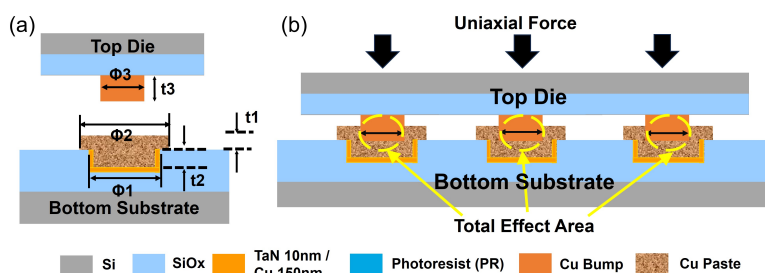


Figure 5.8: (a) Schematic of Cu μ bumps for top to align with CuNPs patterned bottom chip. (b) Schematic representation of bonded dies under uniaxial force, illustrating the total effective bonding area for pressure and shear strength calculations.

The stacked chips were first bonded in air at temperatures of 280 $^{\circ}\text{C}$, 240 $^{\circ}\text{C}$, 210 $^{\circ}\text{C}$, and 180 $^{\circ}\text{C}$, each with a pressure of 75 MPa applied for 15 min. Subsequently, the effects of sintering pressure were investigated and modified at 40 MPa, 75 MPa and 100 MPa. Additionally, we established an extreme condition to perform the sintering process at a higher temperature of 340 $^{\circ}\text{C}$ and a lower pressure of 35 MPa to assess the mechanical performance of CuNP interconnects under these specific parameters. Fig. 5.8a shows the schematic representation of interconnects between Cu μ bumps and

CuNP bumps. Fig. 5.8b illustrates the schematic of bonded chips based on TCB parameters, indicating the effective bonding area of each chip, estimated to be 1.55 mm^2 for each chip.

Formation of Reference Interconnects Using TCB Technology

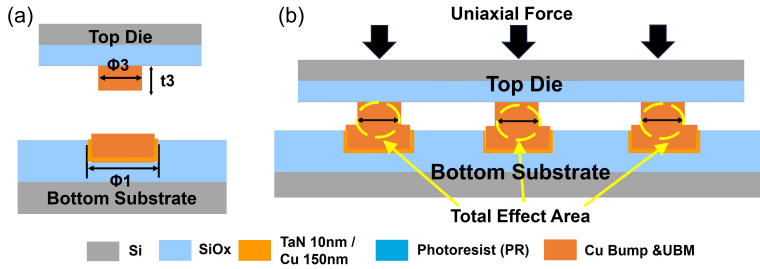


Figure 5.9: (a) Schematic of Cu μ bumps (without CMP procedure) for top to align with Cu UBM on the bottom chip. (b) Schematic representation of bonded dies under uniaxial force, illustrating the total effective bonding area for pressure and shear strength calculations.

We performed two additional types of interconnects as references for calibrating Cu-to-Cu direct bonding using NP sintering technology. Initially, We prepared a bottom substrate with the same layout as depicted in Fig. 5.8. Following this, we employed a Cu damascene process to fabricate Cu UBM, which was embedded in BEOL dielectric to replace the cavities and CuNP patterns. One type of interconnect was implemented through electroplated Cu bump to Cu UBM to achieve B-Cu to B-Cu integration without using the CMP process, as depicted in Fig. 5.9a. During TCB, the applied bonding pressure of 300 MPa and the temperature of 240 °C were set at the same level as in the joint study of the effect of pressure on CuNPs, as shown in Fig. 5.9b.

Another type of interconnect was achieved through Cu-Sn on the top die to Cu UBM on the bottom die. The bumps on top dies were fabricated by electrolytic plating and consisted of Cu bumps and Sn solder caps, as shown in Fig. 5.10a. The solder joint bonding process is illustrated in Fig. 5.10b, where the bottom substrate and top die were heated above the melting point of Sn, set to 250 °C, and combined under 6 MPa for a process time of 2 min to form the solder joint [18]–[20].

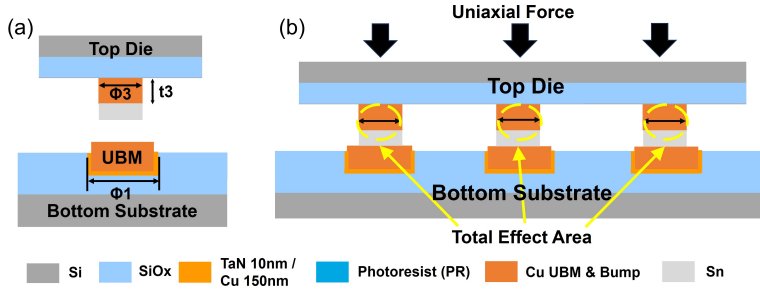


Figure 5.10: (a) Schematic of Cu μ bumps with solder cap for top to align with Cu UBM on the bottom chip. (b) Schematic representation of bonded dies under uniaxial force, illustrating the total effective bonding area for pressure and shear strength calculations.

5

5.2.4. Shear strength test

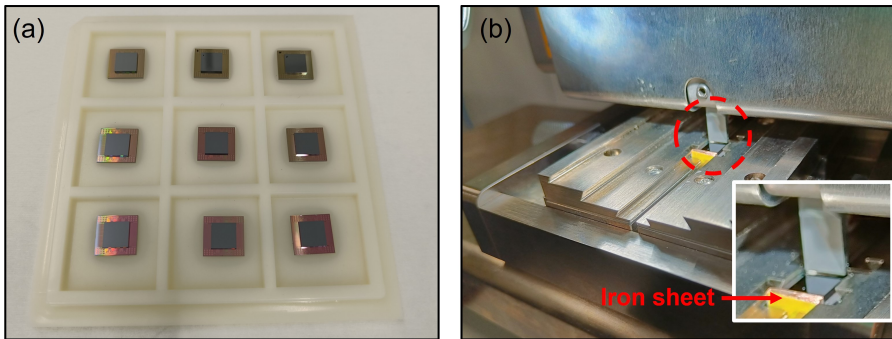


Figure 5.11: (a) Photograph of stacked dies and (b) Die shear test tool with a close-up view of sheared area.

The shear strength of the bonded dies was measured using Royce 650 Universal Bond Tester (Accelonix). The bond test was set up with a tool lift height of 50 μm and a shear rate of 5 $\mu\text{m/s}$. Fig. 5.11a shows nine stacked dies awaiting the bonding strength test. The shear test tool is illustrated in Fig. 5.11b. It can be observed that the stacked dies are clamped in the chuck and secured by an iron sheet during applying shear force.

5.3. Results and Discussions

5.3.1. Evaluation of the sample fabrication process

A 3D profilometer (Keyence VK-X250) was used to measure the profile of the test sample and CuNP patterns transferred using LSP. The height and diameter of the Cu paste after transfer onto the substrate were evaluated from optical and laser images using an image analysis software (MultiFileAnalyzer, Keyence). The resulting samples were characterized using a dual-beam focused ion beam-scanning electron microscope (FIB/SEM) system (FEI Helios G4 CX).

Characterization of the Interconnects Test Sample

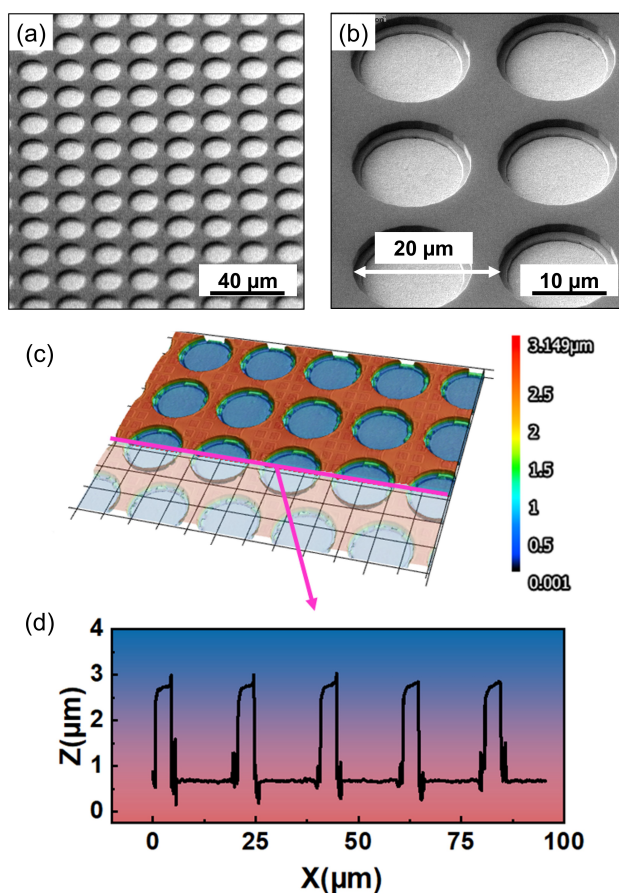


Figure 5.12: (a) and (b) SEM images of test sample. (c) 3D optical image of surface. (d) Surface profile of cavity array indicated by the pink line in (c).

We inspected the substrate covered by photoresist for further patterning studies. The fabricated test sample for the LSP process is illustrated in Fig. 5.3. SEM images in Fig. 5.12a and b depict the resulting Si test coupon containing TaN/Cu-coated holes. It is observed that the fabricated sample exhibits a pitch of 20 μm , an inner diameter of 14 μm , and an outer diameter of 16 μm . In Fig. 5.12d, the surface profile of the photoresist opening cavity array on the test sample is analysed, and the profile is indicated by the pink line in Fig. 5.12c, demonstrating the 3D surface topography of the test sample. The depth of the holes is estimated to be 2.1 μm using the 3D profilometer, corresponding to the sum of depths t_1 and t_2 in Fig. 5.8. t_1 and t_2 respectively representing the thicknesses of the cavity inside the dielectric layer and the photoresist covering on the dielectric layer. The etched cavities were designed to limit the movement of CuNP bumps during the lift-off process, thereby improving the integrity of the CuNP patterns transferred in the next step.

The top chip was characterized as shown in Fig. 5.13. In the SEM images (Fig. 5.13a and b), electroplated Cu μ bumps with regular oblate shapes are arranged in an array on the Cu UBM layer. As illustrated in Fig. 5.13c, it is clear that the μ bump surface is unpolished and has a rough appearance. In Fig. 5.13e, the surface profile of the Cu μ bump array on the top chip was measured, and the profile is indicated by the dark blue line in Fig. 5.13d, demonstrating the 3D topography of the top die. The 3D profilometer revealed that the Cu μ bumps on the top die have a 20 μm pitch, a 7 μm diameter, and a height of approximately 1.7 μm . According to the observations, the height of the μ bumps remains consistent, although the surface is rough and uneven.

Characterization of the Test Coupon after CuNP Paste Printing

Fig. 5.14 presents SEM images depicting the test coupon spread with CuNP paste, facilitating analysis and providing a clearer understanding of the patterning process. As illustrated in Fig. 5.14a, distinct patterns generated by photolithography and covered with CuNPs can be observed. It is evident that the cavity array is populated with CuNPs, while the photoresist surface is coated with CuNP residues. In Fig. 5.14b, a clear photoresist sidewall between the photoresist area and the cavity area can be seen, which is not covered

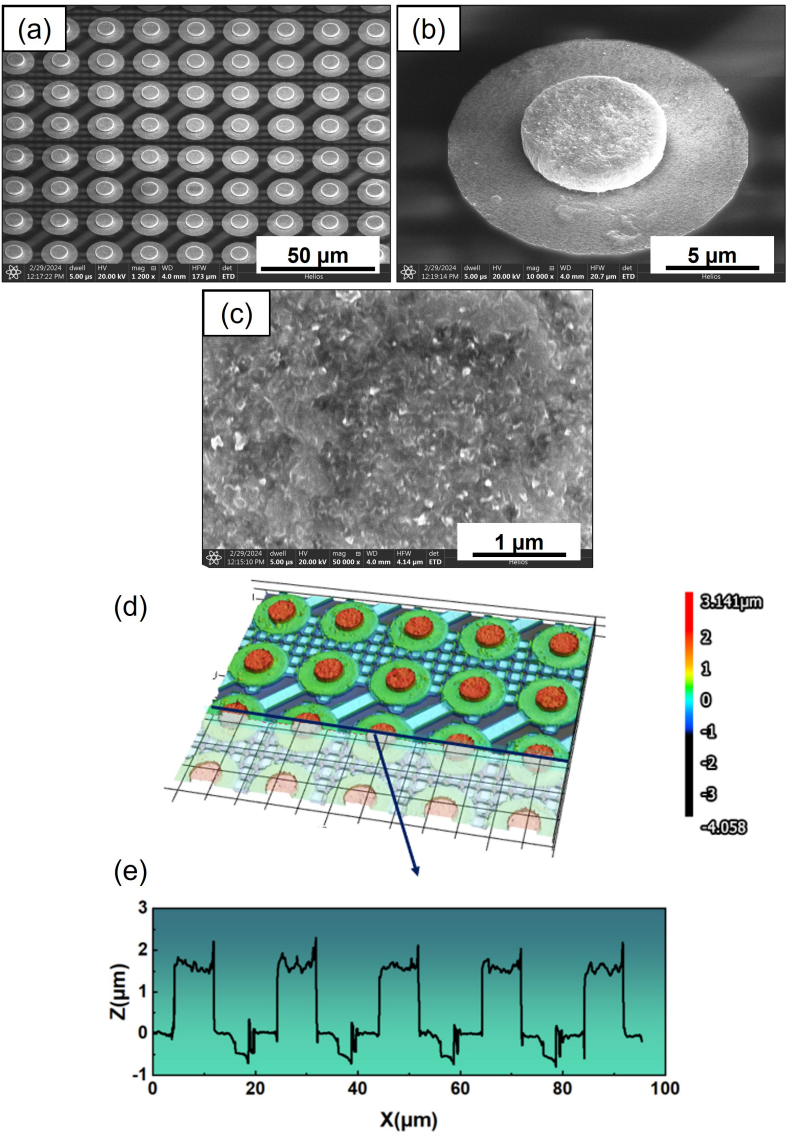


Figure 5.13: SEM images of (a) Cu μ bumps array, (b) a single Cu μ bump and (c) the surface of Cu μ bump. (d) 3D image of the surface of top chip. And (e) surface profile of μ bumps indicated by the dark blue arrow in (d).

by CuNPs. This structure allows the NMP solution to directly contact and dissolve the photoresist without damaging the CuNP pattern inside the cavity. Furthermore, it is observed that only a single or double layer of CuNPs remains on the photoresist, which simplifies the process of stripping CuNPs from the photoresist area and prevents residual particles from remaining on the dielectric layer of the bottom substrate. The evaluation of the lift-off results will be discussed in the next section.

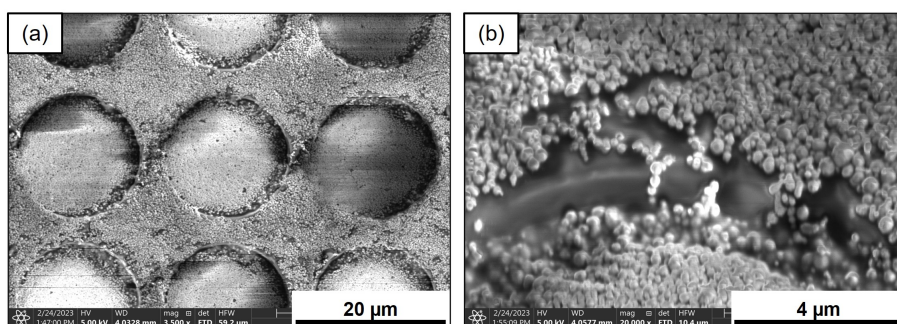


Figure 5.14: SEM images of a test coupon with CuNP paste before lift-off process showing the surface of the bottom substrate (a) and the photoresist edge on the cavity (b).

Characterization of the Test Coupon after the Lift-Off Process

Fig. 5.15a shows a test coupon with a CuNP bump pattern formed using the LSP approach, with the inset indicating a separate bottom substrate after dicing for subsequent die integration. The CuNP pattern was defined by the photoresist stencil mask and evaluated based on the integrity of the CuNP bump array and the bump height, which was determined by the thickness of the photoresist. The integrity of the CuNP pattern after the lift-off process is illustrated in Fig. 5.15b, showing a well-preserved array of bumps. The photoresist between the bumps has been completely removed, leaving no excess material residue between adjacent bumps and retaining only the opening pattern defined in the previous photoresist step.

Fig. 5.15c and d show the 3D image and height profile of the bump array, respectively. It can be observed that the bump pitch is 20 μm , and the surface of the CuNP bumps is highly rough. The height of the CuNP bumps was estimated from the average height of the profile to

be approximately $1.8\ \mu\text{m}$, slightly exceeding the photoresist thickness ($1.6\ \mu\text{m}$). This observation indicates a correlation between bump height and photoresist thickness, with the slight excess of nanomaterial attributed to an additional layer of NPs.

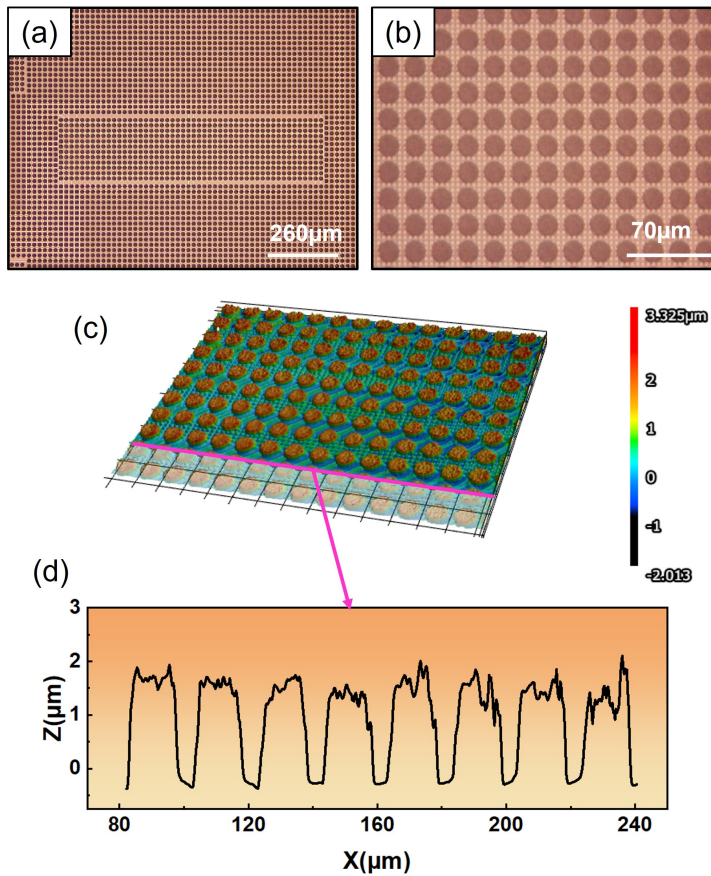


Figure 5.15: (a) and (b) Optical image of the CuNP bump array. (c) 3D image of bottom substrate and (d) height profile along the pink line in (c) of CuNP bumps.

Fig. 5.16 shows SEM images of the bottom substrate after the lift-off process, illustrating the integrity of the transferred CuNP pattern and the morphology of the CuNP bumps. The patterned CuNP bumps remained completely on the bottom substrate. This indicates that the cavity structure helps fix the CuNP patterns in place during the lift-off process in high-resolution patterning applications. It is clearly seen that the shape of each individual pattern maintains

the original structure of the opening area defined by the photoresist. No areas of the bump shape were lost after the lift-off process, leaving CuNPs in the cavities, which created a bump array during the lift-off process. Fig. 5.16f illustrates the thin film of CuNP bumps, which are 1.8 μm thick and consist of multiple layers of CuNPs at the edges.

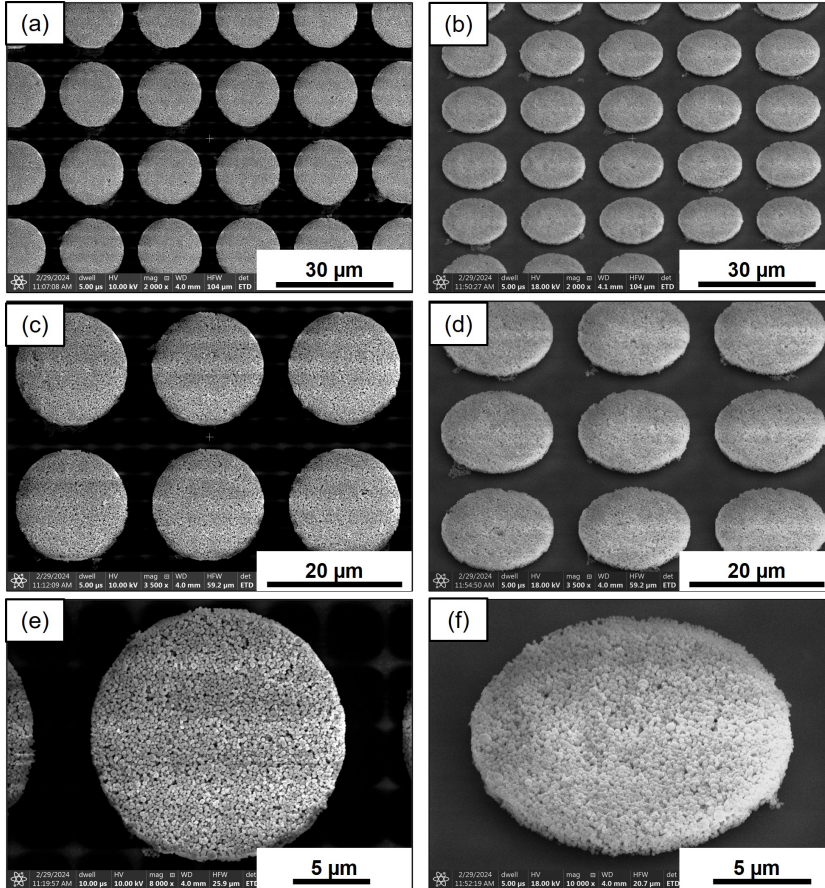


Figure 5.16: SEM images of transferred CuNP patterns after lift-off process in top view in (a)(c)(e) and tilted at 45 degree in (b)(d)(f) at different magnifications.

5.3.2. Evaluation of bonded dies

Examination of Stacked Die Alignment

Fig. 5.17a illustrates a photograph of a single stacked chip after in-air sintering using the TCB approach at a sintering pressure of 75 MPa. To assess the alignment of the flip-chip, infrared microscopy was

employed, as depicted in Fig. 5.17b. By using infrared microscopy, the alignment of stacked dies can be precisely examined, ensuring accuracy during the evaluation process. It can be observed that the misalignment between the top and bottom dies is below $\sim 1\ \mu\text{m}$, which is significantly lower than the estimated misalignment tolerance of $3.5\ \mu\text{m}$ ($\Phi_1/2 - \Phi_3/2$). Such a small misalignment, along with the high accuracy achievable with the TCB approach, confirms the feasibility of applying a bonding pressure of 75 MPa to facilitate flip-chip integration.

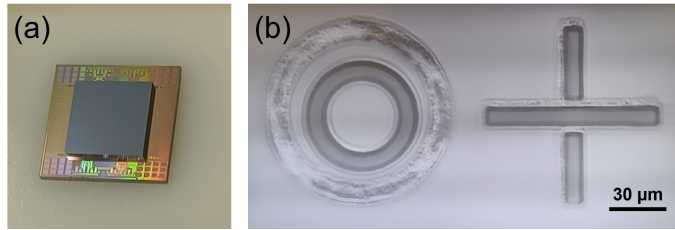


Figure 5.17: (a) A photo of stacked die after bonding in air. (b) an infrared microscope image of the alignment marker on top and landing die.

Effect of Process Temperature on Die Shear Strength

Fig. 5.18 displays the shear strength for bonded dies at different bonding temperatures under the same bonding pressure of 75 MPa and the same bonding time of 15 min in ambient conditions. It is evident that temperature significantly enhances shear strength. The sintering parameters from the DOE and the measured shear strengths are shown in the Table 5.1. It was observed that the shear force was insufficient (below $\sim 1\ \text{kgf}$) to be obtained through bonder testing when the sample was sintered at 180 °C. When the stacked chips were bonded at 210 °C, the shear strength was measured to be 6 MPa, indicating the limits of acceptable mechanical integrity for the stacked chips. Therefore, the lowest sintering temperature of 210 °C can serve as the initial benchmark for determining sintering parameters in future studies. Increasing the sintering temperature to 240 °C resulted in a shear strength of 26 MPa, representing a 300% increase. Further increasing the sintering temperature to 280 °C led to an even higher shear strength of 38 MPa. It was also observed that the standard deviation increased as the temperature rose to 280 °C. Notably, the standard deviation of shear strength at this temperature

was very high. This is assumed to be due to increased substrate warpage caused by the higher temperature.

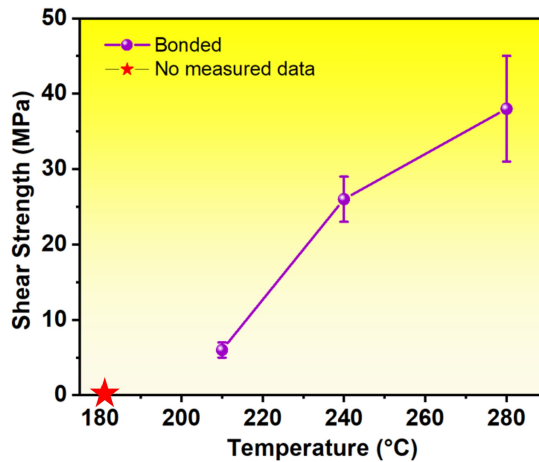


Figure 5.18: (a) Shear strength for the stacked dies with different bonding temperature under bonding pressure of 75 MPa and bonding time of 15 min after TCB process.

Effect of Process Pressure on Die Shear Strength

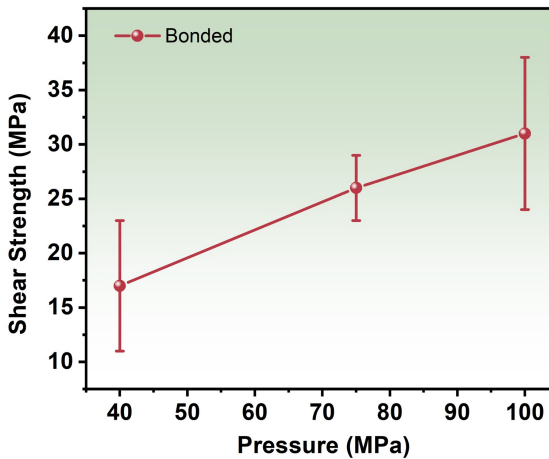


Figure 5.19: (a) Shear strength for the stacked dies with different bonding pressure under bonding temperature of 240 °C and bonding time of 15 min after TCB process.

The curve of shear strength is depicted in Fig. 5.19 in relation to different sintering pressures. The impact of pressure on bonding strength was examined by sintering three groups of samples at 240 °C for 15 min under sintering pressures of 40, 75, and 100 MPa, respectively. The mean shear strength improved from less than 20 MPa to 26 MPa as the sintering pressure increased from 40 MPa to 75 MPa, representing an increase of approximately 44%. Further increasing the sintering pressure to 100 MPa resulted in a shear strength of 31 MPa, corresponding to a 20% increase.

Comparison of Shear Strength

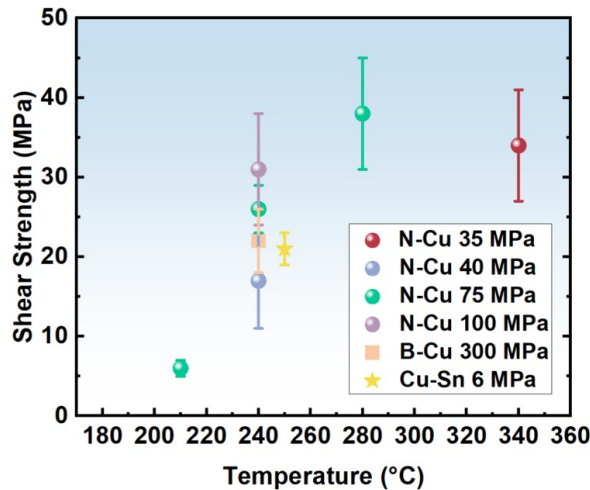


Figure 5.20: Comparison of shear strength among CuNP interconnects, B-Cu interconnects, and solder interconnects. The red dot represents the reference threshold conditions for the interconnection strength of sintered CuNPs. The pink square indicates the shear strength of B-Cu to Cu UBM interconnects. The yellow star represents the strength of Cu-Sn-based interconnects.

Fig. 5.20 provides an overview of the shear strength comparison results. In addition to investigating the influence of sintering temperature and pressure on the flip-chip shear strength of CuNP-sintered joints, we conducted additional tests involving the integration of Cu UBM with solder joint flip-chips and Cu μ bumps.

As described in Sec. 5.2.3, the solder joint integration was achieved using TCB at a pressure of 6 MPa and a temperature of 250

$^{\circ}\text{C}$ for 2 min, resulting in a measured shear strength of 21 MPa. This value falls within the range of shear strengths observed for CuNP-sintered joints at 240°C under pressures of 40 MPa and 75 MPa, which varied from less than 20 MPa to 26 MPa, respectively. The results indicate that sintered CuNP joints require a minimum sintering pressure of 40 MPa to achieve comparable shear strength at a sintering temperature 10°C lower than that of solder joint flip-chips. The standard deviation of CuNP joints is noticeably higher than that of solder joints, which can be attributed to the significantly higher process pressure used in TCB compared to the solder joint integration process.

The direct bonding of Cu UBM to Cu μbumps was performed at the same temperature of 240°C as the CuNP joint integration process but under a much higher process pressure of 300 MPa. Notably, the Cu μbumps were not pre-treated with CMP. The measured shear strength was 22 MPa, which falls within the range of shear strengths observed for CuNP-sintered joints at 240°C , between pressures of 40 MPa and 75 MPa. It should be noted that this bonding process was carried out under 4–7.5 times higher pressure than that of the CuNP sintering process. This finding suggests that Cu-to-Cu direct bonding using NP sintering technology significantly reduces the required TCB process pressure compared to B-Cu direct bonding without CMP treatment, making it more suitable for integrating fragile low-k materials.

To establish benchmark conditions for further sintering studies on CuNP-sintered joints, we conducted a supplementary test, setting the sintering process at 35 MPa and 340°C , to determine the maximum sintering temperature and minimum sintering pressure. The shear strength was approximately 34 MPa, which was slightly higher than the result for CuNP sintering at 100 MPa and 240°C but slightly lower than that at 75 MPa and 280°C . Moreover, when comparing this result to the minimum sintering pressure of 40 MPa at 240°C , the shear strength was significantly higher, exceeding it by more than 40%. This comparison demonstrates that for the in-air sintering process, temperature has a greater impact on bonding strength, with higher temperatures significantly enhancing sintering. Meanwhile, sintering pressure plays a critical role at lower temperatures (240°C), but when the pressure exceeds 75 MPa, its effect becomes less pronounced. No

noticeable changes in oxidation levels were observed at sintering temperatures exceeding 250 °C in air in previous studies [21]. We recommend increasing the sintering temperature appropriately to reduce the sintering pressure, thereby preventing low-k IC chips from cracking. To mitigate oxidation issues, the process can be conducted in a vacuum or a reducing atmosphere.

5.3.3. Microstructural analysis of sintered CuNPs

As discussed in Sec. 5.3.2, the sample that was sintered at 180 °C did not achieve sufficient shear force in bonder testing. To further investigate the bonding results at the lowest bonding temperature of 180 °C, we polished the integrated sample for cross-sectional inspection. The microstructure of sintered CuNPs was observed by using FIB/SEM, as shown in Fig. 5.21. It can be seen that the top chip and the bottom have been bonded successfully, and the alignment accuracy is sufficient for pitch level of 20 μm under bonding pressure of 75 MPa. At the lowest temperature, CuNPs agglomerate and come into contact with each other, only a few adjacent NPs are slightly sintered, forming short sintering necks. Meanwhile, there are some voids at the bonding interface. For the prepared CuNP paste, organic compounds can only evaporate completely above 230 °C [22]. Therefore, a significant amount of organic additives remain inside the CuNPs, hindering the sintering process at lower temperature.

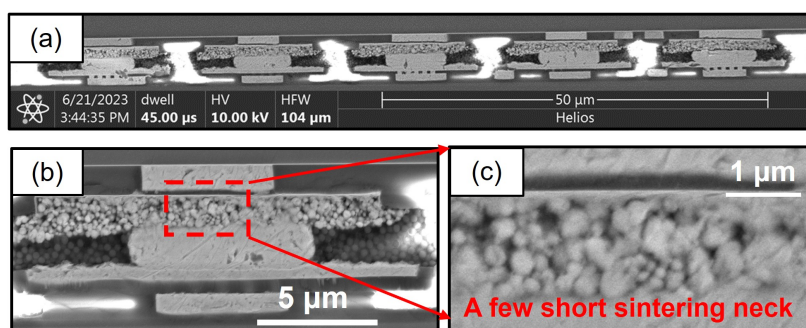


Figure 5.21: SEM images of the cross section of the integrated chip with sintering parameter of 180 °C, 75 MPa and 15 min. (a) Distribution of 20 μm pitch CuNP interconnects, (b) one bonded bump featuring CuNPs and (c) an enlarged image illustrating bonding interface and the morphology of NPs, indicated in the red dashed box in (b).

Interface Fracture

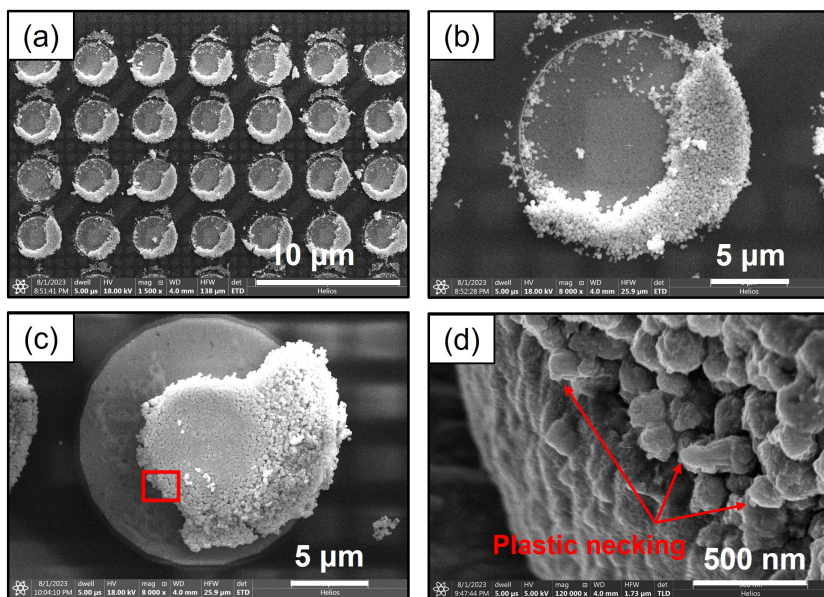


Figure 5.22: SEM images of fracture surfaces after shear test on the bottom substrate (a,b) and on the top chip (c,d). The sintering parameters were 240 °C, 75 MPa and 15 min.

The fracture mode of an in-air bonded flip-chip was investigated by observing the fracture surface morphologies of sample sheared off using SEM. First, the surface of the sheared samples was examined to demonstrate the fracture morphology of CuNP interconnects at a bonding temperature of 240 °C, as shown in Fig. 5.22. The top views of the sheared-off bottom substrate are shown in Fig. 5.22a and b. It can be seen that each cavity has partially patterned CuNPs and exposed TaN/Cu-covered cavity surface. Since the Cu μ bumps were not in contact with the residue parts of the patterned CuNPs, pressure was not applied to the residue CuNPs during the sintering process. Fig. 5.22c demonstrates the fracture morphology of the top chip, which is capped with CuNPs. It can be observed that CuNPs have already developed a significant network area. Fig. 5.22d shows that fracture occurs inside the CuNPs layer at the edge of the Cu μ bump, which is the magnified area as indicated by red frame in Fig. 5.22c. It is identified that the sample exhibits plastic deformation necking in

the regions where fracture occurred inside the CuNP bump, as highlighted by the red arrows.

As previously mentioned, adhesive fractures were observed in all interconnects within the same stacked sample, occurring at the interface between the sintered CuNPs and the TaN/Cu-covered cavity surface, as demonstrated in Fig. 5.23. The stacked chips were subjected to horizontal shear, which caused the sintered CuNP bump in the Cu μ bump contact area to peel off from the bottom substrate surface, resulting in a horizontally oriented fracture surface on the top chip. Additionally, the sintered CuNP bump simultaneously generated a vertically oriented fracture surface at the edge of the Cu μ bump, and plastic deformation was observed, as shown in Fig. 5.22(d).

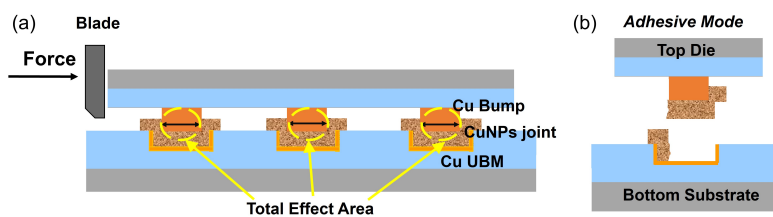


Figure 5.23: Schematic diagram of shear test (a) and adhesive mode of shear test fracture (b)

Fig. 5.24a and b depict the fracture surfaces of the bottom substrate sintered at 240 °C with 100 MPa and at 280 °C with 75 MPa, respectively. The bottom substrates of both samples exhibit residual CuNP bumps and exposed cavities, showing the same fracture mode as described in Fig. 5.23b, indicating an adhesive mode. Fig. 5.24c and d present the sheared-off top chips for the samples processed at 100 MPa and 240 °C, and 75 MPa and 280 °C, respectively. Fig. 5.24e and f show magnified images of the fracture surface morphologies, as indicated by the blue frame in Fig. 5.24c and the purple frame in Fig. 5.24d. A brittle fracture process is inferred from the observation of relatively flat facets on the CuNP surfaces in these two samples, as highlighted by red arrows. The orange arrows indicate that the sample sintered at 100 MPa and 240 °C has a sintering network with large-scale connected sintering necks in Fig. 5.24c. In the sample that was sintered at 75 MPa and 280 °C, there are some long sintering

necks (which are indicated by yellow arrows) but there is no large-scale sintering network, as demonstrated in Fig. 5.24d.

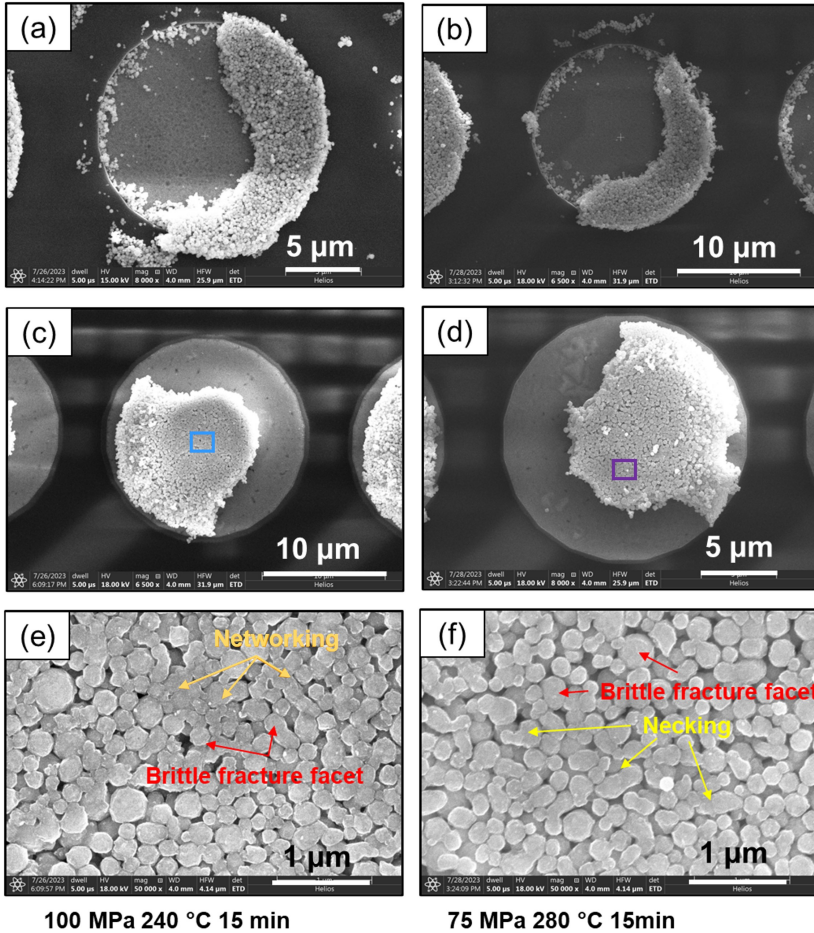


Figure 5.24: SEM images of fracture surfaces after shear test on the bottom substrate (a) and (b), and on the top chip (c)-(f). The samples were sintered for 15 min with different sintering temperature and pressure: (a), (c) and (e) 240 °C, 100 MPa; (b), (d) and (f) 280 °C, 75 MPa.

Based on the observations mentioned above, each sample exhibits the same adhesive fracture mode, although there are variations in the number and length of sintering necks. These differences are related to the sintering pressure and temperature, which will be discussed in the subsequent part concerning the microstructural evolution of cross-sections. During the sintering process, enhanced Cu diffusion

occurs at the Cu-Cu interface between the CuNP bumps and Cu μ bumps on the top chip, resulting in stronger adhesion compared to the bond between CuNPs and TaN/Cu pads. As a result, most fracture behaviour occurs between the CuNPs and the bottom substrate. The same adhesive fracture mode can be the reason why the shear strength of all samples is below 40 MPa [15], [23].

Cross-section Evolution

Next, the SEM cross-sectional images of the sintered joint on the sheared-off top chip were used to analyse the microstructure of the sintered CuNPs and to examine the interface diffusion between CuNPs and Cu μ bumps at different bonding temperatures. The cross-section was created by milling the top die with FIB, followed by imaging with SEM, as depicted in Fig. 5.25.

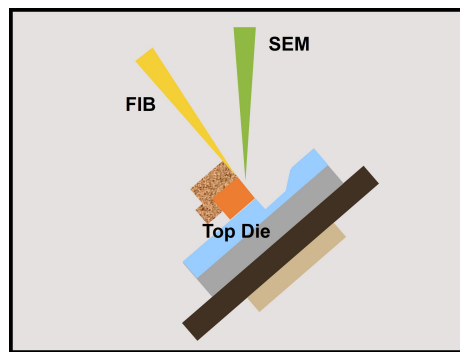


Figure 5.25: A schematic diagram of cross-section preparation using SEM-FIB

Fig. 5.26a-c demonstrate that the morphology of both the sintered CuNPs layer and the bonding Cu-Cu interface is significantly affected by the different bonding pressure of 40, 75 and 100 MPa at 240 °C for 15 min, respectively. It can be observed that at a bonding pressure of 40 MPa, some short sintering necks on the CuNPs layer and numerous small voids are present on the Cu-Cu interface. Also, there are transparent substances present between numerous adjacent NPs that are caused by the residue of organic matter [22]. As the bonding pressure increases to 75 MPa, the sintering necks lengthen and increase in number, as indicated by red dashed circles, while the number of small voids decreases, as marked by orange dashed circles. Furthermore, the sintering neck length of this sample is significantly

longer than that observed at 180 $^{\circ}\text{C}$ with the same pressure of 75 MPa, as shown in Fig. 5.21c. However, due to the weak sintering networking, the bonding strength was only around 26 MPa. By continuously adding the bonding pressure to 100 MPa, the sintered necks expands, forming a large-scale network as shown by the red dashed circles. The size of the small voids observed at the Cu-Cu interface under 100 MPa decreases with those observed at 75 MPa.

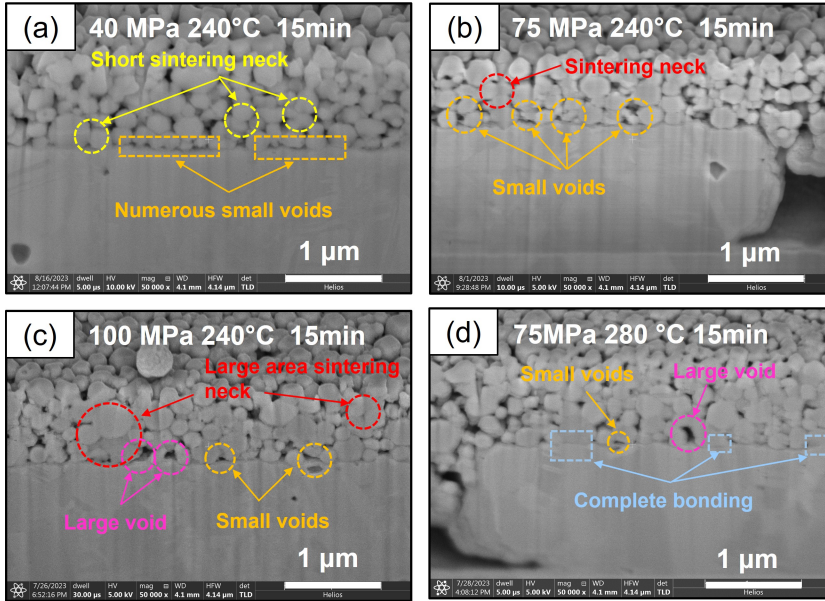


Figure 5.26: SEM images of cross-section morphology with different bonding pressure and temperature for 15 min: (a) 75 MPa, 240 $^{\circ}\text{C}$, (b) 75 MPa, 280 $^{\circ}\text{C}$, (c) 40 MPa, 240 $^{\circ}\text{C}$, and (d) 100 MPa, 240 $^{\circ}\text{C}$.

In addition, the cooperative effect of pressure and temperature on the microstructure was further studied by inspecting and analyzing the cross-section of the sample sintered at 280 $^{\circ}\text{C}$ with 75 MPa. As depicted in Fig. 5.26d, a robust sintering network is observed in the sintered CuNPs layer. The number of interfacial voids decreases with increasing bonding temperature, and there are some intact bonding areas on the Cu-Cu interface, as marked by blue dashed boxes. According to observations for the in-air bonding, bonding pressure has a larger impact on the formation of sintering networking between NPs, with higher pressure resulting in a significant increase in the number of sintering necks. The interface between CuNPs and the Cu

surface is primarily affected by bonding temperature. Higher temperature facilitates the completion of interfacial bonding. We believe that with proper copper oxide cleaning of Cu bumps, the results will be significantly improved and optimization is on-going.

Fig. 5.27 displays the connection and distribution of CuNPs that were analyzed using ImageJ on a selected area of $2.5 \times 0.6 \mu\text{m}^2$ from the cross-sectional SEM images in Fig. 5.26. Subsequently, the porosity value of each sample can be measured. The highest porosity of 18% is observed in large-sized pores at a lower sintering pressure of 40 MPa. As the sintering pressure increases to 75 MPa and 100 MPa, the pore size gradually decreases to 14.5% and 9.4%, respectively. Furthermore, it can also be inferred that temperature has a greater impact on the porosity than pressure. The porosity is reduced from 18% to 8.2% by increasing the temperature to 280 °C, indicating that most of the pores are already isolated. Shrinkage occurs in the sintered CuNPs layer when porosity levels are lower than 10%, and pores are primarily compressed and exhibit a trend of vertical orientation, indicating that the process is anisotropic.

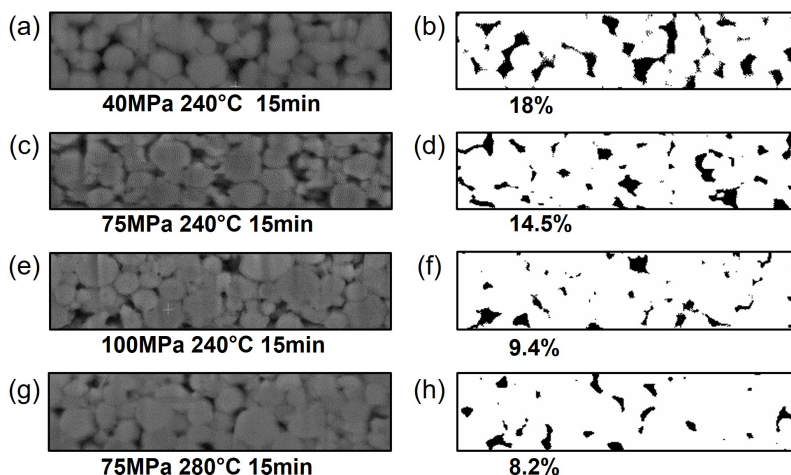


Figure 5.27: Schematic representation of porosity for different sintering parameters was obtained using SEM images. (a), (c), (e) and (g) represent cross-sectional SEM images with dimensions of $2.5 \times 0.6 \mu\text{m}^2$. (b), (d), (f) and (h) represent the corresponding binary images.

5.4. Conclusion

In this work, CuNP paste was applied for 20 μm pitch interconnects, and the patterning process proved feasible for enhancing the integrity and bonding strength of flip-chip integration, making it suitable for 3D integration. An array of CuNP bumps was prepared for subsequent bonding processes and mechanical property characterization. The height of the patterned bumps is determined by the thickness of the applied photoresist. Although the surface of the bumps is highly rough, it enables the integration of the top chip and bottom substrate without the need for CMP, and the sliding between the top and bottom chips after bonding remained within alignment tolerances.

Mechanical performance was evaluated using die shear tests. The sample sintered at 180 °C did not form effective sintering necks; therefore, this stacked sample exhibited no bonding strength. A sintering temperature of 210 °C is defined as the minimum benchmark for achieving sintering strength. The parameter combination of 280 °C, 75 MPa, and 15 min yielded the highest bonding strength of 38 MPa. In the in-air integration process, temperature plays a significant role in enhancing bonding strength. In this study, bonding at 350 °C with 35 MPa resulted in even higher bonding strength than bonding at 240 °C with 100 MPa. The CuNP-sintered joints achieved bonding strength comparable to solder joint flip-chip integration while significantly reducing the required bonding pressure compared to conventional Cu-to-Cu direct bonding.

The fracture mode of all interconnects was adhesive, with fractures mainly occurring at the interface between the TaN/Cu bottom substrate and the CuNP bumps. The formation of sintering networks between NPs is significantly influenced by bonding pressure in in-air bonding, with higher bonding pressure leading to a substantial increase in the number of sintering necks. The interface between the CuNPs and the Cu surface is greatly affected by bonding temperature, and the number of interfacial voids decreases as the bonding temperature increases.

This work confirmed the feasibility of LSP-patterned CuNPs for all-Cu interconnects. Updated samples will be evaluated for their electrical performance. Due to the limitations of the bonding tool,

this experiment was conducted in air. Future research will focus on improving methods in forming gas environments to prevent Cu oxidation.

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6

Conclusions and Recommendations

6.1. Conclusions

The research presented in this thesis aimed to develop a **innovative method for transferring CuNPs in patterns** to create high-density metallic interconnects crucial for advanced chip integration. A novel method for patterning CuNPs for flip-chip integration was developed, where the thickness of CuNP interconnects determined by photoresist thickness and sintering parameters. It highlights the **LSP process**, which uses photoresist stencils to precisely and efficiently transfer CuNPs, resulting in accurate and high-throughput metallic interconnect patterns. The optimized LSP process, combining NP technology with lithographic precision, potentially offers significant improvements over traditional methods in terms of accuracy, cost-efficiency, and throughput. These advancements are pivotal for the next generation of electronic devices, supporting miniaturization and efficiency in semiconductor manufacturing.

To validate the feasibility of the LSP method, several applications, researched in this work demonstrates the feasibility of this technique, including a method for low-temperature bonding of sapphire to silicon using CuNP paste joints. The process also integrates a wafer-scale all-Cu interconnection approach with photopatternable polymer underfill, allowing the epoxy-based photoresist to function as both a stencil and a permanent underfill material. Additionally, a new nanofabrication method utilizing spark ablation and lift-off techniques produces nanoporous films of Au and zinc oxide with fine resolutions down to 2 μm and resistivities of $2.07 \times 10^{-5} \Omega \cdot \text{cm}^{-1}$ for Au. The spark ablation method complements stencil printing by offering additional flexibility in fabricating required nanoporous structures.

To further assess the effectiveness of CuNPs in interconnect applications, the **mechanical and electrical performance characterization of sintered Cu bumps** was investigated. Higher sintering pressure increased compression of the sintered bumps, allowing greater flexibility in interconnect form and thickness. Mechanical properties were evaluated using CSM nanoindentation, revealing that shorter sintering times improved homogeneity and productivity. Optimal sintering conditions were identified as 260°C for 15 min at 25 MPa, yielding the highest Young's modulus of 126 GPa. The sintered CuNPs exhibited a nanoporous structure with

slight oxidation, making them more ductile than B-Cu. This enables a compressible pillar structure, which accommodates more chip topography in flip-chip assembly processes. The resistivity of sintered CuNPs is $9.2 \times 10^{-6} \Omega \cdot \text{cm}$, five times that of B-Cu, but the ductile nature of the CuNPs enables an optimized interconnect structure to compensate for this. These findings provide a high-throughput solution for CuNP bump patterning in flip-chip integration applications.

The CuNP paste was further applied to fabricate **20 μm pitch interconnects**, enhancing the integrity and bonding strength crucial for flip-chip integration in 3D applications. Despite the rough surface of the bumps, integration between the top chip and bottom substrate was achieved without the need for CMP, maintaining alignment tolerances. Mechanical performance evaluations revealed that a sintering temperature of 210 °C is the minimum required for effective bonding, with the optimal conditions of 280 °C, 75 MPa, and 15 minutes yielding a maximum bonding strength of 38 MPa. Notably, bonding at 350 °C with 35 MPa surpassed the strength of joints bonded at lower temperatures with higher pressure. The CuNPs sintered joints exhibited bonding strengths comparable to solder joints while significantly reducing the required bonding pressure compared to traditional Cu-to-Cu direct bonding. The adhesive fracture mode primarily occurred at the interface between the TaN/Cu substrate and the CuNP bumps, with higher bonding pressures resulting in more sintering necks and fewer interfacial voids as bonding temperatures increased.

The research was successful in addressing the challenge of creating a high-throughput, flexible, and effective method for CuNP-based interconnects, with the goal of achieving fine-pitch bonding and strong mechanical performance. By implementing the findings, CuNP sintering can be a viable alternative to conventional interconnect methods and provide a scalable solution for next-generation all-Cu interconnect for semiconductor packaging technologies.

6.2. Recommendations for Future Work

The outlook for future research based on the findings of this thesis is promising, with several key areas identified for further exploration. A critical next step is scaling the demonstrated LSP and NP sintering techniques for mass production. While the processes developed in this research have proven effective in controlled laboratory environments, their reliability, yield, and cost-effectiveness must be optimized for high-volume manufacturing. Additionally, long-term reliability studies are essential to evaluate the mechanical and electrical performance of CuNP interconnects under extended operational conditions. Specifically, future work should focus on assessing their anti-EM properties, high-temperature aging resistance, thermal cycling/shock resilience, and mechanical vibration resistance. These evaluations are crucial for ensuring the robustness and durability of the technology in further applications.

Exploring alternative materials beyond Cu, such as Au NPs, which can be applied in Photonics Integration, could also provide new opportunities. These materials may offer superior conductivity or thermal management properties, making them suitable for specialized applications. The integration of CuNP interconnects with emerging technologies like high-performance computing, 5G, and AI systems presents another promising avenue. These fields demand increasingly smaller, faster, and more reliable electronic components, and CuNP-based interconnects could be an ideal solution. Future research should also investigate their potential integration with advanced packaging technologies like wafer-level packaging and SiP to further enhance performance and miniaturization.

Another area for further investigation is the improvement of sintering processes in controlled environments, particularly in inert gases, to prevent copper oxidation. This approach could reduce bonding time, increasing units per hour, while enhancing the mechanical and electrical properties of CuNP interconnects. In general, the future research directions identified in this thesis pave the way for more efficient, scalable, and reliable interconnect technologies, which are essential for advancing the next generation of high-performance electronic devices.

A

Design Layout

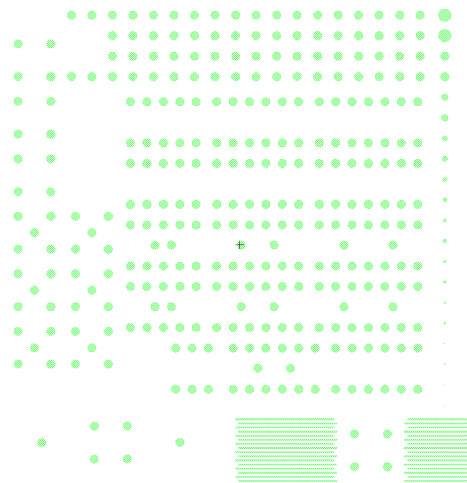


Figure A.1: Mask for CuNP pattern transfer with a diameter of 100 μm

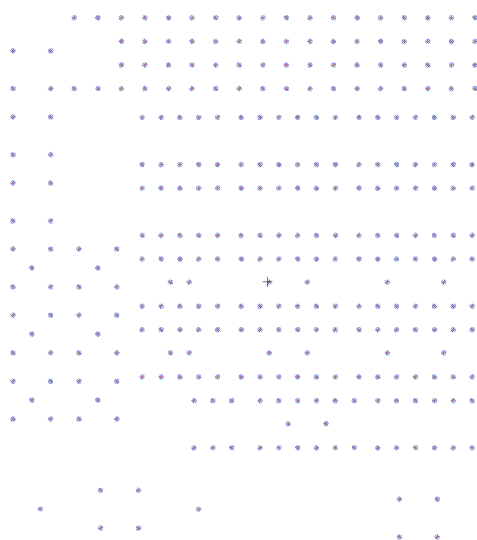


Figure A.2: Mask for CuNP pattern transfer with a diameter of 50 μm



Figure A.3: Mask for CuNP pattern transfer with a diameter of 20 μm

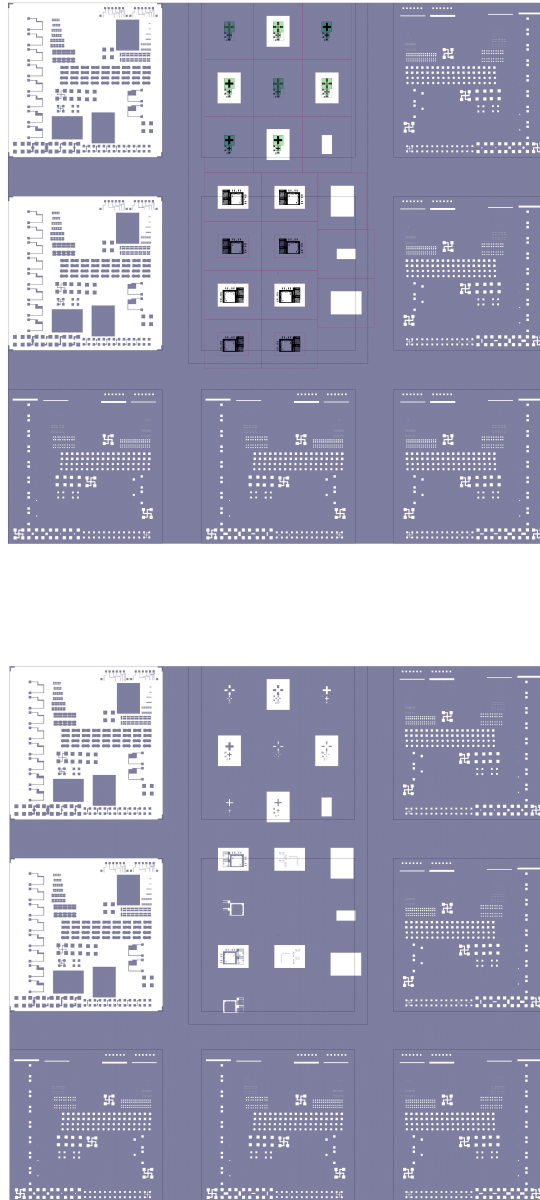


Figure A.4: Designed reticle for Cu-to-Cu direct bonding with photopatternable underfill films

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- | | |
|------|--|
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List of Publications

Journal Papers

3. **Xinrui Ji**, Leiming Du, Henk van Zeijl, Guoqi Zhang, Jaber Derakhshandeh and Eric Beyne, *20 μm Pitch Cu-to-Cu Direct Bonding via Nanoparticle Sintering: A Comparative Study with Solder and Bulk Copper Interconnects for High-Density Integration*, Under Review.
2. Leiming Du, Kai Liu, Dong Hu, Olof Bäcke, Xiao Hu, **Xinrui Ji**, Jiajie Fan, René H. Poelma, Magnus Hoernqvist Colliander and Guoqi Zhang, *Microstructural and micromechanical anisotropy in pressure-assisted sintered copper nanoparticles*, *Acta Materialia* **287**, 115180 (2025).
1. **Xinrui Ji**, Leiming Du, Shan He, Henk van Zeijl and Guoqi Zhang, *Microstructural and micromechanical characterization of sintered nanocopper bump for flip-chip heterogeneous integration*, *Microelectronics Reliability* **150**, 115180 (2023).

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5. Leiming Du, **Xinrui Ji**, Kai Liu, Jiajie Fan and Guoqi Zhang, *Investigating Coalescence Kinetics in Cu Nanoparticle by Molecular Dynamics and 3D Reconstruction*, *International Conference on Electronic Packaging Technology (ICEPT)*, Tianjin, China, August 2024.
4. **Xinrui Ji**, Leiming Du, Henk van Zeijl, Guoqi Zhang, Jaber Derakhshandeh and Eric Beyne, *20 μm pitch Cu-to-Cu flip-chip interconnects through Cu nanoparticles sintering*, *IEEE 74rd Electronic Components and Technology Conference (ECTC)*, Denver, U.S., May 2024.
3. **Xinrui Ji**, Henk van Zeijl, Weiping Jiao, Shan He, Leiming Du and Guoqi Zhang, *Low temperature fine pitch all-copper interconnects combining photopatternable underfill film*, *IEEE 73rd Electronic Components and Technology Conference (ECTC)*, Orlando, U.S., May 2023.

2. **Xinrui Ji**, Henk Van Zeijl, Joost Romijn, Hendrik Joost Van Ginkel, Xu Liu and Guoqi Zhang, *Low Temperature Sapphire to Silicon Flip Chip Interconnects by Copper Nanoparticle Sintering*, [IEEE 9th Electronics System-Integration Technology Conference \(ESTC\)](#), Sibiu, Romania.
1. **Xinrui Ji**, Hendrik Joost van Ginkel, Dong Hu, Andreas Schmidt-Ott, Henk van Zeijl, Sten Vollebregt and Guoqi Zhang, *Patterning of fine-features in nanoporous films synthesized by spark ablation*, [IEEE 22nd International Conference on Nanotechnology \(IEEE-NANO\)](#), Mallorca, Spain, July 2022.