Ultra-low-power, class-AB, CMOS four-quadrant current multiplier

C. Sawigun and W.A. Serdijn

A class-AB four-quadrant current multiplier constituted by a class-AB current amplifier and a current splitter which can handle input signals in excess of ten times the bias current is presented. The proposed circuit operation is based on the exponential characteristic of BJTs or subthreshold MOSFETs. The multiplier is designed using the latter devices and achieves very low power consumption. Simulation results show that from a 0.65 V supply, the proposed circuit consumes 12.4 nW static power while less than −30 dB total harmonic distortion is achieved for an input modulation index up to 10.

Introduction: Based on the well-known exponential characteristics of BJTs or weak inversion MOSFETs, four-quadrant current multiplier circuits have been designed from different principles, e.g. transconductor/conveyor based [1] and translinear circuit based [2] current multipliers. Most of them are restricted to class-A operation that does not allow the input signals' swing to become higher than their bias currents.

In this Letter, a fully class-AB four-quadrant analogue current multiplier is presented. The proposed multiplier is formed by a dual output current amplifier which is biased by controlled currents generated from a current splitter. Both the amplifier and splitter circuits can be realised from the same basic circuit block, called Sinh transconductor, which provides class-AB operation. Therefore, fully class-AB multiplication is obtained. Owing to the class-AB operation, the multiplier circuit can be designed to process high input signal amplitudes while its bias current can be kept low. Circuit simulation using a 0.13 μm model parameter shows that, for a 0.5 nA bias current, input currents with amplitudes of 5 nA can be applied to the circuit and good four-quadrant multiplication is performed.

Proposed class-AB current multiplier: Fig. 1 shows the block diagram of the proposed multiplier. It comprises three identical current controlled nonlinear transconductors, G_o, G_A, G_B, forming a dual output current amplifier and a class-AB current splitter supplying controlled currents I_A and I_B to the output transconductors of the current amplifier. For the case that the I–V characteristic of each transconductor is a strictly monotonic function, described by

$$I_{\text{out}} = I_o f(V_+ - V_-) \tag{1}$$

where I_o is a bias current, the output current of the multiplier can be found to be

$$I_{\text{out}} = I_{\text{out1}} + I_{\text{out2}} = \frac{I_A - I_B}{I_o} I_{\text{in1}} \tag{2}$$

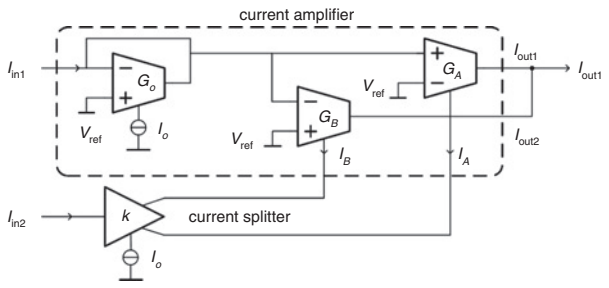

Fig. 1 *Current multiplier block diagram*

It can be seen from (2) that the gain of the amplifier is controlled by the bias current of the input transconductor (connected as a nonlinear input resistor) and the difference between the bias currents of the output transconductors. In this case, I_o is a constant current but I_A and I_B are generated from another input current, I_{in2}, via the current splitter, according to the following relation

$$I_{\text{in2}} = k(I_A - I_B) \tag{3}$$

Substituting (3) into (2), we arrive at

$$I_{\text{out}} = \frac{k}{I_o} I_{\text{in1}} I_{\text{in2}} = A I_{\text{in1}} I_{\text{in2}} \tag{4}$$

We thus obtain a four-quadrant multiplication from the circuit in Fig. 1 with a conversion gain of $A = k/I_o$. In CMOS technology, the multiplier can be designed to operate in class-AB by employing the exponential behaviour of subthreshold devices to design the transconductors and the current splitter which will be described in the following section.

Class-AB circuit building blocks: Fig. 2*a* shows the nonlinear class-AB transconductor which can be directly substituted for G_o, G_A and G_B of Fig. 1. Using the exponential relationship of MOSFETs operating in weak inversion [3], we can find the input–output relation of each transconductor as

$$I_{\text{out}} = 2I_o \sinh\left(\frac{V_+ - V_-}{nV_T}\right) \tag{5}$$

where n is the subthreshold slope factor and V_T is the thermal voltage. This relationship complies with (1) and provides class-AB operation.

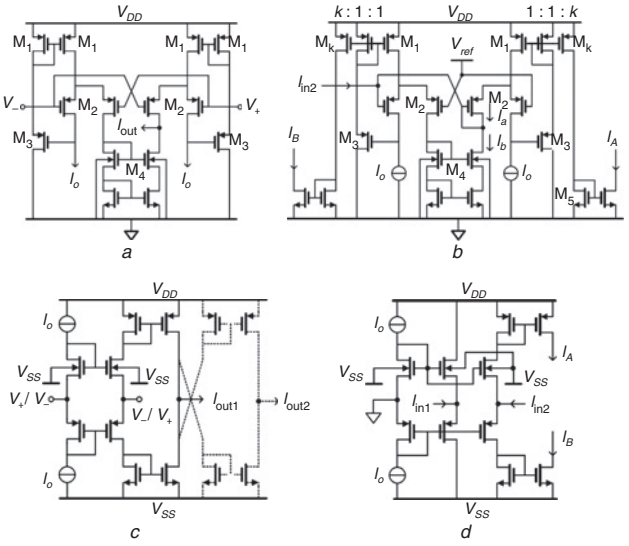

Fig. 2 *Circuit building blocks*

a Sinh transconductor
b Sinh-based class-AB current splitter
c Complementary Sinh transconductor
d Complementary class-AB current splitter

Based on the same circuit topology, connecting the transconductor in a negative feedback scheme, we obtain the current splitter shown in Fig. 2*b*. Driven by the up-down translinear loop topology formed by a set of transistors M2 and a unity gain cascode current mirror M4, input current I_{in2} which is applied at inverting input node, is converted into two components, I_a and I_b, under the condition that $I_{\text{in2}} = I_a - I_b$ and $I_o^2 = I_a I_b$. Then the split currents (I_a and I_b) are superimposed on bias current I_o and copied by the scaled current mirrors, M1–Mk, and their polarities are reversed again by unity gain current mirrors M5 resulting in I_A and I_B which will be delivered to G_A and G_B, respectively.

Another way to design the Sinh transconductor and current splitter is shown in Figs. 2*c* and *d*, respectively. This approach employs complementary devices to implement the same translinear loop equation and thus suffers from different subthreshold slopes owing to the body effect of the NMOS devices, something which is unavoidable in standard CMOS processes [4]. Hence, we choose the circuits in Figs. 2*a* and *b* to validate our design.

Simulation results: The multiplier in Fig. 1 was substituted by the circuit blocks in Figs. 2*a* and *b* and simulated in Cadence using RF spectre and 0.13 μm CMOS model parameters. Transistor widths (W) and lengths (L) are given in Table 1. $V_{DD} = 0.65$ V, $V_{\text{ref}} = 0.4$ V, and $I_o = 0.5$ nA. The quiescent power of the entire circuit equals 12.4 nW.

Table 1: Transistor dimensions

MOSFET	M_1	M_2	M_3	M_4	M_5	M_k
W/L (μm/μm)	1/1	4/4	1/10	2/2	2/2	2/4

The transient response illustrating the four-quadrant multiplication of a 5 nA, 2 kHz, sinusoidal current I_{in1} (modulation index, MI = 10) and a

5 nA, 100 Hz, sinusoidal current I_{in2} (MI = 10) performed by the proposed multiplier is shown in Fig. 3. To examine the circuit linearity, a circuit simulation of the total harmonic distortion (THD) has been performed by varying the amplitude of the 2 kHz, sinusoidal I_{in1} from 1 to 5 nA ($2 \leq MI \leq 10$) and keeping I_{in2} constant at 5 nA. The results shown in Fig. 4 reveal that at an MI of 10, the proposed multiplier provides $\simeq -30$ dB THD.

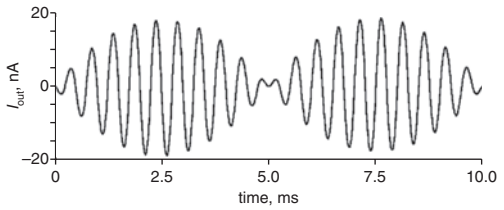

Fig. 3 *Transient response of multiplier*

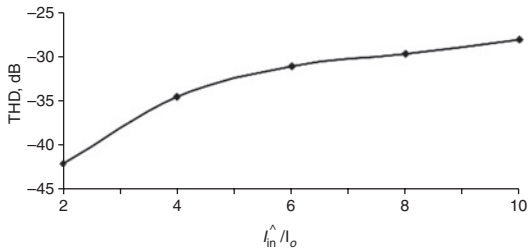

Fig. 4 *Simulated THD against input signal amplitude,* $I_{in2} = 5$ *nA*

Conclusion: A new low-voltage ultra-low-power CMOS four-quadrant current multiplier has been presented. By using a weak inversion Sinh transconductor as a basic cell, fully class-AB multiplication operation is obtained, allowing input signals with a modulation index of 10 to be processed while the circuit power consumption is very low.

18 November 2008
doi: 10.1049/el.2009.3311

C. Sawigun and W.A. Serdijn (*Biomedical Electronics Group, Electronics Research Laboratory, Delft University of Technology, The Netherlands*)

E-mail: c.sawigun@tudelft.nl

References

1 Yuce, E.: 'Design of a simple current mode multiplier topology using a single CCCII + ', *IEEE Trans. Instrum. Meas.*, 2008, **57**, (3), pp. 631–637
2 Chang, C.C., and Liu, S.I.: 'Weak inversion four-quadrant multiplier and two-quadrant divider', *Electron. Lett.*, 1996, **34**, pp. 2079–2080
3 Vittoz, E.A., and Fellrath, J.: 'CMOS analog integrated circuits based on weak inversion operation', *IEEE J. Solid-State Circuits*, 1977, **12**, (3), pp. 224–231
4 Katsiamis, A.G., Glaros, K.N., and Drakakis, E.M.: 'Insights and advances on the design of CMOS Sinh companding filters', *IEEE Trans. Circuits Syst.*, 2008, **55**, (9), pp. 2539–2550