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Original Article

Towards defining a simplified procedure for COTS system-on-chip TID testing

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ABSTRACT

The use of System-on-Chip (SoC) solutions in the design of on-board data handling systems is an important step towards further miniaturization in space. However, the Total Ionizing Dose (TID) and Single Event Effects (SEE) characterization of these complex devices present new challenges that are either not fully addressed by current testing guidelines or may result in expensive, cumbersome test configurations. In this paper we report the test setups, procedures and results for TID testing of a SoC microcontroller both using standard ^{60}Co and low-energy protons beams. This paper specifically points out the differences in the test methodology and in the challenges between TID testing with proton beam and with the conventional gamma ray irradiation. New test setup and procedures are proposed which are capable of emulating typical mission conditions (clock, bias, software, reprogramming, etc.) while keeping the test setup as simple as possible at the same time.

1. Introduction

The availability of multi-million gates Application Specific Integrated Circuits (ASIC) technologies and large Field Programmable Gate Arrays (FPGA) also for radiation hard applications, encourages Hi-Rel electronic units manufacturers to pack very complex systems into single chips [1]. At the same time, the use of Commercial Off-The-shelf (COTS) processors for low-end space applications (educational satellites, cubesats and now in perspective Telecom constellations) is becoming an important challenge for engineers who need to make the suitable architectural choices to guarantee acceptable reliability levels while having little room for silicon-level Rad-hard By Design (RHBD) for those kind of applications (see Refs. [2], [3] and [4] for detailed discussion).

Standard procedures to test TID effects are mostly based on testing damages on discrete devices, like diodes and transistors, and simple integrated circuits [5]. For this kind of devices the test setup is simple, with little ancillary electronics needed [6]. This kind of tests are typically executed with voltages and temperatures of the worst case, to identify the lower boundary in resilience and take some margins for the actual mission [7]. When testing complex SoCs new challenges arise, as emulating real mission functionalities is necessary in order to find which modes of failure will limit the life of the component during the mission. A state-of-the-art SoC contains different memories, high number of I/Os, analog blocks and other internal elements with contrasting worst cases scenarios. Furthermore no complete knowledge, observability and controllability of internal blocks is usually possible. Testing directly with mission-like conditions becomes an interesting option to be investigated at this point. While there is already literature showing TID tests on complex SoCs ([8]–[11]), a standard procedure has not yet been established. One of the main problems is that testing with ^{60}Co makes it really difficult to emulate mission conditions. For example clock and power should be supplied to the Device Under Test (DUT), even if ^{60}Co beam is not directional and ancillary electronics is affected from the source. For this reason, even simple

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TID tests of memories using ^{60}Co can become cumbersome: in order to perform irradiation tests with a high total dose, all sensitive parts except the DUTs must be shielded from the radiation. An example is the testing at ESA-ESTEC reported in Ref. [12], which was performed using a shielding box made of lead and steel. The box (see Fig. 1) weighs about 1300 kg and is assembled from individual parts of about 10 kg–20 kg each. It has several curved channels for feeding electrical wires and water tubes for the cooling system into the box. Previous works have shown the limits of ^{60}Co when a confined irradiation is needed [13] and others describe pros and cons of possible alternatives [14].

Proton sources provide a more confined and directional beam spot compared to ^{60}Co sources, without the need of shielding ancillary electronics. This helps in using typical SoCs modular evaluation boards from the vendor instead of custom designed boards during test setup without major problems, providing a cheaper and faster solution especially for COTS components.

Challenges and solutions for test setups and procedures in case of proton and ^{60}Co sources are presented in this paper, following the novel test methodology proposed in Ref. [15] for the former and following a simplified approach to keep the test setup as simple as possible for the latter. In both cases care will be taken in defining the test setups and procedures in such a way to be able to test the DUT in mission-like conditions.

2. DUT description

The SPC56EL70L5 (Fig. 2) is a microcontroller from STMicroelectronics targeting the electric power steering, chassis and safety applications that require a high safety integrity level in automotive (meeting the ISO 26262 ASILD and the IEC 61508 SIL3) and based on a 90 nm embedded Flash technology. To minimize software redundancy and specific hardware features required to reach this target, dual redundancy is provided for the critical components of the microcontroller in a “Sphere of Replication” (SoR):

- CPU core (e200z4 Power Architecture)
- DMA controller (eDMA)
- Interrupt controller (INTC)
- Crossbar bus system
- Memory Protection Unit
- Flash-memory controller
- SRAM controller
- Peripheral bus bridge (PBRIDGE)

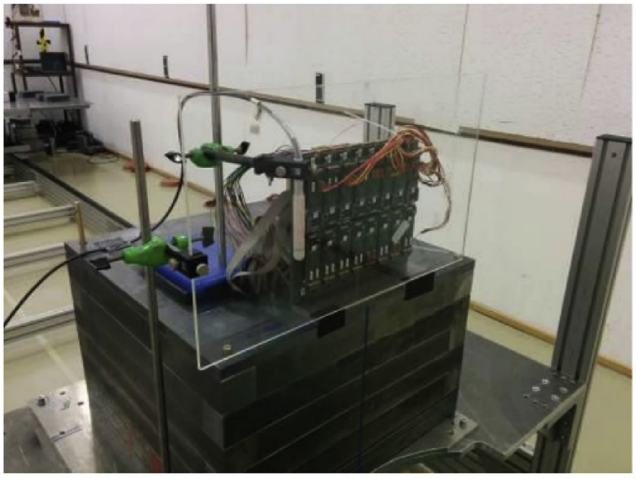

Fig. 1. Test setup used for testing at ESTEC ^{60}Co facility in Ref. [12].

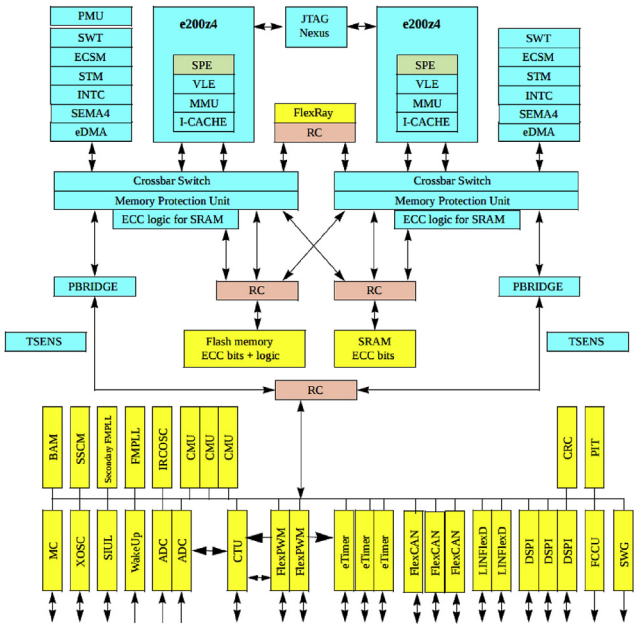

Fig. 2. SPC56EL70L5 block diagram. Cyan: blocks in the redundancy sphere. Red: redundancy checkers. Yellow: peripherals outside of the sphere of replication [16]. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

- System and watchdog timers (STM and SWT)
- Temperature sensor (TSENS)

Lock-step Redundancy Checking Units (RC) are implemented at each output of the SoR to check if there are any mismatches. A programmable Fault Collection and Control Unit (FCCU) monitors the RC and other integrity status flags of the device, reacting to faults both internally (typically causing a reset) and externally (signaling the error). The output of the FCCU are outputted to two pins, and several protocols are available to signal correct or wrong behavior (e.g. two square wave at the same frequency, in-phase or in counter-phase). The device contains many other peripherals outside the SoR, like SPI controllers (DSPI), CAN controllers (FlexCAN), PWM (FlexPWM), timers (eTimer) and internal 12-bit ADCs. For those elements SW techniques must be employed for fault tolerance (e.g. scrubbing). Flash memory (2 MB) and SRAM (192 KB) are available on board and Single Error Correction/Double Error Detection (SEC/DED) is provided for all memories.

2.1. Emulated mission

The use of microcontrollers in space is booming, both thanks to use of commercial components in ‘new space’ endeavors and following the recent release of rad-tolerant and rad-hard components with several more planned for the coming years (see Ref. [2] for a detailed road-map). Microcontrollers are key elements in order to distribute intelligence on satellite platforms or to replace FPGAs in low-demanding instruments. Distributed solutions inherently mitigate Single Points of Failures (SPoF), allow reuse of modular reference designs and of software (even if qualification of software is still more expensive and time consuming than the one for hardware and software reuse is not taken into consideration at the current state of the standards) and reduce cable mass (as shown in the example in Fig. 3). The same trend has been noticed in commercial fields with larger and more competitive markets like automotive [18] and even for aircrafts [19] [20].

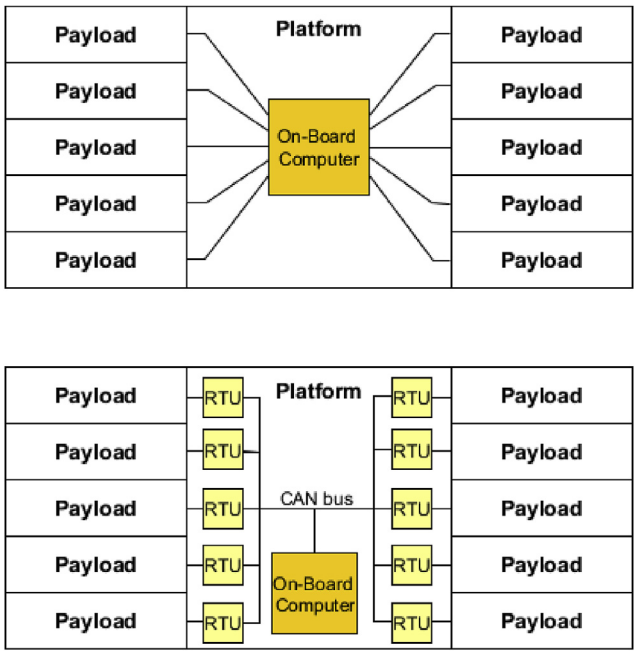

Fig. 3. Above: centralized platform architecture. Below: example of use of microcontrollers on platforms to distribute intelligence on board.

The microcontroller is typically remotely controlled by the On-board Computer (OBC), using remote access protocols (RMAP over SpaceWire (SpW), MIL-STD-1553, commands over SPI, etc.) to either command it as a "slave" without local software running or to reprogram the local software (Application Software and/or boot software in the NVRAM of the device). The microcontroller typically runs simple and repetitive tasks (reading internal and/or external ADCs and/or DACs, communicating using interfaces like CAN and UART and running simple control algorithms). In the case of the selected COTS microcontroller, typical remote memory access for space like MIL-STD-1553 and SpW are not available and large on-board memories are available, making of big interest reprogramming the device occasionally instead of remotely control the microcontroller during the normal operations. The software employed during irradiation and the whole test procedure have to use the resources available in the microcontroller according to the application described, being able to find the critical procedure or block that will limit the life of the component in the targeted mission. Testing the SoC in similar conditions is challenging and special care must be taken in order to keep complexity of the test setup low.

3. ^{60}Co test

3.1. Test facility description: ESTEC ^{60}Co facility

The ESTEC ^{60}Co source consists of multiple small rods about 50 mm long held around the periphery of a 30 mm diameter container. The container is of double-welded steel construction made to the internationally approved standards. The source is stored in its own special housing, built of steel with integral lead shielding. When the source is raised to the irradiation position, the gamma beam produced by the ^{60}Co decay exits the irradiator unit through a collimator window into the radiation cell. The facility (Figs. 4 and 5) consists of the radiation cell a and large external control room with 14 cable feed-throughs that enable the remote monitoring and controlling of experiments [17]. The board is placed in vertical position in front of the source collimator. The dose rate

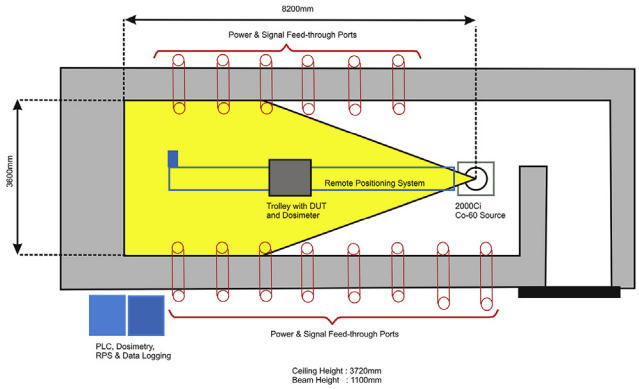

Fig. 4. ESTEC ^{60}Co facility (top) [17].

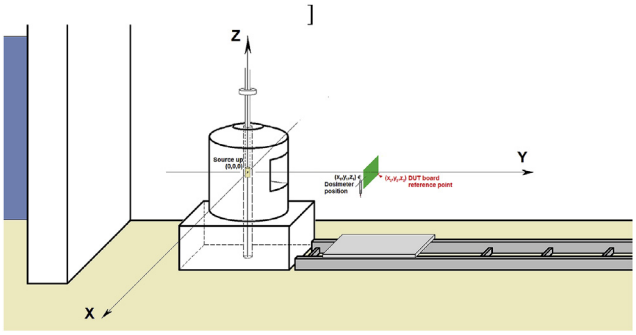

Fig. 5. ESTEC ^{60}Co facility (side) [17].

depends on the distance of the DUT from the source (y in Figs. 5 and 10).

3.2. Test setup

In the general case, an ad-hoc board is required to avoid failures due to other elements on the board with non directional sources like ^{60}Co. In this case the xPC56XLADPT144S commercial board from P&E Microcomputer Systems (shown in Fig. 7) was used to host the DUT, as it was possible to configure this minimodule with jumpers to circumvent the oscillators and voltage regulators on the board, directly providing power and clock from remote ancillary

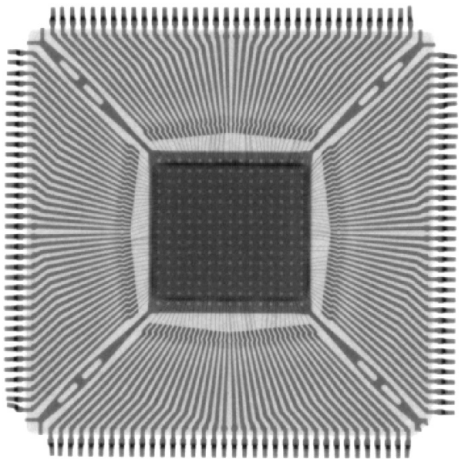

Fig. 6. An X-ray of the DUT (top).

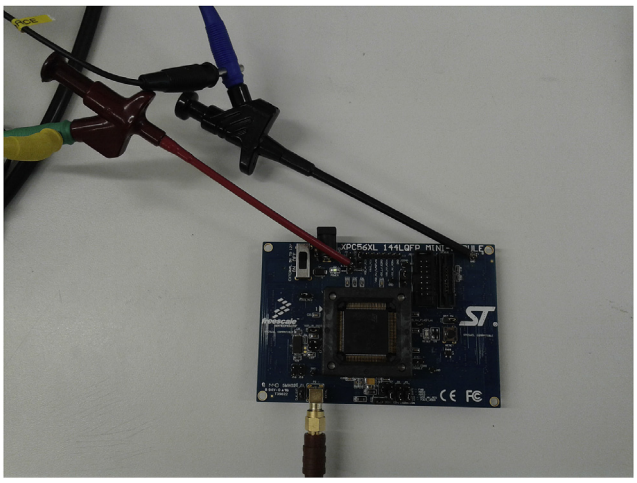

Fig. 7. Minimodule with clock provided via an SMA connector. Power is supplied and monitored with a four-wire sensing configuration for accurate measurements.

electronics not affected from the ^{60}Co source (see Fig. 8), i.e. positioned outside the radiation room. This choice doesn't require any shielding, although it may limit the complexity and amount of possible actions on the DUT during irradiation. DUT's correct behavior must be verified before irradiation, as long cables can cause problems of signal and power integrity. For intermediate operations outside the radiation room, the full evaluation board has been employed, comprising the minimodule and a motherboard that can host the minimodule as a daughterboard (Fig. 9). The rest

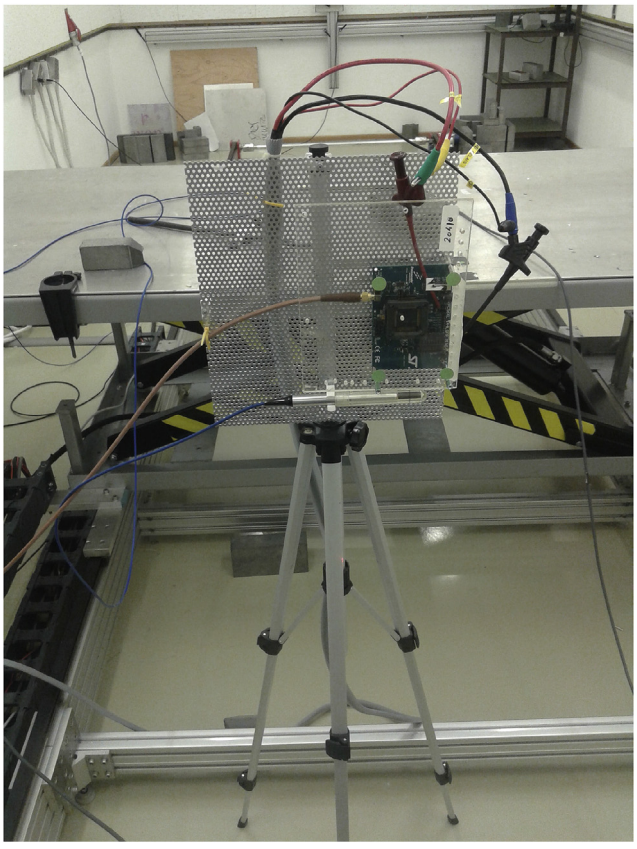

Fig. 8. Minimodule positioned in front of the source to be irradiated. The dosimeter for calibration is visible below the minimodule.

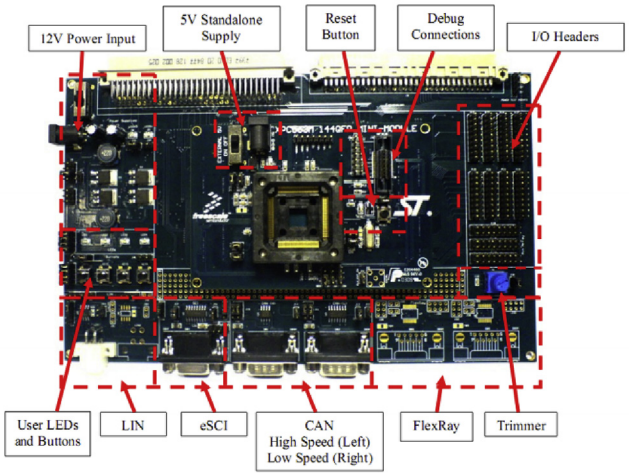

Fig. 9. Complete evaluation board with the motherboard hosting the minimodule.

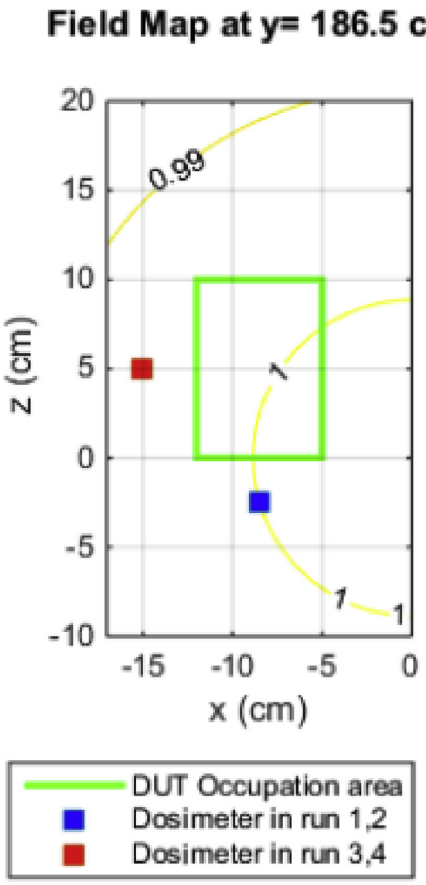

Fig. 10. Dose rate distribution on the DUT normalized to the starting position of the dosimeter. The plane of the DUT and the dosimeter is 186.5 cm away from the source.

of the test setup is reported below:

- The DUT is the SPC56EL70L5CBFSY. X-rays of the DUT in Fig. 6 shows that the die is 0.8 cm x 0.8 cm^2.
- The power was supplied by the Keysight N6705B DC power analyzer, measuring absorbed current with a four-wire sensing configuration and logging data during irradiation to monitor correct functionality of the device. The device was powered with

3.3 V, typical current absorption values before irradiation were found to be:

– unclocked: 36 mA
– while running the “test as you fly” program: between 70 and 80 mA

- The clock was supplied by a Keysight 33612A signal generator, placed outside the radiation room and set to generate a 0–1.3 V square wave with a frequency of 40 MHz and a 50% duty cycle. A SMA cable has been used to connect the clock generator to the device.
- A Fluke 190–104/S ScopeMeter was employed to monitor voltage levels and correct activity of FCCU outputs during intermediate measurements.
- A dosimeter is employed to cross-check absorbed dose (see Figs. 8 and 10).
- A laptop was employed outside the radiation room during intermediate operations to flash the DUT.

3.3. Test programs

Two test programs have been employed (the same from Ref. [15]):

- **“Test as you fly” program**: this program is composed of time slots, each intensively using a part of the DUT. The software is intended to emulate typical program flows during missions (reading and writing SRAM, reading Flash memory, sending data on UART, toggling GPIOs, etc.).
- **ADC program**: program reading a static value from an ADC channel connected to a trimmer on the motherboard.

3.4. Test procedures

Two different procedures were employed with the same test setup. “Procedure A” is described below.

1) Flash the DUT with the ADC program and read ADC value.
2) Flash the DUT with the “test as you fly” program and place the DUT for irradiation (see Fig. 8).
3) Irradiate the device to the dose required, according to the current irradiation step (see Table 1).
4) Stop the irradiation and execute intermediate operations:

   a) Monitor FCCU outputs with the scopemeter to check correct activity of the device, voltage levels and frequency.
   b) Measure current absorption without clock using the power analyzer.
   c) Measure Vcore voltage with a scopemeter (DUT unclocked).
   d) Run the test program and log from UART, looking for anomalous behavior (using additional motherboard).
   e) Reprogram the DUT with the ADC program (using additional motherboard).
   f) Measure ADC value (using additional motherboard).

5) Go to step 2 if other irradiation steps are required (see Table 1)
6) Test again the DUT after several annealing conditions with the procedure described in step 4

In the “Procedure A”, the flash memory is programmed twice for each step. To provide a qualitative relationship between the amount of flash reprogramming and the total dose causing the failure, the following “Procedure B” is defined:

1) Flash the DUTs with the “test as you fly” program and place it for irradiation.
2) Irradiate the DUTs to the dose required from the irradiation step (see Table 1).
3) Stop the irradiation and execute intermediate operations:

   a) Monitor FCCU outputs with the scopemeter to check correct activity of the device, acceptable voltage levels and frequency.
   b) Evaluate current absorption without clock using power analyzer and Vcore voltage without clock with a scopemeter.
   c) Erase and fill the flash block H0 (256 KB of non-code space) with a 0×55 pattern using JTAG and a tool from the vendor.

4) Go to step 2 if other irradiation steps are required (see Table 1).
5) Test again the DUT after several annealing conditions with the procedure described in step 3.

3.5. Test plan

For “Procedure A” one DUT was irradiated. It was biased, clocked and running the “Test-*as*-you-fly” program. For “Procedure B”, two samples were irradiated. One was irradiated exactly like the first run, while the other was unbiased and with pins shorted to ground. In both cases the irradiation schedule in Table 1 has been followed. After each irradiation step, the irradiation was suspended for 0.8 h to allow intermediate operations. After a failure, or at the end of the irradiation schedule, the device was left to anneal in the same conditions used for irradiation (i.e. running the program or unbiased).

3.6. Test results

The results of “Procedure A” are shown in Table 2. In this case, the DUT failed during the reprogramming at 30 Krad. After one day of annealing at room temperature the reprogramming was again possible. The result of the biased device for the “Procedure B” are showed in Table 3. It failed during reprogramming at 45 Krad, and recovered after one day of room-temperature annealing plus three

Table 1
Irradiation schedule.

Step [#]	Dose Rate [*rad/h*]	Duration [*hrs*]	Total Dose [Krad(Si)]
1	625	24	15
2	625	24	30
3	625	24	45
4	625	24	60

Table 2
Result for procedure A.

	0 Krad	15 Krad	30 Krad	1 day room T	3 day room T
FCCU (J16) [V]	3.35	3.25	3.05	3.43	3.43
FCCU (J18) [V]	3.29	3.14	2.96	3.33	3.32
FCCU [KHz]	7.9	7.9	7.9	7.9	7.9
Current [mA]	37.7	38.1	39	39	38.7
ADC value	0xFB0	0xFB3	–	0xFAF	0xFB2
Vcore [V]	1.27	1.26	1.26	1.26	1.26
Reprogramming	Yes	Yes	No	Yes	Yes

Table 3
Procedure B, dut running "test-as-you-fly" program.

	0 Krad	15 Krad	30 Krad	45 Krad	1 day room T	3 days high T
FCCU [KHz]	7.8	7.8	7.8	7.8	7.8	7.8
Current [mA]	38.5	39.9	41.0	41.7	41.4	40.0
Vcore [V]	1.25	1.25	1.25	1.26	1.26	1.27
H0 writing	Yes	Yes	Yes	No	No	Yes

Table 4
Procedure B: Unbiased dut.

	0 Krad	15 Krad	30 Krad	45 Krad	60 Krad	4 days room T
FCCU [KHz]	7.7	7.7	7.7	7.7	7.7	7.7
Current [mA]	36.7	36.7	36.7	36.6	36.7	36.7
Vcore [V]	1.24	1.25	1.26	1.26	1.26	1.26
H0 writing	Yes	Yes	Yes	Yes	Yes	Yes

days of high-temperature annealing. The results of the unbiased device for "Procedure B" are showed in Table 4. No failures were reported in this case and the sample survived a 4 days room-temperature annealing process. The "high temperature" refers to 70° C, while room temperature has been measured to be between 22.5° C and 23° C.

No samples reported permanent failures. No parameter in any samples exceeded the range of pre-irradiation value ± 10%. Comparing the biased and unbiased case in "Procedure B", some trends are clear. From Fig. 11 it is clear that in the biased case the absorbed current rises, while it is stable in the unbiased case. The criticality of testing the DUT biased is confirmed by the lack of any failures during reprogramming in the unbiased case. Some parameters, like the FCCU signaling frequency derived from an internal RC oscillator (16 MHz), had no noticeable shift in both cases. Some samples failed during flash erasing in re-configuration. This operation is very critical because of the high voltages involved. Comparing the result of "Procedure A" and "Procedure B", it can be noted that the less the flash is erased and written, the later the failure happen in terms of absorbed dose. The time needed to erase the flash increases with the increasing of absorbed dose, until a failure due to timeout happens (further investigation is needed in future works). The comparison between writing in non code space and complete reprogramming shows that reprogramming is needed only if the code space is corrupted from a non successful reprogramming. In all cases re-programming was successful after annealing, suggesting that the cause of failure is a temporary shift

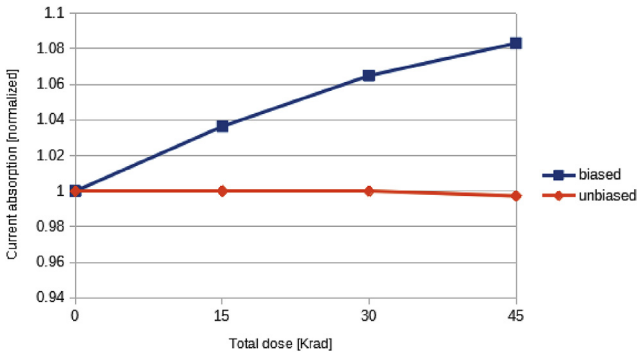

Fig. 11. Current absorption normalized to initial values vs. total dose in case of biased and unbiased samples.

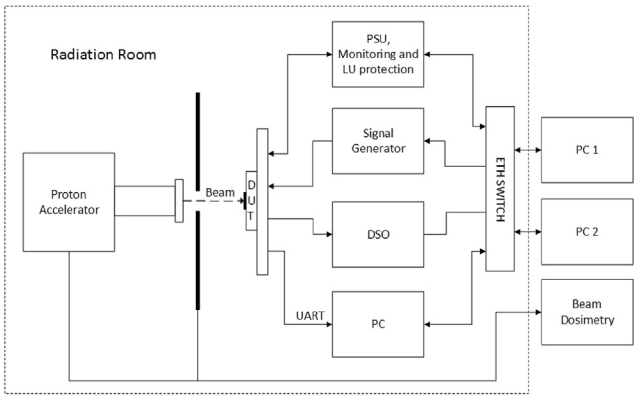

Fig. 12. Block diagram of the test setup for simultaneous test of TID and SEE with protons [22].

and excluding any destructive event.

4. Proton test

4.1. Proton test setup

The experiment here described took place simultaneously to the one described in Ref. [15] at the Proton Irradiation Facility (PIF), located in the Paul Scherrer Institute (PSI) [21]. The primary beam was made of 72.8 MeV protons. Some copper degraders (shown in Fig. 13) were employed to lower their energy. Irradiation was performed in air with plastic packaged chips. Therefore, a GEANT4 simulation has been performed to take into account the resulting energy degradation and dispersion (see Table 5 and Fig. 14). The dose rates, fluence and time required to reach a total dose of 30 Krad(Si), given a flux of 1.00E+07 $(p/cm^2/s)$ for various proton energies is provided in Table 6.

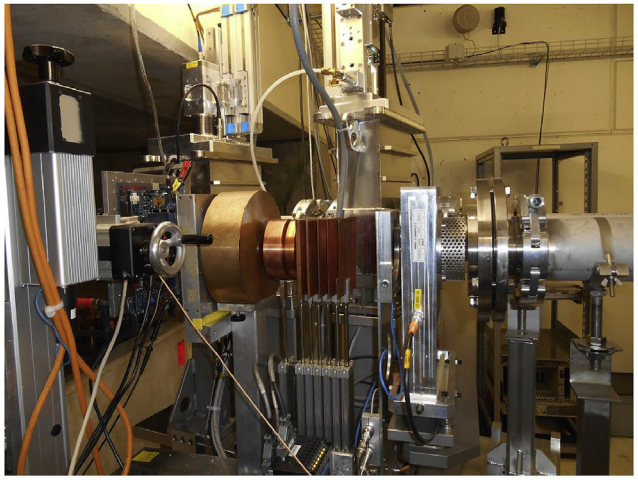

Fig. 13. Board placed at the PIF (PSI).

Table 5
Proton beam energy spread.

Position	Average Energy	Standard deviation
Before degraders	72.8 MeV	~0 MeV
After degraders	17.2 MeV	1.6 MeV
Die surface	16.2 MeV	1.7 MeV

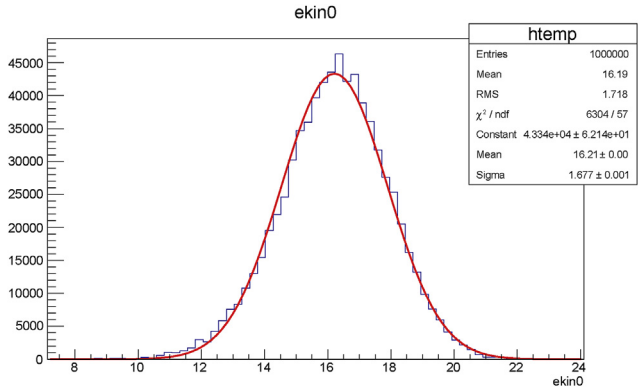

Fig. 14. Proton energy distribution at die surface after degradation.

Table 6
Protons: Dose rates, fluence and time to reach a total dose of 30 krad(si), given a flux of 1.00e+07 $(p/cm^2/s)$ for various energies.

Energy (MeV)	Range(Si) (μm)	LET ($MeV/mg*cm^2$)	Fluence (p/cm^2)	Dose Rate (Krad/h)	Time (hr)
4	148	6.90E-02	2.72E+10	39.7	0.75
5	215	5.86E-02	3.20E+10	33.8	0.89
6	294	5.10E-02	3.68E+10	29.4	1.02
10	709	3.48E-02	5.39E+10	14.6	1.50
15	1440	2.54E-02	7.38E+10	13.2	2.05
20	2390	2.03E-02	9.24E+10	11.7	2.57

The experimental test setup for protons TID test is reported in Fig. 12. It was used to simultaneously perform a TID and a SEE test. The detailed handling of a simultaneous TID and SEE test has been described in Ref. [22] and the SEE results have been shown in Ref. [15]. The test setup is described below:

- A Keysight N6705B DC Power Analyzer powered the board, monitoring the current absorbed from the whole motherboard with a threshold for latch-up protection.
- The clock signal was generated from a Keysight 33612A Waveform Generator, as in subsection 3.2.
- A LeCroy WaveRunner MXi oscilloscope was employed to monitor voltages and frequencies from the two pins of the FCCU (J16 and J18 in Table 2). A current probe was connected to the oscilloscope, monitoring the current absorbed from the chip.
- A laptop in the radiation room logged all the anomalies signaled from the DUT via UART.
- All the equipment in the radiation room was connected to the Ethernet network and remotely operated from the control room.

The beam dosimetry was also provided, measured separately using proper detector cross-checked with beam currents measured from accelerator machine operators.

4.2. Test procedure and programs

The same programs described in subsection 3.3 were employed for this test. The DUTs were verified to be functional and with all the monitored parameters in the datasheet range. They were flashed with the "test as you fly" program in the control room and placed on the motherboard in front of the proton collimator to be irradiated (see Fig. 13). The Total Dose was given in one single step for each sample, except for sample 5. At the end of the irradiation of a DUT, the minimodule with the DUT was replaced with another one hosting the next DUT, and the old DUT brought to the control room for functional tests and other measurements. The DUT was there reprogrammed with the ADC program and the ADC shift was evaluated. At the end of the irradiation, the sample were left at the facility (because after proton irradiation they are typically activated) and received for successive measurements after two weeks of annealing.

Table 7
Irradiation schedule. The last column shows the outcome of the reprogramming phase.

Sample [#]	Energy [MeV]	Dose Rate [Krad/h]	Time [hrs]	Total Dose [Krad(Si)]	Reprogr. [Yes/No]
1	17.2	27.5	1	27.5	Yes
2	17.2	27.5	1	27.5	Yes
3	17.2	27.5	1	27.5	Yes
4	17.2	27.5	1.25	34.4	Yes
5 (step 1)	17.2	27.5	1	27.5	Yes
5 (step 2)	17.2	55	0.5	55	No
6	17.2	55	1	55	No
7	17.2	55	0.63	34.8	Yes
8	17.2	55	0.83	45.4	Yes
9	72.8	15.9	0.75	11.9	Yes

4.3. Test plan and results

The radiation scheduling and the result of the reprogramming are shown in Table 7.

No monitored parameters exceeded the ±10% range. The maximum ADC shift found was ±1 LSB. The reprogramming was performed without failures up to 45.4 Krad (sample 8 in Table 7), and both the attempts at 55 Krad with different dose rates and number of steps failed (samples 5 and 6 in Table 7). All samples were completely functional after the annealing.

5. Conclusion

Testing a complex SoC, like a state-of-the-art microcontroller, while exercising the functionalities of a typical mission is a challenging task, both for test setups and procedures. Nevertheless, in both for ^{60}Co and protons the mission of interest has been successfully emulated during irradiation, while the complexity of the test setup was kept under control. The proton test made it easier to have a simplified test setup (beam more confined), while the ^{60}Co allowed simultaneous testing of more DUTs at once and an easier handling of the annealing (proton beams activate the DUT). A quantitative comparison of ^{60}Co and proton tests is outside the scope of this work, but the same failure mode was observed (failure during the erase of the embedded flash memory). The total dose causing the failure is different for ^{60}Co and protons, although in both cases the monitored parameters didn't exceed the ±10% range. The use of two procedures in the case of ^{60}Co with different number of reprogramming iterations and different size of the reprogrammed portion of the embedded flash shows that the number of times the flash is reprogrammed lowers the total dose causing the failure. Testing the DUT both biased and unbiased confirmed that damages may differ in the two conditions and in this case testing the SoC unbiased underestimates TID effects on the DUT functioning biased and clocked as in the actual mission.

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