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A 2D Ultrasound Phased-Array Transmitter ASIC for High-Frequency US Stimulation and Powering

Hassan Rivandi , *Student Member, IEEE*, and Tiago L. Costa , *Senior Member, IEEE*

Abstract—Ultrasound (US) neuromodulation and ultrasonic power transfer to implanted devices demand novel ultrasound transmitters capable of steering focused ultrasound waves in 3D with high spatial resolution and US pressure, while having a miniaturized form factor. Meeting these requirements needs a 2D array of ultrasound transducers directly integrated with a high-frequency 2D phased-array ASIC. However, this imposes severe challenges on the design of the ASIC. In order to avoid the generation of grating lobes, the elements in the 2D phased-array should have a pitch of half of the ultrasound wavelength, which, as frequency increases, highly reduces the area available for the design of high-voltage beamforming channels. This article addresses these challenges by presenting the system-level optimization and implementation of a high-frequency 2D phased-array ASIC. The system-level study focuses on the optimization of the US transmitter toward high-frequency operation while minimizing power consumption. This study resulted in the implementation of two ASICs in TSMC 180 nm BCD technology: firstly, an individual beamforming channel was designed to demonstrate the tradeoffs between frequency, driving voltage, and beamforming capabilities. Finally, a 12-MHz pitch matched 12×12 phased-array ASIC working at 20-V amplitude and 3-bit phasing was designed and experimentally validated, to demonstrate high-frequency phased-array operation. The measurement results verify the phasing functionality of the ASIC with a maximum DNL of 0.35 LSB. The CMOS chip consumes 130 mW and 26.6 mW average power during the continuous pulsing and delivering 200-pulse bursts with a PRF of 1 kHz, respectively.

Index Terms—2D ultrasound phased-array, high-frequency focused ultrasound, high-voltage beamforming channel, ultrasonically powered implanted devices, ultrasound neuromodulation.

I. INTRODUCTION

IN RECENT years, new ultrasound (US) biomedical applications, such as ultrasound neuromodulation [1], [2], [3], [4], [5], ultrasonic power transfer and communication for medical implants [6], [7], [8], [9], [10], [11], [12] have been emerging, as visualized in Fig. 1. These growing applications require different sonication parameters compared to traditional US imaging systems [13], [14], such as long bursts of US waves with peak acoustic intensities above 1 W/cm^2 and pulse duration in the millisecond range [15]. Moreover, while in ultrasound imaging

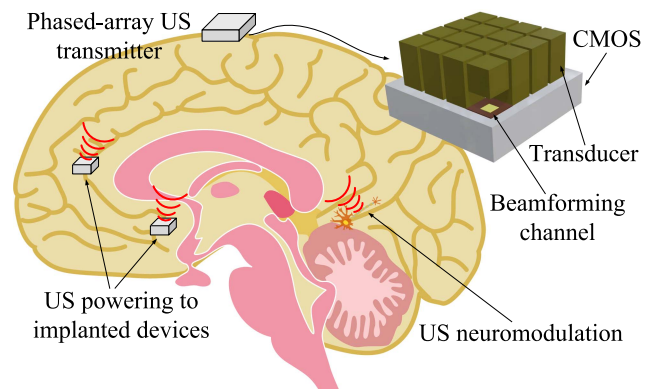


Fig. 1. A conceptual 2D ultrasound phased-array transmitter, performing both US neuromodulation and power delivery to implanted devices with a single transmitter.

applications, the focused ultrasound beam is typically optimized in terms of lateral spatial resolution for high-precision scan lines, in the abovementioned applications, the target is to ideally match the volumetric spatial resolution of the focal spot with the small size of ultrasonically powered implants, which can be as small as 0.065 mm^3 [10], [11], and cover the micrometer-sized neurons with remarkable precision. This is of particular importance in pre-clinical research to match the scales of the transducers, and focal spot dimensions to the rodent nervous system [1], [2], [4], and in emerging human applications such as sub-cranial visual cortex stimulation for the blind [16], [17] and peripheral nerve stimulation [18]. Furthermore, a wearable form factor is a vital characteristic of future US transmitters for both US stimulation and US power delivery applications.

Conventional US transmitters used in ultrasound neuromodulation and ultrasound powering utilize bulky, fixed-focus, single-element transducers that need complex mechanical translation to change the location of the focal spot [19], [20]. Furthermore, they are not applicable to wearable applications due to their large form factor and the need for bench-top electronic signal generators and power amplifiers. In order to overcome these limitations, researchers have been pursuing miniaturized and high-performing ultrasound transducers and interfacing electronics. In particular, the maximum level of integration and performance can be achieved by direct integration of 2D arrays of ultrasound transducers on top of pitch-matched high-voltage beamforming ASICs. In [21], a 2D beamformer chip integrated with a 2D array of capacitive-micromachined-ultrasonic transducers (CMUTs) for wearable US neuromodulation was proposed.

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The choice of CMUT transducers demanded the design of a 60-V power amplifier per channel in order to achieve the necessary acoustic intensity for neuromodulation. The use of 60-V DMOS transistors drastically increases the area per channel, which limited the ultrasound frequency to 3.4 MHz. In addition, the large minimum sizes of 60-V DMOS transistors and their resultant parasitic capacitance, when compared with the CMUT impedance, resulted in an over-dimensioned power amplifier, hence increased power consumption. Finally, each channel included a digital beamforming circuit based on a custom finite-state machine (FSM) and counter approach. In order to achieve the necessary timing resolution for precise acoustic focusing, the proposed digital beamformer required a clocking frequency 16 times larger than the ultrasound frequency. This prevents the scalability of the ultrasound frequency towards high spatial resolution and further contributes to the increased power dissipation, which dominated over the 60-V driver for low duty cycle conditions. Overall, the high power consumption and the corresponding thermal dissipation drastically limit the pulse duration specifications for US stimulation. Another 2D phased-array ASIC integrated with Lead Zirconate Titanate (PZT) piezoelectric transducers has been presented in [22]. This work proposed a split beamformer system, with a shared coarse beamformer implemented with a delay locked loop (DLL) and a fine-beamformer per channel implemented with a phase-interpolator, which allows for a higher frequency of operation without the large penalty of dynamic power consumption as in the previous work. However, as demonstrated in Section II of this work, the 6-bit beamformer is over-designed, which leads to an unnecessarily larger circuit area and power dissipation. Finally, the driver circuit utilizes 5-V transistors, which, despite the higher electroacoustic transmit efficiency of PZT in comparison with CMUTs, only lead to a focal pressure of 100 kPa, which is normally insufficient for ultrasound neuromodulation.

Despite recent efforts, the literature still lacks an ASIC matched with the abovementioned requirements of non-imaging US applications, where high spatial resolution, power efficiency, and high driving voltage are simultaneously achieved. The main challenge towards achieving high-frequency 2D US phased-array operation with high-voltage capabilities relates to the tradeoff between the reduced area of the pitch-matched ASIC beamforming channels and the large area required by high-voltage (HV) transistors. In order to optimize the phased-array US transmitters in terms of spatial resolution along with power efficiency and US intensity, a comprehensive system-level study on US phased-array transmitters is needed. [23] has presented a design methodology for finding the optimal transducer array geometry; however, it was limited to 1D US phased-arrays. In [22], a system-level analysis for 2D arrays was given, where the influence of array size and beamforming timing resolution on the properties of focused ultrasound waves is shown. However, this analysis was limited to 10-MHz ultrasound waves, and no insights about power consumption were given. In this work, we extend the work previously published in [24] by presenting a detailed system-level study to investigate the influence of 2D US phased-array transmitter parameters on the volumetric resolution and US intensity of the focus spot, to guide the design of 2D

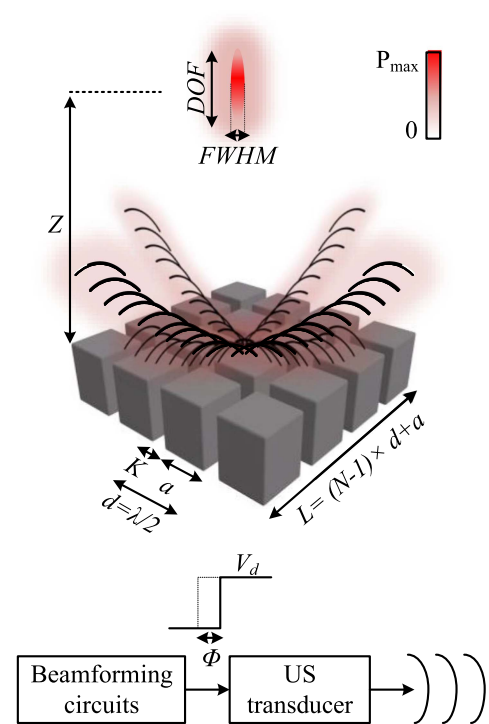


Fig. 2. Principal properties of a 2D phased-array ultrasound transmitter.

phased-arrays with minimum pixel area and power consumption towards the high-frequency operation. Following the results of this study, we augment the previously reported high-frequency individual beamforming channel ASICs [24] with the optimized design and electrical characterization of a 20-V 12-MHz 2D phased-array US transmitter ASIC.

This article is organized as follows: Section II presents the system-level design for a high-frequency 2D US phased-array transmitter. Sections III and IV describe the circuit design implementation and the experimental validation of the ASICs, respectively. Section V provides a discussion of the obtained results, and Section VI concludes the article.

II. SYSTEM DESIGN

In a 2D phased-array US transmitter, as shown in Fig. 2, an $N \times N$ 2D array of electronic beamforming circuits drives the pitch-matched US transducers with a squared signal with a given center frequency (f_{US}), phase (Φ) and driving voltage (V_d). The US transducers are directly integrated with a 2D array of $N \times N$ elements with the inter-element pitch size of d . Assuming that the transducers are fabricated using a dicing saw process [22], the kerf size created by the dicing saw blade is defined as k . By programming the beamforming circuits with specific phases according to the speed of sound in the medium and the relative position of each transducer within the array [25], a focused ultrasound wave is created at a given focal spot depth (Z), with a focus gain (G) and a volumetric spatial resolution (Vol_{res}). The performance of 2D phased-array US transmitters is maximized when the focused ultrasound waves with the desired properties are achieved at the expense of the lowest possible circuit area

and power consumption. In the case of the applications targeted in this work, Vol_{res} should be minimized, and G maximized. Hence, understanding the influence of the beamforming circuits, transducer array, and the resulting ultrasound waves is critical to guide the 2D phased-array system design toward the highest performance.

Firstly, the influence of f_{US} on the focal spot properties is investigated. The Vol_{res} is given by (1), where DOF (2) is the depth of field, representing the spatial resolution in the axial direction, and the $FWHM$ (3) is the full width at half maximum, representing the spatial resolution in the lateral direction. On the other hand, the maximum focal depth Z_{max} is obtained from (4) and G from (5), where L_{eff} is the effective aperture and is obtained from (6). Increasing f_{US} results in a lower wavelength λ , and, as a consequence, it reduces Vol_{res} while increasing G and Z_{max} .

$$Vol_{res} = 1/6 \cdot \pi \cdot DOF \cdot FWHM^2 \quad (1)$$

$$DOF \propto \lambda \cdot \left(\frac{Z}{L}\right)^2 \quad (2)$$

$$FWHM \propto \lambda \cdot \frac{Z}{L} \quad (3)$$

$$Z_{max} \approx \frac{L^2}{\pi \lambda} \quad (4)$$

$$G \propto \frac{\lambda}{Z \cdot L_{eff}} \quad (5)$$

$$L_{eff} = L - k(N - 1) \quad (6)$$

In the context of pre-clinical experiments with rodents or in the case of cortical interfaces in large animals and humans, the penetration depth of ultrasound is in the order of 5–10 mm. Hence, the acoustic absorption, which increases exponentially with frequency at a rate of 0.75 dB/cm/MHz, is not highly penalized frequency up-scaling. However, the fabrication of the piezoelectric ultrasound transducers is normally done using a dicing saw process with a given blade thickness, which results in a kerf size k of the same size, typically in the range of tens of μm . Since k cannot be made arbitrarily small, increasing the frequency reduces the effective aperture L_{eff} , which in turn leads to lower G (5). To investigate all the abovementioned tradeoffs, simulations were performed using the Matlab toolbox k-Wave [26]. To reduce the simulation time, the total size of the 2D array was set to $2 \times 2 \text{ mm}^2$. In the case of pre-clinical experiments with rodents, L is limited to $< 10 \text{ mm}$ due to the maximum size of the craniotomy for direct interface between the chip and the brain; thus, the chosen value is also in line with experimental requirements. The US transducers were configured to form a focal spot at a depth of 2 mm, and the kerf size k was swept during the simulation to study its effect on the beam profile properties. As illustrated in Fig. 3, increasing the frequency leads to a higher phased-array gain for frequencies up to 16 MHz for kerf sizes of $20 \mu\text{m}$ or lower. For kerf sizes of $40 \mu\text{m}$ or larger, G starts to drop for frequencies above 8 MHz. Thus, for high frequencies, it is recommended to minimize k as much as the microfabrication processes allow [27], ideally to values much

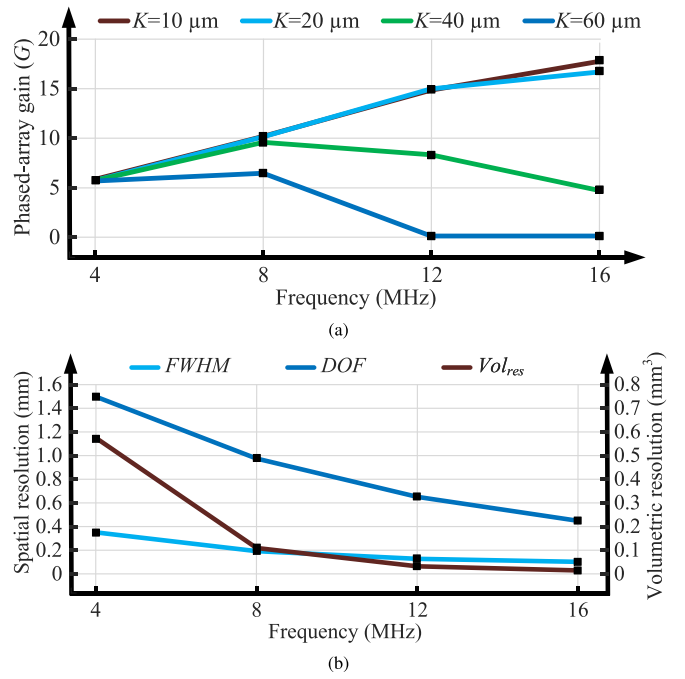


Fig. 3. The influence of center frequency on phased-array gain and spatial resolution. During the k-Wave simulation, the total length of the array and the pitch size were fixed to 2 mm, and the sound half-wavelength. In (b), k is set to $20 \mu\text{m}$.

lower than d . Furthermore, Vol_{res} decreases with increasing the frequency; however, that increase was less significant for frequencies above 12 MHz. Increasing the frequency further would then limit the available area for the beamforming circuitry without significantly improving performance.

Besides the f_{US} , the array length L has a direct influence on acoustic parameters. Fig. 4 depicts the effect of expanding the number of elements, N , or the array length on the phased-array gain and the lateral resolution. From Fig. 4(a), it is evident that increasing the array length in a given center frequency leads to a higher intensity at the focal spot. Moreover, the phased-array gain increases at a higher rate for higher frequencies. Additionally, Fig. 4(a) demonstrates that the phase array gain does not significantly improve with increasing the array length after a given threshold, which at 12 MHz corresponds to an array length of 5 mm. A similar conclusion can be taken with the relationship between the array length and the volumetric resolution of the focal spot, as shown in Fig. 4(b). Moreover, the maximum achievable penetration depth (Z) in phased-array increases with both array length and frequency, as shown in Fig. 4(c), despite the higher acoustic attenuation at higher frequencies.

Regarding the tradeoffs related to the ASIC implementation, phasing the driving signal of the US transducers allows changing the focal spot location electronically. In this regard, the beamforming channels drive the US transducers with a given phase, as illustrated in Fig. 5(a) for transducers along a row or column. Since non-imaging applications require continuous pulse transmission, wrapped phase instead of absolute phase can be used, which allows for simpler circuitry and avoids the need for high-frequency counters [21]. However, finding the optimum

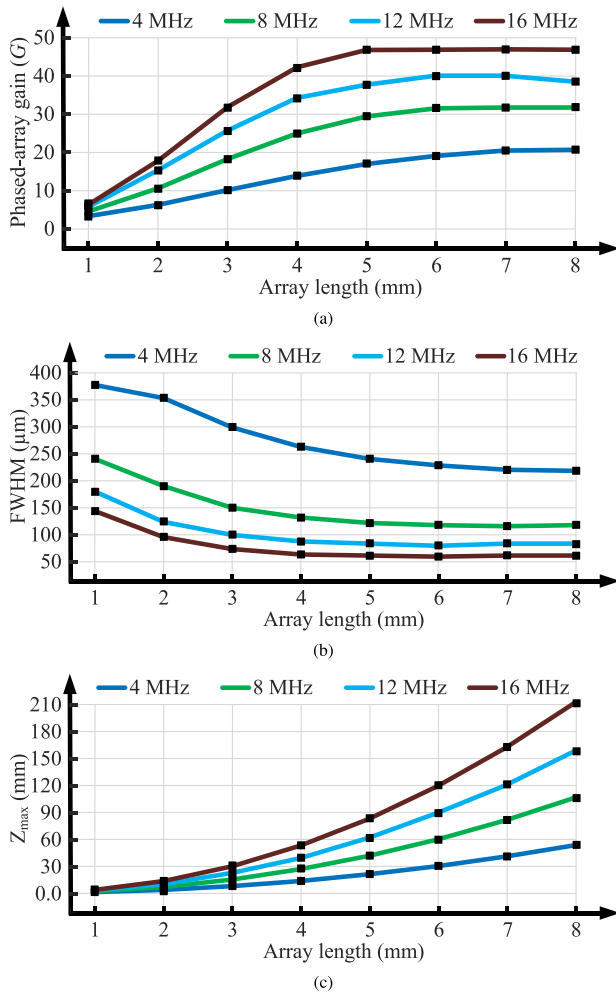


Fig. 4. The effect of array length on (a) phased-array gain, (b) lateral resolution, and (c) maximum depth of focal spot for a 2D US phased-array transmitter. The pitch size matches the sound half-wavelength, and the focal depth in (a) and (b) is equal to 2 mm. A kerf size of $20 \mu\text{m}$ was considered for all the abovementioned simulations.

phase quantization resolution requires studying its influence on the beam profile. From Fig. 5(b), it is evident that the normalized focal pressure and spatial resolution do not significantly improve for phase quantization resolution above three bits. Fig. 5(c) demonstrates the effect of the phase quantization on the steering capability. The simulation results show that reducing the phase quantization resolution from ten to three bits does not affect the steering capabilities in both axial and lateral directions. In this regard, it can be inferred that 3-bit phase quantization is enough for implementing a phased-array US transducer, independent from the center frequency, which reduces the circuit complexity in comparison with other works [21], [22], thus allowing for lower area beamforming circuits and higher operating frequency of the phased-array. The phase array gain and the volumetric resolution also depend on the location of the focal spot, and they vary for different steering angles or Z . Fig. 6 shows the influence of the focal depth on the phased-array gain and volumetric resolution. The ultrasound beam characteristics degrade with

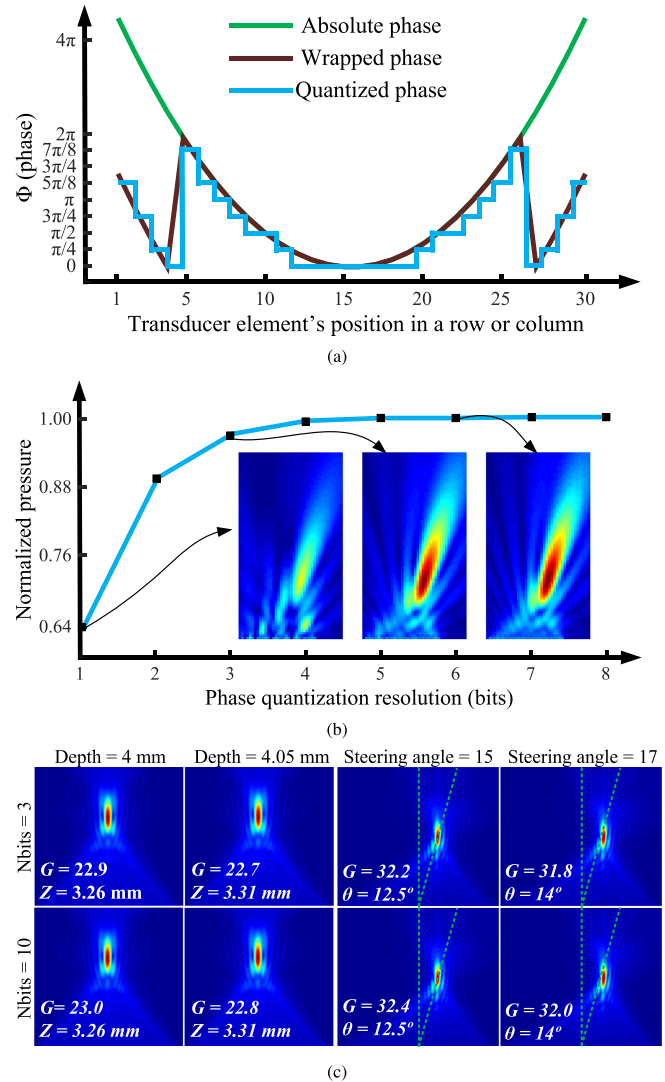


Fig. 5. (a) Phase of US transducers for a given row or column in a 2D US phased-array. (b) and (c) show the effect of phase quantization on the focal spot properties and steering capability of a 2D phased-array; a 40×40 phased-array with the center frequency of 12 MHz and kerf size of $20 \mu\text{m}$ was considered for the k-Wave simulations.

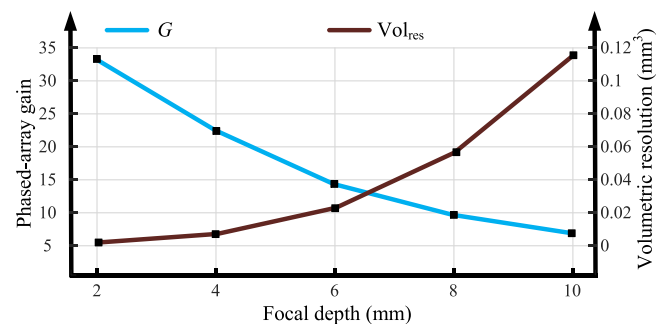


Fig. 6. The influence of the focal depth on volumetric resolution and phased-array gain of a 2D phased array; a 66×66 US phased-array with center-frequency of 12 MHz and kerf size of $20 \mu\text{m}$ was considered for the k-Wave simulations.

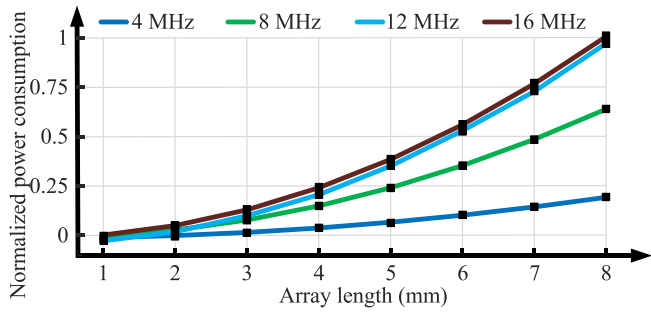


Fig. 7. Simulated power consumption of a 2D US phased-array transmitter for different frequencies and array lengths.

increasing the focal depth; the same applies to changing the steering angle. Therefore, it is crucial to consider these variations in designing the 2D phased-array US transducer.

Finally, power consumption plays an essential role in designing US phased-array transducers. Although increasing the frequency and the array length improves the US beam parameters, it increases the power consumption, as depicted in Fig. 7. This graph is based on the 20-V beamforming circuit from [24] and the modeling of the piezoelectric transducer's impedance. The lumped-element model of the piezoelectric transducer is obtained by electrical impedance estimation close to the resonance frequency. To perform this, the Butterworth-van Dyke lumped-element model is approximated by a capacitor in parallel with a resistor in the resonance frequency. According to the Fig. 7, the power consumption increases with the number of elements and the resonant frequency. In addition, the total power consumption of 12-MHz and 16-MHz 2D phased-arrays are approximately the same. This can be attributed to the fact that increasing the center frequency from 12 MHz to 16 MHz increases the dynamic power consumption of the electronic circuits. On the other hand, the size of the US transducers is comparable with the kerf size in such high frequencies, which results in a smaller load impedance and, therefore, lower power consumption. In the end, it is worth mentioning that increasing the driving voltage leads to higher acoustic intensity at the focal spot. At the same time, it increases power consumption with a square relationship.

According to the conclusions drawn in this Section, the system-level design parameters are chosen as follows. Even though increasing the number of elements improves the volumetric resolution and the phased-array gain, it comes at the cost of extra complexity and a larger form factor. Thus, this work aims to maximize the ultrasound frequency, which results in a smaller available pixel area for circuit implementation. In this regard, this work has implemented a pixel-level pitch-matched beamforming channel and a 2D phased-array to investigate the required electronic circuits for high-frequency phased-array transmitters. Considering the minimum achievable kerf size of 10 μm , according to a commercially available 10- μm dicing blade (HCZZ5012, Disco corporation), the center frequency of the beamforming channel was set to 12 MHz, corresponding to the channel area of $60 \times 60 \mu\text{m}^2$, and can generate continuous pulses with an amplitude of 36 V. The 2D phased-array

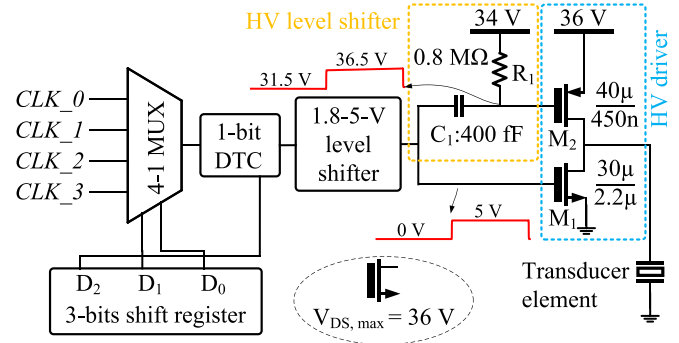


Fig. 8. The schematic of 36-V beamforming channel.

transmitter consists of 12×12 beamforming channels that deliver 12-MHz pulses with 20-V amplitude. To this end, a 3-bit phase quantization scheme is utilized to avoid over-designing of electronic circuits, similar to some prior works [21], [22]. Even though the array length is only 0.72 mm and is not the target of this work, the system-level study presented in this Section can be used to guide the design of larger high-frequency 2D phased-arrays toward higher penetration depths.

III. ELECTRONIC CIRCUIT DESIGN

A. High-Voltage Beamforming Channel

Beamforming channels need to deliver high-voltage pulses with given phases to the US transducer elements to realize a US phased-array transmitter. To carry out such circuits, this article has utilized Bipolar-CMOS-DMOS (BCD) technology to implement an HV pixel-level pitch-match beamforming channel. Due to the large area occupied by HV transistors, the design of the HV beamforming channels is a tradeoff between the driving voltage, the frequency of operation, and the on-pixel beamforming circuitry. The 36-V beamforming channel, as illustrated in Fig. 8, comprises a 3-bit shift register, a 4-1 multiplexer, a 1.8-5-V level shifter, an HV level shifter, and an HV driver [24]. The data corresponding to the phase of the beamforming channel is stored in the shift register. According to the phase, the multiplexer selects one of the input clocks, that are generated off-chip to implement a 2-bit beamformer. Then, the 1-bit digital-to-time converter (DTC) performs the third-bit beamforming. The low-voltage level shifter boosts the clock level to 5 V, which drives the HV NMOS transistor. However, turning on and off the HV PMOS transistor requires an HV level shifter to change the voltage level to 36 V. In the end, an HV class D amplifier drives the US transducer with 36-V phased clocks. The sizing of the HV transistors has a crucial impact on its ability to drive the PZT load. On the other hand, over-designing the HV transistor affects both power efficiency and the available area for LV circuits implementation. Therefore, the best compromise was found with the sizes of HV NMOS and HV PMOS of $30 \mu\text{m}/2.2 \mu\text{m}$ and $40 \mu\text{m}/450 \text{ nm}$.

Regarding the HV level shifter, its area should be minimized in order not to penalize the achievable ultrasound frequency. Several architectures have been reported in the literature to

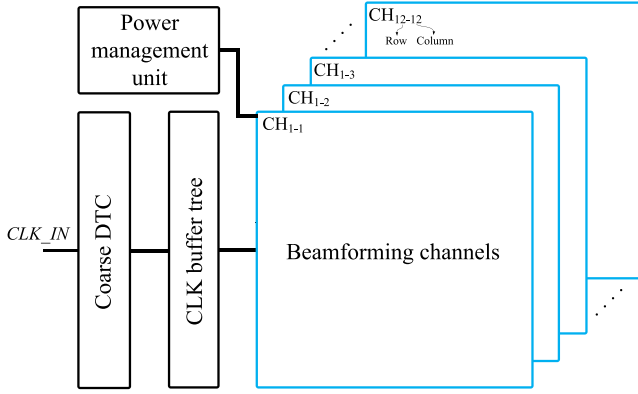


Fig. 9. System architecture of the electronics circuit of the 2D phased-array US transmitter.

implement an HV level shifter. Some works have utilized either bulky HV transistors [28], [29] or low voltage (LV) transistors in the deep-NW layer [30] at the cost of the significant separation distance between the transistors. Alternatively, for continuous pulses, a high-pass RC filter parallel with a diode shapes a high-voltage level shifter [21]. This work has adopted this architecture without the diode towards area minimization. Since the protection diode is removed in this work, connecting the resistor to the 36-V supply results in a 33.5-38.5-V signal at the gate of the HV PMOS that may damage the transistor. In this regard, the top connection of R_1 is connected to 34 V, generating a 31.5-36.5-V pulse at the gate of the HV PMOS transistor. The 36-V and 34-V supply levels require a constant rise time and fall time in such a way that the gate-source voltage of the HV PMOS transistor never exceeds 5 V. For further scaling of the circuit, C_1 and R_1 are implemented utilizing a metal-oxide-metal (MOM) capacitor on top of the active circuit and the poly resistor, respectively. To push the corner frequency of the high-pass filter close to DC frequency, C_1 and R_1 are chosen large enough (i.e., 400 fF and 800 K Ω).

B. 2D Phased-Array Transmitter

The 2D phased-array transmitter ASIC, as depicted in Fig. 9, involves a coarse DTC, a clock buffer tree, and a 12×12 array of beamforming channels. The coarse DTC transforms an external clock into delayed clocks with specific timing resolution. Then a clock buffer tree distributes these clocks among beamforming channels that deliver 20 V to US transducers. Considering the small available circuit area in high-frequency phased-arrays, the beamforming channels share the coarse DTC to generate specific phases for every transducer element. However, a 3-bit coarse DTC suffers from complicated routing challenges in the layout, in particular when scaling up the array size. In this regard, the coarse DTC is configured to generate four phased clocks corresponding to two least significant bits (LSBs), as shown in Fig. 10, while the most significant bit (MSB) is implemented in the beamforming channels as in Fig. 8. The coarse DTC, illustrated in Fig. 11(a), converts a 48-MHz clock to four 12-MHz clocks with a phasing resolution of $\pi/4$. As depicted in Fig. 11(b), the first flip-flop divides the input clock's frequency by a factor

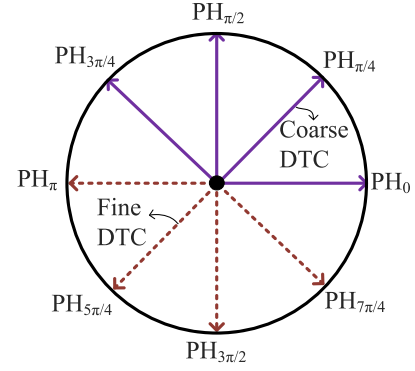


Fig. 10. Phasing diagram of the beamforming circuits.

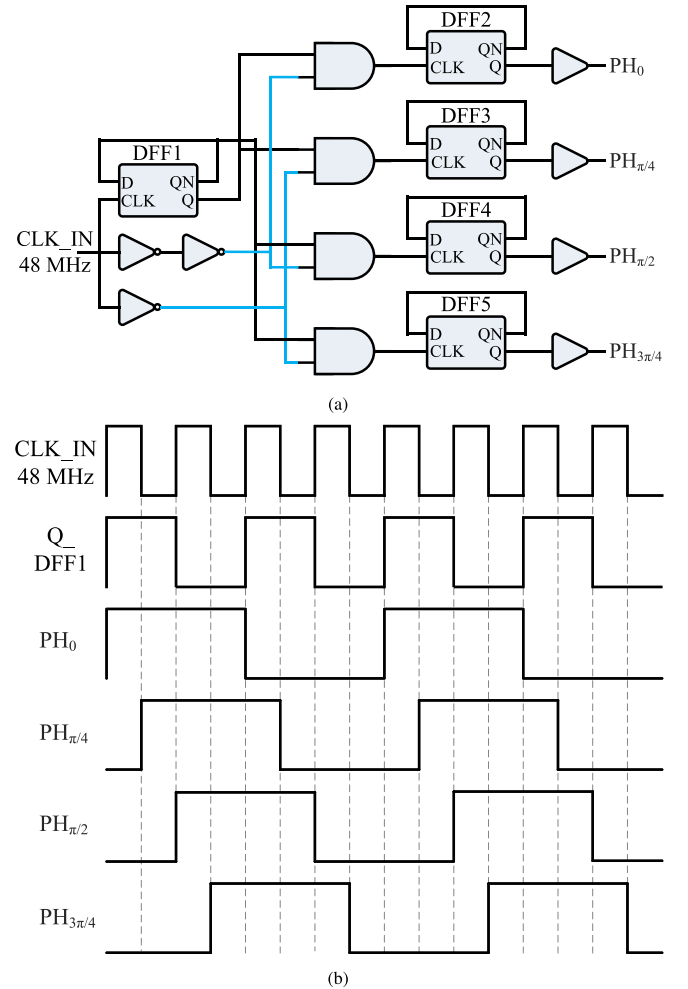


Fig. 11. (a) The circuit diagram and (b) the timing diagram of the coarse DTC.

of two. Then, the phased clocks are generated by logically comparing the input clock and the inverted input clock with the outputs of the flip-flop. Since the coarse DTC is implemented using digital circuits, the delayed clocks are less sensitive to process, voltage, and temperature (PVT) variations.

The beamforming channels in the 2D array are based on the 36-V beamforming channel, Fig. 8. To meet the electrostatic

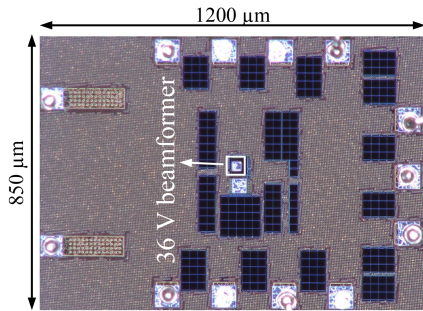


Fig. 12. The chip micrograph of the 36-V beamforming channel.

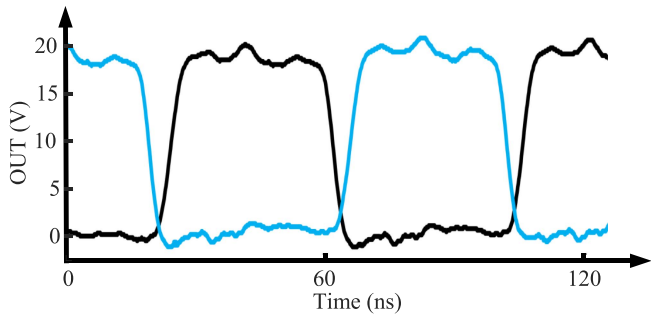


Fig. 13. The measured output waveforms of the 36-V beamforming channel programmed for phase configuration of “000” and “100”.

discharge (ESD) requirements in the 2D array, the 36-V transistors are replaced with 20-V transistors to respect the needed distance between the HV beamforming channels. Moreover, a non-overlap clock generator is used to reduce the dynamic losses of the HV driver. To carry out such a measure, this block adds a dead time between the rising and falling edges of the signals driving the HV transistors. In the end, the HV driver delivers 12-MHz 20-V phased pulses to the US transducers.

IV. MEASUREMENTS RESULTS

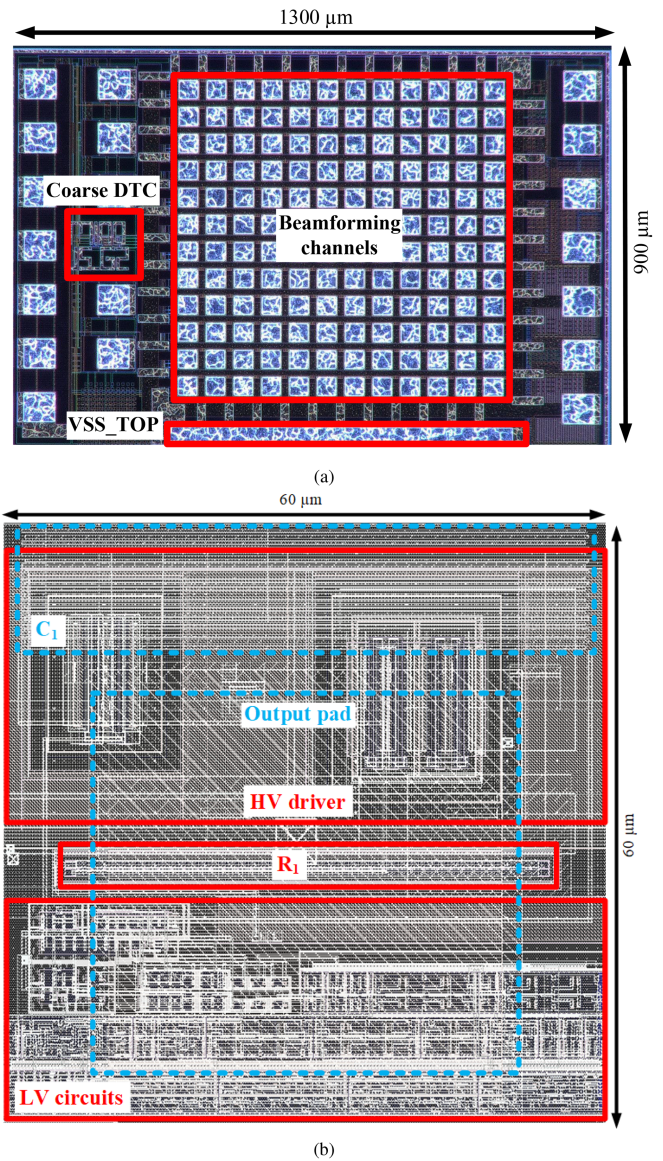
A. High-Voltage Beamforming Channels

The ASICs have been designed and fabricated in TSMC 0.18- μm BCD technology. The chip micrograph of the beamforming channel is shown in Fig. 12. The 36-V beamforming channels occupy an active area of $60 \times 60 \mu\text{m}^2$ [24].

To evaluate the functionality of the 36-V beamforming channel, four external 12-MHz delayed clocks were applied to the beamformer. Fig. 13 shows the output waveforms of the beamforming channel while performing two different phase configurations of “000” and “100”. The measurements were done by direct probing using an active picoprobe (12 C, GGB industries), which has an input impedance of $0.1 \text{ pF} // 1 \text{ M}\Omega$. It is worth mentioning that the maximum voltage limit of the 12 C picoprobe limited the applied HV power supply to 20 V.

B. 2D Phased-Array Transmitter

The chip micrograph of the 2D phased-array transmitter is shown in Fig. 14(a), occupying an active area of $900 \times 1300 \mu\text{m}^2$, including I/O pads. Fig. 14(b) shows the

Fig. 14. (a) The micrograph of the CMOS chip with 12×12 transmit channels. (b) The layout of a single transmit channel.

layout of the pitch-matched beamforming channel that occupies a silicon area of $60 \times 60 \mu\text{m}^2$. The area breakdown reveals that HV transistors occupy 57% of the channel area, while LV circuits and HV level shifter are accountable for 36% and 7% of the pixel area.

Delivering the required supply levels to the phased array transmitter involves several key steps. First of all, system-level power budgeting has been done to determine the overall current dissipation from every power supply level. Moreover, a large pad, VSS _ TOP in Fig. 14(a), is considered to connect the top plates of the piezoelectric transducers to a common ground. In the next step, properly sized power lines are utilized to distribute the required voltage levels inside the chip according to the current budget for every row. Since the 20-V power supply drives the relatively large load of piezo transducers, the whole metal-five layer is used to distribute the 20-V level from two

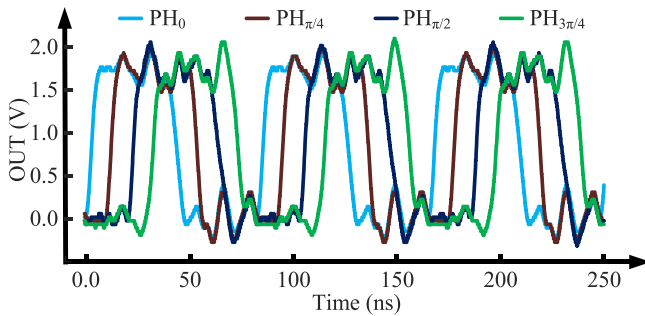


Fig. 15. The measured output waveforms of the coarse DTC.

power pads across the channels. Off-chip components on the test board provide power conversion and regulate the required voltage levels. Since the gate and the source of the HV PMOS are connected to the 18-V and 20-V power supplies, improper power sequencing may damage the HV transistors. In this regard, the same type of low dropout regulators (LDOs) are used to regulate the required HV voltage levels from the same source. Moreover, the load difference between the 18-V and 20-V power supply is compensated in the test board to ensure the correct power sequencing during the start-up and shut-down cycle.

In order to characterize the electrical functionality of the CMOS chip, the ASIC was wire bonded on a printed circuit board (PCB). Then, the wire-bonded PCB was connected to a controller board, which includes the power management unit and a Spartan-7 FPGA development board (CMOD S7, Digilent). The measurement results presented here were obtained by supplying the chip with a 48-MHz input clock and by directly probing the output pads using a 12 C picoprobe.

First, to validate the phasing configurability of the CMOS chip, a 48-MHz clock was applied to the ASIC. Then, the shift registers of the beamforming channels were programmed with random phases using the FPGA of the test board. Fig. 15 illustrates the output signals of the coarse DTC, revealing the expected phases with negligible errors. The maximum measured jitter is around 500 ps which is dominated by the accuracy of the measurement setup and the jitter of the input signal from the external FPGA. However, this value is smaller than the required timing resolution of 10 ns. In the next step, the outputs of eight random beamforming channels with different programmed delays were measured. Fig. 16(a) depicts the transient measured outputs of the beamforming channels, showing that the phases of the outputs are aligned with their programmed phases. The delay transfer function of the measured beamforming channels is shown in Fig. 16(b), where each data point was obtained from a different channel, and the corresponding integral (INL) and differential (DNL) nonlinearity are shown in Fig. 16(c). Furthermore, the delay transfer functions of 16 random beamforming channels from two chips were measured to characterize the uniformity of phases across the beamforming channels. As depicted in Fig. 16(d), the maximum INL and DNL of the measured transfer functions of the beamforming channels are less than 0.35 LSB, which guarantees the monotonicity, with low variability between the two measured chips.

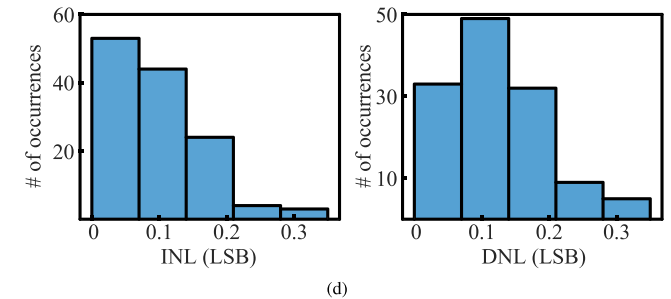
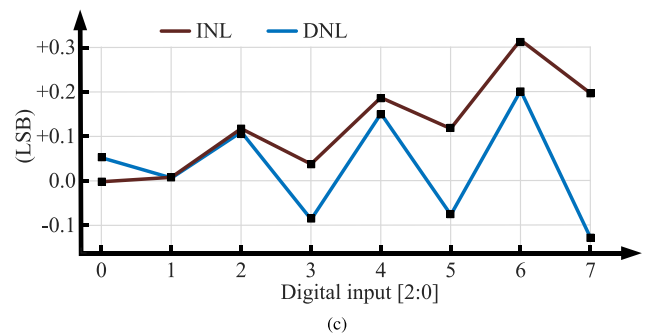
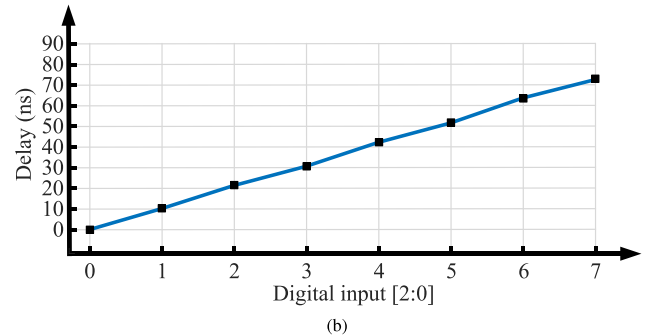
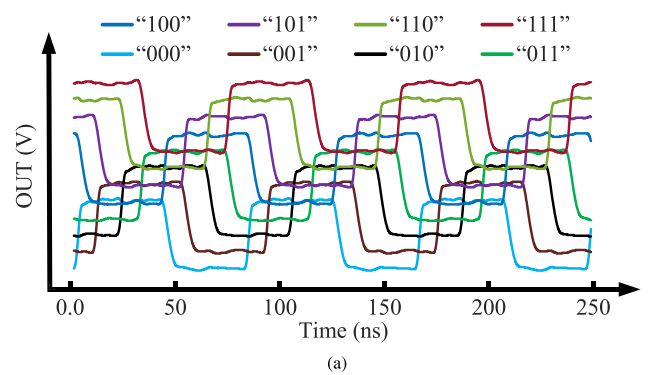


Fig. 16. (a) The measured output waveforms and (b) the delay transfer function of eight randomly selected beamforming channels across the array, showing the linearity of the beamformer circuits. (c) The measured INL and DNL for a beamformer channel in the center of the array. (d) The histograms of measured INL and DNL for 16 randomly selected beamforming channels from two different chips.

These beamforming channels were designed to drive US transducers with resonance frequencies up to 16 MHz. In this work, the pitch size is set to 60 μm , corresponding to a 12 MHz phased-array without any grating lobes in the beam profile, where every beamforming channel drives its pitch-matched US transducer. An array of 2×2 beamforming channels driven with the same phase increases the real pitch size to 120 μm , meaning

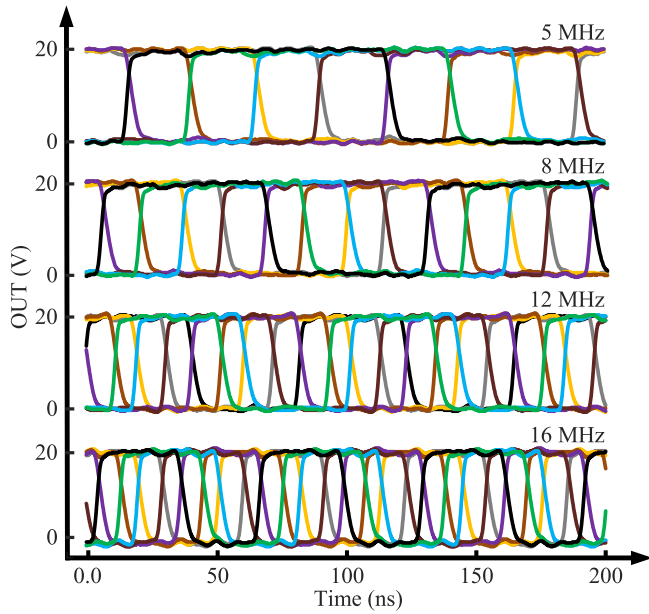


Fig. 17. Measured output waveforms of the beamforming channels for various working frequencies while performing 3-bit phasing.

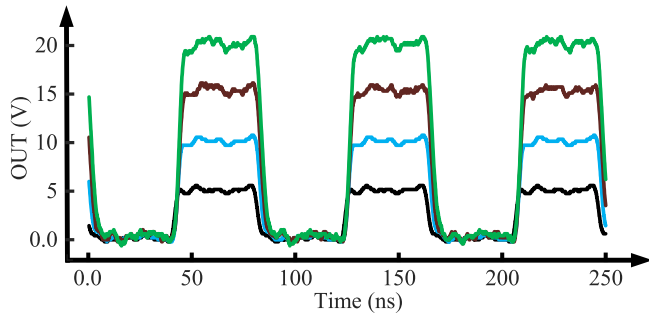


Fig. 18. Measured output waveforms of the beamformer channels for various power supply levels.

that the CMOS chip can drive an array of 6-MHz US transducers without any concerns about the grating lobes. The beamforming channels can be grouped more to increase the real pitch size further. Fig. 17 shows the measured outputs of a transmit channel with different center frequencies, confirming the proper phasing of the ASIC in different center frequencies.

Since changing the acoustic intensity at the focal spot demands varying levels of the HV power supply, the CMOS chip was powered with different supply levels. To perform this controllability, a bench-top programmable power management unit controlled the delivered voltage level to the beamforming channel. In this regard, the source of the HV PMOS and the top connection of the resistor in the HV level shifter are connected to the same potential. This may affect the driveability of the beamforming channels; however, the HV PMOS is over-designed to compensate for this situation. This can also be achieved by connecting both source of the HV PMOS and the HV level shifter to different potentials at the cost of a more complicated power management unit. Fig. 18 reveals that the beamforming channels can generate pulses with variable driving levels from 5 V to 20 V.

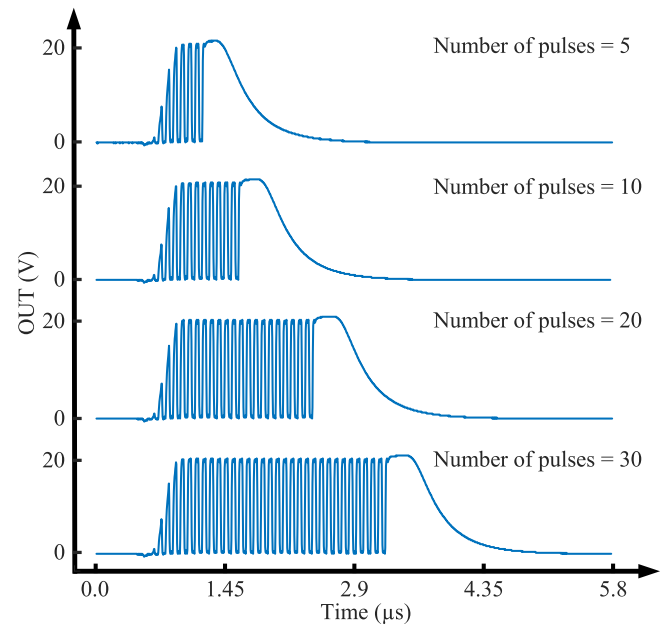


Fig. 19. Measured output waveforms of the beamformer channels while the pulse duration was controlled.

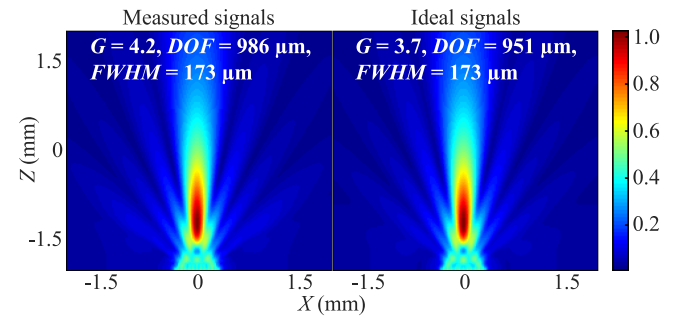


Fig. 20. K-Wave simulation results using the measured electrical signals as acoustic sources for a depth of 2 mm.

Furthermore, the ASIC needs to allow for precise duty cycling to control the pulse duration in ultrasound neuromodulation. Fig. 19 reveals the chip's ability to adjust the pulse duration of the driving signals by controlling the transmitted pulses to the course DTC through the test board. Even though only four different examples from 5 to 30 pulses are shown, the ASIC can operate with an arbitrary number of pulses.

To validate its beam-steering capability, the ASIC was programmed to generate driving signals corresponding to a focal spot at a depth of 2 mm and a steering angle of 0 in both azimuth and elevation planes. The output signals of the beamforming channels were measured for a time duration of 10 μ s. Then, a k-Wave simulation was performed for a 12×12 array of 12 MHz acoustic source with a pitch size of 60 μ m. Fig. 20 compares the beam profile when the measured signals are applied as the acoustic source with the beam profile simulated with ideal signals. It is evident that there is a negligible difference between simulation and measured signals in terms of phased-array gain, DOF, and FWHM.

TABLE I
COMPARISON OF THIS WORK WITH STATE-OF-THE-ART BEAMFORMING CIRCUITS

	[31]	[32]	[23]	[21]	[22]	This work
Application	HIFU	Neuromodulation	Neuromodulation	Neuromodulation	Neuromodulation US powering	Neuromodulation US powering
CMOS process	HV Maxim tech.	Discrete	Discrete	0.18- μm HV	0.18- μm LV	0.18- μm HV
Chip area (mm²)	8 $\times$ 8	N/A	N/A	8 $\times$ 8	5 $\times$ 4	0.9 $\times$ 1.3
# of TX	1024-2D	256-2D	16-1D	1024-2D	676-2D	144-2D
Beam steering	Center focus	2D	1D	2D	2D	2D
Phasing resolution	N/A	N/A	N/A	4-bits	6-bits	3-bits
Driving V_{pp} (V)	60	27-external	100-external	60	5	20
Pitch (μm)	250 (0.84 λ)	1100 (0.74 λ)	1060 (0.58 λ)	250 (0.57 λ)	135 (0.91 λ)	60 (0.5 λ)
Frequency (MHz)	5	1	0.833	3.4	8.4	12
Power consumption per channel (mW)	N/A	N/A	N/A	254 ^a (measured)	N/A	1.6 ^b (measured) 10.9 ^c (simulated)

^aCalculated average power consumption in the continuous pulsing mode. The CMUT transducers are integrated with the CMOS chip.

^bAverage power consumption in the continuous pulsing mode while no load is applied to the CMOS chip.

^cCalculated average power consumption in the continuous pulsing mode. During the circuit-level simulation, the piezoelectric transducers were modeled as a load of 0.3 pF // 20 K Ω , and applied to the beamforming channels.

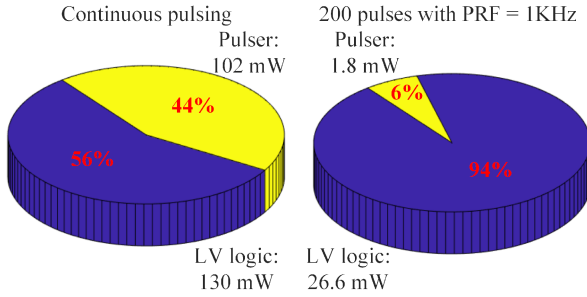


Fig. 21. Measured power consumption breakdown of the CMOS chip for continuous pulsing and 200-pulse bursts with PRF of 1 kHz.

Fig. 21 depicts the power consumption breakdown of the CMOS chip. First, the ASIC was driven by continuous pulses to measure the maximum power consumption of the blocks. In this case, the HV drivers, including only HV PMOS and HV NMOS, contribute to 44 percent of the total power consumption where no load was applied. This is mainly due to the large parasitic capacitance of HV transistors and the array pads. However, a burst of continuous pulses with a given pulse repetition frequency (PRF) is utilized in US neuromodulation. In this regard, 200 pulses with PRF of 1 kHz were applied to the ASIC. In this case, the LV circuits dominate the power as expected, and the total power consumption decreases to less than 30 mW. It is worth pointing that the 5-V, 18-V, and 20-V power supplies are only applied to the HV beamforming channels in the phased array transmitter, and the 1.8-V power supply is shared between the beamforming channels and the coarse DTC. Comparing the size of the coarse DTC with the beamforming circuitry clarifies that most of the power consumption from the 1.8-V power supply is rooted in the LV logic circuits of the beamforming channels.

V. DISCUSSION

Table I shows the comparison between the proposed work and the state-of-the-art of 2D phased-array US transmitters. In terms of the center frequency, this work operates at 12 MHz, the

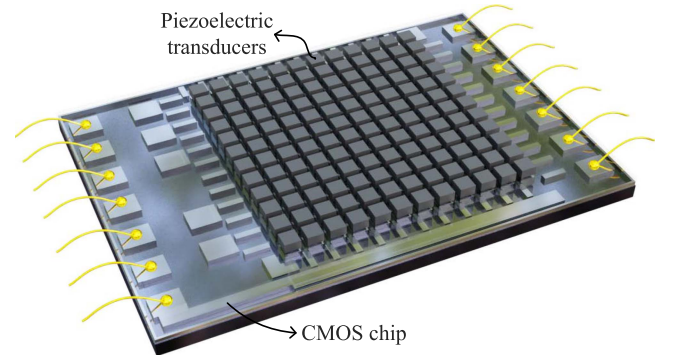


Fig. 22. Envisioned CMOS chip integrated with a 2D array of piezoelectric transducers.

highest among all other works. Furthermore, the pitch size in the center frequency of 12 MHz respects the sound half-wavelength, unlike the others, which can lead to a high-resolution focal spot without any grating lobes in the beam profile, regardless of the steering angle in both the azimuth and elevation planes. Furthermore, the driving signals of the on-chip HV pulsers are four times larger when compared to [22], which only operates at 5 V with limited output intensity, and are lower than [21], which alleviates dynamic power consumption by the ASIC. Since no load is applied to the proposed ASIC, a circuit-level simulation has been done to investigate the effect of piezo load on power consumption. As shown in Table I, integrating the piezoelectric transducers with the CMOS chip will increase the dynamic power consumption; however, the power consumption is still lower than [21] because piezoelectric transducers require lower driving voltages compared with CMUT transducers. In addition, this work has shown that 3-bit phase quantization leads to sufficient focal pressure and spatial resolution while avoiding unnecessarily higher power-consuming and complex circuits [21], [22], and quantization lobes in the field of view.

In summary, to the best of the authors' knowledge, this work constitutes the first 2D pitch-matched ultrasound phased-array

transmitter operating at frequencies exceeding 10 MHz and driving voltages exceeding 5 V. By providing an unprecedented combination of spatial resolution, spatial configurability, and small size, this approach can highly empower ultrasound neuromodulation and ultrasound powering pre-clinical research with rodents, as well as potentiate high-precision sub-cranial cortical stimulation and peripheral nerve stimulation in large animal models and humans. Since this work is used for demonstrating high-frequency operation, the total size of the array is small, which limits the maximum penetration depth to less than 3 mm. This work will continue with the integration of the US transducers with the CMOS chip as illustrated in Fig. 22, for a larger array size towards deeper penetration depth and in vivo validation.

VI. CONCLUSION

This article presents a high-frequency beamforming channel and a 20-V 12×12 phased-array transmitter ASIC, which can allow the implementation of a high spatial resolution and acoustic intensity US transmitter for non-imaging applications. First, an in-depth system-level analysis has been established to study the influence of center frequency, driving voltage, array geometry, and required phasing resolution on the focal spot properties. The presented design methodology allowed us to define the beamforming ASIC's optimum frequency and phasing resolution. Considering the constraint on the fabrication procedure of piezoelectric transducers, the center frequency was set to 12 MHz to achieve a fine spatial resolution and high-intensity focal spot. In addition, the k-Wave simulation results showed that 3-bit phase quantization allows proper steering of the US beam without affecting the spatial resolution and US intensity at the focal spot.

The abovementioned system-level study guided the design of two ASICs presented in this work. Firstly, we present an HV beamforming channel, capable of generating 36-V continuous pulses compatible with 12 MHz pitch-match 2D phased arrays. Secondly, we have shown a 2D pitch-matched beamforming ASIC that generates 12-MHz pulses with 20-V amplitude. The ASIC consists of a coarse DTC and pitch-matched 12×12 beamforming channels, where every channel occupies an area of $60 \times 60 \mu\text{m}^2$, corresponding to half of the ultrasound wavelength. The measurement results proved the functionality of the phased-array transmitter ASIC in terms of phase quantization, showing a maximum DNL of 0.35 LSB. In order to validate the beam-focusing capabilities of the ASIC, the output waveforms of the beamforming channels were applied to the k-Wave, showing a precise focal spot on the determined depth. The CMOS chip allows changing the US intensity of the focal spot by driving the transducers with controllable voltage levels up to 20 V. Although the beamforming ASIC is designed for a center frequency of 12 MHz, it performs 3-bit phasing with various working frequencies. Hence, the integration of this beamforming ASIC with US transducers with different resonance frequencies is possible. This work can pave the way to wearable ultrasound transmitters for emerging non-imaging applications and is tailored for pre-clinical experiments and neuromodulation of superficial neuronal circuits in large animals and humans.

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