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Quasi-vertical Gallium Nitride Diodes for Microwave Power Applications

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Dissertation

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by

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Keywords: quasi-vertical; Gallium Nitride (GaN); Schottky Barrier Diodes (SBD); inductively coupled plasma (ICP) etching; trench etching profile; leakage suppression; edge terminations; microwave power limiter; microwave power detector.

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To all those who have helped and supported me.

Yue Sun

Contents

Summary

The deployment of fifth-generation (5G) networks requires more closely spaced wireless infrastructures with a high output power to deal with high-frequency signal attenuation issues. Microwave power limiters have been widely used in the RF front-end in various wireless communication systems. A diode limiter circuit prevents the damage of sensitive receiver components by allowing RF signals below a certain threshold to pass through, while larger signals exceeding the threshold are attenuated. Many studies have been carried out on Si-based diode limiters in recent years; however, they have shown scant room for further improvement as silicon reaches its theoretical limitations. From this perspective, there is a need for new semiconductor materials to satisfy the requirements of devices. Wide-bandgap materials (e.g., gallium nitride) have recently attracted a great deal of interest due to their superior material properties such as wide band-gap, high electron saturation velocity, and high critical electric field.

Although lateral-structure GaN devices are staying ahead of the pace of industrialization, they still face several constraints and do not reach the GaN material limit due to requiring a high epitaxial layer quality and precise processing. A vertical structure is a convenient solution in Si- or SiC-based devices, which are also attractive alternatives to GaN devices. Quasi-vertical GaN devices have the freedom to select substrates (such as silicon, sapphire, and SiC) by using hetero-epitaxial growth technology. A planar structure design is easy to integrate with other RF components. This dissertation aimed to develop a quasi-vertical GaN diode for high-power RF and microwave applications which could operate in a wide frequency band and at high input power levels, with easy integration and low cost. The scope of this dissertation involved three aspects: design and fabrication of a quasi-vertical GaN device with mesa etching optimization; suppression of reverse leakage with an enhanced breakdown voltage; demonstration of microwave power applications (limiters and detectors) based on developed GaN diodes.

First, a literature summary of the state-of-the-art vertical GaN SBDs is presented in Chapter 2. A trade-off between the $R_{on,sp}$ and BV of a diode is analyzed to characterize the performance of diodes. We discuss the benchmark of $R_{on,sp}$ and BV for vertical GaN SBDs with different substrates (Si, sapphire, and GaN) and various edge terminal techniques. The equivalent circuit model of a diode for studying the high-frequency properties is introduced.

Second, the optimization of mesa etching for a quasi-vertical GaN SBD by inductively coupled plasma (ICP) etching is comprehensively investigated in this chapter. In particular, the microtrench at the bottom corner of the mesa is eliminated by optimizing etch recipes. For the photoresist (PR) masked GaN samples, high source power is the cause of deteriorated mesa sidewall morphology. Although high-temperature (>140 ℃) hard baking prior to etching can produce a smooth

sidewall, the drawbacks are significant and include oblique sidewall profile formation and hard striping. For the SiO_2-masked GaN samples, the micro-trench problem at the bottom corner of the mesa can be reduced or eliminated by reducing the source power or by adding BCl_3 into the Cl_2 plasma. After ICP etching, the use of a TMAH wet treatment for samples can obtain a near-$90°$ steep mesa sidewall that is microtrench-free and has a smooth surface. The proposed etching technique can be extended to other GaN nanostructures, such as hexagonal pyramids and nanowire arrays, which is promising for sensors, vertical transistors, optoelectronics, and photovoltaics.

Third, a quasi-vertical GaN SBD is developed from the perspective of epilayer design, device layout, device modeling, fabrication, and leakage suppression. The design flow and fabrication process of quasi-vertical GaN diodes for microwave power applications are presented. Three solutions are developed to suppress the leakage current, namely, mesa optimization, argon ion terminations, and post-mesa nitridation. The experiment results show that our diode has the lowest leakage current density at 80% of the BV among the reported vertical GaN SBDs for a BV between 120 and 250 V. Combining mesa optimization and post-mesa nitridation technology effectively enhances the breakdown voltage and achieves excellent conduction characteristics.

Fourth, a high-performance quasi-vertical GaN Schottky diode on a sapphire substrate and its application for high-power microwave circuits are investigated. We experimentally demonstrate the use of a vertical GaN SBD for L-band microwave power limiters for the first time ever. The GaN SBD limiter can handle at least 40 dBm of CW input power at 2 GHz without failure, which is comparable to a commercial Si-based diode limiter. Then, we experimentally demonstrate a quasi-vertical GaN SBD with post-mesa nitridation for high-power and broadband microwave detection. The fabricated quasi-vertical GaN diode reaches a high forward current density of 9.19 kA/cm^2 at 3 V, and BV of 106 V. An extremely high output current of 400 mA is obtained when the detected power reaches 38.4 dBm at 3 GHz in pulsed-wave mode.

Finally, all of the research content mentioned in this thesis is summarized, and the problems needing to be further investigated with lucubrate direction are indicated.

Samenvatting

De uitrol van de vijfde generatie (5G) communicatie technologie van de vijfde generatievereist dichter bij elkaar geplaatste draadloze infrastructuren met een hoog uitgangsvermogen om de problemen met de hoogfrequente signaalverzwakking aan te pakken. Microgolfvermogensbegrenzers zijn veel gebruikt in de RF-front-end in verschillende draadloze communicatiesystemen. Een diodebegrenzercircuit voorkomt de schade aan gevoelige ontvangercomponenten door RF-signalen onder een bepaalde drempel door te laten, maar grotere signalen die de drempel overschrijden, worden gedempt. Er zijn de afgelopen jaren veel studies uitgevoerd naar op Si gebaseerde diodebegrenzers, maar ze toonden weinig ruimte voor verdere verbetering naarmate het silicium zijn theoretische beperkingen bereikte. Tegen deze achtergrond is er behoefte aan nieuwe halfgeleidermaterialen om aan de apparaatvereisten te voldoen. Wide band-gap materialen (bijv. Gallium Nitride) hebben onlangs veel belangstelling getrokken, toegeschreven aan hun superieure materiaaleigenschappen zoals brede band-gap, hoge elektronenverzadigingssnelheid en hoog kritisch elektrisch veld.

Hoewel gan-apparaten met laterale structuur de industrialisatie blijven voorblijven, worden ze nog steeds geconfronteerd met verschillende beperkingen en bereiken ze de GaN-materiaallimiet niet vanwege de vereiste hoge epitaxiale laagkwaliteit en nauwkeurige verwerking. De verticale structuur is een handige oplossing in Si-gebaseerde of SiC-gebaseerde apparaten, wat ook een aantrekkelijk alternatief is voor GaN-apparaten. Quasi-verticale GaN-apparaten hebben de vrijheid om substraten (zoals silicium, saffier en SiC) te selecteren met behulp van hetero-epitaxiale groeitechnologie. Het ontwerp van de vlakke structuur is eenvoudig te integreren met andere RF-componenten. Dit proefschrift heeft tot doel een quasi-verticale GaN-diode te ontwikkelen voor rf- en microgolftoepassingen met een hoog vermogen, die kan werken in een brede frequentieband en hoge ingangsvermogensniveaus met eenvoudige integratie en lage kosten. De reikwijdte van dit proefschrift omvat drie aspecten: Ontwerp en fabricage van quasi-verticaal GaN-apparaat met mesa-etsoptimalisatie; Onderdrukking van omgekeerde lekkage met een verbeterde doorslagspanning; Demonstratie van microwave power toepassingen (limiters en detectoren) op basis van ontwikkelde GaN diodes.

Ten eerste werd de literatuursamenvatting voor de state-of-the-art verticale GaN SBD's gepresenteerd in hoofdstuk 2. Een afweging tussen $R_{on,sp}$ en BV van een diode werd geanalyseerd om de prestaties van diodes te karakteriseren. We bespraken de benchmark van $R_{on,sp}$ en BV voor verticale GaN SBD's met verschillende substraten (Si, saffier en GaN) en verschillende edge terminal technieken. Onmiddellijk werd het equivalente circuitmodel van een diode voor het bestuderen van de hoogfrequente eigenschappen geïntroduceerd.

Ten derde is de quasi-verticale GaN SBD ontwikkeld vanuit het perspectief van

epi-laagontwerp, apparaatlay-out, apparaatmodellering, fabricage en lekonderdrukking. Het ontwerpstroom- en fabricageproces van quasi-verticale GaN-diodes voor voedingsmagnetrontoepassingen werd gepresenteerd. Er werden drie oplossingen ontwikkeld om de lekstroom te onderdrukken, waaronder mesa-optimalisatie, Argon-ionafsluitingen en post-mesanitrering. De experimentresultaten tonen aan dat onze diode de laagste lekstroomdichtheid heeft bij 80% van de BV onder de gerapporteerde verticale GaN SBD's voor de BV tussen 120 V en 250 V. De combinatie van mesa-optimalisatie en post-mesa nitridatietechnologie verbetert effectief de doorslagspanning en bereikt uitstekende geleidingseigenschappen.

Ten vierde werden een krachtige quasi-verticale GaN Schottky-diode op Sapphire-substraat en de toepassing ervan voor krachtige microgolfcircuits uitgevoerd. We hebben voor het eerst ter wereld experimenteel een verticale GaN SBD voor L-band microgolfvermogensbegrenzers gedemonstreerd. De GaN SBD-begrenzer kan zonder storing ten minste 40 dBm CW-ingangsvermogen bij 2 GHz aan, wat vergelijkbaar is met de commerciële Si-gebaseerde diodebegrenzer. Vervolgens hebben we experimenteel een quasi-verticale GaN SBD aangetoond met post-mesanitratie voor detectie van hoge vermogens en breedbandmagnetrons. De gefabriceerde quasi-verticale GaN-diode bereikte een hoge voorwaartse stroomdichtheid van 9.19 kA/cm^2 bij 3 V en BV van 106 V. Een extreem hoge uitgangsstroom van 400 mA wordt verkregen wanneer het gedetecteerde vermogen 38.4 dBm bereikte bij 3 GHz in gepulseerde golfmodus.

Ten slotte worden alle onderzoeksinhouden die in dit proefschrift worden genoemd samengevat en worden de problemen aangegeven die verder moeten worden opgelost met lucubrate richting.

1

Introduction

With the introduction of 5G, the modern RF (radio frequency) frontend module requires a high-performance device (transistor or diode), which can operate in a wide bandwidth and a high input power with easy integration and low cost. Today silicon devices have reached their physical limits either in terms of scaling down or in terms of their physical properties. Gallium nitride (GaN) has attracted increased attention because of superior material properties, such as high electron saturation velocity and high electrical field strength. Quasi-vertical GaN diodes have the advantages of withstanding a high reverse voltage without enlarging the device area, a high current density, reliable, and low cost, promising for high-power microwave applications. However, several issues limit the possibility of further improvement, including deep mesa etch, and reverse leakage suppression. Making efforts in device design and fabrication is essential to help quasi-vertical GaN diode reach an excellent performance in power microwave applications.

Parts of this chapter have been published in Electronics **324**, 575 (2019) [1].

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1.1. Background

With the popularity of fifth-generation (5G) mobile communication technology, the enhanced data transmission rate throughout the network delivers a much better experience with customers on the Internet. Fifth-generation base stations consume more power than 4G base stations, thus inevitably increasing the telcos energy costs. The data show that powering cellular base stations worldwide used nearly 1% of all global electricity in 2012 [2]. By 2020, the telecom industry even consumes 2% to 3% of total global energy. Consequently, improving the energy efficiency in 5G communication has become a hot topic in recent years.

In wireless networks, much of the energy is wasted by grossly inefficient electronic components and modules such as power amplifiers and rectifiers. In recent decades, wireless infrastructure systems have mainly employed Si devices such as a laterally diffused metal oxide semiconductor (LDMOS), which showed scant room for further improvement, as the silicon reached its theoretical limitations. The deployment of 5G requires more closely spaced wireless infrastructures with high-output power to deal with high-frequency signal attenuation issues [3]. Thus, with the introduction of 5G, the modern RF (radio frequency) frontend module requires a high-performance device (transistor or diode), which can operate in a wide bandwidth and a high input power with easy integration and low cost.

Microwave power limiters have been widely used in the RF frontend in a variety of wireless communication systems [4], such as cellular infrastructure (including 5G) and microwave radio communications [5]. A diode limiter circuit prevents the damage of sensitive receiver components by allowing RF signals below a certain threshold to pass through, but larger signals exceeding the threshold are attenuated [6]. This means that to develop a high-performance limiter, there are two goals: A very low conduction loss and a very high block voltage. Thus, the target for a limiter diode is to reach a low R_{on}, a low capacitance, and a high BV toward meeting the above goals. Many studies have been carried out on Si-based diode limiters in recent years [7–9]; however, they showed scant room for further improvement as the silicon reached its theoretical limitations. they showed scant room for further improvement, as the silicon reached its theoretical limitations. Today, silicon devices have reached their physical limits either in terms of scaling down or in terms of their physical properties[10]. In this background, there is a need for new semiconductor materials to be satisfying the device requirements. From this perspective, there is a need for new semiconductor materials to satisfy the device requirements. Wide band-gap materials (e.g., gallium nitride) have recently attracted much interest, attributed to their superior material properties such as wide band-gap, high electron saturation velocity, and high critical electric field.

Table 1.1 shows the primary properties of GaN and Si. The critical electric field of GaN is 11 times higher than Si, which enables GaN RF devices to handle a higher reverse voltage. Both electric field and electron velocity are essential material properties for the requirements of a high-frequency power transistor. In 1991, Johnson derived a figure of merit JFOM, which characterizes the power frequency performance of transistors based on materials [11]. A higher JFOM means that GaN is more suitable for high-frequency power transistor applications and requirements

Table 1.1: Physical properties of Si and GaN

Materials	E_g (eV)	μ_n $(cm^2/V \cdot s)$	E_c (MV/cm)	V_{sat} $(10^7 cm/s)$	K $(W/m \cdot K)$	$JFOM$
Si	1.12	1350	0.3	1	145	1
GaN	3.44	1090 (bulk) 2000 (2DEG)	3.3	2.5	253	27.5

E_g, energy band-gap; μ_n, electron mobility; E_c, critical electric field; V_{sat}, electron saturation velocity; K, thermal conductivity; $JFOM = (E_c * V_{sat})/(2\pi)$

than Si. Meanwhile, GaN has the superior material properties of high electron saturation velocity, high electrical field strength, and high operating temperature [12, 13], which is well suited for high-power microwave applications.

1.2. GaN-based RF devices

A RF power amplifier (PA) is an integral part of various wireless transmitters, which is located in the final active stage that drives the transmitting antenna. Figure1.1 compares the semiconductor technologies for RF devices in PA applications [14]. GaAs-based RF high-electron mobility transistor (HEMT) and heterojunction bipolar transistor (HBT) devices consistently dominate the RF PA market, especially in high-frequency applications. Si-based RF devices are competitive against GaAs devices in the low-frequency range due to the advantages of low-cost and large-sized silicon wafers. As GaN technologies ramp up, commercial GaN HEMT discrete power transistors can deliver very high-power density and are more suitable for deploying low-frequency RF PA applications. GaN-based MMICs are of more interest at higher frequencies, as they enable matching, system size reduction, and, eventually, cost efficiency.

A GaN-based lateral structure utilizes an AlGaN/GaN hetero-junction to form a two-dimensional electron gas (2DEG) conduction channel with the good features of a high carrier concentration ($> 10^{13} cm^{-3}$) and high carrier mobility ($2000 cm^2/V \cdot s$). This highlights a GaN HEMT as a most attractive lateral device and has been commercialized in power and RF electronic applications over the past few years. Moreover, lateral AlGaN/GaN SBD with extremely low turn-on voltage and low on-resistance is considered a rectifier, used in microwave power transmission applications [15–17].

The charge trapping effects induced by the interface states from the surface or GaN buffer layer are still the primary challenge in GaN heterojunction devices that will cause a significant drop in RF output power [18–23]. Many solutions have been presented to solve these problems, such as a passivation layer[24], field plate [25, 26], and tri-gate [27] structure. In spite of these efforts for making some progress in improving lateral GaN device performance, they are not reaching the GaN material limit as a result of requiring a high epitaxial layer quality and precise

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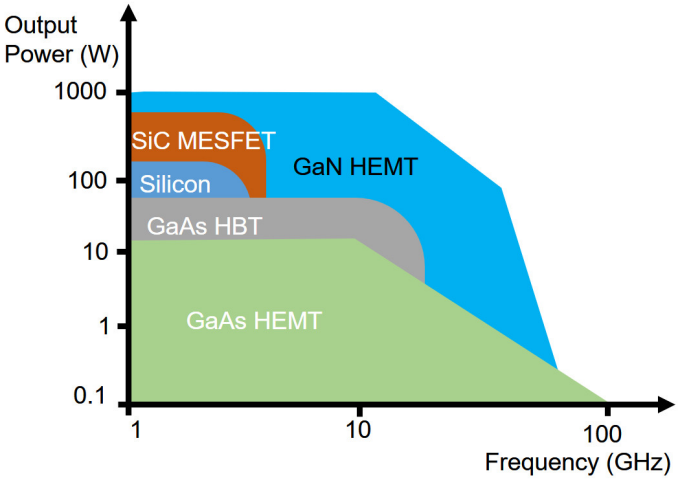


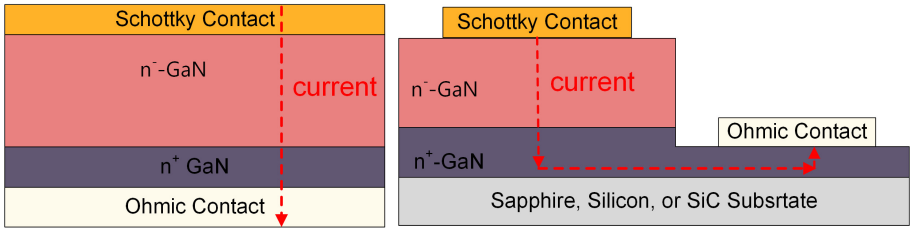
Figure 1.1: Power-frequency diagram of application space for several semiconductor materials.

processing[28].

A vertical structure is a convenient solution in Si- or SiC-based devices, which are also an attractive alternative for GaN devices. Recent progress in vertical GaN transistors has mainly involved current-aperture vertical electron transistors (CAVETs)[29], trench MOSFETs[30], fin-channel MOSFETs[31], and fin-JFET [32]. A vertical diode has drawn more attention to the early exploratory research of GaN-based devices because of the more implementable device structure than vertical transistors. One of the advanced features of a vertical GaN device is withstanding a high reverse voltage without enlarging the device area. Thus, in previous research, most of the vertical GaN diode has been dedicated to high-voltage and high-power applications. Researchers are rarely concerned about vertical GaN devices for RF applications due to the lower carrier mobility of bulk GaN than the AlGaN/GaN 2DEG channel. However, with the rapid development of bulk GaN epilayer growth technology, the mobility of bulk GaN has increased to 1090 $cm^2/V \cdot s$ at room-temperature with a carrier concentration of $\sim 2 \times 10^{16}\, cm^{-3}$ for n-GaN on an Si substrate [33], enabling a lower R_{on} and higher current density of vertical GaN devices than before. In addition, electrothermal simulation results indicate that using a vertical device structure effectively improves the peak operating temperature of GaN transistors to 150 °C with enhanced thermal performance [34]. Therefore, it is really worthwhile exploring vertical GaN devices that further expand the potential of GaN material in a high-power RF application.

1.3. Quasi-vertical GaN Schottky diodes

Since the year 2000, GaN-based rectifiers (including Schottky barrier diodes (SBDs) and PN junction diodes) have attracted considerable interest from researchers.



(a) Fully-vertical structure (b) Quasi-vertical structure

Figure 1.2: Gallium Nitride-based Schottky barrier diode (GaN SBD) structures and current flowing directions.

With the absence of minority carrier accumulation and low barrier height, SBDs can operate at higher frequencies with a lower turn-on voltage (V_{on}) than PN junction diodes. Yoshimoto et al.[35] demonstrated the operation of a GaN SBD at a high frequency with a low power loss in the power converter, comparing it with a commercial Si fast recovery diode (FRD) and an SiC SBD via a typical E resonant rectifier tested at a frequency of 30 MHz.

The schematic of a typical vertical GaN Schottky diode is shown in Figure1.2, including its quasi-vertical and fully vertical structure[1]. For the fully vertical structure, the electrodes are located on the two sides of the wafer separately, with current flowing from anode to cathode through the drift layer in a vertical direction, as shown in Figure1.2a. The fully vertical device has the advantages of an effective device size and good thermal performance by cooling from both sides of the wafer. However, the development of fully vertical GaN devices is limited by the expensive and small-sized homogeneous GaN substrate[36].

For the quasi-vertical structure, a mesa is processed and both the anode and cathode are located on the same side of the wafer, as shown in Figure1.2b. The first quasi-vertical GaN diodes were demonstrated on a sapphire substrate in 2000 [37] and on a silicon substrate in 2014 [38], separately. Quasi-vertical GaN devices have the freedom to select substrates (such as silicon, sapphire, or SiC) by using hetero-epitaxial growth technology. The planar structure design is easy to integrate with other RF components. Another advantage is compatible with the mature semiconductor manufacturing lines if grown on an Si substrate. Therefore, quasi-vertical structures are more promising than fully vertical structures for future GaN-based vertical devices.

1.4. Problems and challenges

To develop a quasi-vertical GaN-based Schottky diode for microwave power applications, we face several problems, split into the following three aspects:

First, the formation of a GaN trench or mesa requires a deep etching technique with a highly anisotropic profile, possibly creating defects on the sidewall and etched surface. These etch defects mainly consist of sidewall erosion, grass on the surface, columns, pits or cavities, and microtrenches. The complicated GaN etching

process makes removing these defects difficult. Different to shallow etching in lateral GaN HEMT devices, deep trench etching technology is not mature and needs further development in vertical GaN devices. Although much effort has been made on GaN etching, some of the critical issues have not yet been solved. A mircotrench on the corner of etched mesa is the most critical defect in these unsolved issues, resulting in a significant leakage current and hiding an enormous risk for the reliability of high-power GaN diodes. A few works on SiC or Si etching have provided some thoughts for eliminating GaN microtrenches. However, due to the diversity of etching reaction mechanisms among semiconductors, it is challenging to effectively solve the microtrench problem in GaN mesa etching.

Second, the power handling of microwave diodes corresponds to the capability of conducting a maximum current and withstanding a peak reverse voltage. A higher R_{on} in a diode brings higher power consumption, thus generating more heat to burn out the device. The peak voltage of an RF signal is not allowed to exceed the BV of a diode, otherwise it will permanently destroy said diode. Therefore, diodes simultaneously require a low R_{on} and a high BV to reach high-power handling. However, a large reverse leakage current of the diode can cause pre-breakdown and reliability problems. Some works suggest that the leakage can be inhibited by using edge terminations[39], reducing the dislocation density of the drift layer[40], passivating the etched mesa [41], or reducing the interface defect density at the Schottky contact interface [42]. In general, the microwave GaN diode requires a small device area and a thin drift layer, which is sensitive to the damage or traps induced by etching or the plasma treatment processes. Therefore, it is essential to find an effective solution and analyze the mechanism of leakage suppression in a microwave power GaN diode more clearly. In addition, current-crowding effects (CCEs) strongly influence the forward characteristic of a quasi-vertical diode, which needs to be further optimized by a certain device structure design[43–45].

Third, silicon-based[1] and GaAs-based[2] microwave diodes have been demonstrated with a high frequency but limited with the input power by the low BV [46]. These diodes show scant room for further improvement, as the semiconductor material reached its theoretical limitations. GaN has a much higher electron velocity in the high electric field, leading to a higher BV and a higher current density of GaN diodes, achieving a high microwave power level. However, due to the limitations of high-quality GaN materials and obstacles of the heterojunction AlGaN/GaN structure, GaN-based high-power microwave diodes are still a gap in the market. The challenge is to design, fabricate, and characterize a vertical GaN Schottky diode for microwave applications with high power and a wide frequency band.

1.5. Aim and scope

This dissertation aimed to develop a quasi-vertical GaN diode for high-power RF and microwave applications, which can operate in a wide frequency band and at high input power levels with easy integration and a low cost. The scope of this

[1] BAT63-02V supplied by Infineon Technologies
[2] MA4E1317 supplied by MACOM

dissertation involves three aspects:

1. Design and fabrication of a quasi-vertical GaN device with mesa etching optimization;
2. Suppression of reverse leakage with an enhanced breakdown voltage;
3. Demonstration of microwave power applications (limiters and detectors) based on developed GaN diodes.

1.6. Thesis outline

This thesis aimed to address the challenges listed above by developing a deep GaN trench etching technology and exploring the potential of quasi-vertical GaN diodes for high-power microwave applications. This research covered the device design and fabrication technology to circuit applications based on the simulation and experimental results. The rest of this thesis is organized into six chapters:

- In Chapter 2, we present the basic structure of the typical vertical Schottky diode and discuss the basic principles under both forward and reverse bias. A trade-off between $R_{on,sp}$ and BV is analyzed to characterize the performance of diodes. At once, the equivalent circuit model of a diode for studying the high-frequency properties is introduced. Then, we provide a literature summary for state-of-the-art vertical GaN SBDs. Finally, the benchmark for vertical GaN SBDs with different substrates (Si, sapphire, and GaN) and various edge terminal techniques are presented and discussed.
- In Chapter 3, the optimization of mesa etching for a quasi-vertical GaN SBD by inductively coupled plasma (ICP) etching is comprehensively investigated, including the selection of the etching mask, ICP power, radio frequency (RF) power, a ratio of mixed gas, flow rate, and chamber pressure. In particular, the microtrench on the bottom corner of the mesa sidewall was eliminated by optimizing the etch recipes. Finally, the mesa structure achieved a highly anisotropic profile by combining ICP dry etching and a tetramethylammonium hydroxide (TMAH) wet treatment. In addition, the proposed etching technique was not confined to fabricating a GaN mesa structure for quasi-vertical devices, also extended to other structures, such as hexagonal pyramids and nanowire arrays, promising for sensors, vertical transistors, optoelectronics, and photovoltaics.
- In Chapter 4, the quasi-vertical GaN SBD is developed from the perspective of an epilayer structure design, device layout, device modeling, fabrication, and leakage suppression solutions. First, the design flow of quasi-vertical GaN diodes for microwave power applications is presented, including the device performance indicators, substrate selection, and device layout. Then, the quasi-vertical GaN SBD fabrication process is elaborated in schematic diagrams and real pictures. Finally, three solutions were developed to suppress the leakage current, including mesa optimization, argon ion terminations, and post-mesa nitridation.
- In Chapter 5, we report the high-performance quasi-vertical GaN Schottky diode on a sapphire substrate and its application for high-power microwave

circuits. First, we report the first demonstration of an L-band high-power limiter based on our quasi-vertical GaN SBD in a real-life setting. By using steep-mesa technology, the spacing between the anode and cathode can be reduced to 2 μm, leading to a further reduction in the on-resistance of the SBD. Second, we experimentally demonstrate a quasi-vertical GaN SBD with post-mesa nitridation for high-power and broadband microwave detection. The simulation of the designed circuit and the experimental results can be well corroborated in the circuit applications.

- Chapter 6 concludes the dissertation, summarizes the contributions, and discusses recommendations derived from the results for future research.

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2

Vertical GaN Schottky diodes and state of the art

Gallium nitride (GaN)-based vertical Schottky barrier diode (SBD) has been demonstrated outstanding features in high-frequency and high-power applications. This chapter first present the basic structure of the typical vertical Schottky diode and discuss the basic principles under both forward and reverse bias. A trade-off between $R_{on,sp}$ and BV was analyzed to characterize the performance of diodes. At once, the equivalent circuit model of a diode for studying the high-frequency properties is introduced. Then, we provide a literature summary for state-of-the-art vertical GaN SBDs. Finally, the benchmark for vertical GaN SBDs with different substrates (Si, sapphire, and GaN) and various edge terminal techniques are presented and discussed.

Parts of this chapter have been published in Electronics **8**, 575 (2019) [1].

2

2.1. Basic principles of vertical Schottky diodes

2.1.1. Forward conduction and reverse blocking

A conventional SBD structure consists of anode metal, drift layer, substrate, and cathode metal. There are four transport processes when forward biasing the Schottky diode. Figure2.1 is the schematic of carrier transport processes.

1. Thermionic Emission. The electrons emitted from the semiconductor into metal over the barrier.
2. Tunneling. The electrons directly move through the barrier based on the quantum mechanical theory.
3. The recombination of electron-hole appears in the depletion region.
4. The recombination of electron-hole appears in the neutral region.

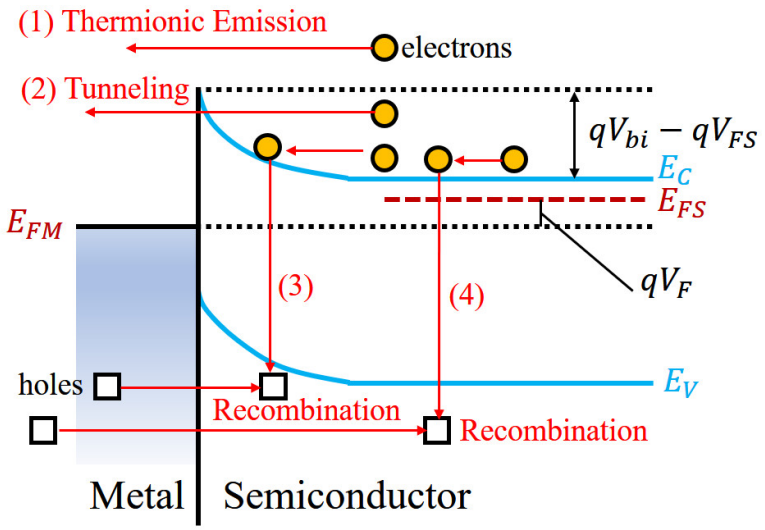

Figure 2.1: Energy band diagram for a metal-semiconductor junction under forward bias (electrons are shown as yellow solid circles and holes as hollow squares).

Due to the sufficiently wide depletion region of the Schottky diode, there is a very low conduction current moves through the barrier in the tunneling process. The recombination current can be negligible in both the depletion and neutral regions. Therefore, thermionic emission (TE) is the primary transport process in this conventional Schottky diode. According to the theory of thermionic emission, the current flow across the Schottky barrier interface [2]

$$J = AT^2 \mathrm{e}^{-(q\Phi_\mathrm{B}/kT)} \left[\mathrm{e}^{(qV/kT)} - 1\right] \tag{2.1}$$

where A is the effective Richardson's constant, Φ_B is the Schottky barrier height (SBH), T is the absolute temperature, k is the Boltzmann's constant, and V is the

applied bias. The ambipolar diffusion coefficient Richardson's constant is expressed as

$$A = (4\pi q m_n^* \, k^2)/h^3 \tag{2.2}$$

where m_n^* is the effective electron quality and h is Planck's constant. The theoretically calculated value of A for GaN is 26.4 $A \cdot cm^{-2} \cdot K^{-2}$ [3].

The saturation current density is given by

$$J_s = AT^2 \mathrm{e}^{-(q\Phi_\mathrm{B}/kT)} \tag{2.3}$$

When applying forward bias, the saturation current is extremely small compared to the forward current that the first term in the square brackets of the equation2.1 becomes dominant. The forward current density is given by

$$J = J_s \mathrm{e}^{(qV_{FS}/kT)} \tag{2.4}$$

where V_{FS} is forward voltage drop across the Schottky contact. Therefore, the total forward voltage drop across the Schottky diode is given by

$$V_F = V_{FS} + V_R = \frac{kT}{q} \ln\left(\frac{J_F}{J_s}\right) + R_{s,sp} J_F \tag{2.5}$$

where $R_{s,sp}$ is the total specific series resistance, J_F is the forward current density.

A typical vertical Schottky diode structure and its electric field distribution under reverse bias are shown in Figure2.2.

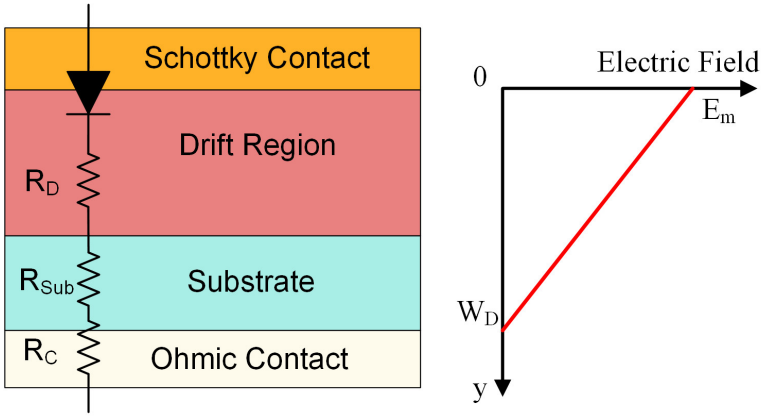

Figure 2.2: Basic vertical Schottky diode structure and the electric field distribution when applying reverse bias.

In terms of the device structure, the total specific series resistance ($R_{s,sp}$) consists of three parts: the Ohmic contact resistance of the cathode (R_C), the substrate resistance ($R_{Sub.}$), and the specific on-state resistance of the drift layer ($R_{D,sp}$). The total specific series resistance is given by

$$R_{s,sp} = R_{D,sp} + R_{Sub.} + R_C \tag{2.6}$$

The $R_{on,sp}$ of an ideal vertical Schottky diode neglects the resistance of substrate and Ohmic, which is equal to $R_{D,sp}$ and delivered by

$$R_{D,sp} = W_D/(q\mu_n N_D) \tag{2.7}$$

where W_D is the maximum width of the depletion region, q is the electronic charge, μ_n is the electron mobility, and $N_D$is the doping concentration of the drift layer. Figure2.2 reveals that the maximum electric field is located at the interface between anode and semiconductor. As a function of depletion distance, the electric field distribution is given by

$$E(y) = -\frac{qN_D}{\varepsilon_s}(W_D - y) \tag{2.8}$$

where ε_s is the relative dielectric constant of the drift layer. Integration of the electric field distribution through the depletion region provides the potential distribution when applied reverse bias (V_R):

$$V(y) = \frac{qN_D}{\varepsilon_s}(W_D y - \frac{y^2}{2}) \tag{2.9}$$

By using the boundary condition $V(W_D) = V_r$, the maximum width of the depletion region can be related to applied reverse bias

$$W_D = \sqrt{(2\varepsilon_s V_r)/(qN_D)} \tag{2.10}$$

According to the equation2.10, the reverse breakdown voltage is inversely dependent on the doping level in the drift layer and positively dependent on the depletion width. From equation2.8-2.10, the relationship of E_m, N_D and V_r can be expressed as

$$E_m = \sqrt{(2qN_D V_r)/\varepsilon_s} \tag{2.11}$$

where E_m is the maximum electric field at the junction. The critical electric field is the maximum electric field of the semiconductor when it appears a significant impact ionization phenomenon under applied reverse bias. The breakdown voltage (BV) is determined by the ionization integral, becoming equal to unity:

$$\int_0^{W_D} \alpha \mathbf{d}y = 1 \tag{2.12}$$

where α is the impact ionization coefficients[1]. The impact ionization coefficients for Si[2], SiC[3], and GaN[4] are presented by

$$\alpha_{(Si)} = 1.8 \times 10^{-35} E^7 \tag{2.13}$$

[1]Impact Ionization Coefficients α is defined as the number of electron-hole pairs created by an electron or hole traversing 1 cm through the depletion layer along the direction of the electric field.
[2]The$\alpha_{(Si)}$ is referred to as the Fulop's approximation[4]
[3]The $\alpha_{(SiC)}$ is referred to as the Baliga's power law approximation[5]
[4]The $\alpha_{(GaN)}$ is referred to as the Ozbek-Baliga power law approximation[6]

$$\alpha_{(SiC)} = 3.9 \times 10^{-42} E^7 \tag{2.14}$$

$$\alpha_{(GaN)} = 1.5 \times 10^{-42} E^7 \tag{2.15}$$

Where E is the electric field. Substituting the integral results into the equation2.8, theoretical solutions for the BV can be derived for Si, SiC and GaN:

$$BV(Si) = 5.34 \times 10^{13} E^{-3/4} \tag{2.16}$$

$$BV(4H-SiC) = 3.0 \times 10^{15} E^{-3/4} \tag{2.17}$$

$$BV(GaN) = 2.51 \times 10^{15} E^{-3/4} \tag{2.18}$$

Combining the equation2.16, equation2.17 and equation2.18 with equation2.10, the critical electric field (E_c) for Si, SiC and GaN are given by

$$E_c(Si) = 0.4 \times 10^4 N_D^{1/8} \tag{2.19}$$

$$E_c(4H-SiC) = 3.3 \times 10^4 N_D^{1/8} \tag{2.20}$$

$$E_c(GaN) = 3.19 \times 10^4 N_D^{1/8} \tag{2.21}$$

According to the above equations, the relationship between $R_{on,sp}$ and BV can be expressed as[7]

$$R_{on,sp} = 4BV^2/\varepsilon_s \mu_n E_C^3 \tag{2.22}$$

where the $R_{on,sp}$ is a ideal specific on-resistance of the drift region, $\varepsilon_s \mu_n E_c$ is the intrinsic properties of semiconductor materials, commonly referred to as Baliga's figure of merit (BFOM)[7].

Table 2.1: Physical properties of Si, GaAs, SiC, and GaN

Materials	E_g eV	ε	μ_n $cm^2/V \cdot s$	E_c MV/cm	V_{sat} $10^7 cm/s$	K $W/m \cdot K$
Si	1.12	11.8	1350	0.3	1	145
GaAs	1.42	13.1	8500	0.4	2	50
4H-SiC	3.26	10	720	2.0	2	370
GaN	3.44	9	1090 (bulk)	3.3	2.5	253

E_g, energy band-gap; ε, relative dielectric constant; μ_n, electron mobility; E_c, critical electric field; V_{sat}, electron saturation velocity; K, thermal conductivity.

Table 1 lists the physical properties of Si, GaAs, SiC, and GaN[1, 8, 9]. The critical electric field of GaN is 11 times greater than Si and the saturation velocity is 2.5 times greater than Si. According to the equations above, the ideal $R_{ON,sp}$ for the drift region of a vertical power device is given by [2, 10]

$$R_{on,sp}(Si) = 5.93 \times 10^{-9} BV^{2.5} \tag{2.23}$$

$$R_{on,sp}(4H-SiC) = 2.97 \times 10^{-12} BV^{2.5} \tag{2.24}$$

$$R_{on,sp}(GaN) = 3.12 \times 10^{-12} BV^{2.5} \tag{2.25}$$

It can be concluded that the ideal specific on-resistance for GaN vertical power devices is 1.78-times smaller than that for 4H-SiC and 2130 times smaller than that for silicon at the same breakdown voltages[10].

2.1.2. RF equivalent circuit

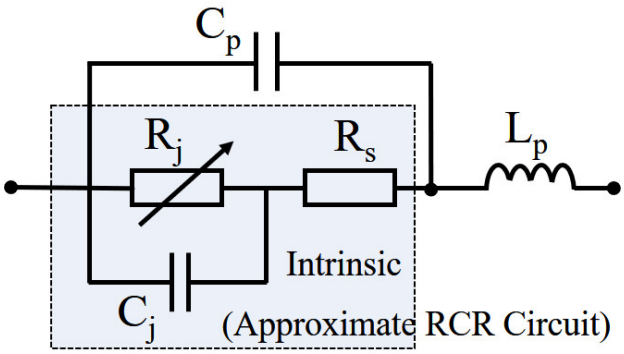

Figure 2.3: The RF equivalent circuit of forward biased Schottky diode.

An equivalent diode circuit describes the electrical characteristics of a diode by choosing a combination of some linear and passive elements, as shown in Figure2.3. According to the RCR network circuit theory, the cut-off frequency of diode intrinsic part is given by

$$f_T = 1/(2\pi R_s C_j)\sqrt{2-(R_s/R_j-1)^2} \tag{2.26}$$

Where R_j is the junction resistance and C_j is the junction capacitance of a diode. R_s is the total series resistance of the diode, as described in equation2.6. Both R_s and C_j are considered as linear components. L_p and C_p are the parasitic inductance and capacitance related to the packaging of the diode.

A useful figure of merit called cut-off frequency would be the quality of high-frequency performance for RF devices. When diode is in off-sate, the $R_j \gg R_s$, the f_T can be simplified as

$$f_T = 1/(2\pi R_s C_j) \tag{2.27}$$

Both low total capacitance and low series resistance are essential for a diode to achieve high cut-off frequency. The specific junction capacitance (capacitance per unit area) of a Schottky diode associated with this depletion region is given by

$$C_{j,sp} = \varepsilon_s / W \tag{2.28}$$

where W is the depletion width, ε_s is the relative dielectric constant of semiconductor. The C_j at zero bias is critical for a diode to achieve a high f_T, which can be reduced by decreasing the doping level of the drift layer or reducing the Schottky contact area, however, leading to an increase of R_{on}.

2.2. Review of the GaN-based vertical SBDs

2.2.1. Selection of different substrates

The GaN crystal substrates are ideal for growing the GaN epi-layer, but it is still not mature due to a limited wafer size and high cost. Thus, the growth of GaN on foreign substrates has become the research focus in recent years. Some obstacles have hindered the implementation of the hetero-epitaxial GaN technology, such as lattice mismatch and thermal mismatch. The large lattice mismatch between GaN and substrate induces high threading dislocation density in the GaN epi-layer[11], resulting in low electron mobility and leakage path. The most common substrate materials for GaN heteroepitaxy structure are Sapphire, Silicon, and SiC. Table2.2 shows the main material properties of GaN and its substrate.

Table 2.2: The main material properties of GaN and its substrate

Substrate	Bulk GaN	SiC	Sapphire	Si
Lattice Mismatch	–	3.5%	16%	−17%
Thermal Mismatch	–	30%	−25%	55%
K $(W/m \cdot K)$	2.53	3.7	0.42	1.45
Wafer Size	2″	up to 6″	up to 4″	up to 8″
Cost	Extreme High	High	Medium	Low

K, thermal conductivity; The Silicon substrate is the (111)-oriented silicon wafers; The elements of Sapphire substrate is the $\alpha - Al_2O_3$. The cost is calculated in accordance with the combination of GaN epitaxy and substrate.

As we can see in this table, the SiC substrate has a minor lattice mismatch with GaN among these materials. The high thermal conductivity of SiC enables a high-power handling capability of the GaN-on-SiC devices by improving the heat dissipation. However, the expensive SiC wafer limits the broad applications of SiC substrate in GaN devices. Thanks to the invention of low-temperature GaN nucleation layer (NL) growth and p-GaN annealing technology[12, 13], Sapphire substrate is widely applied in GaN-based light-emitting diode (LED) and thus more mature technologies than others. High-quality, low-cost, and large-size Silicon substrates are most promising for commercial GaN devices. Researchers aim to improve the crystal quality of GaN on Si substrate and have achieved some good results recently. These GaN hetero-epitaxial growth technology on the different substrates have their merits. Selecting a substrate often considers the demands of device applications, including input power levels, voltage ratings, frequency band, cost, and

other relevant criteria from target applications.

We summarize the data from pieces of literature of vertical GaN SBDs in Table2.3. In the perspective of vertical GaN SBD, before 2001, most were fabricated on a foreign substrate due to the poor availability of free-standing GaN substrates. Research on vertical GaN-on-GaN SBDs has appeared in the last decade and employed for high-voltage applications(voltage rating >650 V). Moreover, with the appearance of the quasi-vertical devices, Sapphire and Si substrates have been investigated in recent years.

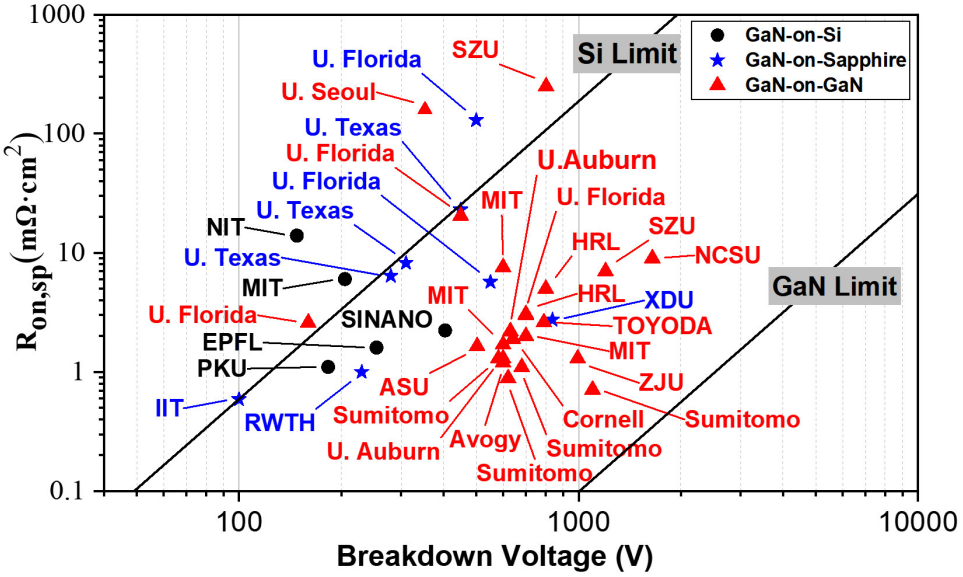

Figure 2.4: Benchmarks of the $R_{on,sp}$ versus breakdown voltage (BV) of vertical SBDs with GaN on Si, sapphire, and GaN substrates.

The GaN epitaxy layer grown on GaN substrate has lower dislocation densities than foreign substrates (e.g., Si, sapphire, or SiC), because of low lattice mismatch and low thermal expansion coefficient mismatch. However, a large number of dislocations in the drift layer can cause leakage when the diode is reverse biased. According to the BFOM of a diode described in the last session, the main objective of designing diodes is to obtain a high BV while keeping the on-resistance as low as possible[2]. To study the impact of the substrate on the performance of vertical GaN SBDs, we benchmark the $R_{ON,sp}$ versus BV of diodes with different substrates in the Figure2.4.

The benchmark shows that the $R_{ON,sp}$ versus BV characteristics of GaN vertical SBD devices are still far from the ideal GaN limit[10]. GaN homoepitaxial has low dislocations and high crystal quality, thus GaN-on-GaN SBD shows much better performance than heteroepitaxial SBD. However, the volume production of vertical GaN-on-GaN SBD has been restricted by the expensive and small scale of mature free-standing GaN substrate[24]. There are few reports on vertical GaN-on-SiC

Table 2.3: Summary of the reported vertical GaN SBDs in the literature.

Year	Substrate	BV V	$R_{ON,sp}$ $m\Omega{\cdot}cm^2$	V_{ON} V	Schottky Metal	Manufacturer	Ref.
1999	Sapphire	450	NA	4.2	Au	CIT	[14]
2000	Sapphire	550	5.7	3.5	NA	U. Florida	[15]
2000	Sapphire	450	23	N.A	Pt/Au	U. Texas	[16]
2000	Sapphire	500	130	3.5	Ni/Pt/Au	U. Florida	[17]
2001	GaN	450	20.5	3	Pt/Au	U. Florida	[18]
2001	GaN	700	3.01	1.8	Pt/Ti/Au	U. Florida	[19]
2002	GaN	160	2.6	1.8	Pt/Ti/Au	U. Florida	[20]
2002	GaN	160	3	1.8	Pt/Ti/Au	U. Florida	[21]
2004	GaN	353	160	NA	Pd/Mo/Ti/Au	Seoul	[22]
2006	GaN	630	2.2	1.2	Pt	U. Auburn	[23]
2007	GaN	580	1.3	1.35	Au	Sumitomo	[24]
2009	GaN	680	1.1	1.2	Au	Sumitomo	[25]
2010	GaN	1100	0.71	1	Ni/Au	Sumitomo	[26]
2010	GaN	600	1.3	0.95	Pt	U. Auburn	[27]
2011	GaN	1650	9	0.5	Pt	NCSU	[28]
2011	Sapphire	1700	NA	NA	Ni	NCSU	[29]
2012	Sapphire	230	1	NA	Ni/Au	RWTH	[30]
2013	GaN	600	1.2	0.9	Pd	Avogy	[31]
2014	Si	205	6	0.5	Ni/Au	MIT	[32]
2014	GaN	620	0.89	1.46	Ni/Au	Sumitomo	[33]
2015	GaN	790	2.25~2.61	0.5	Ni	TOYODA	[34]
2016	GaN	300	NA	NA	Ni/Au	Naval	[35]
2016	GaN	800	4.94	0.77	Ni/Au	HRL	[36]
2016	GaN	700	3.06	0.67	Ni/Au	HRL	[37]
2016	GaN	700	2	0.8	Ni/Au/Ni	MIT	[38]
2017	GaN	NA	0.72	0.73	Ni/Au	MANA	[39]
2017	GaN	610	NA	0.5	Pd/Au	Naval	[40]
2017	GaN	503	1.65	0.59	Pt/Au	ASU	[41]
2017	GaN	1200	7	0.69	TiN	SZU	[42]
2017	GaN	600	7.6	0.7	Ni/Au	MIT	[43]
2017	Sapphire	100	0.59	0.75	Ni/Ti/Pt/Au	IIT	[44]
2017	Si	148	13.9	0.69	Ni/Au	NIT	[45]
2017	GaN	640	1.9	1	Pd	Cornell	[46]
2018	GaN	995	1.3	1.7	Pt/Au	ZJU	[47]
2018	Si	254	1.6	0.76	Ni/Au	EPFL	[48]
2019	GaN	802	250	0.74	Ni/Au	SZU	[49]
2020	Si	183	1.1	0.66	Pt/Au	PKU	[50]
2021	Sapphire	838	2.75	0.5	Ni/Pt	XDU	[51]
2021	Si	405	2.22	0.89	Ni/Au	SINANO	[52]

SBDs because it is not easy to reach a thick GaN epilayer on an expensive SiC substrate[53]. The quasi-vertical GaN SBDs on the sapphire and Si substrate have a low voltage rating below 650V, restricted by the growth of thick GaN film. The latest research result shows a vertical GaN-on-Sapphire SBD with the highest BV of 838V among SBD on foreign substrates, benefiting from the adaption of junction barrier Schottky (JBS) diode structure and a thick GaN drift layer of 9 μm.

2.2.2. Edge termination techniques

In a vertical device, the peak electric field is crowded at the interface between the Schottky contact metal and the n-GaN drift layer, as shown in Figure2.5a, causing early device breakdown at the edge under reverse bias. Thus, novel terminal techniques are needed to improve the vertical device breakdown.

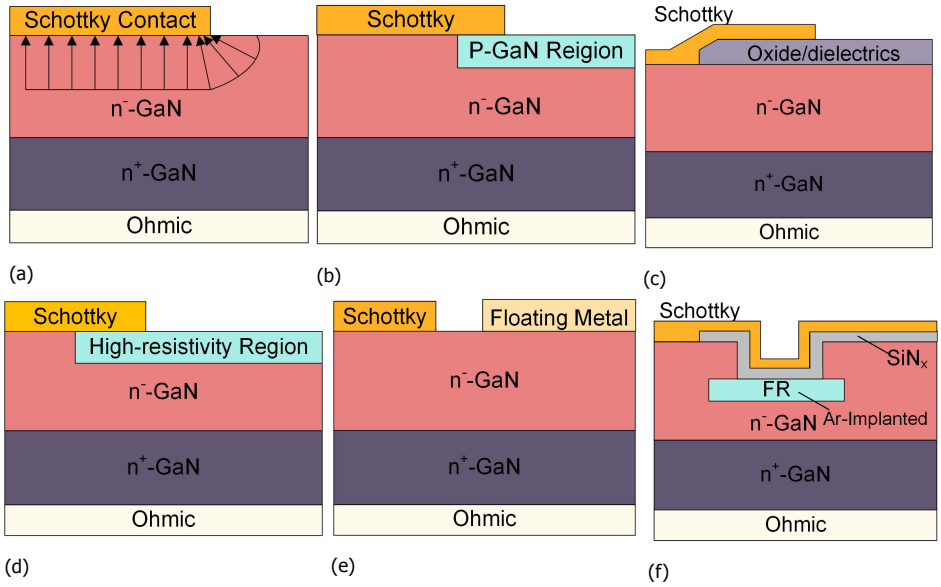

Figure 2.5: (a) Electric field distribution of a typical vertical SBD under reverse bias; (b) Cross-section of GaN SBDs with p-guard ring edge termination structure[23]; Schematic cross-section of a field plate with GaN SBDs: (c) metal field plate[34], (d) resistive field plate[28, 29], and (e) floating field plate[22]; (f) Schematic cross-section of vertical GaN FR-TMBS structure[38].

Edge termination techniques are proposed and utilized to improve the crowded electric field at the periphery of the active region. Figure2.5b-2.5f presents some of the typically used edge terminations of vertical GaN Schottky diodes. The most commonly used termination techniques are discussed in this section, including field rings, junction termination extension (JTE), field plates, trench termination, reduced surface field (RESURF), and N-based termination.

Field Rings

A planar junction termination structure adopting the p-GaN region can provide the redistribution of high electric field at the edge of Schottky contact metal, as shown in Figure2.5b. The p-GaN termination regions are formed by Mg^+ ion implantation under anode edges in the n-GaN drift layer. The superior characteristics are obtained by "moving" the peak electric field at edge away from the surface into bulk with the help of depletion region in PN junction. Furthermore, the peak electric field at the edges can be reduced by extension of PN junction in depletion layer. In early 2002, a research group from the University of Florida reported a vertical GaN-on-GaN SBD structure with p-guard ring junction termination[21]. They found that the BV of a vertical GaN SBD with p-guard ring termination is up to 160 V. However, the p^+-GaN implantation method with high-temperature annealing conditions can increase the significant risk and complexity of the p-guard ring fabrication[54]. Compared with the n-type GaN dopant process (Si implantation, activation temperature of 1250°C), p-GaN dopants require a higher annealing temperature of 1340°C to activate Mg ions[55]. A low activation ratio of Mg^+ for GaN results in low hole concentration, which can affect the GaN crystal quality, causing low mobility and carrier concentration. The poor activation of dopants (Mg^+ atoms) has only produced $10^{15} - 10^{17} cm^{-3}$ orders of magnitude of the carrier concentration. Besides, the extremely high temperatures required to activate the implanted Mg during the annealing process also damage the GaN surface[40]. Greenlee, J.D., et al.[56] reported that the second annealing process followed by multicycle rapid thermal annealing (MRTA) process can compensate for the defects of the GaN surface and improve the crystalline quality of implanted p-GaN.

Field Plates

The field plate is another technique to redistribute the electric field at the edge of the Schottky contact metal under reverse bias. Currently, three types of field plates are used for SBDs, including a metal field plate2.5c, a resistive field plate2.5d, and a floating field plate2.5e. The field plate located at the edge of an electrode can extend the depletion boundary and reduce electric field crowding under the reverse bias. A metal field plate is formed by extending the contact metal over the field oxide/dielectrics at the edge of the junction[34], as shown in Figure2.5c. In 2009, Horii et al.[25] demonstrated improved reverse characteristics in vertical GaN SBDs with a metal field plate (FP) for the first time, achieving 680 V of BV (400 V of BV without FP). Zhang et al.[32, 57] was the first to report a quasi-vertical GaN-on-Si SBD where the destructive BV of the SBD without and with a FP structure is 90 V and 205 V, respectively. Resistive field plate is an alternative field plate technique to smooth the electric field around the surface. This high-resistivity region can help spread the electric field at the edge of the anode metal. As shown in Figure2.5d, Ozbek and Baliga[28, 29] reported two types of GaN SBDs with a resistive field plate formed by Ar ion implantation on GaN and sapphire substrates, respectively. The vertical GaN-on-GaN SBD shows a higher breakdown voltage of 1650 V compared with the diodes without termination (BV of 300 V). Another GaN-on-Sapphire SBD show a BV of 1700 V with a resistive field plate, which is four times higher than that of the conventional SBD. The structure of GaN SBD with floating field plate is

shown in Figure2.5e. When a negative bias is applied to the floating metal plate (or biased field plate) on a n-GaN drift layer it repels electrons away from the device surfaces. This will result in an expansion of the depletion region and then the peak electric field can be reduced around the edges. Thus, vertical SBDs with a biased field plate termination can achieve higher BV than devices without it. However, the introduction of an additional package terminal to provide a separate bias to the biased field plate increases the additional bias circuit cost[58]. Seung-Chul et al.[22] demonstrated that vertical GaN SBDs with a metal floating field plate termination have a higher BV of 353V than conventional structure (159 V).

Trench Termination

Baliga[59] investigated a typical trench metal oxide semiconductor (MOS) barrier Schottky (TMBS) rectifier structure consisting of a MOS structure at the trench region. A trench region containing a MOS structure produces a potential barrier that can shield the Schottky contact at the reverse bias. The potential barrier is against the high electric field in the bulk of the GaN drift region. The reduction of the electric field around Schottky metal enables the reduction of the leakage current under reverse bias. However, it has oxide layer reliability issues due to the high electric field at the corner of the trench. Zhang et al.[38] reported a novel GaN trench metal-insulator-semiconductor (MIS) barrier Schottky diode with trench field rings, as shown in Figure2.5f. They demonstrated that the GaN vertical FR-TMBS has a higher BV (700 V) than conventional SBDs (400 V). The FR regions were formed by Ar ion implantation, which could avoid a peak electric field at the trench corner and premature breakdown in the oxide layer. Zhang et al.[43] also reported a vertical GaN-JBS with Ar-implanted trench termination, achieving a BV of 500–600 V.

Junction Termination Extension (JTE)

The p-type region formed by Mg^{+} implantation can redistribute the surface electric field at the edge of the PN junction. This p-type region has been named JTE[60]. Koehler et al.[40] reported a GaN junction barrier-controlled Schottky (JBS) device with a JTE structure in 2016. Their study shows an improved reverse characteristic in JBS with JTE, achieving a higher BV of 610 V than conventional SBD (BV of 200 V). In the JBS rectifier, the forward current is designed to flow in the undepleted gaps between the P^{+} regions when the diode is forward biased to keep in unipolar operation mode [35]. The pn junction below Schottky metal creates a potential barrier to shield the Schottky contact under reverse bias.

Reduced Surface Field (RESURF)

Planar junction termination is an effective technique to improve breakdown voltage. RESURF is the most popular termination technique in the design of high-voltage power devices. RESURF vertical SBDs can achieve a high BV since the depletion of the Schottky contact in the vertical direction is reinforced by the adjacent PN junction[61, 62]. Li et al.[46] studied the reduced surface field (RESURF) impact on JBS diodes, and reported that the vertical surface field within the trench is much reduced compared to conventional SBD, as shown in Figure2.6.

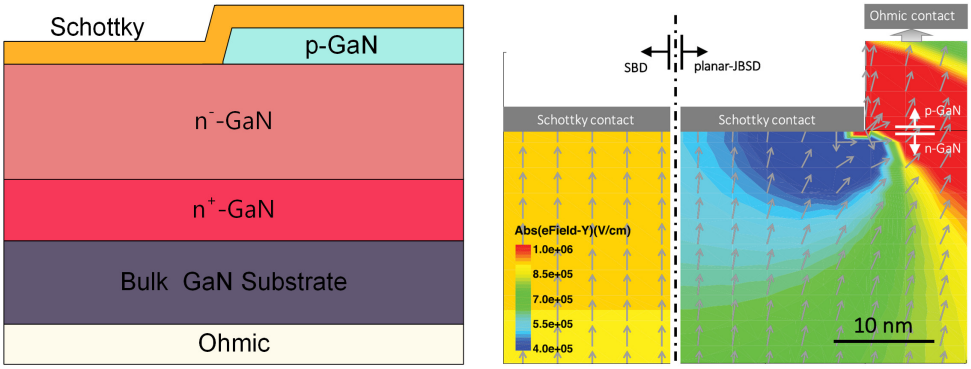

Figure 2.6: Schematic cross-sections of GaN reduced surface field (RESURF) junction barrier-controlled Schottky (JBS) structure and comparison of simulated E-field distribution of typical SBD with RESURF JBS at −200 V[46].

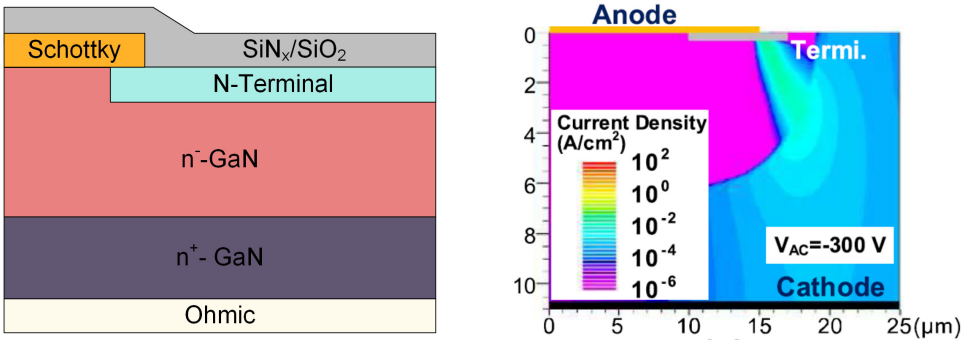

Figure 2.7: Schematic cross-section of the vertical GaN NT-SBD and simulated leakage current distribution of NT-SBD at -300 V[47].

N-Based Termination

N-based termination (NT) technique was reported by Yang et al.[47], as shown in Figure2.7. By utilizing the nitridation plasma to form an N-based termination region around the edge of the anode, the N vacancies can be compensated and the Ga dangling bonds on the GaN surface can also be passivated. The NT structure at the junction edge presents a higher energy barrier height and/or effective barrier thickness around vertical GaN SBDs. Therefore, the leakage current at the edge is decreased under reverse bias due to the suppression of electron transport via thermionic-field emission (TFE) or tunneling. The NT-SBD with a BV of 995 V and a $R_{ON,sp}$ of 1.2 $m\Omega \cdot cm^2$ has shown excellent static (high J_F density of 2000 A/cm^2) and switching characteristics (fast reverse recovery time of 17 ns and small reverse recovery charge of 0.8 nC), which impart potential advantages in high-power and high-frequency applications.

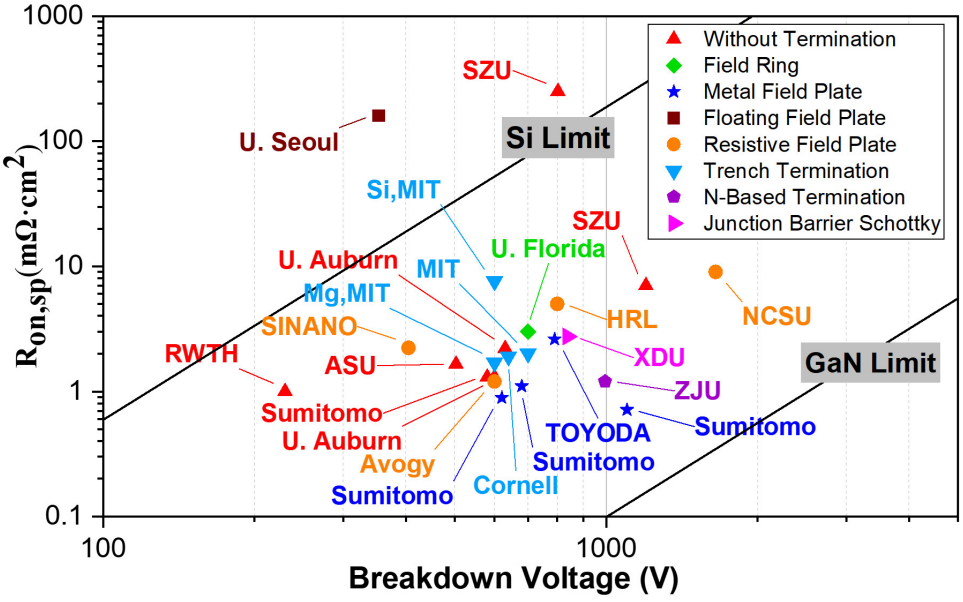

Figure 2.8: Benchmarks of the $R_{ON,sp}$ versus BV of vertical SBDs with different edge termination techniques.

In summary, the benchmark for different edge termination techniques is shown in Figure2.8. A resistive FP termination device with low donor concentration ($N_D = 1 \times 10^{14} cm^{-3}$) has the highest BV (1.6 kV) in this map[28], a TiN-based GaN SBD is followed (1.2 kV) without any termination technique[42]. Utilizing a metal FP termination with low drift layer donor concentration ($N_D = 8 \times 10^{15} cm^{-3}$) can significantly increase the BV (1.1 kV)[26]. Trench termination technique might not evidently improve the BFOM of SBDs, comparing with other techniques, explained by high donor concentration ($N_D = 2 \times 10^{16} cm^{-3}$) in the GaN drift layer[63]. N-based termination structure has a similar reverse breakdown characteristic (BV of

995 V) with metal FP (BV of 1.1 KV) except for high R_{ON}, attributed to a relative thick drift layer (11 μm)[64].

2.3. Summary

This chapter first presented the basic structure of the typical vertical Schottky diode and discussed the basic principles of Schottky diode under both forward and reverse bias. A trade-off between $R_{ON,sp}$ and BV was analyzed to characterize the performance of diodes (Baliga's figure of merit (BFOM)). Then, the equivalent circuit model of a diode for studying the high-frequency properties was introduced. After that, a literature summary for the state-of-the-art vertical GaN SBDs was performed. Finally, the benchmark for vertical GaN SBDs with different substrates (Si, sapphire, and GaN) and various edge terminal techniques were presented and discussed.

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3

Deep and high aspect ratios of GaN trench etching techniques

The optimization of mesa etching for a quasi-vertical GaN SBD by inductively coupled plasma (ICP) etching is comprehensively investigated in this chapter, including the selection of the etching mask, ICP power, radio frequency (RF) power, a ratio of mixed gas, flow rate, and chamber pressure. In particular, the microtrench on the bottom corner of the mesa was eliminated by optimizing etch recipes. Finally, the mesa structure achieved a highly anisotropic profile by combining ICP dry etching and a tetramethylammonium hydroxide (TMAH) wet treatment. In addition, the proposed etching technique was not confined to fabricating a GaN mesa structure for quasi-vertical devices, also extended to other structures, such as hexagonal pyramids and nanowire arrays, promising for sensors, vertical transistors, optoelectronics, and photovoltaics.

Parts of this chapter have been published in Nanomaterials **10**, 657 (2020) [1].

3.1. Common GaN deep etching issues

The growth of GaN epitaxial can be carried out on lower-cost and larger-scale foreign substrates (e.g., silicon, sapphire). Quasi-vertical device structure on foreign substrate is considered a promising candidate for future GaN-based devices.

A mesa structure is formed by etching during the device fabrication process, defining an active region for the quasi-vertical GaN diode. Therefore, exploring a deep and high aspect ratio of trench etching techniques is critical to the fabrication of quasi-vertical GaN devices. First, the etched sidewall of the trench was identified as one of the major leakage current paths[2]. Second, a deep etching trench is essential to reach a high BV of diodes with a thick epitaxial layer. Third, a high aspect ratio of trench allows for reducing the space between electrodes, enabling a reduction of the series resistance.

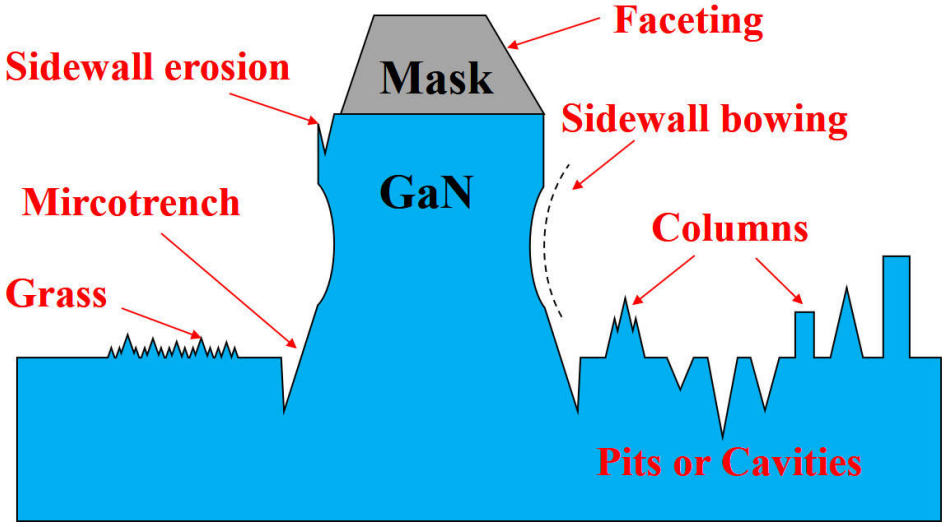
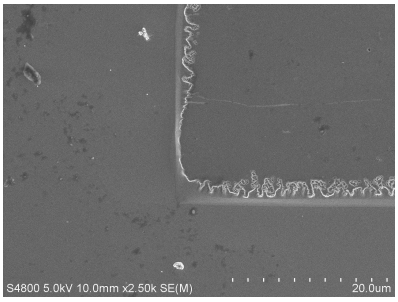
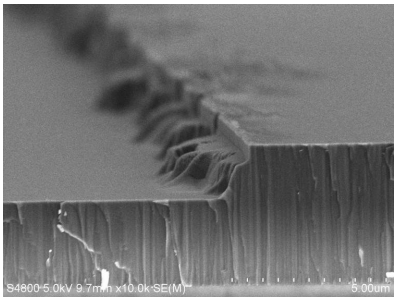


Figure 3.1: Observed issues during deep GaN trench etching

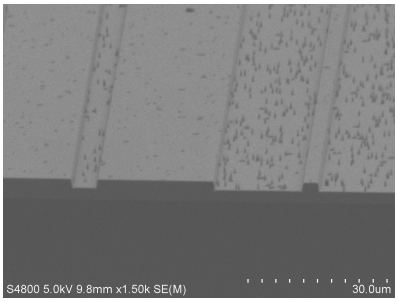
The formation of GaN trench or mesa requires a deep etching technique with a highly anisotropic profile, possibly creating some defects on the sidewall and etched surface. The complicated GaN etching process makes removing these defects difficult. Different from the shallow etching in lateral GaN HMET device, the deep trench etching technology is not mature and needs further development in vertical GaN devices. Figure3.1 summarizes the common issues of GaN trench etching with various defects during the actual fabrication.


S4800 5.0kV 10.0mm x2.50k SE(M)
20.0um

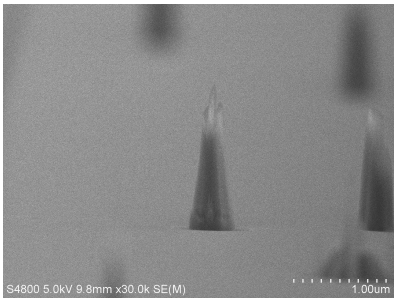
(a)


S4800 5.0kV 9.7mm x10.0k SE(M)
5.00um

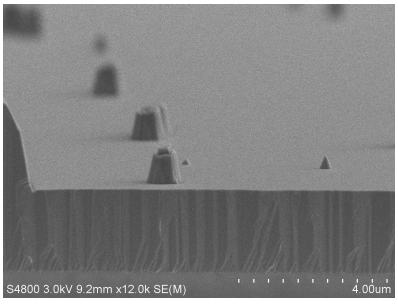
(b)


S4800 5.0kV 9.8mm x1.50k SE(M)
30.0um

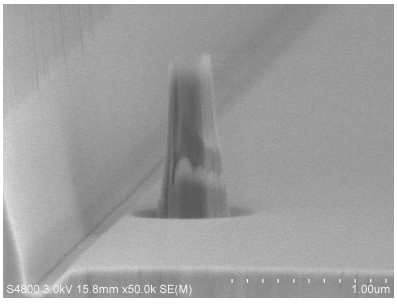
(c)


S4800 5.0kV 9.8mm x30.0k SE(M)
1.00um

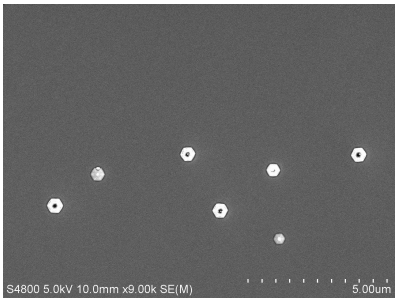
(d)


S4800 3.0kV 9.2mm x12.0k SE(M)
4.00um

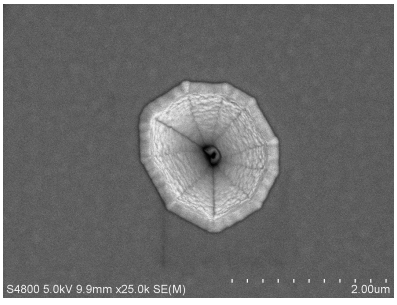
(e)


S4800 3.0kV 15.8mm x50.0k SE(M)
1.00um

(f)


S4800 5.0kV 10.0mm x9.00k SE(M)
5.00um

(g)


S4800 5.0kV 9.9mm x25.0k SE(M)
2.00um

(h)

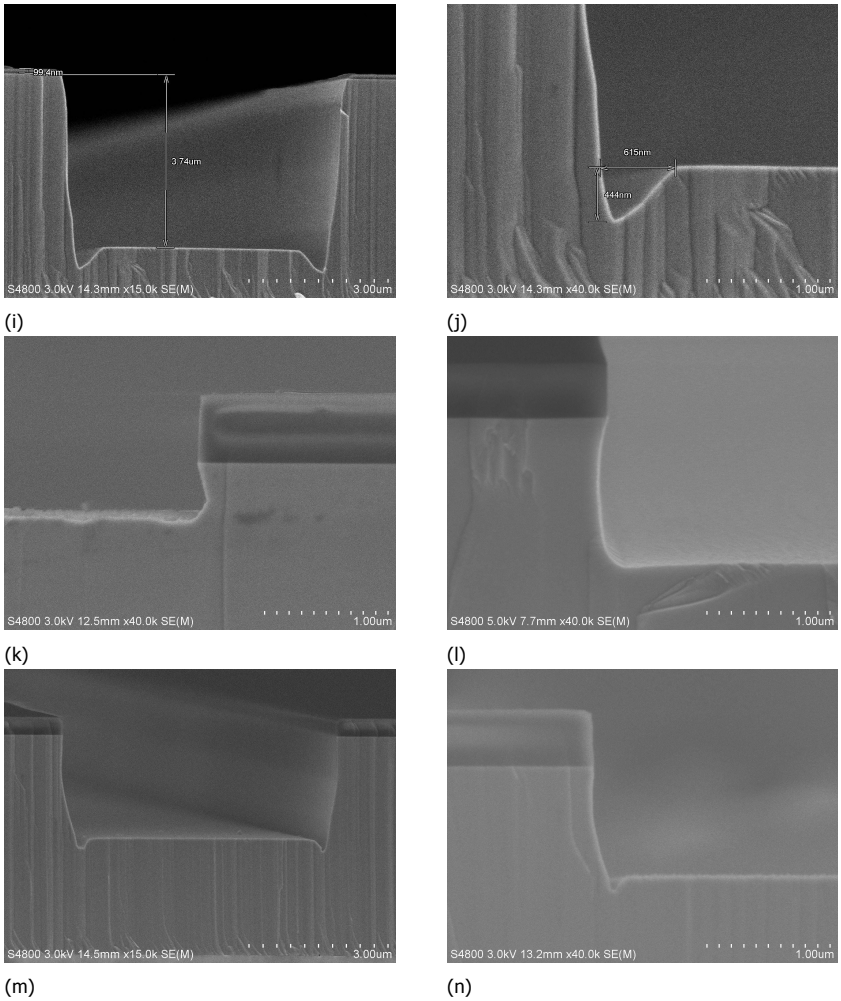


Figure 3.2: SEM photographs of etched GaN trench with different defects: (a) Top view and (b) cross-section of sidewall erosion; (c) and (d) grass on the etching surface; (e) and (f) pillars or columns; (g) and (h) pits or cavities; (i) and (j) micro-trench; (k) and (l) undercut, and (m) and (n) sidewall bowing.

Figure3.2a-3.2m show the scanning electron microscope (SEM) photographs of the etched GaN trench with typical common defects, including sidewall erosion, grass on the etching surface, columns, pits or cavities, micro-trench, undercut, and sidewall bowing. With the development of GaN devices, several of these etching issues have been reported and solved with better solutions.

- The sidewall deterioration is attributed to the physical bombardment of higher energy ions during the ICP dry etching process[3]. A prolonged etch time could destroy the photoresist mask to an erosion morphology that transfers to the mesa sidewall, resulting in a sidewall erosion or deep rifts[4].

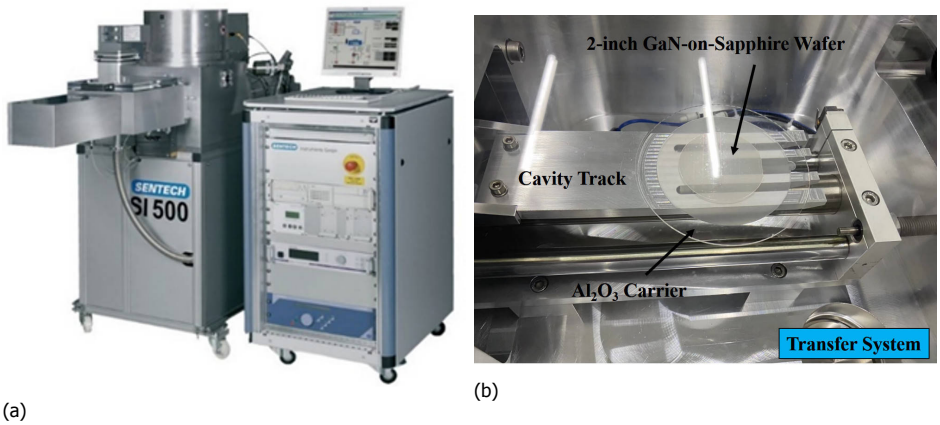
- The etching carrier strongly impacts the morphology of the etching surface. Selecting a suitable carrier substrate could alleviate the needle-like and grass issues due to the element contamination of carrier materials[5].
- A micro-mask can cause the pillars during the etching, related to the residual SiO2 mask material on top of the exposed GaN surface[6]. Ladroue, J., et al. indicated a formation mechanism of the columnar defects that depends on the impurities in the etching chamber[7].
- The etching conditions strongly influence the density of hexagonal pits with high ICP power, low RF power, and high chamber pressure etching conditions, which can help reduce surface etching damage[8].

Although most efforts have been made on GaN etching, some of the critical issues have not been solved yet. Micro-trench at the corner of etched mesa is the most critical defect in those unsolved issues, resulting in a significant leakage current and hiding an enormous risk for the reliability of high-power GaN diodes. A few works on SiC or Si etching provide some thoughts for eliminating GaN micro-trench. However, due to the diversity of etching reaction mechanisms among semiconductors, it is challenging to solve the micro-trench problem in GaN mesa etching effectively.

3.2. Experimental characterization of GaN etching

3.2.1. Method and equipment

The n-GaN sample has an epitaxial layer thickness of 4 μm, growing on 2-inch c-plane (0001) Sapphire substrates by metalorganic chemical vapor deposition. The inductively coupled plasma (ICP) dry etch tools and transfer system are shown in Figure3.3a and 3.3b .



(a) (b)

Figure 3.3: (a)Inductively coupled plasma (ICP) dry etch tools and (b) wafer transfer systems

The ICP source can produce high ion densities and high radical densities plasma by increasing the ICP power. The RF plasma source can control the ion energy by

adjusting RF power or DC bias at the bottom electrode. The exhaust system enables the gas flow rate and pressure adjustment in various process windows. The wafer carrier keeps a constant temperature of 25-30°C by a bottom cooling system with a helium backing flow. An ICP tool allows for the separate control of ICP and RF plasma sources, enabling the independent adjustment of plasma density and ion energy etching process. The ready samples could rapidly transfer into chambers with full vacuum, preventing contaminations from the load-lock area to the reaction chambers.

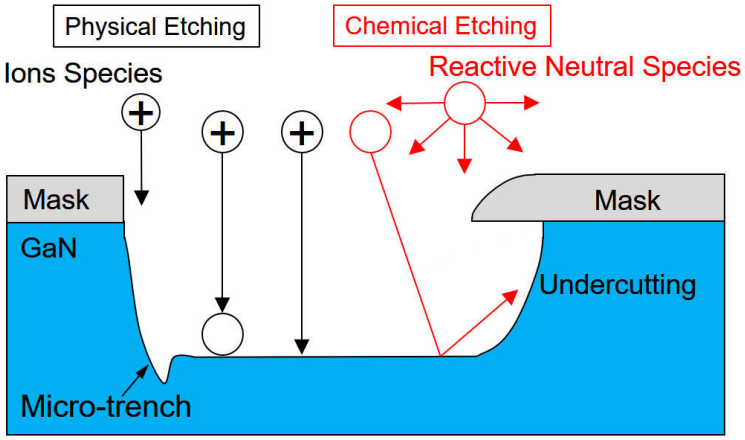


Figure 3.4: Basic schematic diagram of the major reactions during the ICP etching process

Figure3.4 shows the basic schematic diagram of the major reactions during the ICP etching process. Physical bombardment and chemical reactions are the two major reaction procedures. The ion bombardment dominates the physical etching and aims to form an anisotropic etching profile. The increase of the RF power can enhance the ion bombardment by accelerating the ion under the electric field along the normal direction to the sample surface. The yield of chemical reactions primarily depends on the radical density or neutral ion species generated by the ICP power source. Chemical etching can increase the dry etch rate by strengthening the chemical reactive rate, which improves the etch selectivity between the mask and the etched sample. Halogen-based gas is a typical etching reactant for GaN-based materials. The primary chemical reaction of GaN with Chlorin-based species is given by:

$$GaN + 3Cl^* \rightarrow GaCl_3 \uparrow + 1/2N_2 \uparrow \tag{3.1}$$

In this experiment, the ICP power, RF power, pressure, and ratio of mixed etching gas were tailored by the design of etching experiments. Both photoresist (PR) and silicon dioxide (SiO_2) hard masks were employed for ICP mesa etching in this work.

3.2.2. Flow of soft mask (photoresist)

The process flow of mesa etching with the PR mask is illustrated in Figure3.5. A thickness of 7 µm positive photoresist (AZ4620) was coated, exposed, and developed for patterning, followed by hard baking (post develop baking) in the oven. Finally, a mesa was formed after chlorine-based ICP dry etching.

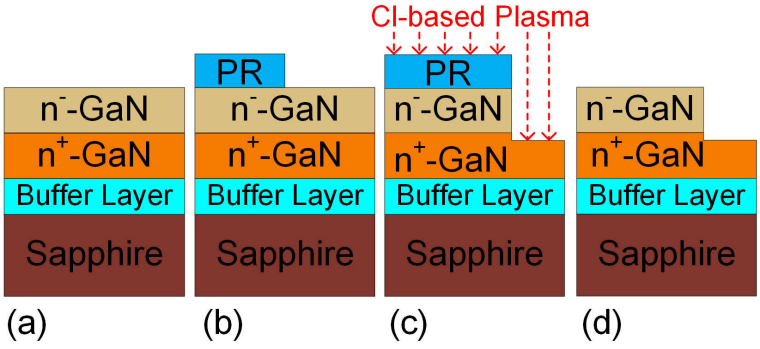


Figure 3.5: Fabrication steps of mesa etch with photoresist (PR) as a mask. (a) Epitaxial structure of the GaN sample; (b) PR mask on GaN; (c) Chlorine-based mesa etching; (d) Stripping of the PR.

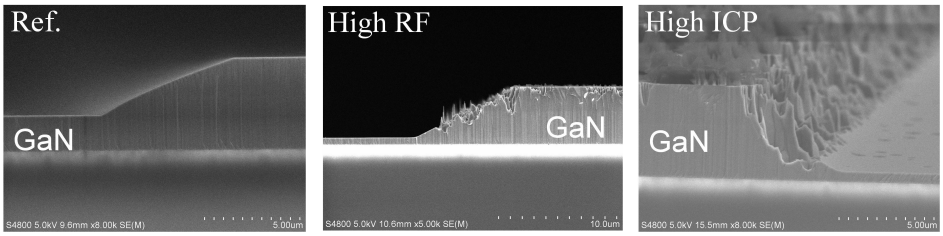
Cl_2 was used as a primary etching gas for the PR-masked etch samples[9]. To investigate the impact of ICP and RF power on the etched sidewall profile, the chamber pressure, flow rate of Cl_2, and etch time were kept identical. The detailed etching parameters and etch rate results are listed in Table3.1.

The etch rate of GaN was observed to increase from 120 nm/min to 550 nm/min when the ICP power varied from 360 W to 540 W. This increased etch rate is mainly attributed to the highly reactive chlorine ion (chemical component) density increasing under high ICP power[10]. In addition, the etch rate of GaN was observed to be positively proportional to the RF power, as well. The etch rate increased from 120 nm/min at 63 W to 537 nm/min at 210 W. The increased RF power enhances the physical sputtering of GaN etching by heavy radicals; then, the enhanced physical bombardment helps to break the Ga-N bonds, speeding up the chemical etching process[11, 12]. Figure3.6 show the cross SEM photomicrographs of GaN mesa sidewalls etched with a PR mask under various Cl_2 plasma conditions.

Table 3.1: Result of PR-masked GaN samples under different etching conditions.

Sample	ICP power (W)	RF power (W)	Pressure (Pa)	Cl_2 (sccm)	GaN etch rate nm/min	θ_{GaN}
Reference	360	63	1.5	130	120	25.0°
High RF	360	210	1.5	130	537	-
High ICP	540	63	1.5	130	550	-

θ_{GaN} is the etched GaN sidewall angle. RF power is the radio frequency power. ICP power is the inductively coupled plasma power.

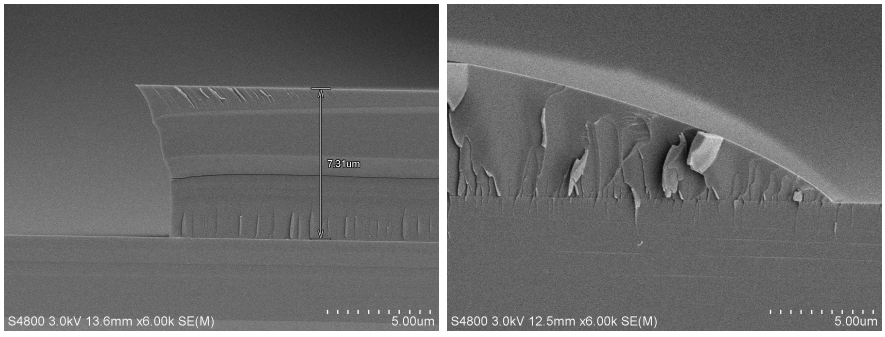


(a) (b) (c)

Figure 3.6: Cross SEM photomicrographs of GaN mesa sidewalls etched with a PR mask under Cl_2 plasma conditions with 1.5 Pa pressure and 130 sccm flow rate. (a) Reference sample. (b) High-RF-power etched sample. (c) High-ICP-power etched sample.

As shown in Figure3.6a, the reference sample was observed to have a smooth sidewall profile. However, numerous pillars emerged on the sidewall for samples with high RF and those with high ICP power, as shown in Figure3.6b-3.6c. Rawal et al. also reported similar observations that mesa edges were damaged by chlorine ions caused by BCl_3/Cl_2 discharge during ICP etching[10]. This is due to the photoresist mask erosion caused by enhanced physical bombardment and chemical components. The distorted pattern is then transferred to the GaN, resulting in deteriorated mesa sidewall morphology[3].

A high-temperature hard baking (post develop baking) prior to the ICP etch can help to eliminate the PR burning/erosion issues[1]. Figure3.7 compares the cross-section of PR profile under different baking temperatures. A slope sidewall profile is observed in the 100 ℃ baked sample because of the PR flow during the baking process.



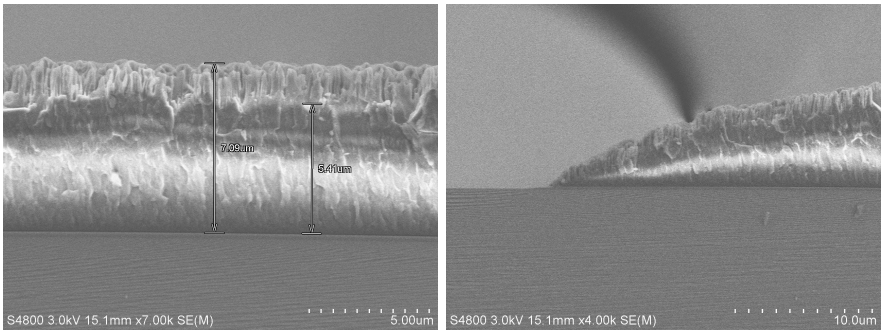
(a) (b)

Figure 3.7: Cross SEM sidewall profiles of photoresist (AZ4620)-masked Si samples (as a reference) with (a) without baking and (b) with 100 ℃ baking.

After that, those samples were etched with a certain amount of Cl_2 within ICP

[1]Reflow of Photoresist. Available online: https://www.microchemicals.com/micro/tds_az_p4000_series.pdf (accessed on 1 February 2022).

tools. A significant deterioration on the etched PR mask is found for both samples, as shown in Figure3.8. The high-temperature baked sample has a slightly better profile than the sample without baken, indicating the necessity of the post-baking process during PR mask etching. We conducted the consequent experiment with a higher baking temperature to further support this point.



(a) (b)

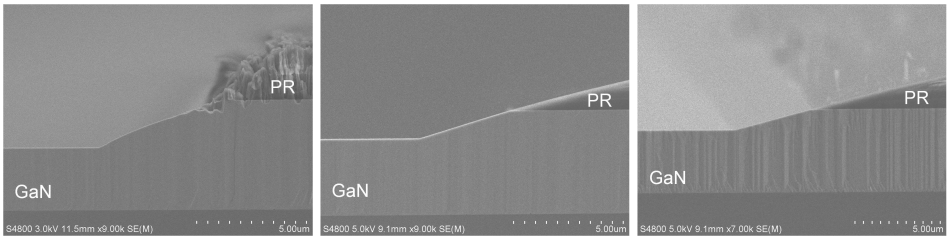
Figure 3.8: Cross SEM sidewall profiles of photoresist (AZ4620)-masked Si samples (as a reference) after etching (a) without baking and (b) with 100 ℃ baking.

Table 3.2: Etched results with different hard baking temperatures.

Sample	ICP power (W)	RF power (W)	Pressure (Pa)	Cl_2 (sccm)	GaN etch rate (nm/min)	θ_{GaN}	T (℃)
1	360	63	1.5	130	135	23.0°	100
2	360	63	1.5	130	123	17.0°	150
3	360	63	1.5	130	117	15.0°	180

θ_{GaN} is the etched GaN sidewall angle. T is the photoresist hard baking temperature.

The detailed conditions and results are listed in Table3.2. The baking temperature was varied from 100 ℃ to 180 ℃, followed by ICP etch under ICP power of 360 W, RF power of 63 W, pressure of 1.5 Pa, and Cl_2 flow rate of 130 sccm.



(a) (b) (c)

Figure 3.9: Cross SEM sidewall profiles of photoresist (AZ4620)-masked GaN samples after etching with different hard baking temperatures. (a) 100 ℃; (b) 150 ℃; (c) 180 ℃.

As shown in Figure3.9a-3.9c, the slope of the mesa sidewall decreased with increasing PR baking temperature, which is due to edge bulge formation at the

photoresist pattern as the baking temperature increased, resulting in photoresist sidewall profile transformation and pattern transfer onto the GaN[13, 14] Although baking at a high temperature can help to obtain a smooth mesa sidewall, there are a few drawbacks when the baking temperature applied is above the glass transition temperature (120℃ - 130 ℃) of the photoresist, such as significant oblique sidewall profile formation, hard striping[15], and volume loss of PR[16].

3.2.3. Flow of hard mask (silicon dioxide)

Although a smooth mesa sidewall was obtained with the PR mask, a steep sidewall is necessary to reduce the series resistance of a quasi-vertical SBD. A hard mask is more suitable for deep etching of GaN devices, because the etch selectivity of GaN/hard mask is relatively high[17]. To achieve a steep mesa sidewall, we used SiO_2 as the hard mask and selected AZ5214 as the mask of SiO_2 in all of the following experiments. The process flow of mesa etch with the SiO_2 hard mask is depicted in Figure3.10.

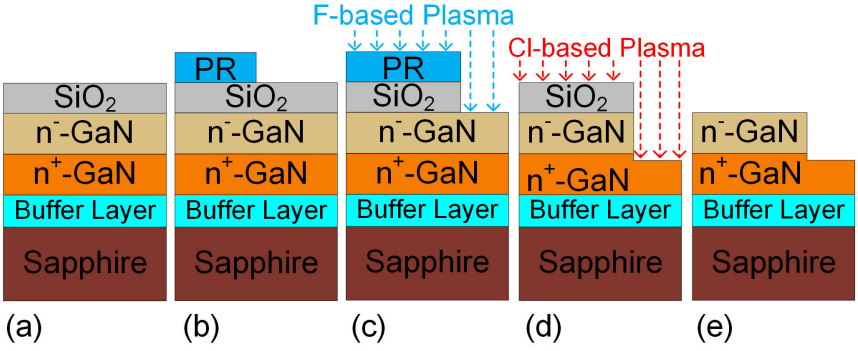


Figure 3.10: Fabrication steps of the SiO_2-masked GaN mesa etch; (a) SiO_2 hard mask deposition on the GaN sample; (b) PR mask on SiO_2; (c) Hard mask etching by fluorine-based plasma; (d) Chlorine-based mesa etching; (e) Stripping of the SiO_2 hard mask.

A 550 nm SiO_2 mask layer was firstly deposited by plasma-enhanced chemical vapor deposition (PECVD), followed by 1 μm reversal photoresist (AZ5214E) coating, exposure, and development. The SiO_2 hard mask was then opened by fluorine-based ICP etch. After the pattern was transferred from the SiO_2 into the GaN layer and the mesa structure was formed by chlorine-based ICP etch, the SiO_2 mask was stripped using a buffer of Etchant (BOE) solution. The AZ5214 reversal photoresist is a unique photoresist intended for lift-off techniques that call for a negative wall profile. A certain baking temperature is crucial for reaching a tapered sidewall due to the PR flow during the baking process. Figure3.11 list the PR (AZ5214E) profile at various baking temperatures.

After the post-baking process with a 120 ℃ baking temperature and 60s baking time, a steep PR (AZ5214E) profile was observed on the top of SiO_2 film. The SiO_2 hard mask was then opened by fluorine-based ICP etch. Figure3.12 shows the SiO_2 mask profile as a function of etching time. An anisotropic etching profile of SiO_2

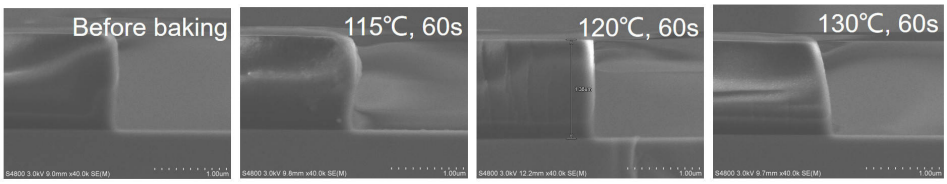


Figure 3.11: Evolution of PR (AZ5214E) profile at various baking temperatures.

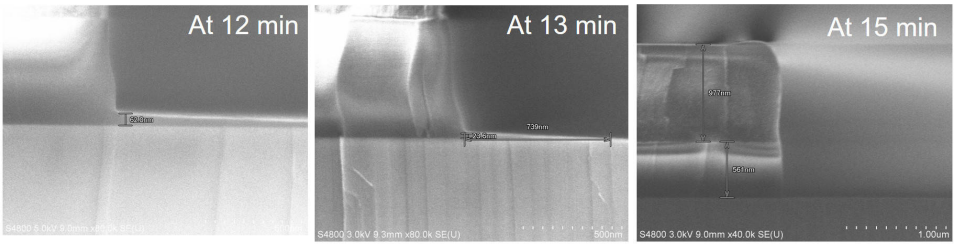


Figure 3.12: SEM images of sidewall profiles of PR-masked SiO_2 on top of the GaN with different etch times: (a) 12 min; (b) 13 min; (c) 15 min;

mask without any residuals has been observed with precise time control and paves the way to the followed GaN mesa etching steps. Consequently, the optimized process and results were repeated on the 2-inch GaN wafer on the Sapphire substrate. Figure3.13a shows a cross-section of photoresist (AZ5214E) after development for the mesa pattern. After fluorine-based ICP etching of the SiO_2 hard mask, Figure3.13b and 3.13c show a cross-section of the SiO_2 hard mask with PR on top and without PR after lift-off process, respectively.

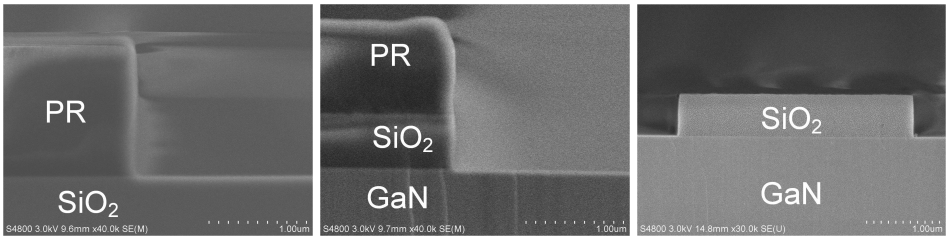


Figure 3.13: Cross SEM images of the sidewall of (a) photoresist (AZ5214E) and of (b) SiO_2 hard mask with PR on top and (c) without PR.

3.3. The influence of etching parameters on micro-trench issues

3.3.1. Effect of etch time, ICP power and RF power

The impact of etch time on the mesa sidewall profile, etching rates, and etch selectivity was also investigated, while keeping the ICP power, RF power, pressure, and flow rate of Cl_2 at 360 W, 63 W, 1.5 Pa, and 130 sccm, respectively. The cross sections of sidewalls with varying etch times are shown in Figure3.14. With increasing etching time, a micro-trench emerged at the bottom corner of the mesa sidewall, as shown in Figure3.14b and 3.14c. In addition, a slight bowing problem was observed at the mesa sidewall after 7 min of etching. The bowing phenomenon is related to various factors, e.g., non-directional incident ions and isotropic spontaneous chemical etching[18].

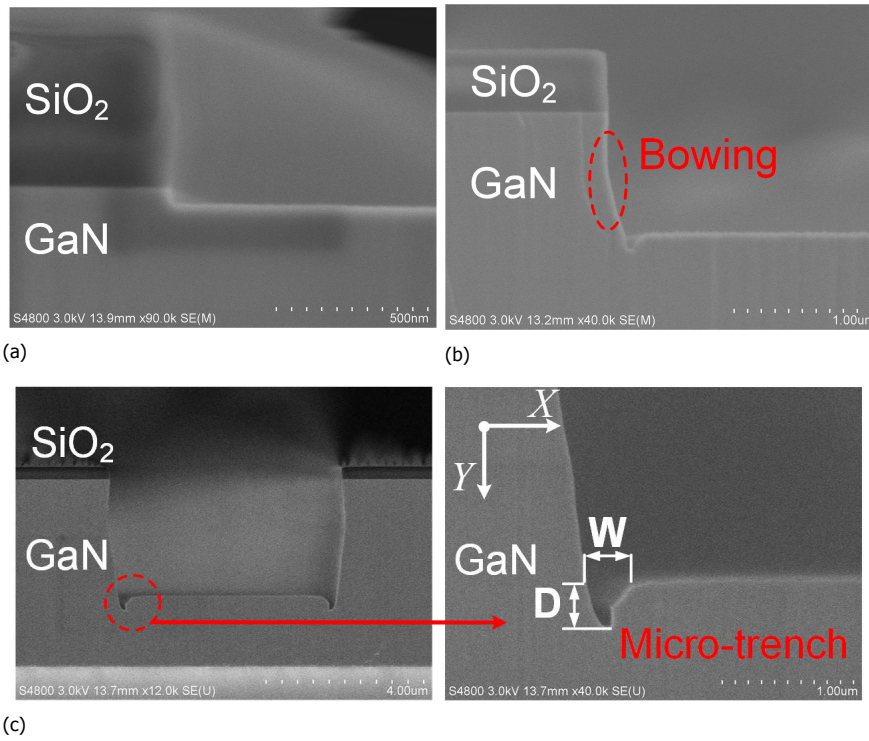


Figure 3.14: SEM images of sidewall profiles of SiO_2-masked GaN with different etch times: (a) 30 s; (b) 7 min; (c) 20 min. The marked corner was chosen to show the details of the microtrench. The inset on the right of (c) is the SEM image of the microtrench at the bottom corner of the mesa. D and W are the depth and width of the microtrench, respectively.

Figure3.15a shows the GaN etch rates and etch selectivity of GaN/SiO_2 with etch time. Both etch rate and selectivity have a weak dependency on etch time, with values of about 120 nm/min and 9.8 nm/min, respectively. As shown in Figure3.15b, the depth and width of the microtrench increased with increasing etching time. The

etch rate of the microtrench along the Y direction slightly increased with etch time, and the etch rate along the X direction showed nearly no change. A number of ions were incident along the bowing sidewall and then focused on the bottom corner of the sidewall, leading to an increased etch rate in the Y direction of the microtrench after a long etching time[18, 19].

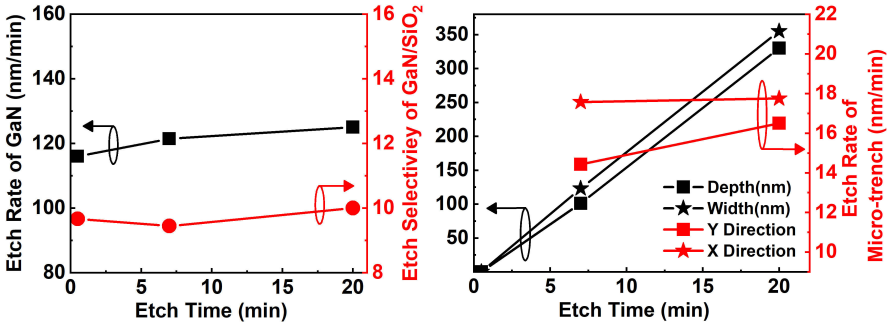
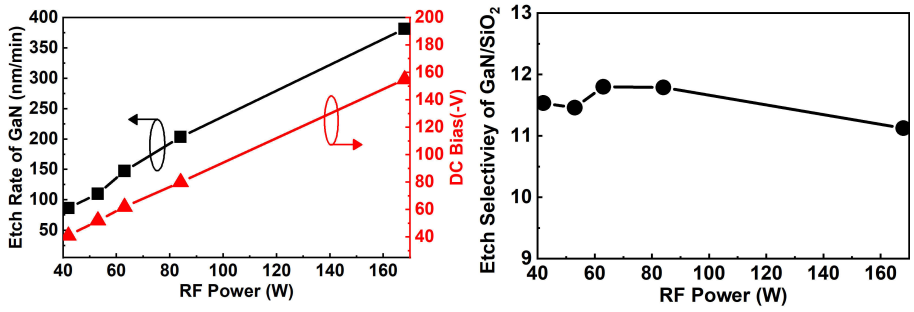


Figure 3.15: (a) Etch rate of GaN and etch selectivity of GaN over SiO_2 as a function of etching time. (b) The effect of etch time on the depth and width of the microtrench, and the etch rates of the microtrench in the X and Y directions.

As seen in Figure3.16a, the etch rate of GaN is a strong function of RF power and increased from 86 nm/min to 380 nm/min when RF power increased from 42 W to 168 W at 1.5 Pa pressure, 360 W ICP power, and a Cl_2 flow rate of 130 sccm. With increased RF power from 42 W to 168 W, the DC bias increased from -40V to -155V. The increased DC bias increases the energy of ions and enhances the physical etching components, which can further increase the chemical etching component[10, 20]. Figure3.16b shows that the etch selectivity of GaN over SiO_2 was reduced slightly as RF power increased. As shown in Figure3.16c, the etch rate of the micro-trench in either the X or Y direction increased with increasing RF power due to the strong physical bombardment[5]. With a low RF power of 63 W, the micro-trench could be reduced. However, it deteriorated when the RF power increased to 168 W, as shown in the inset.

As shown in Figure3.17a, the etch rate of GaN increased monotonically with increasing ICP power under etch conditions of 42 W RF power, 130 sccm Cl_2 flow rate, and 1.5 Pa pressure. The etch rate increased from 84 nm/min to 180 nm/min when the ICP power increased from 360 W to 540 W. The increase in the GaN etch rate is attributed to enhanced chemical etching by increased Cl ion flux density[21]. The observation that the DC bias increases with increasing ICP power is mainly due to the ICP tool operating in capacitive coupling mode (called E mode[22]). When the tool is operated in this mode, ion density is low at low ICP power[23]. Cooke et al.[24], Zhou et al.[21], and Qiu et al.[8] reported similar dependences of DC bias on ICP power. Figure3.17b shows that the selectivity increased slightly as ICP power increased. As shown in Figure3.17c, the etch rates of the micro-trench increased from 3 nm/min to 5 nm/min in the Y direction and from 9 nm/min to 13 nm/min in the X direction when the ICP power increased from 360 W to 450 W. Then, the etch



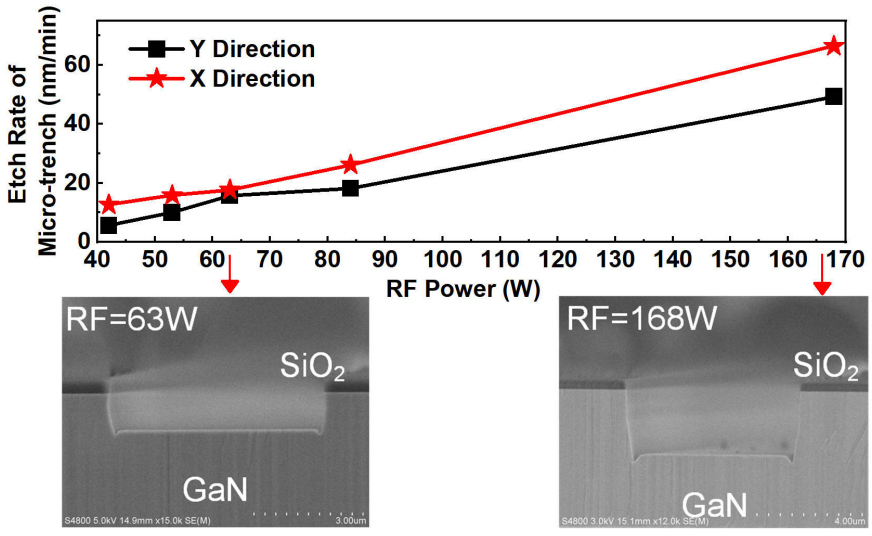


Figure 3.16: (a) Etch rate of GaN and DC bias as a function of RF power. (b) Etch selectivity of GaN over SiO_2 as a function of RF power. (c) The effect of RF power on etch rates of the microtrench in the X and Y directions. The insets of (c) show cross SEM images of samples etched with 63W and 168W RF power.

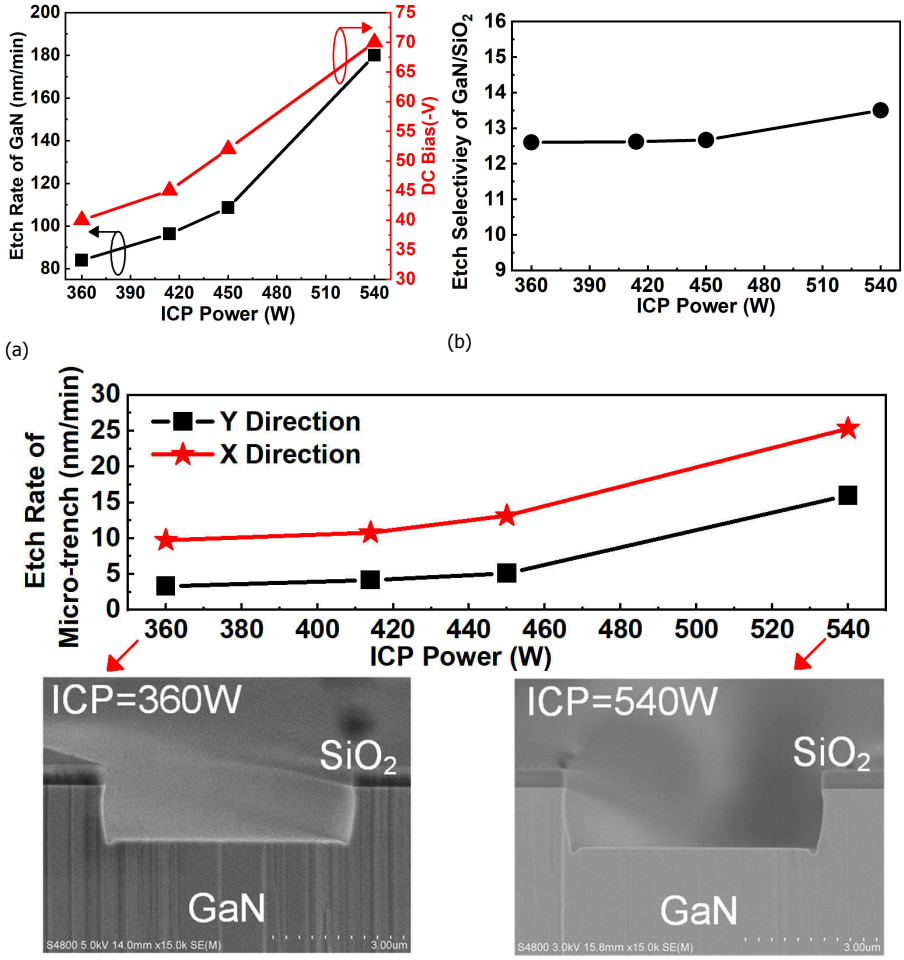


Figure 3.17: (a) Etch rate of GaN and DC bias as a function of ICP power. (b) Etch selectivity of GaN over SiO_2 as a function of ICP power. (c) The effect of ICP power on the etch rates of the microtrench in the X and Y directions. The insets of (c) show cross SEM images for samples etched with 360 W and 540 W ICP power.

rates rocketed to 16 nm/min in the Y direction and 25 nm/min in the X direction at 540 W ICP power. The reason for this is that the sidewall profile becomes bowed at high ICP power when Cl_2 is used as the etch gas, then the bowed sidewall profile leads to the accumulation of ions at the corner of the mesa bottom, causing an increase in the microtrench etch rate[25].

3.3.2. Role of BCl_3 concentration on GaN etching profile

BCl_3 as an additive in the etching gas can increase the etch rate of GaN[26]. Thus, in order to improve the etch rate of GaN and investigate the mesa sidewall profile, the percentage of BCl_3 in the Cl_2/BCl_3 gas mixture was varied from 0% to 39% with fixed ICP power of 540 W, RF power of 168 W, total gas flow of 130 sccm, and pressure of 1.5 Pa. Figure3.18a shows that the etch rate of GaN increased with increasing BCl_3 concentration in the Cl_2/BCl_3 gas mixture up to 9% BCl_3, where the maximum etch rate was reached, then decreased from 415 nm/min to 231 nm/min as the BCl_3 concentration further increased, similar to other reports[27, 28]. When the BCl_3 concentration was below 10% the Cl radicals and Cl^+ positive ions showed increasing tendency in the reaction chamber as the BCl_3 concentration increased[26], intensifying the ion bombardment and chemical etching process, resulting in the increase of the GaN etch rate. However, the Cl and Cl^+ ion density decreased with increasing BCl_3 concentration when the concentration was above 10% resulting in a reduction of the etch rates of GaN and DC bias[29]. The etch selectivity of GaN over SiO_2 was significantly reduced from 10.5 to 4 as the BCl_3 concentration increased (as shown in Figure3.18b. This is attributed to the positive BCl^{2+} ion density increasing as the BCl_3 concentration increases, leading to an increase in the SiO_2 mask etch rate by the formation of BCl_xO_y in the SiO_2[30, 31]. As shown in Figure3.18c, the etch rates of the micro-trench slightly increased with the BCl_3 concentration up to 9% then decreased further at 33% BCl_3 and finally vanished at 39% in both the X and Y directions. A significant reduction in the micro-trench can be observed in the inset SEM image in Figure3.18c as the BCl_3 concentration increases. The reduction of the micro-trench phenomenon is related to the sloped sidewall. With such a sloped sidewall, most ions can be reflected to a position away from the bottom corner of the mesa[32]; thus, less physical bombardment accumulates in the bottom corner of the mesa. The sloped sidewall profile might be attributed to the reduction of etch selectivity of GaN over SiO_2 in the case of highly anisotropic etch[33]. In addition, pillars were observed in the bottom of the mesa, caused by the spontaneous oxidation of dislocations, inhibiting Cl-based dry etch[7]. In this study, flow rates of 9% BCl_3 concentration were considered a good trade-off in terms of several aspects, such as etch rate, steepness of the sidewall, pillar phenomenon, and micro-trench effect.

Figure3.19a shows the impact of chamber pressure on the etching rate of GaN and DC bias. The ICP power, RF power, and flow rates of Cl_2/BCl_3 were set at constant values of 540 W, 168 W, and 118 sccm/12 sccm (Cl_2/9% BCl_3), respectively. The etch rate of GaN slightly increased from 416 nm/min to 440 nm/min with pressure up to 1.5 Pa, and DC bias was decreased as the pressure increased, reaching a minimum value of -115 V at 1.5 Pa. When pressure increases, the mean

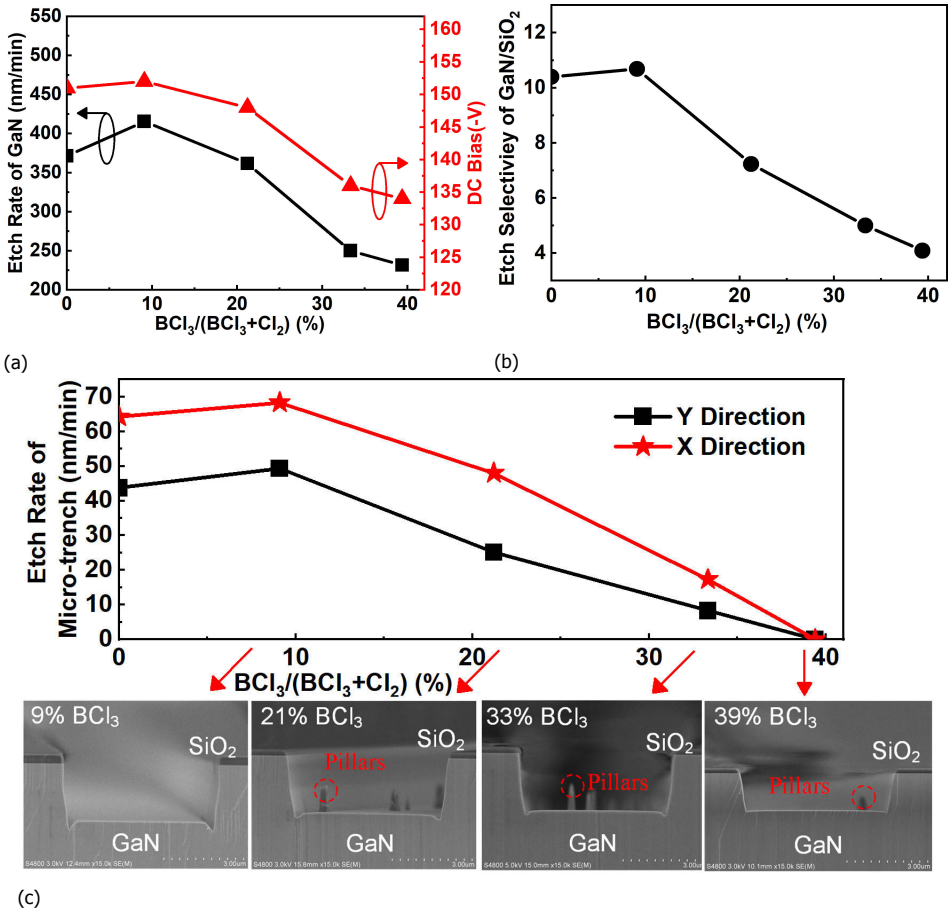


Figure 3.18: (a) Etch rate of GaN and DC bias as a function of BCl_3 content in the Cl_2/BCl_3 gas mixture. (b) Etch selectivity of GaN over SiO_2 as a function of BCl_3 content in the Cl_2/BCl_3 gas mixture. (c) The effect of BCl_3 content in the Cl_2/BCl_3 gas mixture on etch rates of the micro-trench in the X and Y directions. The insets of (c) show cross SEM images for samples etched with different BCl_3 concentrations.

free path of reactive radicals is reduced, followed by an increase of inter-atom collision ionization[5, 21]. Therefore, the etch rate of GaN increased with increasing ion flux and the DC bias decreased as the RF power was kept at a constant value[24]. As shown in Figure3.19b, the etch selectivity of GaN/SiO_2 increased monotonically as the chamber pressure increased, similar to findings by Wang et al.[34]. Figure3.19c shows that etch rates of the microtrench along both the X and Y directions decreased with increased pressure. The etch rate in the X direction has higher dependency on chamber pressure than that in the Y direction, which is attributed to the irregular distribution of incoming ion angles[32]. Therefore, high chamber pressure is preferred to obtain high etch selectivity.

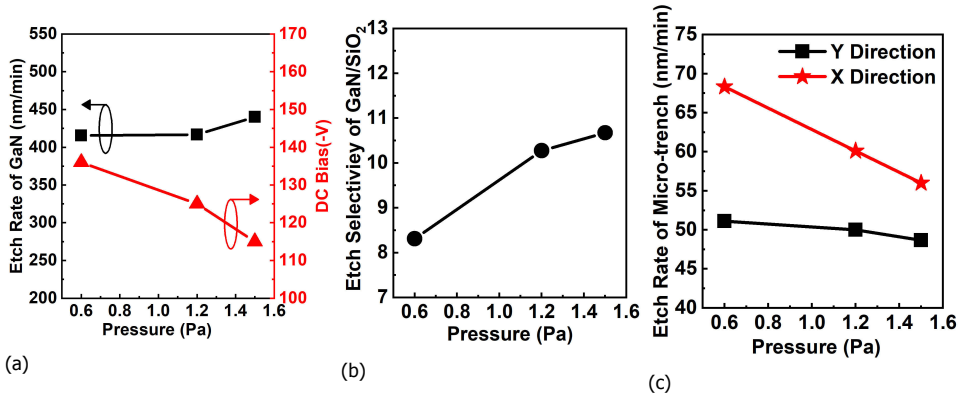


Figure 3.19: (a) Etch rate of GaN and DC bias as a function of pressure. (b) Etch selectivity of GaN over SiO_2 as a function of pressure. (c) The effect of pressure on etch rates of the micro-trench in the X and Y directions.

3.3.3. TMAH wet treatment

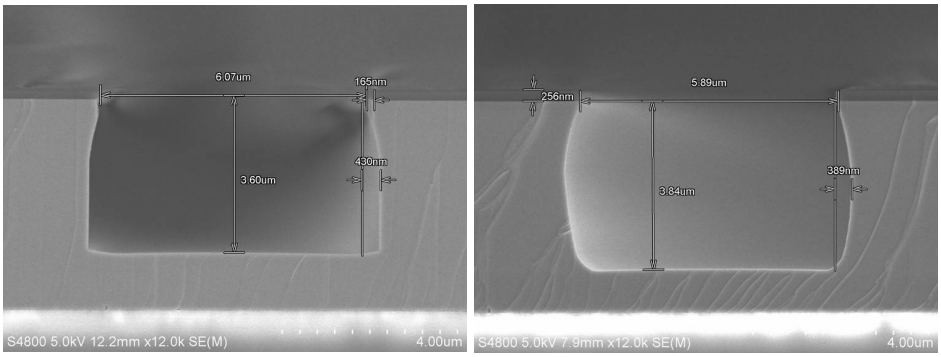
The wet treatment is typically an anisotropic etching process in silicon manufacture and is also found in the GaN etching process[35, 36]. It is reported that wet treatment helps improve the etching morphology of GaN trench or mesa. Both tetramethyl ammonium hydroxide (TMAH) and potassium hydroxide (KOH) is as known as wet treatment electrolytes used in the GaN etching process[37, 38]. In the LED products industry, KOH is an effective and low-cost solution for producing a textured sidewall to improve light extraction efficiency.

TMAH etching solutions are proposed to provide more chemically stable reactions with GaN during the etching process. Kim, K., et al.[39] demonstrated that TMAH treatment solutions enhance the electron mobility in the channel of GaN HEMT because the improvement of surface morphology leads to a reduction of electron scattering at the interface of Al_2O_3/GaN. In 2016, Im, K.-S., et al.[40] reported that the TMAH wet etching along the <1101> crystal orientation of GaN is fast, leading to a transition to vertical (1120) plane in a short time, thus forming a steep trench sidewall. In this experiment, we employed the TMAH solutions treatment to remove the surface or sidewall damage formed after ICP dry etching.

This experiment is carried out on a hot plate using the glass beaker with a bottle of TMAH solutions in the cleanroom, as shown in the figure3.20.

(a) (b) (c) (d)

Figure 3.20: (a) A bottle of TMAH solutions, (b) hot plate, (c) an example of the specimens immersing in TMAH Solutions, and (d) experimental samples under test.



(a) (b)

Figure 3.21: Cross-section SEM images for samples etched (a) with and (b) without TMAH etching.

Figure3.21 shows the etching morphology of GaN mesa with and without TMAH etching. It is observed that the sloped sidewall features a steep and perfect anisotropic profile after a TMAH treatment at 45℃ for 30 minutes. With the increase of dipping temperature from 45 ℃ to 75 ℃, the mesa sidewall shows a trigonal prism morphology with roughness surface (Figure3.22b), due to the fast etch rate in a higher temperature. Unfortunately, the lateral etching of TMAH wet treatment causes the reduction of characteristic dimensions in device area and limits the widespread use in small-size device fabrication. Therefore, the TMAH wet etch solutions are more suitable for high-voltage vertical GaN devices with a large area and thick drift region.

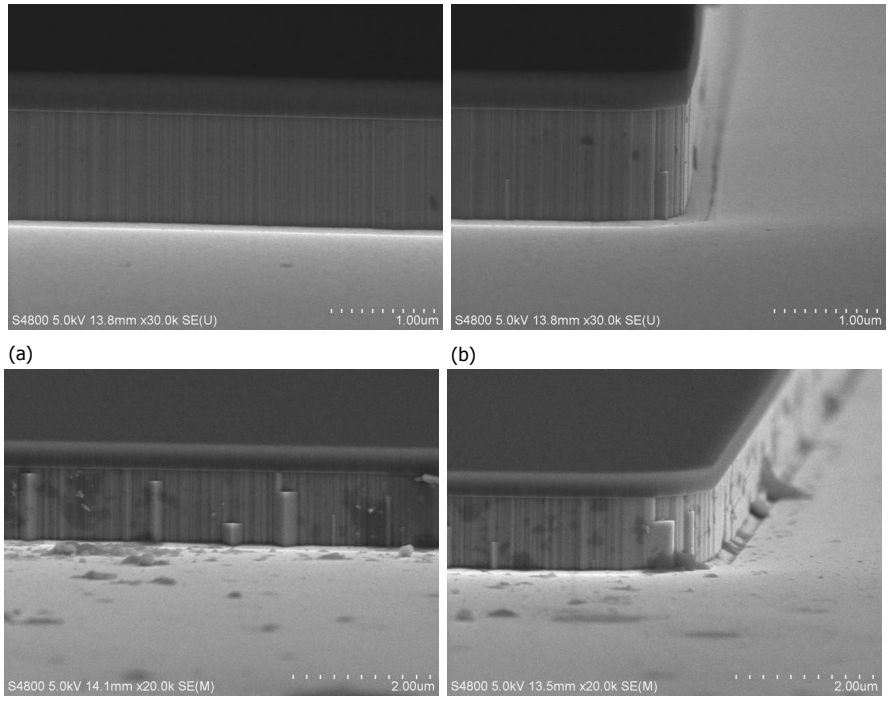


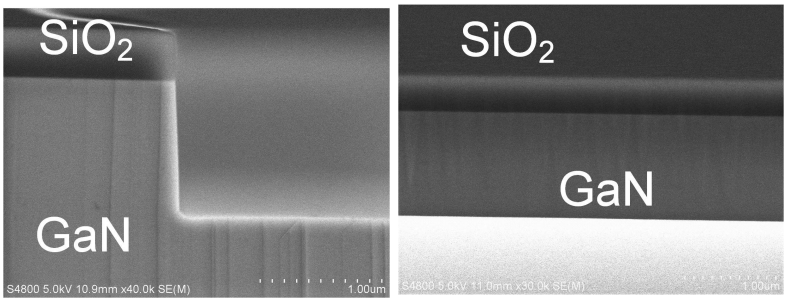
Figure 3.22: SEM images for GaN mesa structure etched with TMAH from different immersing temperatures.(a) and (b) 45℃; (c) and (d) 75℃;

3.4. Optimal GaN etching results

3.4.1. Mesa structure

A mesa structure is formed by etching during the device fabrication process, defining an active region for the quasi-vertical GaN diode. Therefore, the optimized ICP etch recipe is as follows: 360 W ICP power, 42 W RF power, 118 sccm/12 sccm flow rate of Cl_2/BCl_3 mixture gas, and 1.5 Pa pressure. The etch rate of GaN was near 120 nm/min, and the selectivity of GaN over SiO_2 was 10. The etch depth was near 1.2 μm by adjusting etch time. After that, the etched sample was alternatively dipped in 15% TMAH solution at 45℃ for 30 minutes.

Figure3.23 shows cross SEM images of the mesa sidewall and surface of etched GaN with the optimum etching recipe. The micro-trench at the bottom corner of the mesa sidewall was eliminated by optimizing etch recipes. The GaN mesa structure has a near 90° steep sidewall and smooth etched surface. The typical atomic force microscope (AFM) images taken for the etched surface at optimized samples are shown in Figure3.24. The root-mean-square roughness of the etched surface on an optimized GaN sample was about 0.43 nm ~ 0.51 nm over a $5\mu m \times 5\mu m$ area. Hence, the etching process with a smooth surface is suitable for mesa formation during the quasi-vertical GaN diode fabrication.



(a) (b)

Figure 3.23: SEM micrographs of SiO_2-masked GaN etched with the optimum etching recipe: (a) Cross-sectional view of the sidewall; (b) sidewall surface.

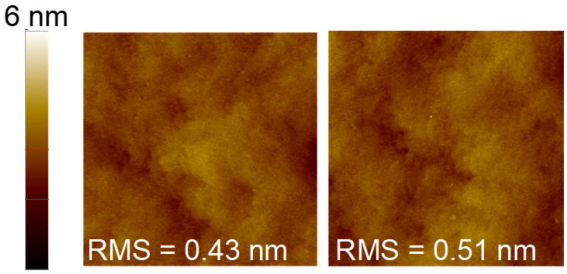


Figure 3.24: SEM micrographs of SiO_2-masked GaN etched with the optimum etching recipe. Surface morphology of the n^+-GaN surface at the mesa bottom in an area of $5 \times 5\ \mu m^2$ obtained by AFM.

3.4.2. GaN microstructures

The proposed etching technique was not confined to fabricating a GaN mesa structure for quasi-vertical devices, also be extended to other structures, such as hexagonal pyramids and nanowire arrays, promising for sensors, optoelectronics, and photovoltaics. Figure3.25 shows that the aspect ratio (depth/width) depends on the trench pitch, increasing from 0.1 to 0.5 with a fixed etching depth of 1um. As shown in the figure3.26b, the etching depth extends to at least 3.5μm without profile defects, exhibiting a relatively deep GaN trench etching capability.

Figure3.27 shows the developed GaN pillar arrays with hexagonal pyramids features, which benefit a total light reflectance from the smooth sidewall[41]. The trench structure used as a gate channel is critical to vertical transistors, demanding a smooth corner and high aspect ratio of a profile like in Figure3.28. Figure3.29 presents GaN nano structure arrays with circle shapes that could be used as a nanowire for improving the output light efficiency of LED. Figure3.30 exhibits a PN GaN mesa structure with a perfectly etching morphology, which has the potential for a high-voltage bipolar transistor in power electronic applications.

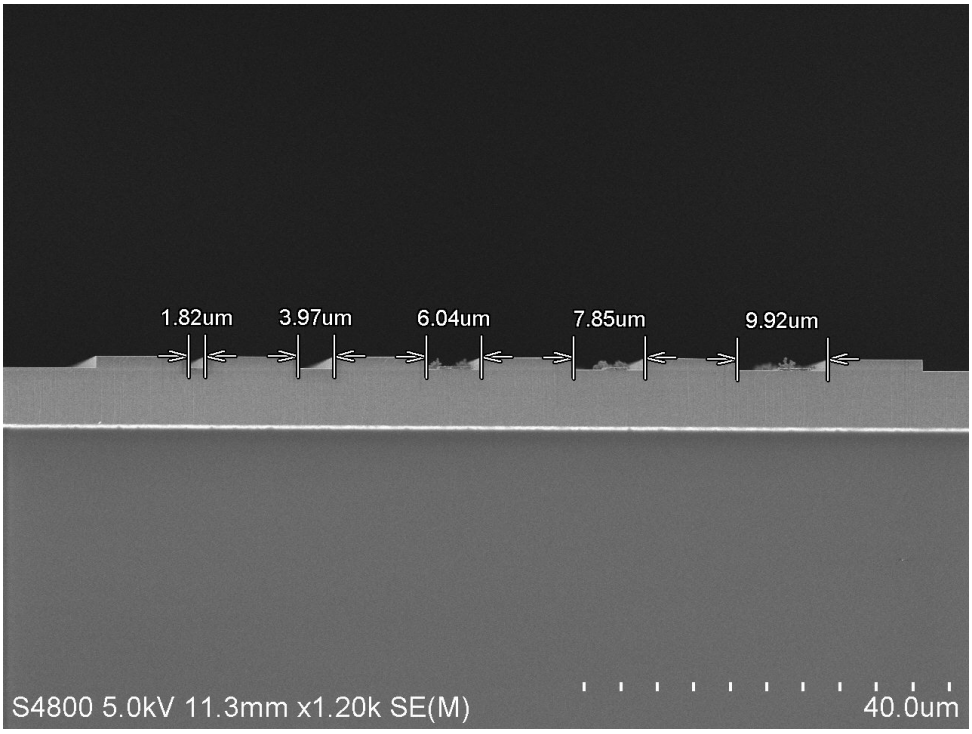
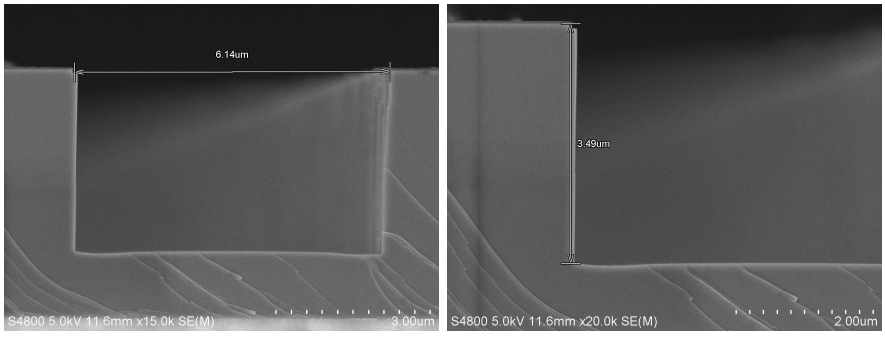
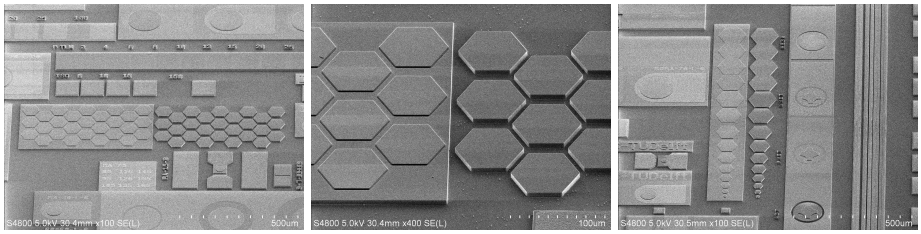


Figure 3.25: SEM images of optimized etch profiles with a depth of 1 μm for variable trench widths using the optimized etching recipe.



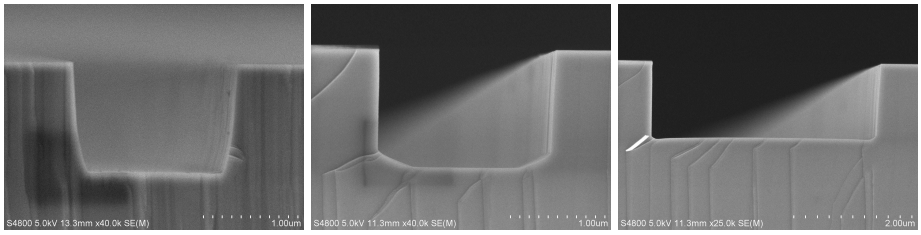
(a) (b)

Figure 3.26: (a) A deep GaN trench etching with straight sidewalls and (b) a depth of 3.5 um using optimized etching recipes.



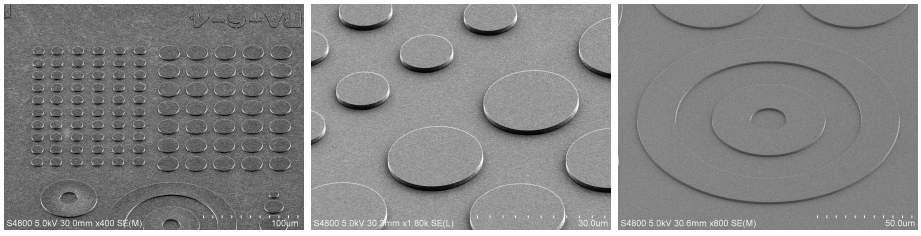
(a) (b) (c)

Figure 3.27: SEM image of the hexagonal pyramids GaN pillars in the 2D array structure.



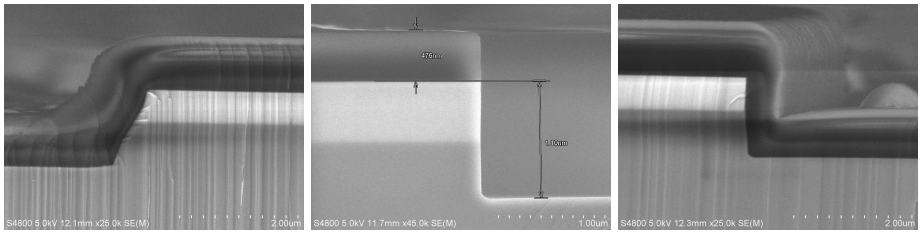
(a) (b) (c)

Figure 3.28: Cross-sectional SEM images of the rounded trench structures.



(a) (b) (c)

Figure 3.29: SEM image of GaN nanowire arrays.



(a) (b) (c)

Figure 3.30: SEM image of a P-N GaN mesa structure. (a) A slope sidewall with passivation layer; A steep sidewall with (b) hard-mask and with (c) passivation layer.

3.5. Summary

In summary, the influence of ICP etch conditions on GaN mesa sidewall profiles was studied using the optimized recipe. For the PR-masked GaN samples, high ICP power and RF power are the causes of deteriorated mesa sidewall morphology. Although high-temperature (>140 ℃) hard baking prior to etching can produce a smooth sidewall, the drawbacks are significant oblique sidewall profile formation and hard striping.

For the SiO_2-masked GaN samples, the etch rate of GaN is dependent on the ICP power, RF power, and ratio of BCl_3/Cl_2 gas flow, but has relatively less dependence on the chamber pressure. The etch selectivity of GaN over SiO_2 decreases with increasing BCl_3 concentration in Cl_2/BCl_3 mixture gas in the range of 0%-40%. The etch selectivity of GaN/SiO_2 can be increased by adjusting the chamber pressure. Moreover, the micro-trench problem at the bottom corner of the mesa can be reduced or eliminated by reducing the ICP power or RF power or by adding BCl_3 into the Cl_2 plasma. After ICP etching, the use of a TMAH wet treatment for samples can obtain a near-$90°$ steep mesa sidewall that is microtrench free and has a smooth sidewall surface.

Therefore, the optimized ICP etch recipe is as follows: 360W ICP power, 42W RF power, 118 sccm/12 sccm flow rate of Cl_2/BCl_3 mixture gas, and 1.5Pa pressure. The etch rate of GaN was near 120 nm/min, and the selectivity of GaN over SiO_2 was 10. In addition, the proposed etching technique was not confined to fabricating a GaN mesa structure for quasi-vertical devices, also be extended to other structures, such as hexagonal pyramids and nanowire arrays, promising for sensors, vertical transistors, optoelectronics, and photovoltaics.

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4

Design, fabrication and characterization of quasi-vertical GaN SBD

Although high-performance GaN SBDs on foreign substrates have been demonstrated, some critical issues still limit the development of GaN quasi-vertical SBDs. This chapter discussed the quasi-vertical GaN SBD from the perspective of epilayer structure design, device layout, device modeling, fabrication, and leakage suppression solutions. First, the design flow of quasi-vertical GaN diodes for microwave power applications is presented, including the device performance indicators, substrate selection, and device layout. Then, the quasi-vertical GaN SBD fabrication process is elaborated in schematic diagrams and real pictures. Finally, three solutions were developed to suppress the leakage current, including mesa optimization, argon ion terminations, and post-mesa nitridation. The experiment results show that our diode has the lowest leakage current density at 80% of the BV among the reported vertical GaN SBDs for the BV between 120 V and 250 V. Combining mesa optimization and post-mesa nitridation technology effectively enhances the breakdown voltage and achieves excellent conduction characteristics.

Parts of this chapter have been published in Electronics **8**, 575 (2019) [1] and in IEEE Transactions on Electron Devices **68**, 1369-1373 (2021) [2].

4.1. Device design and layout

First and foremost, one of the design target for a semiconductor device is to meet the requirements of its applications. This session mainly discusses the design of quasi-vertical GaN diode for microwave power applications from four aspects: application requirements, device performance, material properties, and device processes. Figure4.1 indicates a quasi-vertical GaN diode design flow used in power RF applications.

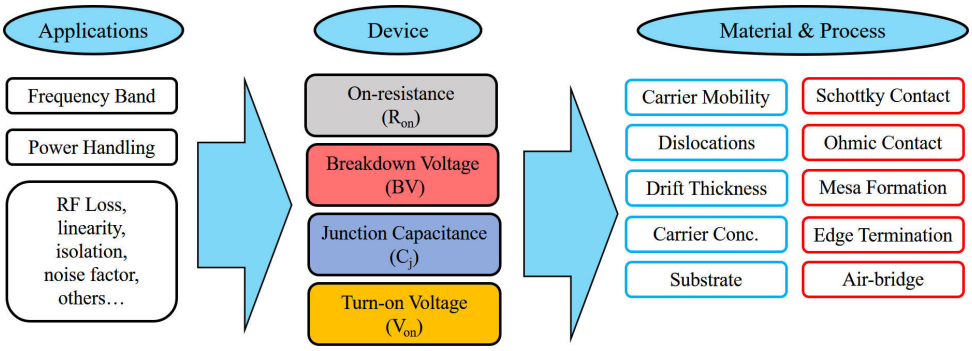


Figure 4.1: Design flow of quasi-vertical GaN diodes for microwave power applications.

Frequency band, power handling level, and RF loss are the primary performance indicators for the microwave power applications, such as power amplifiers, mixers, frequency doublers, etc. Beyond that, the linearity, isolation, and noise factor are also worth attention for designing an excellent microwave device. The first two concerned application indicators of a microwave diode are operation frequency band and power handling levels. Based on the basic physical principles, the main performance characteristics of a diode are attributed to four metrics: BV, R_{on}, C_j and V_{on}. A cutoff frequency can characterize the operation frequency band of a microwave diode. Generally, the output power of the diode is attenuated to half of the maximum value when exceeding the cutoff frequency. According to a diode equivalent circuit, both R_{on} and C_j determine the cutoff frequency expressed with $f_T = 1/(2\pi RC)$. Power handling level is regarded as the capability of a diode to conduct a maximum current and withstand a peak reverse voltage. The higher R_{on} brings higher power consumption, thus generating more heat to burn out the diode. Also, the peak voltage of a microwave signal is not allowed to exceed the BV of a diode otherwise will permanently destroy the diode. A low turn-on voltage (V_{on}) is critical for a diode rectifier to reach high efficiency.

The material properties and device fabrication are important to realizing a high-performance device. From the perspective of material properties, the high carrier mobility of bulk GaN is essential to achieve a low R_{on}, especially in a high electric field. Due to the lattice and thermal mismatch with the foreign substrate, the GaN epilayer inevitably exists in many dislocations. The carrier scattering effect induced by these dislocations results in the reduction of bulk GaN mobility. Meanwhile, the screw dislocations are also regarded as one of the major leakage paths in vertical

GaN devices. So, for the materials properties, an advanced GaN epitaxial growth technology helps to improve the crystal quality of bulk GaN and then achieves high electron mobility with low dislocation density.

The selection of substrate mostly depends on the application requirements of the GaN devices. SiC substrate has a higher thermal conductivity of 3.7 - 4.5 $W/cm \cdot K$ at 300 K, leading to a higher capability of power handling through excellent heat dissipation. At the same time, SiC substrate has a low lattice mismatch (3.5%) and low thermal mismatch (30%), leading to a low dislocation density of $10^4 cm^{-3}$. However, the small size and high cost have constrained the use of SiC wafers in the market. Silicon substrate has tremendous potential for volume production in the GaN device markets because GaN-on-silicon can be processed on standard semiconductor manufacturing lines. The GaN RF power devices grown on a large diameters (200 mm) Silicon substrate has been demonstrated in both research and commercial communities[1]. The growth of GaN on a Sapphire substrate is a mature technology with a significantly low cost. GaN-on-Sapphire devices have the advantage of a low RF loss in high frequency because of the excellent insulation properties of Sapphire substrate. Although limited by the low thermal conductivity, Sapphire is still regarded as the potential substrate in applying for relatively low-power RF devices. In the early development stage of vertical GaN RF diodes, we adapt the cheaper and available GaN-on-Sapphire wafers, which help us carry out many experiments for the critical fabrication process.

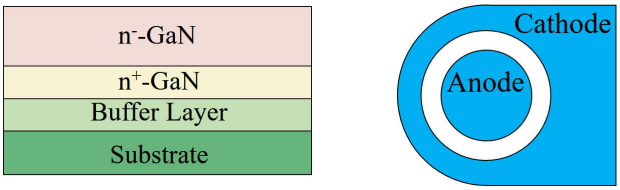


Figure 4.2: (a) Epi-layer structure and (b) circular layout of quasi-vertical GaN SBD

The GaN SBD epitaxial structure is shown in Figure4.2a. The epitaxial wafer was grown on a 2-inch sapphire (0001) substrate by MOCVD, consisting of the buffer layer, n^+-GaN conducting layer, and n^--GaN drift layer. According to the physical mechanisms of Schottky diode mentioned in chapter 2, the thickness and doping concentration of the GaN drift layer is vital for SBD to achieve a high breakdown voltage. The doping concentration of n^--GaN drift layer is designed as low as possible to suffer a maximum reverse voltage. The BV ratings of diode applications determine the thickness of the n-GaN drift layer. The n^+-GaN conducting layer has a relatively high doping concentration to form an excellent ohmic contact and alleviate the current crowding effect in the quasi-vertical diode. As shown in Figure4.2b, a circular structure was adopted in the quasi-vertical GaN SBD layout design to avoid the spherical junction and reduce the curvature effect. The device layout design

[1]https://www.imec-int.com/en/200mm-GaN-on-Si-technology

consists of three major parameters: R_A: anode radius; R_C: cathode radius; L_{AC}: The spacing between anode and cathode.

4.2. Fabrication of vertical GaN diode

4.2.1. Fully-vertical GaN diode

A typical process flow [3] of fully-vertical GaN SBD on foreign substrate is shown in Figure4.3. The GaN epilayer was subsequently grown on sapphire substrates by metal organic chemical vapor deposition (MOCVD)[4]. In Figure4.3a, the contact metal was deposited on GaN epilayer. After that, the samples were annealed at a certain condition to further improve the ohmic behavior. (Ti/Al/Ni/Au at $600℃$ - $840℃$ in N_2 for $20s$-$30s$; Ti/Al/Pt/Au at $700℃$ -$850℃$ in N_2 for $30s$; Ti/Al; Ti/Al/Ti/Au ; Ti/Al/Au.) Then, the nickel layer is formed on ohmic contact metal by an electroplating process, as shown in Figure4.3b. To remove the sapphire substrate, a laser power was used to cause local heating at the GaN/sapphire interface which in turn lead to the decomposition of the GaN, as shown in Figure4.3c and 4.3d. Finally, the Schottky metal (Ni/Au) was deposited using e-beam evaporation, as shown in Figure4.3e.

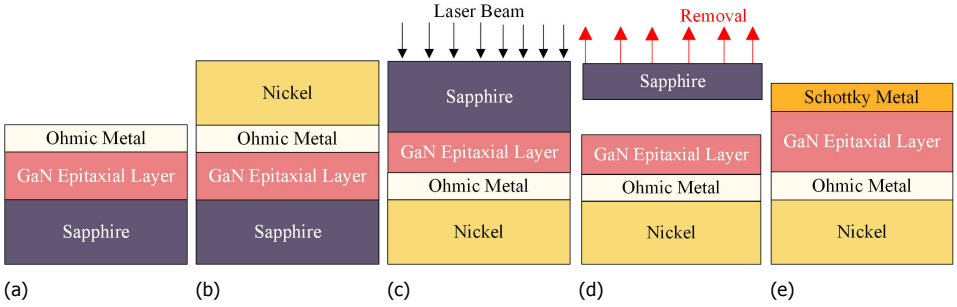
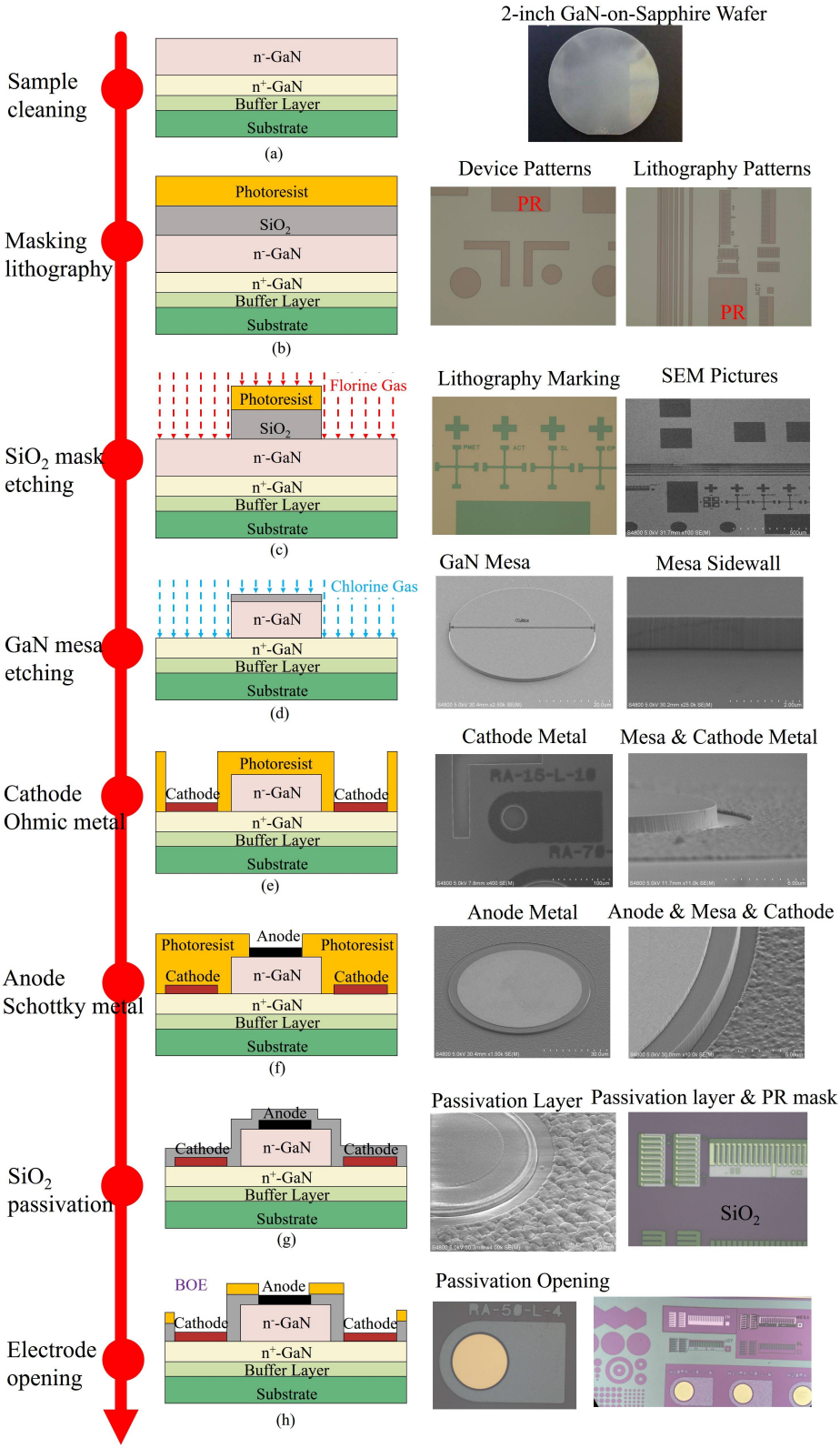


Figure 4.3: Vertical GaN SBD device process flowchart: (a) ohmic contact, (b) nickel electroplating, (c) laser lift-off, (d) sapphire removal, and (e) Schottky contact.

4.2.2. Quasi-vertical GaN diode

The quasi-vertical GaN SBD has a different fabrication flow from fully-vertical devices. The fabrication flow of the quasi-vertical GaN SBD is shown in Figure4.4. The GaN wafer consisted of a substrate, undoped buffer layer, n^+-GaN conducting layer (Si doping), and n^--GaN drift layer (Si doping). First, a SiO_2 mask layer was deposited by plasma-enhanced chemical vapor deposition (PECVD), followed by the reversal photoresist (AZ5214E) coating, exposure, and development. The SiO_2 hard mask was then opened by fluorine-based ICP etch. After the pattern was transferred from the SiO_2 into the GaN layer and the mesa structure was formed by chlorine-based ICP etch, the SiO_2 mask was stripped using a Buffer of Etchant (BOE) solution. The optimized etching recipe in chapter 3 was used to form a low-damage GaN mesa.


Sample cleaning
n⁻-GaN
n⁺-GaN
Buffer Layer
Substrate
(a)
2-inch GaN-on-Sapphire Wafer
Masking lithography
Photoresist
SiO2
n⁻-GaN
n⁺-GaN
Buffer Layer
Substrate
(b)
Device Patterns
Lithography Patterns
PR
PR
SiO2 mask etching
Florine Gas
Photoresist
SiO2
n⁻-GaN
n⁺-GaN
Buffer Layer
Substrate
(c)
Lithography Marking
SEM Pictures
GaN mesa etching
Chlorine Gas
n⁻-GaN
n⁺-GaN
Buffer Layer
Substrate
(d)
GaN Mesa
Mesa Sidewall
Cathode Ohmic metal
Photoresist
Cathode
n⁻-GaN
Cathode
n⁺-GaN
Buffer Layer
Substrate
(e)
Cathode Metal
Mesa & Cathode Metal
Anode Schottky metal
Photoresist
Anode
Photoresist
Cathode
n⁻-GaN
Cathode
n⁺-GaN
Buffer Layer
Substrate
(f)
Anode Metal
Anode & Mesa & Cathode
SiO2 passivation
Anode
Cathode
n⁻-GaN
Cathode
n⁺-GaN
Buffer Layer
Substrate
(g)
Passivation Layer
Passivation layer & PR mask
SiO2
Electrode opening
BOE
Anode
Cathode
n⁻-GaN
Cathode
n⁺-GaN
Buffer Layer
Substrate
(h)
Passivation Opening

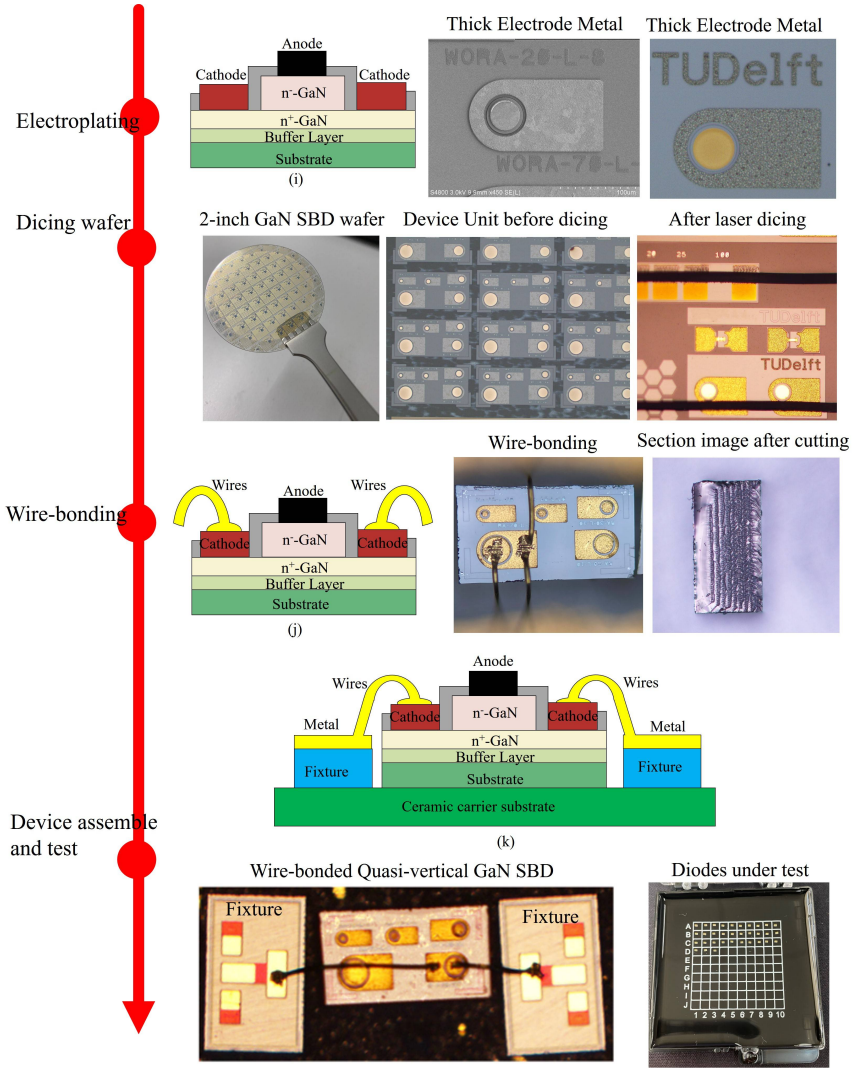


Figure 4.4: A typical process flow diagram of the quasi-vertical GaN SBD.

Then, Ti/Al/Ni/Au was deposited and annealed to form ohmic contacts with the n^+-GaN layer, which acted as the cathode electrode. A Ni/Au circular electrode was deposited to form a Schottky contact with the n^--GaN drift layer, which acted as the anode electrode. Consequently, the SiO_2 passivation layer was deposited by PECVD and then opened by BOE to expose the electrodes. A thick power metal (Au) was plated on anode and cathode to aid wire-bonding on the test board. Finally, we used the bonding wires to connect the electrode of GaN SBD with a test fixture.

4.3. Device modeling and optimization

The semiconductor manufacturing process is complicated, which takes a bit of time and consumes expensive materials. Therefore, developers usually use the commercial technology computer-aided design (TCAD) simulation tools to perform the characteristic analysis of new devices. The optimized simulation results can provide more support for subsequent fabrications. The available TCAD simulation tools for semiconductor devices were initially developed based on silicon, such as Mentor Sentaurus and Atlas Silvaco. The silicon material parameters and models are mature and can accurately reflect the performance of silicon-based devices. However, there are still some problems for wide-bandgap semiconductor devices in TCAD simulation tools, including model convergence and prediction precision.

The current-crowding effect and peak electric field are the two critical issues in quasi-vertical GaN SBD. We performed Silvaco tools to analyze and predict the problems as a reference for device design and fabrication (The Silvaco simulation code used in this section can be found in Appendix A).

4.3.1. Current crowding effect (CCE)

Quasi-vertical GaN diodes have a n^+-GaN spreading layer with a large lateral resistance that restricts the forwarding current nearby the mesa corner, called the current-crowding effect (CCE)[5, 6]. The schematic of CCE in a quasi-vertical diode is shown in figure4.5a. This effect will induce a large amount of current in a small region around the mesa corner, thus reducing the effective conductive area and causing uneven heating generation over the diode[7]. To solve the CCE issue, we need to optimize the resistance of n^+-GaN spreading layer by changing the doping concentrations and thickness. Table4.1 lists the epitaxial structure parameters used in the diode simulation. Figure4.5b-4.5d shows the simulated current density distribution in GaN SBD at varies thickness under a froward bias of 3 V.

Table 4.1: The primary structure parameters of quasi-vertical GaN SBD for TCAD simulation

Parameter	Variable	Values
n^--GaN Thickness (μm)	T_{drift}	1
$N_D - N_A$ in n^--GaN (cm^{-3})	$N_{D,drift}$	4×10^{15}
n^+-GaN Thickness (μm)	$T_{cond.}$	0.2; 1; 3
$N_D - N_A$ in n^+-GaN (cm^{-3})	$N_{D,cond.}$	$5 \times 10^{17}; 1 \times 10^{18}; 5 \times 10^{18}; 1 \times 10^{19}$

$N_D - N_A$ is the electron concentration; n^--GaN is the drift layer; n^+-GaN is the conducting layer.

The simulated results of the thickness variation are shown in figure4.5b-4.5d. A very high current density is observed near the surface of the n^+-GaN layer. With increasing the thickness of n^+-GaN from 0.2 to 3μm, the current spreads closer to the device center due to the reduction of lateral resistance of n^+-GaN conduction layer. Similar results are observed in figure4.6a-4.6d. With the increase of doping concentration, the resistance of n^+-GaN is small enough that the current tends to

spread away from the device edge. Therefore, making the lateral resistance of the n^+-GaN layer as low as possible can alleviate the CCE problem to a degree. The quasi-vertical structure is more suitable for a small diode with enough conductive area since the CCE strongly impacts current density in a large diode with a spreading layer with high lateral resistance.

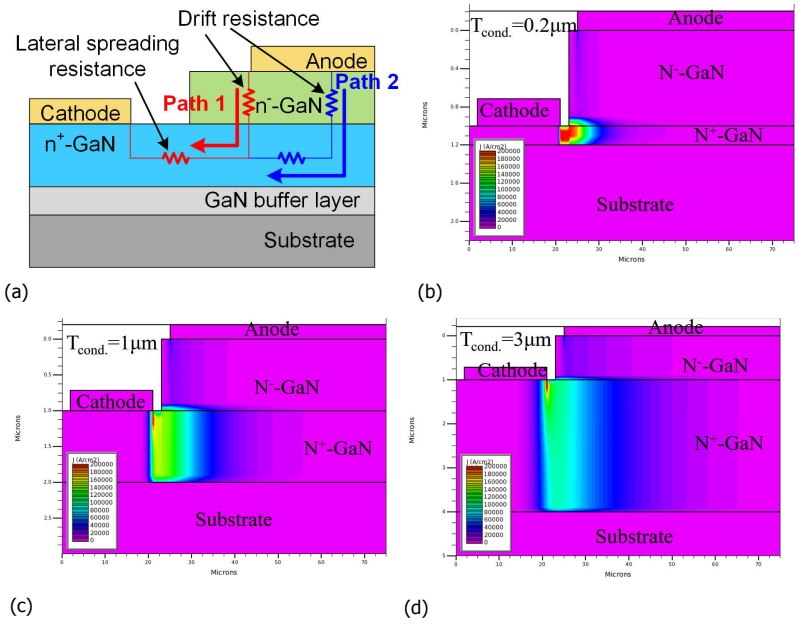


Figure 4.5: (a) The schematic of current-crowding effect (CCE) in a quasi-vertical GaN SBD. Path 1 and path 2 represent different conductive paths. Forward current profiles of quasi-vertical GaN SBD with different n^+-GaN layer thickness. (b) 0.2 μm; (c) 1 μm;(d) 3 μm.

As a consequence, we defined a low-mobility region near the surface of the etching region to simulate the effect of etching damages on the forward characteristics[8], as shown in Figure4.7. The project codes are presented in Appendix A. The simulated results show that the etching damages significantly affect the current distribution, leading to a decrease of forward current density. The current choke effect in the etching region can be explained as the enhancement of carrier scattering when introducing the etching damage defect (e.g., micro-trench, pits, and pillars).

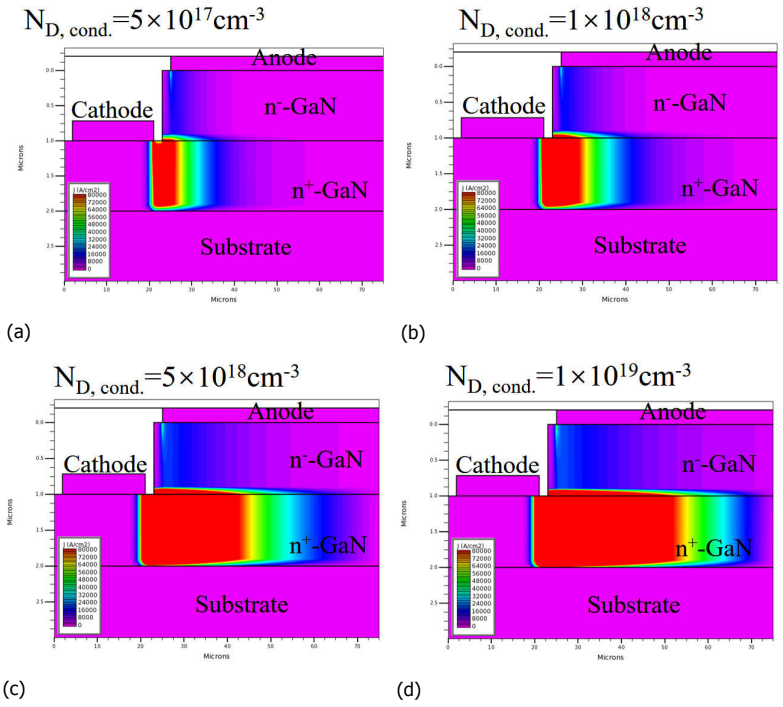


Figure 4.6: Forward current profiles of quasi-vertical GaN SBD with different n^+-GaN layer doping concentrations. (a) $5 \times 10^{17} cm^{-3}$; (b) $1 \times 10^{18} cm^{-3}$; (c) $5 \times 10^{18} cm^{-3}$; (d) $1 \times 10^{19} cm^{-3}$;

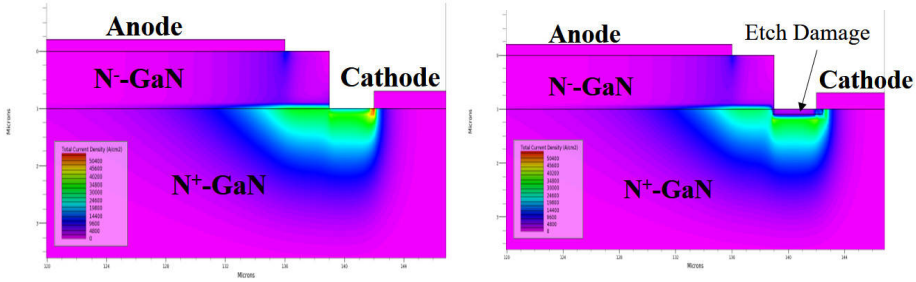


Figure 4.7: Simulated current density distribution in quasi-vertical GaN SBD (a) without and (b) with damages nearby the surface in the etch region at a forward bias of 3 V.

4.3.2. Peak electric field

The peak electric field is crowded at the edge of Schottky contact metal, causing the early device breakdown under reverse bias. A reverse characteristic simulation of the quasi-vertical GaN SBD was performed with different applied voltages. The simulated electric fields distribution at -40 V, -80 V, and -150 V are shown in Figure4.8a-4.8c, respectively.

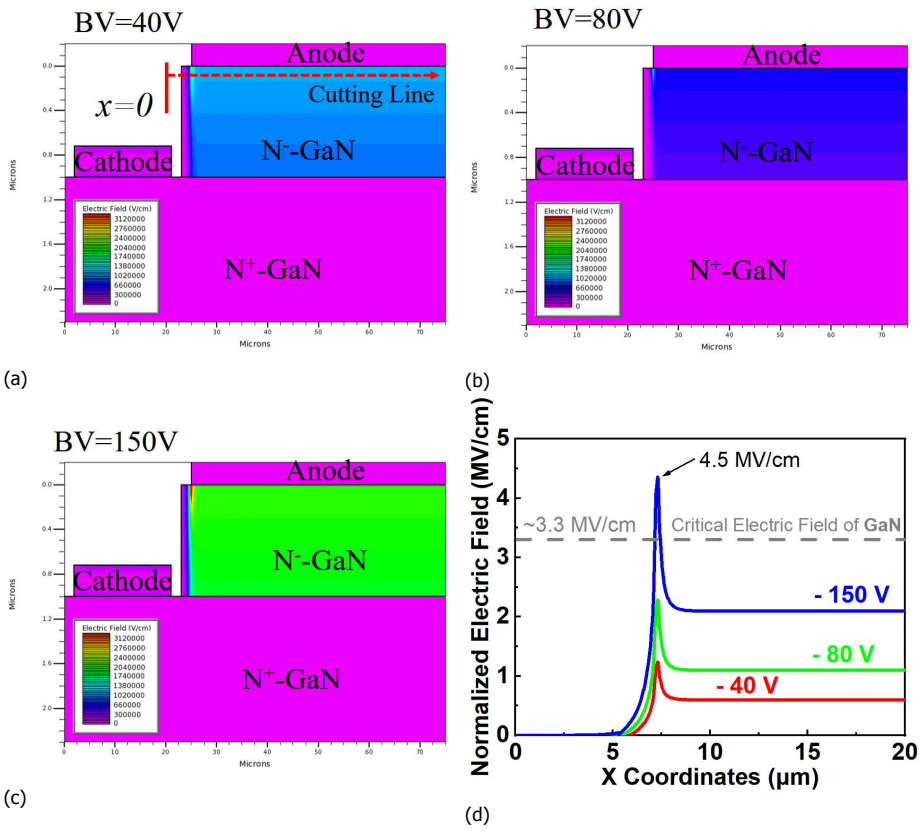


Figure 4.8: Electric field distribution of peak electric field as a function of reverse bias voltage (a) at -40V, (b) at -80V, (c) at -150V and (d) electric field along cutline in the simulation results presented in (a)-(c).

Figure4.8d plots the normalized electric field distribution for a diode various reverse biases along the cut-lines (red dotted line in Figure4.8a). It is observed that the peak electric field strength near the Schottky junction edge reached a strong electric field of 4.5 MV/cm, exceeding the critical electric field of GaN materials (3.3 MV/cm). Therefore, the simulated BV of the proposed GaN diode is predicted in the range of 80V-150V. It is noticed that the predicting accuracy of BV is rough due to the incomplete physical model of GaN. Meanwhile, the depletion region can reach the mesa edge, possibly introducing an additional leakage path along the

mesa sidewalls.

4.4. Suppression of leakage current

A large reverse leakage current can cause off-state power loss and reliability problems[9, 10], limiting the development of GaN quasi-vertical SBDs. It is reported [8] that the off-state leakage of the GaN-on-Si vertical p-n diode can be classified into four possible paths: 1) through the transition layers and Si substrate; 2) through the drift layer; 3) along the etch sidewall; 4) through the passivation layer. Figure4.9 shows the schematic of the GaN-on-Si vertical p-n diodes and marks the four possible leakage paths.

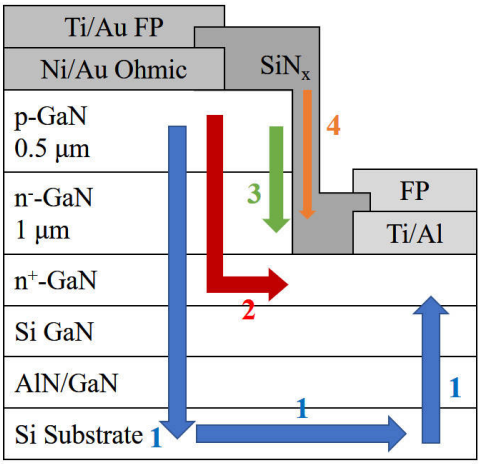


Figure 4.9: Design flow of quasi-vertical GaN diodes for microwave power applications[8].

Since the excellent insulation properties of a sapphire substrate, the leakage current through the substrate is much less than in the other three paths. The GaN-on-Sapphire GaN SBD has three primary leakage paths, including through the drift layer, along the etch sidewall, and through the passivation layer.

A large number of traps and threading dislocations exist in GaN materials in reality. The leakage through the drift layer is relevant with the threading dislocations in bulk GaN, which can be improved by optimizing the quality of the crystal. The presence of unintentional surface defect donors (e.g., nitrogen vacancy) at the Schottky interface cause a reduction of the Schottky barrier width, inducing a large leakage current explained by the thin surface barrier (TSB) model[11]. Trap-assisted tunneling (TAT) is another trap-related leakage conduction mechanism[12]. The leakage through the passivation layer can be blocked with a low-damage passivation technology. The leakage current along the mesa sidewall is typically due to the damage or defects induced by high-energy ion etch, which can be suppressed by optimizing the deep-etching technology and advanced edge termination technology[8].

For the high-voltage vertical GaN diodes, some works suggest that the leakage

can be inhibited by using edge terminations[13], reducing dislocation density of the drift layer[14], passivating the etched mesa[15], or reducing the interface defect density at the Schottky contact interface[16]. In general, the microwave devices requires a low junction capacitance (< 10 pF), low R_{on} and relatively low BV (< 200 V), which requires that the microwave GaN diode have a small device area and a thin drift layer (< 1.5 μm). The small GaN diode is sensitive to the damages or defects induced by high-energy ion treatment during etching or implantation processes. Therefore, it is essential to analyze the leakage mechanism and find an effective suppression solution in microwave GaN diode. We adapt three solutions to suppress the leakage: mesa optimization, Argon ion terminations, and post-mesa nitridation. The leakage suppression solutions for quasi-vertical GaN diode are schematically shown in Figure4.10.

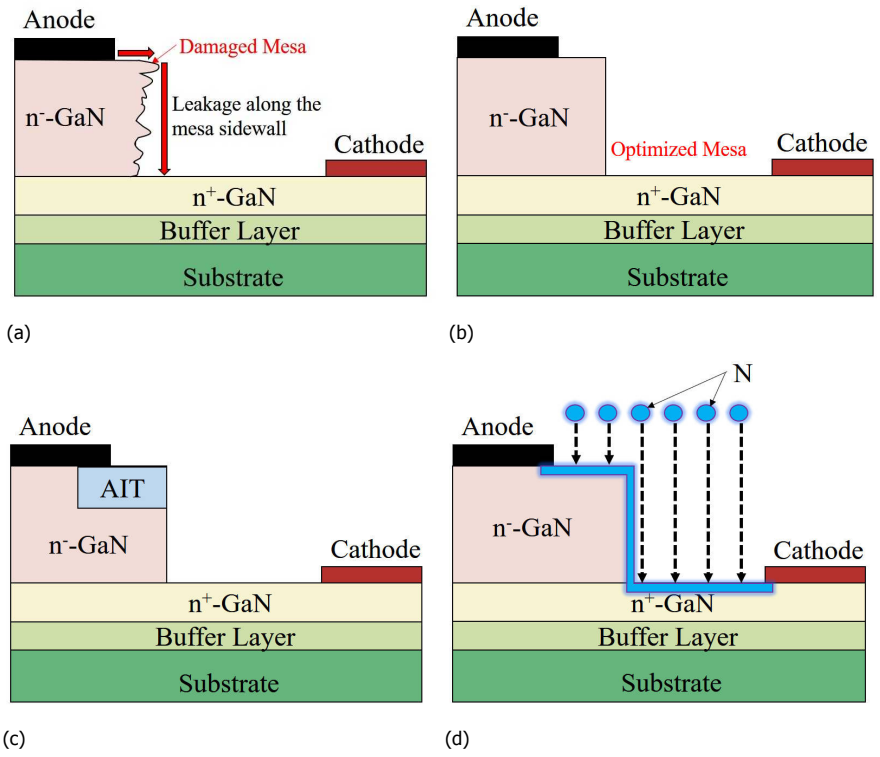


Figure 4.10: Schematic of the quasi-vertical GaN SBD structure with three suppression solutions. (a) Reference, (b) optimal mesa, (c) optimal mesa with Argon implanted termination, and (d) optimal mesa with N_2 plasma treatment.

The GaN epilayer structure consists of a 2 μm undoped buffer layer, a 3 μm n^+-GaN conducting layer (Si doping: $5 \times 10^{18} cm^{-3}$), and a 1 μm n^--GaN drift layer (Si doping: $1 \times 10^{16} cm^{-3}$). The total dislocation density of the GaN epitaxial layer was $4 \times 10^8 cm^{-2}$, which is calculated with the full width at half maximum of the plane rocking curves orientations. All samples in this section have grown the 2-

inch Sapphire (0001) substrate with the same epitaxial structure in the same batch. Figure4.11 shows the experiment plan of these four samples.

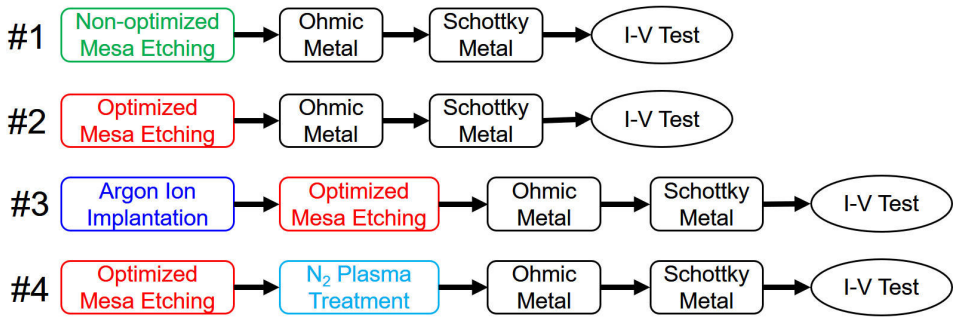


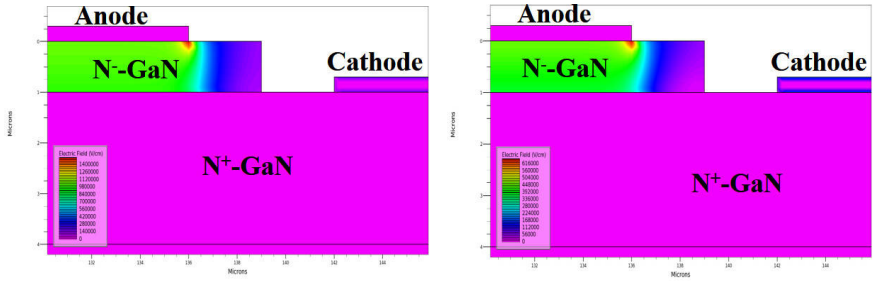
Figure 4.11: Experiment plan of the leakage suppression for quasi-vertical GaN Schottky diode.

The first sample was etched with non-optimized conditions as a reference. The rest of the samples were dry-etched with optimized recipes by ICP etching tools. Before the mesa etching process, the third sample was implanted with Argon ions to form an edge termination on a designed region. The fourth sample was performed N_2 plasma treatment after the mesa etching process. All samples have the same metallization process, including Schottky and ohmic contact. Ti/Al/Ni/Au was deposited and annealed at 600℃ for 2 minutes to form ohmic contacts with the n^+-GaN layer, which acted as the cathode electrode. A circular Ni/Au electrode was deposited to form a Schottky contact with the n^--GaN drift layer, which acted as the anode electrode.

4.4.1. Mesa etching optimization

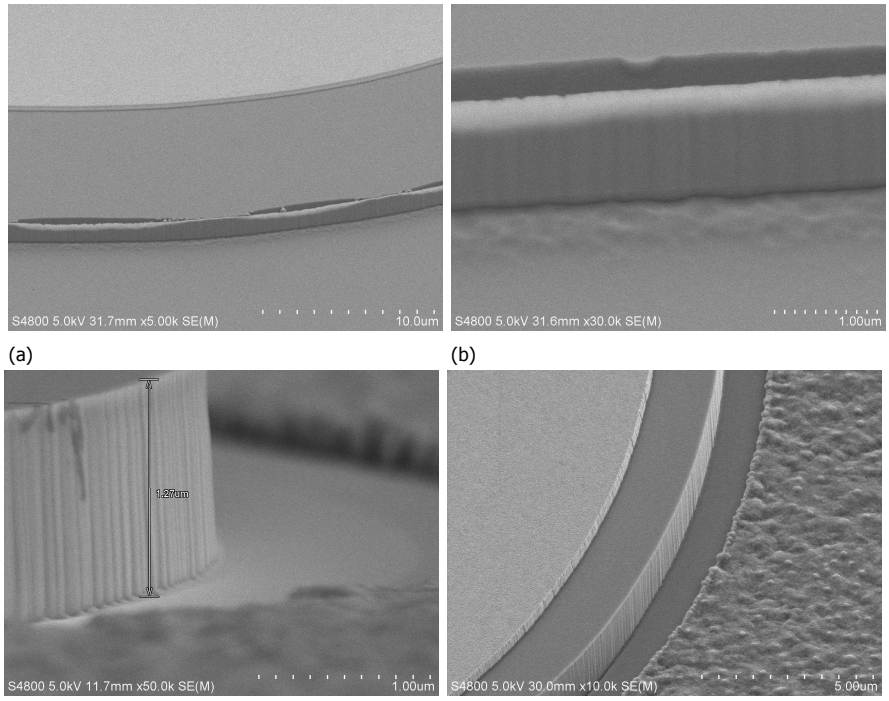
It is reported that not well-treated mesa sidewall can be one of the reasons to cause the high reverse leakage[17–19] and lead to potential reliability problems[10]. We optimized the etch recipe to form a GaN mesa structure with a highly anisotropic profile and low-damage sidewall in chapter 3. Consequently, we pursued a comparative study about the effect of the mesa on the reverse characteristics of a diode. The first step is to verify whether the depletion region has enough lateral length to reach the mesa sidewall. We simulated the reverse characteristic to study the effect of mesa sidewall damage on leakage. The model and structure parameters were set close to the actual conditions in the simulation. The simulated electric fields distribution of our diode at -40 V and -100 V are shown in Figures4.12a-4.12b, respectively.

According to the simulation results, the lateral depletion region has reached the mesa edge with a distance of 3 μm between anode edge and mesa sidewall, when the reverse bias is greater than 40 V. The leakage current will move along the mesa sidewall once the surface is damaged by etching. Thus, the damaged mesa will act as a leakage path to degrade the BV of a diode, which also can be improved by realizing a low-damage and perfect anisotropic profiles.



(a) (b)

Figure 4.12: Simulated electric fields distribution in quasi-vertical GaN SBD at (a) -40 V and (b) -100 V.



(a) (b)

(c) (d)

Figure 4.13: Cross SEM image of the mesa for quasi-vertical GaN SBD with different etch conditions. The sidewall profile of mesa structure was etched with non-optimized ((a) and (b)) and optimized etching conditions ((c) and (d)).

After completing the fabrication process, the local SEM view of the mesa sidewall has been compared and shown in Figure4.13. The non-optimized sample was processed without mesa optimization, resulting in an erosion device edge and relatively rough etched surface. In contrast, the optimized sample with optimal mesa achieves near-90° steep, micro-trench free, and smooth sidewall, shown in Figure4.13c and reffig4.13d.

The samples were repetitively measured on the Keysight B1500 semiconductor analysis instrument. The forward and reverse characteristics are shown in Figure4.14a and Figure4.14b, respectively. The optimized mesa sample had a reverse leakage current density of $10^{-8}A/cm^2$ at -10 V, which is 2 orders of magnitude lower than that of the non-optimized one. The nearly 1 ideality factor indicates less of a trapping effect, both in bulk and interface. Moreover, the state-of-the-art low reverse leakage current indicates that the damage to the mesa sidewall is low[20–23]. The leakage current in this work is much lower than AlGaN/GaN heterostructures SBD[24]. Both GaN diodes have a similar specific on-resistance ($R_{ON,sp}$) of 0.47 $m\Omega \cdot cm^2$and turn-on voltage of 0.7 V (extracted at 1 A/cm^2), indicating the mesa optimization process not affects the Schottky interface.

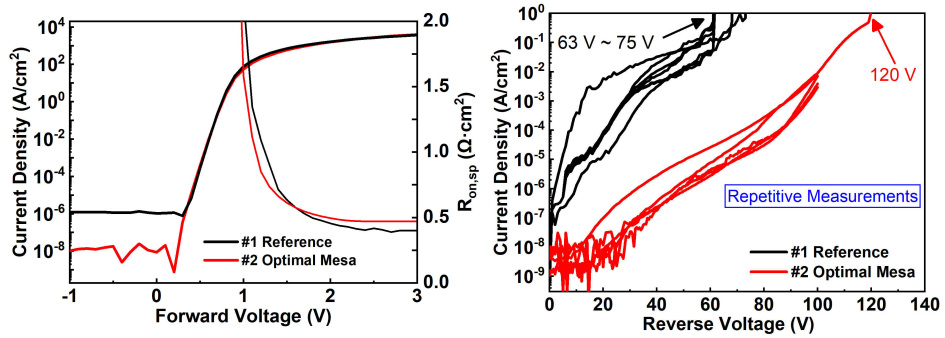


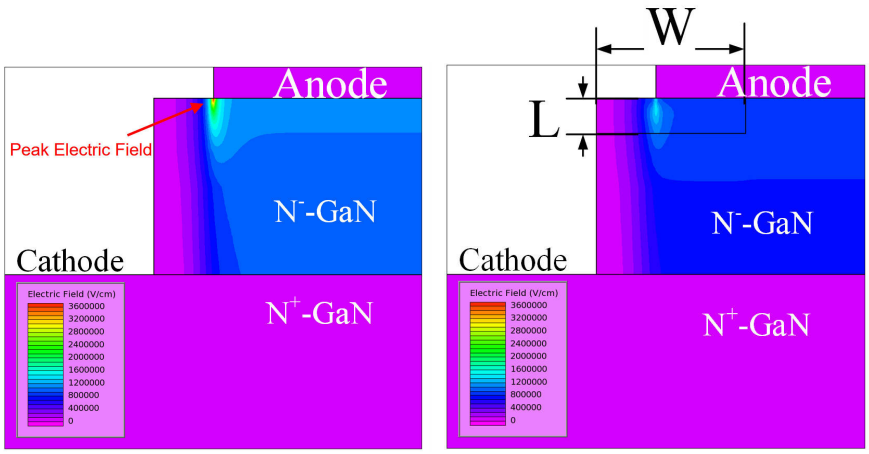
Figure 4.14: (a) Forward and (b) reverse I-V characteristics of the quasi-vertical GaN SBDs with and without optimal mesa in this study.

4.4.2. Argon-implanted termination (AIT)

High BV and low R_{on} are essential for microwave power devices operating at a high input power level and high-frequency band. In the early stage of GaN development, Wu Y. F. et al.[25] reported a field-plate structure HEMT device applied for a high-power RF system that achieved a BV of 120V and operated at 4GHz and 8 GHz. At present, Moser, N. et al.[26] presented a vertical Ga_2O_3-based RF power device with a BV of 50V with a gate length of 0.5 μm, achieving a 2.1 GHz-μm $f_T - f_G$ product (gate scaling factor). The future high-power RF devices should be towards a high blocking voltage above 100V and operate at frequencies above 10 GHz. Therefore, the BV needs to be increased further to make the RF diode operate with a high voltage swing possible.

Typically, the peak electric field nearby the edge of Schottky junction leads to a

pre-breakdown under reverse bias. Edge termination techniques are proposed and utilized to improve the crowded electric field at the periphery of the active region. The most commonly used termination techniques are discussed in the previous chapter, including field rings, junction termination extension (JTE), and field plates. A resistive field plate termination has a high-resistivity region at the edge of the anode to smooth the peak electric field around the surface. Ozbek and Baliga[27, 28] reported two types of GaN SBDs with a resistive field plate formed by Argon ion implantation (AIT) on GaN and sapphire substrates, respectively. However, the edge terminations need to be optimized with more effective and suitable solutions because the RF diodes generally have a relatively lower BV rating than power diodes.



(a) (b)

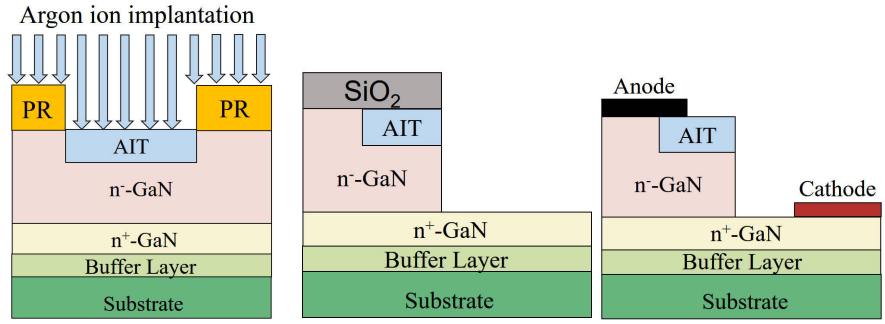
Figure 4.15: The simulated electric fields distribution at -100 V of a diode (a) without and (b) with AIT.

The effect of implantation region on the distribution of electric field was firstly analyzed by the device simulation. After defining the layout of device with terminations, the Argon implantation process parameters were designed using the process simulation tools - SRIM (Stopping and Range of Ions in Matter). Finally, the quasi-vertical GaN Schottky diode with AIT has been fabricated and characterized. The forward and reverse characteristics were measured by the B1500 Semiconductor Analysis Network.

The simulated electric field distribution of quasi-vertical GaN SBD without and with AIT are shown in Figure4.15. Figure4.15a shows that the peak electric field strength near the device edge has exceeded the critical electric field (3.3 MV/cm) of GaN materials for a diode without AIT. Consequently, we define a termination region at the edge and then set a couple of size parameters for simulation, including width (set as W) and length (set as L). The implanted region uniformly distributes a lot of deep-level acceptor defects with a concentration of $1.0 \times 10^{18} cm^{-3}$ [29–31] and a Fermi energy level of 1.5 eV (located in the middle of the bandgap[27]). After optimizing the edge termination structure parameters, the peak electric field

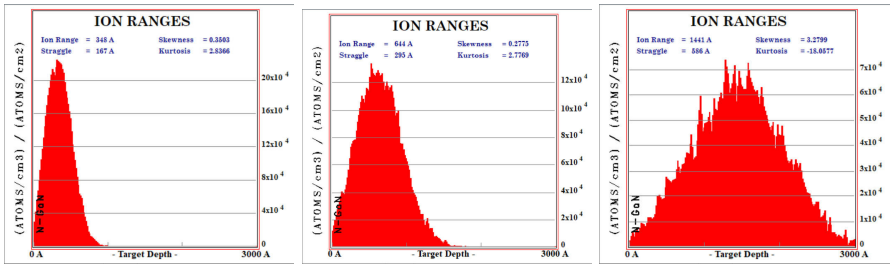
strength has been effectively reduced to a low value. According to the simulation results in Figure4.15b, the termination region has an optimized size of 5 μm width and 200 nm length.

The simplified diode fabrication flow combing an Argon ion implantation process is shown in Figure4.16. A thick photoresist mask (AZ4620) was coated and post-baked as a protective layer to protect the non-implanted area at the surface of the GaN wafer. The post-baking process of the photoresist has carried on the hotplate with a temperature of 120℃ for 2 minutes. After that, the Argon ion was implanted into the GaN wafer using an ion implanter tools. Finally, the mesa was etched with optimized etching recipes, followed by the deposition of anode and cathode.



(a) (b) (c)

Figure 4.16: Simplified fabrication flow of quasi-vertical GaN diode with AIT structure. (a) Ion implantation; (b) mesa etch; (c) electrodes deposition.

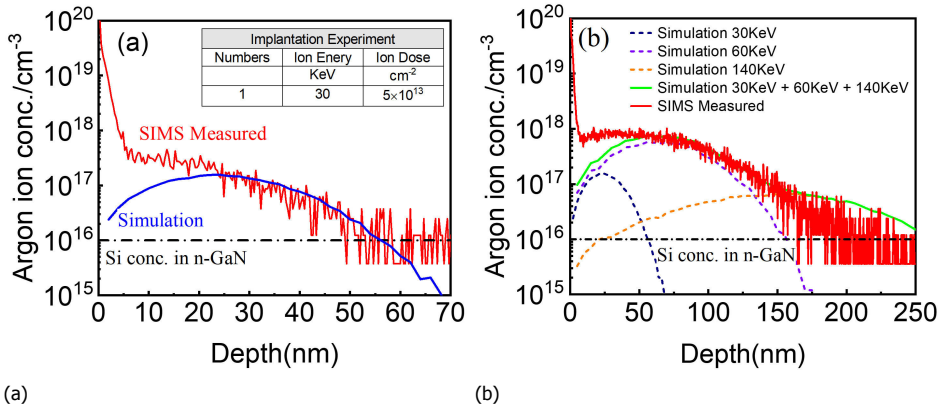


(a) (b) (c)

Figure 4.17: One-dimensional concentration distribution of Argon ion implantation in linear coordinates. (a) 30 KeV; (b) 60 KeV; (c) 140 KeV.

We used the process simulation tool - SRIM to optimize the parameters of Agron ion implantation. The implantation dose and energy are the two critical process parameters that determine the depths and concentrations of implanted ions inside the material, respectively. The implantation dose was set to the same value of $1 \times 10^{14} cm^{-2}$ in these three conditions. Figure4.17 presents the simulated Argon ion concentration versus depth varied with implantation energy. It is observed that

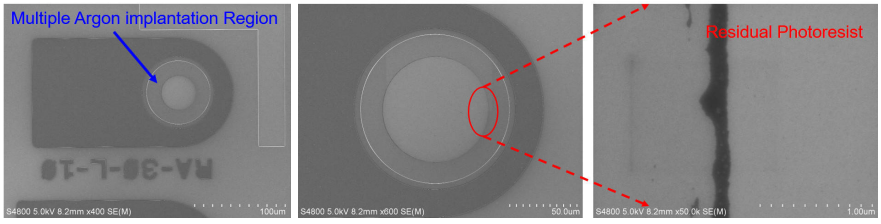
the implanted ion concentration has a normal distribution in a vertical direction. With the increase of implantation energy from 30 KeV to 140 KeV, the position of peak ion concentration to the surface increases from 40 nm to 170 nm.



(a) (b)

Figure 4.18: Comparison of simulated and SIMS measured distribution of Argon ion concentration in GaN. (a) Single implantation; (b) multiple implantation.

Then, to verify the SRIM simulated results, an Argon ion implantation experiment was carried on the 2-inch n-GaN wafer with two recipes, including single implantation with an energy of 30 KeV and multiple implantations with 30 KeV, 60 KeV, and 140 KeV. The implantation dose holds on the value range of $5 \times 10^{13} cm^{-2}$ to $1 \times 10^{14} cm^{-2}$. The following SIMS (Secondary Ion Mass Spectroscopy) analysis was conducted on the implantation region and focused on the Argon ion concentration distribution inside materials. As shown in Figure4.18, the SRIM simulated results are consistent with the SIMS experiment results. The multiple implantation region has a high ion concentration above $10^{16} cm^{-3}$ with a vertically distribution length of 170 nm inside the material, which is more suitable for forming an AIT structure in the quasi-vertical GaN diode.

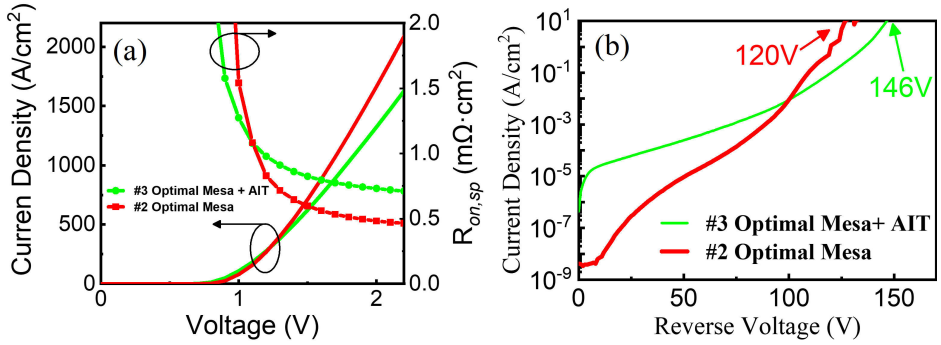


(a) (b)

Figure 4.19: Microscopic picture of diode with (a) multiple Ar implantation before the anode process. (b) A larger version and local SEM image of damaged photoresist edge (in the inset of (b)).

In addition, the edge of the implantation region was deteriorated by multiple high-energy Argon ion implantation due to the thin photoresist in the periphery, as shown in Figure4.19a-Figure4.19b. It is hard to stripe the residual photoresist with

a regular stripping process. Hence, UV/Ozone exposure and O_2 plasma treatment were combined to depolymerize the residual photoresist. Meanwhile, the plasma etching treatment inevitably damages the surface, affecting the diode performance.



(a) (b)

Figure 4.20: Comparison of simulated and SIMS measured distribution of Argon ion concentration in GaN. (a) Single implantation; (b) multiple implantation.

Finally, the quasi-vertical GaN Schottky diode with AIT has been fabricated and measured. Figure4.20a illustrates the measured forward I-V characteristics of the diodes. By comparing the measured results, GaN diode with AIT structure has a higher specific on-resistance ($R_{on,sp}$) of 0.71 $m\Omega \cdot cm^2$ and lower turn-on voltage of 0.65 V (extracted at 1 A/cm^2) than without AIT structure. One reason is the number of surface defects in the anode region produced by the O_2 plasma treatment when striping the residual photoresist. The high-energy implanted oxygen ions break the Ga-N bond and then produce a lot of N vacancies regarded as a shallow donor, enhancing the tunneling process of the Schottky diode[32, 33]. Therefore, the turn-on voltage of a diode is slightly reduced from 0.7 V to 0.65 V after O_2 plasma treatment. Meanwhile, the specific on-resistance of the diode has increased from 0.47 $m\Omega \cdot cm^2$ to 0.71 $m\Omega \cdot cm^2$, attributed to the high-resistivity implantation region near the device periphery.

Figure4.20b presents the measured reverse I-V characteristics of the diode with and without AIT. The AIT structure enhances the BV of the GaN diode with a higher value of 146 V, benefiting from the alleviation of the peak electric field under high reverse voltage. However, the defects induced by multiple high-energy Argon ion implantation produce the extra leakage path, resulting in the significant leakage of the diode with AIT in a low reverse voltage[28, 34]. A possible explanation for the extra leakage path is that the defects-induced traps in the implantation region enhance the space-charge-limited conduction (SCLC) process[35].

4.4.3. N_2 plasma treatment

Some literature has illustrated that N_2 plasma treatment in a vertical GaN-on-GaN diode can effectively inhibit the sidewall leakage by compensating the N vacancies along with the etched surface and sidewall[36]. Figure4.21 shows the schematic

of the atomic arrangement of GaN surface after mesa etching and with N_2 plasma treatment. The native oxide was removed by dry etch while the nitrogen-vacancy (V_N) was formed near the etched surface. A large amount of V_N was introduced as donor-like traps, resulting in the band bending and the increase of surface state density of the etched GaN[37]. The traps will create a primary path for leakage current along the etched mesa sidewall. During the N_2 plasma treatment on the GaN surface, nitrogen radicals were reacted with Ga atoms and then formed a new Ga-N bond, leading to a reduction of surface defect density and a significant reduction of leakage current.

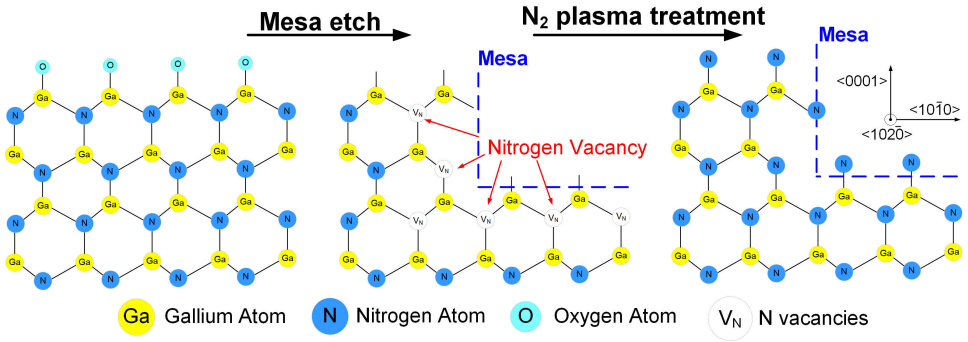


Figure 4.21: Schematic of the atomic arrangement of GaN surface after mesa etch and N_2 plasma treatment.

The fabrication flow of the quasi-vertical GaN SBD with post-mesa nitridation shown in Figure4.22. Firstly, the steep mesa was formed by using SiO_2 mask and a combination of inductively coupled plasma (ICP) dry etch with optimized conditions. Next, N_2 plasma treatment was performed on the mesa for 4 minutes at a pressure of 0.5 Pa and an N_2 flow rate of 80 sccm to reduce the plasma etch damage. Then, the cathode metal Ti/Al/Ni/Au were deposited on the n^+-GaN layer, and annealed at 600℃ for 2 minutes to form ohmic contact. Finally, circular Schottky metal was formed with Ni/Au on n^--GaN drift layer.

Figure4.23 show the forward J-V characteristics in semi-log and linear scale of quasi-vertical SBD with post-mesa nitridation and the reference, both with anode diameter of 100 μm. In Figure4.23a, the quasi-vertical GaN SBD with post-mesa nitridation has shown three orders of magnitude lower leakage current than the reference and a very high on/off current ratio (I_{on}/I_{off}) of 10^{12}. In Fig4.23b, the SBD with post-mesa nitridation has obtained a low specific on-resistance ($R_{on,sp}$) of 0.3 $m\Omega \cdot cm^2$, nearly unity ideality factor (η) of 1.04, low turn-on voltage (V_{on}) of 0.7 V (extracted at 1 A/cm^2), showing much better forward characteristics, compared to the reference. The improved forward characteristics might be attributed to the post-mesa nitridation process, leading to the reduction of sidewall traps or defects, or additional current choke in the access region outside of mesa[8].

Figure4.24ashows the breakdown voltage (BV) characteristics of the GaN SBD with and without post-mesa nitridation at room temperature. The hard-breakdown

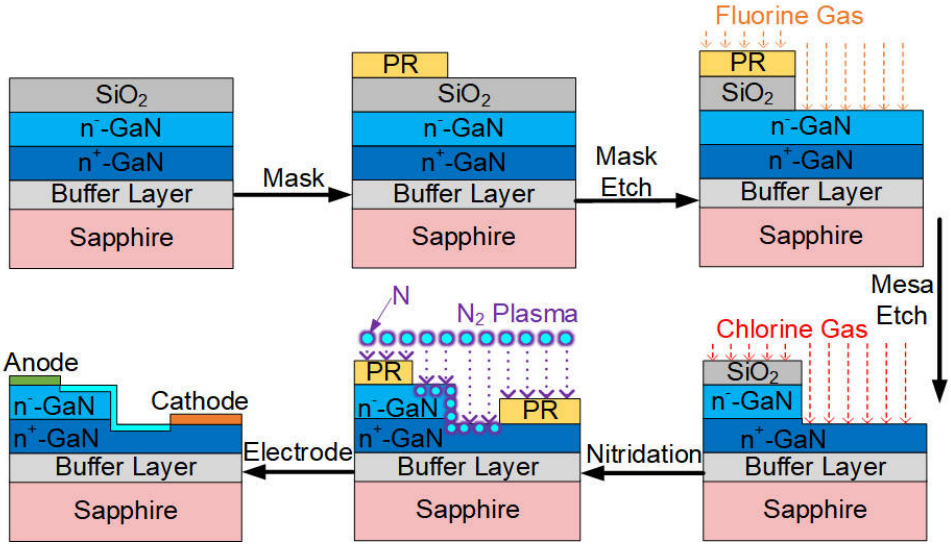
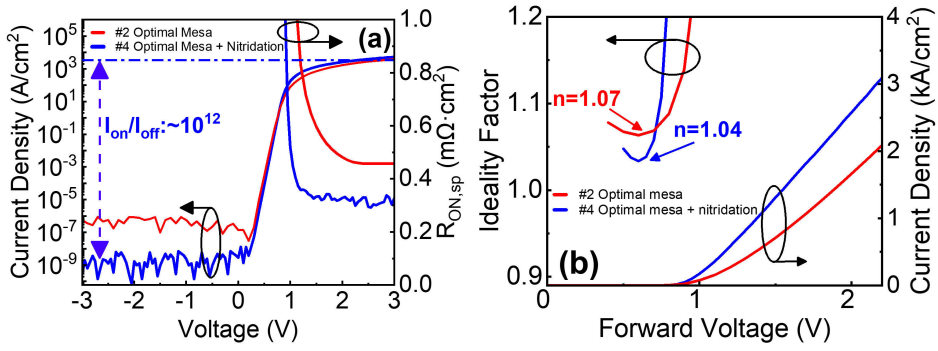
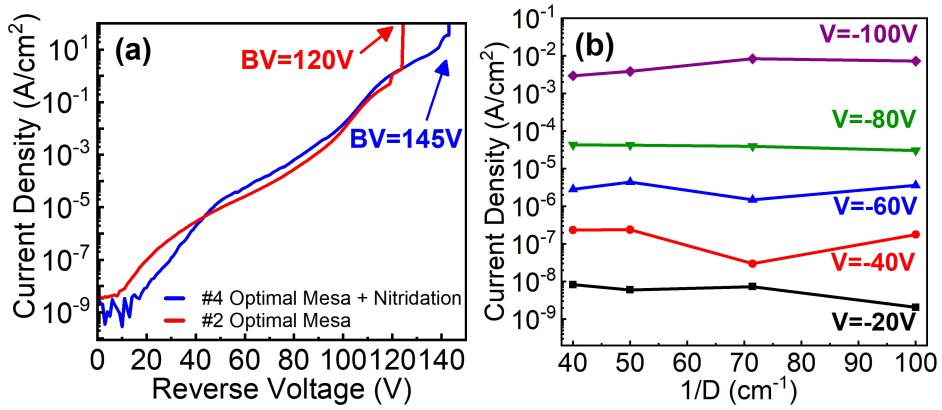


Figure 4.22: Process flows diagram of the quasi-vertical GaN SBD with post-mesa nitridation.



(a) (b)

Figure 4.23: Electrical characteristics of the GaN SBD with post-mesa nitridation and reference with a diameter of 100 μm. Forward J-V characteristics (a) in semi log-scale and $R_{ON,sp}$, and (b) in linear-scale and ideality factor.



(a) (b)

Figure 4.24: (a) Reverse breakdown characteristics of GaN SBD with a diameter of 100 μm. (b) Leakage current density of SBD with post-mesa nitridation for different anode diameters D (D = 100, 140, 200 and 250 μm), as a function of 1/D at a reverse bias of 20, 40, 60, 80, and 100 V.

voltage of SBD with post-mesa nitridation is 145 V. The leakage current density of optimized SBD is $10^{-9} A/cm^2$ at -10 V and $10^{-7} A/cm^2$ at -50 V. On the one hand, leakage current along the sidewall is one of the main leakage path for quasi-vertical GaN SBD, as ICP dry etch might create surface damage (e.g., N vacancies)[38, 39]. The post-mesa nitridation technique has been developed to remove the sidewall damage and reduce leakage. In addition, the slight overlap between the anode and nitridation region helps increase the Schottky barrier height around the anode periphery[36], thus reducing the leakage current. Moreover, the leakage current density, shown in Figure4.24b, is nearly independent of the anode diameters at different reverse bias for the optimized SBD, verifying that the leakage current along the sidewall is well suppressed.

4.5. Performance benchmark

In the session, we benchmark the performance of GaN diodes using various leakage suppression technologies. All the samples use the same epitaxial GaN layer on 2-inch sapphire substrate. The device structure consists of a 2 μm undoped buffer layer, a 3 μm n^+-GaN conducting layer (Si doping: $5 \times 10^{18} cm^{-3}$), and a 1 μm n^--GaN drift layer (Si doping: $1 \times 10^{16} cm^{-3}$). Firstly, the I-V characteristics of GaN diodes with different leakage suppression technology are compared and shown in Figure4.25.

The AIT technology helps the quasi-vertical GaN Schottky diode achieve the highest BV of 146 V among those developed diodes. The specific on-resistance of the diode with AIT has the highest value of 0.71 $m\Omega \cdot cm^2$, attributed to the high-resistivity implantation region near the device periphery. Although the AIT technology effectively enhances the BV of the GaN diode, there are still two apparent flaws: the complex photoresist mask striping process and the degradation

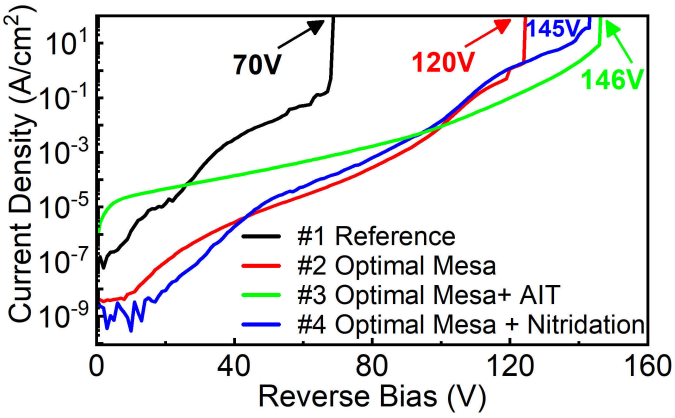


Figure 4.25: Comparison of the reverse I-V characteristics of quasi-vertical GaN-on-Sapphire Schottky diode with different leakage suppression solutions. (The measured diodes have the same anode radius of 50 μm).

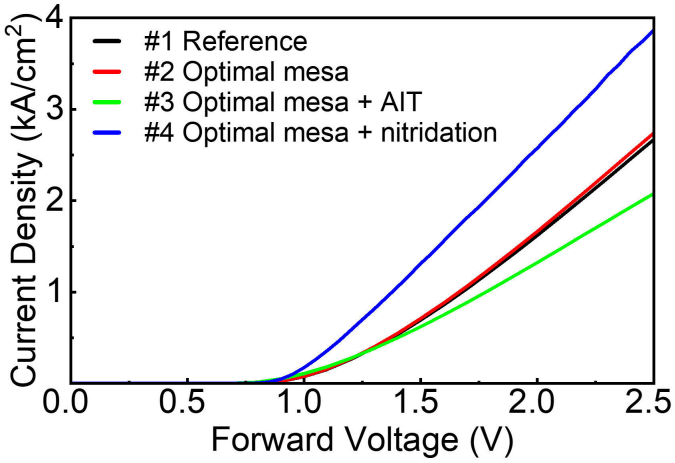


Figure 4.26: Comparison of the forward I-V characteristics of quasi-vertical GaN-on-Sapphire Schottky diode with different leakage suppression solutions. (The measured diodes have the same anode radius of 50 μm).

of on-state resistance. Compared with the AIT technology, a diode used the post-mesa nitridation technology features lower treatment damage and reaches a similar BV of 145V. Meanwhile, the diode with post-mesa nitridation has the lowest $R_{on,sp}$ of 0.3 $m\Omega \cdot cm^2$, benefiting from the compensation of etch-induced N vacancies along the current path.

Mesa optimization technology makes the quasi-vertical GaN diode realize a perfect mesa morphology with steep, micro-trench free, and low-damage sidewalls, enhancing the BV from 70 V to 120 V with a suppression of the edge leakage. However, due to the peak electric field crowding issues near the edge, the GaN diode with optimal mesa has a lower BV of 120 V than with edge termination structure.

Table 4.2: Comparison of performance parameters for a diode with various leakage suppression technologies

Technologies	$R_{on,sp}$ $m\Omega \cdot cm^2$	BV V	V_{on} V	$I_{on/off}$ -	Leakage A/cm^2
Reference	0.45	65-75	0.7	10^{10}	$\sim 10^{-1}$
Optimal Mesa	0.47	120	0.7	10^{12}	$\sim 10^{-3}$
Optimal Mesa +AIT	0.71	146	0.65	10^{8}	$\sim 10^{-1}$
Optimal Mesa + Nitridation	0.3	145	0.7	10^{12}	$\sim 10^{-3}$

$R_{on,sp}$ is the differential specific on-resistance. BV is the breakdown voltage, which is defined as the correspondent voltage when leakage reaches 1 A/cm^2. $I_{on/off}$ is the ON/OFF current ratio from -3 V to 3 V. V_{on} is the turn-on voltage of a diode extracted at 1 A/cm^2. The leakage current density is at 80 % of the BV.

Table4.2 compares the key performance parameters of the diode with different technologies. The fabricated quasi-vertical GaN SBD combined with mesa optimization and post-mesa nitridation technology has achieved a high BV of 145V and a low specific on-resistance ($R_{on,sp}$) of 0.3 $m\Omega \cdot cm^2$, and a high on/off current ratio (I_{on}/I_{off}) of 10^{12}. In order to exhibit the advancement of leakage suppression technology proposed in this work, the GaN diode using post-mesa nitridation technology was selected to compete with the diodes from the latest literature on vertical GaN SBD.

The main objective of diode design is to obtain a high BV while keeping the $R_{on,sp}$ as low as possible. To make a fair comparison, we have selected the diodes in the literature with a similar BV ranging from 100V to 250 V. The benchmark of V_{on} vs. leakage current density and differential $R_{on,sp}$ vs. BV are shown in Figure4.27 and Figure4.28, respectively. Our diode shows the lowest leakage current density at 80% of the BV among the reported vertical GaN SBDs for the BV between 120 V and 250 V[17, 20, 40–42]. A reason for adapting 80% BV is that the devices are generally used below the breakdown. Thus, comparing leakage at 80% of the knee of breakdown (or 80% of voltage rating for actual products) is more reasonable. The performance of our diode is beyond the theoretical limit line of silicon, achieving

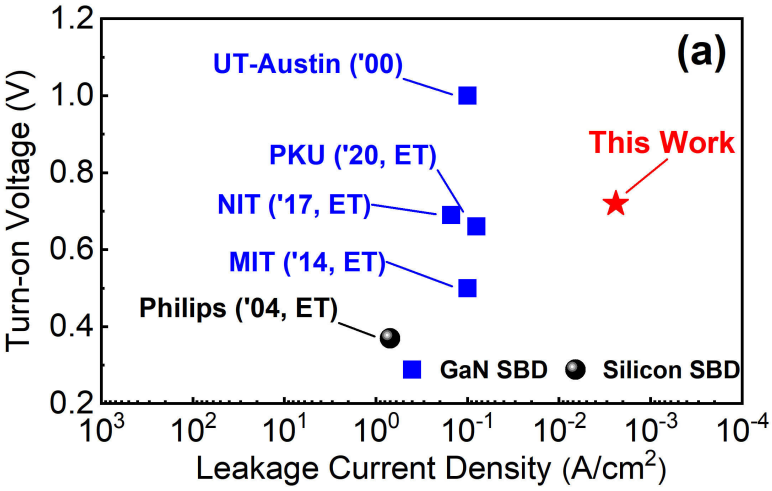


Figure 4.27: Benchmark of V_{on} vs. Leakage current density for vertical GaN SBDs with foreign substrates and silicon SBD for the BV between 120 V and 250 V.

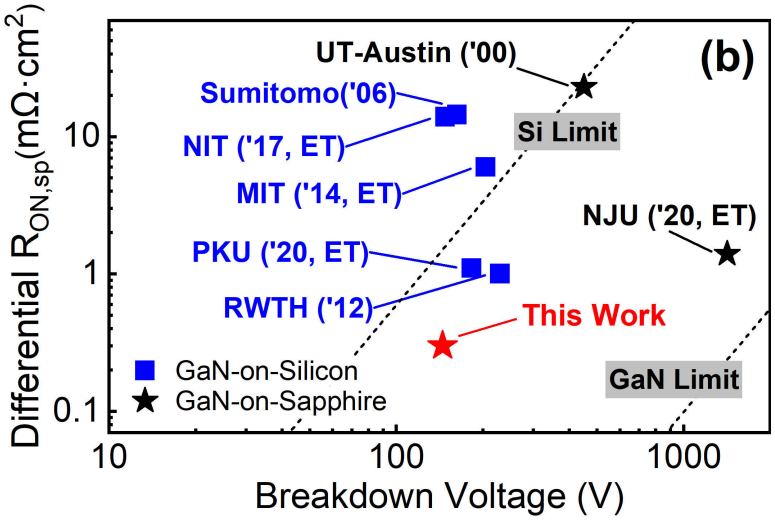


Figure 4.28: Differential $R_{on,sp}$ vs. BV for vertical GaN SBDs with foreign substrates and silicon SBD. ET: Edge Termination.

a BV of 145 V, and a small differential $R_{on,sp}$ of 0.3 $m\Omega cm^2$.

Therefore, using a combination of mesa optimization and post-mesa nitridation technology effectively enhances the breakdown voltage and achieves excellent conduction characteristics. However, the additional processing steps (Argon ion implantation or N_2 plasma treatment) might introduce defects in the device fabrication, resulting in potential reliability problems. There may be uncertainty about whether the proposed AIT and post-mesa nitridation technology in this work can be developed to apply in the industry. Although showing limited benefits, the optimized mesa etching technique is critical to fabricate a quasi-vertical GaN diode, promising for volume production.

4.6. Summary

This chapter discussed the quasi-vertical GaN SBD from the perspective of epilayer structure design, device layout, device modeling, fabrication, and leakage suppression solutions. First, the design flow of quasi-vertical GaN diodes for microwave power applications was presented, including the device performance indicators, substrate selection, and device layout. We adapt the cheaper and available GaN-on-Sapphire wafers, which help us carry out many experiments for the critical fabrication process. Then, the quasi-vertical GaN SBD fabrication process was presented and elaborated in schematic diagrams and reality pictures. One of the critical issues is the large reverse leakage current, which can cause OFF-state power loss and reliability problems. Finally, three solutions were developed to suppress the edge leakage, including mesa optimization, Argon ion terminations, and post-mesa nitridation. The experiment results show that our diode has the lowest leakage current density at 80% of the BV among the reported vertical GaN SBDs for the BV between 120 V and 250 V. Combining mesa optimization and post-mesa nitridation technology effectively enhances the breakdown voltage and achieves excellent conduction characteristics.

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5

Applications of quasi-vertical GaN SBD in microwave circuits

We report the high-performance quasi-vertical GaN Schottky diode on a sapphire substrate and its application for high-power microwave circuits. First, we report the first demonstration of an L-band high-power limiter based on our quasi-vertical GaN SBD in a real-life setting. By using steep-mesa technology, the spacing between the anode and cathode can be reduced to 2 µm, leading to a further reduction in the on-resistance of the SBD. Second, we experimentally demonstrate a quasi-vertical GaN SBD with post-mesa nitridation for high-power and broadband microwave detection. The simulation of the designed circuit and the experimental results can be well corroborated in the circuit applications. The fabricated quasi-vertical GaN diode reached a high forward current density of 9.19 kA/cm^2 at 3 V and BV of 106 V. The GaN SBD limiter can handle at least 40 dBm of CW input power at 2 GHz without failure, which is comparable with the commercial Si-based diode limiter. An extremely high output current of 400 mA is obtained when the detected power reached 38.4 dBm at 3 GHz in pulsed-wave mode.

Parts of this chapter have been published in Electronics **10**, 433 (2021) [1] and Semiconductor Science and Technology **36**, 03LT01 (2021) [2].

5.1. First demonstration of high-power microwave limiters based on quasi-vertical GaN SBD

5.1.1. Introduction

Microwave power limiters have been widely used in the RF front-end in a variety of wireless communication systems[3], such as cellular infrastructure (including 5G) and microwave radio communications[4]. A diode limiter prevents the damage of sensitive receiver components by allowing RF signals below a certain threshold to pass through, but larger signals exceeding the threshold to be attenuated[5]. The development of modern RF receivers requires a high-performance diode limiter[6], which can operate in a wide band-width and high input power level with compactness, easy for integration and low cost.

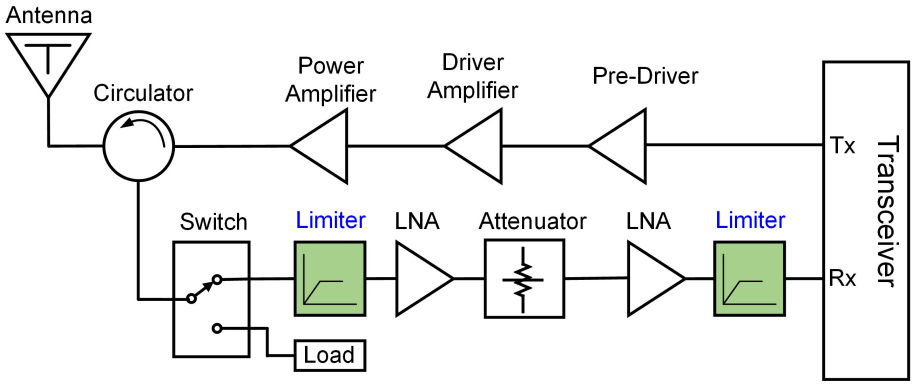
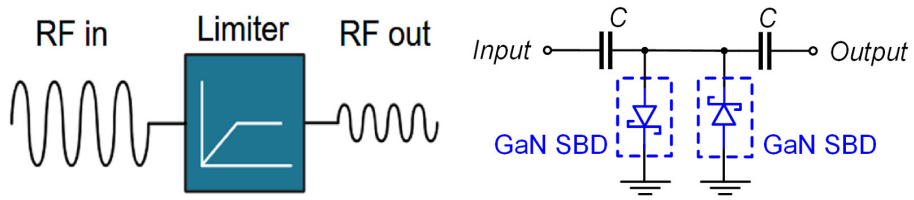


Figure 5.1: A typical radio transceiver block diagram.



(a) (b)

Figure 5.2: (a) The function of microwave power limiter. (b) Circuit schematic of the one-stage anti-parallel diode limiter.

Figure5.1 shows a typical radio transceiver block diagram. The limiter is located at the receiver stage to protect the low noise amplifier (LNA) and transceiver from high-power microwave signal transduced by the antenna. Figure5.2a shows the function of microwave power limiter. Figure5.2b shows the circuit schematic of the one-stage anti-parallel diode limiter. The two capacitors were used as a DC block, not shown in the photograph. The anti-parallel diodes were used to clip

the input large signal symmetrically. For a low input power level, the diodes are both in "off-state". When the input power exceeds the threshold level, the diodes are both in "on-state" and become low impedance, forming a conducting path to ground. Therefore, the peak amplitude of the input power is limited at threshold level to prevent the damage of LNA stage. Table5.1 lists the primary characteristics of commercial diode-based limiters. To make a fair comparison of different diode limiters, we select the same circuit topology with a one-stage anti-parallel structure.

Table 5.1: Comparison of diode limiter products with different semiconductors

Supplier	Number	Material	CW Power Handling	Frequency Band
Skyworks	SKY16602-632LF	Si	12 W	0.2-4 GHz
Qorvo	TGL2209-SM	GaAs	10 W	8-12 GHz

CW: Measured with continuous wave applied at the input.

The silicon-based limiter has higher power handling levels of 12W and a lower frequency band from 0.6 GHz to 6 GHz than the GaAs-based limiter, because of the limitation of material properties among different semiconductors. The carrier mobility and saturated velocity are the two main parameters in a semiconductor, which tells us how fast the carriers move under the externally applied electric field. The carrier mobility is defined as the slope of the velocity versus the electric field. The electron velocity must be high in order for us to achieve a high current.

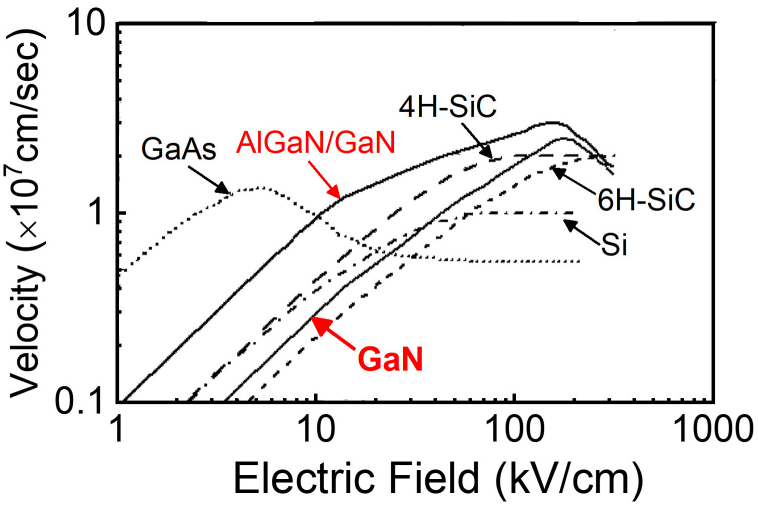


Figure 5.3: Electron velocity versus electric field characte ristics for several semiconductors [7] ($N_d = 10^{17} cm^{-3}$).

As we can see in Figure5.3, the GaAs has a higher electron velocity than others in the low electric field. The electron response fast even if in a low bias, making GaAs a

fantastic material for high-frequency applications. When the electric field applied is much higher, the velocity is become saturation and does not increase by increasing the electric field. GaN has a much higher electron velocity in the high electric field, leading to a higher BV and higher current density of GaN diodes, achieving a high microwave power level. That is why GaN would be an ideal material for high-power microwave devices. However, due to the slow development of GaN material growth technology and several unsolved obstacles in heterojunction AlGaN/GaN structure in the past decades, GaN-based diode limiter is still a gap in the microwave power limiter market.

At present, Silicon-based[8] or GaAs-based[9, 10] diodes have been demonstrated with a high frequency, however, limited with the input power by the low breakdown voltage[11]. As we reviewed in chapter 2, high-performance vertical GaN p-n diodes[12]and SBDs[13] have been demonstrated for high breakdown and good thermal properties. Most of the RF and microwave GaN diodes have been reported on the rectifier[14, 15] and frequency doubler[16]. GaN-based microwave power limiter has rarely been reported up to date.

5.1.2. Design and fabrication of GaN SBD

The epitaxial structure was grown on c-plane Sapphire substrates by metalorganic chemical vapor deposition (MOCVD), consists of buffer layer, 2 μm n^+-GaN conducting layer (N_D: $6 \times 10^{18} cm^{-3}$), and 0.9 μm n^--GaN drift layer (N_D : $9 \times 10^{15} cm^{-3}$). The spacing between anode and cathode (L_{AC}) is varied from 2 μm to 10 μm.

Figure5.4 describes the fabrication steps of vertical GaN SBD. First, the 1 μm mesa was formed by a combination of inductively coupled plasma (ICP) dry etching with Cl_2/BCl_3 gas mixture. Both photoresist (PR) and silicon oxide (SiO_2) hard-mask were employed for mesa etch. The ICP etching conditions were optimized to form a steep-mesa structure with the optimized etching recipes: 360 W ICP power, 42 W RF power, and 100 sccm/10 sccm Cl_2/BCl_3 flow rates. Secondly, the cathode metal (Ti/Al/Ni/Au, 30/120/40/50 nm) was deposited on the bottom of the mesa and annealed in N_2 at 600 ℃ for 1 min to form an ohmic contact. As shown in Figure5.5, a specific contact resistivity as low as $4.06 \times 10^{-6} \Omega \cdot cm^2$ was obtained for cathode metal contacts on n-GaN, extracted from the circular transmission line method (CTLM) measurements.

Then, the Schottky metal (Ni/Au) was formed on n^--GaN layer with a radius of 30 μm. Finally, the SiO_2 passivation layer was deposited by plasma enhanced chemical vapor deposition (PECVD). Figure5.6 shows the cross-section and the top-view SEM image of the fabricated vertical GaN SBD.

5.1.3. Results and discussion

Figure5.7a shows the forward I-V characteristics in the semi-log scale for vertical GaN-on-Sapphire SBDs with various L_{AC}. A high on/off current ratio (I_{on}/I_{off}) of 10^{13}, ideality factor (η) of 1.04, and low turn-on voltage (V_{on}) of 0.7 V (defined at 1 A/cm^2) were extracted from the forward I-V curves of GaN SBDs with various L_{AC}. Figure5.7b shows the forward I-V characteristics in linear scale and $R_{on,sp}$ for

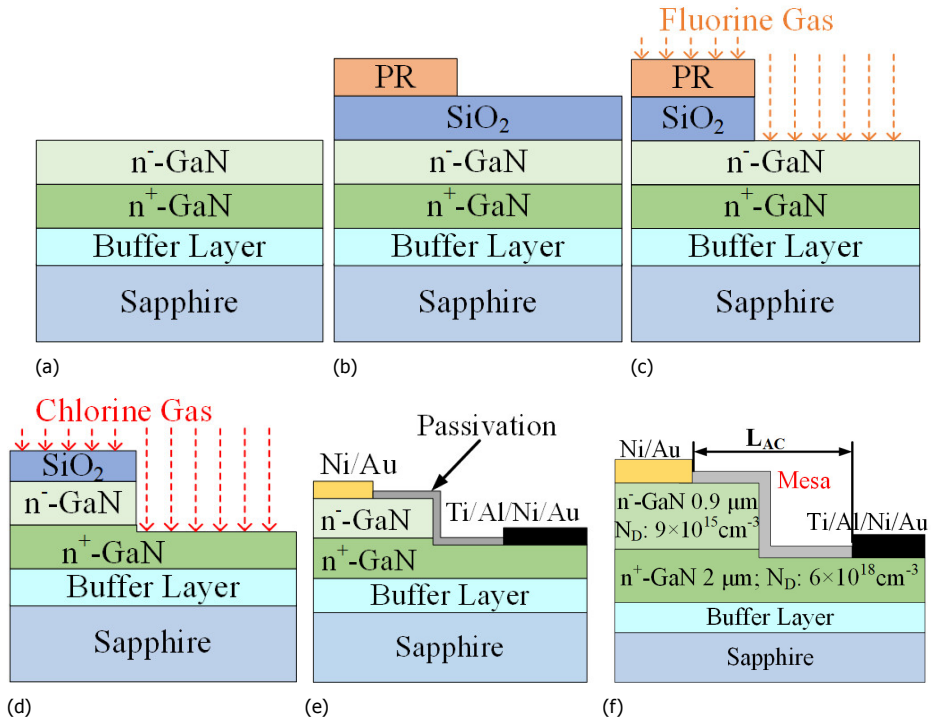


Figure 5.4: Simplified fabrication steps of vertical GaN SBD. (a) Epitaxy structure of vertical GaN SBD on Sapphire substrate; (b) Photoresist (PR) and SiO_2 mask on GaN; (c) Fluorine-based hard mask etching; (d) Chlorine-based mesa etching; (e) Electrode deposition and SiO_2 passivation; (f) Cross-section schematic of the device structure.

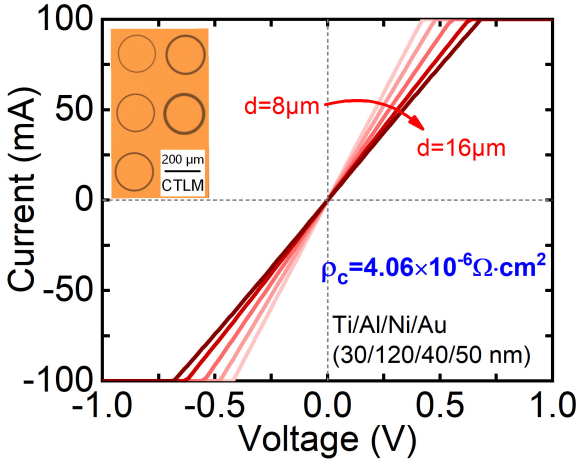


Figure 5.5: The I-V curves of Ti/Al/Ni/Au contact on n^+-GaN as a function of contact spacing, measured from CTLM patterns. The insert is an optical microscopy image of CTLM patterns. The inner radius of the measured pattern was 100 μm with a different spacing of d ($d = 8, 10, 12, 14, 16\mu m$) to the outer ring.

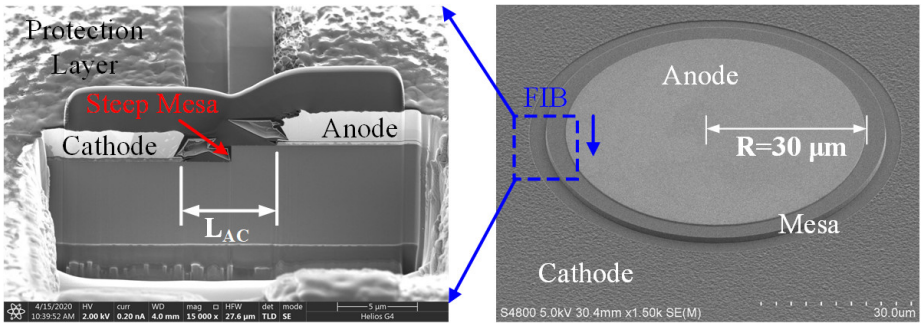


Figure 5.6: (a) Cross-section and (b) top view of SEM image of the vertical GaN-on-Sapphire SBD.

the GaN SBD. The GaN SBD with a small L_{AC} of 2 μm has a high forward current density (defined as the total current divided by the anode area) of 9.4 kA/cm^2 at 3 V and low $R_{on,sp}$ of 0.21 $m\Omega \cdot cm^2$. The differential $R_{on,sp}$ of SBD with a large L_{AC} of 10μm was 1.16 times higher than that with a small L_{AC} of 2 μm, which was attributed to the additional resistance introduced by increasing L_{AC}. A steep-mesa etching technology was expected to form a near-90° mesa structure and added sufficient freedom to reduce the spacing between anode and cathode, enabling a low differential $R_{on,sp}$ in the vertical GaN SBD.

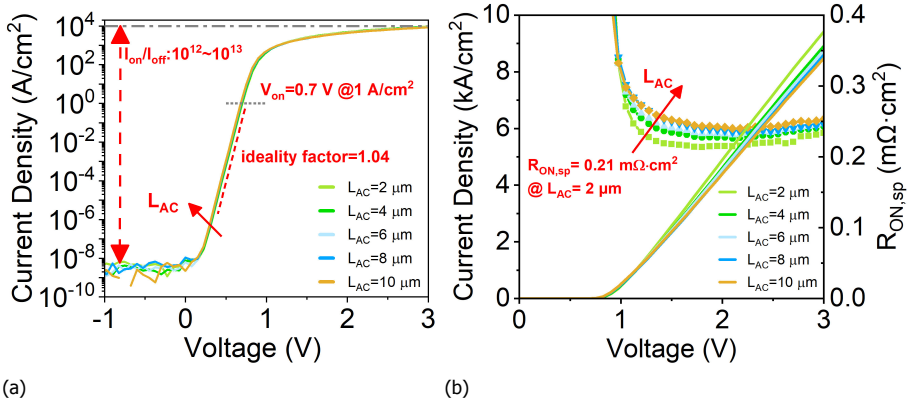


Figure 5.7: (a) Forward I-V characteristics in semi-log scale, and (b) in linear scale (left) and $R_{on,sp}$ vs. voltage (right) for vertical GaN SBDs with different spacing between anode and cathode (L_{AC} = $2, 4, 6, 8, 10\mu m$).

Figure5.8a shows the reverse I-V characteristics of the GaN SBDs with various L_{AC} at room temperature. The GaN SBDs with various L_{AC} show a similar breakdown voltage (BV) of 106 V at 1 A/cm^2 and a similar leakage density of $10^{-8}A/cm^2$ until -30 V. L_{AC} had a minor impact on reverse BV, which can be explained by the electric field distributed mostly in the drift layer. When the reverse bias exceeded 30 V, the leakage behavior showed a variable range-hopping (VRH) process, which could be attributed to the threading dislocation in bulk[17, 18]. Figure5.8b shows the

temperature-dependent I-V characteristics of the SBD, which ranged between 300 and 425 K. With increasing temperature, the current density increases from 300 K (room temperature) to 425 K when the forward voltage is below 1 V, which was attributed to the thermionic emission (TE) behavior. However, the current density decreased with the temperature at a high forward bias (>1 V), mainly attributed to a decrease of electron mobility in the drift region. Thermionic emission behavior can usually be proved by a Richardson plot as follows[19, 20]:

$$\ln J_s / T^2 = \ln A^* - \frac{q\varphi_{B0}}{KT} \tag{5.1}$$

where J_s, K and A^* are the saturation current density, Boltzmann's constant, and Richardson's constant, respectively. In the inset of Figur5.8b, the Richardson plot of $\ln(J_s / T^2)$ versus $1000/T$ is linear, and the calculated A* is about 26.25 $A\cdot(cm\cdot k)^{-2}$, which are very close to the theoretical value of 26.64 $A\cdot(cm\cdot k)^{-2}$[19]. As a result, the temperature-dependent I-V characteristic of our GaN SBD can be well explained by the TE model.

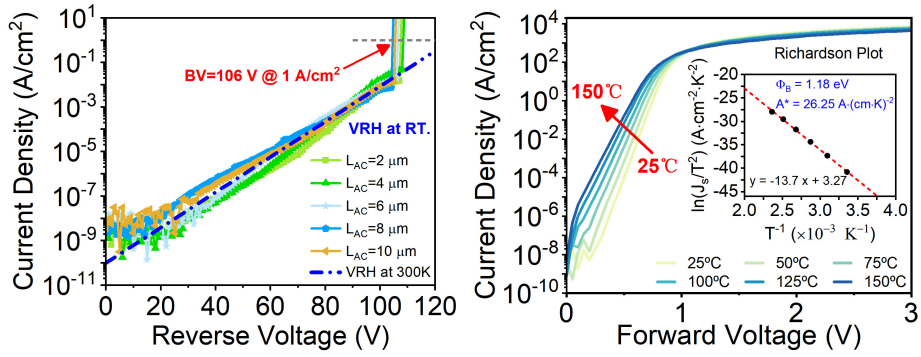


Figure 5.8: (a) Reverse I-V characteristics of the vertical GaN SBDs with various L_{AC}. (b) Temperature-dependent I-V characteristics of the GaN SBD with L_{AC} of 2 μm in semi-log scale at temperatures ranging from 25℃ to 150℃ and corresponding Richardson plot (inset).

A circuit simulation was built for designing the diode-based power limiter and device selection. Figure5.9 shows the schematic of the one-stage anti-parallel diode limiter simulation approach. This study adapted the harmonic balance (HB) analysis technique to analyze large-signal distortion in nonlinear circuits. The capacitance on both sides of the diode blocks the DC components, much like the RF SMA connectors. The simulation was performed under certain source power levels with the source, and load impedance defaulted to 50 Ω. The current probe and voltage test point are located at the output port to calculate the output power. We used the SPICE device model to describe diode electrical characteristics accurately in this simulation. The R_{on}, C_j, I_s, V_{on}, and BV are the essential parameters of a diode SPICE model.

An ideal power limiter has the following characteristics[21]:

$$P_{out} = P_{in}, (when P_{in} < P_{th}) \tag{5.2}$$

$$P_{out} = P_{th}, (when P_{in} > P_{th}) \tag{5.3}$$

where P_{out} is the output power, P_{in} is the input power, and P_{th} is the threshold level. The threshold level is usually defined at the input 1 dB compression point. According to the previous results, the V_{on}, I_s, and BV our GaN SBD are 0.6 - 0.7 V, $1 \times 10^{-12} A$, and 100 - 150 V, respectively. R_{on} and C_j are the primary parameters for optimizing the simulation. The C_j of the diode dominates the insertion loss of the limiter at a low input power, especially for a high-frequency signal. For an ideal limiter, the output power should have no attenuation when a low power signal is incidentally added to the input port. A lower R_{on} of the diode can sufficiently attenuate the output power at a high input power that exceeds the threshold level. In this simulation, the R_{on} and C_j are varied with 1 - 20 Ω and 0.1 - 5 pF, receptively.

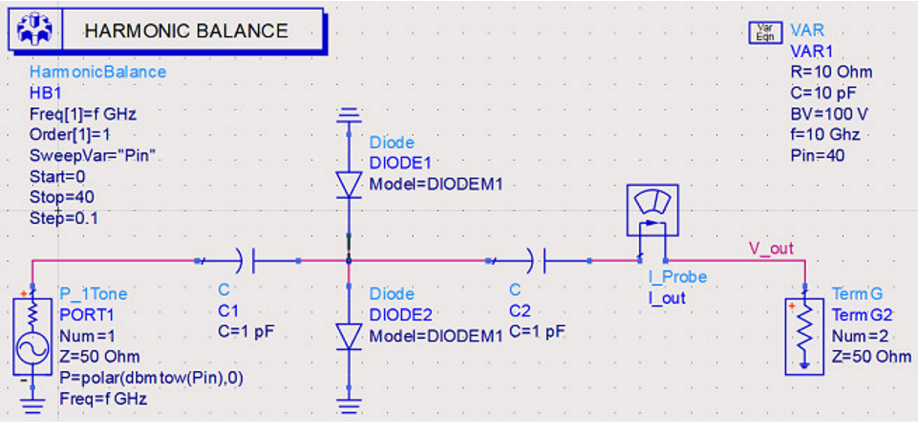
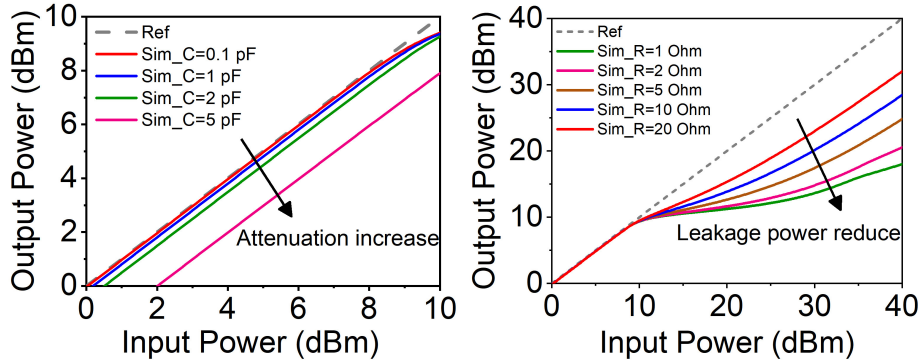


Figure 5.9: Schematic of circuit setup used for the design of one-stage anti-parallel diode limiter.

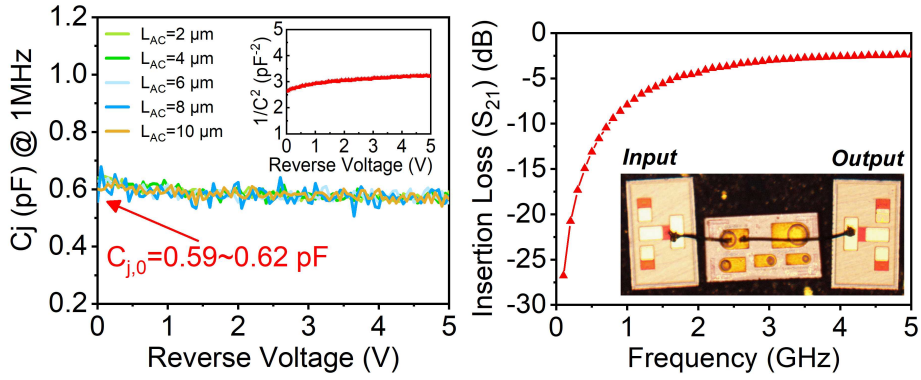
By controlling the primary variable of a diode, the input-output power characteristics of microwave limiter at 2 GHz are shown in Figure5.10.As seen from Figure5.10a, the simulated result shows a low insertion loss of less than 1 dB in a junction capacitance range of 0.1 - 2 pF at 2 GHz with a R_{on} of 10 Ω when P_{in} is below 10 dBm. The C_j of GaN SBD is firstly designed to be less than 2 pF in the simulation. Then, Figure5.10b shows that the leakage power increased with R_{on} when P_{in} is above the threshold level (>10 dBm). Therefore, to satisfy the requirement of a diode limiter operating at L-band (1 - 2 GHz) and with a low leakage power, the target of a diode is designed to reach a low R_{on} possible with a capacitance of below 2 pF.

Figure5.11a shows the junction capacitance of the GaN SBD varied with the applied reverse voltage from 0 V to 5 V at a measurement frequency of 1 MHz. The junction capacitance ($C_{j,0}$) at zero bias was between 0.59 pF and 0.62 pF with various L_{AC}. The extracted $C^{-2} - V$ plot shows normal linearity, which indicates the



(a) (b)

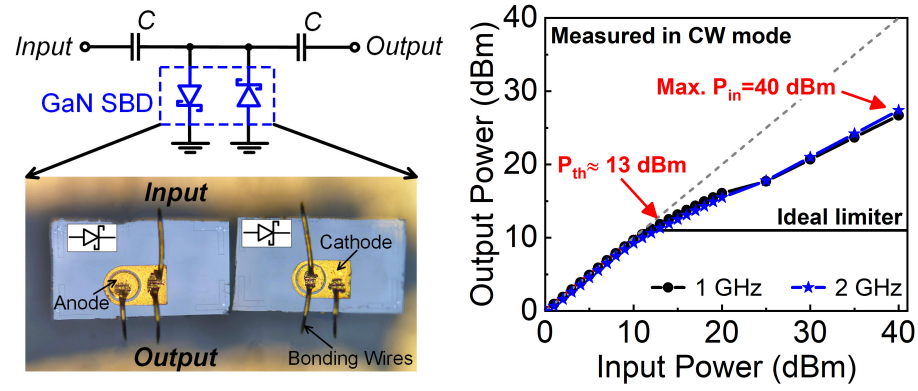
Figure 5.10: (a) The simulated small-signal transfer curve of the diode limiter as a function of junction capacitance. (b) The simulated large-signal transfer curve of the diode limiter as a function of on-resistance.



(a) (b)

Figure 5.11: (a) C-V characteristics of the GaN SBD at a measurement frequency of 1 MHz with an anode radius of 30 μm and different L_{AC} of 2, 4, 6, 8, and 10 μm. Inset is the corresponding $C^{-2} - V$ plot. (b) Insertion loss (S21) of the GaN SBD over a frequency range of 0.1 GHz to 5 GHz in the small-signal S-parameter measurements. Inset is the wire-bonded GaN SBD with two GSG test fixture modules.

relatively uniform net donor concentration along the depth direction. Figure5.11b shows the transmission characteristics of the GaN SBD with a L_{AC} of 2 μm over a frequency range of 0.1-5 GHz. The inset figure shows that the anode and cathode were wire-bonded to co-planar transmission line test fixtures. The measured results showed that the insertion loss (S21) was lower than -3 dB from 0.1 GHz to 3 GHz when the diode was in an off-state. The insertion loss increased with increasing input frequency, which was attributed to the off-state junction capacitance of the GaN SBD[22].



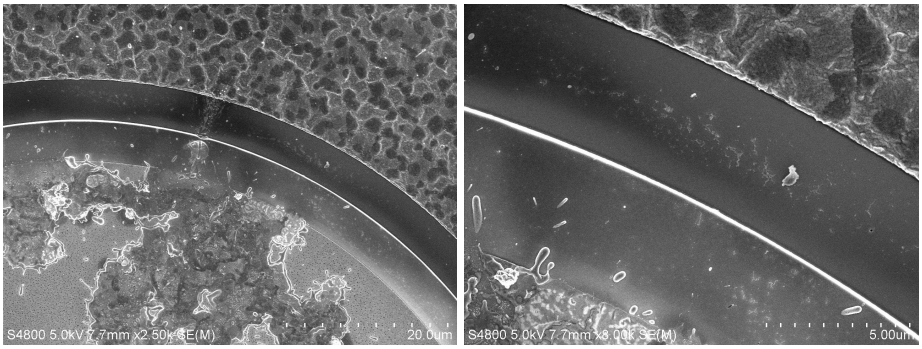
(a) (b)

Figure 5.12: (a) Circuit schematic and microscope image of the one-stage anti-parallel diode limiter using the wire-bonded GaN SBD. (b) Output power versus input power for the GaN SBD limiter at 1 GHz and 2 GHz.

Therefore, the fabricated GaN SBD with a L_{AC} of 2 μm has a differential R_{on} of 8 Ω and $C_{j,0}$ of 0.6 pF was selected and assembled to the limiter circuit. Figure5.12a shows the circuit schematic and a photograph of the one-stage anti-parallel diode limiter using the wire-bonded vertical GaN SBD. The microwave power limiter circuit with an anti-parallel diode was measured on an alumina substrate.

Figure5.12b presents the input and output characteristics of the ideal limiter and our GaN SBD limiter. The input power was increased from low power (0 dBm) to high power in CW mode at a frequency of 1 GHz and 2 GHz. The measured results showed a limiting threshold level (or input 1-dB compression point) of 13 dBm. The limiter had a negligible loss when the input power was below 13 dBm at 1 GHz and 2 GHz, which we attributed to the low junction capacitance of our GaN SBD. The leakage power was 16.7 dBm and 27.4 dBm when the input power was 20 dBm and 40 dBm at 2 GHz, respectively. The GaN SBD limiter can handle at least 40 dBm of CW input power at 2 GHz without failure. As the results of simulation accord with the experimental data whereby the circuit simulation is essential to the design of limiter and diode selection.

When the input power was beyond the maximum power, the SBD suffered a catastrophic failure due to a self-heating problem. Figure5.13 visually shows the local SEM image of the failure diode after a high-power microwave signal (>40 dBm)



(a) (b)

Figure 5.13: The local SEM image of burnout area for a failure diode after the high-power microwave signal is injected. (a) The damage appears mainly in the anode region above the mesa. (b) The cathode and mesa region are not be destroyed.

is inputted. The anode electrode region above the mesa was destroyed, and the damaged region has extended to the inside of GaN material. This observation is in agreement with the Silicon-based diode limiter reported by Zhao, J. et al. [23]. In addition, we monitored the surface temperature of the diode during the test process through the thermal imaging temperature measurement technology and observed a very high temperature of 175 ℃ - 193 ℃ when the diode is about to fail. Consequently, we conclude that the cause of the limiter failure is due to the accumulation of heat, causing surface temperature over high.

5.1.4. Outlook

To further improve the performance of the GaN SBD limiter, four aspects should be addressed:

First, the junction capacitance (C_j) of the diode dominates the insertion loss of the limiter at a low input power, especially for a high-frequency signal. Stacking multiple diodes can reduce the total capacitance but increase the threshold level of the diode limiter. The C_j of a GaN SBD can be reduced by decreasing the doping level of the drift layer, increasing the width of the drift layer, or reducing the Schottky contact area; however, this leads to an increase of R_{on}.

Second, a lower R_{on} of the diode can sufficiently attenuate the output power at a high input power that exceeds the threshold level. For the vertical GaN SBD, a high doping level or thin drift layer result in a low R_{on}, but with a low breakdown voltage (BV). Diodes with a low R_{on} and a high BV can be achieved by improving the crystal quality of the GaN, owing to its high electron mobility and low dislocation density in drift region.

Third, improving the heat dissipation of the GaN diode enhances the power-handling capability of the GaN diode limiter. Advanced thermal management methods are required to cool the GaN SBD, such as using a high thermal conductivity substrate (SiC and diamond) or removing the foreign substrate (sapphire and silicon).

Finally, a multi-stage limiter based on GaN PiN diodes and GaN SBDs can reduce the leakage power and adjust the threshold level[24]. Monolithic and microwave integrated circuits (MMICs) offer the possibility of integrating the multi-stage diode limiter, enabling better limiting performance with high power handling at a high-frequency band.

5.2. Microwave power detector based on quasi-vertical GaN SBD

5.2.1. Introduction

Schottky diodes are widely used in frequency conversion applications, such as rectifiers, detectors, and mixers. The diode detectors utilize high-frequency diodes to detect the RF power, mainly used for transmitter output power measurement and control[25].

In the PIN diode based quasi-active microwave limiter, an SBD based power detector is often utilized to generate bias current for PIN diode to lower the limiting threshold[26–29]. Figure5.14 illustrates a typical circuit schematic of a quasi-active PIN power limiter using SBD[1]. The threshold level of the limiter circuit can be lowered arbitrarily by adding a branch with a Schottky detector diode to the circuit. The Schottky diode is used as a peak detector and coupled to the output of the limiter circuit.

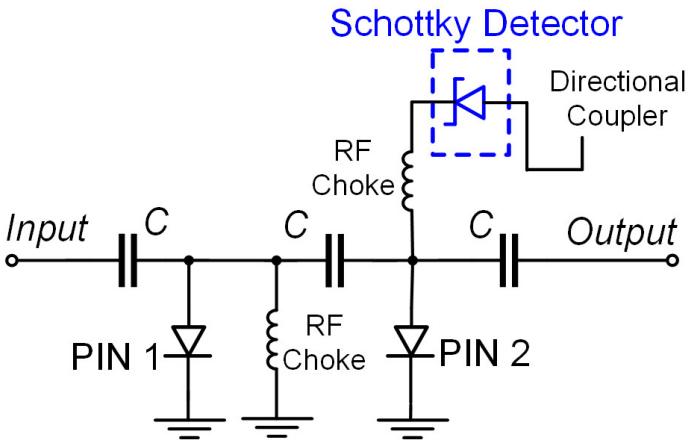


Figure 5.14: A typical circuit schematic of a quasi-active PIN power limiter using an SBD detector.

A high power and high output current microwave SBD is required to reach a high detection power. Silicon-based or GaAs-based SBD detectors have been demonstrated with high sensitivity for microwave power detection at high frequency, however, limited with microwave detectable power level, due to the low breakdown field strength of Si or GaAs[8–11]. On the other hand, GaN SBD is a promising candidate

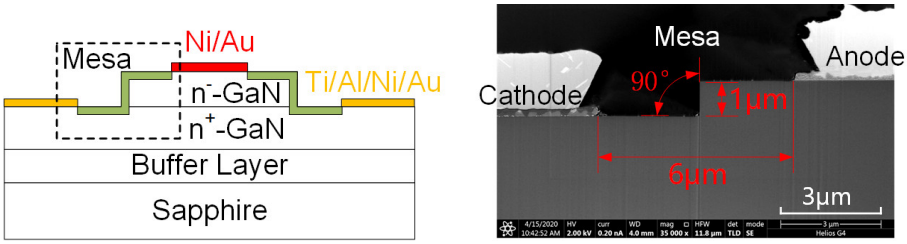
[1]https://www.skyworksinc.com/-/media/SkyWorks/Documents/Products/1-100/200480C.pdf

to improve the microwave detection power. Lateral GaN SBDs have been reported on the rectifying circuit but limited by cost and difficulty for mass production[30].

In this section, we have demonstrated a quasi-vertical GaN SBD with a very high forward current, assisting in increasing the detectable microwave power.

5.2.2. Design and fabrication of GaN SBD

The GaN epi structure was grown on a c-plane sapphire substrate and consisted of a 3 μm buffer layer, 2.5 μm n^+-GaN conducting layer ($N_D : 1 \times 10^{18} cm^{-3}$), and 0.7 μm n^--GaN drift layer ($N_D : 1 \times 10^{16} cm^{-3}$). The followed fabrication process is the same as the previously developed procedures in Chapter 4. In this study, we used the post-mesa nitridation technique to improve the BV of a diode. N_2 plasma treatment was carried out for 4 minutes in a plasma-enhanced chemical vapor deposition (PECVD) system. Figure5.15a and 5.15b show the quasi-vertical GaN SBD schematic diagram and the FIB photograph that zooms on the device mesa structure, respectively.



(a) (b)

Figure 5.15: (a) Schematic diagram of quasi-vertical GaN SBD, and (b) FIB photograph which zooms on the device mesa structure.

5.2.3. Results and discussion

Figure5.15a shows the forward J-V in semi-log scale (left) and specific differential on-resistance ($R_{on,sp}$) in linear scale (right) of quasi-vertical GaN SBD with an anode diameter of 70 μm. The diode has reached a record of forward current density of 9.19 kA/cm^2 at 3 V. Meanwhile, a low $R_{on,sp}$ of 0.22 $m\Omega \cdot cm^2$, forward voltage (V_F) of 0.76 V at 1 A/cm^2, and nearly unity ideality factor (η) of 1.04 has been obtained, showing a better forward performance. Figure5.15b shows the reverse characteristics at room temperature. The diode demonstrates a higher breakdown voltage of 106 V, which is defined at 1 A/cm^2. According to the explanation in Chapter 4, the improved forward characteristics might be attributed to the post-mesa nitridation technique, leading to the reduction of sidewall traps or defects or additional current choke in the access region outside of the mesa.

A typical circuit schematic of a microwave power detector is shown in Figure5.17a. The fabricated GaN SBD was wire-bonded in the circuit, as shown in Figure5.17b. It consists of a microwave source, inductor, GaN SBD, capacitor, and load resistor. The inductor L is shunted with microwave source, providing the DC

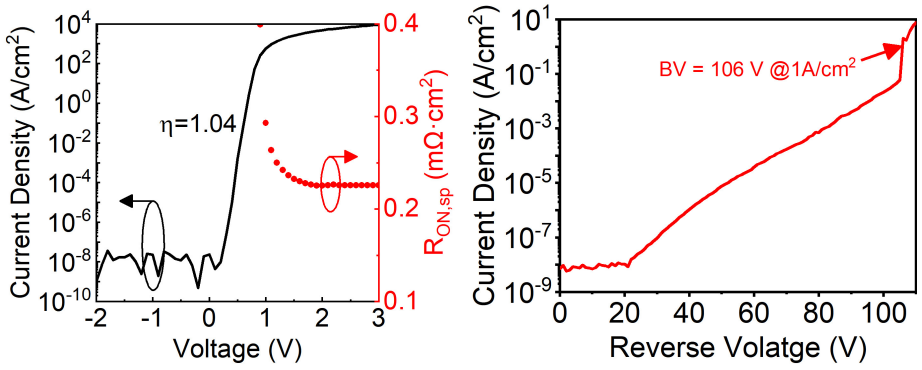


Figure 5.16: (a) Measured forward J-V (left) and $R_{on,sp}$ (right), and (b) reverse J-V characteristics of quasi-vertical GaN SBD with an anode radius of 35 μm.

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return path to ensure all the AC components appear across the SBD terminal. The capacitor C is shunted with a load resistor, yielding a DC output and keeping the DC components from high-frequency harmonics. The output current was measured using the amperemeter with a load impedance (R_L) of 1 Ω. We built a circuit simulation for designing the detector, as shown in Figure5.18. The input power signal is operated in continue wave (CW) mode.

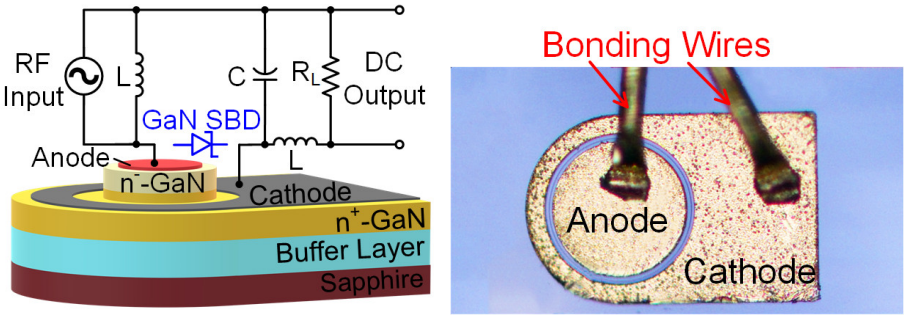


Figure 5.17: (a) Schematic of the microwave power detector with GaN SBD. (b) Photograph of GaN SBD with bonding wires.

The C-V characteristics were measured with the applied reverse voltage from 0 V to 5 V at a measurement frequency of 1 MHz. The junction capacitance ($C_{j,0}$) at zero bias is 0.73 pF. Therefore, the cut-off frequency (f_T) of GaN SBD is 36.9 GHz, calculated with the formula $f \approx (2\pi R_s C_{j,0})^{-1}$. A simple diode SPICE model with the key parameters was extracted from I-V and C-V curves for simulation. In this case, the V_{on}, I_s, R_{on}, $C_{j,0}$ and BV of our GaN SBD used for detector are 0.76 V, $1 \times 10^{-11} A$, and 5.9 Ω, 0.73 pF, and 104V, respectively. All the diode SPICE parameters are taken to the circuit model, and the simulation results are shown in

Figure5.19b.

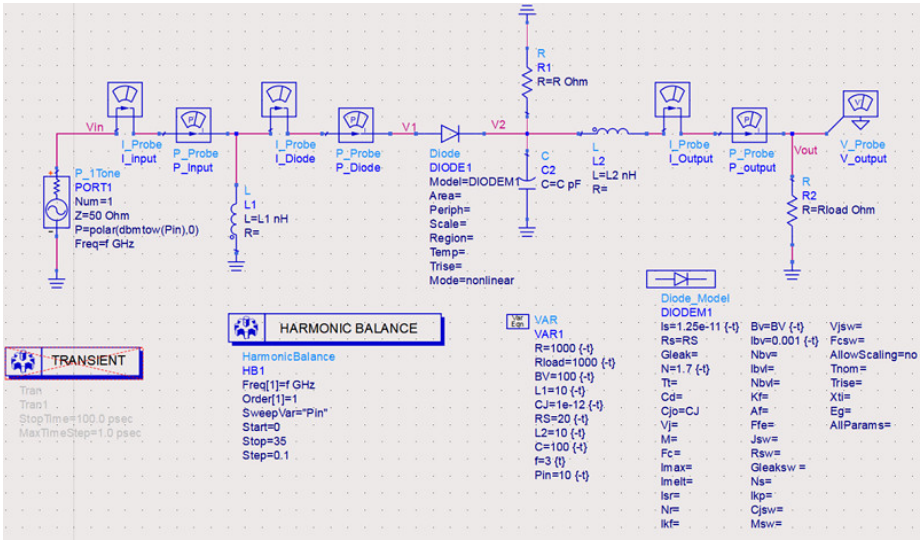
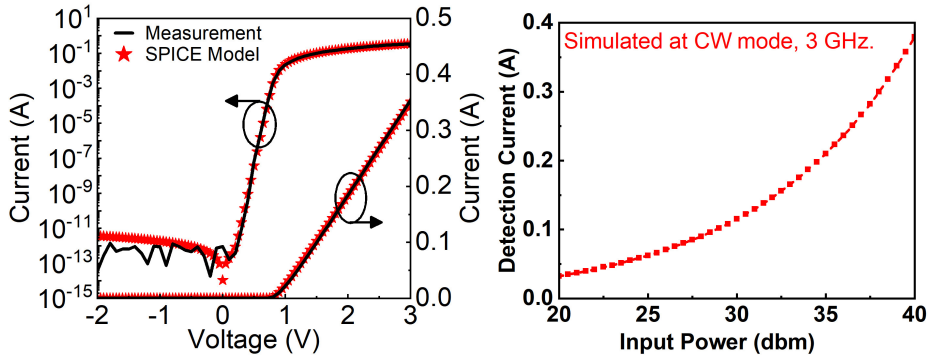


Figure 5.18: Schematic of the diode detector circuit model using ADS simulation.



(a) (b)

Figure 5.19: (a) Measured and simulated forward I-V characteristic in semi-log scale (left) and in linear scale (right). (b) Simulated transfer characteristics of detector circuit using our diode SPICE model.

In the detector circuit simulation, the input power varies from 20 dBm to 40 dBm at a frequency of 3 GHz. Figure5.19b illustrates the simulated result that the detector has a maximum output current of 0.37 A at an input power of 40 dBm (or 10W) in CW mode. Consequently, we measured the assembled detector circuit with our GaN SBD in CW and pulsed-wave (PW) mode.

Figure5.20a shows the output current versus P_{in} of the GaN SBD detector at a frequency of 3 GHz in continuous-wave (CW) mode and pulsed-wave mode (PW) mode. In PW mode, a pulsed sinusoidal signal with a duty cycle of 1% and a

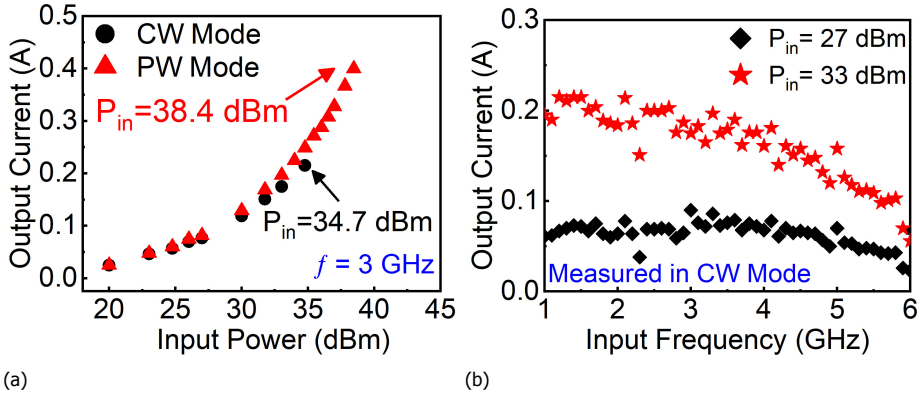


Figure 5.20: (a) The output current as a function of P_{in} at 3 GHz in the CW and PW mode. (b) Output current as a function of input frequency at 27 dBm and 33 dBm in CW mode.

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pulse width of 10 μs. The maximum output current is 210 mA and 400 mA at an input power of 34.7 dBm (CW) and 38.4 dBm (PW), respectively. The simulated result is consistent with the experiment before the diode failure. When the P_{in} is beyond the maximum power, the SBD suffers from catastrophic failure because of self-heating. Therefore, the capability of high-power detection of GaN SBD might be much improved using a high thermal conductive substrate, such as GaN-on-SiC or GaN-on-Diamond.

Figure5.20b shows the output current versus frequency at an input power of 27 dBm and 33 dBm in the CW mode. The output current gradually decreases with increased frequency from 1 GHz to 5 GHz and significantly declines when reaching 6 GHz. The proposed GaN SBD-based detector can generate high output current at high input power in broadband, implying that GaN SBD is a good candidate for PIN-based quasi-active microwave limiter[26].

Table 5.2 lists the characteristics of commercial silicon detector SBDs and our GaN detector SBD. The GaN SBD shows the best performance with the highest detectable power level among all other listed commercial Schottky diodes, attributed to the high electron saturation velocity and high electrical field strength of GaN. Meanwhile, the GaN SBD has shown a higher BV, higher forward current, and lower leakage current. In the future, the R_S of the diode is expected to be further reduced, which can provide a larger current to the PIN diode and sufficiently attenuate the output power in a high input-power signal that exceeds the threshold level.

5.3. Summary

In this chapter, we reported on a high-performance quasi-vertical GaN Schottky diode and its demonstration in a microwave power limiter for the first time. The fabricated SBD achieved a very low differential specific on-resistance ($R_{on,sp}$) of 0.21 $m\Omega \cdot cm^2$, attributed to the steep-mesa technology, which assists in reducing the spacing between the edge of the anode and cathode to 2 μm. Scattering parameter

Table 5.2: Comparison of performance parameters for a diode with various leakage suppression technologies

Items	This Work	HSMS 2820	BAT62-02V
Material	GaN	Si	Si
BV (V)	**106**	15	40
$C_{j,0}$ (pF)	0.73	0.7	0.35
R_S (Ω)	5.9	6	-
I_m (mA)	340	-	20
V_F (V)	0.76	0.34	0.44
I_s (A)	2E-13	2.2E-8	-
η	1.04	1.08	-
CW P_{in} (dBm)	33 @6 GHz	30 @0.9 GHz	15 @5.5 GHz
PW Pin (dBm)	38.4 @3 GHz	-	-

BV = breakdown voltage, $C_{j,0}$ = junction capacitance at zero bias, R_S = series resistance, which is equal to the on-resistance (R_{on}) in a diode; I_{max} = maximum forward current, V_F = forward voltage at 1 mA or the turn-on voltage (V_{on}) in a diode; I_s = reverse saturation current, η = ideality factor, CW P_{in} = incident power in continuous-wave mode at a given maximum frequency. PW P_{in} = incident power in pulsed-wave mode.

measurements showed that the insertion loss (S21) was lower than -3 dB until 3 GHz. A microwave power limiter circuit with two anti-parallel GaN Schottky diodes was built and measured on an alumina substrate. The input power level reached 40 dBm (10 watts) in continuous-wave mode at 2 GHz, with a corresponding leakage power of 27.2 dBm (0.5 watts) at the output port of the limiter.

Second, we have experimentally demonstrated a quasi-vertical GaN SBD with post-mesa nitridation for high power and broadband microwave power detection. The fabricated quasi-vertical GaN diode reached a high forward current density of 9.19 kA/cm^2 at 3 V and BV of 106 V. An extremely high output current of 400 mA is obtained when the detected power reached 38.4 dBm at 3 GHz in pulsed-wave mode. Meanwhile, broadband detection at frequencies ranging from 1-6 GHz was achieved at 33 dBm in continuous-wave mode.

Therefore, the results suggest great potential for high-power microwave application with quasi-vertical GaN SBD.

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6

Conclusions and recommendations

This chapter points out its main work and prospects its future orientation of research.

6.1. Conclusions

Based on the first five chapters, this chapter summarizes the main research and development works.

A **literature summary** of the state-of-the-art vertical GaN SBDs was presented in Chapter 2. The trade-off between the $R_{on,sp}$ and BV of a diode was analyzed to characterize the performance of diodes. We discussed the benchmark of the $R_{on,sp}$ and BV for vertical GaN SBDs with different substrates (Si, Sapphire, and GaN) and various edge terminal techniques. Alongside this, an equivalent circuit model of a diode for studying high-frequency properties was introduced. GaN homoepitaxial has low dislocations and a high crystal quality; thus, a GaN-on-GaN SBD shows a much better performance than a heteroepitaxial SBD. Quasi-vertical GaN SBDs on sapphire and Si substrates have a low voltage rating below 650 V, restricted by the growth of a thick GaN film.

Exploring the **deep and high aspect ratio of trench etching techniques** is critical for fabricating a quasi-vertical GaN SBD. The optimization of mesa etching by inductively coupled plasma (ICP) etching was comprehensively investigated, including the selection of an etching mask, ICP power, radio frequency (RF) power, ratio of mixed gas, flow rate, and chamber pressure. In particular, the microtrench on the bottom corner of the mesa sidewall was eliminated by optimizing the etch recipes. The optimized ICP etching recipe was as follows: 360 W ICP power, 42 W RF power, 118 sccm/12 sccm Cl_2/BCl_3 flow rates, and 1.5 Pa chamber pressure. The etch rate of GaN was near 120 nm/min, and the selectivity of GaN over SiO_2 was 10. For the SiO_2-masked GaN samples, the etch rate of GaN was shown to be dependent on the ICP power, RF power, and ratio of BCl_3/Cl_2 gas flow, but was relatively less dependent on the chamber pressure. The etch selectivity of GaN over SiO_2 decreased with increasing BCl_3 concentration in Cl_2/BCl_3 gas mixture in the range of 0%-40%. The etch selectivity of GaN/SiO_2 could be increased by adjusting the chamber pressure. Moreover, the microtrench problem on the bottom corner of the mesa could be reduced or eliminated by reducing the ICP or RF power or by adding BCl_3 into the Cl_2 plasma. After ICP etching, the use of a TMAH wet treatment for samples could obtain a near-$90°$ steep mesa sidewall that was microtrench-free and had a smooth surface. The proposed etching technique can be extended to other GaN nanostructures, such as hexagonal pyramids and nanowire arrays, and is promising for sensors, vertical transistors, optoelectronics, and photovoltaics.

In this paper, the **design** flow and **fabrication** process of quasi-vertical GaN diodes for microwave power applications were presented. Although limited by its low thermal conductivity, sapphire is still regarded as a potential substrate that could be applied for relatively low-power RF devices. In the early development stage of vertical GaN RF diodes, we adapted cheap and widely available GaN-on-sapphire wafers, which helped us carry out many experiments on the critical fabrication process. According to the device simulation results, we need to make the lateral resistance of the n^+-GaN layer as low as possible so that the CCE issue can be alleviated. Three solutions were developed to suppress the leakage current, namely, mesa optimization, argon ion terminations (AIT), and post-mesa nitrida-

tion. Although AIT technology effectively enhances the BV of GaN diodes, there are still two apparent flaws: The complex photoresist mask striping process and the degradation of on-state resistance. The additional processing steps (argon ion implantation or N_2 plasma treatment) might introduce defects in the device fabrication, resulting in potential reliability problems. The experimental results showed that our diode has the lowest leakage current density, at 80% of the BV, among the reported vertical GaN SBDs for a BV between 120 and 250 V. Combining mesa optimization and post-mesa nitridation technology effectively enhances the breakdown voltage and helps to achieve excellent conduction characteristics. There may be uncertainty about whether the AIT and post-mesa nitridation technology proposed in this work can be developed for applications in industry. Despite the optimized mesa etching technology showing limited benefit, it is still critical to fabricate a quasi-vertical GaN diode that is promising for volume production.

We proposed a high-performance quasi-vertical GaN Schottky diode on a sapphire substrate and discussed its **applications** for high-power microwave circuits. First, we reported the first ever demonstration of an L-band high-power limiter based on our quasi-vertical GaN SBD. A microwave power limiter circuit with two anti-parallel GaN Schottky diodes was built and measured on an alumina substrate. The measured results showed a limiting threshold level (or input of a 1 dB compression point) of 13 dBm. The limiter had a negligible loss when the input power was below 13 dBm at 1 and 2 GHz, which we attributed to the low junction capacitance of our GaN SBD. The GaN SBD limiter can handle at least 40 dBm of CW input power at 2 GHz without failure. The results suggest the great potential of high-power microwave power limiters using a GaN SBD. Second, we experimentally demonstrated a quasi-vertical GaN SBD with post-mesa nitridation for high-power and broadband microwave detection. The fabricated quasi-vertical GaN diode reached a high forward current density of 9.19 kA/cm^2 at 3 V and a BV of 106 V. An extremely high output current of 400 mA was obtained when the detected power reached 38.4 dBm at 3 GHz in pulsed-wave mode with a small anode radius of 35 μm. Meanwhile, broadband detection at frequencies ranging from 1 to 6 GHz was achieved at 33 dBm in continuous-wave mode. These demonstrations are the beginning of a very promising future for quasi-vertical GaN diodes in high-power microwave applications.

6.2. Recommendations

The recommendations of this study are based on a summary of the research results in this thesis. While this work has made advancements, it is still far from perfect and needs further improvement.

GaN drift layer: The drift layer requires a high electron mobility to reach a low series resistance (R_s) under a specific blocking voltage in a vertical device. In RF and microwave applications, a low R_s of a diode helps to operate in a wide frequency band, according to the equation $f_T = 1/(2\pi RC)$. In addition, the carrier density needs to be kept as low as possible ($<10^{16} cm^3$) to reach a relatively high BV. Therefore, the GaN drift layer is expected to reach high electron mobility (>1090 $cm^2/V \cdot s$) and low carrier density.

GaN-on-sapphire: The growth of GaN on a sapphire substrate is a mature technology with a significantly low cost. GaN-on-sapphire devices have the advantage of a low RF loss at high frequencies because of the excellent insulation properties of sapphire substrates. However, due to the low thermal conductivity of sapphire, the GaN-on-sapphire solution has historically been dismissed. In the future, with the development of advanced thermal management techniques, GaN-on-sapphire devices will be given more attention with regard to RF applications.

GaN trench etching techniques: This work experimentally illustrated the improvement of mesa etching by optimizing ICP dry etch recipes. However, with the adaptation of a more expensive SiC or diamond substrate in the future, the experimental characterization of GaN etch processes will result in significantly more research and the development of the cycle and cost. A process simulator used for the high-density plasma etching of GaN needs to be created in the future.

Edge termination structure: According to the benchmark for vertical GaN diodes (discussed in Chapter 2), they do not reach the GaN material limit through adapting different edge termination techniques. The edge termination structure needs to be optimized for vertical GaN devices, which are critical to realizing a high blocking voltage, such as junction barrier Schottky (JBS) with p-type GaN edge terminations.

High-power microwave applications: First and foremost, improving the heat dissipation of GaN diodes helps to enhance the power-handling capability of GaN diode limiters. Advanced thermal management methods are required to cool GaN SBDs, such as using a high-thermal conductivity substrate (SiC and diamond) or removing foreign substrates (sapphire and silicon). Meanwhile, monolithic and microwave integrated circuits (MMICs) offer the possibility of integrating a multi-stage diode limiter, enabling better limiting performance with high power handling in a high-frequency band.

A

Appendix A

Silvaco codes used for simulating the quasi-vertical GaN SBD that are discussed in chapter 4.

```
go atlas

———-Set Variables————

set Thick_i=1
set Thick_n=3
set implant_depth=0.2
set implant_width=5
set Doping_i=1e16
set Doping_n=5e18
set fermi=0.6
set char=0.1
set SA=100
set SC=20
set Gap_A=2
set Gap_B=2
set width=1
```

(In a quasi-vertical GaN SBD, Thick_i and Thick_n are the thickness of drift layer and conduction layer; implant_width and implant_depth are define the region of edge terminations; Doping_i adn Doping_n are the carrier density in n-type drift layer and conduction layer; fermi, char are the trap fermi levels and distribution parameters in the edge termination region; SA, SC, Gap_A and Gap_A are the anode diameter, cathode diameter, space between the edge of anode to mesa, and space between the edge of mesa to cathode, respectively; width is the device width.)

```
———-Define Mesh————
```

```
mesh width=$width
x.m l=0 spac=1
x.m l=1+0.5*$SC spac=1
x.m l=1+$SC spac=0.1
x.m l=1+$SC+$Gap_A spac=0.05
x.m l=1+$SC+$Gap_A+$implant_width spac=0.05
x.m l=1+$SC+$Gap_A+$Gap_B spac=0.05
x.m l=1+$SC+$Gap_A+$Gap_B+0.5*$SA spac=1
y.m l=-0.2 spac=0.1
y.m l=-0.02 spac=0.02
y.m l=0 spac=0.02
y.m l=$implant_depth spac=0.01
y.m l=$Thick_i spac=0.5
y.m l=$Thick_i+$Thick_n spac=0.5
y.m l=$Thick_i+$Thick_n+2 spac=1

———-Define Region————

region num=1 material=air y.min=-1
region num=2 material=GaN x.min=1+$SC+$Gap_A x.max=1+$SC+2*$Gap_B+$SA+$Gap_A
y.min=0 y.max=$Thick_i
region num=3 material=GaN y.min=$Thick_i y.max=$Thick_i+$Thick_n
region num=4 material=GaN x.min=1+$SC+$Gap_A x.max=1+$SC+$Gap_A+$implant_width
y.min=0 y.max=$implant_depth
region num=5 material=Sapphire y.min=$Thick_i+$Thick_n y.max=$Thick_i+$Thick_n+5
elec name=anode x.min=1+$SC+$Gap_A+$Gap_B x.max=1+$SC+$Gap_A+$Gap_B+$SA
y.min=-0.2 y.max=0
elec name=cathode x.min=1 x.max=1+$SC y.min=$Thick_i-0.3 y.max=$Thick_i

———-Doping Profile of Region————

doping region=2 uniform conc=$Doping_i n.type
doping region=3 uniform conc=$Doping_n n.type
doping region=4 uniform conc=$Doping_i n.type

doping region=4 gaussian conc=$Doping_d peak=0 characteristic=0.3*$implant_depth
trap acceptor e.level=$fermi degen.fac=1 sign=1e-16 sigp=1e-16 (used for mod-
eling Argon implantation terminations)
———-Model————

model srh auger print temperature=300
contact name=anode workf=5.1 SURF.REC E.TUNNEL
impact selb
mobility material=GaN chen.p gansat.p (used for modeling Current Crowding Effect
(CCE) in a quasi-vertical diode)
```

output e.field con.band val.band band.para flowlines e.lines e.mobility e.velocity impact charge traps traps.FT
method newton dvmax=1e8 climit=1.e-5
save outf=SBD.str

———-*IV Characteristics*————

log outf=IV.log
solve init
save outf=V_0V.str
solve previous
solve vanode=-0 vstep=-2 name=anode vfinal=-120
save outf=V_-120V.str *(will be adjusted according to the requirements)*
log off
quit

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List of Publications

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7. **Y. Sun**, X. Kang, Y. Zheng, J. Lu, X. Tian, K. Wei, H. Wu, W. Wang, X. Liu, and G. Zhang, *Review of the Recent Progress on GaN-Based Vertical Power Schottky Barrier Diodes (SBDs)*, Electronics **8**, 575 (2019)..

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