Screen Printed Fire-Through Contact Formation for Polysilicon-Passivated Contacts and Phosphorus-Diffused Contacts

Chaudhary, Aditya; Hos, Jan; Lossen, Jan; Huster, Frank; Kopecek, Radovan; van Swaaij, Rene; Zeman, Miro

DOI
10.1109/JPHOTOV.2022.3142135

Publication date
2022

Document Version
Final published version

Published in
IEEE Journal of Photovoltaics

Screen Printed Fire-Through Contact Formation for Polysilicon-Passivated Contacts and Phosphorus-Diffused Contacts

Aditya Chaudhary, Jan Hoß, Jan Lossen, Frank Huster, Radovan Kopecek, René van Swaaij, and Miro Zeman

***Abstract*—In this article, we investigate the passivation quality and electrical contact properties for samples with a 150 nm thick n^+ polysilicon layer in comparison to samples with a phosphorus diffused layer. High level of passivation is achieved for the samples with n^+ polysilicon layer and an interfacial oxide underneath it. The contact properties with screen-printed fire-through silver paste are excellent (no additional recombination from metallization and specific contact resistivity (ρ_c) $\leq$ 2 mΩ·cm^2) for the samples with the polysilicon layers. Fast-firing peak temperature was varied during the contact formation process; this was done to see the trend in the contact properties with the change in the thermal budget. The differences in the $J_{0\mathrm{met}}$ and ρ_c for the two different kinds of samples are explained with the help of high-resolution scanning electron microscope imaging. Finally, we prepare M2-sized n-passivated emitter rear totally (PERT) diffused solar cells with a 150 nm thick n^+ polysilicon based passivated rear contact. The best cell achieved an efficiency of 21.64%, with a V_{oc} of 686 mV and fill factor of 80.2%.**

***Index Terms*—Cross-sectional scanning electron microscope (SEM), metallization, passivated contacts, phosphorus-doped layer, polysilicon, screen printing.**

I. Introduction

INDUSTRIALIZATION of solar cells utilizing polysilicon-based passivated contacts is on the horizon. It is seen as the next step after passivated emitter and rear totally (PERT) diffused cells and passivated emitter and rear cells (PERC). PERT and PERC cells have efficiencies in the range of 21%–22% at the commercial level but still suffer from recombination losses, specifically at the metal-semiconductor interface [1]–[3]. This is the reason for the utilization of the polysilicon-based passivated layers in next-generation cells. Coupled with their compatibility to high-temperature back-end processes in large-scale manufacturing, they are a viable choice for the next evolutionary step in photovoltaics.

For polysilicon/silicon oxide (SiO_x) passivated cells efficiencies of 26.1% have been obtained on interdigitated back contact cells of 3 × 3 cm^2, while for front and back contacted cells an efficiency of 26.0% has been reported on 2 × 2 cm^2 cells [4], [5]. For industrial cells (156.75 × 156.75 cm^2), an average efficiency of 23% and a maximum of 24.6% have been demonstrated [6], [7].

One of the topics to be addressed further in improving the efficiency of the polysilicon-based passivated contact cells is the metal-semiconductor (silver-polysilicon) interface. Excellent contact properties with silver-phosphorus doped (n^+) polysilicon recombination current density of less than 50 fA·cm^{-2} have been reported [8], [9]. Specific contact resistivity below 3 mΩ·cm^2 has also been achieved for polysilicon layers with different thicknesses [8]–[14]. Coupled with the high level of passivation (implied open-circuit voltage (iV_{oc}) $\geq$ 735 mV, recombination current density of the doped region ($J_{0\mathrm{pass}}$) $\leq$ 3 fA·cm^{-2}), the utilization of the polysilicon passivated contacted is expected to increase further [8], [9], [10]. Recent study by Padhamnath *et al.* [8] detailing the impact of firing temperature on metallization for a ∼150 nm thick n^+ doped polysilicon layer shows the variation in specific contact resistivity and metal-semiconductor recombination current density ($J_{0\mathrm{met}}$) with the peak fast-firing temperature [10]. The polysilicon layers used in this work are *ex situ* doped and have a low-pressure chemical vapor deposition (LPCVD)-based thermal oxide below them. This study details the impact of glass layer thickness and the number of silver crystallites on the specific contact resistivity with respect to the fast-firing peak temperature. Here in the method of computation of $J_{0\mathrm{met}}$ utilizes a combination of photoluminescence (PL) images and a finite element simulator, Griddler.

In order to increase the solar-cell performance further, it is important to improve the metallization and understand the interaction of the metal with the silicon layers [5], [7]. For this purpose, it is essential to understand how the metallization of the n^+ polysilicon-based passivated contact differs from a phosphorus-doped silicon layer. In this article, we present a detailed and systematic study to understand the contacting of

Manuscript received August 16, 2021; revised October 15, 2021 and December 1, 2021; accepted January 7, 2022. Date of publication January 21, 2022; date of current version February 19, 2022. This work was supported in part by German Federal Ministry for Economic Affairs and Energy under Contract 0324198A (TuKaN). *(Corresponding author: Aditya Chaudhary.)*

Aditya Chaudhary, Jan Hoß, Jan Lossen, and Radovan Kopecek are with the International Solar Energy Research Center (ISC) Konstanz, 78467 Konstanz, Germany (e-mail: aditya.chaudhary@isc-konstanz.de; jan.hoss@isc-konstanz.de; jan.lossen@isc-konstanz.de; radovan.kopecek@isc-konstanz.de).

Frank Huster is with the Department of Physics, University of Konstanz, 78464 Konstanz, Germany (e-mail: frank.huster@uni-konstanz.de).

René van Swaaij and Miro Zeman are with the Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: r.a.c.m.m.vanswaaij@tudelft.nl; m.zeman@tudelft.nl).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JPHOTOV.2022.3142135.

Digital Object Identifier 10.1109/JPHOTOV.2022.3142135

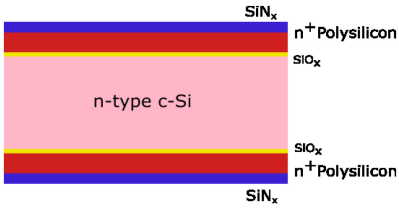


Fig. 1. Schematic representation of the sample type A used in this article.

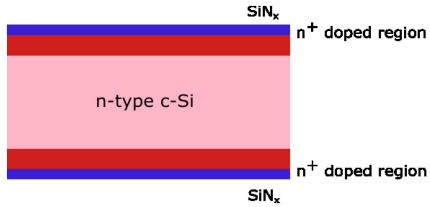


Fig. 2. Schematic representation of the sample type B used in this article.

the n^+ polysilicon/SiO_x based passivated layer stack and of a phosphorus-doped silicon layer. We have utilized our n^+ polysilicon (*in situ* doped) based passivated contact layer stack and phosphorus diffused layer, to study the metallization with a fire-through silver paste. We use a simple method to compute the contact recombination from PL imaging calibrated with the implied V_{oc} (iV_{oc}). High-resolution scanning electron microscope (SEM) images (cross-sectional and surface images) are also used to explain the trends between the contact properties and the fast-firing peak temperature as well as the differences between the metal contacts for the n^+ polysilicon layer and the phosphorus diffused layer.

Furthermore, we prepared M2-sized (156.75 × 156.75 cm^2) nPERT solar cells with rear side n^+ polysilicon-passivated contacts. The champion cell with the n^+ polysilicon-passivated contact achieved an efficiency of 21.64% with a V_{oc} of 686 mV and a fill factor of 80.20%.

II. Experimental

A. Symmetrical Sample Preparation

Two types of symmetrical samples were utilized in this article. Sample type A refers to the sample with n^+ polysilicon layer stacked on top of a ∼1.4 nm thin interfacial oxide layer. Sample type B refers to the one with a phosphorus diffused layer.

Sample type A: We used standard M2 (156.75 by 156.75 cm^2) n-type solar-grade Czochralski wafers (CZ) with a nominal thickness of 180 ± 10 μm and a base resistivity of 1.6 ± 0.3 Ω·cm. The wafers were dipped in a NaOH solution (22%, 80 °C, 500 s) to remove the saw damage. After this, an approximately 1.4 nm thick wet chemical interfacial oxide (nitric acid oxidation of silicon) was grown on the wafers. This was followed by deposition of *in situ* phosphorous-doped silicon layers of 150 nm thickness by LPCVD at a temperature of about 600 °C. To form polysilicon layers by solid-phase crystallization, the samples were annealed at 825 °C for 30 min. The sheet resistance of the layers was ∼90 Ω/sq. A schematic representation of Sample type A is shown in Fig. 1.

Sample type B: For sample type B, we also used M2 n-type CZ silicon wafers (180 ± 10 μm, R_{base} = 1.0 ± 0.2 Ω·cm), which also saw damage etched in NaOH solution. After this, phosphorus was diffused using a diffusion tube with $POCl_3$. This resulted in a doped layer with a sheet resistance of 150 Ω/sq. This was done to replicate the n^+ region in the nPERT cell we utilize. A schematic representation of sample type B is shown in Fig. 2.

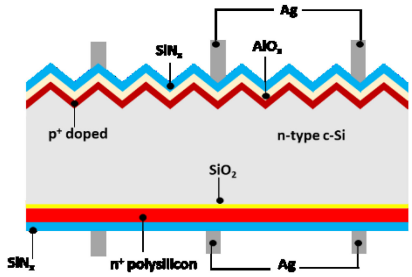


Fig. 3. Schematic representation of the polysilicon/SiO_x passivated cell.

On both sample types, later a silicon nitride layer with a thickness of ∼80 nm was deposited by plasma-enhanced chemical vapor deposition on both sides of the wafers.

An identical fire-through silver paste was used for contacting the two sample types. A high-temperature step is needed to form the metal-semiconductor contact after screen printing. We used a fast-firing furnace, c.FIRE, from Centrotherm International AG for this purpose.

In this experiment, we varied the set point for the zone with the highest temperature, hereafter referred to as fast-firing peak temperature, from 760 °C to 820 °C in steps of 15 °C. The belt speed was kept constant at 3 m/min for this experiment.

B. nPERT Solar Cell With Rear Side n^+ Polysilicon-Passivated Contact

We used our standard techniques for producing M2 nPERT solar cells, which employ homogeneous gas-phase diffusions of front and rear sides as the starting point in order to produce rear side n^+ polysilicon-passivated solar cells. The fabrication process of our standard front and rear side diffused nPERT cells is well explained in literature [15] and [16]. We modified this process to incorporate a 150 nm thick n^+ polysilicon-based passivated contact on the rear side by using LPCVD, a single-side chemical etching process (done in RENA inline wet bench) and a polysilicon etching step to remove the front side polysilicon layer, deposited during LPCVD process. A schematic representation of the cell is shown in Fig. 3. The cells were screen printed with silver fire-through paste and featured 5 bus bars and 100 fingers on both sides.

C. Measurement Techniques

A Sinton WCT-120 lifetime tester was used for the measurement of implied open-circuit voltage (iV_{oc}) for the symmetric samples [17]. The iV_{oc} was measured after silicon nitride deposition and fast-firing in the central unmetallised

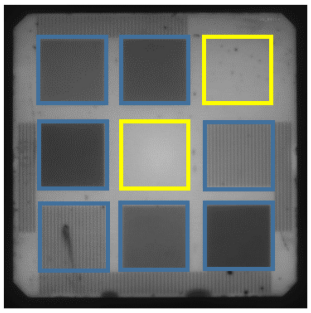


Fig. 4. Example of a PL image with the print pattern of the sample used in this work. The blue boxes show the areas with different finger spacing and the yellow boxes are the unmetallized areas. The fingers at the edges were used for specific contact resistivity measurements.

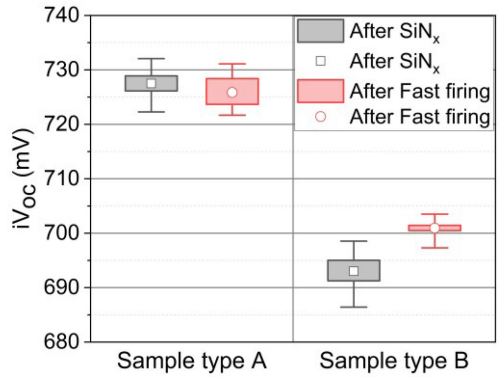


Fig. 5. iV_{oc} (V) values for the two types (25 samples each) of symmetric samples. The measurements were carried out in the center of the samples.

region of the sample. The thickness of the polysilicon layer was measured using spectroscopic ellipsometry with a SENTECH SE 800-PV tool. The thickness measurements were done on separate samples with a thick thermal oxide (∼187 nm) below the polysilicon layer. This was done to have a good fitting in the ellipsometer measurements. We also compared the ellipsometer measurements with polysilicon layer thickness measured from SEM images. Both the measurements were in good agreement with each other. We also performed active dopant profiling (ECV) for the samples using a Wafer profiler CVP 21.

PL images calibrated with the iV_{oc} were used to extract the metal-semiconductor recombination current density (J_{0met}). This was done by plotting the J_{01} as a function of metal fraction and then getting the slope of the linear fit, as described in [9] and [18]. For this purpose, we print a dedicated pattern having different metal line density and record the PL images after contact formation. The central patch is not metallized and is used to measure the iV_{oc} after and before metallization. An example of a sample metallized with this pattern is shown in Fig. 4. In addition to J_{0met}, we also use contact resistivity values to characterize the metal-semiconductor contact. The specific contact resistivity values were determined based on the transmission line measurement (TLM) using a GP 4-Test PRO from GP Solar on equidistant finger of 10 mm length, with finger spacing of 2 mm.

SEM images were done by our project partner – the University of Konstanz using, Zeiss Neon 40 EsB thermal field emission SEM apparatus, at the University of Konstanz. Sequential etch-back using nitric acid and hydrofluoric acid was used to remove the silver and glass frits from the samples. We took SEM images after each etching step to compare the images between the samples. This has been explained in our previous work [9]. To view the metal-semiconductor interface, we did cross-sectional SEM images after milling the metallized fingers. The fingers were ion milled with a Hitachi Ar Blade 5000 (University of Konstanz), using Argon ions to sputter the target. This was done without any chemical treatment.

The IV characteristics of the solar cells were recorded with a H.A.L.M flasher system with hysteresis measurement.

III. Results and Discussion

A. Passivation Quality in Nonmetallized Areas

The passivation quality for the two types of samples (25 samples for each type) is presented in Fig. 5. The implied open-circuit voltage (iV_{oc}) after SiN_x deposition shows that the n^+ polysilicon-based samples have substantially higher passivation quality. The average iV_{oc} for these samples is almost 32 mV higher as compared with the phosphorus diffused samples. Similarly, the recombination current density of the doped region (J_{0pass}) value was almost 25 fA·cm^{-2} less (J_{0pass} for polysilicon samples $\leq$ 8 fA·cm^{-2}). This result is associated with the high level of passivation from the interfacial oxide as well as the field-effect passivation from the highly doped polysilicon layer [14], [19].

After fast firing, the results for the iV_{oc} of the samples are also shown in Fig. 5. The fast-firing process did not lead to a deterioration of the passivation quality of sample type A. For sample type B, fast firing led to an increase in implied V_{oc}. Still, the samples with interfacial oxide and polysilicon have higher iV_{oc} as compared with the phosphorus-doped samples after fast firing.

B. Metallization

In Fig. 6(a) and (b), we present iV_{oc} calibrated PL images for the two sample types fast fired at a peak temperature of 820 °C. The metallized areas appear dark as compared with the unmetallized areas of the samples. It is important to mention that the scale of the implied V_{oc} in the images is different. The difference between the iV_{oc} in metallized patches and the unmetallized patches is due to the additional recombination coming from the metal semiconductor interface. At a lower fast-firing peak temperature of 760 °C, the iV_{oc} drop between the metallized and unmetallized patches becomes negligible for sample type A as shown in Fig. 6(c). This is a fully passivated contact, as irrespective of the metallization and metal fraction, there is no drop in the iV_{oc} after metallization. For sample type B, a drop in iV_{oc} is still present.

Utilizing these iV_{oc} calibrated PL images, J_{0met} values were extracted, as presented in Fig. 7. The J_{0met} values for sample

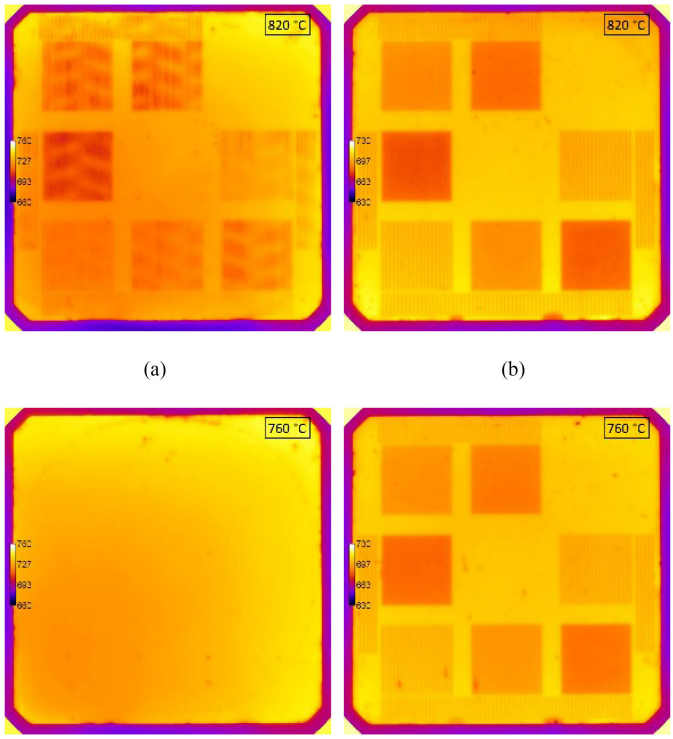


Fig. 6. iV_{oc} calibrated PL images of sample types A and B fast fired at peak temperatures of 820 and 760 °C. The scale for the iV_{oc} is different in the images. (a) Sample type A. (b) Sample type B. (c) Sample type A. (d) Sample type B.

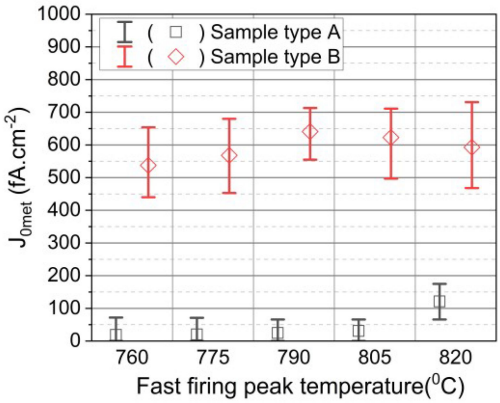


Fig. 7. J_{0met} (fA·cm^{-2}) for the samples, after fast firing at the five different peak temperatures.

type B are higher in the investigated range of fast-firing peak temperature. A small increase in the mean value of J_{0met} occurs when the fast-firing peak temperature is increased from 760 to 820 °C. This figure also shows the uncertainty arising from the inhomogeneity in individual samples due to processing steps, as well as the uncertainty in the extracted values for the four–five samples in a group.

As for sample type A, we obtained J_{0met} of the order of J_{01}, for fast-firing peak temperatures below 820 °C, as shown in the plot with the values approaching zero. Even the J_{0met} of samples fired at 820 °C is below 200 fA·cm^{-2}, which is almost three

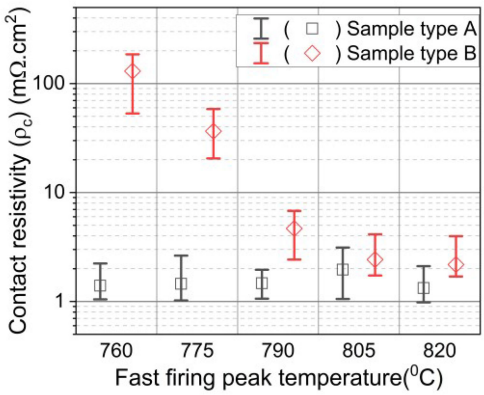


Fig. 8. Contact resistivity (mΩ·cm^2) for the samples, after fast firing at the five different peak temperatures.

times smaller than that for comparable samples of type B. Due to J_{0met} being of the order of J_{01}, the samples fast fired with peak temperatures below 820 °C, with polysilicon/SiO_x layer stack, can be called nearly perfect-passivated contacts.

The specific contact resistivity values are presented in Fig. 8, the mean values remain below 2 mΩ·cm^2 for sample type A throughout the investigated range of fast-firing peak temperatures. The values for sample type B are higher, and they increase with the reduction in fast-firing peak temperature. To understand the contact microstructure for the two types of samples, we took cross-sectional SEM images.

In Fig. 9, the cross-sectional SEM images for sample type A fired at the peak temperature of 760 °C, 790 °C, and 820 °C are presented. We have marked the different components in the images, the bulk silver, glass layer, silver crystallites.

From the images of sample type A, we can conclude that as the fast-firing peak temperature is increased, the number and size of the silver crystallites penetrating the polysilicon layer starts to increase. This could be the reason for the increase in J_{0met} value when the fast-firing peak temperature is increased. As a higher thermal budget is favorable to increased crystallization of silver from the paste, it leads to more sites where silver is in contact with the polysilicon layer. Still, the number of crystallites at 760 °C is enough to provide electrical conductivity (mean $\rho_c \leq$ 2 mΩ·cm^2).

For sample type B, cross-sectional images are also presented in Fig. 9. At 760 °C, there is almost no silver crystallite penetrated into the diffused layer. This corresponds to a situation where the specific contact resistivity goes above 50 mΩ·cm^2, meaning that low resistance electrical contact is not formed at this temperature. Increasing the fast-firing peak temperature from 760 °C to 820 °C leads to an increase in the size of the crystallites as seen in the cross-sectional images. Although the silver crystallites are not as big as seen in the case of sample A, still at 820 °C, the mean specific contact resistivity value for Sample B is close to 2 mΩ·cm^2.

In the samples fired at 820 °C, we marked the length of the silver crystallites penetrating the silicon layer in the samples using an open-source image processing software. For better visualization, we marked the 150 nm nominally thick polysilicon

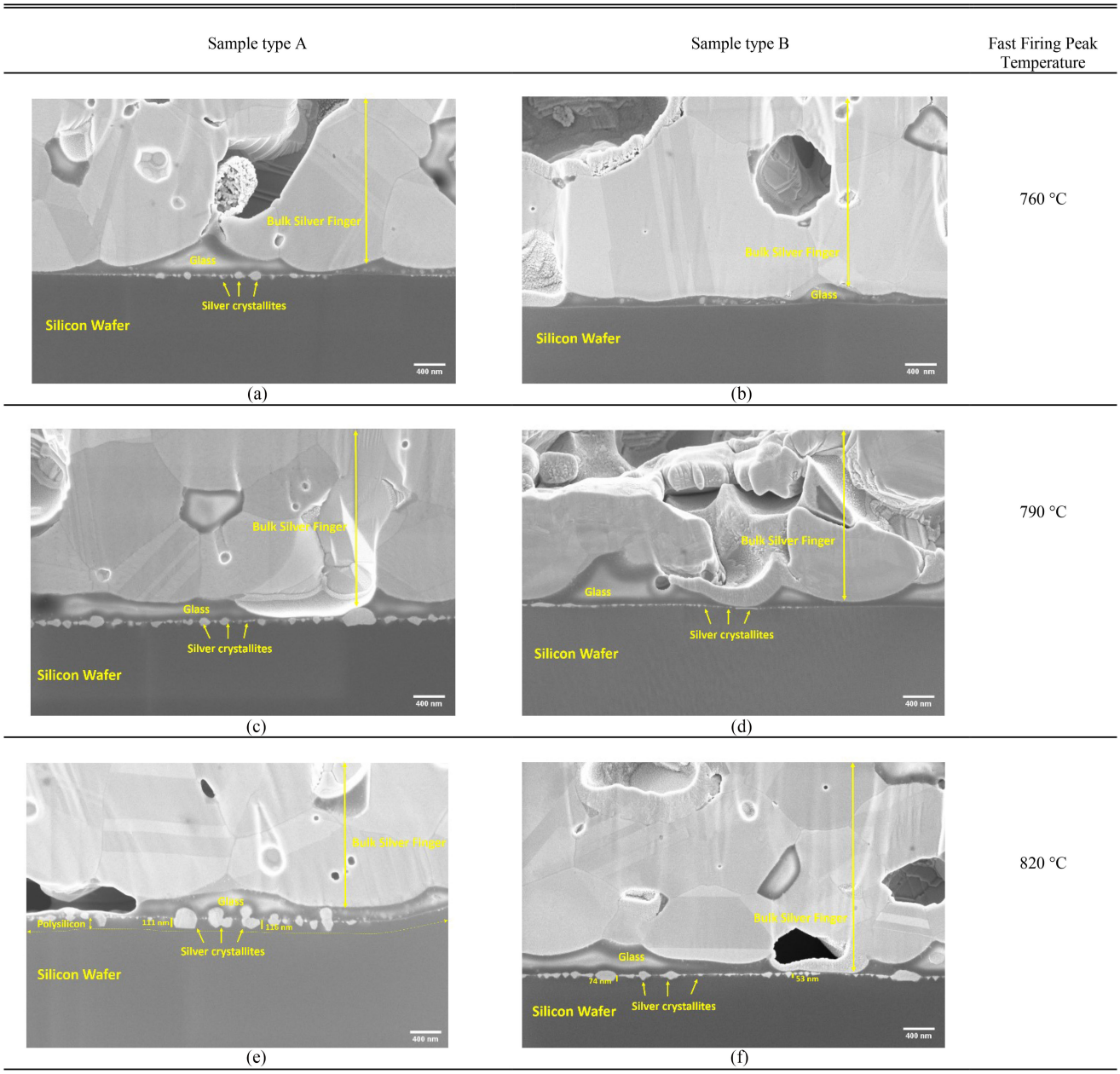


Fig. 9. Cross-sectional SEM images for the two sample types fast fired at different peak temperatures.

layer with a dashed line. For sample Type B, the silver crystallites are not as deep (< 100 nm) as compared with those for sample type A. This shows that the polysilicon layer favors the formation of deeper crystallites as compared with diffused surface even at the same fast-firing peak temperature. The increased size of the silver crystallites can be attributed to the low sheet resistance (90 Ω/sq) in sample type A, which, in turn, is the result of a higher dopant concentration [20]. In Fig. 10, we present doping profiles for the sample types A and B, fast fired at a peak temperature of 820 °C. This figure shows that there is an order of magnitude difference in active phosphorus (surface doping) concentration between the two types of samples, corroborating the hypothesis that the dopant concentration influences the Ag crystallization. Another reason that can be behind the larger number and bigger dimensions of silver crystallites in polysilicon is the higher oxidation rate of polysilicon as compared with crystalline silicon (<100>) [21]. A higher oxidation rate of polysilicon leads to a higher reduction rate of silver oxide, enhancing the precipitation of silver in the redox reactions during contact formation [22], [23].

We further investigated the samples and took SEM images after removing the bulk silver, glass layer, and silver crystallites as explained in Section II-C. In Fig. 11, the top view for sample types A and B are presented; these samples were fast fired at the peak temperature of 820 °C.

In the image in Fig. 11(a), we have marked a region where the polysilicon is damaged (darker features which appear as trenches in the image) with a yellow boundary. This kind

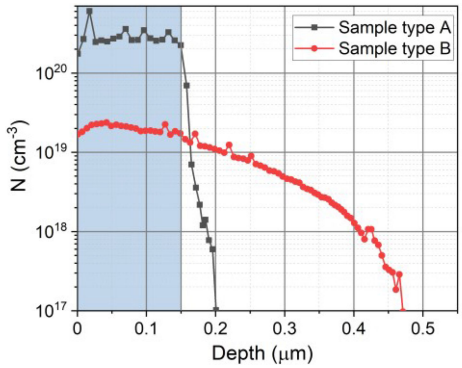
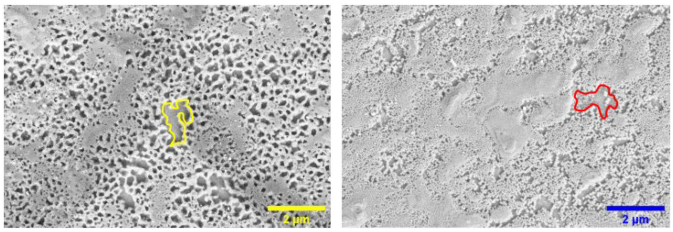


Fig. 10. ECV profile for sample type A and sample type B fast fired at a peak temperature of 820 °C.



(a) (b)

Fig. 11. Top-view SEM image for (a) sample type A and (b) sample type B, fast fired at 820 °C. Region with a yellow boundary shows a region with damaged polysilicon layer, while the region with a red boundary shows the damage to the crystalline silicon.

of damage to the polysilicon layer by the silver paste constituents has also been observed previously [9], [13]. From the results of J_{0met} presented in Fig. 7, we conclude that this damage to the polysilicon does not lead to an excessively high J_{0met} (> 200 fA·cm^{-2}). Similarly, in Fig. 11(b), as an example, we also marked damage to the silicon wafer for sample type B with a red boundary. The scale of this damage to the crystalline silicon wafer is positively correlated to J_{0met}. It is difficult to quantify the damage from the SEM images, so an absolute number is difficult to generate. For sample type B, we observe that when the fast-firing temperature is changed the J_{0met} remains similar. This is unexpected as from the specific contact resistivity measurements and the cross-sectional SEM we expected to have low values of J_{0met} at low fast-firing temperature, as there are almost no silver crystallites in contact with the silicon layer. We also took SEM images for samples fired at lower fast-firing peak temperature and found out that there is less damage to the silicon, but still for sample type B, the remaining damage is enough to lead to higher J_{0met} values as compared with that for sample type A. As an example in Fig. 12, we present a top-view SEM image for Sample type B fast fired at a peak temperature of 790 °C. Here also the damage to the crystalline silicon is visible, as marked as an example with a red boundary. This means that the damage to the silicon layer in the case of sample type B is detrimental to the J_{0met} value. We suggest that in addition to the damage caused to the diffused layer, the etching of the silicon nitride passivation layer by the paste constituents can be a possible additional contributor. These two factors lead to a reduction of

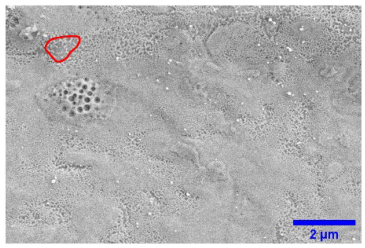


Fig. 12. Top-view SEM images for sample type B fast fired at peak temperature of 790 °C.

TABLE I
CELL RESULTS

V_{oc} (mv)	FF (%)	J_{sc} (mA/cm^2)	Efficiency (%)	
684	80.1	39.37	21.51	Mean value (This work)
686	80.2	39.33	21.64	Best cell (This work)
663	80.1	39.30	20.90	Best cell (nPERT [15])

the passivation quality of the layers, which translates, into a high value of J_{0met}.

To investigate the influence of silicon nitride passivation layer etching on the high J_{0met} for sample type B, we completely etched the silicon nitride layer on unmetallized areas of the fast-fired samples in a 2% HF solution and then performed QSSPC measurements. From the measurements, an absolute drop of 7–12 mV (equal to 1%–1.7% abs) in iV_{oc} is observed for sample type A. The drop in iV_{oc} for sample type B is 110–112 mV (equal to 16%–16.2% abs). This large drop for sample type B comes from the reduced surface passivation owing to the absence of the silicon nitride passivation layer. While for sample type A, passivation is dominated by the interfacial oxide and polysilicon, hence a smaller drop in passivation is observed. This shows that the removal of silicon nitride passivation layer for the diffused samples is also a factor and adds to higher recombination after metallization.

Using the knowledge gained from the above experiment, we applied a 150 nm thick n^+ polysilicon layer deposited on top of an interfacial oxide, in an nPERT solar cell. The results for a group of nine cells are presented in Table I. These cells were fast fired at a peak temperature of 805 °C.

The efficiency values presented for the polysilicon cell in Table I are ~0.7% absolute higher than the efficiency values for our standard nPERT cells [15]. The major gain comes from the V_{oc} improvement when a polysilicon-based passivated contact is applied. This gain is the result of the reduction in the J_{0met} and J_{0pass} because of the n^+ polysilicon/SiO_x and the interfacial oxide layer stack.

IV. CONCLUSION

The passivation quality achieved with n^+ polysilicon layers with an interfacial oxide is superior as compared with samples with a phosphorus-diffused layer.

Metal silicon recombination current density and the specific contact resistivity values were compared and the n^+ polysilicon-based contacts outperform the phosphorus-diffused samples.

Excellent values ($J_{0met} \approx J_{01}$ and $\rho_c \leq 2$ mΩ·cm^2) are obtained for polysilicon-based samples. The presence of a larger number and bigger size of silver crystallites is observed in the SEM images for samples with an n^+ polysilicon layer. The n^+ polysilicon layer favors the formation of deeper silver crystallites as compared with phosphorus-doped layers. This is thought to be because of higher surface doping and higher oxidation rate of n^+ polysilicon as compared with crystalline silicon. The damage to the crystalline silicon wafer during the metallization in the case of phosphorus-doped samples is critical. This in addition to the damage to the silicon nitride passivation layer is the reason for higher J_{0met} for these samples.

We made nPERT solar cells with the 150 nm n^+ polysilicon-based passivated contact and achieved an efficiency of 21.64% with a V_{oc} of 686 mV and fill factor of 80.20%, for the best cell. This amounts to an overall improvement in the efficiency of $\sim$0.7% absolute from our standard nPERT solar cells. This improvement mainly comes from a reduction in J_{0met} and J_{0pass} because of the n^+ polysilicon and the interfacial oxide layer.

ACKNOWLEDGMENT

The authors would like to thank their project partners- Heraeus, for supply of the silver paste and University of Konstanz, especially to Dr. Barbara Terheiden (University of Konstanz) for the support for high-resolution SEM images.

REFERENCES

[1] A. W. Blakers, A. Wang, A. M. Milne, J. Zhao, and M. A. Green, "22.8% efficient silicon solar cell," *Appl. Phys. Lett.*, vol. 55, no. 13, pp. 1363–1365, 1989.

[2] B. Min *et al.*, "Roadmap toward 24% efficient PERC solar cells in industrial mass production," *IEEE J. Photovolt.*, vol. 7, no. 6, pp. 1541–1550, Jun. 2017.

[3] J. Rodriguez *et al.*, "Towards 22% efficient screen-printed bifacial n-type silicon solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 187, pp. 91–96, 2018.

[4] F. Haase *et al.*, "Laser contact openings for local poly-Si metal contacts enabling 26.1%-efficient POLO-IBC solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 186, pp. 184–193, 2018.

[5] A. Richter *et al.*, "Design rules for high-efficiency both-sides-contacted silicon solar cells with balanced charge carrier transport and recombination losses," *Nature Energy*, vol. 6, pp. 429–438, 2021.

[6] Y. Chen *et al.*, "Mass production of industrial tunnel oxide passivated contacts (iTOPCon) silicon solar cells with average efficiency over 23% and modules over 345 W," *Prog. Photovolt., Res. Appl.*, vol. 27, pp. 827–834, 2019.

[7] D. Chen *et al.*, "24.58% total area efficiency of screen-printed, large area industrial silicon solar cells with the tunnel oxide passivated contacts (i-TOPCon) design," *Sol. Energy Mater. Sol. Cells*, vol. 206, 2020, Art. no. 110258.

[8] P. Padhamnath *et al.*, "Characterization of screen printed and fire-through contacts on LPCVD based passivating contacts in monoPoly^{TM} solar cells," *Sol. Energy*, vol. 202, pp. 73–79, 2020.

[9] A. Chaudhary, J. Hoß, J. Lossen, R. van Swaaij, and M. Zeman, "Screen printed Ag contacts for n-type polysilicon passivated contacts," *AIP Conf. Proc.*, vol. 2147, 2019, Art. no. 040002.

[10] P. Padhamnath, A. Khanna, N. Nandakumar, A. G. Aberle, and S. Duttagupta, "Impact of firing temperature on fire-through metal contacts to P-doped (n+) and B-doped (p+) poly-Si," *Sol. Energy Mater. Sol. Cells*, vol. 230, 2021, Art. no. 111217.

[11] J. Melskens, L. Bas WH van de, B. Macco, E. B Lachlan, S. Sjoerd, and W. M. M Kessels, "Passivating contacts for crystalline silicon solar cells: From concepts and materials to prospects," *IEEE J. Photovolt.*, vol. 8, no. 2, pp. 373–388, Feb. 2018.

[12] F. Feldmann *et al.*, "Large area TOPcon cells realized by a PECVD tube process," in *Proc. 36th Eur. Photovolt. Sol. Energy Conf. Exhib.*, 2019, pp. 1–5.

[13] H. E. Çiftpınar *et al.*, "Study of screen printed metallization for polysilicon based passivating contacts," *Energy Procedia*, vol. 124, pp. 851–861, 2017.

[14] P. Padhamnath *et al.*, "Development of thin polysilicon layers for application in monoPoly^{TM} cells with screen-printed and fired metallization," *Sol. Energy Mater. Sol. Cells*, vol. 207, 2020, Art. no. 110358.

[15] F. Buchholz, P. Preis, H. Chu, J. Lossen, and E. Wefringhaus, "Progress in the development of industrial nPERT cells," *Energy Procedia*, vol. 124, pp. 649–656, 2017.

[16] J. Lossen *et al.*, "From lab to fab: Bifacial n-type cells entering industrial production," in *Proc. 31st Proc. 30th Eur. Photovolt. Sol. Energy*, 2015, pp. 965–968.

[17] R. A. Sinton, A. Cuevas, and M. Stuckings, "Quasi-steady-state photoconductance, a new method for solar cell material and device characterization," in *Proc. Conf. Rec. 25th IEEE Photovolt. Spec. Conf.*, May 1996, pp. 457–460.

[18] C. Comparotto, J. Theobald, J. Lossen, and V. D. Mihailetchi, "Understanding contact formation on n-PERT-RJ solar cells," in *Proc. 33rd Eur. Photovolt. Sol. Energy Conf. Exhib.*, 2017, pp. 832–836.

[19] Z. P. Ling, Z. Xin, P. Wang, R. Sridharan, C. Ke, and R. Stangl, "Double-sided passivated contacts for solar cell applications: An industrially viable approach toward 24% efficient large area silicon solar cells," *Silicon Mater.*, vol. 89, pp. 1–3, 2019.

[20] M. M. Hilali *et al.*, "Understanding and development of ag pastes for silicon solarcells with high sheet-resistance emitters," in *Proc. 19th Eur. Photovolt. Sol. Energy Conf.*, 2004, pp. 1300–1303.

[21] T. I. Kamins and E. L. MacKenna, "Thermal oxidation of polycrystalline silicon films," *Metallurgical Mater. Trans. B*, vol. 2, no. 8, pp. 2292–2294, 1971.

[22] K.-K. Hong, S.-B. Cho, J.-Y. Huh, H. J. Park, and J.-W. Jeong, "Role of Pbo-based glass frit in Ag thick-film contact formation for crystalline Si solar cells," *Metal Mater. Int.*, vol. 15, no. 2, pp. 307–312, 2009.

[23] S.-B. Cho, K.-K. Hong, J.-Y. Huh, H. J. Park, and J.-W. Jeong, "Role of the ambient oxygen on the silver thick-film contact formation for crystalline silicon solar cells," *Curr. Appl. Phys.*, vol. 10, no. 2, pp. S222–S225, 2010.