

## A 60 GHz Frequency Generator Based on a 20 GHz Oscillator and an Implicit Multiplier

Zong, Z.; Babaie, M.; Staszewski, R. B.

**DOI**

[10.1109/JSSC.2016.2528997](https://doi.org/10.1109/JSSC.2016.2528997)

**Publication date**

2016

**Document Version**

Final published version

**Published in**

IEEE Journal of Solid State Circuits

**Citation (APA)**

Zong, Z., Babaie, M., & Staszewski, R. B. (2016). A 60 GHz Frequency Generator Based on a 20 GHz Oscillator and an Implicit Multiplier. *IEEE Journal of Solid State Circuits*, 51(5), 1261-1273.  
<https://doi.org/10.1109/JSSC.2016.2528997>

**Important note**

To cite this publication, please use the final published version (if applicable).  
Please check the document version above.

**Copyright**

Other than for strictly personal use, it is not permitted to download, forward or distribute the text or part of it, without the consent of the author(s) and/or copyright holder(s), unless the work is under an open content license such as Creative Commons.

**Takedown policy**

Please contact us and provide details if you believe this document breaches copyrights.  
We will remove access to the work immediately and investigate your claim.

# A 60 GHz Frequency Generator Based on a 20 GHz Oscillator and an Implicit Multiplier

Zhirui Zong, *Student Member, IEEE*, Masoud Babaie, *Student Member, IEEE*,  
and Robert Bogdan Staszewski, *Fellow, IEEE*

**Abstract**—This paper proposes a mm-wave frequency generation technique that improves its phase noise (PN) performance and power efficiency. The main idea is that a fundamental 20 GHz signal and its sufficiently strong third harmonic at 60 GHz are generated simultaneously in a single oscillator. The desired 60 GHz local oscillator (LO) signal is delivered to the output, whereas the 20 GHz signal can be fed back for phase detection in a phase-locked loop. Third-harmonic boosting and extraction techniques are proposed and applied to the frequency generator. A prototype of the proposed frequency generator is implemented in digital 40 nm CMOS. It exhibits a PN of  $-100$  dBc/Hz at 1 MHz offset from 57.8 GHz and provides 25% frequency tuning range (TR). The achieved figure-of-merit (FoM) is between 179 and 182 dBc/Hz.

**Index Terms**—60 GHz, frequency divider, harmonic boosting, harmonic extraction, implicit multiplier, mm-wave, oscillator, phase noise (PN), PLL, transformer.

## I. INTRODUCTION

HIGH DATA-RATE wireless communications in the unlicensed 60 GHz band have recently aroused a great interest. Complex modulation and coding schemes employed there require low distortion, leading to strict specifications on a transmit (TX) error vector magnitude (EVM). For example, the IEEE 802.11ad standard requires a TX EVM of  $-21$  dB for a 16 QAM modulation [1], which sets stringent phase noise (PN) requirement on the local oscillators (LOs) [2], [3]. Wide tuning range (TR) is also necessary to cover the specified frequency bands (e.g., 57–65 GHz) with margin for process and temperature spreads. Meanwhile, long battery lifetime calls for high power efficiency, thus high figure-of-merit (FoM). Unfortunately, 60 GHz frequency generation in CMOS has typically suffered from poor PN, limited TR, and high power consumption [4]–[9].

Several mm-wave frequency synthesizer architectures have been reported and can be categorized into three groups [7]: 1) a PLL with a fundamental oscillator [4]–[7]; 2) a low-frequency PLL together with a frequency multiplier [8]–[10];

Manuscript received June 02, 2015; revised November 27, 2015; accepted January 28, 2016. Date of publication March 15, 2016; date of current version April 28, 2016. This paper was approved by Associate Editor Brian A. Floyd. This work was supported by European Research Council (ERC) Consolidator Grant 307624 TDRFSP.

Z. Zong and M. Babaie are with the Department of Microelectronics, Delft University of Technology, Delft, The Netherlands (e-mail: Z.Zong@tudelft.nl).

R. B. Staszewski is with the School of Electrical and Electronic Engineering, University College Dublin, Dublin 4, Ireland, and also with Delft University of Technology, 2628 CD Delft, The Netherlands.

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2016.2528997

and 3) a PLL with  $N$ -push oscillators [11]–[13]. In the first architecture [Fig. 1(a)] [4]–[7], the mm-wave oscillators and high-frequency dividers are the key design challenges [14]–[19]. The difficulties of 60 GHz oscillators are: 1) the parasitic capacitance of active devices takes up a large share of the relatively small tank capacitance, thus limiting the frequency TR; 2) to achieve a TR of  $>15\%$ , the poor  $Q$ -factor of the tuning capacitance dominates the  $Q$ -factor of the 60 GHz resonator, thus limiting the achievable PN. The 60 GHz frequency dividers must achieve large locking range to ensure sufficient overlap with the oscillator TR under PVT variations. However, there is a strong tradeoff between the locking range and the power consumption [17]–[19]. Recently, several injection-locked frequency dividers were reported with large locking range and low power consumption, but at the cost of large silicon area [20], [21]. The aforementioned design challenges in the oscillators and frequency dividers are relieved in PLLs based on frequency multipliers [Fig. 1(b)] [8]–[10]. However, the 60 GHz frequency multipliers in this architecture typically have limited locking range, or consume large power, in order to achieve large locking range [10], [22]–[24]. In PLLs with  $N$ -push oscillators [as shown in Fig. 1(c) for  $N = 2$ ] [11]–[13], the frequency dividers operate at  $60/N$  GHz, and frequency multipliers are avoided. However, this oscillator type suffers from low output power and mismatches among the  $N$  oscillators if  $N > 2$ . Among this type, push–push oscillators are the most common and easiest to implement. However, the required large common-mode (CM) swing can increase the  $1/f$  noise upconversion [25]. Moreover, the conversion from single-ended CM signal to a differential output may introduce large phase error [11].

To alleviate the design challenges for mm-wave oscillators and dividers without shifting more stress onto other blocks, a 60 GHz frequency generation technique based on a 20 GHz oscillator and an implicit  $\times 3$  frequency multiplier [26] is proposed in this paper. As a result, the 60 GHz LO signal is delivered to the output, while its  $\div 3$  version is destined to be used for phase detection in the feedback path of a PLL. Fig. 1 summarizes the evolution of 60 GHz PLLs, and introduces in Fig. 1(d) a new PLL architecture that employs the proposed 20/60 GHz generator. To realize that goal, third-harmonic boosting and extraction techniques are proposed and applied to a 20 GHz transformer-based dual-resonance oscillator. The third-harmonic techniques have been exploited in single-GHz oscillators to shape the oscillation waveforms for a better PN performance [27], [28]. However, instead of acting as an auxiliary therein, the third-harmonic component in our work is the signal of interest. Its direct extraction and utilization require precise control of the harmonic generation process. Therefore,

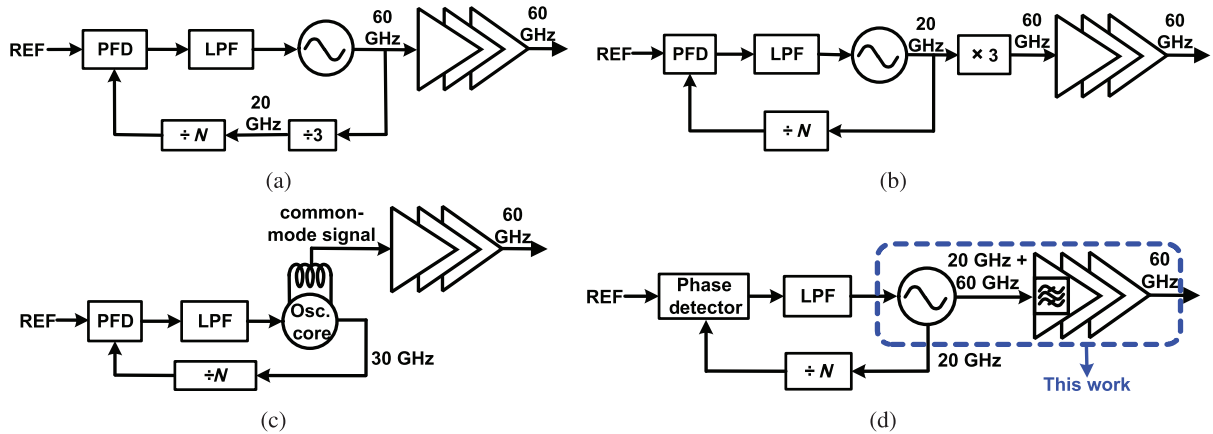


Fig. 1. Evolution of the mm-wave PLL architecture. PLL with (a) fundamental oscillator; (b) frequency multiplier; and (c) push-push oscillator. (d) Proposed PLL with harmonic boosting and extraction.

a detailed insight into its operational principle is given. Further, the PN mechanism for the oscillator with two resonant peaks is investigated, and a corresponding PN analysis approach is developed.

This paper is organized as follows. Section II describes the basic idea of the proposed 20/60 GHz generator, as well as the third-harmonic boosting and extraction techniques. Detailed PN analysis is presented in Section III. Then, Section IV brings more insights into the operational principles of the third-harmonic tuned oscillators. The experimental results are given in Section V.

## II. THIRD-HARMONIC BOOSTING AND EXTRACTION

The basic concept of this work is to simultaneously generate both 20 GHz and a significant level of its third harmonic at 60 GHz inside a 20 GHz oscillator. The generated 60 GHz signal is fed forward to a buffer with natural bandpass filtering, whereas the 20 GHz signal is fed back for phase detection after further frequency division, as shown in Fig. 1(d). Since buffers are typically needed for LO distribution in any mm-wave transceivers, there is no extra circuitry cost in the proposed solution. Consequently, the ideal  $\times 3$  functionality is inherent such that no physical divider or multiplier operating at the 60 GHz is needed anymore. This should lead to an improvement in the power efficiency of 60 GHz frequency synthesizers.

Since the oscillator runs at the fundamental frequency of 20 GHz, its resonant tank achieves a better  $Q$ -factor than at 60 GHz, which leads to a better PN performance. Moreover, the tank has a larger inductance ( $L$ ) and capacitance ( $C$ ). This increases the variable portion of the total tank capacitance and the frequency TR.

### A. Third-Harmonic Boosting Techniques

To generate the third harmonic, one possible approach is to use multiple series-connected LC-tanks resonating at the fundamental and third harmonic [21], [27]. The multiple inductors occupy large area. Since the two resonances have the same phase response and transconductance gain in the oscillation

loop, undesired oscillation at the auxiliary resonance could be triggered by increasing the level of third harmonic. Therefore, it appears problematic in our case.

A more compact implementation would be a transformer-based dual-tank resonator. The  $L$  and  $C$  ratios in primary and secondary windings were optimized in [28] to realize fundamental oscillation and its third-harmonic resonance. However, the third harmonic generated there is relatively weak ( $\sim 15\%$  of the fundamental tone); therefore, to make it sufficiently stronger, a high-gain buffering amplifier would be needed. This implies a large power consumption, which would negate the effectiveness of the proposed architecture. Moreover, thick-oxide transistors were used in [28] due to reliability concerns. In the technology at hand, cut-off frequency ( $f_T$ ) of the thick-oxide device is  $< 40$  GHz. To provide sufficient  $g_m$  for the startup of oscillation, either larger power consumption or larger transistor size (i.e., larger parasitic capacitance) would be required. Consequently, thick-oxide device is avoided in this design. In order to reduce the required gain of the following buffer stage, a much stronger third harmonic must be provided by the oscillator. This paper proposes such a harmonic boosting technique.

Simplified diagram of the proposed mm-wave oscillator and its operational principle are shown in Fig. 2.  $I_{DH1,3}$ ,  $R_{p1,3}$ , and  $V_{DH1,3}$  represent the tank's current, equivalent parallel resistance, and voltage, respectively, of the first- and third-harmonic components. According to the linear model of oscillators, the oscillation amplitude at the first and third harmonics is determined by the current component and tank impedance at their respective frequencies. To achieve a larger  $V_{DH3}/V_{DH1}$ , there are two possible options: 1) increasing  $I_{DH3}/I_{DH1}$  or 2) increasing  $R_{p3}/R_{p1}$ . The  $I_{DH3}/I_{DH1}$  is typically fixed for a certain type of oscillator (e.g., 0.33 for class-B and 0.2 for class-C). Consequently, larger  $R_{p3}/R_{p1}$  is desired. On the other hand, the equivalent  $Q$ -factor ( $Q_{eq}$ ) at the two resonant frequencies affect the oscillator performance dramatically. High  $Q_{eq}$  at  $\omega_{osc}$  promotes low PN, while low  $Q_{eq}$  at  $3\omega_{osc}$  is appreciated for better tolerance to the possible frequency misalignment between the second resonance and  $3\omega_{osc}$ . Moreover, large  $R_{p1}$  is beneficial for low power consumption.

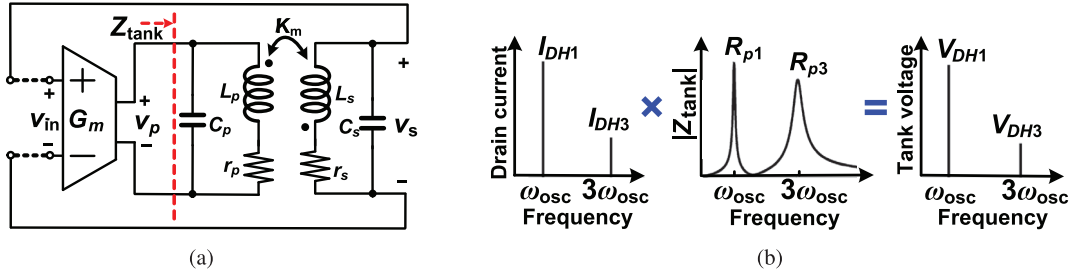
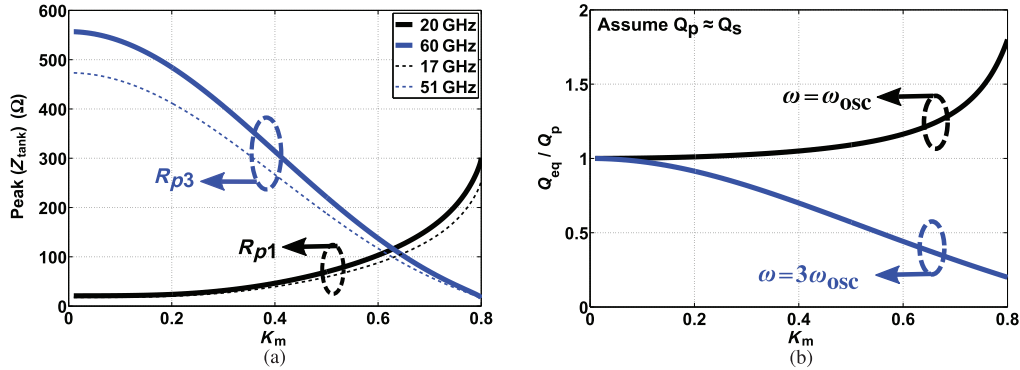


Fig. 2. (a) Simplified diagram and (b) operational principle of the proposed oscillator.


 Fig. 3. Dependency of (a) tank impedance on  $k_m$  (1) and (b)  $Q_{eq}$  on  $k_m$  from (3).

The tank impedance of this oscillator can be derived as

$$Z_{\text{tank}}(j\omega) = \frac{1}{\frac{1}{j\omega L_p \left(1 + \frac{\omega^2 L_s C_s k_m^2}{1 - \omega^2 L_s C_s + j\omega C_s r_s}\right) + r_p} + j\omega C_p}. \quad (1)$$

Since it is a two-port dual-tank oscillator, its equivalent  $Q$  is not so straightforward to estimate as in traditional one-port resonators. The equivalent  $Q$ -factor ( $Q_{eq}$ ) is derived from the phase response of the open-loop transfer function  $v_s/v_{in}$  [29]

$$H_{ol}(j\omega) = \frac{v_s(j\omega)}{v_{in}(j\omega)} = -G_m \cdot Z_{\text{trans}}(j\omega) \quad (2)$$

$$Z_{\text{trans}}(j\omega) = \frac{j\omega M}{(1 + j\omega C_p r_p - \omega^2 L_p C_p)(1 + j\omega C_s r_s - \omega^2 L_s C_s) - \omega^4 M^2 C_p C_s} \quad (3)$$

$$Q_{eq} = \frac{\omega}{2} \cdot \left| \frac{d[\angle H_{ol}(j\omega)]}{d\omega} \right| = \frac{1 + \alpha_p \alpha_s \cdot k_m^2 - \alpha_p \alpha_s}{\frac{\alpha_p}{Q_p} + \frac{\alpha_s}{Q_s} - \alpha_p \alpha_s \left( \frac{1}{Q_p} + \frac{1}{Q_s} \right)} \quad (4)$$

where  $Z_{\text{trans}}(j\omega)$  is the trans-impedance from primary to secondary winding in the tank,  $\alpha_p = \omega^2 L_p C_p$ ,  $\alpha_s = \omega^2 L_s C_s$ ,  $Q_p$  and  $Q_s$  are the  $Q$ -factors for each winding (i.e.,  $Q_p = \omega L_p / r_p$  and  $Q_s = \omega L_s / r_s$ ). The two resonances ( $\omega_L$  and  $\omega_H$ ) appear at the frequencies where  $\text{Im}[Z_{\text{trans}}(j\omega)] = 0$ . For a transformer-based dual-tank resonator,  $\alpha_{p,s} < 1$  is always true at the low-frequency resonance (i.e.,  $\omega = \omega_L$ ). At the high-frequency resonance ( $\omega = \omega_H$ ),  $\alpha_{p,s} > 1/\sqrt{1 - k_m^2}$ . From (4), we can conclude that increasing  $k_m$  can result in higher  $Q_{eq}$  at  $\omega = \omega_L$ . However,  $Q_{eq}$  at  $\omega = \omega_H$  will be lower with larger  $k_m$ .

The above analysis shows that  $k_m$  affects both the tank impedance ( $Z_{\text{tank}}$ ) and  $Q_{eq}$ . Based on (1) and (4), the relationships at  $\omega_{\text{osc}}$  and  $3\omega_{\text{osc}}$  on  $k_m$  are shown in Fig. 3. In the calculations,  $L_p$  and  $L_s$  are kept constant, whereas  $C_p$  and  $C_s$  are tuned to achieve the fundamental and third-harmonic resonances for each  $k_m$  value. As we can see in Fig. 3,  $R_{p1}$  decreases with smaller  $k_m$ , while  $R_{p3}$  behaves opposite. Therefore, smaller  $k_m$  is desired for larger  $R_{p3}/R_{p1}$ . However, larger  $k_m$  is required for high  $Q_{eq}$  at  $\omega_{\text{osc}}$  and low  $Q_{eq}$  at  $3\omega_{\text{osc}}$ . By reducing  $k_m$  for larger  $R_{p3}/R_{p1}$ , both the PN performance and the tolerance to the possible frequency misalignment between the second resonance and  $3\omega_{\text{osc}}$  will be degraded. Moreover, due to the smaller  $R_{p1}$ , larger power consumption is required to achieve the same oscillation amplitude with reduced  $k_m$ . As a tradeoff between large third harmonic and optimal oscillator performance,  $k_m = 0.61$  is chosen for  $R_{p3}/R_{p1} > 1$  with sufficient  $Q_{eq}$  and  $R_{p1}$ .

A concern might arise that the oscillation could happen at  $\omega_H$  ( $\sim 60$  GHz) rather than at  $\omega_L$  ( $\sim 20$  GHz) due to  $R_{p3} > R_{p1}$ . Start-up conditions are examined to ensure that the oscillation can only happen at  $\omega_L$ , even if  $R_{p3} > R_{p1}$ : Barkhausen's phase and gain criteria should be satisfied for a stable oscillation. Referring to (2) and (3), there is no zero between the two pairs of conjugate poles ( $\pm\omega_L$  and  $\pm\omega_H$ ) in  $H_{ol}(j\omega)$ , which makes this oscillation loop different from [27]. Analysis and simulations show that the open-loop phase response  $\angle H_{ol}(j\omega) = 0^\circ$  at  $\omega_L = \omega_{\text{osc}}$ , while  $\angle H_{ol}(j\omega) = -180^\circ$  at  $\omega_H = 3\omega_{\text{osc}}$ , as shown in Fig. 4. The phase criterion is satisfied only at  $\omega_L$ . At  $\omega_H$ , the phase response is  $-180^\circ$ , which implies a negative feedback. Therefore, only one stable oscillation mode at  $\sim 20$  GHz is possible here. This phenomenon also explains the behavior of  $Q_{eq}$  in Fig. 3. Since the fundamental components at both windings are in-phase, its  $Q_{eq}$  at  $\omega = \omega_{\text{osc}}$  benefits from

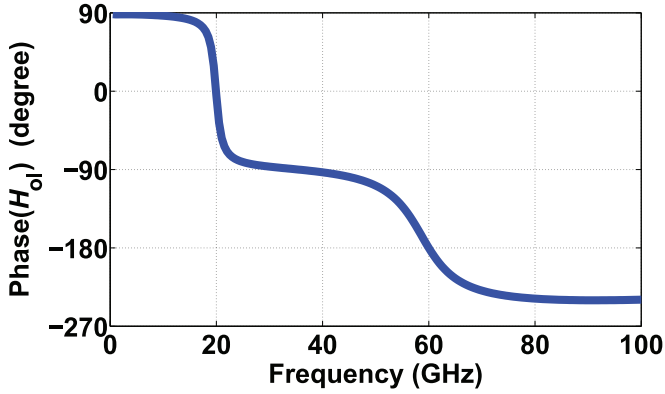


Fig. 4. Simulated open-loop phase response of  $v_s/v_{in}$  in the oscillator.

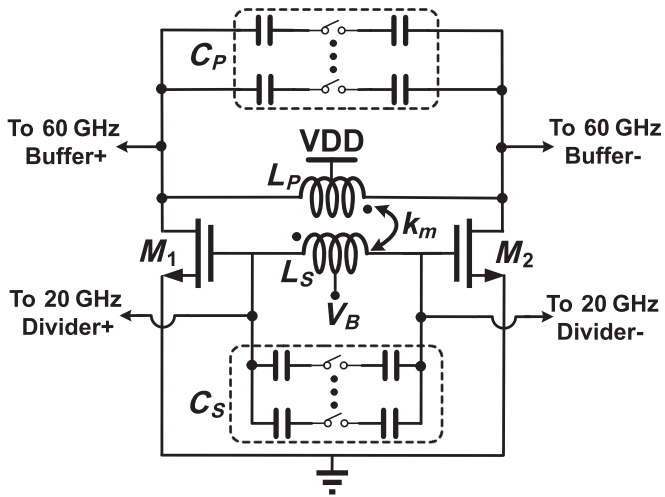


Fig. 5. Schematic of the third-harmonic boosting oscillator.

the mutual inductance. However, because the third-harmonics at both windings are antiphase,  $Q_{eq}$  at  $\omega = 3\omega_{osc}$  decreases with larger  $k_m$ .

Moreover, the transformer tank provides different voltage gain at these two frequencies. The magnitude response of  $v_s/v_p$  is investigated. At  $\sim 20$  GHz, the transformer tank exhibits a voltage gain of 2.2 (6.85 dB); whereas, at  $\sim 60$  GHz, it has a voltage gain of 0.24 ( $-12.40$  dB). This property filters out the third harmonic in the secondary winding.

Circuit implementation of the proposed third-harmonic boosting oscillator is shown in Fig. 5. A 1:2 transformer ( $k_m = 0.61$ ) together with 4 bit binary-weighted switched MOM capacitor banks in both primary and secondary windings comprises the resonant tank. By changing the separation space between primary and secondary windings,  $k_m$  is adjusted to the desired value.  $C_s$  provides coarse tuning, while  $C_p$  adjusts the second resonance close to  $3\omega_{osc}$ . LSB sizes of the switched-capacitor step ( $\Delta C$ ) are 3.5 fF for  $C_p$  and 5.8 fF for  $C_s$ . To mitigate the breakdown stress on the core transistors while avoiding thick-oxide devices, a lower supply voltage of  $V_{DD} = 0.7$  V is used.

Fig. 6 shows the simulated tank impedance for the complete design. In this case,  $R_{p1} = 102 \Omega$  and  $R_{p3} = 129 \Omega$ . The oscillation waveforms are shown in Fig. 7 and reveal that the third harmonic ( $V_{DH3}$ ) to fundamental component ( $V_{DH1}$ )

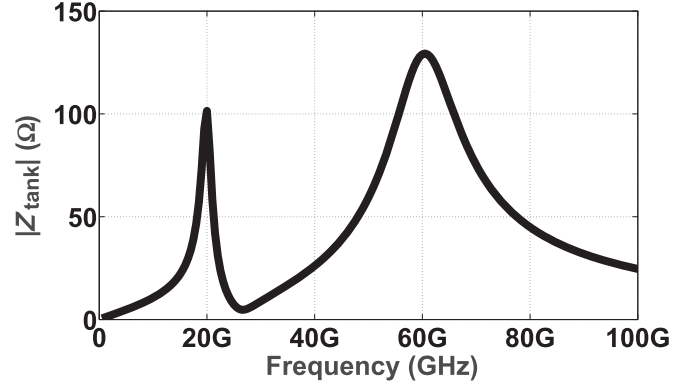


Fig. 6. Tank input impedance with  $k_m = 0.61$ .

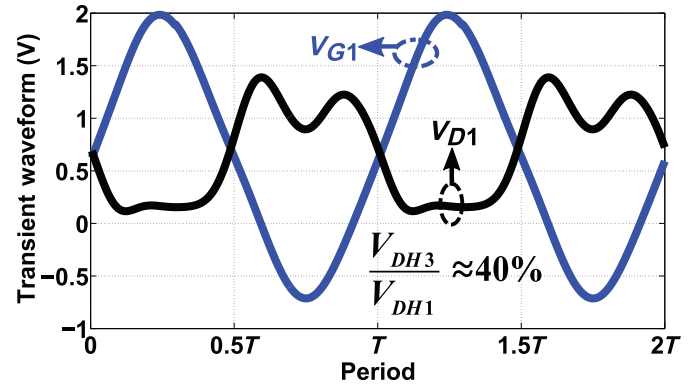


Fig. 7. Simulated oscillation waveforms at drain and gate nodes.

ratio is  $\sim 40\%$  at the drain nodes. Simulated differential amplitude of the third-harmonic tone varies from 350 to 510 mV across the frequency. A sinusoidal waveform at the fundamental frequency is restored at the gate nodes.

### B. Third-Harmonic Extraction

With the above third-harmonic boosting techniques, the oscillator is able to generate a significant harmonic amplitude at  $\sim 60$  GHz in addition to the fundamental tone at  $\sim 20$  GHz. To obtain a clean output spectrum at 60 GHz, the fundamental tone needs to be filtered out. LO buffers, which are commonly found in 60 GHz transceivers, are good bandpass filters by nature and are able to provide such filtering capabilities.

A common-source amplifier with transformer loading is designed as one buffer stage, as highlighted in Fig. 8(a). At the output of this stage, the simulated fundamental harmonic rejection ratio is 14–25 dB across 48–64 GHz, as shown in Fig. 8(b). It is comparable to or better than that of many wideband injection-locked frequency triplers (ILFTs) [30]. This stage consumes 10.5 mA from 1 V supply. No extra cost (e.g., the gain or driving capability) is incurred to obtain such an HRR.

The presence of 20 GHz tone may create several side effects. Inside the amplifier stage, the two-tone (i.e., 20/60 GHz) input could result in harmonic-mixing products. High-order nonlinearities are weak and not a concern. The second and fourth harmonics are closest to the 60 GHz band, but are still 20 GHz away. Moreover, they are generated through the second-order nonlinearity, which can only express itself as a CM distortion. The CM second harmonic at the oscillator output, at  $\sim 18\%$  of

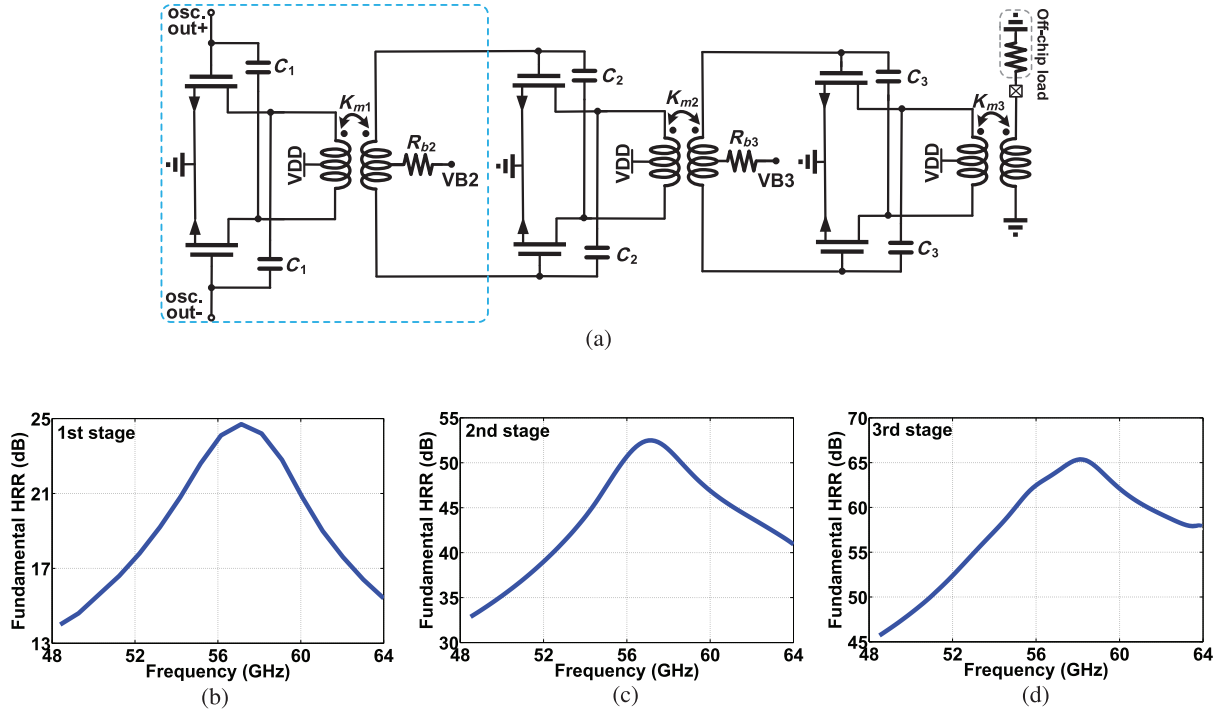


Fig. 8. (a) Schematic of the three-stage power amplifier and (b)–(d) simulated fundamental HRR for the each amplifier stage.

the fundamental tone level (see  $V_{D1}$  in Fig. 7), is also a harmonic source. A large resistor ( $R_{b2} = 1.5 \text{ k}\Omega$ ) is placed at the center-tap of VB2 to prevent the CM signal from propagating to the next stage. However, any unavoidable slight asymmetry in the layout of the oscillator and amplifier could result in some weak conversion from the CM to differential output.

With EM-extracted passives, postlayout simulations show that the second and fourth-harmonic levels are  $< -40$  and  $< -55.8$  dBc, respectively, at the differential output of the first amplifier stage over the TR. They are low enough and far away from the 60 GHz band. Therefore, harmonic distortion is not an issue.

At the output of the buffer/amplifier stage, the residual 20 GHz in the 60 GHz LO signal may cause several types of concerns at the system level. One is the out-of-band emission in transmitters (TXs), which should be  $< -30$  dBc at  $> 3.06$  GHz offset as specified in [1], and  $< -40$  dBm per FCC regulations [31]. The 60 GHz PLLs will drive upconversion mixers in I/Q TXs, or directly drive PAs in polar TXs. Multistage PAs are typically needed to deliver a sufficient output power [32]–[35]. To satisfy the out-of-band emission mask, the LC tank in upconversion mixers and multistage matching network in the PAs should provide enough suppression of the 20 GHz residual to minimize its transmission. Two extra amplifier stages are added in this design [shown in Fig. 8(a)] to verify the adequacy of the natural filtering capability of the TX chain [36]. The simulated 20 GHz HRRs at the output of each amplifier stage are shown in Fig. 8(b)–(d).

Another concern is the 20 GHz blocker tolerance on the receiver side. Any incident 20 GHz out-of-band blocker is significantly attenuated by the antenna and LNA matching network. Due to the residual 20 GHz in LO, a 20 GHz blocker will have a nonzero conversion gain in the down-conversion mixer. With the worst case HRR of  $-14$  dB, the 20 GHz

blocker has a conversion gain which is 20 dB lower than that at 60 GHz. In a typical 60 GHz receiver [37], with a 20 GHz blocker level as high as  $-30$  dBm, the down-converted blocker power is well below the receiver's sensitivity. The above analysis also explains the reasons why the ILFTs, which face similar scenarios as in this design, have found their use in 60 GHz transceivers [32], [33], [35].

### III. PN ANALYSIS

The linear time-variant (LTV) PN model [38] predicts that the PN of an LC-tank oscillator at an offset frequency  $\Delta\omega$  is

$$L(\Delta\omega) = 10 \log_{10} \left( \frac{\sum_i N_{L,i}}{2 q_{\max}^2 \Delta\omega^2} \right) \quad (5)$$

where  $N_{L,i}$  is the power of the perturbation generated by the  $i$ th noise current source, and  $q_{\max}$  is the maximum charge displacement in the tank capacitance. In the case at hand, there are mainly two noise sources that will be converted into PN: 1) resonant tank losses and 2) the channel noise of the active devices ( $M_1/M_2$ ).

Complexity arises from the fact that there are now two resonances (i.e., 20/60 GHz) in the tank. We can no longer rely on the general approach that models the tank losses as a fixed resistance together with a corresponding current noise source in-parallel to the LC tank. The mechanism of how the two resonant peaks affect the PN is investigated in this section. Regarding the PN contributed from the oscillator core transistors ( $M_1/M_2$ ), the periodically time-varying  $g_m$  and  $g_{ds}$  indicate that these noise sources are cyclostationary. Their calculation is discussed later. The oscillator noise sources are shown in Fig. 9. The  $R_{\text{eq}}$  is frequency-dependent to reflect the tank's multiresonance.

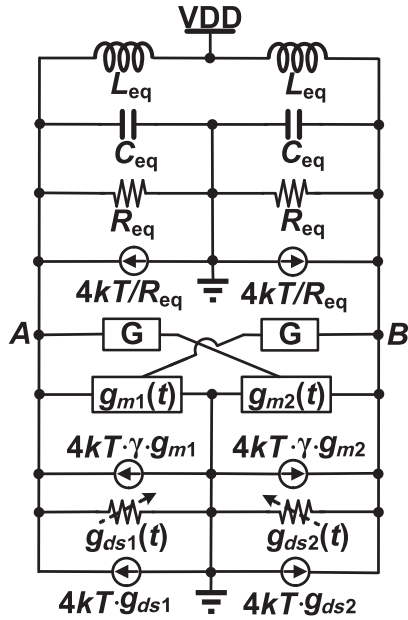


Fig. 9. Equivalent noise sources in the oscillator.

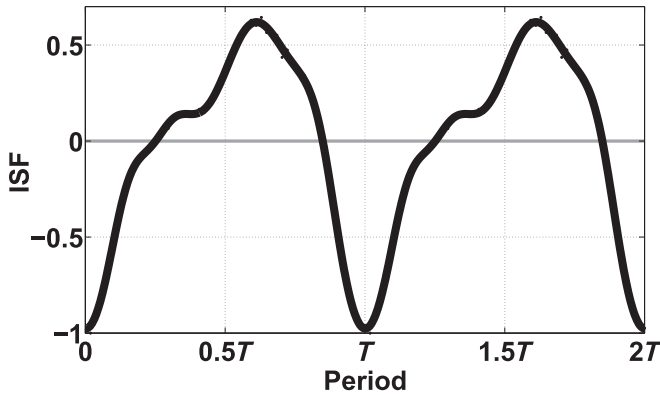


Fig. 10. Simulated ISF function at the drain nodes.

Prior to the detailed PN analysis and calculations, the ISF function is obtained through simulations. By injecting current pulses at the drain of  $M_1/M_2$  (node A/B in Fig. 9) throughout the oscillation period and measuring the resulting phase shift after settling, the ISF function is extracted and shown in Fig. 10.  $\text{ISF} \approx 0$  in the area when the drain waveform is in the bottom flat region (see the waveform  $V_{D1}$  in Fig. 7). As the rising transition is faster than falling transition, the ISF is larger at the negative side than at the positive side. It reveals that more circuit noise will be converted to PN during the falling transitions.

### A. Tank Noise Upconversion

In our oscillator design, the second resonant impedance at  $\sim 60$  GHz is boosted deliberately for a larger third-harmonic magnitude. However, up to this point, the mechanism of how the coexisting two resonant peaks affect the PN has not been discussed.

With Fourier series decomposition, the phase perturbation due to the noise source  $i_n(t)$  is

$$\phi_{\text{tank}}(t) = \frac{1}{q_{\text{max}}} \cdot \int_{-\infty}^t i_n(\tau) \cdot \sum_{m=0}^{\infty} c_m \cdot \cos(m\omega_o\tau) d\tau \quad (6)$$

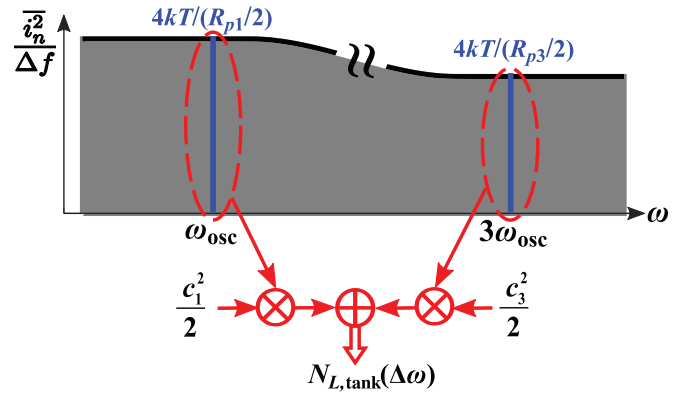


Fig. 11. Conversion of tank thermal noise into PN.

where  $c_m$  ( $m = 0, 1, 2, \dots$ ) is the Fourier series coefficient of the ISF function  $\Gamma(\omega_o t)$ . For close-in PN at an offset  $\Delta\omega$  ( $\Delta\omega \ll \omega_o$ ), only the noise at  $m\omega_o \pm \Delta\omega$  will be converted to PN. Since power spectral density (PSD) of the tank noise source is nonuniformly distributed, it is necessary to divide the spectrum into separate bands around  $m\omega_o \pm \Delta\omega$ . Each individual band experiences a different conversion factor ( $c_m$ ) during the conversion process from circuit noise to PN. Fig. 11 illustrates such conversion in the frequency domain.

Consequently, the effective noise power generated by the tank losses is

$$N_{\text{tank}} = 2 \cdot \left( \frac{c_1^2}{2} \cdot \frac{4kT}{R_{p1}/2} + \frac{c_3^2}{2} \cdot \frac{4kT}{R_{p3}/2} \right) \quad (7)$$

where the factor of 2 accounts for the two single-ended noise sources in the differential oscillator. With stronger third harmonic,  $c_3$  is larger. It facilitates the conversion from tank noise at third-harmonic frequency to PN.

### B. Channel Noise Upconversion

In [28], the effective transconductance ( $G_{MEF}$ ) and conductance ( $G_{DSEF}$ ), which was originally derived from the equivalence in the analysis of average power dissipation [39], was adopted in the PN analysis. The cyclostationary properties of the channel noise sources were not fully considered in the PN analysis and calculations. This approach has greatly simplified the analysis process, but has partially omitted the strong correlation between the ISF function and the channel noise PSD. In some cases, the simplification error might be large.

The periodic time-varying  $g_m(t)$  and  $g_{ds}(t)$  in our design are shown in Fig. 12. Without losing general applicability, the conversion process from cyclostationary channel noise  $i_{n0,Gm}(t)$  to PN is equivalent to that of a stationary white noise source  $i_{n0,Gm}(t)$  with an effective ISF to account for the time-varying effects of  $i_{n0,Gm}(t)$  [38]

$$\overline{i_{n0,Gm}^2(t)} = 4kT \cdot \gamma \cdot \max[g_m(t)] \quad (8)$$

$$\Gamma_{Gm,\text{eff}}(\omega_o t) = \Gamma(\omega_o t) \cdot \sqrt{\frac{g_m(t)}{\max[g_m(t)]}} \quad (9)$$

Fig. 13(a) shows the corresponding effective ISF for the channel noise  $i_{n0,Gm}(t)$ . Most of the PN conversion happens during

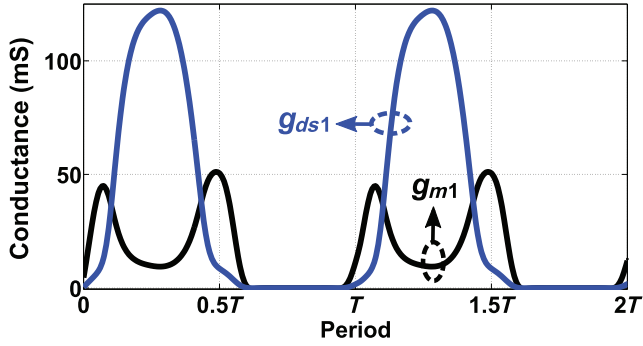


Fig. 12. Simulated time-varying transconductance and channel conductance of the core transistors in oscillator.

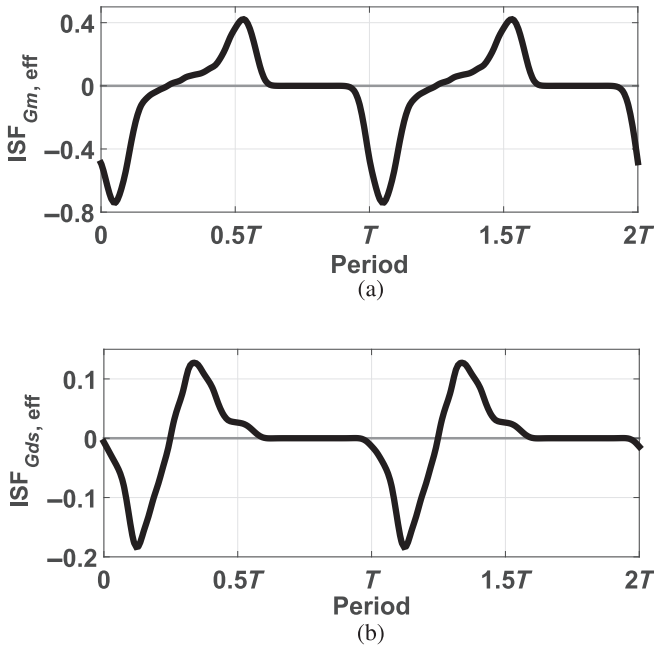


Fig. 13. Effective ISF function for the noise from (a) transconductance  $g_m(t)$  and (b) channel conductance  $g_{ds}(t)$ .

the rising and falling transitions. The effective noise power generated from  $g_m$  of the core devices ( $M_1$  and  $M_2$ ) is

$$N_{Gm} = 2 \cdot \Gamma_{Gm,eff,rms}^2 \cdot \overline{i_{n0,Gm}^2(t)} = 0.6 \cdot N_{tank}. \quad (10)$$

The same approach is also applied to the PN generated from  $g_{ds}$  of the core devices. Its equivalent ISF is shown in Fig. 13(b). The effective noise power converted from this part is

$$N_{Gds} = 2 \cdot \Gamma_{Gds,eff,rms}^2 \cdot \overline{i_{n0,Gds}^2(t)} = 0.41 \cdot N_{tank}. \quad (11)$$

In our case, the total PN generated from the channel noise of the core devices happens to be approximately the same as the PN generated from the tank losses. As we can see in Fig. 13, the conversion from channel noise to PN mainly happens during the transitions. When the transistors work in the deep triode region, the channel resistance is low. Due to the absence of a tail current source, the small channel resistance will load the tank. However, since  $ISF \approx 0$  during this interval, the effective

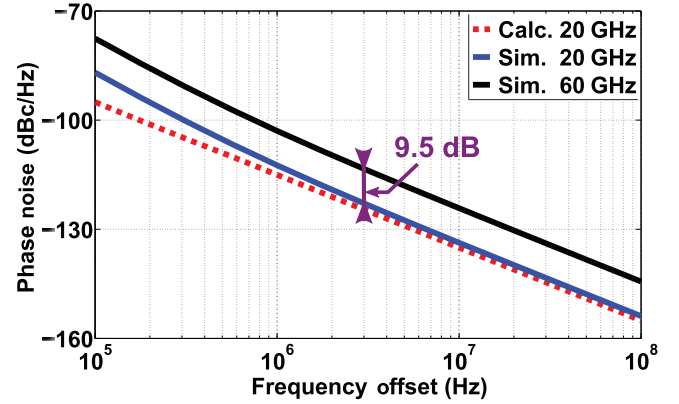


Fig. 14. Comparison between the simulated and the analytical PN results.

ISF is small. This alleviates the concerns that the small channel resistance in the deep triode region will deteriorate the PN.

To verify the validity of the PN analysis presented above, the derived equations are compared against simulations in SpectreRF at 20 GHz fundamental carrier, as shown in Fig. 14. Within the 20 dB/dec region, the difference between the calculated and the simulated PN is merely 1.3 dB, testifying to the accuracy of the presented PN analysis. Furthermore, Fig. 14 shows that the PN at the extracted 60 GHz carrier is 9.5 dB higher (as predicted) than at the 20 GHz signal.

#### IV. MORE ON THE OPERATIONAL PRINCIPLES OF THE PROPOSED OSCILLATOR

##### A. Phase Shift in the Oscillation Loop

In traditional single-port LC oscillators, there is no phase shift expected between the drain current and the voltage waveforms. In our oscillator, there are two ports (i.e., primary and secondary windings) inside the oscillation loop. Ideally, the phase shift across the two ports ( $v_s$  and  $v_p$ ) would be  $180^\circ$  for  $\omega_L = \omega_{osc}$  and  $0^\circ$  for  $\omega_H = 3\omega_{osc}$ . The gate and drain waveforms are expected to be antiphase, and the phases of the first and third harmonics in the drain waveform should be exactly aligned. However, the waveforms shown in Fig. 7 indicate that there is some unexpected phase shift between  $V_{G1}$  and  $V_{D1}$ , and also between the first and third harmonics in  $V_{D1}$ .

This phenomenon indicates that the two-port transformer-based resonator exhibits nonideal phase response. To get an insight into this phenomenon, the transfer function from primary to secondary windings is derived

$$\frac{v_s}{v_p} = - \frac{k_m \cdot \sqrt{L_s/L_p}}{1 - \alpha_s(1 - k_m^2) + \frac{\alpha_s}{Q_p Q_s} + j \left( \frac{\alpha_s}{Q_p} + \frac{\alpha_s}{Q_s} - \frac{1}{Q_p} \right)}. \quad (12)$$

Fig. 15 shows the phase response of  $v_s/v_p$  at  $\omega_L$  and  $\omega_H$  for  $k_m = 0-0.8$ . As we can see,  $\angle v_s/v_p$  is never exactly  $180^\circ$  at  $\omega_L$ , and also never exactly  $0^\circ$  at  $\omega_H$ . The nonideal phase shift decreases with larger  $k_m$  at  $\omega_L$ , while it behaves the opposite at  $\omega_H$ . To achieve an open-loop  $\angle v_s/v_{in}$  as shown in Fig. 4, the phase response of  $v_p/v_{in}$  needs to provide an extra phase shift to compensate for the  $\angle v_s/v_p$  nonideality. To realize that,



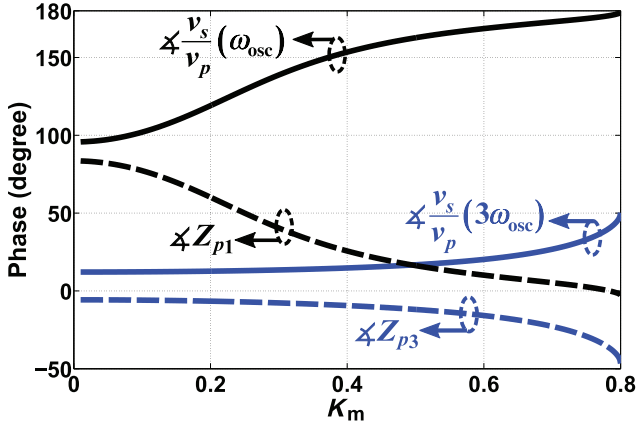


Fig. 15. Phase response of the transformer-based two-port resonant tank at fundamental and third-harmonic frequencies.

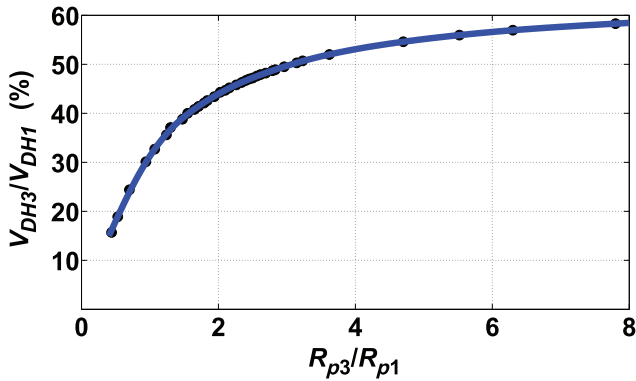


Fig. 16. Simulated dependency of  $V_{DH3}/V_{DH1}$  ratio on  $R_{p3}/R_{p1}$ .

we recognize that the tank's input impedance  $Z_{\text{tank}}$  is not a pure resistance at  $\omega_L$  and  $\omega_H$ , so the phase shift is generated between the current and the voltage waveforms at drain nodes. It is perhaps counter-intuitive at first glance. Tracing it to the source, it is the leakage inductance and the ohmic losses within each winding that contribute to the extra phase shift. Referring to (1), the phase of  $Z_{\text{tank}}$  at  $\omega_L$  ( $\angle Z_{p1}$ ) and  $\omega_H$  ( $\angle Z_{p3}$ ) is calculated and plotted in Fig. 15. As expected,  $\angle Z_{p1}$  and  $\angle Z_{p3}$  can fully compensate for the nonideal phase difference introduced in the  $v_s/v_p$  transfer path.

The nonzero  $\angle Z_{p1}$  and  $\angle Z_{p3}$  result in the phase shift between the gate and the drain voltage. The difference between  $\angle Z_{p1}$  and  $\angle Z_{p3}$  will contribute to phase misalignment between the 20/60 GHz components. Since  $\angle Z_{p1} > 0$  and  $\angle Z_{p3} < 0$ , the fundamental component always leads the third harmonic. By tuning the second resonance  $\omega_H$  to a proper frequency that is above  $3\omega_{\text{osc}}$ , it would be possible to make  $\angle Z_{p3} = \angle Z_{p1}$  and therefore eliminate that phase misalignment. However, the original reactive power balance between  $L$  and  $C$  in the steady-state oscillation tank would be perturbed. The third harmonic of the drain current has to flow through the inductive part in  $Z_{\text{trans}}(j\omega)$ , and it can facilitate the flicker noise to PN conversion [25], [40]. Simulations also show that the flicker noise corner and the close-in PN get worse in that case.

Although the nonzero  $\angle Z_{p1}$  and  $\angle Z_{p3}$  create waveform misalignment, the reactance part happens to be just a small portion

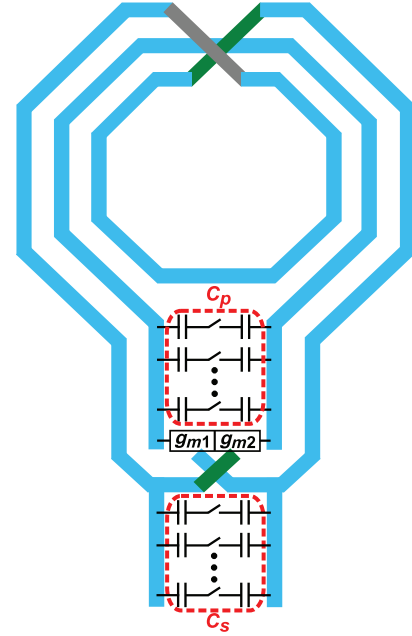


Fig. 17. Proposed layout for the transformer-based dual-tank oscillator.

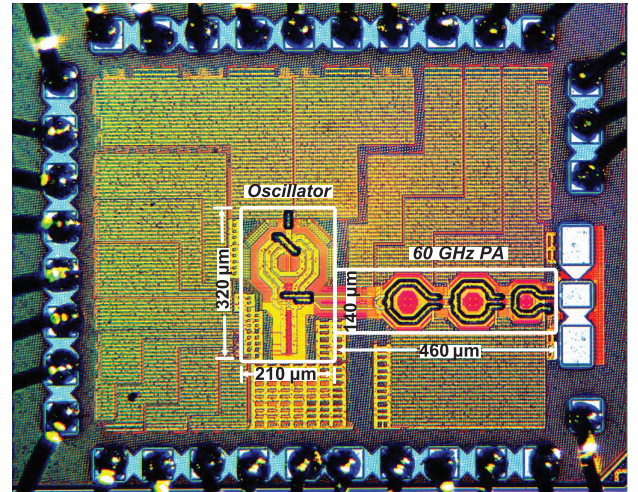


Fig. 18. Chip micrograph; the core area is  $0.13 \text{ mm}^2$ .

of  $Z_{p1}$  and  $Z_{p3}$  in our design. Without sacrificing the accuracy, we assume that  $R_{p1} \approx |Z_{p1}|$  and  $R_{p3} \approx |Z_{p3}|$  for simplicity in the PN analysis in Section III.

### B. Amount of Third Harmonic: Bounded or Not?

From Section II, we know that the  $V_{DH3}/V_{DH1}$  ratio has a positive correlation with  $R_{p3}/R_{p1}$ . This begs a question: Will  $V_{DH3}/V_{DH1}$  be unbounded with an ever-increasing  $R_{p3}/R_{p1}$ ? In the linear oscillator model, the drain current will only flow through the tank impedance represented by  $R_p$ . The third-harmonic amplitude is, therefore, proportional to  $R_{p3}$ . Therefore, until now, the answer seems to be affirmative. This model assumes that the oscillation state is time-invariant over the oscillation period. However, in our design, the absence of an ideal current source forces the proposed oscillator to somewhat deviate from the classical linear model.

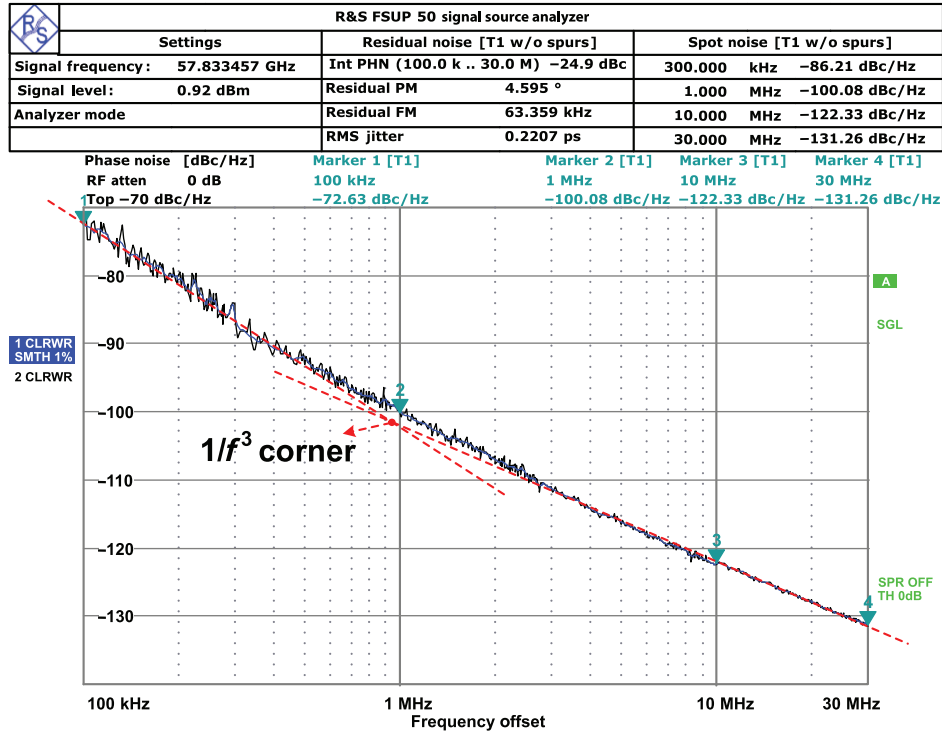


Fig. 19. Measured PN at 57.8 GHz.

Due to the lack of good isolation between the transistors and ground, the tank can directly see the loading effects of the channel resistance.  $M_1/M_2$  traverse through different operational regions (saturation, triode, and shut off) over the oscillation period, and the channel conductance ( $g_{ds}$ ) varies dramatically. Fig. 12 shows the typical  $g_{ds}(t)$  of  $M_1/M_2$  in our design. When the large fundamental-harmonic swing drives the transistor into deep triode (during 0.1–0.4 T in Fig. 7), the transistor behaves like a small resistor that conducts the drain node to ground. The inductor  $L$  stops commuting its current with the tank capacitors  $C$ , but instead leaks the current to ground through the small channel resistance. Therefore, the oscillation states are forced to change. Due to the time-variant nature of the oscillator [41], the linear model fails to characterize it. During this interval within each period, the oscillation waveform is enforced to flatten. This phenomenon will limit the maximum achievable third harmonic.

Simulations have been carried out to verify this hypothesis. In Fig. 16,  $R_{p1}$  and  $V_{DH1}$  are controlled to be constant, while  $R_{p3}$  is swept. When  $R_{p3}/R_{p1} < 1.5$ ,  $V_{DH3}/V_{DH1}$  increases dramatically with growing  $R_{p3}/R_{p1}$ . However,  $V_{DH3}/V_{DH1}$  starts to saturate after  $R_{p3}/R_{p1} > 1.5$ . Therefore, keeping on increasing  $R_{p3}/R_{p1}$  cannot increase  $V_{DH3}/V_{DH1}$  indefinitely.

## V. IMPLEMENTATION AND EXPERIMENTAL RESULTS

To demonstrate the effectiveness of the proposed mm-wave frequency generation scheme, the third-harmonic boosting oscillator together with the three-stage 60 GHz output amplifier is prototyped in TSMC 40 nm 1P7M LP CMOS. The 1:2 transformer in the oscillator uses a 3.5  $\mu\text{m}$  ultra-thick metal

(UTM) layer. Its  $k_m$  is designed to be 0.61. The differential self-inductance of primary and secondary windings is 150 and 390 pH, respectively. The  $Q$ -factors for primary and secondary windings are similar, and  $Q_p \approx Q_s = 15$  at 20 GHz. The switched-capacitors'  $Q$  is 25 at 20 GHz. In total, an overall  $Q$  of 10.5 is achieved at 20 GHz for the entire tank.

The dual-tank oscillator requires special care in layout. The dense interconnects to the two capacitor banks around the core transistors may contribute an extra parasitic inductance and undesired magnetic coupling. Therefore, the layout routing should be optimized to minimize the undesired coupling between the two capacitor banks. Due to the relatively small tank inductance and capacitance, it is sensitive to the layout asymmetry and parasitics. This makes the layout routing challenging. A layout topology is proposed in Fig. 17. The transformers in the matching network of the three amplifier stages use the UTM layer for primary windings and 1.45  $\mu\text{m}$  aluminum capping layer for secondary windings. The chip micrograph is shown in Fig. 18.

An R&S FSUP50 signal source analyzer is used with an external mixer to measure the oscillator's PN, whose plot is shown in Fig. 19 at 57.8 GHz. The oscillator's power consumption is 24 and 13.5 mW with and without the first amplifier stage, respectively. At 1 MHz offset, the PN is  $-100.1$  dBc/Hz, which is the best ever reported in CMOS. The  $1/f^3$  PN corner is 920 kHz. The 60 GHz frequency generator achieves a 25% TR from 48.4 to 62.5 GHz.

To verify the suppression of the fundamental tone at  $\sim 20$  GHz, the spectrum is measured around the 58.75 GHz carrier and also from 0 to 50 GHz, as shown in Fig. 20. At 1 V supply, the three-stage amplifier delivers a maximum of +6 dBm to the 50  $\Omega$  load while consuming 58 mW. The

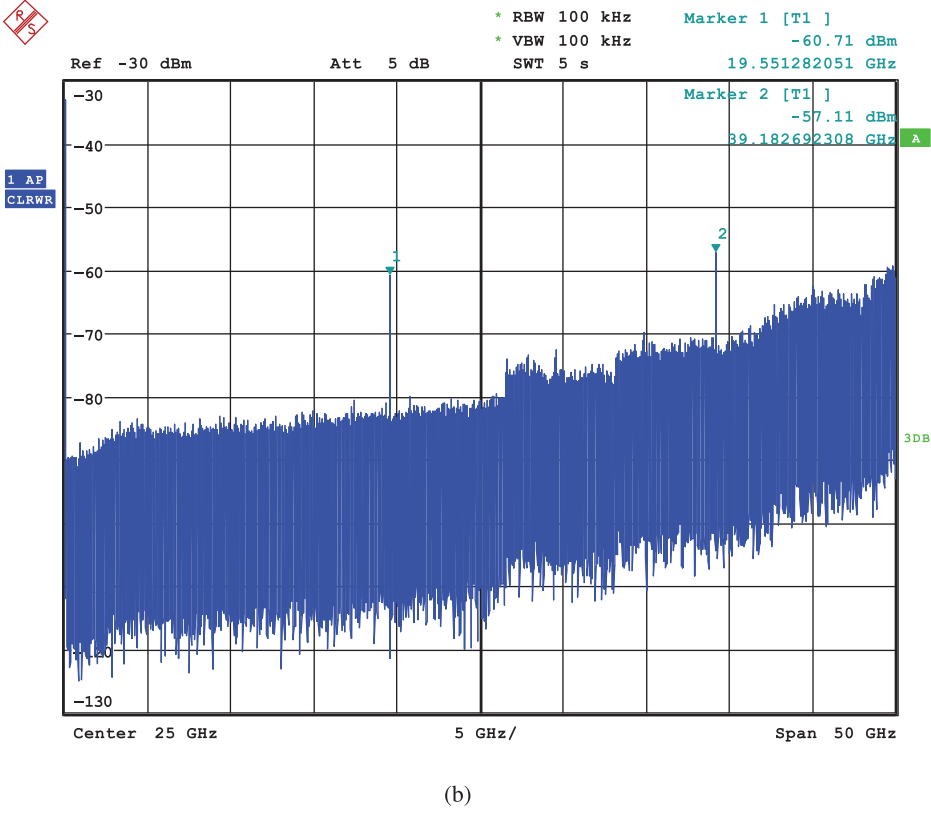
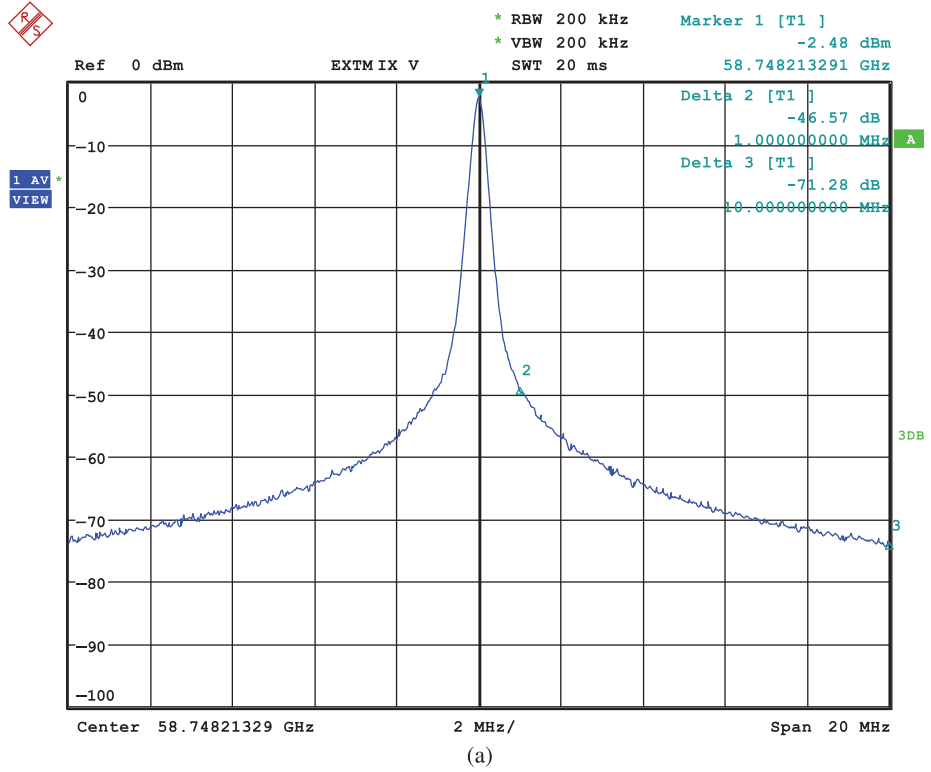


Fig. 20. Measured spectrum at (a) 58.75 GHz and (b) 0–50 GHz.

output power across the oscillator’s TR is shown in Fig. 21(a). Since wideband amplifiers are not the focus in this work, the bandwidth of the amplifiers is not large enough to cover the oscillator’s 25% TR, hence the drop in amplitude at <math>< 54\text{ GHz}</math>.

The literature offers a number of wideband techniques [45] to extend the amplifier bandwidth. The measured power of the  $\sim 20\text{ GHz}$  fundamental is  $-56.5\text{ dBm}$ , which is 62 dB below the carrier. The second harmonic at  $\sim 40\text{ GHz}$  is visible at

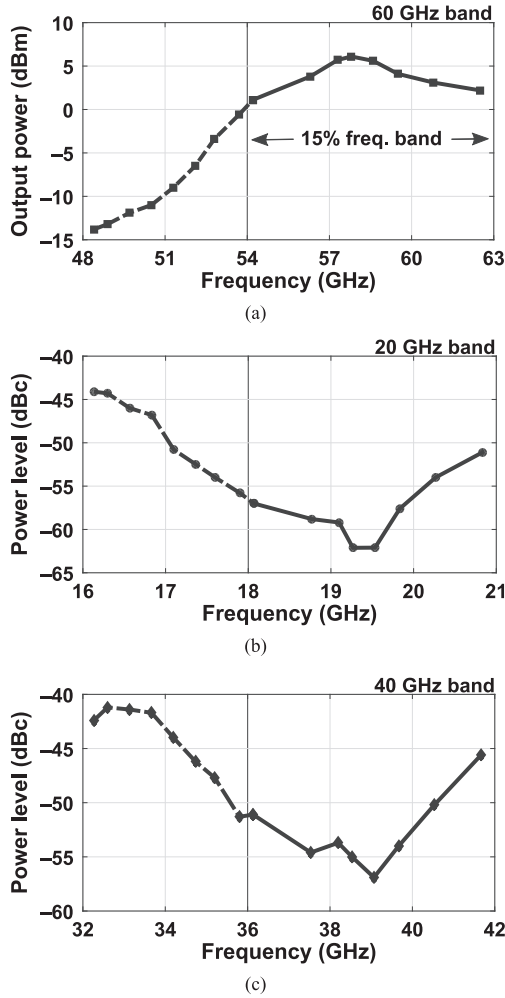


Fig. 21. Measured power level at (a) 60 GHz band; (b) fundamental frequency; and (c) second harmonic.

-51.5 dBm, which is -57 dBc. The leakage power level of the fundamental and second-harmonic tone at the output across the TR is shown in Figs. 21(b) and (c). When the amplifiers are supplied at a reduced  $V_{DD} = 0.7$  V, they deliver 0 dBm maximum while consuming 22 mW. The HRR varies only 3 dB when changing  $V_{DD}$  between 0.7 and 1 V. The fundamental and second-harmonic power levels satisfy the out-of-band emission mask in IEEE 802.11ad [1] and FCC regulations [31] with sufficient margin. This demonstrates that with the natural filtering from a multistage PA in the TX, the 20 GHz residual emission is not an issue.

Fig. 22 shows the PN at 1 MHz offset and the corresponding FoM across the 25% TR. In Fig. 22(b), the power consumption of the first amplifier stage (10.5 mW from 1 V) is included in the FoM calculation. When taking the total power consumption of the three amplifier stages (22 mW from 0.7 V) into account, the FoM drops by 1.7 dB. The PN varies between -98.8 and -100.1 dBc/Hz. The corresponding FoM changes between 179 and 181.9 dBc/Hz across the frequency range. Since the switched capacitors have lower  $Q$ -factor in on-state, the FoM at lower frequencies decreases.

Compared to traditional 60 GHz oscillators, the proposed solution offers several advantages. Larger  $L$  and  $C$  of the

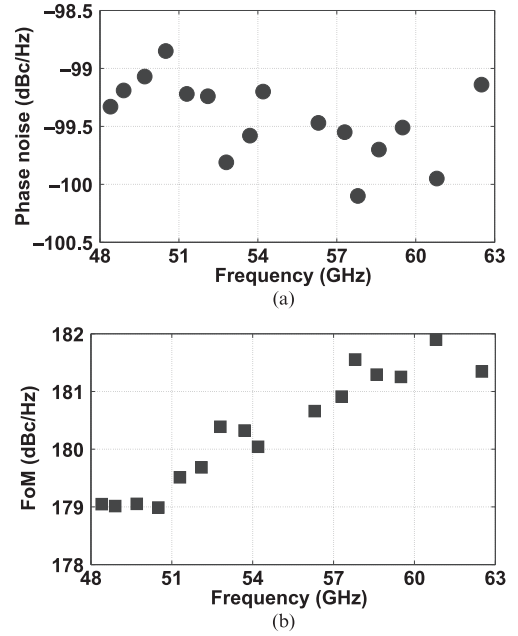


Fig. 22. (a) Measured PN at 1 MHz offset and (b) corresponding FoM across the TR.

tank lowers its sensitivity to parasitics, thus resulting in wider TR. The relatively small contribution of the nonlinear parasitic capacitance from the core transistors points to less  $1/f$  noise upconversion. Oscillation at 20 GHz benefits from a better  $Q$ -factor of the resonant tank. The third-harmonic injection reduces the ISF value, thus lowering the PN.

Table I summarizes the performance of the proposed 60 GHz frequency generator and compares it with the relevant state-of-the-art. The PN is the best, and advances state-of-the-art by 4.3 dB at 1 MHz offset. Since the output of the first amplifier stage could not be directly probed in this chip, two sets of FoM and  $FoM_T$  are included: 1) with the power consumption of the first amplifier stage at  $V_{DD} = 1.0$  V and 2) with the total power consumption of the three amplifier stages at  $V_{DD} = 0.7$  V. Compared to state-of-the-art designs which also include 60 GHz frequency dividers/multipliers [6], [11], [24], [42], [44], our achieved FoM and  $FoM_T$  are, respectively, >3 and >5 dB better.

## VI. CONCLUSION

A 60 GHz frequency generator based on third-harmonic boosting and extraction is proposed to improve power efficiency and PN performance of a 60 GHz PLL. A harmonic boosting technique is described and applied to a 20 GHz oscillator to increase its third-harmonic level. Analysis of the oscillator operational principles are provided for better performance optimization. PN mechanism is investigated and an analysis approach is developed to account for the multiple tank resonances as well as the time-varying channel noise. The undesired fundamental tone at 20 GHz is suppressed by the fundamental HRR inherent with the oscillator buffer stage, and the 60 GHz component appears amplified at the output. Prototyped in 40 nm CMOS, the frequency generator advances the state-of-the-art

TABLE I  
PERFORMANCE COMPARISON WITH THE STATE-OF-THE-ART 60 GHz OUTPUT OSCILLATOR SYSTEMS

Technology (nm)		This work	[42]	[43]	[15]	[16]	[6]	[24]	[44]	[11]
Type		Harmonic extraction	Fundamental	Fundamental	Fundamental	Fundamental	Fundamental	Freq. tripling	Freq. tripling	CM extraction
$P_{DC}$ (mW)	Osc.	13.5	14	3.9	8.1	8.4–10.8	14	24	10.6	42
	buf./amplif.	10.5 <sup>1</sup> 22 <sup>2</sup>	NA	NA	NA	NA	NA	NA	NA	
	$\times / \div$ <sup>3</sup>	0	4.8	NA	NA	NA	10	23.3	14	
$V_{DD}$ (V)		0.7/1   0.7	1.2	1	0.7	1.2	0.9	1.2/1	1.2	1
Tuning range (GHz)		48.4–62.5 (25.4%)	55.8–61.6 (9.8%)	59–65.2 (10%)	53.2–58.4 (9.3%)	57.5–90.1 (41.1%)	53.8–63.3 (16%)	70.5–85.5 (19.2%)	58.3–65.4 (11.5%)	46.4–58.1 (22.4%)
PN (dBc/Hz)	1 MHz	–100.1	–94	–95/–91	–91	NA	–91 to –94.5	–91.7 to –95.8	NA	–89
	10 MHz	–122.3	NA	NA	NA	–104.6 to –112.2	NA	NA	–115	–118
FoM (dBc/Hz)	1 MHz	181.5 <sup>1</sup> 179.8 <sup>2</sup>	176.8	185/181	177.2	NA	172.7–175.4	176.6	NA	167.7
	10 MHz	183.7 <sup>1</sup> 182 <sup>2</sup>	NA	NA	NA	172–180	NA	NA	176.9	176.7
FoM <sub>T</sub> (dBc/Hz)	1 MHz	189.6 <sup>1</sup> 187.9 <sup>2</sup>	176.6	185/181	176.6	NA	176.6–179.5	182.6	NA	174.7
	10 MHz	191.8 <sup>1</sup> 190.1 <sup>2</sup>	NA	NA	NA	184.2–192.2	NA	NA	178.1	183.7

<sup>1</sup>Including the power consumption of the first buffer/amplifier stage (10.5 mW) at  $V_{DD} = 1.0$  V.

<sup>2</sup>Including the total power consumption of the three amplifier stages (22 mW) delivering 0 dBm at  $V_{DD} = 0.7$  V.

<sup>3</sup>Power consumption of the 60 GHz frequency divider or multiplier.

PN performance by 4.3 dB. It is worth to note that the ready presence of the 20 GHz output will significantly help with the feedback phase detection, thus improving the power efficiency and reducing the hardware complexity when used in a PLL.

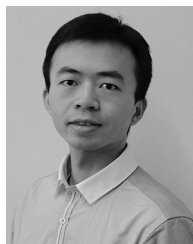
#### ACKNOWLEDGEMENT

We acknowledge TSMC university shuttle program for chip fabrication, Integrand Software for EMX license, and Atef Akhnouk, and Wil Straver for measurement supports.

#### REFERENCES

- [1] Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications Amendment 3: Enhancements for Very High Throughput in the 60 GHz Band, IEEE Standard 802.11ad, 2012.
- [2] S. Emami *et al.*, “A 60 GHz CMOS phased-array transceiver pair for multi-Gb/s wireless communications,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2011, pp. 164–166.
- [3] M. R. Khanzadi *et al.*, “Calculation of the performance of communication systems from measured oscillator phase noise,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 5, pp. 1553–1565, May 2014.
- [4] W. Wu, R. B. Staszewski, and J. R. Long, “A 56.4-to-63.4 GHz multi-rate all-digital fractional-N PLL for FMCW radar applications in 65 nm CMOS,” *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1081–1096, May 2014.
- [5] X. Yi *et al.*, “A 57.9-to-68.3 GHz 24.6 mW frequency synthesizer with in-phase injection-coupled QVCO in 65 nm CMOS technology,” *IEEE J. Solid-State Circuits*, vol. 49, no. 2, pp. 347–359, Feb. 2014.
- [6] V. Szortyka, Q. Shi, K. Raczkowski, B. Parvais, M. Kuijk, and P. Wambacq, “A 42 mW 230 fs-jitter sub-sampling 60 GHz PLL in 40 nm CMOS,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2014, pp. 366–367.
- [7] S. Kang, J.-C. Chien, and A. M. Niknejad, “A W-band low-noise PLL with a fundamental VCO in SiGe for millimeter-wave applications,” *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 10, pp. 2390–2404, Oct. 2014.
- [8] A. Musa *et al.*, “A low phase noise quadrature injection locked frequency synthesizer for mm-wave applications,” *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2635–2649, Nov. 2011.
- [9] W. Deng *et al.*, “A sub-harmonic injection-locked quadrature frequency synthesizer with frequency calibration scheme for millimeter-wave TDD transceivers,” *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1710–1720, Jul. 2013.
- [10] A. Li *et al.*, “A 21–48 GHz sub-harmonic injection-locked fractional-N frequency synthesizer for multi-band point-to-point backhaul communications,” *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1785–1799, Aug. 2014.
- [11] B. Sadhu, M. Ferriss, and A. Valdes-Garcia, “A 46.4–58.1 GHz frequency synthesizer featuring a 2nd harmonic extraction technique that preserve VCO performance,” in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2014, pp. 173–176.
- [12] Y. Chao, H. C. Luong, and Z. Liang, “Analysis and design of a 14.1-mW 50/100-GHz transformer-based PLL with embedded phase shifter in 65-nm CMOS,” *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 4, pp. 1193–1201, Apr. 2015.
- [13] B. Catli and M. M. Hella, “Triple-push operation for combined oscillation/division functionality in millimeter-wave frequency synthesizers,” *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1575–1589, Aug. 2010.
- [14] C. Cao and K. K. O, “Millimeter-wave voltage-controlled oscillators in 0.13- $\mu$ m CMOS technology,” *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1297–1304, Jun. 2006.
- [15] L. Li, P. Reynaert, and M. S. J. Steyaert, “Design and analysis of a 90 nm mm-wave oscillator using inductive-division LC tank,” *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 1950–1958, Jul. 2009.
- [16] J. Yin and H. C. Luong, “A 57.5–90.1-GHz magnetically tuned multimode CMOS VCO,” *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1851–1861, Aug. 2013.
- [17] Y.-H. Wong, W.-H. Lin, J.-H. Tsai, and T.-W. Huang, “A 50-to-62 GHz wide-locking-range CMOS injection-locked frequency divider with transformer feedback,” in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2008, pp. 435–438.
- [18] Q. Gu *et al.*, “A low power-band CMOS frequency divider with wide locking range and accurate quadrature output phases,” *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 991–998, Apr. 2008.
- [19] S. Rong, A. W. L. Ng, and H. C. Luong, “0.9 mW 7 GHz and 1.6 mW 60 GHz frequency dividers with locking-range enhancement in 0.13  $\mu$ m CMOS,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2009, pp. 96–97.
- [20] Y. Chao and H. C. Luong, “Analysis and design of a 2.9-mW 53.4–79.4-GHz frequency-tracking injection-locked frequency divider in 65-nm CMOS,” *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2403–2418, Oct. 2013.
- [21] L. Wu and H. C. Luong, “Analysis and design of a 0.6 V 2.2 mW 58.5-to-72.9 GHz divide-by-4 injection-locked frequency divider with harmonic boosting,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 8, pp. 2001–2008, Aug. 2013.
- [22] W. L. Chan and J. R. Long, “A 56–65 GHz injection-locked frequency tripler with quadrature outputs in 90-nm CMOS,” *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2739–2746, Dec. 2008.
- [23] G. Mangraviti *et al.*, “A 52–66 GHz subharmonically injection-locked quadrature oscillator with 10 GHz locking range in 40 nm LP CMOS,” in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2012, pp. 309–312.
- [24] Z. Huang, H. C. Luong, B. Chi, Z. Wang, and H. Jia, “A 70.5-to-85.5 GHz 65 nm phase-locked loop with passive scaling of loop filter,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2015, pp. 448–449.

- [25] J. J. Rael and A. A. Abidi, "Physical processes of phase noise in differential LC oscillators," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2000, pp. 569–572.
- [26] Z. Zong, M. Babaie, and R. B. Staszewski, "A 60 GHz 25% tuning range frequency generator with implicit divider based on third harmonic extraction with 182 dBc/Hz FoM," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, May 2015, pp. 279–282.
- [27] H. Kim, S. Ryu, Y. Chung, J. Choi, and B. Kim, "A low phase-noise CMOS VCO with harmonic tuned LC tank," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 7, pp. 2917–2923, Jul. 2006.
- [28] M. Babaie and R. B. Staszewski, "A class-F CMOS oscillator," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3120–3133, Dec. 2013.
- [29] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 331–343, Mar. 1996.
- [30] Y.-L. Yeh and H.-Y. Chang, "A W-band wide locking range and low dc power injection-locked frequency tripler using transformer coupled technique," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 2, pp. 860–870, Feb. 2013.
- [31] Federal Communications Commission. (2013 Aug.) *Rules for Unlicensed Operation in the 57–64 GHz Band* [Online]. Available: <https://www.fcc.gov/document/part-15-rules-unlicensed-operation-57-64-ghz-band>
- [32] K. Okada, *et al.*, "A full 4-channel 6.3 Gb/s 60 GHz direct-conversion transceiver with low-power analog and digital baseband circuitry," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2012, pp. 218–220.
- [33] K. Okada *et al.*, "A 64-QAM 60 GHz CMOS transceiver with 4-channel bonding," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2014, pp. 346–347.
- [34] W. L. Chan and J. R. Long, "A 60-GHz band 2×2 phased-array transmitter in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2682–2695, Dec. 2010.
- [35] V. Vidojkovic *et al.*, "A low-power 57-to-66 GHz transceiver in 40 nm LP CMOS with 17 dB EVM at 7 Gb/s," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2012, pp. 268–270.
- [36] W. L. Chan and J. R. Long, "A 58–65 GHz neutralized CMOS power amplifier with PAE above 10% at 1-V supply," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 554–564, Mar. 2010.
- [37] S. K. Reynolds *et al.*, "A silicon 60-GHz receiver and transmitter chipset for broadband communications," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2820–2830, Dec. 2006.
- [38] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.
- [39] D. Murphy, J. J. Rael, and A. A. Abidi, "Phase noise in LC oscillators: A phasor-based analysis of a general result and of loaded," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 6, pp. 1187–1203, Jun. 2010.
- [40] J. Groszkowski, "The interdependency of frequency variation and harmonic content, and the problem of constant-frequency oscillators," *Proc. IRE*, vol. 21, no. 7, pp. 958–981, Jul. 1933.
- [41] L. Fanori and P. Andreani, "Class-D CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3105–3119, Dec. 2013.
- [42] W. Wu, J. R. Long, and R. B. Staszewski, "High-resolution millimeter-wave digitally controlled oscillators with reconfigurable passive resonators," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2785–2794, Nov. 2013.
- [43] J. Borremans *et al.*, "VCO design for 60 GHz using differential shielded inductors in 0.13  $\mu\text{m}$  CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, 2008, pp. 135–138.
- [44] T. Siriburano *et al.*, "A 60-GHz sub-sampling frequency synthesizer using sub-harmonic injection-locked quadrature oscillators," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2014, pp. 105–108.
- [45] S. V. Thyagarajan, A. M. Niknejad, and C. D. Hull, "A 60 GHz drain-source neutralized wideband linear power amplifier in 28 nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 8, pp. 2253–2162, Aug. 2014.



**Zhirui Zong** (S'12) received the B.Eng. degree (with honors) in electronic and information engineering from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2012. He is currently working toward the Ph.D. degree in electrical engineering at Delft University of Technology, Delft, The Netherlands.

His research interests include frequency synthesizer techniques and integrated circuits for RF/mm-wave transceivers.



**Masoud Babaie** (S'12) received the B.Sc. degree (with highest honors) in both communication systems and electronics engineering from Amirkabir University of Technology (Tehran Polytechnic), Tehran, Iran, in 2004, and the M.Sc. degree in microelectronics from Sharif University of Technology, Tehran, Iran, in 2006. He is currently working toward the Ph.D. degree in electrical engineering at Delft University of Technology, Delft, The Netherlands.

He joined Kavoshcom R&D Group, Tehran, Iran, in 2006, where he was involved in designing tactical communication systems.

He was appointed a CTO of the company between 2009 and 2011. He was consulting for the RF Group of TSMC, Hsinchu, Taiwan, from 2013 to 2015, designing 28 nm all-digital PLL and Bluetooth low-energy transceiver chips. From 2014 to 2015, he was a Visiting Scholar Researcher at Berkeley Wireless Research Center (BWRC), Berkeley, CA, USA, within the group of Prof. Ali Niknejad. His research interests include analog and RF/mm-wave integrated circuits and systems for wireless communications.

Mr. Babaie serves as a reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He was the recipient of the 2015–2016 IEEE Solid-State Circuits Society (SSCS) Predoctoral Achievement Award.



**Robert Bogdan Staszewski** (M'97–SM'05–F'09) was born in Bialystok, Poland. He received the B.Sc. (*summa cum laude*), M.Sc., and Ph.D. degrees in electrical engineering from the University of Texas at Dallas, TX, USA, in 1991, 1992, and 2002, respectively.

From 1991 to 1995, he was with Alcatel Network Systems, Richardson, TX, USA, working on SONET cross-connect systems for fiber optics communications. He joined Texas Instruments, Dallas, TX, USA, in 1995, where he was elected as a Distinguished

Member of Technical Staff (limited to 2% of technical staff). Between 1995 and 1999, he was engaged in advanced CMOS read channel development for hard disk drives. In 1999, he co-started a Digital RF Processor (DRP) Group within Texas Instruments with a mission to invent new digitally intensive approaches to traditional RF functions for integrated radios in deeply scaled CMOS processes. He was appointed a CTO of the DRP Group between 2007 and 2009. In July 2009, he joined Delft University of Technology, Delft, The Netherlands, where he is currently a part-time Full Professor. Since September 2014, he has been a Professor with the University College Dublin (UCD), Dublin, Ireland. He has authored/coauthored 3 books, 5 book chapters, 190 journal and conference publications, and holds 140 issued U.S. patents. His research interests include nanoscale CMOS architectures and circuits for frequency synthesizers, transmitters, and receivers.

Dr. Staszewski has been a TPC member of ISSCC, RFIC, ESSCIRC, ISCAS, and RFIT. He was the recipient of the IEEE Circuits and Systems Industrial Pioneer Award.