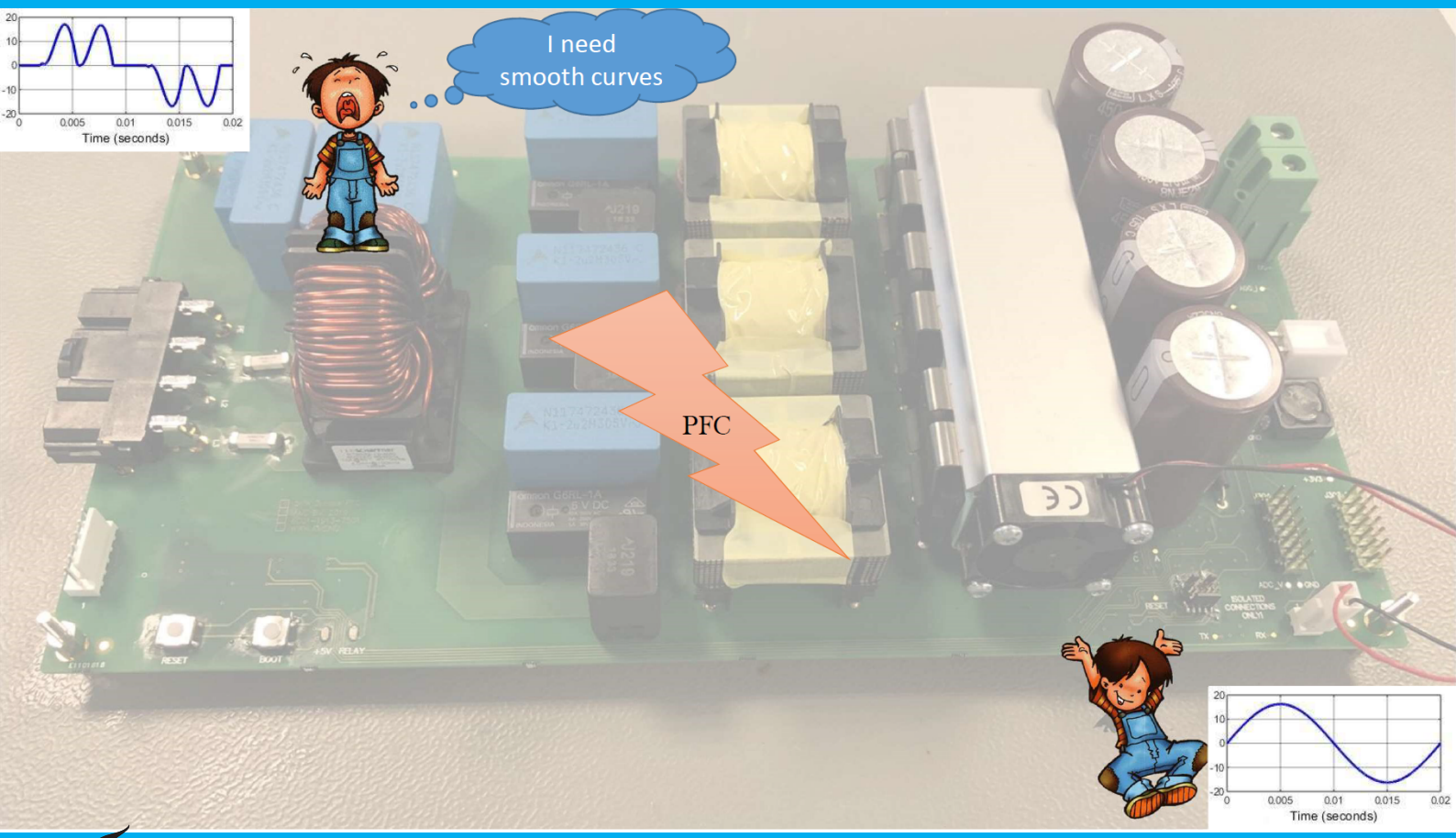
Low-cost uni-directional PFC for 3-phase systems

P. Chitlure Prahallad

3 ϕ Power factor correction
The device which can even correct the 3 phase power !!!



TU Delft

Low-cost uni-directional PFC for 3-phase systems

by

P. Chitlure Prahallad

to obtain the degree of Master of Science
at the Delft University of Technology,
to be defended publicly on Friday May 24, 2019 at 14:00.

Student number:	4735447	
Project duration:	September 3, 2018 – May 24, 2019	
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This thesis is confidential and cannot be made public until May 24, 2021.

TU Delft

Preface

This thesis is submitted for the accomplishment of the degree of Master of Science at TU Delft. The research described herein was conducted under the supervision of prof. dr. ir. P. Bauer, TU Delft and dr. ir. Jan Schellekens, Applied Micro Electronics "AME" B.V. at the company Applied Micro Electronics "AME" B.V., Eindhoven.

Power consumed by any equipment connected to the grid must be regulated to facilitate the reliable and efficient operation of the grid and for smooth equipment operation of other consumers. Power factor is one of the major power quality measurement tool. All the electrical equipment connected to the grid must comply with the power factor limits as specified under various standards. This thesis aims at the development of a cost-effective power factor correction converter for a motor drive with a power range up to 10 kW, which is also robust for line and load transients.

Even though I am not a great believer, I would like to thank god for his grace towards the completion of this project.

I would like to take this moment to thank my thesis supervisor prof. dr. ir. P. Bauer for his support and encouragement in the completion of this thesis. And, I would like to thank Sharmila Rattansingh, for her constant support in non-technical activities for this thesis.

I would like to thank dr. ir. Jan Schellekens of AME for his constant support and advice which were really important for the successful development of the prototype. I would also thank my colleagues at AME, who constantly helped me whenever I was stuck during my design and development stages of the prototype.

I would like to take this opportunity to thank my friends in Europe and my friends from India, who lightened my mood whenever I was feeling low. I would like to convey my heartfelt thanks to the crush of my life, whose constant remembrance kept me motivated to finish my graduation soon.

Last but not least, I would like to thank my parents, brother and rest of the family members for their constant understanding, support and encouragement throughout this masters course.

P. Chitlure Prahallad
Delft, May 2019

Contents

1 Introduction

Electrical motors play a vital role in present-day life. Right from the device which can tell time, up to but not limited to the devices which wander in space, almost every electrical apparatus which can move has a motor in it. The advent of Power Electronics has boosted the applications of motors further, due to the capability of versatile control of motors. But along with this advantage, the advancement of power electronic circuits are introducing harmonics (fluctuations) in grid voltage and current and are causing additional losses in the power grid. This lowers the power transmission capacity of the grid. These harmonics may also damage the other equipment connected to the grid. In order to avoid these, there are various grid standards which govern the power quality utilized by the equipment connected to the grid. Power factor correction (PFC) circuits can be used in the electrical equipment to improve the quality of power used by it.

Depending on the application, motors might be rated from a few milliwatts up to megawatts of power. Standard IEC 61000-3-2 defines the harmonic limits for the equipment input current up to 16 A per phase, i.e. about 10 kW of power for three-phase equipment. This thesis aims at the investigation of a cost-effective power factor correction device for these three-phase motor drives which are rated up to 10 kW of power.

1.1. Document structure

The report has been divided into several chapters for the ease of understanding. The first chapter begins with the basic definitions and the system overview. After the basics, a brief analysis of the different available topologies of PFC circuits is done and discusses the system under consideration. Finally, the chapter ends with a discussion regarding the research question and the methodology in which the thesis has been carried out.

The second chapter briefs about the working of the converter, and it includes the novel control system design for the robust operation of the converter, along with its stability analysis.

The third chapter deals with the detailed design of the converter. It includes the estimation of the power circuit losses and the estimation of the power circuit volume to decide the frequency of operation of the system. Apart from the power circuit, the converter requires control circuit, auxiliary circuits and additional components for the proper functioning of the converter. These as well are discussed in the third chapter.

The final chapter discusses the experimental results of the designed converter. It also discusses the possible areas of future research for the proposed converter and its control strategy.

1.2. Standards and definitions

Total harmonic distortion: The amount of distortion in the voltage or current waveform is qualified by means of an index called the total harmonic distortion (THD)[9].

The THD in the current is defined as,

$$\text{THD} = \sqrt{\sum_{h\neq 1}^{\infty} \frac{I_h}{I_1}}$$

Displacement power factor: Displacement power factor (DPF) is the cosine of the phase angle between the current and voltage fundamental sine waves.

DPF is defined as, DPF = $\cos\phi$, where ϕ is the phase angle between the current and voltage.

Power factor: The power factor (PF) of an AC electrical power system is defined as the ratio of the real power absorbed by the load to the apparent power flowing in the circuit.

The power factor can be expressed as,

$$\text{PF} = \frac{1}{1+\text{THD}^2}\text{DPF} = \frac{\text{Real Power}}{\text{Apparent Power}}$$

IEC 61000-3-2: IEC 61000-3-2 is an international standard that limits mains voltage distortion for equipment input current ≤16 A per phase by prescribing the maximum value for harmonic currents from the second harmonic up to and including the 40^{th} harmonic current.

CISPR 14-1:2005: CISPR 14-1:2005 is an international standard which defines the Electromagnetic compatibility requirements for household appliances electric tools and similar apparatus. This standard applies to radio frequency disturbances from appliances whose main functions are performed by motors, switching or regulating devices, or by RF generators used in induction cooking appliances.

1.3. System overview

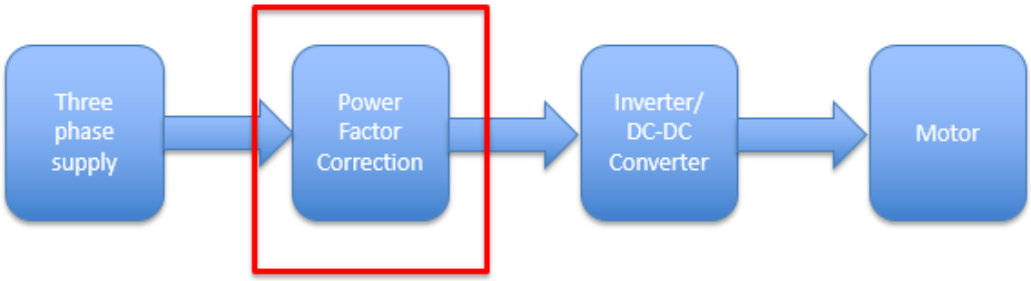


Figure 1.1: Complete system overview for a three-phase motor drive

The complete system overview of a three-phase motor drive is as shown in figure 1.1. The motor is powered using a motor driver circuit which will be either an inverter or a DC/DC converter depending on the type of the motor is used. A power factor correction circuit is necessary to make sure that the power factor of the power processed by the motor and drive is complying the limits prescribed by the harmonic standards. Thus a power factor correction converter is placed before the motor drive while powering it. The main focus of this thesis is the development of the power factor correction converter which can generate a DC power output while regulating the input power factor according to the Harmonic standard.

1.4. PFC topologies

PFCs can be either passive or active. Passive PFCs do not require any control and are made up of passive devices like inductors and capacitors. Generally, they are big and yet the power factor of the equipment will be still low. Thus they are only suitable for low powered equipment whose power is in the range of few watts. Active PFCs generally have switching devices along with passive devices. They are usually smaller, and cheaper compared to passive PFCs. Also, they can produce power factors in the range of 0.99 with a THD less than 10 %.

For the sake of comparison, three-phase active PFCs are further classified as PFCs with fewer (<4) switches and PFC with many (>4) switches. It might appear that the topologies with more number of switches will be costlier, but when compared thoroughly, the cost difference between these topologies appears negligible, and it also suggests that for higher power applications, the topologies with many switches seem more cost-effective.

For the comparison, few well known topologies have been neglected since they are not cost effective. These topologies are as follows:

- Ćuk converter:
  - Similar to buck boost converter with opposite polarity.
  - Necessity of a high energy capacitor in line, which makes the topology costly and bulky[2].
- SEPIC converter:
  - Similar to Ćuk converter, but with non-inverted polarity.
  - It has more components than the Ćuk converter, which makes it much costlier topology[2].
- Resonant converter:
  - Energy is transferred with the help of LC tank circuits.
  - THD is reduced compared to a discontinuous conduction mode operated PFC.
  - The tank circuits increases the cost and space[3].

Apart from the above-mentioned topologies, buck converter topologies are also not considered, to make the comparison among the similar type of converters. However, for comparison among the buck converter PFCs, [5] can be referred.

The following topologies have been compared briefly to obtain a cost-effective solution for a unidirectional PFC in the power range up to 10 kW. They are sorted according to the increase in complexity of the circuit.

- Passive PFCs:
  - Single inductor passive PFC
  - Triple inductor passive PFC
  - Three phase rectifier Slim DC Link
- Active PFCs with fewer switches:
  - Single switch single inductor PFC
  - Single switch traditional PFC
  - Three switch bridgeless PFC
- Active PFCs with many switches:
  - Six switch bidirectional PFC
  - Hybrid 3rd harmonic current injector PFC
  - Delta-switch boost converter
  - Vienna rectifier

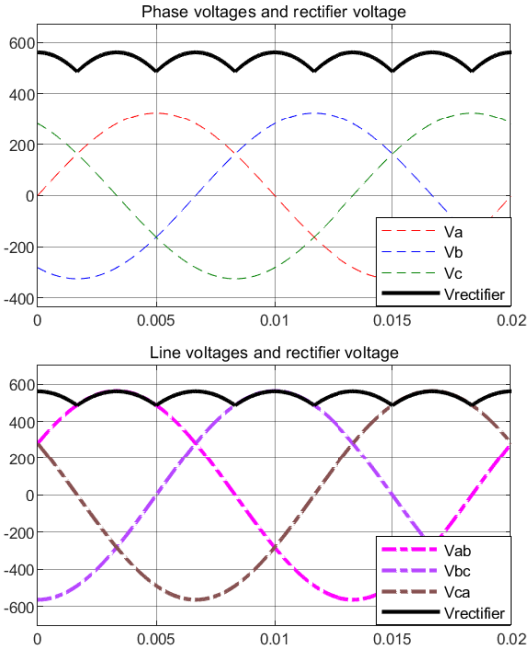
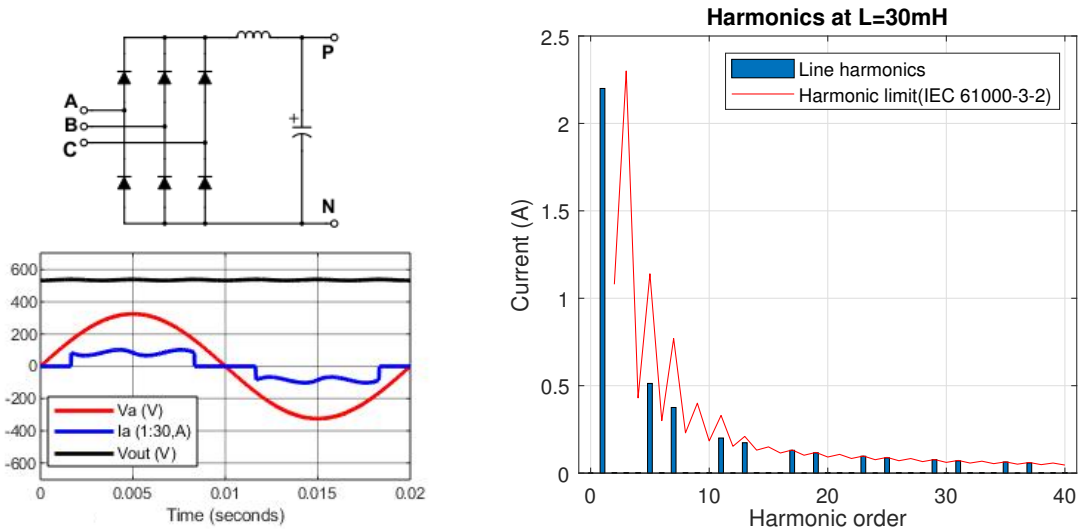


Figure 1.2: Three phase rectifier waveform

A brief investigation of these topologies is given in the upcoming sub-sections.

1.4.1. Single inductor passive PFC

The topology is just a simple extension of three-phase rectifier as seen in Figure 1.3(a). The inductor smooths the rectified current, but can't control the current in any of the phases.

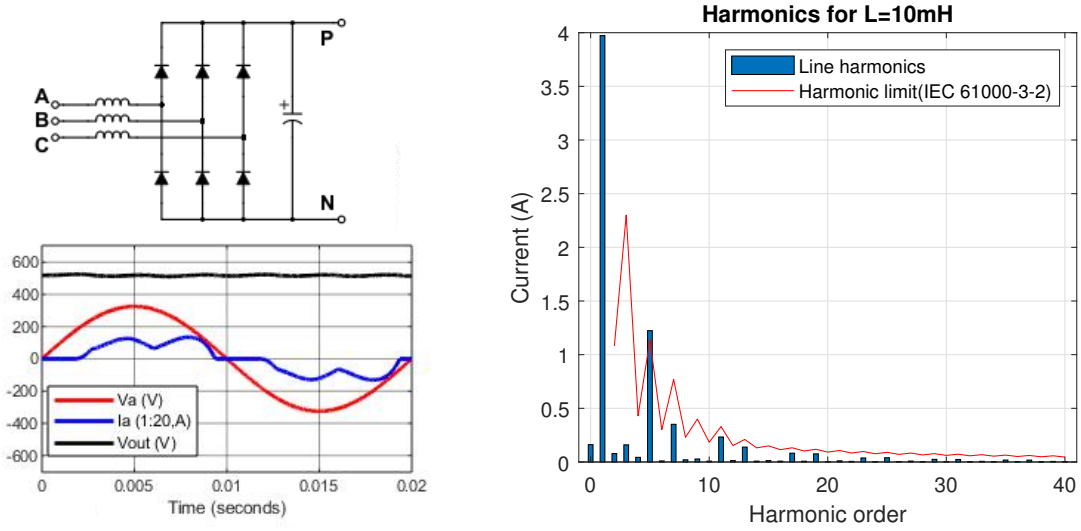


(a) (b)

Figure 1.3: Single inductor passive PFC: (a) Circuit and waveform; (b) THD spectrum for L=30mH

Since, for a three-phase rectifier in positive half cycle, each phase voltage is effective only after a phase angle of 30° and till 150°, see figure 1.2. Thus the current in each phase will also be present only for the same phase angles. Since the current in each phase will not be an exact sine wave, it contains a lot of low order frequency harmonics and it is difficult to achieve higher current output while satisfying harmonic standards, see figure 1.3(b).

According to simulations, while satisfying harmonic standards, it can just carry a power of 0.95 kW with 6 mH inductor and will require a 30 mH inductor to carry 1.5 kW of power. From this, we can infer that a passive single inductor PFC would require a very big inductor as the output power is increased. Inductor being one of the major cost deciding component of the PFC, it is unwise to use a single inductor passive PFC for higher power levels.



(a) (b)

Figure 1.4: Triple inductor passive PFC: (a) Circuit and waveform; (b) THD spectrum for L=10mH

1.4.2. Triple inductor passive PFC

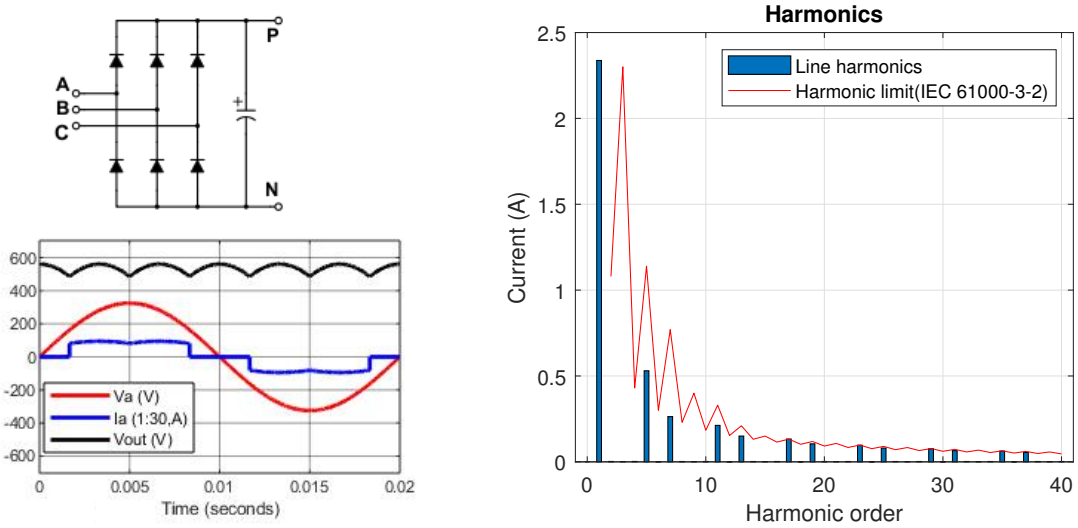
The topology is an extension of the single inductor passive PFC. It can be obtained by adding the inductors to each phase instead of having a common DC inductor, as seen in figure 1.4(a).

As discussed in the previous topology, for a passive rectifier, each phase conducts for only 120°. Thus, the current will not be sinusoidal. According to simulations, while satisfying harmonic standards, it can carry a power of 0.7 kW with 2 mH inductors and 2.5 kW with 10 mH inductors (To have a fair comparison, inductors of value one third with respect to single inductor version are used). The THD spectrum for this circuit is as shown in figure 1.4(b). When compared to the previous topology, this topology can deliver a higher power without exceeding the standard limits at higher inductance values. From this, it can be inferred that the passive triple inductor PFC could carry higher power than a single inductor passive PFC. But the inductors of these passive topologies are big and are not preferable to use for higher powers.

1.4.3. Three phase rectifier slim DC link

For a three-phase rectifier, if the DC side capacitor is too small or removed, a slim DC link three-phase rectifier is obtained. Due to the low output capacitance, a 6^{th} harmonic ripple is observed in the output of the rectifier, see figure 1.5(a). Since a motor drive doesn't require a constant input voltage, a slim DC link can be used as a low-cost option for low powered applications.

Since there is no requirement of a constant DC output voltage, the harmonic components in the AC side appear to be lesser than that for a triple inductor passive PFC and thus can be a suitable option for applications where reasonable DC side harmonics are accepted. The THD spectrum for this circuit is as shown in figure 1.5(b). According to simulations, while satisfying harmonic standards, it can convert the power of 1.6 kW. The simulations were carried for a resistive load with no load capacitor. For motor drive applications, a small DC link capacitor would be recommended to filter out switching harmonics and for other purposes. This addition of a capacitor would stabilize the DC voltage but increases the harmonics at the AC side. Also, there will be a resonance due to grid inductance and the small DC link capacitor, which further adds more ripples. Hence, for an actual motor drive application, the power that can be converted while satisfying the harmonic limit will be much lesser than 1.6 kW.



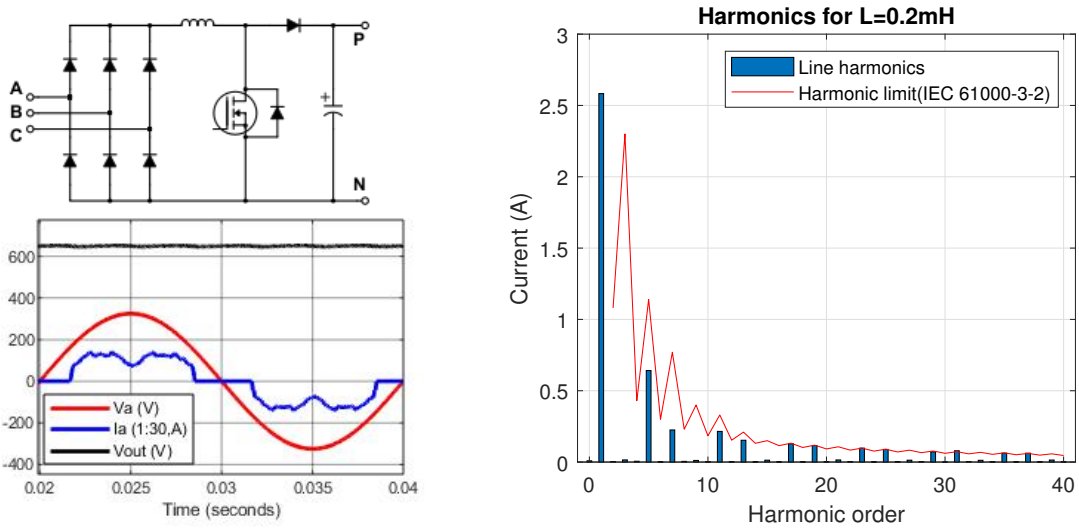
(a) (b)

Figure 1.5: Three phase rectifier slim DC link: (a) Circuit and waveform; (b) THD spectrum

1.4.4. Single switch single inductor PFC

This topology is an extension of a single phase boost converter to a three-phase version, see figure 1.6(a).

Since the inductor is present after the three-phase rectifier, it cannot enforce current through all the three phases. As discussed in the previous topologies, each phase conducts only for 120° and thus, at any particular instant, even though switching is done, one phase does not conduct any current as seen in figure 1.7. Thus a unity power factor is not possible with this topology as well. The THD spectrum with limits, for a single



(a) (b)

Figure 1.6: Single switch single inductor PFC: (a) Circuit and waveform; (b) THD spectrum for L=0.2mH

switch single inductor, is as shown in figure 1.6(b). A filter has been used to remove the switching frequency components in the current waveform.

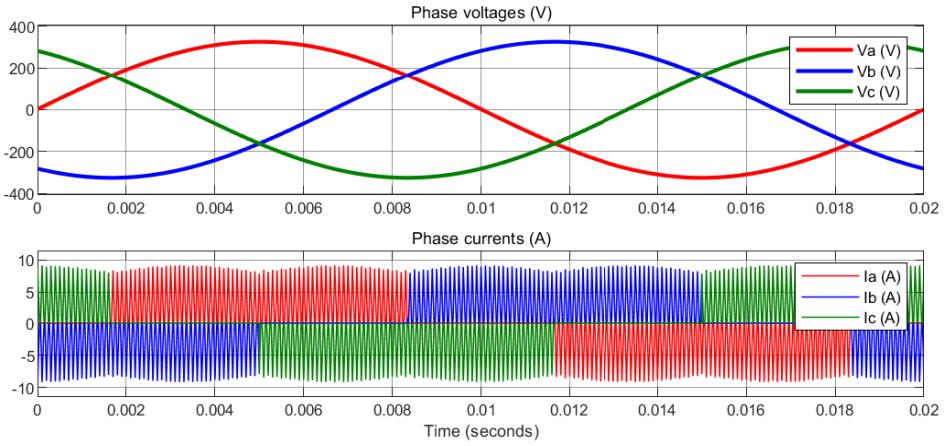


Figure 1.7: Three phase input waveform of a Single switch single inductor PFC circuit

According to simulations, while satisfying harmonic standards, it can carry a power of 2 kW while using 2 mH inductor and also with 0.2 mH inductor. It can be inferred that, whenever a switching device is used, the inductance value is inversely proportional to the switching frequency. Thus, the inductor size can be varied by changing the switching frequency accordingly.

1.4.5. Single switch traditional PFC

Single switch traditional PFC circuit is the most widely used single switch PFC topology came into light around 1989[10]. It is a simple topology (see figure 1.8) which can achieve power factor correction for low powers without using bulky inductors as required in the previously discussed topologies. But the only drawback is that the output voltage needs to be increased as the output power increases to make sure that the converter satisfies the harmonic standards. When a Fourier analysis is done on the input current the equations for the average input current in phase-a is obtained as shown in (1.1)[11].

- For $0° \leq \omega t \leq 30°$,

$$i_a = \frac{V_m t_{on}}{2L} \frac{\sin(\omega t) - \frac{\sqrt{3}}{2M} \sin(2\omega t)}{1 - \frac{3}{M} \sin(\omega t)} \tag{1.1a}$$

- For $30° \leq \omega t \leq 60°$,

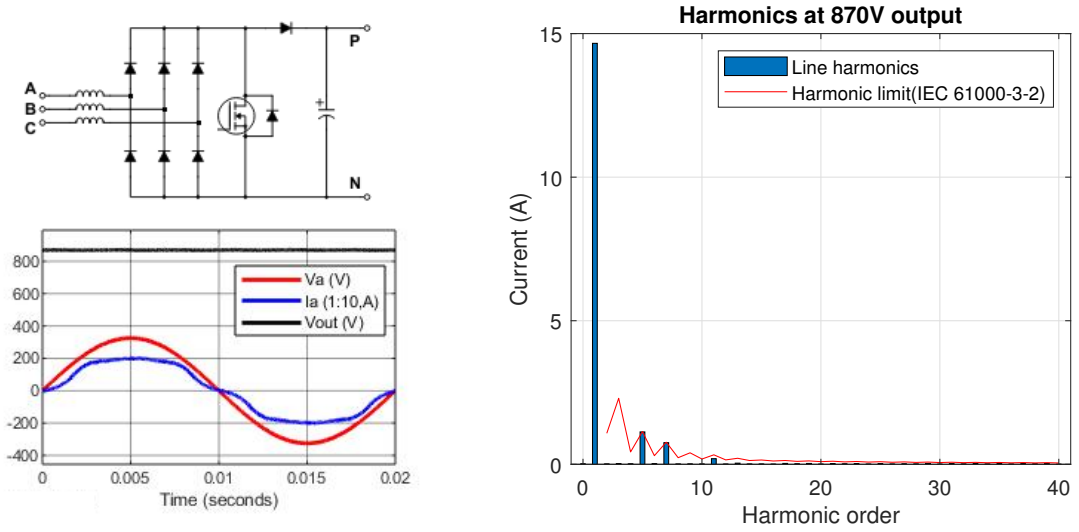
$$i_a = \frac{V_m t_{on}}{2L} \frac{\sin(\omega t) + \frac{\sqrt{3}}{2M} \sin(2\omega t - 120°)}{1 - \frac{3}{M} \sin(\omega t - 240°)} \tag{1.1b}$$

- For $60° \leq \omega t \leq 90°$,

$$i_a = \frac{V_m t_{on}}{2L} \frac{\sin(\omega t) + \frac{\sqrt{3}}{2M} \sin(2\omega t + 60°)}{1 + \frac{3}{M} \sin(\omega t - 240°)} \tag{1.1c}$$

Where V_m is the peak input phase voltage, t_{on} is the time for which the switch is in the ON state and M is the boost ratio which is the ratio of DC output voltage to peak input phase voltage.

From the Fourier analysis, it can be deduced that the lower order harmonics of the phase currents decreases as the boost ratio increases. And thus, it can be concluded that as the power output is increased, the output voltage needs to be increased to make the converter comply with the harmonic standards. The simulations were carried out by using 6^{th} harmonic injection technique [2] and a filter has been used to remove the switching frequency components in the current waveform.



(a) (b)

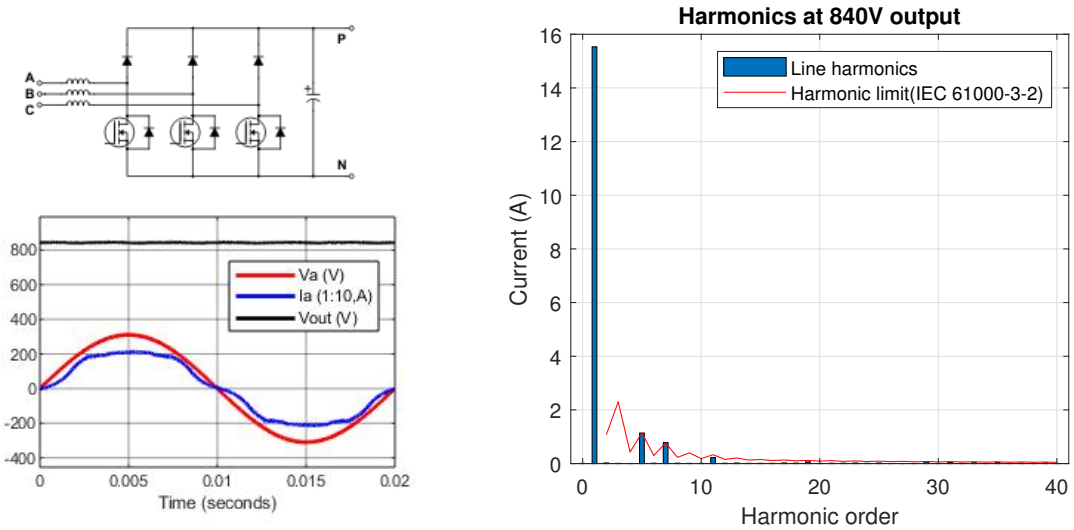
Figure 1.8: Single switch traditional PFC: (a) Circuit and waveform; (b) THD spectrum for 10 kW at 870V output

1.4.6. Three switch bridgeless PFC

A three switch bridgeless PFC can be obtained by replacing the bottom side diodes of the bridge with the semiconductor switches as can be seen in figure 1.9(a). The three switch bridgeless PFC can operate in a way similar to that of a single switch traditional PFC which can be realized when all the switches are closed at the same time. The results are also similar except that the output voltage can be lowered for given power output.

For a PFC to control all the three phases, the converter must be capable of controlling at least two of the three-phase currents at all the instants. Since the third phase current is just the negative sum of the other two phase currents, it will be automatically controlled.

In the bridgeless converter, when two of the currents are negative, the converter can't control the currents, since the switches can conduct the negative currents but can't control them. Thus a three switch PFC still cannot fully achieve the unity power factor at a given output voltage and behaves in a similar way as the single switch traditional PFC as depicted in figure 1.9(b). The simulations were carried out by using 6^{th} Harmonic injection technique to have a fair comparison with respect to single switch traditional topology and a filter has been used to remove the switching frequency components in the current waveform.

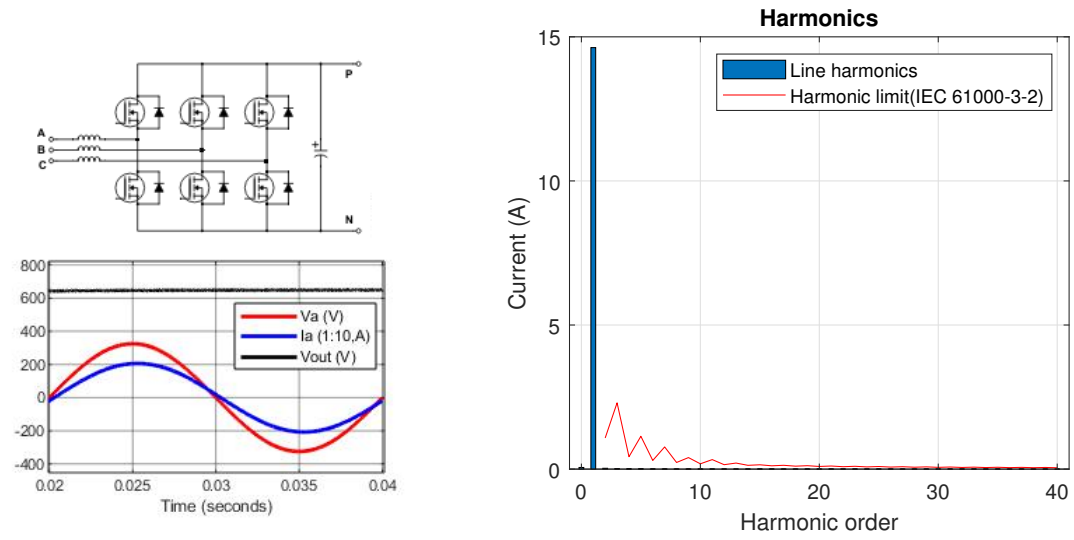


(a) (b)

Figure 1.9: Three switch bridgeless PFC: (a) Circuit and waveform; (b) THD spectrum for 10 kW at 840V output

1.4.7. Six switch bidirectional PFC

A six switch boost converter is the same as the three-phase rectifier with all the diodes being replaced by the semiconductor switches and three inductors in the input of each phase as seen in figure 1.10(a). Since there are six switches, the circuit can control the currents even when two currents are negative, unlike the previous topology. Thus the circuit is capable of having a perfectly sinusoidal input current waveform under all load conditions as seen in figure 1.10(a). Since the current waveform are perfectly sinusoidal, the PF for this topology is greater than 0.99 with a THD less than 5 %. The harmonic distribution of this topology can be seen from figure 1.10(b). The only disadvantage of using this topology when compared to previous topologies is the control of high side switches of the bridge. But, since the circuit contains switches in place of all the diodes, it has a capability to transfer the power from output to input and act as an inverter. Thus, being bidirectional is the biggest advantage when compared to the previous topologies.



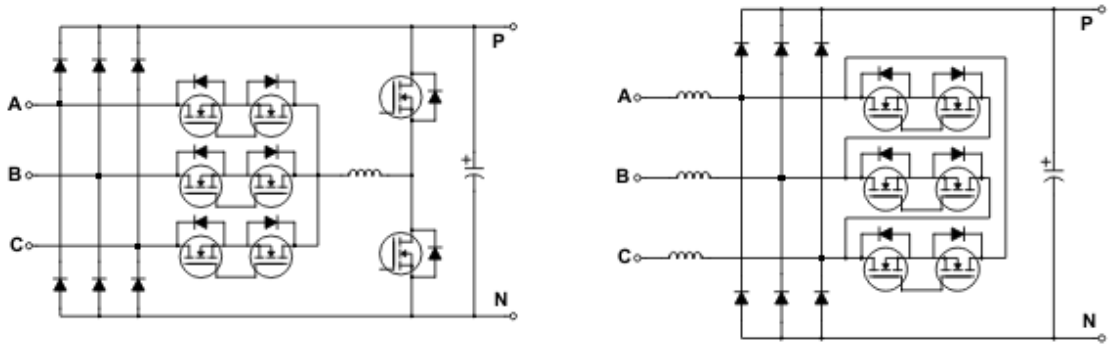
(a) (b)

Figure 1.10: Six switch bidirectional PFC: (a) Circuit and waveform; (b) THD spectrum for 10 kW at 650 V output

1.4.8. Hybrid 3rd harmonic current injector PFC

In a three-phase rectifier, as discussed in previous topologies, it is known that the phase current will be zero for first 30° and last 30° of a half cycle, which is similar to that when a third harmonic component is subtracted from the actual sine wave. Thus the addition of a third harmonic component to the rectifier phase currents could result in sinusoidal phase currents. Thus the hybrid 3rd harmonic injection circuit can be obtained by just adding a third harmonic injector circuit to the three-phase rectifier as seen in figure 1.11(a).

Since the main power only flows through the diodes, and the switches are used only for harmonic injection, the efficiency of this topology is quite high. While the efficiency is increased with respect to the six switch bidirectional PFC, the number of switches is also increased, leading to the more complex control circuitry. Also, the circuit will no longer be bidirectional capable when compared to the six switch PFC.



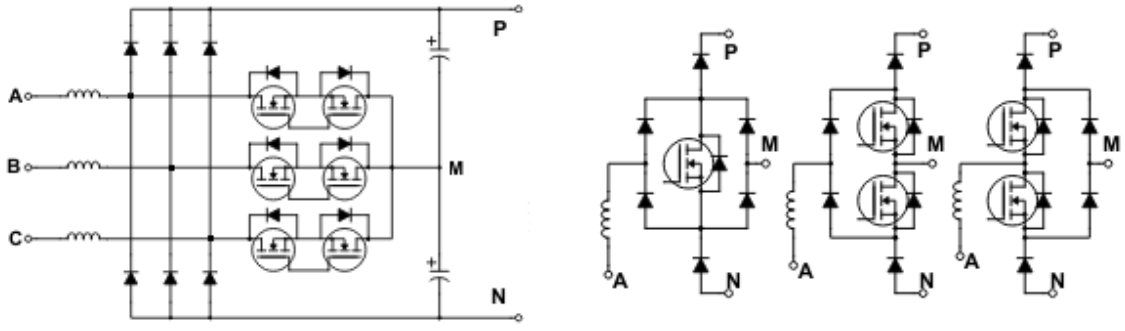
(a) (b)

Figure 1.11: Circuit diagram: (a) Hybrid third harmonic current injector PFC; (b) Delta-switch boost converter

1.4.9. Delta-switch boost converter

Delta switch converter works in similar principles to the hybrid third harmonic injector PFC, but the method of third harmonic generation is different. In delta switch configuration, the delta switches are used to generate the third harmonic content and are fed to the phase currents. The main advantage of this topology is the reduced number of switches when compared to the previous topology.

1.4.10. Vienna rectifier



(a) (b)

Figure 1.12: Vienna rectifier: (a) Circuit diagram; and (b) its other leg configurations

Vienna rectifier is one of the most commonly used three-phase boost PFC for high power applications. The converter circuit is almost similar to the delta switch rectifier, but the delta has been transformed to star and the midpoint is connected to the DC midpoint, thus reducing the stress among the switches when compared to the delta switch configuration. The circuit is as shown in figure 1.12(a). Vienna rectifiers are also available in other configurations by modifying the phase legs as shown in the figure 1.12(b). Each has its own advantages and disadvantages. Considering the cost, if a leg with a single switch is chosen then the cost of the

power and control circuit will reduce, but the current needs to pass through multiple semiconductor devices which decreases the efficiency to a large extent. Thus the three switch version of Vienna rectifier will not be of much interest in most of the applications.

1.5. Topology and control method selection

1.5.1. Comparison of the topologies

Among the topologies discussed under section 1.4, it is obvious that it is possible to use the passive PFC topologies only for power ranges up to 1 kW. Even though they are simple, their volume increases as the power increases due to the increase in inductor size. However, for three-phase applications, power range will be usually much higher than 1 kW. Hence, three-phase passive PFCs are generally not seen in many applications.

While considering the active PFCs with fewer switches, it is known that the single inductor version of PFC works only for powers below 2 kW. For the single switch traditional and three switch bridgeless PFCs, the output voltage needs to be increased as the output power increases as seen in figure 1.13. Which is undesirable, since the high voltage devices become costly. The three switch bridgeless converter can achieve a power of 10 kW for an output voltage of 840 V, when compared to the single switch traditional PFC, which achieves that at an output voltage of 870 V. Both the topologies have similar output voltage range and hence a detailed comparison is required among the two for choosing the cost-effective solution.

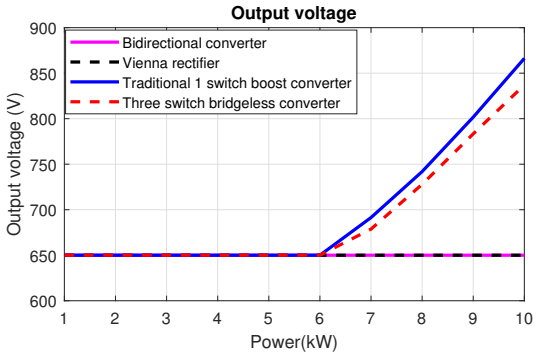


Figure 1.13: Comparison of the output voltage

While considering the active PFCs with many switches, all the third harmonic injection topologies are having many components and their performance is almost same with almost negligible THD. The hybrid third harmonic injector circuit has many components and is thus costlier than delta and Vienna rectifiers, hence not considered for further comparison. Delta and Vienna rectifiers are having the same number of components, but in Vienna rectifier, the DC midpoint reduces the stress and thus the cost of the switches of Vienna rectifier, hence delta switch rectifier is not considered for the further comparison. Thus, a detailed comparison is done for the Vienna rectifier, six switch bidirectional rectifier and, single and three switch PFCs.

Parameters for the comparison

For a given input peak phase voltage of $\hat{V}_{ph}$, the minimum output voltage of any boost converter will be $\sqrt{3}\hat{V}_{ph}$. Thus for a three-phase input RMS phase voltage of 230 V, considering around 10 % over rating, the output voltage will nearly be 650 VDC. Hence, 650 VDC is considered as the minimum output voltage for any boost converter in the rest of this paper.

Since the operation of three switch and single switch PFCs are almost similar, the inductance values of these PFCs can be approximated by rearranging equation (25) of the reference paper [12]. While the inductor values for bidirectional PFC is obtained by rearranging equation (7) of reference paper [7] and for Vienna rectifier, the inductance is calculated from equation (3.14) of reference paper [8]. The equations are not reproduced here for brevity.

To have the low-cost configurations of bidirectional and Vienna rectifiers, the ripple ratio is considered in such a way that the inductor energy product is minimum. Thus total inductor energy product for different current ripple ratios is obtained as shown in figure 1.14. From this, it can be seen that the topologies have minimum cost at a ripple ratio of 1.2. Also, the ripple ratio of 1.2 gives ripples of similar

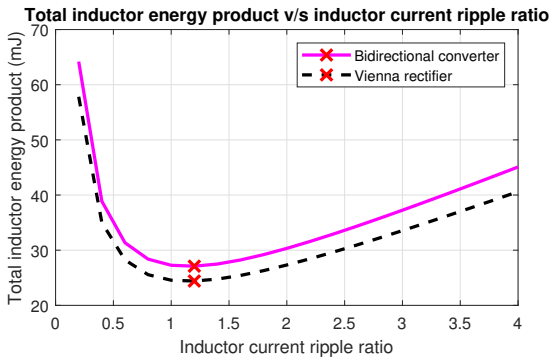


Figure 1.14: Inductor energy v/s ripple ratio

magnitude to that in the single switch and three switch topologies. Thus, all the topologies will be requiring a similar EMI filter, which makes a fair comparison between the topologies.

The voltage and current ratings of all the semiconductor devices are considered as the DC output voltage and peak inductor current respectively for all the topologies, except for Vienna rectifier. The DC midpoint in the Vienna rectifier reduces the voltages stress across the switches to half the DC output voltage. Hence the switches of the Vienna rectifier are rated to half the DC voltage.

Factors affecting the cost of the converter

Semiconductor kVA rating: Cost of a semiconductor device depends on the peak voltage and current rating of the device. Thus, the product (kVA rating) of voltage and current ratings is considered as a factor of comparison of cost for the topologies. But, it is known that the cost of a MOSFET for a given kVA is more than the cost of a switching diode of the same kVA rating, and it will be unfair to just add both the ratings in the same ratio. Thus a sample of MOSFETs and switching diodes are considered with their kVA ratings and costs, and then the ratio “cost/kVA" is calculated for both MOSFETs and switching diodes. It was found that the cost/kVA for a MOSFET is around 1.15 times larger than cost/kVA for a switching diode. Thus, the kVA rating for a converter is calculated using (1.2).

$$\sum \text{kVA} = \sum_{\forall \text{Switches}} \text{kVA} + \frac{1}{1.15} \sum_{\forall \text{Diodes}} \text{kVA} \tag{1.2}$$

Switch utilization factor: Switch utilization factor (SUF) is defined as the ratio of the output power to the sum of the product of peak voltage and peak current ratings of all the switches used in the circuit[13]. SUF generally determines how effectively the switches are used in the circuit. But, in a PFC circuit, even the diodes will be switching, when the switches are switching. Hence, it will be unfair if the diodes are not considered for comparison. Hence SUF is calculated as the ratio of the output power to the semiconductor kVA rating of the circuit and given by (1.3). Higher the SUF value, the utilization of the semiconductor devices in the circuit is more (cost-) effective.

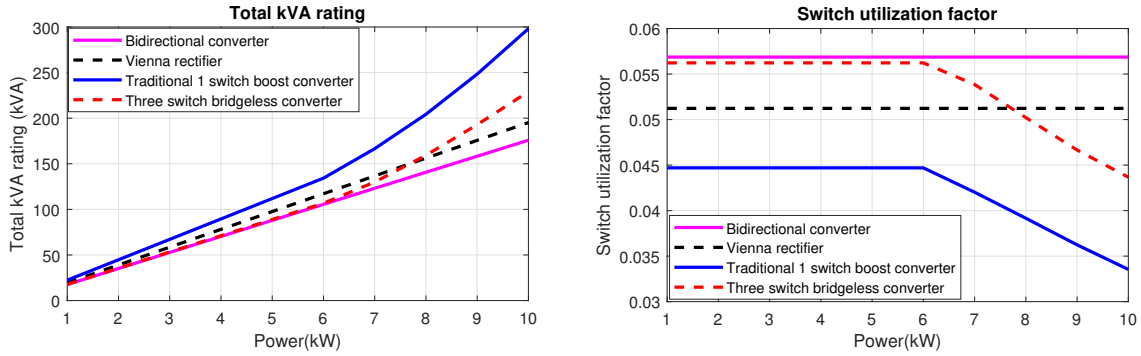
$$\text{SUF} = \frac{\text{Output power}}{\sum \text{kVA}} \tag{1.3}$$

Inductor energy product: Cost of the inductor depends on the size of the inductor which depends on the peak stored energy i.e, peak current ($\hat{I}$), RMS current (I_{RMS}) and the inductance (L) values as seen in the equation (1.4)[9]. Thus, calculating the total peak energy stored in all the inductors of a converter will be a good factor for a cost comparison.

$$\sum_{\forall \text{Inductors}} (L\hat{I}I_{\text{RMS}}) = \sum_{\forall \text{Inductors}} (k_{\text{Cu}} J_{\text{RMS}} \hat{B} A_{\text{w}} A_{\text{core}}) \tag{1.4}$$

Where k_{Cu} is the copper fill factor for a wire, J_{RMS} is the current density of the wire, $\hat{B}$ is the peak magnetic flux density in the core, A_{w} is the total winding area and A_{core} is the core area of the inductor.

Analysis of the proposed topology



(a) (b)

Figure 1.15: Comparison of: (a) Total kVA rating; (b) Switch utilization factor

Using the equations, (1.2), (1.3) and (1.4) a comparison has been done between the PFC converters for a power range between 1-10 kW. The plots of the comparison are as seen in the figures 1.15(a), 1.15(b) and 1.16. From the figure 1.15(b), it is definite that the SUF rating for the bidirectional converter is the best for the complete power range. Figure 1.15(a) also reveals that the cost of the semiconductor devices in the bidirectional converter is more cost-effective when compared with the other converters. But the figure 1.16 suggests that the cost of the inductors in the bidirectional converter is the highest up to power range of 7.5 kW. Thus, the bidirectional converter is not efficient for power ranges below 7.5 kW. But above 7.5 kW, Vienna rectifier requires the least inductor energy and its kVA rating is just above that of the bidirectional converter. Thus, above 7.5 kW Vienna and bidirectional rectifier are most suitable. But, it is difficult to further compare which among them is better, since it depends on the comparison of different factors. However, the comparison in [5], suggests that Vienna rectifier is cost-effective than the bidirectional converter.

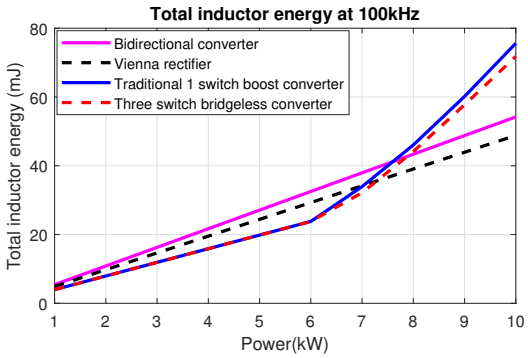


Figure 1.16: Comparison of total inductor energy

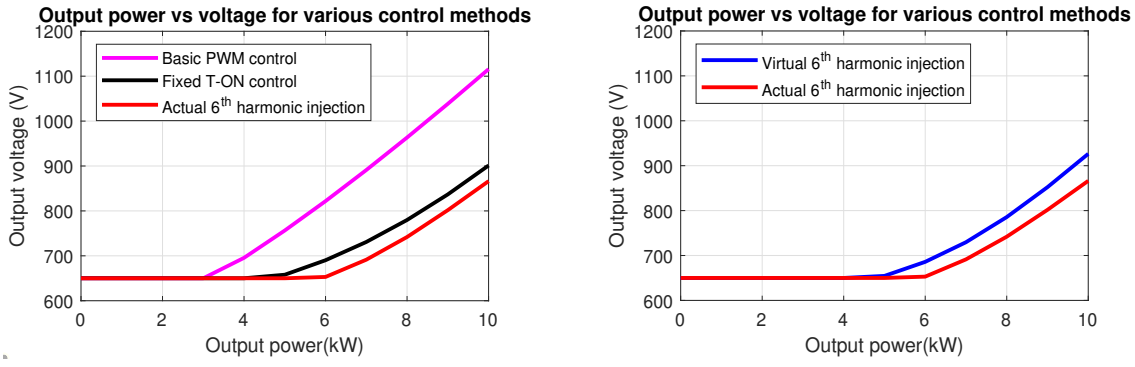
For power ranges below 7.5 kW, the single switch and the three switch PFCs have the lowest inductor energy. And, the three switch PFC has the kVA ratings almost the same as the bidirectional converter. Thus, for power ranges below 7.5 kW, three switch PFC is the cost-effective solution. **Hence, three switch bridgeless PFC is the topology under consideration.**

1.5.2. Comparison of the control methods

Comparing the major control methods of single switch traditional PFC

Single switch traditional converters can be operated using three major control strategies, namely, basic PWM control, fixed T-ON control and 6th harmonic injection control. Detail analysis regarding these controls can be found in the article [6].

Basic PWM control is the simplest of all the controls. The control involves just the duty cycle control of the PWM depending on the voltage or load changes. But the output voltage for a given power is very high, as can be observed in figure 1.17(a). Thus the technique is not a feasible solution since the higher output voltages require high voltage rated components for the circuit and will be costly.



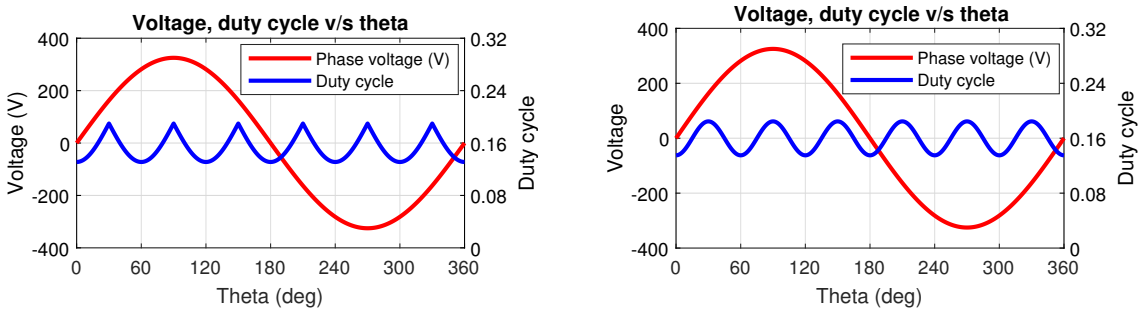
(a) (b)

Figure 1.17: Output power v/s voltage graphs for various: (a) Control methods; (b) 6th harmonic injection methods

In fixed T-ON control method, the switch is switched ON for a constant time and will be switched OFF till the current at the rectifier output reaches zero and then the next cycle begins. The output voltage required for a given power is much lower compared to the basic PWM control[11], but since the switching happens depending on the load, the switching frequency varies for a large range of values and will make it difficult for the design of EMI filters. Hence, might lead to bigger EMI filters than the expected and will result in higher cost and volume.

6^{th} harmonic injection control is a bit complex control, it involves the injection of 6^{th} harmonic into the duty cycle of the basic PWM modulation. The addition of 6^{th} harmonic component will reduce the 5^{th} harmonic content in the phase currents, which is the major harmonic content in a basic PWM control[2]. But, the 6^{th} harmonic injection control increases 7^{th} harmonic content in the current making the THD almost same, but still complying the harmonic limits for a lower output voltage. However, the 6^{th} harmonic injection technique seems more economical when compared to the other techniques and thus, **6^{th} harmonic injection technique is used as the control method.**

Comparing the virtual and actual 6^{th} harmonic injection techniques



(a) (b)

Figure 1.18: 6^{th} harmonic waveform injection: (a) Virtual; (b) Actual

Virtual 6^{th} harmonic injection was introduced as a simpler way of 6^{th} harmonic injection technique when the controller is implemented in an analogue way[4]. The output voltage required for a given power is comparatively higher when used virtual instead of the actual 6^{th} harmonic injection technique. But, the technique could be easily implemented using an additional low power rectifier or a low pass filter whereas the actual 6^{th} harmonic injection technique would have required a PLL and a 6^{th} harmonic generator circuit, which were costly for implementation in the earlier days. However, these days, almost all the control circuits are done digitally and are cheaper to implement the controls in a digital way rather than analogue way and thus, **actual 6^{th} harmonic injection method is the preferred control method for the chosen topology.**

1.6. Research question and methodology

1.6.1. PFC under consideration

As per the comparisons done under the sections 1.5.1 and 1.5.2, the cost effective PFC considered for this project is **three switch bridgeless PFC controlled by actual 6^{th} harmonic injection control.** As per the analysis done in the previous section, the converter is cost effective up to 7.5 kW with an output of 700 V. However, for the thesis purpose, **a 5 kW converter is considered at 650 V** to have a safe margin.

1.6.2. Problems in the topology under consideration

A 6^{th} harmonic component is present in the DC output of the three switch bridgeless PFC when a 6^{th} harmonic injection controller is implemented.

If the controller is designed to be stiff, it tries to maintain a constant output voltage by eliminating the harmonic component in the DC side, which would increase the AC side harmonics in the circuit, leading to failing the power factor correction action. Thus the controller should not be so rigid, to allow the 6^{th} harmonic content in the DC output of the converter.

If the controller is not so stiff, it is vulnerable to the output voltage fluctuations during load transients and input voltage variations. Hence the controller must be stiff enough to control the PFC circuit during these variations.

1.6.3. Research question

Design of an improved dynamic control/modulation of a three switch bridgeless PFC.

- A controller needs to be designed which can ignore the low-frequency harmonics at the output, yet capable of regulating the output voltage during load transients and input voltage fluctuations.
- The aim is also to have a cost-effective implementation of the hardware with reduced volume.

1.6.4. Methodology

- Simulate the proposed PFC circuit to analyze the control required during different load transients and input voltage variations.
- Design a control strategy to ignore low-frequency harmonics at the output and yet be robust towards load transients and input voltage fluctuations.
- Simulate the control strategy and analyze the results for the load and voltage fluctuations.
- Determine the frequency of operation such that converter volume and cost are minimum with acceptable efficiency.
- Hardware implementation of the proposed circuit with the control strategy.
- Testing and evaluation of the developed hardware.

2

Control System Design

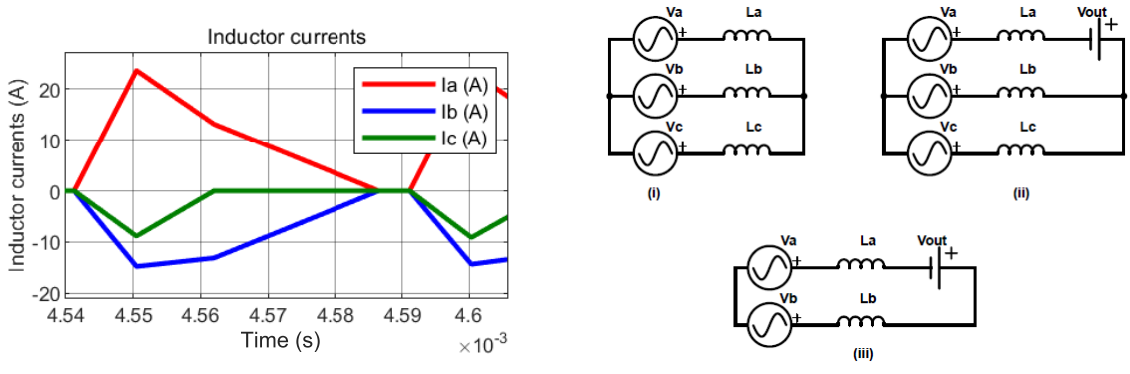
As discussed in the previous chapter, the selected topology is the cost-effective topology among all the other active power factor correction topologies. But due to the discontinuous mode of operation, the design of the hardware is comparatively more complex than it seems. The detailed working of the converter and its control design are discussed in the further sections of this chapter.

2.1. Working of three switch bridgeless PFC

In simpler terms, the aim of the converter is to generate a sinusoidal current. This can be achieved by switching continuously such that the average of the switched currents is sinusoidal.

Disregarding the various switching control strategies, every time whenever the switches are ON, the complete input voltage appears across the inductors since the closed switches act as the star point of the three-phase short. Since the current rise in the inductor of each phase is proportional to the applied voltage, the current peak during each switching will be proportional to its instantaneous phase voltage. Thus for an overall period, the peak currents are sinusoidal and follow the same phase of the phase voltage.

Even though the peak currents are sinusoidal, the average current is not necessary to be sinusoidal. Because for the average current to follow the shape of the peak current, the current in the inductor should be either raising or falling without having a period of zero current state (or even if there is a zero current period, this period must be same for all the switching periods for all the phases). Since there will be periods of zero current in the inductors which vary in each switching period disregarding the type of switching control used, it is not possible to obtain an average current which is completely sinusoidal. In this topology, the switching of all the switches occurs simultaneously. This makes its operation similar to that of a single switched traditional PFC. The reduction in boost diode increases the efficiency comparatively.



(a) (b)

Figure 2.1: (a) Current waveform during switching; (b) Equivalent circuit during (i)Switch ON (ii)Switch OFF (iii)Zero current in Lc

It can be seen in figure 2.1(a), whenever the switches are ON (as shown in figure (i) of 2.1(b)), the instantaneous input voltages are applied on the inductors, depending on the phase voltages, one or two inductors

have positive voltage across them leading them to increase their currents from zero to a peak value and the rest of the inductor/s have a negative voltage across them making them have their currents increase negatively from zero to a negative peak value. The currents are in such a way that the sum of all the three current will be always zero since it is a balanced system. When the switches are OFF, the equivalent circuit will be as shown in figure (ii) of 2.1(b) (the picture is considered, when phase-a has a positive voltage and remaining are having negative voltages). The inductor having the shortest peak current at that switching cycle will reach zero faster than the currents in the remaining inductors, since the voltages across the inductors during OFF state are not same as the voltages across them during ON state. Thus it can be observed that the zero periods are varying in each inductor for each switching cycle. Thus resulting in a non-sinusoidal average current.

When observed carefully, once when one of the phases reaches zero current period, the slopes of the currents of other two inductors change due to the change in the effective equivalent circuit (see figure (iii) of 2.1(b)). The detailed analysis of the average currents during different control strategies can be found in the article [6].

Since the operation of the converter is in discontinuous mode with the zero current period changing every switching cycle and having a change in slope during decreasing currents, it has been difficult to completely analyze and derive equations which exactly dictates the voltages and currents at each and every component. However few of the references have tried to derive approximate equations for few of the parameters of a single switch traditional converter, but not for three switch bridgeless converter.

2.2. Review of control system strategies

Control system plays an important role in the proper functioning of a converter circuit. As discussed in the previous section, it is difficult to determine the converter parameters and also the transfer function of the converter, due to the discontinuous operation of the three-phase converter. The unavailability of the state space model of the converter makes it difficult to design a simple proportional integral differential (PID) Controller for the converter. Moreover, even though if an approximate state space model is developed, implementing a simple PID controller wouldn't have helped in achieving a controller capable of having a good transient stability and yet capable of being flexible to allow 6^{th} harmonic variations in the converter output, as discussed in the section 1.6.2. Hence various available control strategies have been evaluated and then a control strategy suitable for the application is designed.

2.2.1. Non linear control strategies

The approximate formula for the average output current, I of a single switch traditional converter[12] is as given in the equation (2.1). Since the operation of three switch bridgeless converter is similar, the same equation is considered for the considered topology as well.

$$I = \frac{\hat{V}_{\text{ph}}^2 d^2 T_{\text{sw}}}{2L} \frac{1.46}{V_{\text{out}} - 1.67\hat{V}_{\text{ph}}} \tag{2.1}$$

Where $\hat{V}_{\text{ph}}$ is the peak voltage value of RMS phase input voltage V_{ph}, d is the duty cycle of the converter, T_{sw} is the switching period of the converter, L is the inductance of each phase of the converter and V_{out} is the output voltage of the converter.

The duty cycle can be calculated by rearranging the equation (2.1) as shown in the equation (2.2).

$$d = \sqrt{\frac{2LI}{\hat{V}_{\text{ph}}^2 T_{\text{sw}}} \frac{V_{\text{out}} - 1.67\hat{V}_{\text{ph}}}{1.46}} \tag{2.2}$$

It can be seen that the output voltage does not have a linear relation with the duty cycle of the converter. Hence the converter operation is non-linear. The time required for current in the inductor to reach zero from maximum value changes continuously as discussed previously, hence it is difficult to determine the state space model for the considered converter. In [12], a set of approximate equations have been developed to analyze the output voltage variations with respect to the variations in the duty cycle and the input voltage. But a complete system transfer function/state space model has not been developed in any of the available literature.

One way of designing a controller for the non linear system will be to create a state space model and then linearize the model at the operating point. But since there is no exact state space model, the control

techniques based on linearization can't be used. Other control techniques are based on Lyapunov based methods, which as well require state space models for designing the controller.

Thus, it is difficult to design a conventional controller for a system without a state space model for the converter. A novel control strategy has to be developed to design the control system for the converter under consideration.

2.3. Controller design

The unavailability of the state space model for the converter urges for an unconventional controller, which is based on the approximate formula for the duty cycle under various converter parameters and voltage and current conditions. From the equation, (2.2), the average duty cycle value for the given load current and input/output voltages can be obtained. The advantages of using this formula based controller are, the reference duty cycle value will be instantaneously changed and fed to the converter, as soon as the line/load transients are detected. Whereas the disadvantage is that, the formula depends on the converter parameters which might vary in real time, hence there is a constant error in the duty cycle value and thus the output voltage. Thus, the developed formula based controller will be fast with a constant steady state error.

In order to remove the steady-state error, a controller based on output error needs to be created such that, it will continuously adjust the duty cycle generated by the formula based controller until the steady state error has become zero or acceptable value.

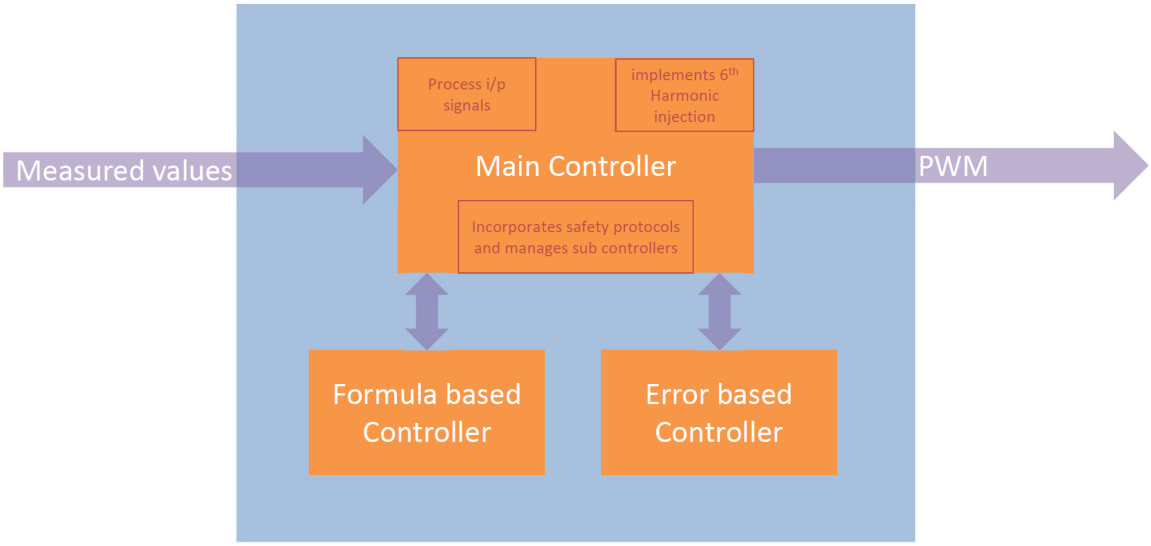


Figure 2.2: Control System Overview

Apart from the formula based controller and error based controller, there is a necessity of the main controller which coordinates the overall activities of the controllers and also to implement some safety limits.

2.3.1. Formula based controller design

The formula (2.2) requires the load current value and the RMS of the input phase voltage, along with the converter parameters such as frequency of operation and the inductance value, to calculate the duty cycle at any particular instant.

By measuring the instantaneous output voltage, V_{out} and the current, I the controller measures the power requirement of the motor drive and thus calculates the load current, I_{ref} requirement at the reference output voltage according to the equation (2.3), V_{ref} and then calculates the duty cycle according to the equation (2.4).

$$I_{\text{ref}} = \frac{V_{\text{out}} I}{V_{\text{ref}}} \tag{2.3}$$

$$d = \sqrt{\frac{2LI_{\text{ref}}}{\hat{V}_{\text{ph}}^2 T_{\text{sw}}} \frac{V_{\text{ref}} - 1.67\hat{V}_{\text{ph}}}{1.46}} \tag{2.4}$$

2.3.2. Error based controller design

The change in output voltage, ∂V_{out} with respect to the change in the duty cycle, ∂d can be found using the transfer function (2.5)[12]. As in the previous case, the equation (2.5) is also defined for a single switch converter, but considering the same since the operation of three switch version is similar.

$$\frac{\partial V_{\text{out}}}{\partial d} = \frac{j_2 r_{\text{eq}}}{(r_{\text{eq}} C_o)s + 1} \tag{2.5}$$

Where j_2 and r_{eq} are defined as equations (2.6) and (2.7).

$$j_2 = \frac{1.46 d \hat{V}_{\text{ph}}^2 T_{\text{sw}}}{L(V_{\text{ref}} - 1.67\hat{V}_{\text{ph}})} \tag{2.6}$$

$$r_{\text{eq}} = \frac{r_2 R_l}{r_2 + R_l} \tag{2.7}$$

Where, the converter resistance, r_2 is given by the equation (2.8). The load resistance R_l of a motor load can be approximated as the ratio between the output voltage and the load current. The equivalent resistance r_{eq} will be maximum when there is no load and is minimum under full load. For the considered converter, j_2 is calculated to be 46 (The parameter values are considered from the chapter 3.)

$$r_2 = \frac{V_{\text{ref}} - 1.67\hat{V}_{\text{ph}}}{I_{\text{ref}}} \tag{2.8}$$

From the equation (2.8), it can be concluded that the converter resistance r_2 is also inversely proportional to load current. Considering a minimum load of 500 W, the maximum equivalent resistance for the considered converter can be calculated as 120 Ω.

From the Laplace equation, (2.5), it can be said that a unit change in duty cycle, ∂d will lead to a voltage change, ∂V_{out} of value equal to $j_2 r_{\text{eq}}$ with a time constant of $r_{\text{eq}} C_o$. The maximum voltage change, ∂V_{out} per unit change in duty cycle for the considered converter is calculated to be 5500 V. Thus, for an output voltage error of $V_{\text{out}} - V_{\text{ref}}$, the error based controller subtracts a duty cycle error of $\Delta d_{\text{error}} = (V_{\text{out}} - V_{\text{ref}})/5500$ from the duty cycle, d calculated by the formula based controller. For larger error values, it takes more than one iteration for the output voltage to reach the reference value, since the system is non-linear, while the formulae derived are for a linearized system which are valid for small operating range.

Time constant is maximum when the load is minimum since the equivalent resistance is inversely proportional to the load current. Considering a minimum load of 500 W and settling time as thrice the time constant, the maximum time, T_{settle} required for a voltage to settle for a change in the duty cycle can be calculated. For the chosen converter application, the settling time is calculated to be 0.1 s.

When, the error based controller iterates very fast, even before the voltage output of the converter settles, it considers that the error is still present and it adds the same error again, which would eventually cause overshoot and might lead to instability of the controller if the iteration is too fast. Thus to obtain a stable operation, each iteration of the error based controller is carried only after a time period equal to the settling time, T_{settle}, so that the output voltage is a stable value for next iteration.

2.3.3. Main controller design

The main controller has many important functions. They are as follows:

- To measure the required real time parameters, such as output current, input and output voltages.
- To co-ordinate the formula based and the error based controllers.
- To generate a 6^{th} harmonic injected pulse width modulation signal, using the average duty cycle information from the other controllers.
- To turn off the duty cycle, in case output voltage is 130 % higher than the rated value.
- To turn off the duty cycle, in case of no load condition.
- To limit the range of duty cycle between 0 to 0.17, as a factor of safety. Since the maximum duty cycle calculated at the maximum load is around 0.16 only.

2.4. Stability analysis

The derived controller is not a conventional controller therefore stability analysis with frequency domain analysis is not possible. Instead, the worst possible scenarios are checked to determine whether the controller is stable under that scenario.

The formula based controller is an open loop controller, hence it will be stable always, but there might be an error in its output due to the inaccuracies in either measurements or input parameters.

In the error based controller, the settling time is high enough to allow the output voltage to settle down before the next iteration of the error controller begins. The large settling time period in the operation of error based controller makes it as a virtually open loop controller. Hence, it can be said that it will be always stable even though it is actually a closed loop controller.

The added duty error is directly proportional to the output voltage error and will proportionally reduce the output voltage error. Thus, the error in the duty cycle will finally become zero when the output voltage error is zero. Hence, it can be said that the error based controller will converge the output voltage to the reference value and will be stable in its operation.

Scenario-1: Formula based controller is providing lower duty cycle due to changes in parameter values/faulty sensors

Considering the maximum error in the formula based controller, i.e, when it wrongly gives the duty cycle as zero. In such a case, the output voltage falls down. The output voltage can fall down to a minimum voltage of average three-phase rectified voltage, 540 V and not less than that. This voltage fall would be detected by the error based controller and will add the duty cycle accordingly to restore most of the voltage within one settling time, i.e., at a maximum of 0.1 s.

Scenario-2: Formula based controller is providing higher duty cycle due to changes in parameter values/faulty sensors

Since the maximum duty cycle is limited to 0.17, the maximum error in the duty cycle will be around 0.01, which can still increase the output voltage to a value of $5500 \cdot 0.01 = 55$ V (which is still not more than the 130 % rating of the output voltage). But the error based controller will detect this voltage rise and will reduce the voltage to almost nominal level in one settling time, i,e, at a maximum of 0.1 s. If by any chance, the error based controller is yet to detect the error(since it has a large time period for each iteration) then, the main controller has an additional safety, where it shuts the PWM when the voltage is higher than 130 % rated voltage.

2.5. Simulation results

The controller has been simulated to drastic changes in the line voltage from 220 V to 240 V with step increases in the load. The output voltage of the converter seems to reach a stable value as shown in the figure 2.3.

From figure 2.3, it can be observed that during low load transient conditions, the converter output voltage takes a bit more time to settle down than the transients during high load conditions. The duty cycle from the formula based controller can be observed to change instantaneously during transients and thus will reduce the magnitude of voltage fluctuations to a lower level, but still results in a bit of offset in the output voltage. It can also be observed that the error value to the duty cycle is only added after the settling time, thus making the system stable during transient conditions.

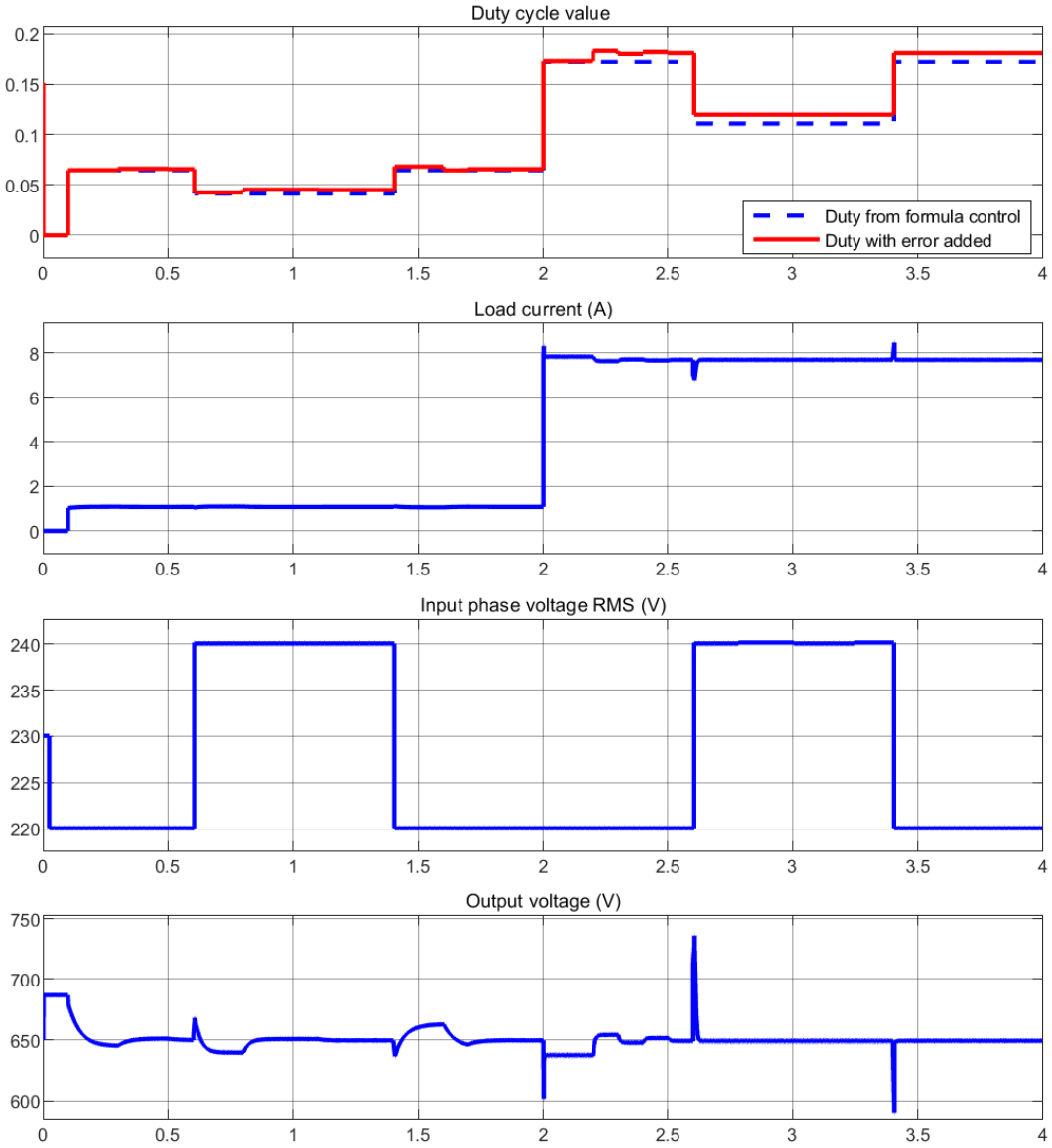


Figure 2.3: Converter output for load and line transients

3

Hardware Design

This chapter aims at complete hardware design of the converter. A detailed loss analysis with respect to different switching frequencies is considered to select the converter operation frequency. To start with the detailed analysis, the next section deals with the estimation of all the parameter values for the converter.

3.1. Parameters calculation/estimation

A 5 kW converter needs to be designed with an output of 650 V and an input phase voltage of 230 V with a deviation of ±10 V. But for the converter to achieve power factor correction, it has to have a certain boost ratio M, as discussed in the section 1.4.5. Hence for input voltages higher than 230 V, even though the output voltage is regulated at 650 V, the power factor correction is not guaranteed up till 5 kW of power.

Since the operation of three switch bridgeless converter is similar to the single switch traditional converter, equations relevant to single switch version will be used to derive few of the parameters. One of the first papers which discussed regarding the traditional single switch PFC[10] also discusses regarding the inductor selection by considering that the peak RMS current is 0.418 times the peak inductor current, I_{Lp} (3.1) in the circuit by doing Fourier analysis of the input current. The paper considers duty cycle, d as 0.5 for calculation of inductor. But, the duty cycle of 0.5 will create a large output voltage. Thus, the equation is generalized by using the duty cycle in the equation as shown in (3.2).

$$I_{Lp} = \frac{\hat{I}_{\text{RMS}}}{0.418} \tag{3.1}$$

$$L = \frac{\hat{V}_{\text{ph}} d\, T_{\text{sw}}}{\hat{I}_{\text{RMS}}} 0.418 \tag{3.2}$$

Where L is the maximum inductance that can be used in the circuit, $\hat{V}_{\text{ph}}$ is the peak voltage value of RMS phase input voltage V_{ph}, $\hat{I}_{\text{RMS}}$ is the peak current of the RMS phase input current, I_{RMS} and T_{sw} is the switching period of the converter.

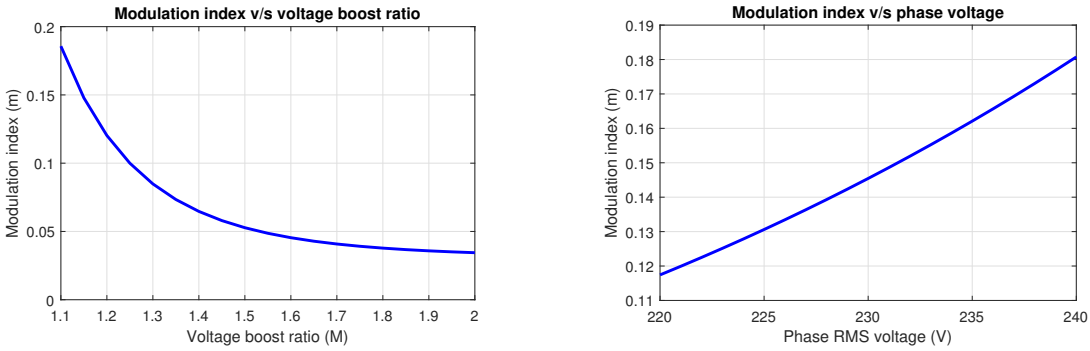
However, the derived equation is applicable for a basic PWM operation with constant duty cycle operation. If the 6^{th} harmonic injection control is used, the duty cycle will change instantaneously and will also depend on the modulation index of the injected harmonics. The minimum instantaneous duty cycle will be much lesser than the average duty cycle and the formula (3.2) can't be directly used to calculate the inductance value.

Instantaneous duty cycle, D of the harmonic injected PWM is defined according to the equation (3.3)[2].

$$D = d\left[1 + m \cdot \sin\left(6\omega t + \frac{3\pi}{2}\right)\right] \tag{3.3}$$

Where d is the average duty cycle, m is the modulation index of the harmonic injection ω is the angular frequency of the input phase voltage. The minimum value of the duty cycle can be calculated when the sine function is negative maximum as shown in the equation (3.4),

$$D_{\text{min}} = d[1 - m] \tag{3.4}$$



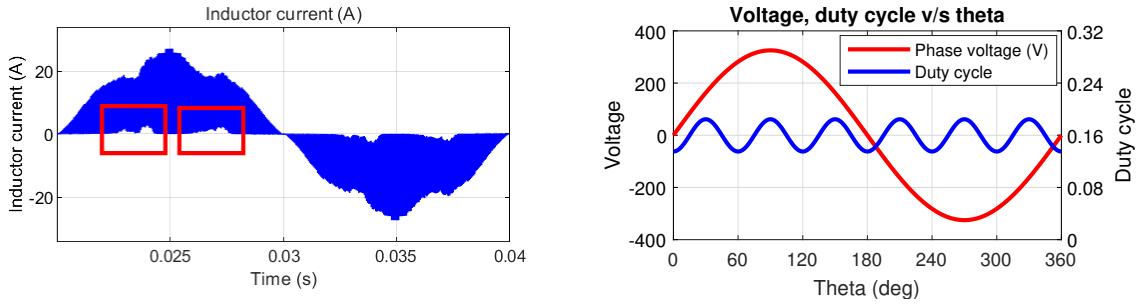
(a) (b)

Figure 3.1: Modulation index with respect to: (a) Voltage boost ratio; (b) RMS phase voltage

Modulation index value, m depend on the voltage boost ratio, M as shown in the figure 3.1(a)[14]. The derivation is not shown in this report for brevity. Where the voltage boost ratio is defined as equation (3.5).

$$M = \frac{V_{\text{out}}}{\sqrt{3}\sqrt{2}V_{\text{ph}}} \tag{3.5}$$

Where V_{out} is the output voltage of the converter. For V_{out} =650 V and V_{ph} =230 V, boost ratio is calculated to be M =1.15. From 3.1(a), the modulation index of the converter is m =0.15 for M =1.15. Since the converter is expected to be operated at an input phase voltage of 230 V with a deviation of ±10 V, modulation index for different input voltages are plotted as seen in figure 3.1(b).



(a) (b)

Figure 3.2: (a) Inductor current waveform when inductance is high; (b) Phase voltage, duty cycle with respect to phase angle

The current waveform through an inductor with inductance higher than maximum inductance can be as seen in the figure 3.2(a). It can be observed that the currents are not reaching zero at angles 60° and 120° in each half cycle. The input phase voltage and the instantaneous duty cycle are as shown in figure 3.2(b). It can be observed that the duty cycle is minimum at 60° and 120° angles of the phase voltage. Thus, the equation (3.2) can be used with instantaneous values of voltage across inductor at 60° and the minimum possible duty cycle. Since the time required for the current to reach zero is not sufficient, the OFF period is considered for the derivation, where the voltage across the inductor will be the difference of output voltage and instantaneous input voltage. Thus, the inductance can be calculated using the formula (3.6).

$$L = \frac{\left[V_{\text{out}} - \hat{V}_{\text{ph}} \sin(60°)\right] D_{\text{min}} T_{\text{sw}}}{\hat{I}_{\text{RMS}} \sin(60°)} 0.418$$

$$L = \frac{\left[V_{\text{out}} - \hat{V}_{\text{ph}} \sin(60°)\right] d[1-m] T_{\text{sw}}}{\hat{I}_{\text{RMS}} \sin(60°)} 0.418 \tag{3.6}$$

To calculate inductance, the average duty cycle value, d needs to be calculated. The average load current, I can be estimated by the equation (3.7) defined in the paper [12].

$$I = \frac{\hat{V}_{\text{ph}}^2 d^2 T_{\text{sw}}}{2L} \frac{1.46}{V_{\text{out}} - 1.67\hat{V}_{\text{ph}}} \tag{3.7}$$

Considering P as the output power and η_{est} as the estimated efficiency of the converter, the input and output currents can be related as,

$$I_{\text{RMS}} = \frac{P}{3\eta_{\text{est}} V_{\text{ph}}} = \frac{V_{\text{out}} I}{3\eta_{\text{est}} V_{\text{ph}}} \tag{3.8}$$

Using equations, (3.6)-(3.8), the equation for average duty cycle can be obtained as given in equation (3.9)

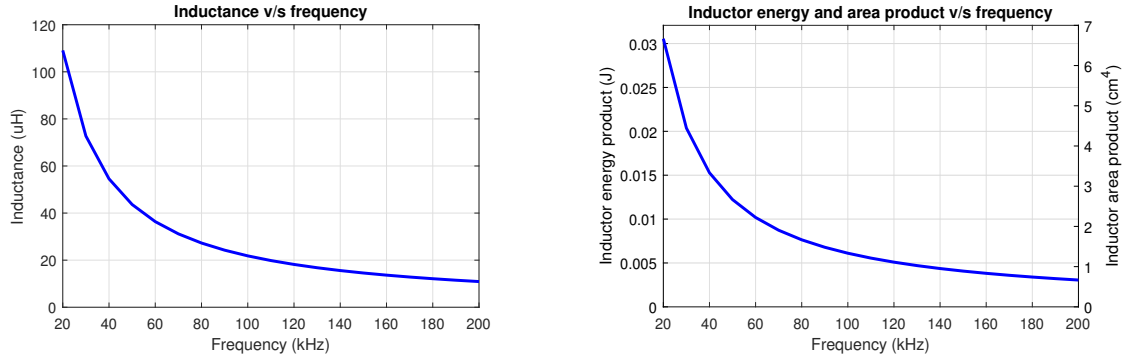
$$d = \frac{\eta_{\text{est}}[1-m][V_{\text{out}} - 1.67\hat{V}_{\text{ph}}]\left[V_{\text{out}} - \hat{V}_{\text{ph}}\sin(60°)\right]}{1.164 V_{\text{out}} \hat{V}_{\text{ph}} \sin(60°)} \tag{3.9}$$

From the duty cycle equation, (3.9), it can be observed that the equation depends only on input and output voltages and the estimated efficiency. Thus, the average duty cycle is independent of the frequency of operation and is calculated to be d =0.1529.

From the average duty cycle value, the maximum inductance can be calculated using the equation, (3.6). But the obtained value is the maximum value, above which the converter won't be at discontinuous conduction mode of operation as shown in the figure 3.2(a), which will make the power factor correction of the converter not achievable.

Hence, an inductance of 95 % the maximum value is selected, which also results the average duty cycle value to 95 % of its initially calculated value, i.e, 0.1452. Hence d =0.1452 is used for the further calculations in this chapter.

Frequencies below 20 kHz can't be used since they fall under audible range and when frequencies which are of several hundreds of kHz are used, the influence of parasitic inductance and capacitances come into the picture, which are complex to analyze for each and every component of the circuit. Thus a frequency range from 20 kHz to 200 kHz is considered for further analysis. The inductance values with energy and area products (95 % of the maximum value) for the various frequencies of operation are calculated using the equations (3.6) and (1.4), and are plotted in the graph as shown in the figure 3.3 for 230 V input and 5 kW, 650 V output.



(a) (b)

Figure 3.3: (a) Inductance; and (b) Inductor's energy and area product with respect to switching frequency (considering k_{Cu} =0.3, J_{RMS} =4.02 A/sqmm and $\hat{B}$ =380 mT)

The voltages and currents of the converter input and output are calculated as below:
Output power, P =5000 W
Output voltage, V_{out} =650 V
Load current, $I = \frac{P}{V_{\text{out}}}$ =7.7 A
Input phase voltage, V_{ph} =230 V
Estimated efficiency, η =98 %
Input power, $P_{in} = \frac{P}{\eta_{\text{est}}}$ =5102 W
Input current, $I_{\text{RMS}} = \frac{P}{3V_{\text{ph}}}$ =7.4 A

3.2. Components design, selection and loss estimation

3.2.1. Inductor:

Component ratings

When the switch is ON, phase voltage appears across the inductor and the inductor current rises from zero to peak current. When the switch is OFF, the differential voltage of input phase voltage and the output voltage appears across the inductor and the inductor current drops back to zero. Hence the maximum voltage across the inductor is the output voltage. After considering a safety limit of 30 % overrating, the inductor components must be rated to a minimum of 845 V.

Calculation of the RMS current through the inductors are quite complex since it involves triangular currents with the different switch OFF time in each switching cycle. Hence the RMS current is found as 9.2 A through simulation. The peak current through the inductor can be estimated using the equation (3.1), which gives a value of 24.5 A. With 30 % overrating, the inductor must be rated to a minimum of 32 A peak current and 12 A RMS current.

Component selection and losses

For a frequency range of 20 kHz to 200 kHz, ferrite materials with MnZn as a base material, are found to have very good permeability, high flux density saturation values and low core losses. Hence are more appropriate to be used as power inductor cores [17]. The detailed design of inductors is presented in appendix A.

Core losses:

At a given frequency of operation, f_s for a designed inductance, the flux density, B can be calculated using (A.8) as given in appendix A. Using these values, the specific loss of a core can be estimated from the specification sheet of the core. Which when multiplied with the core volume, gives the total core losses, P_{core} of the inductor designed.

Copper losses:

The average winding length, l_{Wavg} of wire on an inductor core former will be mentioned in its specification sheet, and also the DC resistance, R_{DC} of wire per unit length will be specified in the wire specification sheet. Using this information, and the number of turns, N of the inductor as calculated from the equation (A.6), the total AC Resistance of the wire can be calculated as follows:

The total wire length, l_{Wtotal} is given by (3.10),

$$l_{\text{Wtotal}} = l_{\text{Wavg}} N \tag{3.10}$$

The total DC resistance, R_{DCtotal} of the wire can be calculated as (3.11)

$$R_{\text{DCtotal}} = l_{\text{Wtotal}} R_{DC} \tag{3.11}$$

But the losses in an inductor depend on the AC resistance of the wire. The AC resistance of the wire mainly depends on the skin effect and the proximity effect of the strands of the wire.

In order to avoid skin effect, the thickness of the individual strands of the wire must be less than the skin depth, δ which can be calculated according to the equation (3.12)[16].

$$\delta = \sqrt{\frac{\rho}{\pi f_s \mu_0 \mu_r}} \tag{3.12}$$

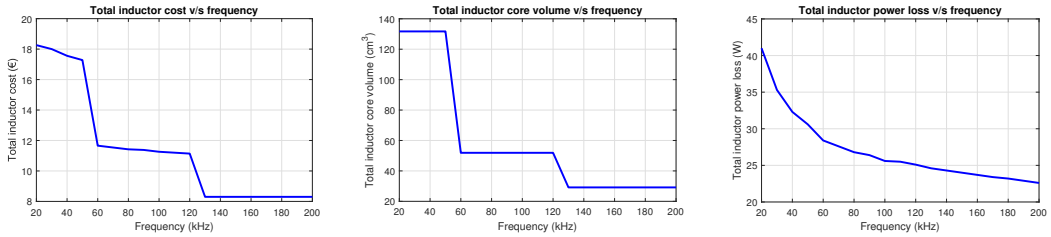
Where μ_0 =$4\pi \times 10^{-7}$ H/m is the permeability of free space and ρ and μ_r are respectively the resistivity (1.68×10^{-8} Ωm for copper) and the relative permeability (1 for copper) of the conductor.

If the winding is having many layers then due to proximity effect the AC resistance of the wire will be high. For less number of layers, and wire thickness less than the skin depth, the AC resistance, R_{ACtotal} can be approximated as twice the DC resistance.

Using the AC resistance of the wire, the copper losses, P_{copper} of the inductor can be calculated as (3.13).

$$P_{\text{copper}} = I_{\text{RMS}}^2 R_{\text{ACtotal}} \tag{3.13}$$

The inductors are designed as specified in appendix A and the core and the copper losses are calculated as discussed in this section. The designed inductors' cost, volume and losses are compared in the figure



(a) (b) (c)

Figure 3.4: Total inductor's: (a) Cost; (b) Volume; (c) Loss with respect to switching frequency

3.4. It can be observed that for lower frequencies, the core volume and the inductor costs are higher and will decrease as the frequency is increased. Instead of a smooth curve, a step change is observed in these curves 3.4(a), 3.4(b), because the cores are available in discrete sizes, and each core is capable of achieving inductance for a particular range of frequencies rather than a single frequency.

The average power loss per unit volume, P_v of an inductor can be approximated [15] using Steinmetz's relation (3.14).

$$P_v = k f_s^a B^b \tag{3.14}$$

Where k, a and b are Steinmetz's coefficients. Considering only the hysteresis and neglecting all the other nonlinearities, the coefficient a will be close to 1 and b will be 2 for nearly all modern magnetic materials.

Since the inductance required and hence the flux required is inversely proportional to the frequency of operation, from Steinmetz's relation (3.14), the losses will also be inversely proportional to the frequency of operation. This can be observed from the figure 3.4(c).

3.2.2. Diode:

Component ratings

When the switch is ON, a complete line-line voltage appears on each of the diodes. When the switch is OFF, a maximum of the output voltage appears on each diode. Thus the diode must be rated to the maximum output voltage. As a factor of safety, components are 30 % overrated. Hence, the diodes are rated for a minimum voltage of 845 V.

The RMS current, I_d through the diodes are found to be 6 A from the simulation. And the peak currents are the same as peak inductor currents. Hence with 30 % higher rating, the diodes are rated for minimum RMS current of 8 A and peak current of 32 A.

Component selection and losses

The major losses in a diode are due to the forward voltage drop of the diodes. However, the diodes also experience switching losses, since the currents switch in the diodes when the switch turns ON/OFF. Hence the diode must also have a lower junction capacitance, C_dj. Diode VS-E5TH3012-N3 is considered for the application.

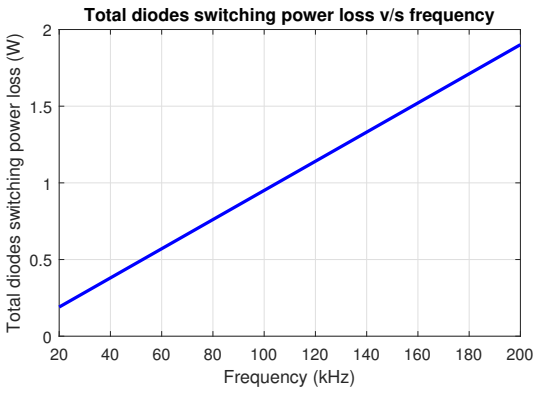


Figure 3.5: Total switching losses in diodes for different switching frequencies

Switching Losses:

The total switching losses for 6 diodes is given by the equation (3.15)

$$P_\mathrm{Sd} = 6\left[0.5 C_\mathrm{dj} V_\mathrm{out}^2 f_s\right] \tag{3.15}$$

The switching losses of the diodes depend on the frequency of operation and will be as shown in figure 3.5.

Conduction Losses:
For a diode with a forward voltage, V_{fd} the conduction loss in the diodes is given by the equation (3.16)

$$P_d = I_d V_{fd} \tag{3.16}$$

For the converter, with the parameters as discussed in the previous section, the conduction loss in each diode is 9.5 W causing a total loss of 28.5 W.

3.2.3. Switch:

Component ratings

RMS current through the switch part, I_{sw} is found to be 3.2 A and through the reverse diode part, I_{srd} is 6.7 A through the simulation. With 30 % higher rating, a switch with a current rating higher than 9 A is considered. The peak current of the switch is the same as peak inductor current 24.5 A. Thus, the peak current rating is 32 A.

The peak voltage across the switch is the same as the output voltage. Hence the rated voltage rating of the switch should be 845 V.

Component selection and losses

For the power circuit to have a small volume, inductance needs to be reduced, in turn, the switching frequency has to be increased in the ranges of tens and hundreds of kHz. Clearly, semiconductor switches other than MOSFETs are not capable of operating at these higher frequencies. Some IGBTs can operate up to around 100 kHz, but have higher ON state voltage drops and are not recommended for low powered applications. Hence MOSFET is considered for the switching of the converter. The losses for a MOSFET depend on the output capacitance of the MOSFET and the ON state resistance of the switch. Hence a switch with comparatively lower output capacitance and lower ON-state resistance is selected. MOSFET STW20N95K5 is considered for the application.

Turn ON Losses:
Turn ON losses of the switch depending on the product of voltage across the switch just before it is switched on and the current of the switch just after the switch is ON. But since the converter is operating in the discontinuous mode of operation, every time the switch becomes ON, the current just starts to rise from zero. Since the current is zero at the instant when the switch is switched ON, the turn ON losses for the converter is zero.

Turn OFF Losses:
Turn OFF losses depend on the product of voltage across the switch at the instant when the switch is OFF and the current through the switch at the instant just before the switch is OFF. The losses will be sufficiently high if the current and the voltage are high. To avoid these losses a snubber circuit could be implemented, the simplest would be to place a capacitor, C_{snub} in parallel to the MOSFET (as a turn OFF snubber). Thus, at the instant of turn OFF, the current is diverted to the capacitor and the current through the MOSFET will be negligible resulting in zero turn-OFF losses in the MOSFET.

The required snubber capacitor for the converter can be calculated from the equation (3.17) [9].

$$C_{snub} = \frac{I_{Lp} t_{fi}}{2 V_{out}} \tag{3.17}$$

Where t_{fi} is the current fall time of the switch, which is 18 ns for the considered switch. For a peak current of 24.5 A and an output voltage of 650 V, the snubber capacitance value is obtained as 340 pF.

When the switch starts to OFF, the voltage across the switch will be still low, at this stage the output capacitance of the switch is in the range of 10 000 pF according to the datasheet. Thus there is no requirement of additional snubber capacitor for the considered converter.

However, there will be a loss due to the output capacitance of the switch, which can be calculated as equation (3.18).

$$P_{Coss} = E_{oss} f_s \tag{3.18}$$

Where E_{oss} is the stored energy of switch's output capacitor, which is a function of drain-source voltage, V_{ds}. At V_{ds} =650 V, E_{oss} =15 µJ from the datasheet. Thus, the switch capacitor loss is the only switching loss of the MOSFET and it linearly depends on the frequency of switching as shown in figure 3.6.

Conduction Losses:

Apart from the switching losses, there are losses in the MOSFET during conduction as well. These losses depend on the ON state resistance, R_{dsON} of the MOSFET and the forward voltage drop, V_{SD} of the reverse diode. The conduction losses for the MOSFET part and the diode part can be calculated as shown in the equations 3.19 and 3.20 respectively.

$$P_{sM} = I_{\text{sw}}^2 R_{\text{dsON}} \tag{3.19}$$

$$P_{sRD} = I_{\text{srd}} V_{\text{SD}} \tag{3.20}$$

For the selected MOSFET, R_{dsON} =0.74 Ω (at 150 °C) and V_{SD} =0.8 V, thus leading to a MOSFET losses of P_{sM} =7.4 W and P_{sRD} =5.4 W, causing totally 12.8 W per MOSFET and 38.4 W for all the MOSFETs.

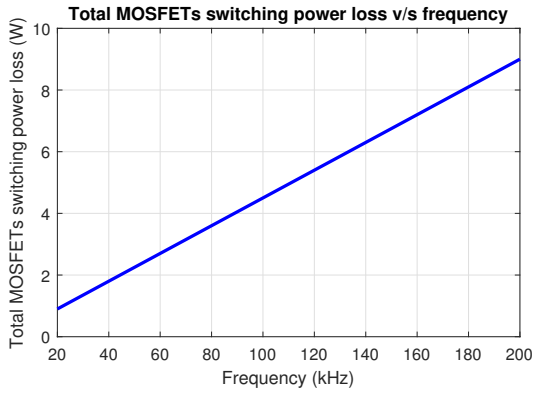


Figure 3.6: Switching losses in MOSFET for different switching frequencies

3.2.4. Output capacitor:

Component ratings

The simulation results suggest that the ripple current through the output capacitor, I_{Crms} is 7.5 A.

The voltage across the capacitor will be the same as the output voltage. Hence the capacitor must also be rated at 845 V.

Component selection and losses

For the capacitors to have a lifetime of around 10 years, the capacitors ELXS451VSN271MQ45S are considered in 2 series and 2 parallel configuration [1].

The dissipation factor, $\tan\delta$ of each capacitor is 0.2. Thus, the equivalent series resistance (ESR) of the capacitor is given by the equation (3.21).

$$ESR = \frac{\tan\delta}{2\pi f_s C} \tag{3.21}$$

Depending on the series and parallel configurations connected the total ESR, ESR_t of the combined capacitance can be calculated similar to the total resistance calculation from a series-parallel combination. For two series, two parallel connection the equivalent resistance remains the same as the resistance of the single component. Hence, $ESR_t = ESR$.

The losses in the capacitor due to its ESR is given by equation (3.22)

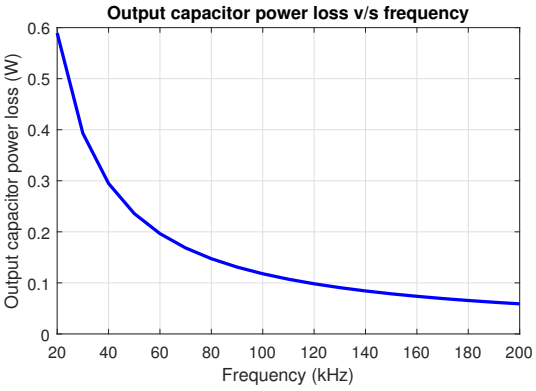


Figure 3.7: Losses in output capacitor for different switching frequencies

$$P_C = I_{\text{Crms}}^2 ESR_t \tag{3.22}$$

The ESR of the capacitor varies with respect to frequency of operation, and thus the losses in the capacitor vary with respect to the frequency of operation and are as shown in the figure 3.7.

3.3. Frequency of operation

In the previous section, all the possible losses for the components used in the converter are considered. The frequency of operation can be finalized once the total converter losses/efficiency and the volume comparisons are done. It must be noted that the EMI filters are still not considered for the comparisons since EMI filter will be designed based on the EMI content, which depends on the frequency of operation.

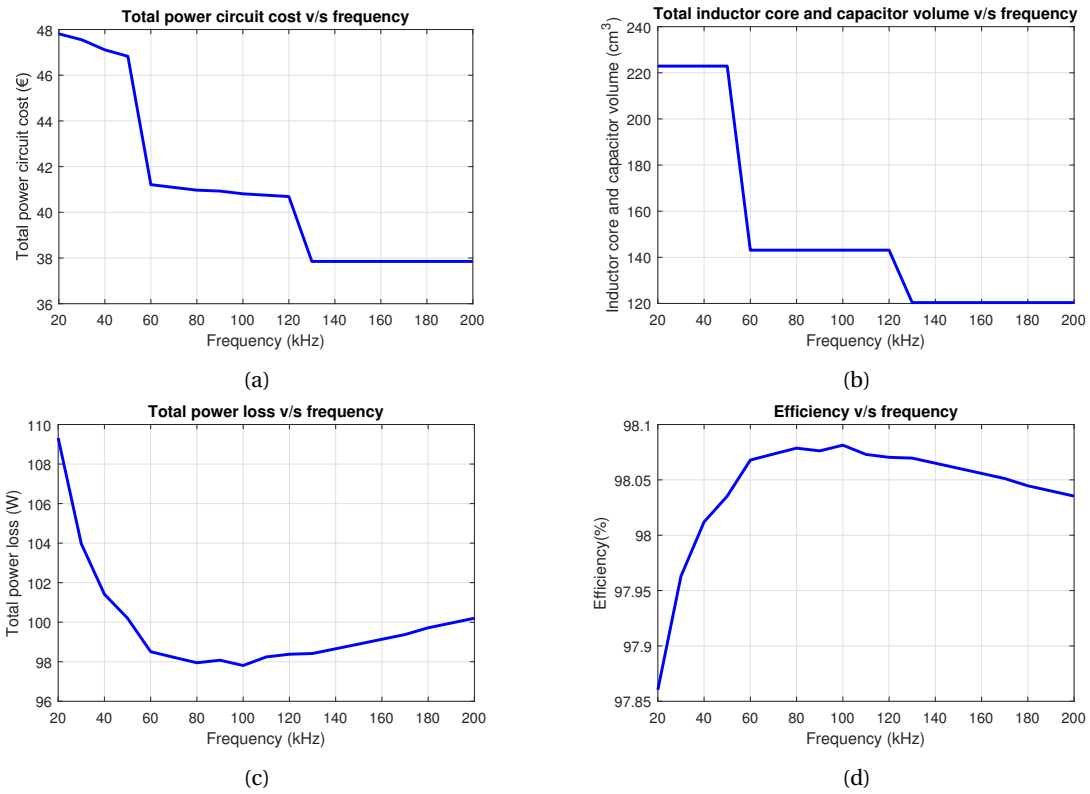


Figure 3.8: Converter's: (a) Cost; (b) Volume; (c) Losses; (d) Efficiency with respect to switching frequency

The comparisons for the total cost, volume, losses and efficiency are done in figure 3.8. From the cost and volume comparisons it can be analyzed that for frequency less than 60 kHz, the converter volume is considerably bigger (50 %) and costlier (14 %) than for the medium frequency (around 100 kHz) range of operation. Whereas, for frequencies above 130 kHz, the reduction in converter size (14 % smaller) and cost (7 % cheaper) are a bit less.

From the loss/efficiency analysis, it can be observed that the efficiency for all the frequency ranges is around 98 %, with ±0.15 % deviation only, which is not a considerable difference in efficiency.

However, as the operating frequency is nearing to 200 kHz, the effect of parasitic components in the circuit starts increasing. Hence, the frequency of operation is considered to be 130 kHz, where the converter size is the smallest, cost is the cheapest and the effect of parasitic components are not considerable and efficiency is almost near the maximum possible efficiency. At 130 kHz, the inductance is calculated to be 17 µH, according to the procedure given under section 3.1.

3.4. Heat sink design

The chosen diodes and switches are non-insulated. Hence a thermally conductive insulation material is required to connect them to the heat sink. Insulation for the heat sink is considered to be PL-05-3-1016, which has a thickness, Δl of 0.5 mm, and diode case to heat sink thermal resistivity, $R_{\theta\mathrm{CH,d}}$ of 1.5 °C/W and MOSFET case to heat sink thermal resistivity, $R_{\theta\mathrm{CH,M}}$ of 0.75 °C/W.

The diodes are having a conduction and switching power losses of 9.5 W and 0.4 W each respectively, causing a total dissipation of around 10 W per diode. The junction to case thermal resistance, $R_{\theta\mathrm{JC,d}}$ of a diode is 1.2 °C/W. Considering the maximum junction temperature, $T_{\mathrm{J,d}}$ as 170 °C and a maximum ambient temperature, T_{A} as 50 °C, for diode power dissipation, $P_{\mathrm{loss,d}}$ of 10 W, the maximum possible heat sink temperature, T_{H} should be 150 °C according to (3.23).

$$T_{\mathrm{H}} = T_{\mathrm{J,x}} - P_{\mathrm{loss,x}}\left[R_{\theta\mathrm{JC,x}} + R_{\theta\mathrm{CH,x}}\right] \tag{3.23}$$

Where x can be either d (diode) or M (MOSFET) according to the application of the equation.

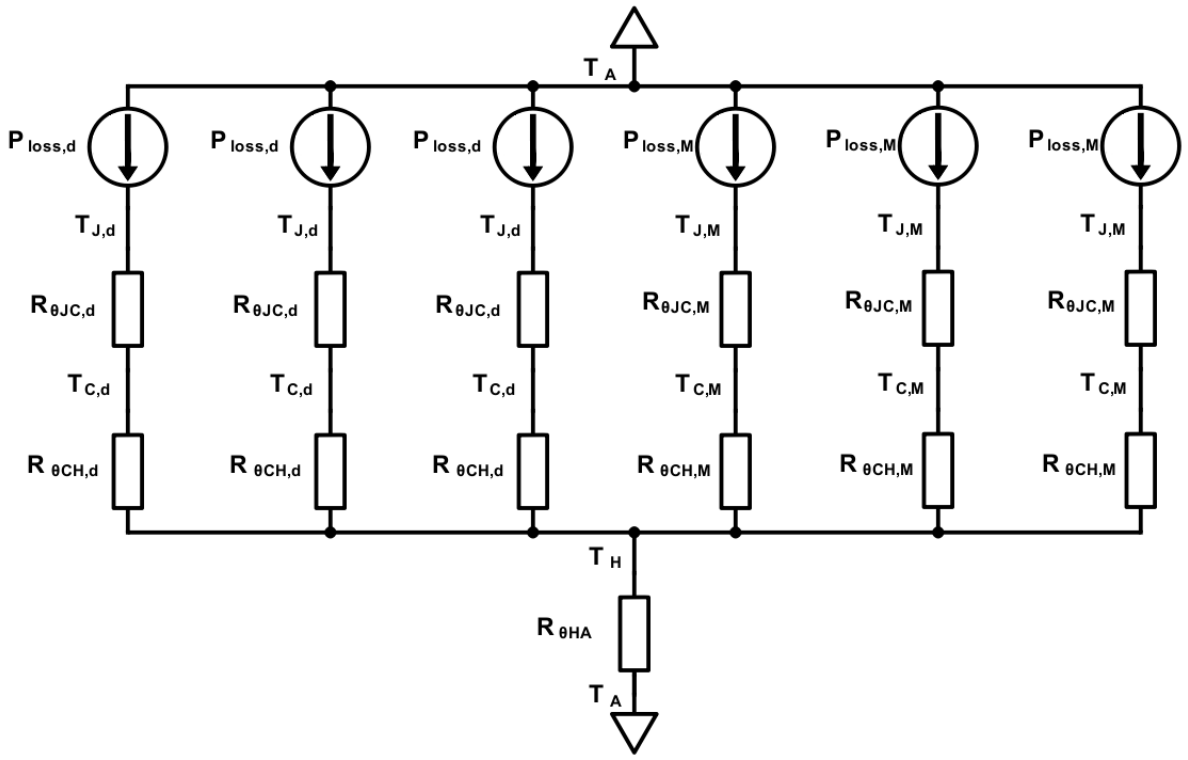


Figure 3.9: Thermal circuit for diodes and MOSFETs of the converter

The MOSFET has a conduction loss of 12.8 W and switching loss of 2.1 W, causing a total loss of around 14.9 W. The MOSFET has a $R_{\theta JC,M}$ of 0.5 °C/W. Considering the $T_{J,M}$ as 145 °C and T_A as 50 °C, for MOSFET power loss, $P_{loss,M}$ of 14.9 W, the maximum possible heat sink temperature according to (3.23) will be, $T_H = 126$ °C.

Thus, considering both MOSFETs and diodes, the maximum heat sink temperature can be 126 °C. Considering all the six semiconductor devices, the total losses will be 74.7 W. Thus, the thermal resistance, $R_{\theta HA}$ of the heat sink must be less than 1 °C/W according to (3.24).

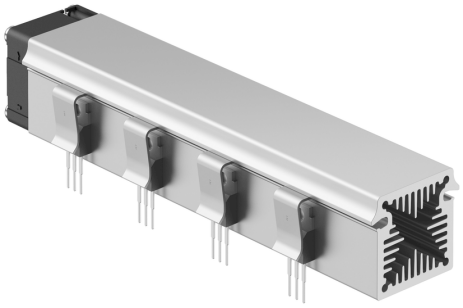


Figure 3.10: Heat sink for the power diodes and MOSFETs

$$R_{\theta HA} = \frac{T_H - T_A}{\sum_{\forall \text{diodes,MOSFETs}} P_{loss,x}} \tag{3.24}$$

The considered heat sink, LAM 3 K 100 12 is as shown in the figure 3.10.

3.5. EMI filter design

Due to the switching of MOSFET, there will be EMI emitted from the converter circuit. The body capacitance of the diodes and the switch causes the generation of common mode EMI. When the heat sinks of semiconductor devices are not grounded, the EMI will be very negligible, but it will not be safe to operate the converter having a large ungrounded metal object. Hence, it is important to model the body capacitance of the semiconductor devices.

The diodes and switches are un-insulated but have a silicone insulation material between them and heat sink, which act as a capacitor. The maximum dielectric constant, ε_r of the silicone material will be around 5. The thickness, Δl of the considered material is 0.5 mm. Thus the capacitance can be calculated using the formula (3.25).

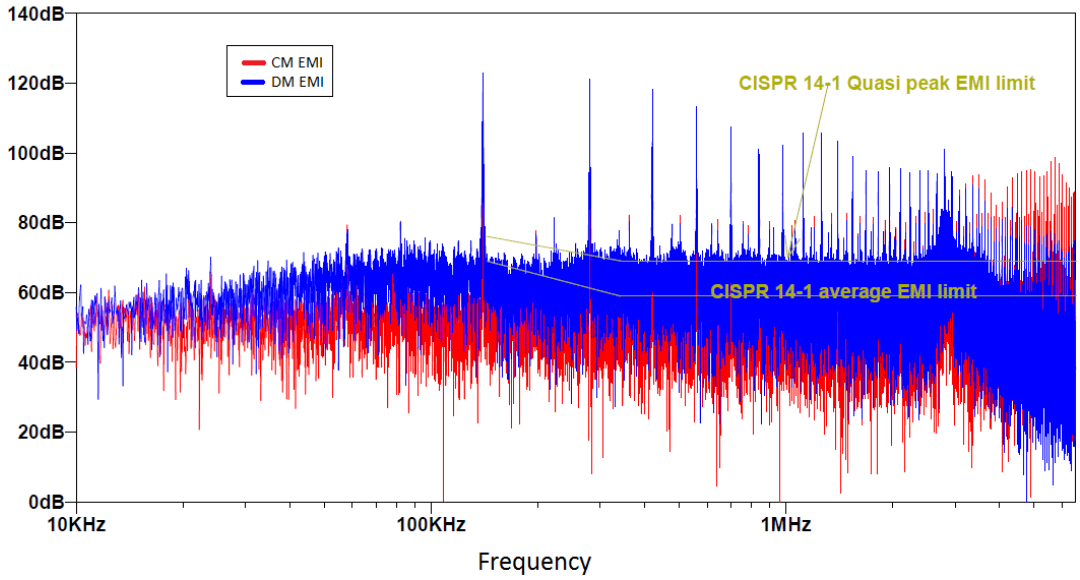


Figure 3.11: Simulated CM and DM EMI emission from the converter without EMI Filter

$$C_{body} = \frac{\varepsilon_0 \varepsilon_r A}{\Delta l} \tag{3.25}$$

Where A is the area of the insulator(area of Diode/MOSFET).
Thus the body capacitance of the diodes and MOSFETs are modelled to be capacitors of 14.5 pF and 29.7 pF capacitance respectively. With the selected frequency of operation, the converter is simulated in the Simulink along with a line impedance stabilization network (LISN) model to measure the EMI content generated from the converter. The common mode (CM) EMI and differential mode (DM) EMI are simulated and are plotted as shown in figure 3.11.

From the figure, DM EMI needs to be reduced by 60 dB and CM EMI needs to be reduced by 40 dB above 150 kHz in order to satisfy the EMI Standard CISPR 14-1:2005.

Since the power source will be associated with the line inductance and the converter consist of inductors at its first part of the circuit, the line and the converter are of high impedance for the high-frequency components. Thus, a Π filter (CLC) needs to be designed for the converter with noise suppression for both CM and DM EMI at 150 kHz, as shown in figure 3.12. The capacitors connected between two lines are called X capacitors and the capacitors connected between PE and other lines are considered to be Y capacitors. The Y capacitors along with CM choke remove the CM EMI. CM choke also has a bit of differential inductance. The X capacitors along with the differential inductance remove the DM EMI.

3.5.1. Common mode filter design:

To limit the PE current less than 3.5 mA as suggested by IEC 60335 standard, the Y capacitors must have smaller capacitance. Thus, the CM choke needs to be of higher inductance. The considered CM choke is RT8532-10-4M0, which has a CM inductance of 4 mH and a DM inductance of 16 µH. To obtain an attenuation of 40 dB, the Y capacitors are chosen to be 33 nF and 47 nF. When this CM filter is simulated, a high peak is observed at 10 kHz, to decrease this peak, a damping resistor of 3.3 Ω has been used in the CM path. The resistance dampens the peak by 40 dB.

3.5.2. Differential filter design:

The inductors of the converter along with the X-filter capacitors connecting to it will form the first LC filter (2^{nd} order filter with suppression of 40 dB/decade). Another pair of an inductor (differential inductance of the CM choke) and a capacitor present in the Π filter will form the second LC filter. The combined attenuation of both the filters must be optimized to achieve 60 dB noise suppression at 150 kHz.

Each of the filter is designed for a 30 dB attenuation, so that the total attenuation at 150 kHz is 60 dB. Since both the filter stage have the nearly same differential inductances, their design will be the same.Since

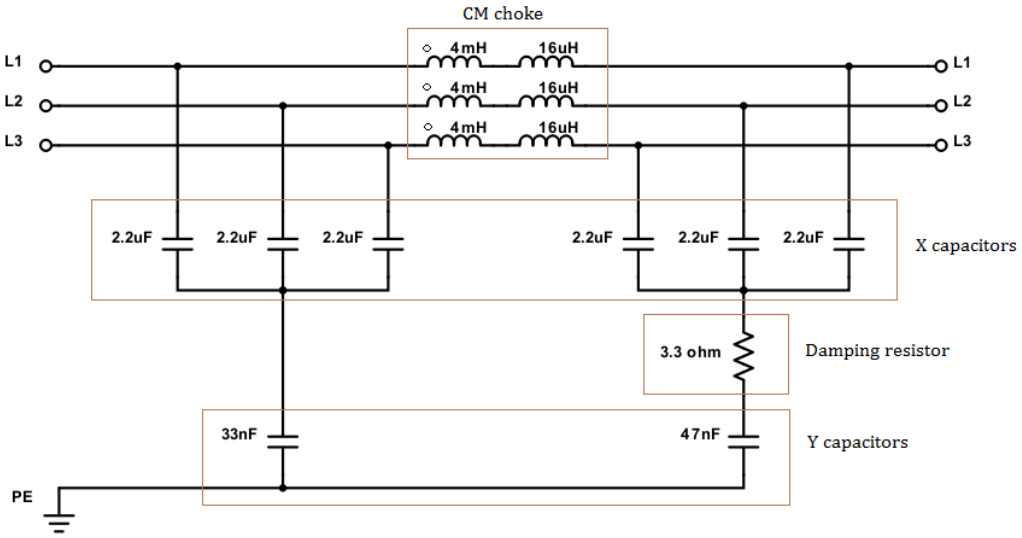


Figure 3.12: EMI filter

the required attenuation is 30 dB, the cut off frequency must be calculated as shown below:
For a second order filter, attenuation is 40 dB/decade, thus for an attenuation of 30 dB, 30/40 =0.75 decade is necessary. Since, $\log \frac{150000}{f_{c1}}$ =0.75 decade
Cut off frequency is given by, $f_{c1} = \frac{150000}{10^{0.75}}$ =27 kHz.
The cut-off frequency, f_c of a LC filter is given by the equation (3.26).

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{3.26}$$

Where L and C are the inductance and capacitance of the filter respectively.
Since the inductance of the converter is 17 µH. Using equation (3.26), the capacitors for the filters, C are calculated to be 2.2 µF.

With the designed filter, the converter is simulated with the LISN circuit again to verify the EMI attenuation as shown in figure 3.13. From the figure 3.13 it can be observed that the EMI emission is below the limits prescribed by EMI standard.

3.6. Microcontroller

The converter requires a controller to generate the gate pulses for the MOSFET. Since the application is having only one MOSFET, a simple micro-controller would be sufficient for the application.

Required microcontroller specification:

- To drive gate driver circuits, the output current of the pins must be rated at least around 20 mA.
- For easy programming, the micro-controller must have an FPU, so that it is compatible with floating point numbers.
- For controlling, the controller requires a current measurement and two voltage measurements and hence must contain at least 3 analog to digital converter (ADC) to measure input and output voltages and current. In the actual motor drive application, the output voltage and current details could actually be taken from the motor drive itself. But for implementation of the converter without motor drive, additional current/voltage measurements might be required.
- Considering a voltage measurement of 1000 V, with an accuracy of 0.25 V, the ADC must at least have the capability of 1000/0.25 = 4000 digital values, hence ADC must have a 12bit (2^{12} = 4096 values) conversion.

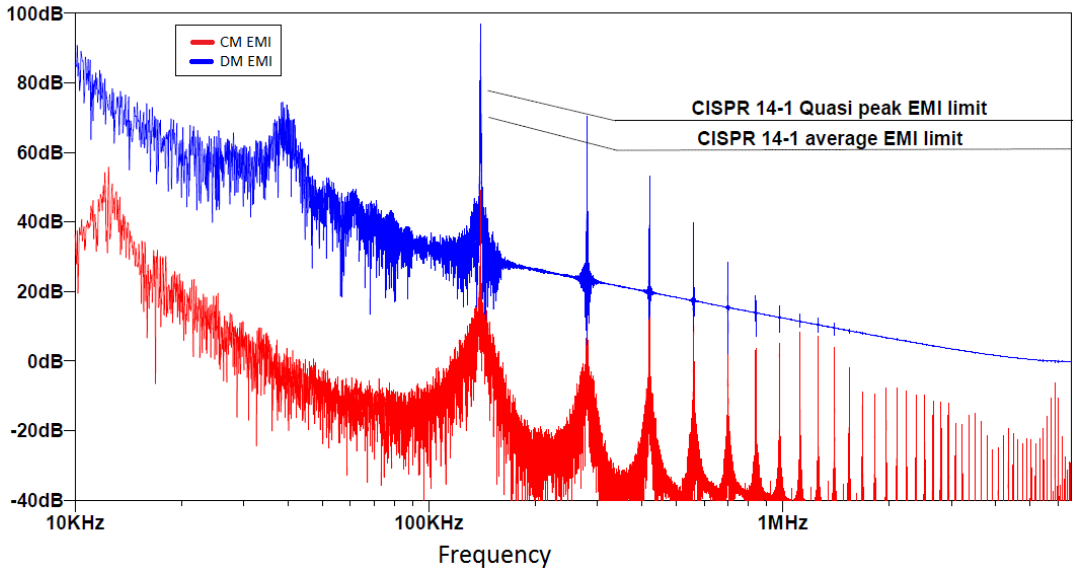


Figure 3.13: Simulated CM and DM EMI emission from the converter with EMI filter

- Micro-controller must have at least 2 basic timer circuits to implement delays and other functions in the program.
- To have an option of reprogramming, either FLASH or EPROM is necessary.
- Considering each instruction as 2 bytes and considering a maximum of 500 instructions, a 1 kB program memory would be sufficient.

Microcontroller STM32F407VET6, is selected for the application, since it is capable of delivering an output current of maximum of 25 mA, it has 3 channel 12 bit ADC, with 1 MB of FLASH type program memory, 4 kB RAM, 17 timers, 32-Bit Cortex®-M4 processor, which is fast enough to do the basic duty cycle calculations and generating gate pulses.

The microcontroller can be operated with a supply voltage of 2.4 VDC to 3.6 VDC. Hence a voltage of 3.3 VDC is selected as supply voltage. The microcontroller is capable of producing a low logic output voltage less than 0.4 V and a high logic output voltage more than 2.9 V, for a load current of 8 mA. Hence a power supply IC generating 3.3 VDC is required. The maximum current consumption is 240 mA, hence a maximum power requirement of 792 mW.

3.7. Gate driver

The converter is operating at discontinuous conduction mode and has almost zero switching losses. Thus, there is no strict requirement for the switch ON and switch OFF times of the MOSFET.

The switch used in the converter is a low sided single MOSFET. Hence a low side single MOSFET driver IC is required for our application. Gate driver FAN3100T suits the required application. The driver circuit is capable of driving around 2 A gate current using a controller current of only 0.2 mA. The gate driver considers input voltage less than 0.8 V as low logic and greater than 2 V as high logic. The gate voltage is considered to be 12 V, which is almost thrice the plateau voltage of the selected switch. The switch is having a very low input capacitance around 1 nF. From the data sheet of the gate driver, it can be observed that the gate driver provides the current through bypass capacitor which prevents oscillations during switching and the datasheet recommends to keep the line resistance and inductance minimum to achieve a fast switching. However, the datasheet of the MOSFET specify the typical gate resistance value as 1 Ω, hence a resistance of 1 Ω is used for the gate driver circuit.

The gate driver requires a 12 VDC power source, hence a power supply IC generating 12 VDC is required. The maximum current consumption is 0.8 mA, hence a maximum power requirement of 9.6 mW.

3.8. Efficiency and volume of the complete circuit

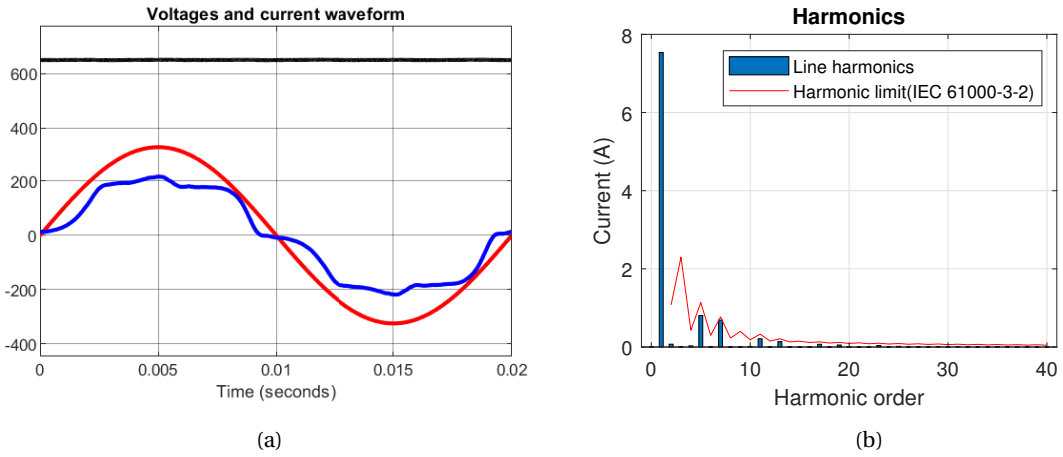
The addition of all the other circuits to the power circuit has added additional cost, volume and losses. These additional quantities are tabulated and the total cost, volume and the losses of the complete power circuit and thus the efficiency of the complete circuit is calculated and tabulated as shown in the table 3.1.

Table 3.1: Total cost, volume and losses of the complete converter circuit (cost is considered for 1000pcs from digikey.com)

	Components	Cost (€)		Volume(cm3)		Losses/power consumption (W)	
EMI Filter	Inductors	5.70	10.11	88.30	157.36	2.46	2.46
	Capacitors	4.41		69.06		0.00	
Power Circuit	Inductors	8.20	37.75	29.16	127.50	24.30	98.61
	Rectifier Diodes	2.55		2.24		29.63	
	MOSFETs	17.40		4.90		44.60	
	Output Capacitors	9.60		91.20		0.08	
	Total	47.86		284.86		101.07	

From the tabulation, it can be observed that the total losses in the complete converter is 101.07 W. Hence the estimated efficiency of the designed converter is 98 % at full load. Also, from the simulation, PF of the converter is around 0.989.

The voltage and current waveform are as shown in figure 3.14(a). It can be observed that the input current is almost sinusoidal, but has few lower order harmonics. These harmonics are as shown in figure 3.14(b). It can be observed that the considered converter satisfies the IEC harmonic limits at 5 kW output.



(a) (b)

Figure 3.14: (a) Voltage and current waveform of the converter; (b) Input current harmonics at 5 kW output

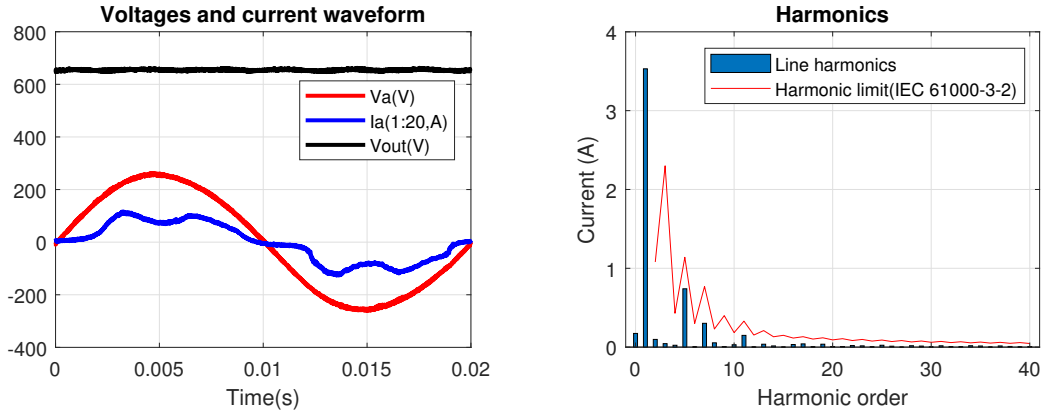
4

Converter Testing and Evaluation

The converter designed in the chapter 3 is developed in the lab of Applied Micro Electronics "AME" B.V. and has been experimented to evaluate its performance and to prove the validity of the novel controller as designed in the chapter 2. Due to the unavailability of the high power isolated power supply at the lab, the developed converter is tested only up to the power range of 2.4 kW instead of 5 kW. This chapter discusses the experimental results of the designed converter and also discusses the feasibility, merits and demerits of the converter and its control strategy in the subsequent sections.

4.1. Performance evaluation

The converter is operated around 2.4 kW, the waveform of the current and its harmonic distribution are as shown in the figures 4.1(a) and 4.1(b) respectively.



(a) (b)

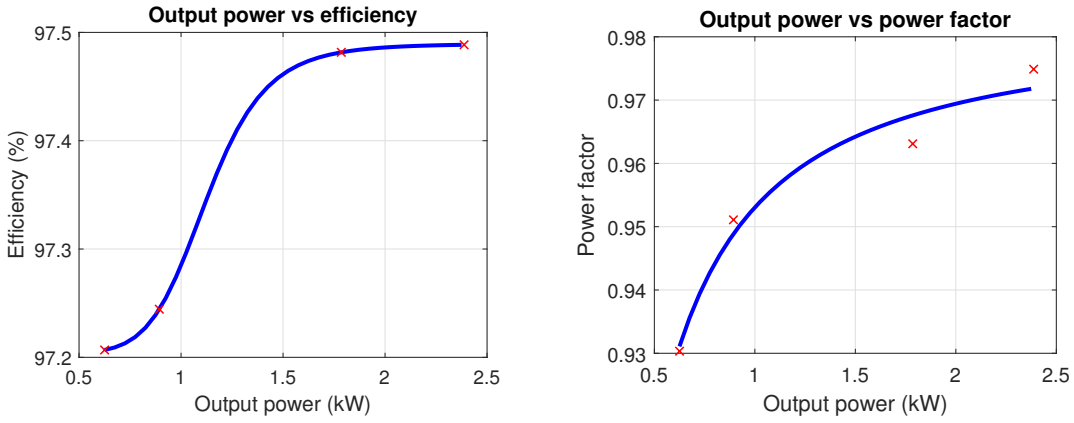
Figure 4.1: (a) Voltage and current waveform of the developed converter; (b) Input current harmonics at 2.4 kW output

From the figure 4.1(a), it can be observed that the output current is still not a perfect sine wave and it still has different harmonic contents, but the harmonic contents are well with in the prescribed limit of the standards as seen in the figure 4.1(b). From figure 4.1(a), it can also be observed that there are slight variations in the output voltage due to the 6^{th} harmonic content in the output voltage.

The converter has been tested to measure the efficiency and the power factor at different output power levels. The results are plotted as shown in the figures 4.2(a) and 4.2(b) respectively.

It can be observed from the figures that the efficiency and the power factors are increasing with respect to the output power levels. This is because the converter is designed to have the highest efficiency and power factor at its full load.

According to the chapter 3, the efficiency at full load is supposed to be 98 %. Since the voltage drops across the semiconductor devices and the inductor core losses remain almost the same even for the lower power



(a) (b)

Figure 4.2: (a) Efficiency; (b) Power factor at different output power levels

output, the efficiency at lower power levels decreases. But from figure 4.2(a) it appears that the efficiency at full load might still not reach the expected value of 98 %. This lowered efficiency might be due to higher losses in inductors and semiconductor devices than the expected. The calculations in the chapter 3 considers the respective RMS currents for the voltage drop/resistance values of the semiconductor devices. However, the currents in the converter are in discontinuous conduction mode, which causes high peak currents which might lead to a bit higher losses than expected.

According to the chapter 3, the power factor at full load is supposed to be 0.989. From figure 4.2(b), the power factor of the developed converter appears to reach the expected power factor at full load.

4.2. Controller design validation

The designed novel controller is supposed to be stable with respect to the line and the load transients. Hence the developed converter is subjected to the line and load transients and its performance is analysed if it works similar to the simulation results of the chapter 2.

4.2.1. Controller stability for line transients

The converter is operated with a load of 2.25 A and the input phase voltages are changed instantaneously to check the stability of the designed controller for line transients.

The figures showing the voltage and duty cycle values are having noisy waveform, but step changes can still be observed to analyse the controller behaviour.

From figure 4.3, it can be seen that the input phase voltage is decreased suddenly from 220 V RMS to 210 V RMS at 0.05 s. This decrease in input voltage leads to a sudden decrease in the output voltage. It can be observed that the duty of the formula controller changes as soon as it detects a change (requires at least one cycle of input voltage to detect the change, i.e.,20 ms) in the input voltage. The change in the duty cycle from the formula controller makes the output voltage to increase back to 640 V. It can be observed that the output voltage value gets settled almost after 0.05 s, for lower loads, the settling time is much higher as discussed in the chapter 2. Since there will be errors in the calculation from the formula based controller at real time, the output voltage is settling at a voltage different from the reference voltage 650 V. This difference in the output voltage act as feedback to the error based controller. It can be observed from the figure 4.3, that the error based controller changes the error value, only after 0.1 s after the formula based controller acts, this allows sufficient time for the voltage to settle down even for low load conditions. This change in the duty error value will make the output voltage to reach the reference voltage.

From figure 4.4, it can be observed that the input phase voltage is increased suddenly from 220 V RMS to 230 V RMS at 0.05 s. This increase in input voltage leads to a sudden increase in the output voltage. It can be observed that the duty of the formula controller changes as soon as it detects a change in the input voltage. The change in the duty cycle from the formula controller makes the output voltage to decrease back to 650 V. Since the output voltage is the same as the reference voltage 650 V, there will be no change in the duty cycle from the error controller in this case.

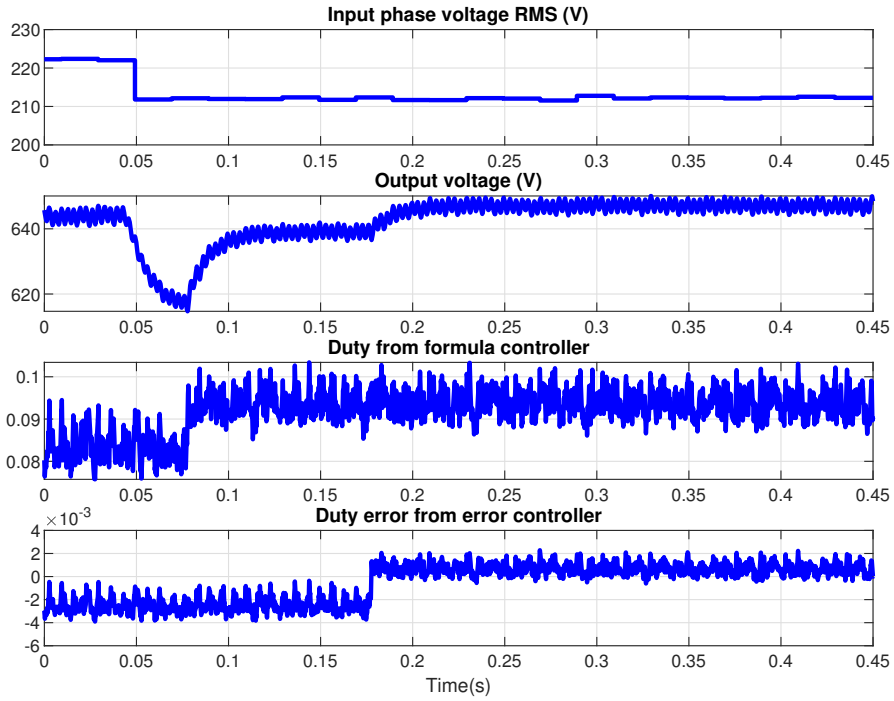


Figure 4.3: Converter output for decrease in RMS phase voltage

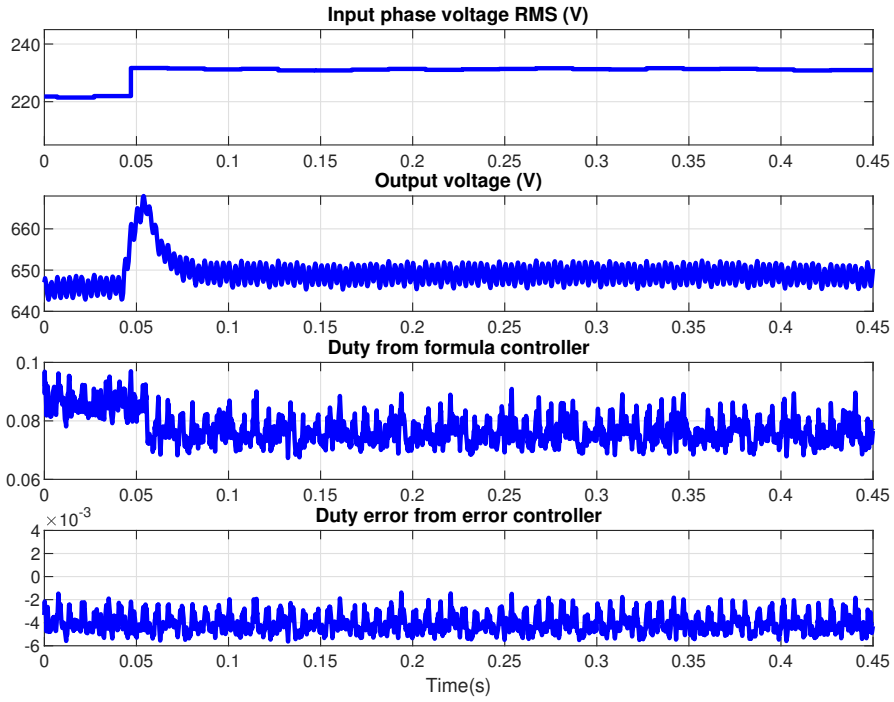


Figure 4.4: Converter output for increase in RMS phase voltage

4.2.2. Controller stability for load transients

The converter is operated with at an input phase voltage of 230 V RMS and the load is changed instantaneously to check the stability of the designed controller for load transients.

From figure 4.5, it can be seen that the load is decreased suddenly from 2.25 A to 1.2 A at 0.05 s. This decrease in load leads to a sudden increase in the output voltage. It can be observed that the duty of the formula controller changes as soon as it detects a change in the load. The change in the duty cycle from the formula controller limits the output voltage increase to increase till 680 V. It can be observed that the output voltage value gets settled almost after 0.1 s, since the load is half compared to the previous cases.

The difference in the output voltage act as feedback to the error based controller and it changes the duty error value. This change in the duty error value will make the output voltage to converge towards the reference voltage, but still not to the reference voltage itself. This is because the error based controller is a linearised controller, which will be accurate only for smaller voltage differences. For higher voltage differences as discussed in section 2.3.2, it requires more iterations of the error based controller to make the output voltage converge to the reference voltage level as seen in the figure 4.5.

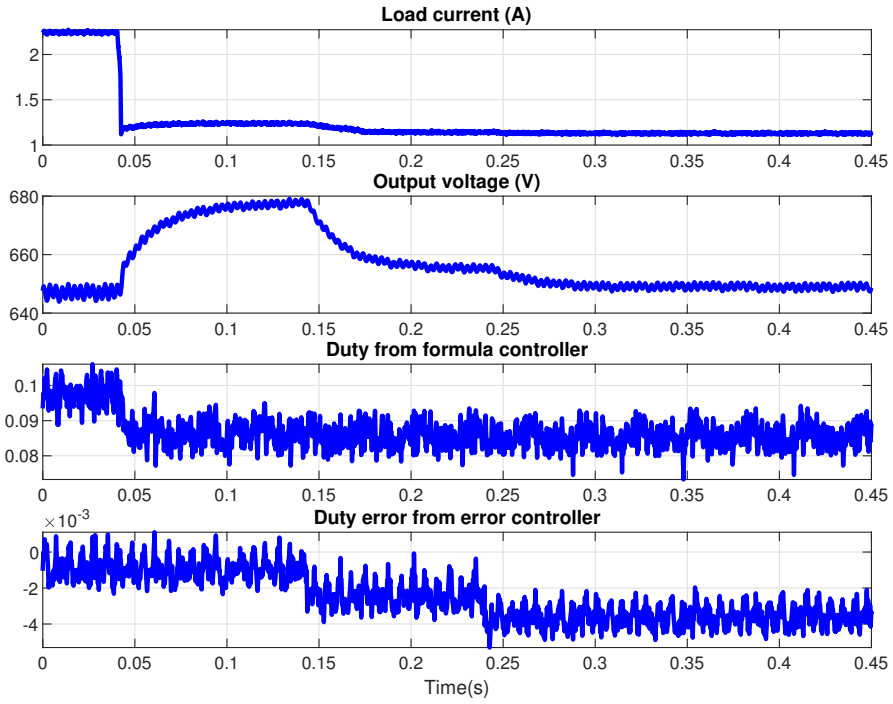


Figure 4.5: Converter output for decrease in load

Similarly the converter is subjected to a sudden load increase from 1.2 A to 2.25 A at 0.05 s as shown in the figure 4.6. It can be observed that the formula based controller together with error based controller stabilises the output voltage for the load transients as well.

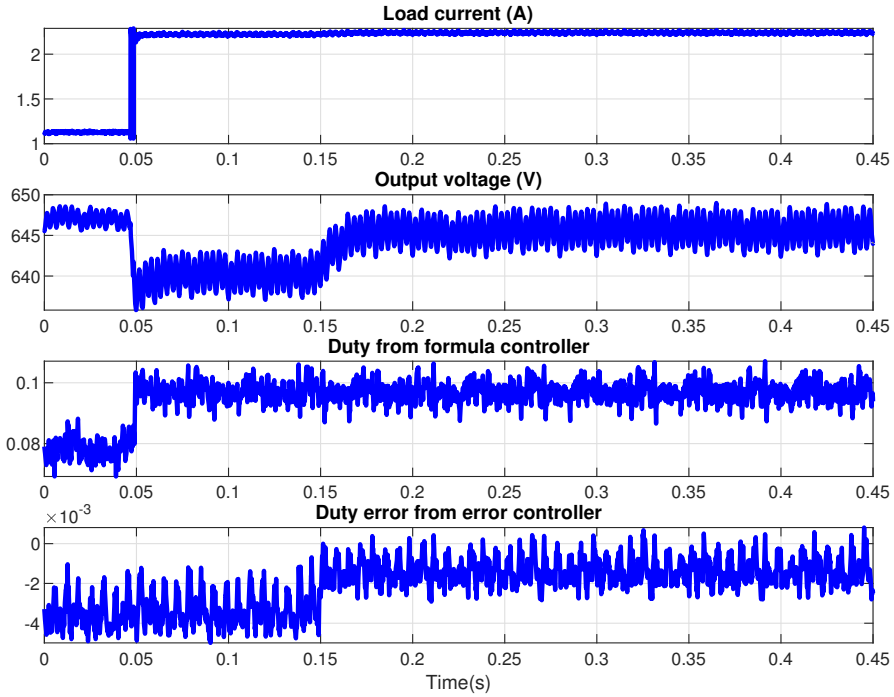


Figure 4.6: Converter output for increase in load

4.3. Conclusion

The three-phase PFCs for various power ranges are analyzed and compared. It can be concluded that the cost-effective solution for power ranges less than 7.5 kW will be the three switch bridgeless PFC and for power ranges above 7.5 kW Vienna rectifier will be the cost-efficient solution.
A robust unconventional controller comprised of formula based and an error based controller has been designed to control the three switch bridgeless PFC converter in a stable way during the line and the load transients.
The converter and its frequency of operation have been designed considering the minimum cost and volume of the complete converter with an almost maximum possible efficiency.
From the testing and validation of the developed converter, it can be concluded that the designed controller, is capable of ignoring the low-frequency harmonics at the output, yet capable of regulating the output voltage during load transients and input voltage fluctuations as per the research question of this thesis.

Thus, the obtained converter is robust and the cost-effective implementation of a three switch bridgeless PFC converter.

4.4. Future research

During the testing of the designed converter, it was found that the modulation level of sixth harmonic injection as determined in section 3.1 is best applicable for the full load conditions. During lower load conditions, a reduced modulation level was sufficient for achieving a better power factor. However, in literature, the modulation index level depends only on the output voltage level. Thus, a detailed study on the modulation index with respect to the various load level can be done.

During the testing of the converter, the three phase isolated power supply was supplying an unbalanced phase voltage, this resulted in a higher current through the damping resistor of the common mode filter than its rating. Hence, this resistor was removed for testing purposes, resulting in the loss of a common mode path for EMI filtering. Since this common mode path was supposed to filter around 36 dB of CM EMI, the total EMI content in the converter is supposed to be increased by the same amount. However, the actual results suggest that the total EMI is around 46 dB higher than the limit as seen in figure 4.7. Thus, the EMI filter needs to be

increased by a bit to compensate for this extra 10 dB of EMI, which might have caused due to inaccuracies in component values.

The developed converter measures a single phase voltage assuming that the supply is balanced. But this could damage the converter during the connection of an unbalanced supply. Hence the converter must be programmed to measure all the three phase voltages and stop the converter operation whenever it detects an unbalanced supply.

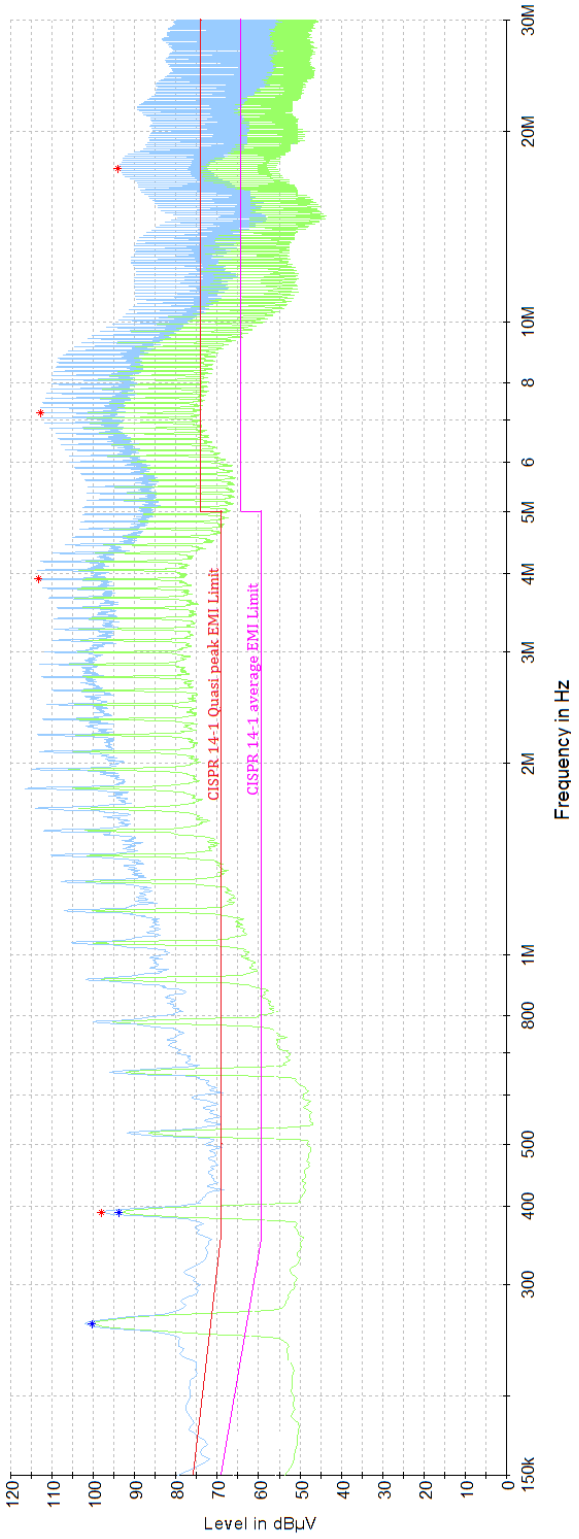


Figure 4.7: Total (CM+DM) EMI measured (blue: quasi peak emission, green: average emission) from the developed converter

A

Appendix: Design of an inductor

Designing an inductor is an iterative process, where it can be told whether the selected core is suitable for a particular inductance and currents, but it is impossible to tell an exact dimension of the required inductor core from the inductance values and current values. The fact that there are cores with many different shapes and sizes, makes it still cumbersome for the inductor design. The following method is used in this report to design an inductor of required inductance, L.
Energy product of the inductor can be found my multiplying the inductance value with the peak, $\hat{I}$ and RMS currents, I_{RMS} of the inductor. The preliminary requirement of the inductor core selection is that the core should be capable of having the product value higher than the required energy product according to the equation (A.1).

$$L\hat{I}I_{\text{RMS}} = k_{Cu}J_{\text{RMS}}\hat{B}A_wA_{\text{core}} \tag{A.1}$$

Where, k_{Cu} is the copper fill factor for a wire which will be generally 0.3 for litz wire and around 0.5 for single conductor wire, J_{RMS} is the current density of the wire which will be around 4.02 A/sqmm for copper, $\hat{B}$ is the peak magnetic flux density in the core which can be generally considered as 300 mT while designing for MnZn ferrite cores (This is an approximate value only, exact value will be found in the core data sheet), A_w is the total winding area and A_{core} is the core area of the inductor.

Thus for a given frequency of operation, the inductor area product, which is the product of winding area and the core area can be obtained by using the above parameters in the equation (A.1). Thus, just by finding the area product value of the cores, many of the cores can be filtered out.
Even though a core having the minimum energy product requirement is found, it will be not sure whether the required inductance can be obtained from that core because the core will not have enough space to wound the coil of a high number of turns required for designing the required inductor value. In that case, a similar core of higher dimensions needs to be checked again for the feasibility of the inductor.
Ungapped cores requires higher flux densities, which will be costly and hence are not considered. Planar cores and other smaller cores are not considered since they don't have enough space for winding. Hence only pot cores, RM cores and other variants of E cores are considered. Inductor cores which satisfy the energy product are considered and are sorted with the increasing price, so as to achieve the cost effective solution. With the increasing cost, the cores sizes also increase. Thus, the sorted cores are checked one after the other to check whether the required inductance can be achieved or not as presented in the text below.

Procedure to check if the particular inductance can be built on a given core:
In order to avoid saturation of the core, air gaps must be present in the core[9]. But if air gap is too big, there will be fringing effect. To avoid fringing effect, maximum air gap, l_{gmax} that can be used is given by the equation (A.2).

$$l_{\text{gmax}} = 0.1\sqrt{A_e} \tag{A.2}$$

Where A_e is the effective cross section of the selected core.

Air gap value, l_g can be chosen such that the maximum flux density in the core will be much less than the saturation flux density of the core. An added advantage is lower the flux in the core, lower will be the core losses. Also, it must be noted that if the air gap is more, the number of turns in the coil will be more which

can be seen in the further equations given below. When the number of turns are higher, copper losses due to wire resistance is also higher. It must be noted that the copper losses reduce with load, but core losses remain same. Hence a balance between the two losses during different loading operation plays an important role in the selection of air gap. The reluctance due to the air gap is given by the equation (A.3).

$$R_g = \frac{l_g}{\mu_0 A_e} \tag{A.3}$$

Where μ_0 is the permeability of free space.

The reluctance of the core excluding air gap is given by the equation (A.4).

$$R_c = \frac{l_e}{\mu_r \mu_0 A_e} \tag{A.4}$$

Where μ_r is the relative permeability of the core material.

Thus the total reluctance of the air and the core is given by (A.5).

$$R_t = R_g + R_c \tag{A.5}$$

The number of turns, N required to obtain the required inductance is given by the formula (A.6).

$$N = \sqrt{LR_t} \tag{A.6}$$

But, the maximum number of turns, N_{max} capable of wounding on the core must be calculated whether the number of turns as obtained in the equation (A.6) is achievable or not. The maximum number of turns on a coil former is given by the equation (A.7).

$$N_{\text{max}} = \frac{A_w K_{\text{Cu}}}{A_{\text{wire}}} \tag{A.7}$$

Where A_{wire} is the cross section area of the wire used for inductor winding. For simplicity, a solid wire, instead of litz wire is considered here for the calculations. To carry a current of 9.6 A (after considering 30 % overload of the maximum current), a 16 AWG wire is considered, which has a cross section area of 1.3 sqmm.

The inductor designed according to the equation (A.6) is valid, if the number of turns is less than the maximum number of turns calculated in (A.7), else the number of turns need to be reduced. But if the number of turns is reduced, the flux density inside the inductor will increase. The flux density in the inductor is given by the formula (A.8).

$$B = \frac{N I_{\text{RMS}}}{\frac{l_e}{\mu_r \mu_0} + \frac{l_g}{\mu_0}} \tag{A.8}$$

If the number of turns, N is equal to the maximum number of turns, N_{max} and the flux density in the inductor, B is higher than the saturation limit, B_{sat}, (as a factor of safety, 90 % of the saturation value of flux density is considered) then a bigger core size needs to be considered for the next iteration. And thus the iterative procedure continues till the core which is capable of producing the required inductance is obtained.

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