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A Highly Linear Wideband Polar Class-E CMOS Digital Doherty Power Amplifier

Mohsen Hashemi, *Student Member, IEEE*, Lei Zhou, Yiyu Shen, *Student Member, IEEE*, and Leo C. N. de Vreede, *Senior Member, IEEE*

***Abstract*— This article presents the first application of a digital-intensive intrinsically linear digitally controlled class-E technique in a Doherty configuration. By careful nonlinear segmentation and multiphase RF-clocking along with overdrive-voltage control and automatic duty-cycle correction, it is shown that even the nonlinearities related to Doherty operation can be fully handled by the underlying design such that digital predistorion (DPD) can be, in principle, omitted. The nonlinearity behavior of the whole digital Doherty power amplifier (PA) is analyzed, and closed-form equations are given to predict the AM–AM and AM–phase modulation (PM) curves. In addition, time/phase mismatch between the peak and main branches and the AM and PM signals is accurately compensated. In order to achieve the maximum intrinsic linearity, two separate chips with the same architecture, but different design parameters, are fabricated as the main and peak amplifiers in 40-nm bulk CMOS. To achieve a large RF bandwidth and high passive combiner efficiency, a differential low-loss, wideband Marchand balun-based Doherty power combiner, implemented using reentrant coupled lines with independent second-harmonic control is proposed, and together with the matching network is fabricated on a two-layer PCB. The measured peak/6-dB power back-off P_{OUT}, drain efficiency/power-added efficiency at 2.4 GHz are 17.5 dBm/12.2 dBm, 57%/52% and 36%/25% with VDD main/peak = 0.6 V/0.7 V. Measured results without using DPD show −41-dBc adjacent channel power ratio (ACPR) and −36-dB error vector magnitude (EVM) for a 16-MHz OFDM signal at 2.5 GHz. By using DPD, the measured ACPR and EVM of a 16-MHz /32-MHz OFDM signals are −52 dBc/−48 dBc and −50 dB/−48 dB, respectively.**

***Index Terms*— CMOS, digital power amplifier (DPA), digital predistortion (DPD), Doherty PA, efficient, linear, multiphase RF-clocking, nonlinear sizing, overdrive-voltage control, wideband.**

I. Introduction

THE biggest challenge in designing a transmitter (TX) for wideband mobile application is to achieve high energy efficiency combined with high spectral purity. Highly efficient but not necessarily linear power amplifiers (PAs) often use switch-mode operation such as class-E, F, or D ([-1]) [1]–[7]. In order to benefit from the advances in digital CMOS process technology, it is highly desirable to push the digital/analog boundary in mixed-mode RF circuits toward the antenna interface as much as possible. A switch-mode digital-PA (DPA), implemented as an array of small sub-PA cells, is therefore a logical candidate for such a transmitter, as it can be directly driven by digital (i.e., square-wave) signals [8]–[18].

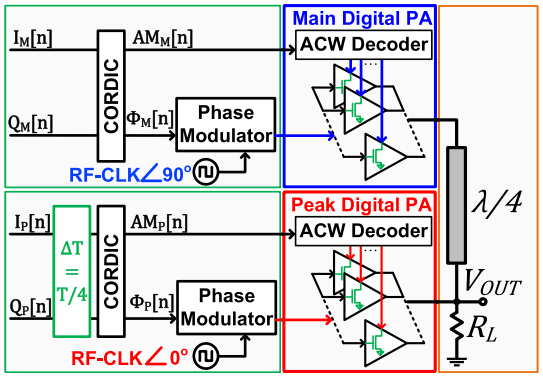

Fig. 1. Digital-intensive polar TX with digital Doherty PA.

In a digital-intensive polar TX, as shown in Fig. 1, the input complex I/Q data are converted to amplitude $AM[n] = ((I[n]^2 + Q[n]^2))^{1/2}$ and phase $\phi[n] = \text{Arctan}(Q[n]/I[n])$. The conversion from the Cartesian domain to polar is a highly nonlinear operation, which can limit the maximum signal bandwidth in practical implementations. However, since there is only one RF path per PA in a polar TX, the efficiency is normally higher than its Cartesian counterpart. On the other hand, high data-rate signals normally have a high peak-to-average-power ratio (PAPR), which compels a PA to operate in deep power backoff (PBO), thus reducing its power efficiency if no efficiency enhancement technique is applied. Among different efficiency enhancement techniques such as envelope-tracking [19], [20] and Doherty [7], [21]–[31], Doherty PA [21] is still one of the most widely used efficiency enhancement techniques, because of its relatively simple and low-cost implementation. Using an off-chip matching network reduces the passives losses, thus increasing the efficiency, especially at PBO compared to implementations with on-chip matching network [27]–[29].

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M. Hashemi is with the Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands, and also with the ItoM Company, 5624 CL Eindhoven, The Netherlands (e-mail: m.hashemi@tudelft.nl).

L. Zhou is with the Ampleon Company, 6534 AV Nijmegen, The Netherlands.

Y. Shen and L. C. N. de Vreede are with the Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands.

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Conventional TX design approaches are often based on using a nonlinear PA to achieve high efficiency and then linearize it by applying digital predistortion (DPD) techniques [7], [21]–[24], [26], [28], [29], [31]. Furthermore, as will be discussed in Section IV, even with an ideal DPD, due to the highly nonlinear operation mode of class-E DPAs, it is not possible to achieve maximum spectral purity and minimum error vector magnitude (EVM) for a given number of bits with a conventional uniform DPA structure [32]. The bandwidth of the digital AM signal is mostly limited by the sampling rate and not by analog blocks as in an analog-intensive polar TX [33], [34]; thus, it can handle a higher signal bandwidth [9]–[12], [16]–[18], [29], [30].

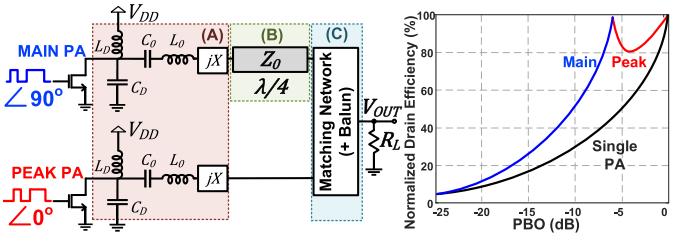
In addition to high video bandwidth, high RF bandwidth is also of great importance. There are three main challenges in increasing the RF bandwidth of a class-E Doherty PA, namely, class-E PA limited bandwidth, impedance converter limited bandwidth, and the balun limited bandwidth, which can be mitigated using three different techniques, namely, reactance compensation [35], a shunt open-circuit $\lambda/8$ section [26], [31], [36] parallel to the load, and compensated Marchand balun with reentrant coupled lines [18], [37]–[39], respectively.

In this article, for the first time, a linear digital-intensive polar class-E Doherty PA is demonstrated, in which the linearity is significantly enhanced using circuit-level linearization techniques with automatic duty-cycle correction (DCC). Wideband efficiency enhancement is achieved by using reactance-compensated parallel-circuit class-E along with wideband impedance inverter and a novel wideband Marchand balun-based Doherty power combiner, implemented using reentrant coupled lines with independent second-harmonic control. Nonlinear sizing, multiphase RF-clocking, and overdrive-voltage control have been recently successfully used to linearize single PAs with both on-chip [16], [17] and off-chip [18] matching networks in circuit-level without using DPD.

In the following, a wideband class-E Doherty PA and a digital Doherty PA are discussed in Sections II and III, respectively. System-level design considerations are discussed in Section IV, and the circuit-level linearization techniques are described in Section V. The final design and implementation are explained in Section VI, followed by the measurement results and conclusion in Sections VII and VIII, respectively.

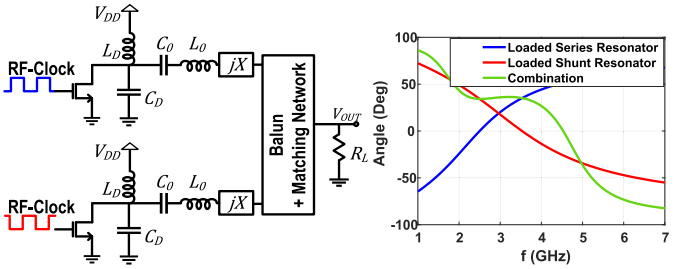
II. Wideband Class-E Doherty PA

In a symmetric Doherty PA, as shown in Fig. 2(a), there are the main (or carrier) and peak (or auxiliary) PAs, where the peak PA is only active beyond the 6-dB PBO point resulting in an additional peak in the efficiency, as shown in Fig. 2(b). The output powers are combined using an impedance inverter. To maintain linearity, efficiency is typically compromised at the high-efficiency power backoff point to ease DPD [7], [21]–[24], [26]–[28], [31]. To achieve higher efficiency, switch-mode PAs can also be considered to be used as branch amplifiers. Among the switch-mode PAs, the class-E has one of the simplest load networks and can theoretically provide



(a) (b)

Fig. 2. (a) Simplified single-ended structure of a class-E Doherty PA with TL-based impedance inverter, highlighting three different bandwidth limiting factors in the circuit. (b) Normalized DE versus output power backoff.



(a) (b)

Fig. 3. (a) Single push–pull class-E PA. (b) Angle of the impedance seen by drain.

up to 100% drain efficiency (DE) while absorbing the drain capacitance in its load network [1], [2], [5]–[7]. In this section, different techniques to mitigate the bandwidth liming factors, as highlighted in Fig. 2(a), are described.

A. Reactance Compensated Parallel-Circuit Class-E PA

The general topology of a push–pull class-E PA with finite dc feed inductance is shown in Fig. 3(a). The normalized resonance frequency of the parallel resonator is defined as $q_D = 1/(\omega_0(L_D C_D)^{1/2})$. It has been shown that for $q_D = 1.412$, the output power for a given V_{DD} and R_L is maximum, and the series reactance X can be zero [35], [40], [41]. Such a structure, known as parallel-circuit class-E, has higher maximum operating frequency and higher load resistance [41]. To have a wideband RF operation, the load angle seen by the intrinsic drain should remain constant over the required bandwidth. This can be done through reactance compensation [35], [40]. By properly choosing the parameters of the series resonator, a constant load angle, as shown in Fig. 3(b), over a wide frequency band can be achieved, resulting in the optimum $Q_{\text{series}} = 1.026$ [40]. However, in an ideal class-E PA, high Q_{series} is required to block all the harmonics in the series resonator; otherwise, the efficiency drops. By using a push–pull configuration with differential matching network, the orthogonality between odd and even terminations can be used to ensure a very high even mode (second harmonic) impedance, and as such relax the Q_{series} requirement of the series resonator, achieving wideband operation without compromising the class-E efficiency.

B. Compensated Impedance Inverter

Doherty implementations normally use a quarter-wave transmission line (QWTL) or its lumped equivalent as the

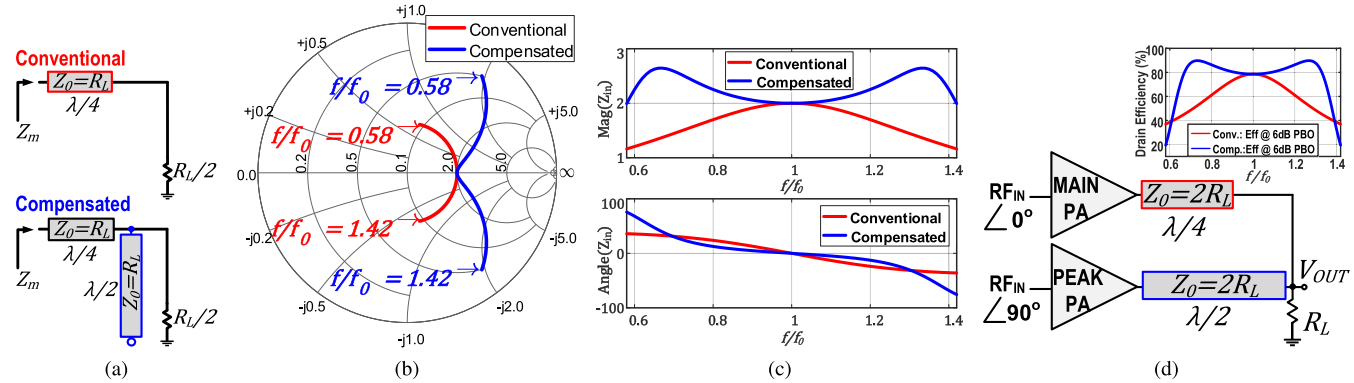


Fig. 4. (a) Conventional and compensated impedance inverter. (b) Smith chart showing the input impedances at 6-dB PBO. (c) Normalized magnitude and angle of the input impedances at 6-dB PBO versus normalized frequency. (d) Doherty PA with compensated impedance inverter and the ideal class-B 6-dB PBO DE curves versus frequency.

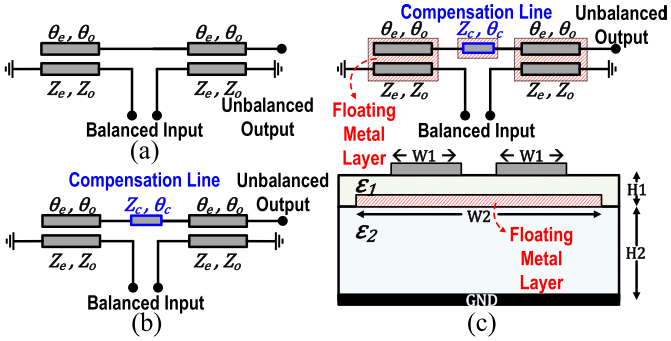


Fig. 5. (a) Marchand balun. (b) Compensated Marchand balun. (c) Compensated Marchand balun with reentrant coupled lines.

impedance inverter [Fig. 4(a)] [7], [21]–[24], [27]–[30]. As can be seen from Fig. 4(b)–(c), the magnitude and phase of the impedance Z_m seen by the main PA are highly sensitive to frequency. By adding an open-circuit compensation half-wave TL (HWTL) in parallel to the load [26], [31], [36], as shown in Fig. 4(a), the input impedance is given by

$$Z_m(f)=\frac{R_L Z_0\left(1-\tan\left(\pi\frac{f}{f_0}\right)\tan\left(\frac{\pi}{2}\frac{f}{f_0}\right)\right)+jZ_0^2\tan\left(\frac{\pi}{2}\frac{f}{f_0}\right)}{Z_0+jR_L\left(\tan\left(\pi\frac{f}{f_0}\right)+\tan\left(\frac{\pi}{2}\frac{f}{f_0}\right)\right)} \tag{1}$$

which shows smaller variations of the magnitude and phase of Z_m over a larger bandwidth. This structure can be employed in Doherty configuration as depicted in Fig. 4(d) to expand the efficiency bandwidth.

C. Compensated Marchand Balun With Reentrant Coupled Lines and Second-Harmonic Control

1) Compensated Marchand Balun: The planar Marchand balun, shown in Fig. 5(a), is one of the best TL-based topologies for offering wideband amplitude and phase balance while having a relatively simple implementation [39], [42]. A conventional Marchand balun is constructed from two $\lambda/4$ coupled lines with short and open terminations at their specific ports, ideally providing a balanced loading condition from a single-ended load. However, in practice, due to the unequal even-mode and odd-mode phase velocities, the conversion from single-ended to balanced operation is not perfect and results some imbalance. To correct for this imbalance, a compensation technique [42] can be adopted, where an extra compensation line section is added between the two $\lambda/4$ coupled line sections [Fig. 5(b)] whose parameters can be calculated as follows:

$$Z_{\rm cm}\cot\left(\frac{\theta_{\rm cm}}{2}\right)=\frac{Z_{0o}\csc\theta_e-Z_{0e}\csc\theta_o}{\csc\theta_e\cot\theta_o-\csc\theta_o\cot\theta_e} \tag{2}$$

where Z_o and Z_e are the characteristic impedance and θ_o and θ_e are the electrical length of odd-mode and even-mode, respectively. $Z_{\rm cm}$ and $\theta_{\rm cm}$ are the characteristic impedance and the electrical length of the compensation section, respectively.

2) Reentrant Coupled Lines: The bandwidth of a Marchand balun at low (odd-mode) impedance levels depends on the Z_{0e}/Z_{0o} ratio. This can be very challenging in practice with single-layer transmission lines, as a very small horizontal gap between the coupled lines is required. However, reentrant coupled lines, as shown in Fig. 5(c), can achieve a very tight coupling without strict requirements in fabrication [39]. In the odd-mode, $Z_{0o}=Z_{0,1}$, where $Z_{0,1}$ is the impedance between transmission lines and floating layer. In the even-mode, $Z_{0e}=Z_{0,1}+2Z_{0,2}$ where $Z_{0,2}$ is the impedance between the floating layer and the bottom plate. In this case, the coupling factor $K=(Z_{0e}-Z_{0o})/(Z_{0e}+Z_{0o})=1/(1+Z_{0,1}/Z_{0,2})$ mostly depends on the $Z_{0,1}/Z_{0,2}$ ratio rather than the horizontal spacing between the coupled lines, thus relaxing the dimensional requirements in fabrication. In general, a low $Z_{0,1}/Z_{0,2}$ ratio is preferred. Therefore, having an upper layer with a larger dielectric constant but a smaller thickness compared to the lower layer ($\epsilon_{r1}>\epsilon_{r2}$ and $H_1<H_2$), a strong coupling coefficient can be expected, resulting in a low-loss and wideband balun. Furthermore, since the effective dielectric constants of even and odd modes are different, the wavelength $\lambda=\lambda_{\rm air}/(\epsilon_{\rm reff})^{1/2}$ of these modes, namely, $\lambda_{\rm even}$ and $\lambda_{\rm odd}$, are also different.

3) Second-Harmonic Control: In a differential PA, the even harmonics are seen open-circuit at the input of the balun. However, the use of a QWTL impedance transformer at the

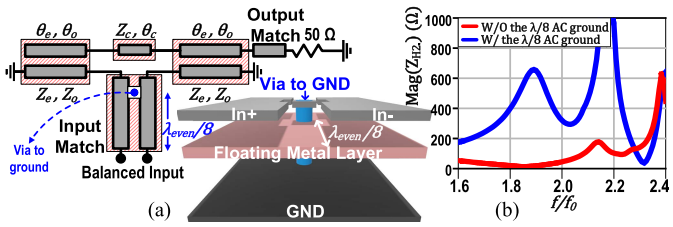


Fig. 6. (a) AC grounding at $\lambda_{\text{even}}/8$ for second-harmonic control, using a via from the floating metal layer to the ground plane, shown for a single PA. (b) EM simulation results of the input impedance at second harmonic, shown for a single PA.

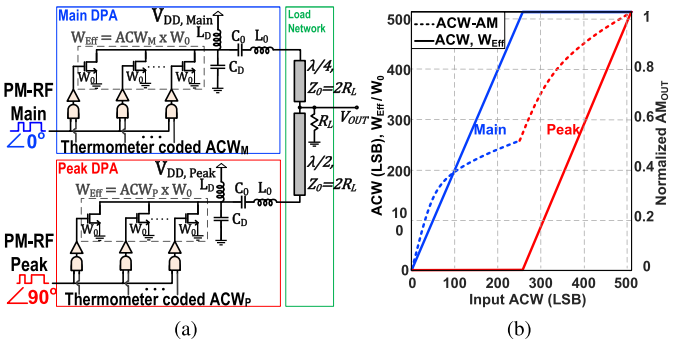


Fig. 7. (a) Simplified linearly sized single-ended class-E digital Doherty PA with compensated impedance inverter. (b) ACW and effective width of each branch versus the input ACW.

input can provide very low impedance levels for the even harmonics at the PA reference plane, which conflicts the loading conditions of class-E PA operation. To address this issue, the center of the floating metal layer in the re-entrant $\lambda/4$ sections is connected to the ground by a via at $\lambda_{\text{even}}/8$ distance from the PA, as depicted in Fig. 6(a). Therefore, thanks to the tight coupling between the top and floating metal layers, the TL is ac-ground in even-mode, thus seen as open-circuit by the PA at second harmonic, as shown by electromagnetic (EM) simulation in Fig. 6(b). In the odd-mode, the center of the floating metal is virtually ground thus barely affecting the odd-mode impedance levels.

III. Digitally Controlled Class-E Doherty PA

In an RFDAC-based class-E digital Doherty PA, the output amplitude is directly modulated by changing the effective width or R_{ON} of the final PA stage, as shown in Fig. 7(a) for a 10-bit Doherty DPA with two 9-bit DPAs. The input amplitude-control word (ACW) varies between 0 and $\text{ACW}_{\text{Max}} = 1022$, and the ACW of the main (ACW_M) and peak DPA (ACW_P) both have a range of 0–$\text{ACW}_{\text{MP,Max}} = 511$. For $\text{ACW} \leq \text{ACW}_{\text{MP,Max}}$, we have $\text{ACW}_M = \text{ACW}$ and $\text{ACW}_P = 0$. For $\text{ACW} > \text{ACW}_{\text{MP,Max}}$, as shown in Fig. 7(b), the main DPA is fully on ($\text{ACW}_M = \text{ACW}_{\text{MP,Max}}$) and the peak DPA starts turning on ($\text{ACW}_P = \text{ACW} - \text{ACW}_{\text{MP,Max}}$).

The total drain capacitance (C_D, including the transistors and interconnect parasitics) is tuned for class-E operation at $\text{ACW}_M(\text{ACW}_P) = \text{ACW}_{\text{MP,Max}}$. Therefore, when the main (peak) DPA is fully on, it operates in class-E. As the number of switching transistors in the main (peak) DPA decreases (at PBO), the fundamental impedances become complex with positive reactances, and the second-harmonic impedances become mostly negative reactances (capacitive) thus operating similar to a class-J PA [43]–[45]. For small $\text{ACW}_M(\text{ACW}_P)$ (<30), the voltage swing on drain of the main (peak) DPA is small, therefore operating similar to a current source with an almost linear behavior [17]. The C_D change is rather small since all the devices in the output stage are in parallel all the time. Therefore, only their gate potential is changing, which affects C_D to a little extend (varying 110 fF in total from ACW = 1 to ACW = 511 for each DPA, equivalent to less than 3% change). Consequently, the variations of C_D for $\text{ACW}_M(\text{ACW}_P) > 30$ does not change the intended class-E operation significantly. However, the efficiency drops due to the increased R_{ON}.

Using an analysis approach similar to [17], the single-ended Norton equivalent linear time-invariant (LTI) model of the DPAs in odd-mode is shown in Fig. 8(a)–(d). Since the HWTL section of the compensated impedance inverter does not alter the impedances seen by the main and peak PAs at center frequency f_C (except for a phase-offset); therefore, the conventional QWTL is used for theoretical simplicity. The switching transistors are replaced by a series of paralleled current sources representing the harmonics of the drain current.

For theoretical simplicity, the amplitude of the fundamental is assumed to be proportional to the total effective (switched-on) width. The output resistance is modeled in parallel to the current sources and inversely proportional to the total effective width. Ideally, the series resonator only allows the fundamental component I_{H1} to pass through. Therefore, by neglecting the higher harmonics and using the superposition theory, the output signal equals $V_{\text{OUT}} = V_{\text{OUT},M} + V_{\text{OUT},P}$ where $V_{\text{OUT},M}$ and $V_{\text{OUT},P}$ are the contributions of the main and peak DPAs to the output signal, given in (3) and (4) at the bottom of this page. R_L is the load resistance seen from the matching network, $R_{D,0}$ is the output resistance of a unit transistor with W_0 width, and K_M and K_P are the ratio of total width of the activated sub-PA cells of the main and peak DPAs to the unit transistor, respectively. L_D is dc-feed inductance (implemented by wirebonds in this work), and ω_0 is the radian center frequency. Since the variation of the transistors total output capacitance is small (<3%),

$$V_{\text{OUT},M} = \frac{K_M I_{H1}}{K_M/R_{D0} + j\left(1-q_D^2\right)/\left(q_D^2 L_D \omega_0\right) + jL_D\omega_0/\left(4R_L^2 - 4R_L/q_D^2 + j4R_L L_D \omega_0 (1 + K_P R_L/R_{D0})\right)} \tag{3}$$

$$V_{\text{OUT},P} = \frac{K_P I_{H1}}{K_P/R_{D0} + j\left(1-q_D^2\right)/\left(q_D^2 L_D \omega_0\right) + 1/R_L + jL_D\omega_0/\left(4R_L^2 - 4R_L/q_D^2 + j4R_L^2 L_D \omega_0 K_M/R_{D0}\right)} \tag{4}$$

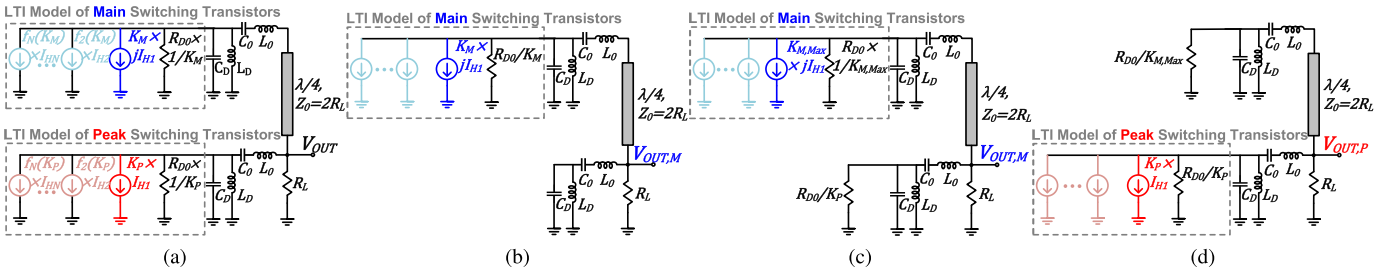


Fig. 8. Simplified single-ended Norton equivalent LTI model of (a) digital Doherty PA, (b) main DPA for ACW $<$ $\mathrm{ACW}_{\mathrm{MP,Max}}$, (c) main DPA for ACW $>$ $\mathrm{ACW}_{\mathrm{MP,Max}}$, and (d) the peak DPA for ACW $>$ $\mathrm{ACW}_{\mathrm{MP,Max}}$.

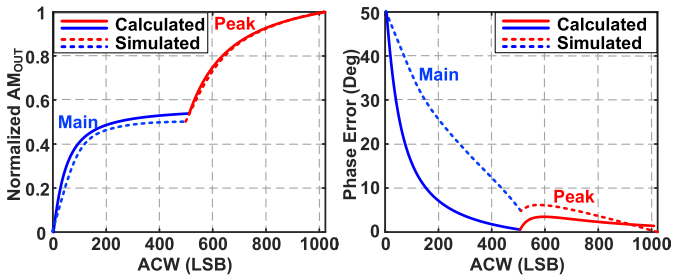


Fig. 9. Calculated and simulated ACW-AM and ACW-PM curves.

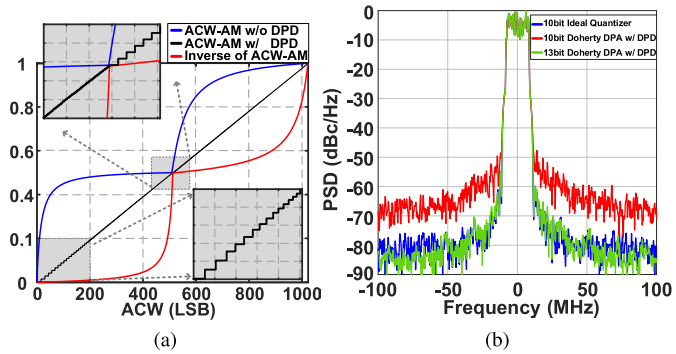


Fig. 10. (a) ACW-AM curve of a 10-bit Doherty DPA with and without an ideal DPD, the inverse of ACW-AM curve. (b) Effect of 10-bit nonuniform quantizer on the output spectrum, compared with an ideal 10-bit quantizer and 13-bit nonuniform quantizer.

we consider C_D as constant. Therefore, the ACW-AM and ACW-phase modulation (PM) functions can be easily calculated as $AM_{\mathrm{OUT}} = (V_{OUT,Re}^2 + V_{OUT,Im}^2)^{1/2}$ and $\phi_{\mathrm{OUT}} = \arctan(V_{OUT,Im}/V_{OUT,Re})$. In contrast to the output phase, the normalized output amplitude is not a strong function of q_D, therefore by assuming $q_D = 1$ for theoretical simplicity, the output amplitude can be calculated as follows:

$$\begin{aligned} AM_{\mathrm{OUT}} &\approx R_{D0} I_{H1} \\ &\quad \times \left(\frac{K_M}{K_M + \frac{R_{D0}^2}{4K_P R_L^2 + 4R_L R_{D0}}} + \frac{K_P}{K_P + \frac{R_{D0}}{R_L} + \frac{R_{D0}^2}{4K_M R_L^2}} \right) \\ &= R_{D0} I_{H1} \times \frac{2K_M K_P R_L^2 + K_M R_L R_{D0}}{K_M K_P R_L^2 + K_M R_L R_{D0} + R_{D0}^2/4}. \end{aligned} \tag{5}$$

By assuming K_M, $K_P \gg R_{D0}/R_L$, the normalized ACW-AM can be approximated by

$$AM_{\mathrm{Norm}}(K_M, K_P) \approx \frac{4K_M K_P K_{\mathrm{NL}}^2 + 2K_M K_{\mathrm{NL}}}{4K_M K_P K_{\mathrm{NL}}^2 + 4K_M K_{\mathrm{NL}} + 1} \tag{6}$$

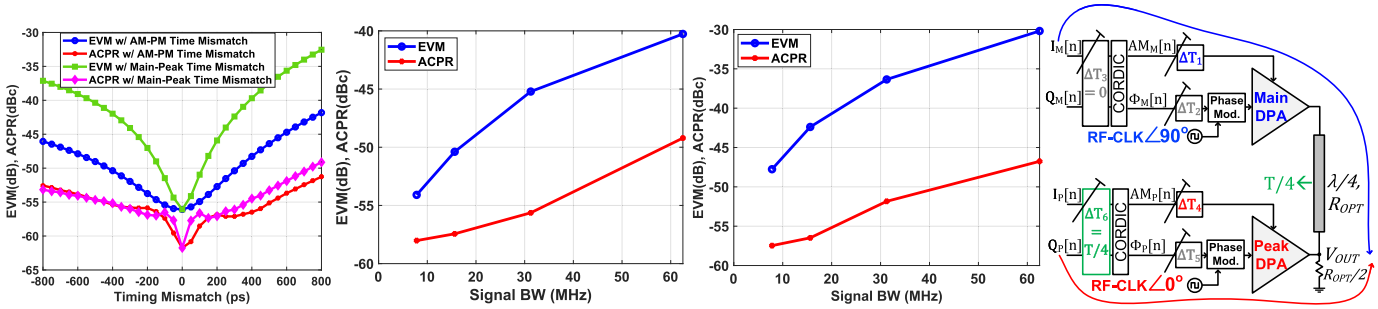
where $K_{\mathrm{NL}} = R_L/R_{D0}$ is defined as the nonlinearity factor. In a linearly sized array, for ACW $\leq$ $\mathrm{ACW}_{\mathrm{MP,Max}}$, $K_M =$ ACW, and $K_P = 0$; otherwise, $K_M = \mathrm{ACW}_{\mathrm{MP,Max}}$ and $K_P =$ ACW$-\mathrm{ACW}_{\mathrm{MP,Max}}$. The calculated ACW-AM/PM curves and the full-circuit (differential class-E DPA with real transistor model and TL-based Merchand balun) simulation results are plotted in Fig. 9, showing a reasonable (ACW-PM) to good agreement (ACW-AM) between the proposed model and the real circuit simulation results. As can be seen, although a switch-mode (class-E) DPA is a nonlinear time-variant circuit, the proposed LTI model provides good insight in predicting the nonlinearity behavior of the Doherty DPA for the fundamental band.

IV. System-Level Design Consideration

As explained in Section III, a Doherty DPA with conventional uniform array and single-phase RF-clocking is highly nonlinear as characterized by its static ACW-AM and ACW-PM curves. Such nonlinearities are typically corrected using DPD, which can lead to nonuniform quantization effect [17], [32]. In addition, in a polar PA, since the AM and PM signal paths are different from each other, they will have different time delays, thus requiring delay adjustments before reaching the final stage of the DPA. Furthermore, in a Doherty configuration, the paths of main and peak PAs are also different from each other, thus requiring timing alignment between these two branches. In the following, these system-level design considerations are explained in more detail.

A. Nonuniform Quantization

Although DPD is very common for linearizing a nonlinear PA, the cascaded combination of DPD and an N-bit DPA with a highly nonlinear ACW-AM curve constructs a nonuniform quantizer. Such a nonuniform quantizer cannot achieve the dynamic range (DR) and linearity levels as expected from an ideal N-bit quantizer (i.e., the DPA). In Fig. 10, the ACW-AM curve of a 10-bit Doherty DPA with and without an ideal DPD, the inverse of ACW-AM curve, the probability distribution



(a) (b) 300 ps AM-PM timing mismtach (c) 300 ps Main-Peak timing mismtach (d)

Fig. 11. (a) EVM and ACPR of a 16-MHz OFDM signal versus AM–PM/main-peak timing mismatch. (b) EVM and ACPR with 300-ps AM–PM timing mismatch versus signal bandwidth. (c) EVM and ACPR with 300-ps main-peak timing mismatch versus signal bandwidth. (d) Block diagram of AM–PM and main-peak timing mismatch correction in a digital polar TX with Doherty DPA.

function (PDF) of atypical quadratic-amplitude modulation (QAM) signal, and the zoomed-in view around the transition point where the peak DPA starts operating are plotted. As can be seen, the quantization levels at small ACWs for both the main and peak DPAs are much higher than at larger ACWs. This is due to the fact that the slope of the nonlinearized ACW-AM curve significantly decreases as the ACW increases. The PDF of a QAM signal has its peak around the transition point, where the slope suddenly increases as the peak DPA turns on. Therefore, the rms power of the quantization noise varies dynamically with variation of the signal's amplitude, leading to degradation of output spectral purity. In Fig. 10(b), the effect of this phenomena on the output spectrum is shown and compared with an ideal 10-bit quantizer, and a nonlinear 13-bit DPA after ideal DPD. Therefore, compensating for such nonidealities, requires about 2–3 extra bits in the DPA and the whole preceding digital processing blocks, increasing the complexity, area, and power consumption.

B. AM–PM Timing Mismatch

The AM and PM signals in a polar TX are separated from each other. After the CORDIC block at the input, the baseband digital AM signal can be directly applied to the DPA array, while the digital baseband phase data are first upconverted to the RF carrier signal by a phase modulator, thus becoming a passband signal, and then applied to the DPA cells. Consequently, these two signals pass through totally different channels with different timing delays. Because of the bandwidth expansion of the AM and PM signals, any timing mismatch will significantly degrade the adjacent channel power ratio (ACPR) and EVM. Increasing the input signal bandwidth makes it even more challenging to achieve a good linearity since it directly increases the impact of time alignment errors, as shown in Fig. 11(a) and (b). For example, for a signal bandwidth of 32 MHz, the timing mismatch should be less than 100 ps to have enough margin for ACPR <-50 dBc and EVM <-45dB after linearization. Therefore, as shown in Fig. 11(d) for a single DPA, tunable delay cells should be used in the AM/PM signal paths to correct for the timing mismatch between them.

C. Main-Peak Timing Mismatch

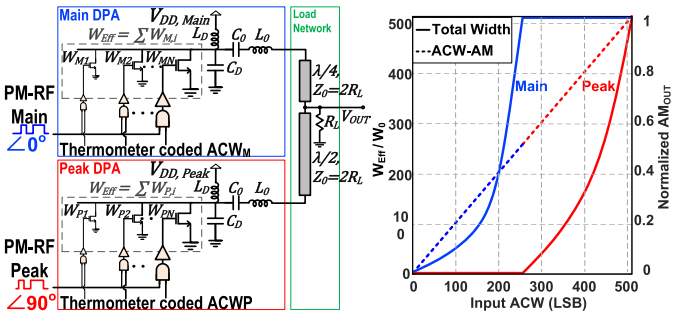
In a Doherty PA, the output signals of the main and peak DPA pass through transmission lines with different lengths, thus seeing different delays, which can degrade the ACPR and EVM significantly. The simulated effect of such a timing mismatch on ACPR and EVM is shown in Fig. 11(a) and (c). In a typical analog Doherty PA shown in Fig. 2(a), the output of the main PA passes through a QWTL, while at the input, the input of the peak PA passes through a QWTL. Therefore, the overall input–output signals of the main and peak DPA are automatically self-aligned and there is ideally no timing mismatch between them (note that in practical implementations, the different impedance terminations of the lines can strongly degrade this property). However, in a digital Doherty PA as shown in Fig. 11(d), while the phase of the carrier signals is corrected by applying a 90° phase-offset, the output signals are not automatically self-aligned. Therefore, this delay difference should be compensated accurately, which can be done in the digital domain. Furthermore, it is interesting to see in Fig. 11(a) that for an OFDM signal, EVM and ACPR are more sensitive to main–peak timing mismatch than AM–PM timing mismatch.

V. Circuit-Level Linearization

As explained in IV-A, a digital Doherty PA is, in fact, so nonlinear that even with an ideal DPD, the nonlinearity lowers the effective number of bits, thus reducing the DR of the output signal [32]. In this work, the DPAs are made intrinsically linear by using three different circuit-level techniques: nonlinear sizing and overdrive-voltage control for ACW-AM correction, and multiphase RF-clocking for ACW-PM correction [16]–[18]. Therefore, not only the burden on DPD for strict cellular wireless standards is reduced but also the ACW-AM and ACW-PM distortions are corrected well enough to pass the WiFi mask even without using DPD. In the following, these techniques are described in detail.

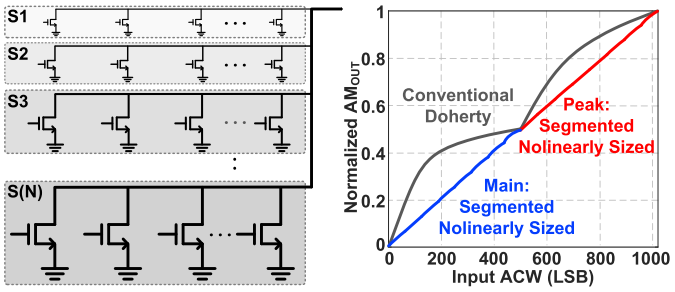
A. ACW-AM Correction

In a conventional DPA, as shown in Fig. 7(a), the sub-PA cells in the array are sized linearly, meaning that as the input ACW increases, the effective width of the total active cells (W_{Eff}) increases linearly. Linear sizing can result in substantial ACW-AM distortion as shown in Fig. 7(b). Assuming a width of W_0 for a unit cell, the effective width of the array is ACW $\cdot$ W_0. In this work, as shown in Fig. 12(a), in order to linearize the ACW-AM conversion, the sub-PA cells in both



(a) (b)

Fig. 12. (a) Concept of nonlinear sizing to its full extend in a digital Doherty PA. (b) Total width of the main and peak DPA versus ACW and the resulting linear ACW-AM curve.



(a) (b)

Fig. 13. (a) Concept of segmented nonlinear sizing shown for a single DPA. (b) Resulting ACW-AM curve for a Doherty DPA with eight segments in each main/peak DPAs.

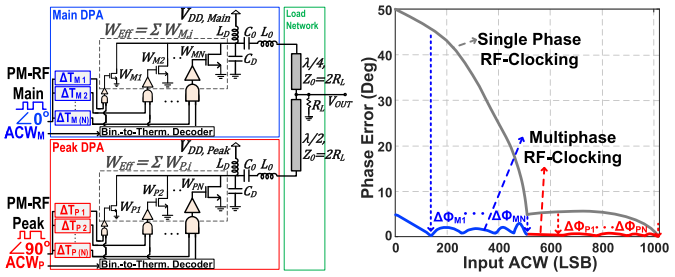


Fig. 14. Concept of multiphase RF-clocking for ACW-PM correction shown for a nonlinearly sized Doherty DPA.

of the main and peak are sized nonlinearly, meaning that as the ACW increases, the effective size of the total active cells increases nonlinearly. Assuming an N-bit fully thermometer-coded array comprising $2^N - 1$ cells, the transistors corresponding to small ACWs are sized smaller than W_0, and the transistors corresponding to large ACWs are sized larger than W_0. This yields a linear ACW-AM conversion, as shown in Fig. 12(b). By calculating the inverse function of (6) for main and peak DPA, and then scaling its maximum to the same total width of $\mathrm{ACW}_{\mathrm{MP,Max}} \cdot W_0$, the widths of the main DPA transistors corresponding to each ACW_M are initially calculated by

$$W_{\mathrm{Eff},M,\mathrm{NL}}[\mathrm{ACW}] = \frac{\mathrm{ACW_M}.\mathrm{W_0}}{1 + 4\mathrm{K_{NL}}(\mathrm{ACW_{MP,Max}} - \mathrm{ACW_M})}. \tag{7}$$

The widths of the peak DPA transistors corresponding to each ACW_P are given in (8), shown at the bottom of this page, where F_{WP} is given in (9), shown at the bottom of this page.

Due to the impact of other nonidealities, it is more practical to extract W_{Eff} by actually simulating the ACW-AM curve of a linearly sized DPA, then calculating the inverse curve and scaling its maximum to $\mathrm{ACW}_{\mathrm{MP,Max}}.W_0$. Using (7), the width of each transistor corresponding to each ACW is calculated by $W_{\mathrm{Eff,NL}}[\mathrm{ACW}] - \mathrm{W}_{\mathrm{Eff,NL}}[\mathrm{ACW} - 1]$. Obviously, for a nonlinearly sized N-bit DPA, this results in $2^N - 1$ different transistors sizes, requiring fully thermometer coding, which results in high power consumption in the drivers stages. Therefore, in order to benefit from the well-known binary-unary segmentation [46] to reduce the array complexity and power consumption, segmented nonlinear sizing is used in this work. In a segmented nonlinearly sized DPA, as shown in Fig. 13(a), the array is divided into N segments with the same ACW range but different total sizes. Although the effective size of the active cells inside each segment increases linearly, the overall effective size of the total active cells increases nonlinearly such that the resulting $W_{\mathrm{Eff}}[\mathrm{ACW}]$ curve is a piecewise linear version of the original fully nonlinearly sized $W_{\mathrm{Eff}}[\mathrm{ACW}]$ curve. Since the cells inside each segment are sized linearly, it is possible to apply binary-unary segmentation to reduce the power consumption by the drivers. By increasing the number of the segments, the overall linearity improves. It has been shown in [17] that eight segments are enough to lower the ACPR and EVM to an acceptable level with enough margin for other sources of nonlinearities. The simulated ACW-AM curve of segmented nonlinearly sized Doherty DPA with eight segments in each main/peak DPAs is plotted in Fig. 13(b), showing significant improvement in ACW-AM linearity over a Doherty DPA using uniformly sized arrays.

As can be seen from (7) and (8) for a nonlinearly sized array, the optimum sizes of the sub-PA cells depend on the nonlinearity factor $K_{\mathrm{NL}} = R_L/R_{D0}$. However, after fabrication or during the operation of the chip, the load or frequency may change, which will change R_L. In addition, the process/voltage/temperature variations will change R_{D0}, thus changing K_{NL} from its desired design value. Consequently, the resulting ACW-AM curve will somewhat deviate from its optimum linearity in a practical implementation. To correct for this,

$$W_{\mathrm{Eff},P,\mathrm{NL}}[\mathrm{ACW}] = W_0 \frac{F_{\mathrm{WP}}\mathrm{ACW_{MP,Max}}K_{\mathrm{NL}} + F_{\mathrm{WP}}/4 - \mathrm{ACW_{MP,Max}}K_{\mathrm{NL}}/2}{\mathrm{ACW_{MP,Max}}K_{\mathrm{NL}}^2 - F_{\mathrm{WP}}K_{\mathrm{NL}}^2\mathrm{ACW_{MP,Max}}} \tag{8}$$

$$F_{\mathrm{WP}} = \mathrm{ACW}_P \frac{\mathrm{AM_{Norm}}(\mathrm{ACW_{MP,Max}}, \mathrm{ACW_{MP,Max}}) - \mathrm{AM_{Norm}}(\mathrm{ACW_{MP,Max}}, 0)}{\mathrm{ACW_{MP,Max}}} + \mathrm{AM_{Norm}}(\mathrm{ACW_{MP,Max}}, 0) \tag{9}$$

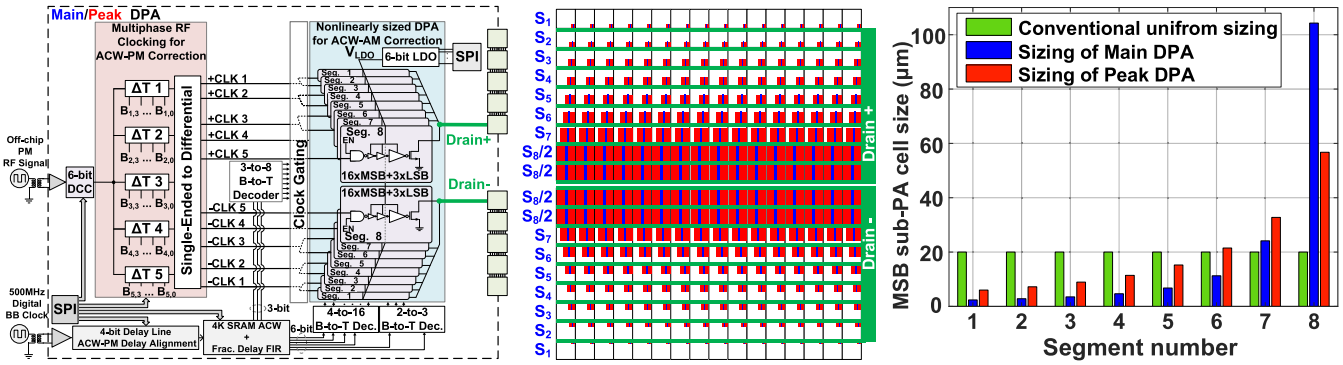


Fig. 15. (a) Overall structure of main/peak DPA. (b) Conceptual layout of the nonlinearly sized array where only the output MSB transistors are shown. (c) Realized sizing of the MSB sub-PA cells of the main and peak DPA compared to a conventional uniform array with the same total size.

we can tune K_{NL} by tuning the ON-resistance of the transistors. Since $R_{D0} = (W_0/L \times K_n \times V_{\mathrm{OD}})^{-1}$ [47], we can tune K_{NL} by controlling the overdrive-voltage V_{OD}. To facilitate this, the VDD of the buffers that drive the output transistors is tuned. Therefore, the peak voltage of the RF clock changes, changing the overdrive-voltage $V_{\mathrm{OD}} = V_{GS} - V_{TH}$, consequently, the ACW-AM curve can be linearized back to its desired level. The details of the circuit-level implementation will be described in Section VI.

B. ACW-PM Correction

In a conventional DPA with single-phase RF-clocking, all of the sub-PA cells are driven by the same (modulated) RF clock. In energy-efficient class-E like DPAs that reliy on reactive loading, the variation of the ON-resistance of the transistor with ACW variations yields significant ACW-PM distortion as shown in Fig. 9(b). To correct for this, a concurrent multi-phase RF-clocking technique is used to reduce the ACW-PM conversion. For a single DPA line-up, the resulting AM–PM curve using five multiphase RF clocks is shown in Fig. 14. In this technique, different phases of RF clocks are applied to various segments of the DPA array. The output currents of these segments are summed; thus, the overall output phase is averaged, resulting in a considerable reduction of ACW-PM distortion.

The delayed RF clocks are generated by a bank of delay lines. Since their delay can change due to PVT variations, or the ACW-PM curve itself can also change due to variations in the load or frequency, the delay lines are designed to be partly digitally programmable in order to compensate for the PVT/load/frequency variations. Once the ACW-PM is flattened, the normalized ACW-AM curve will be still almost identical to that of a single-phase nonlinearly sized DPA. Therefore, no dynamic modification is needed for each ACW, and once the delay-offsets are programmed, they are fixed during the normal operation. The required phase-offsets are roughly proportional to the phase error of each segment with respect to the output phase at maximum ACW. In practice, during the design process or chip operation, the delay-offsets can be found using an iterative algorithm as proposed in [17].

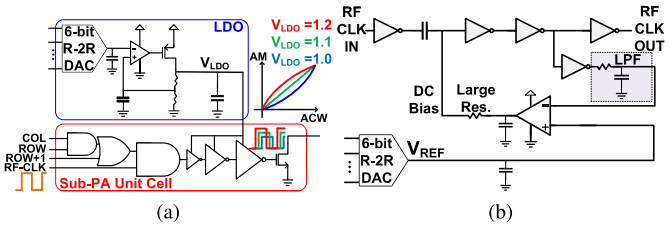
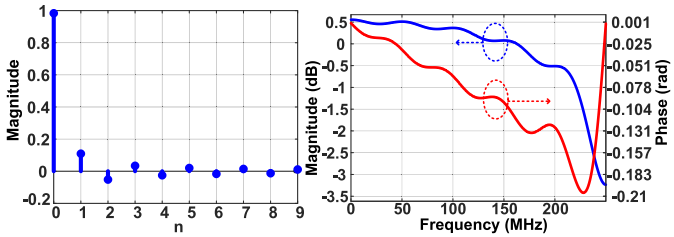


Fig. 16. (a) 6-bit programmable LDO for overdrive voltage tuning and the sub-PA unit cell circuit. (b) 6-bit programmable DCC circuit.

VI. Implementation and Fabrication

A. CMOS Chips

Since the load seen by the mean and peak DPA is not the same (except at peak power), their ACW-AM and ACW-PM curves are also different. Therefore, two chips with the same structure but different nonlinearly sized segments and delay-offsets have been designed. The overall block diagram of the chips as well as the conceptual layout of the nonlinearly sized array are shown in Fig. 15. Since the sub-PA cells of the eighth segment are very large, they are implemented in two parallel rows, each with the half size of segment 8, as shown in Fig. 15(b). The arrays of both the main and peak DPAs are 9 bit, each with a total width of 2.555 mm distributed over eight segments with different sizings as shown in Fig. 15(c). Each segment consists of 16 thermometer-coded MSB cells and three LSB cells, which are 1/16 and 1/64 the total size of each segment, respectively. In order to control the overdrive voltage, a programmable on-chip low-dropout (LDO) voltage regulator has been designed, as depicted in Fig. 16(a) [17]. The input reference voltage of the LDO is controlled by a 6-bit R-2R digital-to-analog converter (DAC), while the output voltage supplies the positive dc voltage of the buffers, which drive the output transistors. In each chip, there is only one LDO for the whole array. The LDO is capable of driving 50 mA with a resolution of 10–12 mV. The input RF-clock and BB-clock are amplified by on-chip differential amplifiers and then converted to single-ended clocks. Although the input RF-clock amplifier and the digital buffers are designed to have 50% duty-cycle, in practice, due to the PVT variations, the duty-cycle might



(a) (b)

Fig. 17. (a) Impulse response (coefficients) and (b) frequency response of the FIR-based digital fractional delay for a delay of 200 ps with a sampling rate of 500 MHz.

change, degrading the output power/efficiency or linearity. Therefore, an on-chip 6-bit programmable automatic DCC circuit, shown in Fig. 16(b), has been designed to compensate for such practical nonidealities. The DCC monitors the dc voltage of the RF-clock and compares it with a reference voltage supplied by a 6-bit R-2R DAC, then adjusts the dc voltage of the RF-clock path. Because of the voltage clipping caused by the digital buffers, changing the offset voltage of the RF-clock modifies the duty-cycle within a control range of 33%–66%. The output of the DCC is applied to the multiphase RF-clocking generator, which consists of five fine resolution single-ended delay lines. The output of the first to fifth delay-offsets is applied to the segments 1–2, 3–4, 5–6, and 7–8, respectively. The required resolution of delay-offsets is less than 6 ps, which are realized by 4-bit programmable Vernier (relative) delay lines to cover the PVT/frequency/load variations [17]. The outputs of the delay lines are converted to differential signals before being applied to the DPA array. Furthermore, clock gating is applied in the paths of the RF clocks to reduce the drivers power consumption in PBO. In order to correct for the timing mismatch between the AM and PM paths, a digital ten-tap finite-impulse response (FIR) filter is implemented on-chip as a fractional delay cell [48] in the path of the ACW data, as depicted in Fig. 15(a). The coefficients of the filter are given by $h[n] = sin[\pi(n-\Delta)]/[\pi(n-\Delta)]$, in which n is the tap index and Δ is the desired delay as a fractional of sampling time $T_S = 1/F_S$, which is the group delay of the FIR filter. For example, for a delay of 200 ps with 500 MHz, a sampling rate, the impulse response (coefficients), and frequency response of the FIR filter are plotted in Fig. 17(a) and (b). The chips are fabricated in 40-nm bulk CMOS. The core area of each DPA including the multiphase RF-clocking and LDO blocks is 0.8 mm × 0.3 mm. The die micrograph of the two chips (main and peak DPA) is shown in Fig. 18. The LDO settings, delay-offsets, and coefficients of the FIR filter are programmed via a SPI interface. The input ACW data are also loaded via the SPI interface to an on-chip 4-K sample SRAM memory. During the normal operation, the stored ACW data words are read out in a loop to be fed to the DPA array using the BB-clock.

B. Balun and Matching Network

In this work, the compensated impedance inverter is combined with Marchand balun with reentrant coupled lines to form the wideband load network of the proposed Doherty

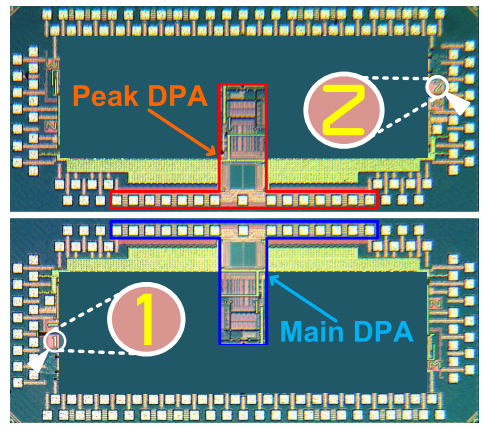


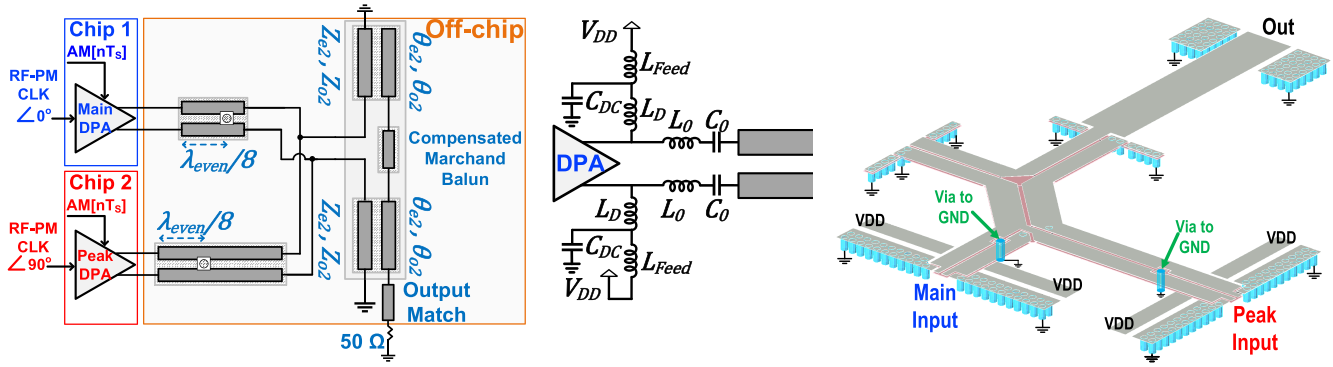
Fig. 18. Die micrograph of the main and peak DPAs.

DPA, as depicted in Fig. 19(a). The reentrant coupled lines are adopted to achieve tight coupling without violating the stringent fabrication design rules. The design parameter for the reentrant-type coupled lines is $\epsilon_{r1} = 10.2$, $H_1 = 0.13$ mm and $\epsilon_{r2} = 3.0$, $H_2 = 0.75$ mm. The width of the top layer metal lines is $W_1 = 1.5$ mm with $S = 0.2$ mm spacing, and the width of the middle metal layer is $W_2 = 3.2$ mm, resulting in $Z_{0e} = 71\Omega$ and $Z_{0o} = 7.5\Omega$ impedances for the main DPA. The even- and odd-mode wavelengths at $f_0 = 2.5$ GHz are around $\lambda_{\text{even}} = 59$ mm and $\lambda_{\text{odd}} = 36$ mm. The $\lambda_{\text{odd}}/4$ and $\lambda_{\text{odd}}/2$ reentrant coupled (differential) TL sections are placed in front of the main and peak DPA, respectively (as described in Section II-B), to make a wideband compensated impedance inverter, and also to connect them to the Marchand balun.

The Marchand balun is optimized to compensate for the nonperfect ground (via inductance) and port transitions. A $\lambda/4$ transmission line is placed after the Marchand balun to match to 50 Ω. Moreover, since it is not practically easy to make blind vias (e.g., from the middle layer to the bottom), two islands with a through via from the top metal layer to the bottom ground plate, as shown in Fig. 19(c), are placed at an optimized distance in front of the main and peak DPA to provide a second-harmonic open impedance. Due to nonideal effects, in practical situations, this distance is slightly different from $\lambda_{\text{even}}/8$. Furthermore, besides the use of the compensated $\lambda_{\text{odd}}/4$ $\lambda_{\text{odd}}/2$ Doherty power combiner, the succeeding cascaded impedance stepped TL sections further increase the bandwidth.

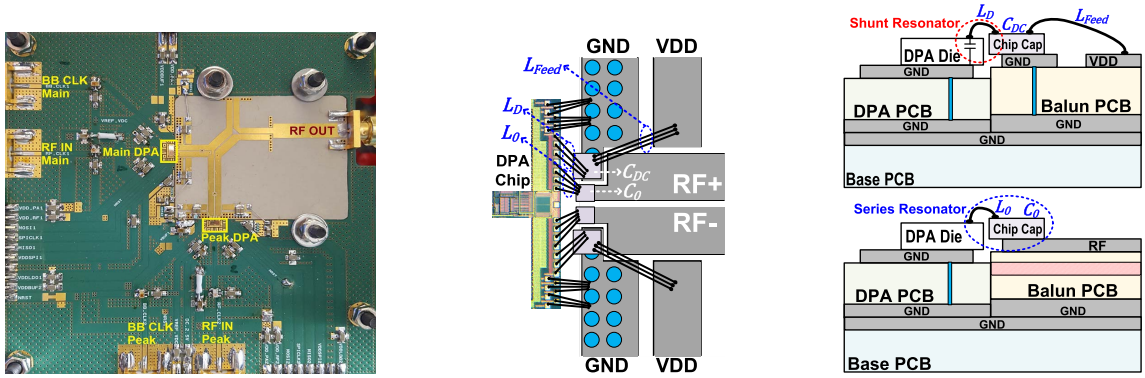
C. Overall Implementation

The main and peak chips are mounted on a FR-4 PCB, while the Marchand balun has been implemented separately on a two-layer Rogers material, as shown in Fig. 20(a). The top layer of the matching network is Rogers-3003, and the bottom layer is Rogers-3010. Both of the PCBs are mounted on a FR-4 substrate as the base. The area of the matching network PCB is 41.4 mm × 32 mm. The inductances of the shunt and series resonators are implemented by three and four parallel wirebonds, respectively, as shown in Fig. 20(b). Chip capacitors are used to complete the implementation of the series resonator and to realize the decoupling capacitors



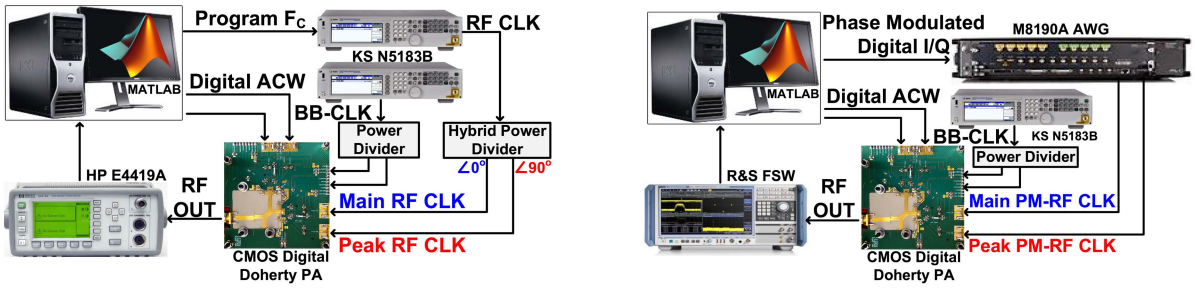
(a) (b) (c)

Fig. 19. (a) Conceptual structure of the proposed Doherty matching network. (b) Connection of the DPA to the matching network. (c) Final realization of the proposed Doherty matching network.



(a) (b) (c)

Fig. 20. (a) PCB photograph. (b) Structure of wirebonding the DPA chips to the matching network. (c) Side view of dc feed/decoupling and RF path connections.



(a) (b)

Fig. 21. Measurement setups used for (a) static and (b) dynamic measurements.

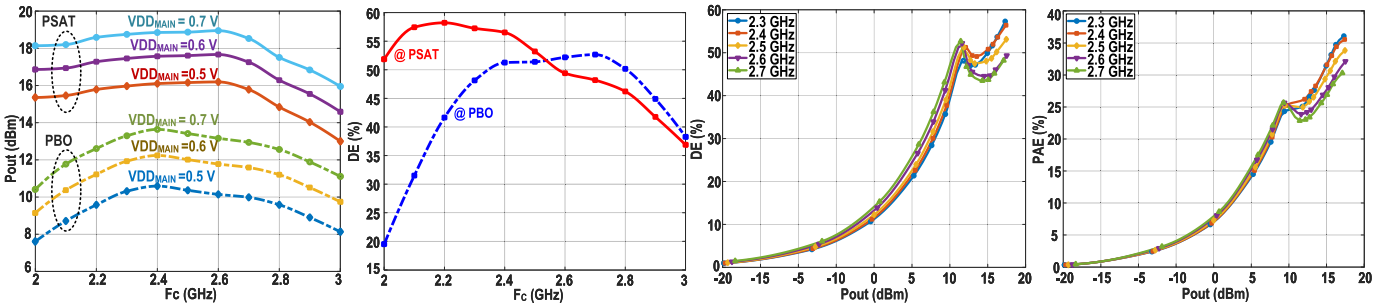
of the dc feed. The assembly structure of the PCBs with DPA chips, wirebonds, and the chip capacitors for RF and dc feed connection and decoupling is shown in Fig. 20(b). Transformer-based RF baluns are used on the FR-4 PCB to convert the single-ended clocks to differential ones before feeding them to the DPA chips.

VII. Measurement Results

A. Static Measurements

Two different measurement setups are used for the static and dynamic measurements as shown in Fig. 21(a) and (b), respectively. In the static measurements, a signal generators with a power divider arec used to provide the BB-clock to both DPAs, and another signal generator with a hybrid power divider is to provide two RF clocks with 90° phase difference for the main and peak DPAs. The BB-clock frequency is 500 MHz, which is limited by the readout speed of the SRAM used to store the data, and the RF clock varies between 2 and 3 GHz.

1) Power/Efficiency Measurement: The output power (P_{OUT}), DE, and power-added efficiency (PAE) are measured with different VDDs ranging from 0.5 to 0.7 V, for continuous-wave (CW) output signals over the frequency range of 2–3 GHz, both at full power ($\mathrm{ACW}_M = \mathrm{ACW}_P = 511$) and backoff power ($\mathrm{ACW}_M = 511, \mathrm{ACW}_P = 0$). The ACW data are generated in MATLAB and then loaded into the



(a) (b) (c) (d)

Fig. 22. Measured (a) P_{OUT} at full power and power backoff for different VDD_{Main}, (b) DE with VDD_{Main} = 0.6 V versus center frequency, (c) DE, and (d) PAE with VDD_{Main} = 0.6 V versus output power.

TABLE I

PERFORMANCE SUMMARY AND COMPARISON TABLE WITH STATE-OF-THE-ART DIGITAL DOHERTY PA

	This Work		[30]	[29]	[28]	[27]
Technology	CMOS 40nm		CMOS 65nm (LP)	CMOS 40nm	CMOS 65nm	CMOS 130nm
Frequency (GHz)	2.5		0.9	2.5	3.5	2.4
VDD (V)	0.6 / 0.7		2.4	0.7	3	3.3
Psat (dBm)	17.5		24	21.4	27	32
DE / PAE @ Psat (%)	54 / 34		N.A. / 45	50 / N.A.	30 / 26	N. A. / 51
DE / PAE @ 6dB PBO (%)	52 / 25		N.A. / 34	34 / N.A.	21 / N.A.	N. A. / 27**
Efficiency Improvement* @ 6dB PBO (%)	92		51	36	40	6
Modulated Signal BW (MHz)	16 (OFDM)	32 (OFDM)	40 (802.11ac)	20 (64QAM)	0.5 (16QAM)	20 (OFDM)
ACPR (dBc) / EVM (dB)	-52 / -50	-48 / -48	-45 / -35	-35** / -30	-28 / -27	-25 / -25
Matching Network	Off-Chip		Off-Chip	On-Chip	On-Chip	Partially On-Chip

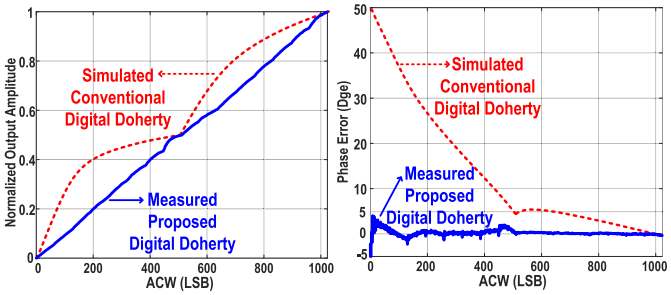
* The ratio of DE @ 6dB PBO to the DE of a normalized class-B PA @ 6dB PBO.

** Estimated graphically.

on-chip SRAMs. The output power is measured using a power meter. The PAE includes the power consumption of all the main building block on the chips, such as power the sub-PA drivers, digital decoder/encoders, multiphase RF clocking circuit, DCC, and LDO. The measured peak and backoff output power over the 2–3-GHz range are shown in Fig. 22(a), which range from 16 to 19 dBm, and 10.6 to 13.6 dBm, respectively.

The measured peak and backoff DE over the 2–3-GHz range are shown in Fig. 22(b). As can be seen, DE is more than 50% within the 2.35–2.8-GHz frequency range. The efficiency at backoff power is within 10% of its maximum value over a 750-MHz span, equivalent to 30% relative bandwidth. At F_C= 2.4 GHz with VDD_{Main}=0.6 V and VDD_{Peak}=0.7 V, the peak/backoff DE and PAE are 57%/52% and 36%/25%, respectively. The DE and PAE are plotted versus output power in Fig. 22(b) and (c) showing a well-shaped Doherty efficiency curve.

2) Linearity Measurement: Using a similar measurement setup, the static linearity is measured using a spectrum analyzer at the output to downconvert and digitize the output signal to digital baseband. Since the input signal to the DPAs is digital, it is trivial to generate a perfect quantized triangle (or ramp) signal for measuring the ACW-M and ACW-PM conversion curves. For this purpose, a 4096-sample triangle signal is generated in MATLAB, from which the main ACW_M and peak ACW_P signals are created, then loaded into the on-chip SRAMs. These SRAMs are read out in a loop with



(a) (b)

Fig. 23. Measured static (a) ACW-AM and (b) ACW-PM at F_C = 2.5 GHz without using DPD, compared to a simulated digital Doherty PA using conventional uniformly sized output stages.

a 500-MHz clock frequency, creating a 122.07-kHz triangle waveform as the input signal for the DPA branches. The digital downconverted output data are processed in MATLAB to extract the ACW-AM and ACW-PM curves. The delay mismatch between the main and peak branches is also measured. The integer part is compensated in MATLAB, while the fractional part is programmed into the chips. The resulting static linearity curves are measured at F_C = 2.5 GHz. These results are plotted in Fig. 23. As can be seen, compared to a Doherty DPA with conventional segmentation, the proposed Doherty DPA shows a significant improvement in the linearity without using any kind of DPD.

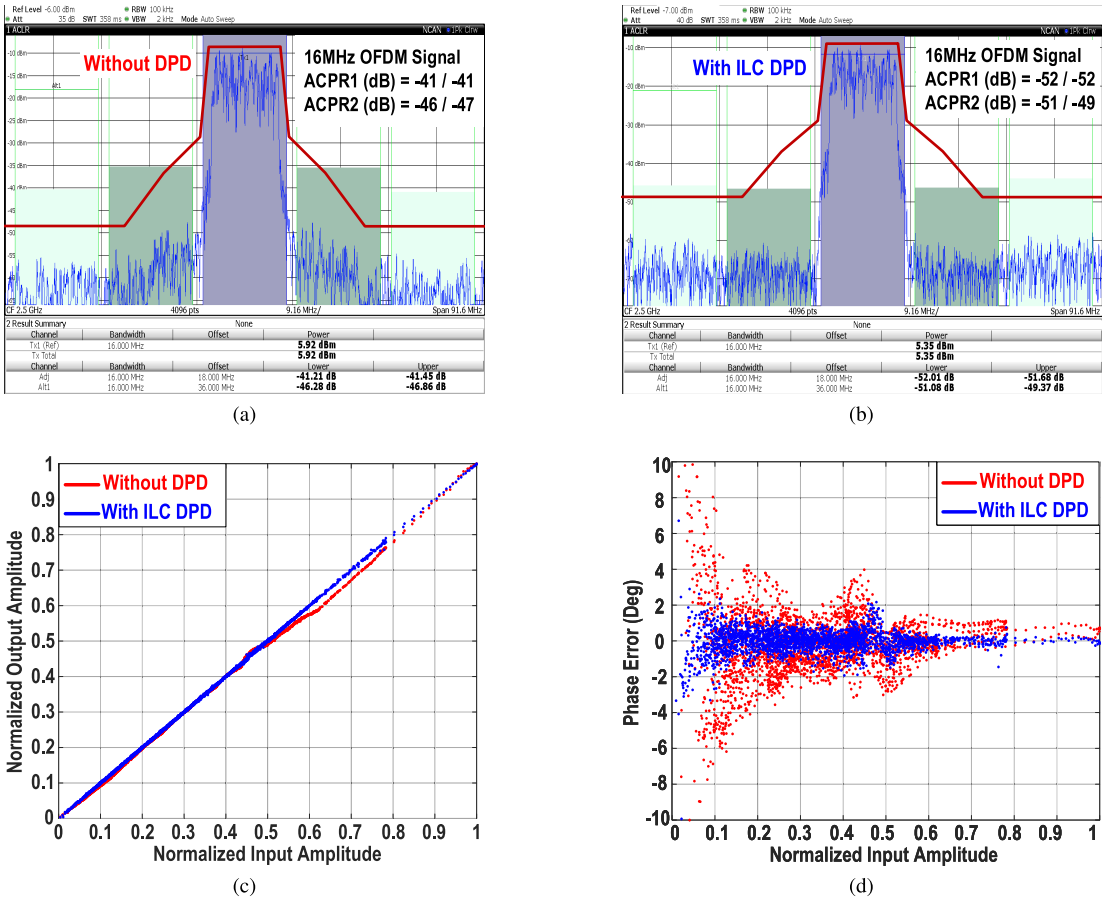


Fig. 24. Measured results of a 16-MHz OFDM signal at F_C = 2.5 GHz. Output spectrum (a) without DPD and (b) with ILC DPD. (c) ACW-AM with and without ILC DPD. (d) ACW-PM with and without ILC DPD.

B. Modulated Signal Measurements

The proposed Doherty DPA is also measured with modulated signals with the measurement setup shown in Fig. 21(b). The input I/Q signal is converted to digital AM and PM signals in MATLAB with F_S = 500 MHz. A 12-GSa/s arbitrary waveform generator (AWG) is used for generating phase modulated RF signals. For this purpose, the phase data are upconverted in MATLAB to a 2.5-GHz sine wave and then loaded into the AWG. The AM data are converted to ACW_M and ACW_P and loaded into the on-chip SRAM memories running at 500 MHz. The BB-clocks are generated using a signal generator with a power divider. Similar to the static measurements, the delay mismatch between the main and peak branches as well as the AM and PM signals are compensated both in MATLAB for integer part, and in the on-chip FIR filters for the fractional part. The output spectrum of a 16-MHz OFDM with PAPR=8.1 dB is measured with and without using DPD as shown in Fig. 24(a) and (b). The measured ACPR and EVM without DPD are −41 dBc and −36 dB, respectively. By using a simple DPD based on iterative learning control (ILC) with LUT [32], the measured ACPR and EVM are −52 dBc and −50 dB. The measured ACW-AM and ACW-PM curves of the 16-MHz OFDM signal, with and without ILC DPD, are shown in Fig. 24(c) and (d). The output spectrum of a 32-MHz OFDM signal is also measured with the ILC DPD, as shown in Fig. 25. The measured ACPR and EVM with ILC DPD are −48 dBc and −48 dB, respectively. Table I summarizes and gives the comparison of the performance of this work with the state-of-the-art in digital Doherty PAs.

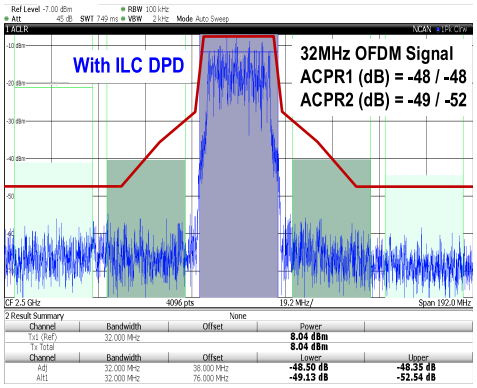


Fig. 25. Measured spectrum of a 32-MHz OFDM signal at F_C= 2.5 GHz with ILC DPD.

VIII. Conclusion

A highly linear wideband Class-E CMOS digital Doherty PA is presented. Closed-form equations are extracted to predict the AM–AM and AM–PM curves. By using a wideband

Marchand balun with reentrant coupled lines for the output matching network, more than 50% DE at ∼6-dB PBO within the 2.35–2.8-GHz frequency range is achieved. The DE at 6-dB PBO is within 10% of its maximum value over a 7500-MHz span, equivalent to 30% relative bandwidth. The measured peak/6-dB PBO P_{OUT} and DE and PAE at 2.4 GHz are 17.5 dBm/12.2 dBm, 57%/52% and 36%/25% with VDD main/peak=0.6 V/0.7 V. The linearity has been significantly improved by nonlinearly sizing of the DPA arrays along with overdrive-voltage control and concurrent multiphase RF clocking as well as accurately compensating the time/phase mismatch between the peak and main branches and the AM and PM signals. In order to achieve the maximum intrinsic linearity, two different chips with the same architecture, but with different design parameters, are fabricated as the main and peak amplifiers. Measured results show −41-dBc ACPR and −36-dB EVM for a 16-MHz OFDM signal at 2.5 GHz without using DPD. By using DPD, the measured ACPR and EVM of the 16-MHz OFDM signal are −52 dBc and −50 dB, respectively. For a 32-MHz OFDM signal, the measured ACPR and EVM are −48 dBc and −48 dB, respectively.

The proposed concept in this article is scalable to higher power levels. The future versions will include on-chip phase modulators and complete (both integer and fractional) delay calibration blocks, eliminating the need for any off-chip PM or signal processing.

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Mohsen Hashemi (S'14) was born in Ilam, Iran. He received the B.Sc. degree in electrical engineering from Shahid Beheshi University, Tehran, Iran, in 2006, and the M.Sc. degree in microelectronics engineering from the Sharif University of Technology, Tehran, in 2010. He is currently pursuing the Ph.D. degree in microelectronics engineering at the Electronics Research Laboratory Group, Delft University of Technology (TU Delft), Delft, The Netherlands.

He was the Manager of the RF Research Group, Baregheh Company, Tehran, where he was involved in designing wideband receivers and frequency synthesizers. He was with TU Delft. In November 2018, he joined the ItoM Company, Eindhoven, The Netherlands, where he is currently a Senior RF/Analog IC Designer. His current research interests include wideband efficient transmitters, analog/digital signal conditioning for high accuracy in transceivers, high-speed data converters, and high-performance phase-locked loops (PLLs).

Mr. Hashemi was a recipient of the IEEE Solid-State Circuits Society Student Travel Grant Award in 2017. He has been serving as a Reviewer for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS since 2014, and the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES since 2018.

Lei Zhou received the B.Sc. degree in electrical engineering from the Huazhong University of Science and Technology (HUST), Wuhan, China, in 2013, and the M.Sc. degree in microelectronics from the Delft University of Technology (TU Delft), Delft, The Netherlands, in 2016.

Since 2016, she has been with Ampleon, Nijmegen, The Netherlands, where she is involved in advanced high-efficiency wideband power amplifier designs.

Yiyu Shen (S'17) received the M.S. degrees in microelectronics from Tsinghua University, Beijing, China, and Katholieke Universiteit Leuven, Leuven, Belgium, in 2014. He is currently pursuing the Ph.D. degree in electrical engineering at the Delft University of Technology (TU Delft), Delft, The Netherlands.

His current research interests include power amplifiers and digital-assisted RF integrated circuits and systems.

Leo C. N. de Vreede (M'01–SM'04) received the Ph.D. degree *(cum laude)* from the Delft University of Technology (TU Delft), Delft, The Netherlands, in 1996.

In 1996, he was appointed as an Assistant Professor with TU Delft, where he was involved in the nonlinear distortion behavior of bipolar transistors at the Delft Institute of Microelectronics and Sub-Micrometer Technology. He was appointed as an Associate Professor and a Full Professor with TU Delft, in 1999 and 2015, respectively, where he became responsible for the Electronic Research Laboratory. He was involved in solutions for improved linearity and RF performance at the device and circuit and system levels. He is also the co-founder/advisor of Anteverta-mw, Eindhoven, The Netherlands, a company that is specialized in RF device characterization. He has coauthored more than 110 IEEE refereed conference and journal articles. He holds several patents. His current research interests include RF transmitters and measurement systems, RF technology, and circuit/system concepts for wireless systems.

Dr. de Vreede was a co-recipient of the IEEE Microwave Prize in 2008. He was a recipient of the TUD Entrepreneurial Scientist Award 2015. He co-guided several students who were the recipients of the Best Paper Award of BCTM, ProRISC, GAAS, ESSDERC, IMS, and RFIC Symposium.