STELLINGEN

behorende bij het proefschrift

SYNCHRONOUS DETECTION IN MONOLITHICALLY INTEGRATED AM UPCONVERSION RECEIVERS

van

J. van der Plas

1. Synchrone detectie is een zeer complexe, maar desondanks in een geïntegreerde uitvoeringsvorm bruikbare methode voor het realiseren van selectiviteit in een radio-ontvanger.

   Dit proefschrift, algemeen

2. De keuze van de middenfrequentie van een upconversie-ontvanger is een compromis tussen de complexiteit van het preselectiefilter en implementatieaspecten van het middenfrequentfilter.

   Dit proefschrift, Hoofdstuk 1

3. Het dynamisch bereik van de PLL voor draaggolfregeneratie in een synchrone detector kan aanzienlijk worden vergroot door toepassing van postdetectie-AGC en autozero-technieken.

   Dit proefschrift, Hoofdstuk 2

4. Als geïntegreerde tijdcontinue filters voor audiofrequente toepassingen zijn MOSFET-C implementaties te prefereren boven transconductantie-implementaties.

   Dit proefschrift, Hoofdstuk 4

5. Bij vele ontvangerconcepten is aan de intermodulatie en het daaraan verwante selectiviteitsverlies weinig aandacht besteed.

6. In de toekomst zal kortegolf-omroep voor de lange afstand steeds meer onder druk komen te staan van satellietomroep.

7. Semi-custom integratie is een uitstekende methode voor silicon breadboarding. Voor geïntegreerde prototypes van tijdcontinue filters is desondanks full-custom integratie veelal onvermijdelijk.

8. Het basisidee van de catamaran (en andere multihulls) berust op het vergroten van de bootstabiliteit, waarbij, in tegenstelling tot een monohull, de waterweerstand niet noodzakelijkerwijs wordt vergroot.

9. Om vervreemding van de elektrotechniek te voorkomen is het noodzakelijk dat elektronicavakken reeds in de eerste jaren van de studie voor elektrotechnisch ingenieur worden gedoceerd.

10. In het tweedejaars elektrotechnisch practicum dient het ontwerpen van en het meten aan analoge elektronische circuits een centrale plaats te behouden.

11. Verlagen van de studie-eisen is een onverantwoorde en onaanvaardbare methode om het studierendement te vergroten.

12. Gezien de problemen met de huidige tweede-fase opleiding en de afnemende externe waardering van eerste-fase ingenieurs, kan de twee-fasen structuur als mislukt worden beschouwd. Herinvoering van de oude stijl studie gekoppeld aan o.a. gefaseerde studieduurbeperking is een veel beter alternatief.

SYNCHRONOUS DETECTION IN MONOLITHICALLY INTEGRATED AM UPCONVERSION RECEIVERS

PROEFSCHRIFT

ter verkrijging van de graad van doctor aan de
Technische Universiteit Delft, op gezag van de Rector Magnificus,
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van een commissie aangewezen door het College van Dekanen
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door

Jacob van der Plas

geboren te Leiden,
elektrotechnisch ingenieur.

Dit proefschrift is goedgekeurd door de promotor
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Chapter 1

Design aspects of monolithically integrated AM upconversion receivers with synchronous detection

1.1 Introduction

The traditional receiver architecture, shown in Figure 1.1, is based on the superheterodyne principle in which the received frequency (RF) is converted to a fixed intermediate frequency (IF) by a local oscillator (LO) signal. Except for the long-wave band (150kHz-300kHz) the IF frequency (455kHz) is lower than the RF frequency and the receiver is called a downconversion receiver. The input preselection filter is a tunable bandpass filter that must accurately track with the local oscillator. Preselection is necessary to suppress the image channel at a distance twice the IF frequency from the tuned RF frequency. For optimal suppression of the image channel and spurious channels caused by local oscillator harmonics, the LO frequency should be higher than the RF and the IF frequency [1, Ch. 1].

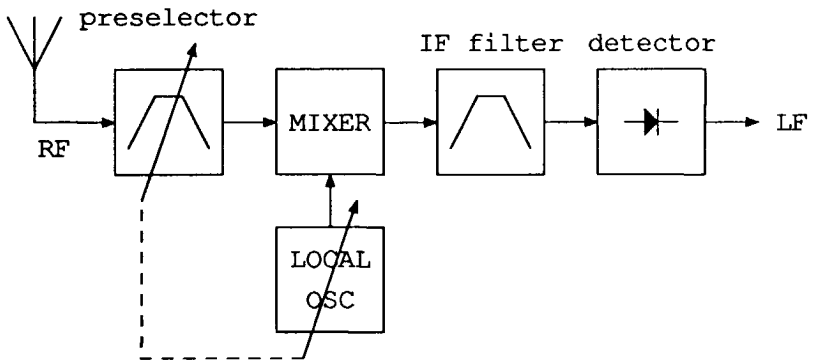

Figure 1.1: Traditional superheterodyne downconversion architecture.

In a traditional long-wave and medium-wave receiver, a band switch is implemented in the preselection filter and the local oscillator in order to reduce the relative tuning range, and to avoid tuning of the receiver within the frequency range in the proximity of the IF frequency, where there are no broadcasting stations. With an IF frequency of 455kHz and an RF frequency ranging from 150kHz to 300kHz for the long-wave band

and from 510kHz to 1600kHz for the medium-wave band, the LO frequency ranges from 605kHz to 755kHz and from 965kHz to 2055kHz respectively. Without band switches, the preselection filter must be tuned over more than 1 decade, which leads to accuracy and tracking problems. For the short-wave band with RF frequencies up to 30MHz, preselection will be quite a burden, because the narrow relative bandwidth of the preselection filter at high RF frequencies causes even worse accuracy and tracking problems. Many band switches, tunable bandpass filters and adjustments will be necessary, which makes the downconversion receiver architecture unattractive for monolithic integration.

If synthesiser tuning is desired, the required voltage-controlled tuning capability of the preselection filter is hard to implement properly, because the nonlinear behaviour of the varactors may cause unacceptable intermodulation and cross modulation of strong received signals. For optimal linearity, mechanical tuning with variable coils or capacitors cannot be avoided.

Coming to the conclusion that the tuned preselection filter in the traditional downconversion receiver architecture is the major bottleneck to monolithic integration, other receiver architectures must be found in order to get rid of this tuned preselection filter. Figure 1.2 shows the elementary superheterodyne *upconversion* architecture in which the RF frequency is converted to an IF frequency higher than the highest RF frequency. Now preselection is established by a simple fixed low-pass filter, while tuning is performed with the local oscillator only, which makes this receiver architecture very attractive for monolithic integration.

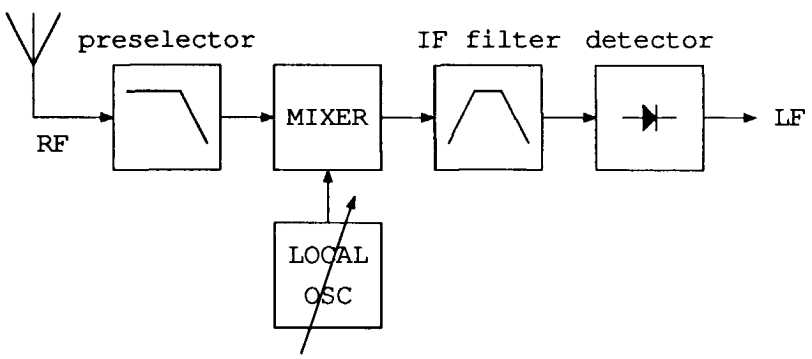

Figure 1.2: Elementary superheterodyne upconversion architecture.

Although the preselection problem disappears when upconversion is applied, several other problems arise [2, Ch. 1]. In the wide-band front end,

no channel selection is done until the IF bandpass filter. Consequently, the front-end circuitry must be extremely linear in order to prevent selectivity degradation caused by intermodulation and cross modulation. The phase noise of the local oscillator must be extremely low in order to prevent selectivity degradation caused by reciprocal mixing. The high long-term stability, required to prevent drifting from the tuned channel, can generally be obtained by the application of synthesiser tuning.

Another problem arises from the IF selectivity requirement to be obtained at high frequencies, which demands an IF filter with an extremely small relative bandwidth. If only long-wave and medium-wave reception is desired, the selectivity at an IF frequency of eg 10.7MHz can be obtained using a crystal filter. The upconversion concept using crystal IF filters has resulted in a successful design for an AM car radio [3, 4, 5]. In this case, advantages such as a high receiver performance, a minimum of peripheral components and a complete absence of adjustments finally outweigh the cost of relatively expensive crystal filters.

In a short-wave upconversion receiver, the required IF selectivity has to be obtained at an IF frequency of about 70MHz, for which (until now) only surface acoustic wave (SAW) filters have been available. Several limitations of such SAW filters concerning spurious responses, feedthrough and accuracy completely exclude the possibility of obtaining complete channel selectivity at the high IF frequency. Additional selectivity has to be obtained at a second and lower IF frequency, for which the demands concerning feedthrough, accuracy and the relative bandwidth are less stringent. This second conversion introduces an additional image channel at a distance twice the *second* IF frequency from the tuned RF frequency, which has to be suppressed by the *first* IF filter. Although the limited first IF selectivity results in a limited image selectivity, this concept may still be favoured over the traditional downconversion concept with its preselection problem.

If the first IF signal is directly converted to the baseband by means of synchronous detection, which principle is shown in Figure 1.3, additional selectivity at lower frequencies is obtained without introducing an image channel. Synchronisation of the second local oscillator is performed with a phase-locked loop (PLL), keeping the second local oscillator exactly in phase with the desired carrier in the IF signal. Although a synchronous detector can be regarded as a receiver on its own, its performance is not sufficient to provide for the overall receiver selectivity demands. However, if the superheterodyne upconversion concept is combined with synchronous detection, an integration friendly receiver design is feasible, especially if the

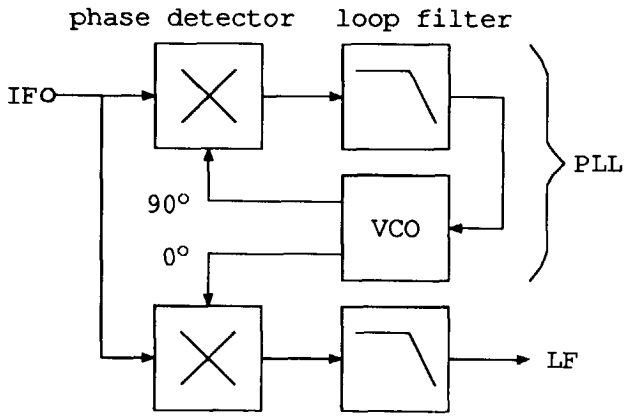

Figure 1.3: Principle of synchronous detection.

low-pass filters can be implemented on-chip.

This thesis is focussed upon the design of a synchronous detector, intended to provide additional selectivity in an AM upconversion receiver with a tuning range from 150kHz to 30MHz and an IF frequency of (preliminarily) 70MHz. The complete receiver has to be silicon integrable with a minimum of peripheral components. The receiver circuits will be designed for a single 8V power supply. The design of the receiver front end is described in [2], while the fundamental aspects of monolithically integrated AM receivers can be found in [1].

After a brief introduction to AM modulation and detection in Section 1.2, an analysis of the distribution of selectivity and signal dynamic range in the receiver is given in Section 1.3. Subsequent sections deal with general receiver aspects, such as spurious channels in Section 1.4, intermodulation effects in Section 1.5, oscillator and filter accuracy in Section 1.6 and finally the oscillator spectral purity in Section 1.7. The design specifications in this chapter are those used in the synchronous detector architecture design in Chapter 2 and the circuit design in the subsequent chapters.

1.2 Introduction to AM modulation and detection

In an amplitude modulated (AM) signal, the information is coded as the instantaneous amplitude of a periodic carrier. In broadcasting techniques this carrier is commonly a sine wave. With $m(t)$ representing the information

or the baseband signal, the AM signal is described in the time domain by:

$$v_{am}(t) = \hat{v}_0\{1 + m(t)\}\cos(\omega_0 t + \phi) \tag{1.1}$$

In this equation $\hat{v}_0$ denotes the unmodulated carrier level and ω_0 denotes the carrier frequency. The level of the baseband signal $m(t)$ is normalised to that carrier level. If the carrier is suppressed, the AM signal can be described as:

$$v_{am}(t) = \hat{v}_0 m(t)\cos(\omega_0 t + \phi) \tag{1.2}$$

In the frequency domain, the baseband spectrum convolves around the carrier frequency, which results in two sidebands around the carrier frequency. Taking $M(\omega)$ as the double-sided Fourier transform of the baseband signal $m(t)$, the AM signal can be described in the frequency domain by:

$$V_{am}(\omega) = V_0\{1 + M(\omega)\} * \frac{1}{2}\{\delta(\omega + \omega_0) + \delta(\omega - \omega_0)\} \tag{1.3}$$

$$V_{am}(\omega) = \frac{1}{2}V_0\{M(\omega + \omega_0) + \delta(\omega + \omega_0) + M(\omega - \omega_0) + \delta(\omega - \omega_0)\} \tag{1.4}$$

In this equation V_0 denotes the complex amplitude, for which $|V_0| = \hat{v}_0$ and $\arg(V_0) = \phi$. The baseband signal bandwidth is assumed to be smaller than the carrier frequency so no folding around the origin occurs.

For calculation purposes, the baseband signal is modelled as a single sine wave with frequency μ, resulting in an AM signal like:

$$v_{am}(t) = \hat{v}_0\{1 + m\sin(\mu t)\}\cos(\omega_0 t + \phi) \tag{1.5}$$

In this equation, m denotes the modulation depth. If $m \geq 1$ the carrier is overmodulated, but it is still possible to recover the baseband signal properly. Expanding this equation into single frequency components results in:

$$\begin{aligned} v_{am}(t) &= \hat{v}_0\left\{\cos(\omega_0 t + \phi) + \frac{m}{2}\cos((\omega_0 + \mu)t + \phi)\right. \\ &\quad \left. + \frac{m}{2}\cos((\omega_0 - \mu)t + \phi)\right\} \end{aligned} \tag{1.6}$$

The power ratio between the sidebands and the carrier is calculated as:

$$\frac{P_{\text{modulation}}}{P_{\text{carrier}}} = \frac{m^2}{2} \tag{1.7}$$

The average modulation depth of AM long-wave, medium-wave and short-wave broadcasting stations is about 0.3, while the channel spacing (in Europe) is 9kHz. For numerical calculation purposes, a modulation depth of 0.3 and a baseband frequency of 1kHz is taken. With a modulation depth of 0.3, the power ratio between the sidebands and the carrier is 0.045 or -13dB

AM modulation is based on multiplication of the baseband signal by a carrier, so the inverse process, AM demodulation or AM detection, is based on division by, or multiplication by the inverse of that carrier. Electronic division or the generation of an inverse sine wave, however, can hardly be implemented. Multiplication of the AM signal by a coherent periodic signal with arbitrary waveform, the reference signal, represented by its Fourier series:

$$v_{ref}(t) = \sum_{n=1}^{\infty} \hat{b}_n \cos(n\omega_0 t + \phi_n) \tag{1.8}$$

yields:

$$v_{det}(t) = \hat{v}_0\{1 + m(t)\}\left(\frac{\hat{b}_1}{2}\cos(\phi - \phi_1) + \sum_{n=1}^{\infty} \hat{c}_n \cos(n\omega_0 t + \theta_n)\right) \tag{1.9}$$

With the assumption that the bandwidth of the baseband signal is smaller than half the carrier frequency, the higher-order frequency components can be suppressed by subsequent low-pass filtering, which leaves the baseband signal:

$$v_{lf}(t) = \hat{v}_0\frac{\hat{b}_1}{2}\{1 + m(t)\}\cos(\phi - \phi_1) \tag{1.10}$$

Only the amplitude and the phase of the fundamental frequency component of the reference signal are important in demodulation.

The low-pass filter following the multiplying detector not only suppresses unwanted detection products, but it can also provide for bandpass selectivity seen at the input of the detector as well. This can be illustrated if an input signal with frequency ω is multiplied by a reference signal with frequency ω_0:

$$v_{det}(t) = \hat{v}\cos(\omega t + \phi)\cos(\omega_0 t + \phi_1) \tag{1.11}$$

$$v_{det}(t) = \frac{\hat{v}}{2}\cos((\omega + \omega_0)t + \phi + \phi_1) + \frac{\hat{v}}{2}\cos((\omega - \omega_0)t + \phi - \phi_1) \tag{1.12}$$

Assuming $\omega \geq 0$, $\omega_0 \geq 0$ and $\omega_0 \gg B$, the low-pass filter bandwidth, the sum frequency term falls far outside the filter bandwidth. For the frequency

components in the detected signal, which fall inside the filter bandwidth, we obtain a bandpass characteristic:

$$|\omega - \omega_0| \leq B \tag{1.13}$$

Multiplication transforms the subsequent low-pass characteristic into a bandpass characteristic. Since the low-pass filter characteristic is convolved around every frequency component in the reference signal, selectivity in order to suppress interfering channel signals can only be accomplished if the reference signal, apart from its harmonics, is spectrally pure.

In a receiver, the reference frequency required for detection is generally not present and must be derived from the received signal itself. The reference signal should be unmodulated and in-phase with the received frequency. Although AM demodulation also occurs when the AM signal is squared, this method also produces serious second-order distortion of the baseband signal, because this baseband signal is also squared.

One method to derive the reference signal, shown in Figure 1.4, is limiting of the received signal, producing an unmodulated square wave, in-phase reference signal. Obviously, interfering channel signals will introduce spurious frequency components in this reference signal. Consequently a subsequent low-pass filter will not contribute to the receiver selectivity, so all interfering signals must be suppressed with a bandpass filter in front of the detector [6]. This kind of AM detector is called an envelope detector, because the detected signal follows the envelope $|1 + m(t)|$ of the AM signal. As a result, this detector is unable to demodulate overmodulated AM signals $(m(t) < -1)$ properly.

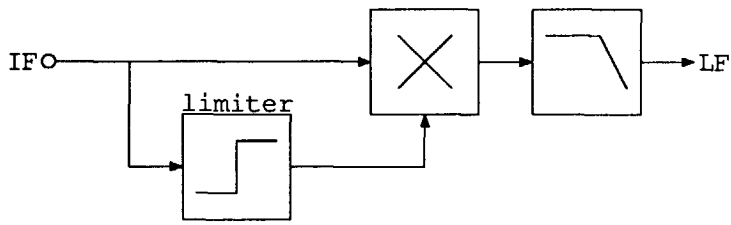

Figure 1.4: Principle of envelope detection.

The major advantage of an envelope detector is its simplicity, since the combination of limiting and multiplication can be implemented by using a rectifier. For proper operation, the rectifier should be current driven in order to eliminate the influence of the voltage drop over the diodes and the

output load impedance. Examples of an integrated envelope detector can be found in [5] or [7]. Also the simple but very popular diode detector can be regarded as an envelope detector.

If selective detection is desired, the spurious frequency components in the reference signal caused by interfering channel signals must be suppressed. Although these spurious frequency components can be suppressed by using a bandpass filter, the suppression of interfering channel signals by using a bandpass filter in front of the complete detector gives better results.

A selective detector becomes attractive if the reference signal is derived from the received signal with a PLL, shown in Figure 1.3. The phase detector is also a multiplier, so the bandpass characteristic, necessary to get a spectrally pure carrier, is obtained by the low-pass PLL loop filter. This type of detector, in which bandpass selectivity is obtained by low-pass filtering and synchronisation of the reference frequency is performed with a PLL is called a coherent detector or a synchronous detector [8]. An additional advantage of this detector is its capability to demodulate overmodulated AM signals properly.

A major drawback of synchronous detection is the amount of overhead circuitry required for regenerating a spectrally pure carrier. For this reason, synchronous detection is only applied where high linearity together with special forms of AM (eg TV sets [9]) or built-in selectivity (eg instrumentation systems and upconversion receivers) is required. Although some experimental synchronous receivers have been made (see eg. [10]), the application of a synchronous detector as a selective detector for AM receivers has sporadically been used.

1.3 Distribution of selectivity, signal levels and dynamic range

In this thesis, we define the dynamic range of any subcircuit of a receiver system part as the ratio between the maximum carrier level it can handle and the noise floor. In order to present a clear overview of the distribution of selectivity and dynamic range, any carrier level will be expressed relative to its maximum level. For the sake of simplicity, maximum carrier levels are normalised to 0dB.

For the carrier regenerating PLL, the signal-handling dynamic range is defined as the ratio of the maximum and the minimum PLL input carrier level the PLL is able to lock onto.

The sensitivity of a receiver is defined as that minimum input level that results in a signal-to-noise ratio (SNR) of 26dB of the detected baseband

signal in a 2.5kHz bandwidth, under the condition that only the desired channel signal is present. With a modulation depth of 30%, the ratio between the modulation and the carrier is 13dB, so the sensitivity corresponds to a carrier-to-noise ratio (CNR) of about 40dB. The calculation of the RF or IF noise bandwidth of the receiver corresponding to an LF bandwidth of 2.5kHz can be found in Section 3.1.1.

The selectivity of a receiver is defined as the ratio between an interfering input carrier level and the desired input carrier level that result in equal LF output levels, under the condition that both carriers have equal modulation depths. For the adjacent channel selectivity, the interfering carrier is one channel space (9kHz) away from the desired carrier, while for the stopband selectivity, the interfering carrier is at least five channel spaces away from the desired carrier. For the ultimate selectivity, the interfering carriers are far away from the desired carrier. These selectivity specifications are schematically shown in Figure 1.5.

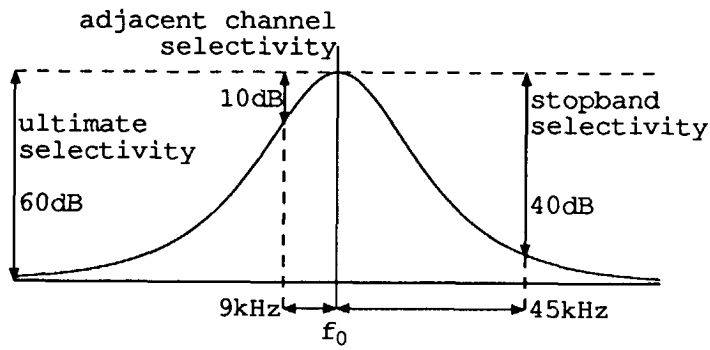

Figure 1.5: Selectivity specifications for a typical selectivity curve. The numerical values indicate the feasible selectivity of a coupled SAW resonator.

It has been shown in [2] that a 120dB dynamic range of a wide-band front end (150kHz–30MHz) is feasible. This dynamic range is sufficient for portable and HIFI receiver sets provided that no extremely strong field strengths (in the close proximity of transmitters) are present. For the complete receiver, a manageable specification is that all interfering channel signals in the stopband have to be suppressed to at least below the sensitivity level. With the given front-end dynamic range, the sensitivity level corresponds to a carrier level of −80dB. With a margin of about 10dB, because of possible simultaneously occurring interfering signals, the required stopband selectivity amounts to 90dB. Since a 90dB adjacent channel selectivity

would result in unrealistic filter specifications, a reduced adjacent channel selectivity of 45dB has been chosen here as a compromise between quality and filter complexity.

With a coupled surface acoustic wave resonator [2, Ch. 4], a stopband selectivity of 40dB and an ultimate selectivity of about 60dB is feasible. The adjacent channel selectivity, however, is limited to some 10dB. Consequently, the synchronous detector has to provide for the additional 50dB stopband selectivity and 35dB adjacent channel selectivity.

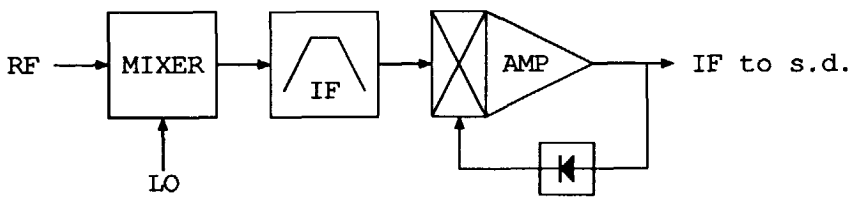

Figure 1.6: Functional implementation of AGC amplification in the IF part.

Behind the IF bandpass filter, the level of interfering signals is decreased. With an automatic gain control (AGC) amplifier, it is possible to accommodate the IF level to the maximum input level of the synchronous detector. This reduces the dynamic range demands of the synchronous detector. The functional implementation of the AGC amplifier is shown in Figure 1.6. We will assume that the AGC amplifier delivers the strongest signal to the synchronous detector at a (relative) level of 0dB.

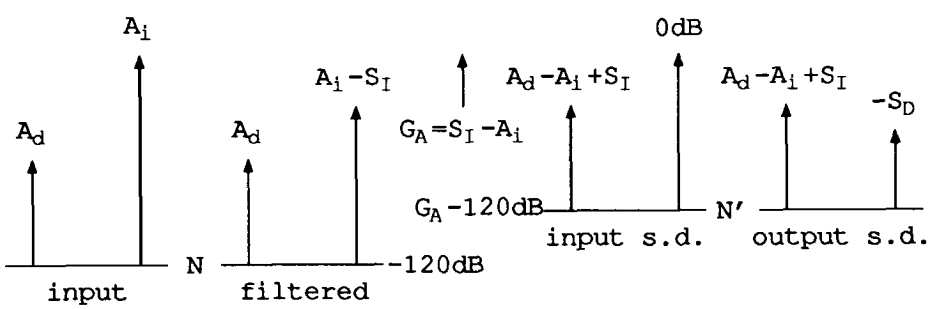

Figure 1.7: Signal level distribution with $A_d < A_i - S_I$.

Figure 1.7 shows a signal level distribution at the antenna input, behind the IF bandpass filter, at the synchronous detector input and at the synchronous detector output respectively. The values of the desired antenna input carrier level A_d, the interfering antenna input carrier level A_i, the IF

selectivity S_I, the detector selectivity S_D and the IF AGC amplification G_A are given in dB. This signal level distribution is based on a specific antenna input level range, for which $A_d < A_i - S_I$. Another signal level distribution, for which $A_d \geq A_i - S_I$ is shown in Figure 1.8. The base lines of both signal level distributions correspond to the noise floor N at the front end and N' at the detector input respectively.

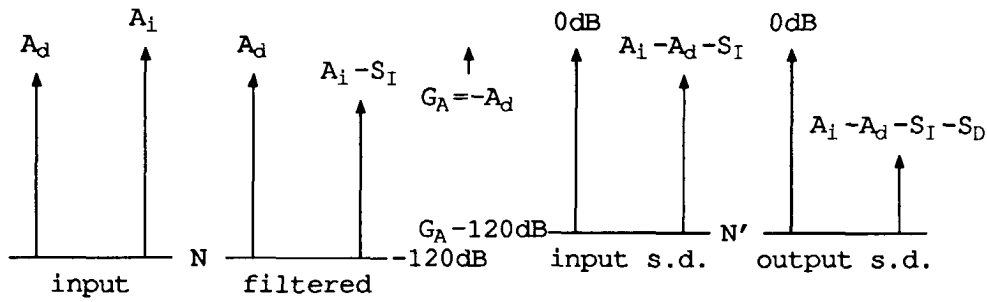

Figure 1.8: Signal level distribution with $A_d \geq A_i - S_I$.

If we examine Figure 1.7 and Figure 1.8, the (possible) AGC amplification G_A can be derived as:

$$G_A = \begin{cases} S_I - A_i & \text{if } A_d < A_i - S_I \\ -A_d & \text{if } A_d \geq A_i - S_I \end{cases} \tag{1.14}$$

and the resulting noise floor N' at the input of the synchronous detector can be derived as:

$$N' = \begin{cases} S_I - A_i - 120\text{dB} & \text{if } A_d < A_i - S_I \\ -A_d - 120\text{dB} & \text{if } A_d \geq A_i - S_I \end{cases} \tag{1.15}$$

In this equation, the noise contribution of the IF circuitry is disregarded. For the desired carrier level at the input of the synchronous detector A'_d, we can derive:

$$A'_d = \begin{cases} A_d - A_i + S_I & \text{if } A_d < A_i - S_I \\ 0\text{dB} & \text{if } A_d \geq A_i - S_I \end{cases} \tag{1.16}$$

The carrier level A'_d and the noise floor N' at the input of the synchronous detector and also the possible AGC amplification G_A as a function of the desired antenna input carrier level A_d are visualised in Figure 1.9 for different values of $S_I - A_i$.

If we consider a worst case situation, in which a maximum level interfering carrier is present in the stopband ($S_I - A_i = 40$dB), the 120dB antenna

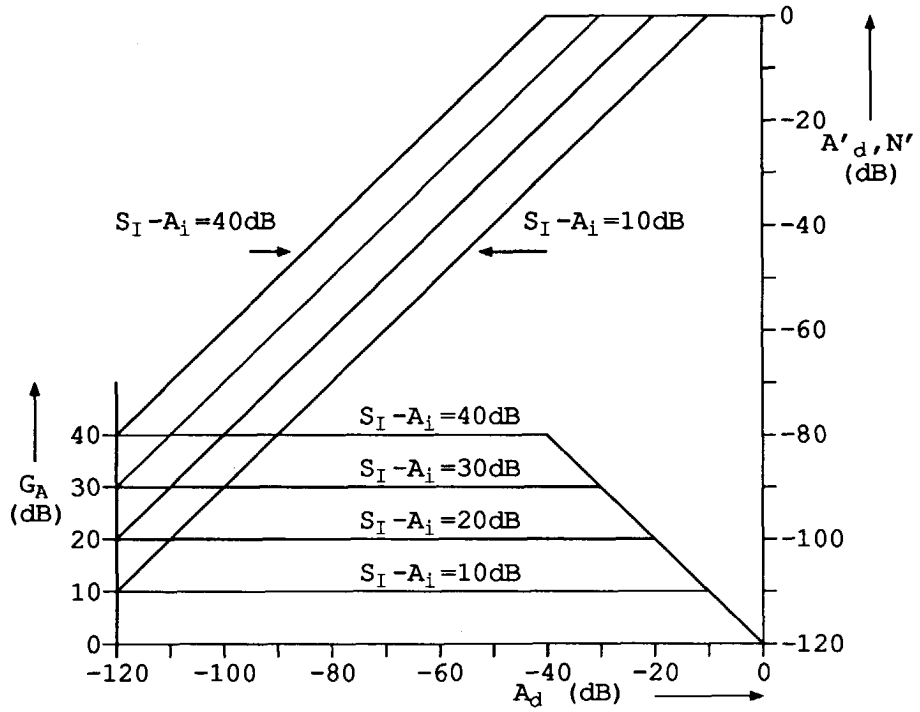

Figure 1.9: AGC amplification G_A, noise floor N' (lower curves) and the carrier level at the synchronous detector input A'_d (upper curves) against the desired antenna input carrier level.

input level range of the desired carrier is reduced to an 80dB detector input level range. Obviously, the control range of the IF AGC amplifier has to be at least 40dB. For $A_d < -40$dB, the noise floor N' at the detector input is -80dB, which is not increased if the dynamic range of the synchronous detector is at least 80dB. In order to guarantee this minimum dynamic range, a minimum dynamic range of 90dB for the individual circuit parts (mixer, filter, amplifiers etc.) is recommended. For $A_d \geq -40$dB, an 80dB dynamic range results in a sufficient signal-to-noise ratio of the detected signal (66dB).

If we consider a worst case situation, in which a maximum level interfering adjacent carrier is present ($S_I - A_i = 10$dB), the 120dB antenna input level range of the desired carrier is reduced only 10dB to a 110dB level range at the detector input. Consequently, the synchronous detector dynamic range should be 110dB in order to prevent degradation of the

carrier-to-noise ratio for weak desired carriers in this worst case situation. However, the high interference level of the detected signal, which is -35dB if $A_d < -10$dB ($S_D = 35$dB), is 45dB higher than the noise floor, if the detector dynamic range is 80dB. Apart from the fact that a synchronous detector with a dynamic range of 110dB is very hard to implement, such a high dynamic range is regarded as useless because of the high interference level.

Figure 1.10 shows the synchronous detector output carrier levels as a function of the antenna input level of the desired carrier for different values of $S_I - A_i$. The synchronous detector dynamic range is 80dB. The straight lines indicate the output level of the desired carrier. The dash-dotted lines indicate the output level of interfering carriers for a maximum level interfering carrier in the stopband (the lower one) and a maximum level interfering adjacent carrier (the upper one).

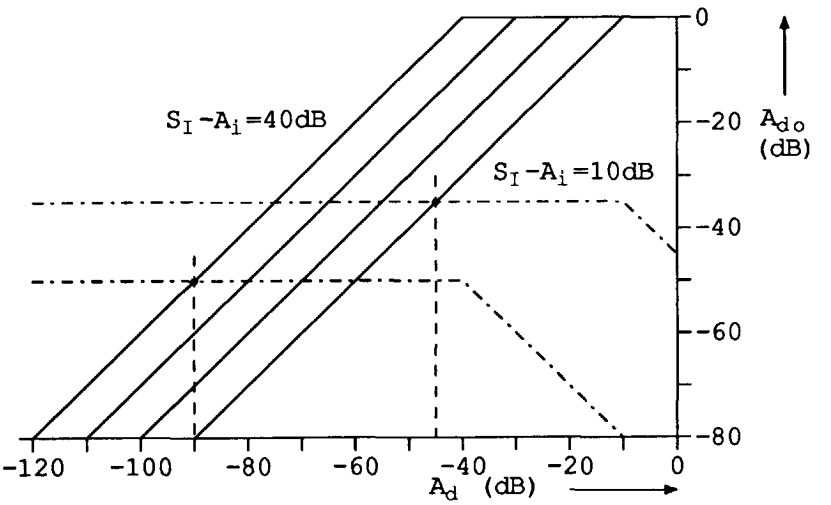

Figure 1.10: Synchronous detector output carrier levels against the desired antenna input carrier level.

The reception of a desired carrier is regarded as completely useless if its synchronous detector output level is not higher than the output level of the interfering signal. If we look at the interference levels in Figure 1.10, we can conclude that the minimum usable input level is -50dB at the synchronous detector input and -90dB at the antenna input if a maximum level interfering carrier is present in the stopband. However, if a maximum level interfering adjacent carrier is present, the minimum usable input car-

rier level is −35dB at the synchronous detector input and −45dB at the antenna input.

The 50dB stopband selectivity of the synchronous detector can only be accomplished if the carrier regenerating PLL is able to lock onto the desired carrier with an input level from −50dB to 0dB. Consequently, the minimum signal-handling dynamic range of the PLL has to be 50dB. In a situation where no strong interfering signal is present, the minimum 40dB IF AGC control range and the minimum 50dB signal handling dynamic range guarantee reception of desired signals with a level down to 10dB below the sensitivity limit (−90dB at the antenna input).

1.4 Spurious channels

Spurious channels are unwanted sensitivities of the receiver caused by the upconversion in the front end and the synchronous conversion in the detector. A conversion model for calculation of the spurious channel frequencies is shown in Figure 1.11. The local oscillator and the VCO signals are assumed to be symmetrical square waves, so the harmonic conversion gains of the corresponding mixers can be written as:

$$G_{Cn} = \begin{cases} \frac{1}{n} G_C & \text{n odd} \\ 0 & \text{n even} \end{cases} \tag{1.17}$$

In this equation, G_C is the conversion gain resulting from the oscillator fundamental frequency component and n is the harmonic number (see also Section 1.2 and 3.1.1)

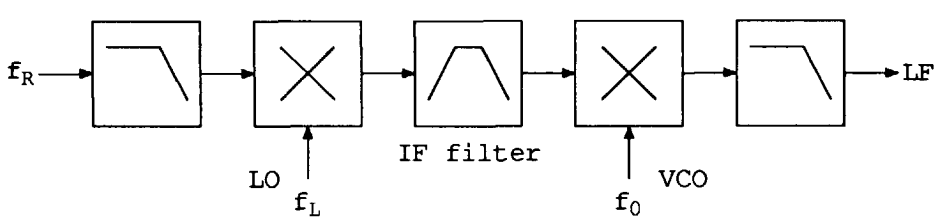

Figure 1.11: Conversion model of the receiver.

In this thesis, we define the spurious selectivity of a particular spurious channel as the ratio of the corresponding spurious input carrier level and the desired input carrier level that results in equal LF output levels, under the condition that both carriers have equal modulation depths. Special kinds of spurious channels, called image channels, are those resulting from the

fundamental frequency components of the oscillators. The definition of the corresponding image selectivity conforms that of the spurious selectivity. Obviously, the upconversion receiver with synchronous detection has only one image channel, for which the image selectivity is completely determined by the preselection filter. For this receiver, the spurious selectivity (and also the image selectivity) is presumed to be at least the stopband selectivity (90dB).

For a given desired RF frequency f_R and a given IF frequency f_0, two possible local oscillator frequencies can be calculated:

$$f_L = f_0 - f_R \text{ , a low LO frequency and} \quad (1.18)$$

$$f_L = f_0 + f_R \text{ , a high LO frequency.} \quad (1.19)$$

For both local oscillator frequencies, the desired RF frequency is equal to $f_R = |f_0 - f_L|$ and the image frequency is equal to $f'_R = f_0 + f_L$. The image frequency in terms of f_0 and f_R can be calculated as:

$$f'_R = 2f_0 - f_R \text{ , for a low LO frequency and} \quad (1.20)$$

$$f'_R = 2f_0 + f_R \text{ , for a high LO frequency.} \quad (1.21)$$

The high local oscillator frequency results in the highest image frequency, and therefore the highest suppression by the low-pass preselection filter. For this reason, the high local oscillator frequency is preferred. An additional advantage of a high local oscillator frequency is a smaller relative tuning range.

For the complete receiver, all spurious RF channel frequencies f_C including the desired channel frequency and the image channel frequency can be calculated according to the conversion model in Figure 1.11 as:

$$f_C = |(n \pm m)f_0 - nf_R| \text{ , for a low LO frequency and} \quad (1.22)$$

$$f_C = |(n \pm m)f_0 + nf_R| \text{ , for a high LO frequency.} \quad (1.23)$$

In these equations, f_R is the tuned RF frequency, n is the harmonic number of the local oscillator frequency and m is the harmonic number of the VCO frequency.

First we will concentrate upon the spurious channels, for which $m = 1$. If a low local oscillator frequency is taken, the spurious channel frequencies with $n > 1$ may be lower than the image frequency. However, if a high local oscillator frequency is taken, all spurious channel frequencies with $n > 2$ are higher than the image frequency (see also [1, Ch. 1.2]). In this case, a

sufficiently high image selectivity automatically includes a sufficiently high spurious selectivity for $m = 1$.

Spurious channels for which $m > 1$ may fall directly into the RF band and are not suppressed by the preselection filter. For $m = n$, the corresponding spurious channel frequencies are harmonics of the tuned RF frequency. The spurious selectivity of these channels is determined by the ultimate selectivity of the IF bandpass filter at the odd harmonics of the IF frequency f_0 and the conversion gain of the mixers. With a third harmonic conversion gain being 10dB lower than the fundamental conversion gain and an ultimate selectivity of 60dB, the spurious selectivity of these channels is at least 80dB. Additional spurious selectivity of these spurious channels can be obtained by additional (low-pass or bandpass) IF filtering.

If a high local oscillator frequency is chosen, the image channel frequency is larger than the highest RF frequency if the IF frequency is larger than half the highest RF frequency. However, due to direct feedthrough of the upconversion mixer and spurious reception in the IF filter, the IF frequency should not be chosen in the RF band. Since the 70MHz IF frequency is situated just above the first television band, this IF frequency is also used for professional (short-wave) receivers.

The preselector filter used in the upconversion receiver is a low-pass filter with a bandwidth of 30MHz. For a maximum suppression outside the filter passband, a Chebyshev characteristic is chosen. Some passband ripple can be tolerated, since the channel bandwidth is much smaller than the filter bandwidth and the ripple within this channel bandwidth is negligible. With a high local oscillator frequency, the nearest image frequency is equal to $2f_0 + 150\text{kHz} \approx 2f_0$. Consequently, the filter suppression at $2f_0$ has to be at least 90dB.

The amplitude transfer of an all-pole Chebyshev filter [11] can be written as:

$$|H(\Omega)|^2 = \frac{1}{1 + \epsilon^2 T_n^2(\Omega)} \tag{1.24}$$

In this equation, $T_n(\Omega)$ is a Chebyshev polynomial of the first kind with order n, Ω is the (angular) frequency normalised to the (angular) cut-off frequency of the preselection filter and ϵ depends on the passband ripple. The passband ripple ϵ_{dB} expressed in dB is written as:

$$\epsilon_{dB} = 10\log(1 + \epsilon^2) \tag{1.25}$$

For frequencies outside the filter passband, the filter attenuation A_{dB} is

approximated by:

$$A_{dB} = 20\log(\epsilon T_n(\Omega)) \tag{1.26}$$

For an IF frequency of 70MHz, a 90dB suppression of the nearest image channel of 140MHz can be obtained with a fifth-order Chebyshev filter with a 3dB passband ripple ($\epsilon = 1$). The fifth-order Chebyshev polynomial of the first kind is equal to:

$$T_5(\Omega) = 16\Omega^5 - 20\Omega^3 + 5\Omega \tag{1.27}$$

If we wish to apply a lower IF frequency, this frequency must be chosen below the television band (< 47MHz). The required 90dB image selectivity at an IF frequency about 40MHz can be obtained with a seventh-order Chebyshev filter with a 3dB passband ripple. The seventh-order Chebyshev polynomial of the first kind is equal to:

$$T_7(\Omega) = 64\Omega^7 - 112\Omega^5 + 56\Omega^3 - 7\Omega \tag{1.28}$$

The main advantage of a lower IF frequency is a lower relative bandwidth and hence a lower demand upon the accuracy and quality of the IF filter. The disadvantage is a more complex preselection filter. The required 120dB dynamic range can only be realised with passive, external LC filters.

1.5 Intermodulation effects

Intermodulation products in the receiver, caused by nonlinearities, degrade the receiver selectivity, since they may fall into the passband of the IF filter or the synchronous detector. An important figure of merit combining the nonlinearity with the dynamic range is the intermodulation-free dynamic range (IMFDR). The upper limit of the IMFDR is defined by that level of two signals with equal amplitude that produces intermodulation products with a level equal to the noise floor, while the lower limit is the noise floor itself.

Evidently, a high linearity demand is imposed upon all circuits in the signal path of the receiver. For such circuits, a weak nonlinearity approximation can be applied, which implies that the nonlinearities have no significant effect upon the first-order transfer. For circuits such as amplifiers, mixers and active filters, this weak nonlinearity approximation is generally valid for signal levels up to the 1dB compression point.

In order to enable a convenient calculation of the nonlinearity of the IF circuits, for which the main signal frequency spectrum is concentrated

around the IF frequency f_0, a narrow-band approximation can be applied. In this narrow-band approximation, frequency dependent elements are given their value for the IF frequency f_0, while subsequently the elements are regarded to be frequency independent within a certain bandwidth around f_0. A similar approximation can be applied to the noise and subsequently to the IMFDR.

The output voltage (or current) of a nonlinear system as a function of the input voltage (or current) can be written as a power series:

$$v_o = \sum_{n-1}^{\infty} a_n v_i^n \tag{1.29}$$

For weak nonlinear transfers, only the first-, second- and third-order terms are considered:

$$v_o = a_1 v_i + a_2 v_i^2 + a_3 v_i^3 \tag{1.30}$$

If two sine functions with equal amplitude are taken as the input signal:

$$v_i(t) = \hat{v}\{\sin(\omega_1 t) + \sin(\omega_2 t)\} \tag{1.31}$$

the level of the second- and third-order intermodulation components relative to the level of the first-order component, called for short the intermodulation, is calculated as:

$$\mathrm{IM}_2 = \frac{a_2}{a_1}\hat{v} \tag{1.32}$$

$$\mathrm{IM}_3 = \frac{3a_3}{4a_1}\hat{v}^2 \tag{1.33}$$

The output voltage components according to the power series in Equation 1.30 are visualised in Figure 1.12. The horizontal axis corresponds to the noise floor N. If the n^{th} order intermodulation IM_n and the carrier-to-noise ratio CNR are given for a certain signal level, the n^{th} order intermodulation-free dynamic range IMFDR_n (all values in dB) can be derived as:

$$\mathrm{IMFDR}_n = \frac{n-1}{n}\mathrm{CNR} - \frac{1}{n}\mathrm{IM}_n \tag{1.34}$$

For weak nonlinear circuits in the receiver, only the second- and third-order IMFDR are of interest.

In order to prevent selectivity degradation by intermodulation distortion, the intermodulation distortion $-\mathrm{IM}_n$ resulting from two maximum level interfering channel signals has to be at least equal to the stopband selectivity

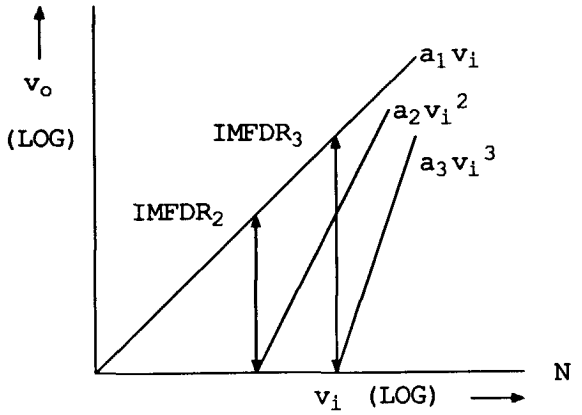

Figure 1.12: Illustration of the IMFDR.

S. Obviously, the CNR of maximum level channel signals is equal to the dynamic range R. The required IMFDR of a radio circuit part, expressed in its required dynamic range R and the required selectivity S is written as:

$$\text{IMFDR}_n = \frac{n-1}{n} R + \frac{1}{n} S \tag{1.35}$$

The values of the selectivity S and the dynamic range R of all receiver parts have been calculated in Section 1.3.

For the receiver front end, containing the input amplifier, the preselection filter, the upconversion mixer and the IF filter, the dynamic range is 120dB, while the stopband selectivity is 90dB. Consequently, the required second- and third-order IMFDR is equal to 105dB and 110dB respectively.

At the output of the IF filter, the dynamic range of adjacent channel signals is reduced to 110dB and the dynamic range of interfering channel signals in the stopband is reduced to 80dB. The remaining adjacent channel and stopband selectivity, to be obtained in the synchronous detector, is 35dB and 50dB respectively. This results in a minimum second- and third-order dynamic range of 75dB and 85dB respectively for the IF AGC amplifier.

For the circuits behind the IF AGC amplifier, a 90dB dynamic range is recommanded in order to guarantee an 80dB dynamic range of the synchronous detector (see Section 1.3). With the remaining 50dB stopband selectivity, the required second- and third-order IMFDR of these circuits is equal to 70dB and 77dB respectively. Although second-order intermodulation products in the IF part do not fall into the passband of the synchronous detector, second-order distortion causes spurious detection of AM

modulated carriers. The resulting spurious baseband components may penetrate through the synchronous mixer because of unbalance and fall into the passband of the subsequent low-pass filter. Spurious detection also occurs in the (active) low-pass filters behind the synchronous mixers.

Behind the channel selective low-pass filters of the synchronous detector, the nonlinearity specification depends on the maximum acceptable audio distortion (no remaining selectivity). For AM receivers, a (harmonic) audio distortion less than 0.5% is generally accepted.

1.6 Accuracy of oscillators and filters

In this section, the accuracy demands imposed upon the local oscillator frequency, the IF filter central frequency and the VCO initial frequency are discussed. These accuracy demands are based upon two criteria. The first one is the requirement that the desired carrier, including at least one complete sideband, has to be converted into the passband of the IF filter. The second one is the requirement that the initial beat note has to fall within the capture range of the carrier regenerating PLL. This initial beat note is the phase detector output frequency if the VCO operates on its initial frequency. The accuracy specifications in this section are given over the entire operating temperature range.

Figure 1.13 shows a simplified conversion model of the receiver. The frequency f_0 denotes both the nominal IF frequency and the nominal VCO initial frequency. With Δf_L the absolute local oscillator inaccuracy and Δf_F the absolute IF filter inaccuracy, the absolute detuning of the IF filter Δf_I can be written as:

$$|\Delta f_I| = |\Delta f_F| + |\Delta f_L| \tag{1.36}$$

Both inaccuracies are assumed to be uncorrelated and the inaccuracy of the RF frequency is neglected. With Δf_V the absolute inaccuracy of the VCO initial frequency, the initial beat note f_B can be expressed as:

$$f_B = |\Delta f_L| + |\Delta f_V| \tag{1.37}$$

Here again, both inaccuracies are assumed to be uncorrelated.

Applying a high local oscillator frequency ($f_L = f_0 + f_R$), the relative IF filter detuning can be calculated as:

$$\frac{|\Delta f_I|}{f_0} = \frac{|\Delta f_F|}{f_0} + \frac{f_0 + f_R}{f_0}\frac{|\Delta f_L|}{f_L} \tag{1.38}$$

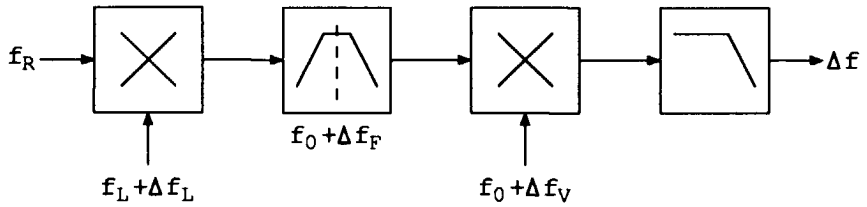

Figure 1.13: Conversion model of the receiver.

With an audio bandwidth of 3kHz and an IF filter bandwidth of 6kHz, the maximum permitted absolute filter detuning is 3kHz. With the IF frequency of 70MHz, the maximum permitted (relative) tolerance of the local oscillator frequency and the IF filter central frequency at the highest RF frequency is calculated as:

$$\frac{|\Delta f_I|}{f_0} = \frac{|\Delta f_F|}{f_0} + 1.4\frac{|\Delta f_L|}{f_L} \leq 43\text{ppm} \tag{1.39}$$

The local oscillator has to be synthesiser tuned using a highly accurate quartz reference crystal, the tolerance of which is about 10ppm. The resulting maximum 29ppm tolerance of the SAW IF filter is almost impossible to obtain. Consequently, the IF filter bandwidth has to be increased in order to fulfill the requirement for filter detuning (see also [2]). This is the main reason why we may not expect more than 10dB adjacent channel selectivity with a coupled SAW resonator.

In order to fulfill the beat-note capture range criterion, the tolerance of the local oscillator frequency and the VCO initial frequency is calculated as:

$$\frac{f_0 + f_R}{f_0}\frac{|\Delta f_L|}{f_L} + \frac{|\Delta f_V|}{f_0} = \frac{f_B}{f_0} \tag{1.40}$$

With the application of acquisition methods in the carrier regenerating PLL (see Section 2.4.4), a capture range of about 2kHz is feasible. With a 70MHz IF frequency, the maximum combined local oscillator and VCO tolerance at the highest RF frequency is expressed by:

$$\frac{f_B}{f_0} = 1.4\frac{|\Delta f_L|}{f_L} + \frac{|\Delta f_V|}{f_0} \leq 29\text{ppm} \tag{1.41}$$

With a 10ppm tolerance of the local oscillator frequency, the maximum 15ppm tolerance of the VCO initial frequency can only be achieved by incorporating a second, highly accurate quartz crystal.

The accuracy demands, imposed upon the local oscillator frequency, the IF filter central frequency and the VCO initial frequency, can only be fulfilled

by using high precision and hence expensive quartz devices. If a lower IF frequency (about 40MHz, see Section 1.4) is chosen, these accuracy demands are slightly reduced at the cost of a more complex preselection filter. With a 40MHz IF frequency, a quartz bulk resonator might be used as an IF filter. Generally, a bulk resonator has a better accuracy than a SAW resonator.

The accuracy demands can be reduced if the local oscillator frequency, the IF filter central frequency and the VCO initial frequency can be derived from one (quartz) reference frequency f_x. Unfortunately, it is not possible to relate the fixed central frequency of the IF SAW filter to a reference frequency. As an alternative, the reference frequency might be derived from a SAW resonator on the same substrate as the IF SAW filter. However, feedthrough effects and matching problems make this a doubtful solution.

If the VCO initial frequency is derived from the reference frequency of the local oscillator synthesiser, its relative tolerance is equal to the tolerance of that reference frequency. The inaccuracies Δf_L and Δf_V are completely correlated, so the initial beat-note frequency can be written as:

$$f_B = |\Delta f_L - \Delta f_V| \tag{1.42}$$

The initial beat-note frequency relative to f_0 can be written as:

$$\frac{f_B}{f_0} = \frac{f_R}{f_0}\frac{|\Delta f_x|}{f_x} \tag{1.43}$$

This equation can be rewritten to:

$$\frac{f_B}{f_R} = \frac{|\Delta f_x|}{f_x} \tag{1.44}$$

At the maximum RF frequency, the maximum initial beat note resulting from a 10ppm tolerance of the reference frequency is 300Hz.

The implementation of a VCO system, for which the initial frequency is derived from the local oscillator reference frequency is dealt with in Section 2.3. With this VCO system, one extremely accurate and hence expensive quartz crystal can be circumvented.

1.7 Influence of oscillator noise and spurious components

Spurious oscillator (LO or VCO) frequency components are discrete, unwanted and nonharmonic oscillator frequency components that may convert

interfering channel signals into the passband of the IF filter or the synchronous detector. In other words, spurious oscillator frequency components introduce additional spurious channels, for which the required spurious selectivity has to be equal to the selectivity (see also Section 1.4). Spurious oscillator components are generally caused by the LO or VCO synthesiser. For the VCO, additional spurious components are also caused by the finite interfering carrier suppression of the PLL.

In analogy with the harmonic mixer conversion gain given in Section 1.4, the spurious mixer conversion gain resulting from a spurious component can be written as (see also Section 1.2 and 3.1.1):

$$G_{Cs} = \frac{G_C}{\text{CSR}} \tag{1.45}$$

In this equation, G_C is the regular conversion gain and CSR is the carrier-to-spurious ratio, which is the amplitude or rms ratio of the regular frequency component and the corresponding spurious component.

In contrast to the spurious channels caused by the local oscillator harmonics, spurious channels caused by local oscillator spurious components in the proximity of the regular local oscillator frequency are not suppressed by the preselection filter. Consequently, a corresponding 90dB spurious selectivity requires a spurious conversion gain, which is at least 90dB lower than the regular conversion gain and hence a 90dB carrier-to-spurious ratio. If a spurious component is situated only one channel space (9kHz) away from the regular local oscillator frequency, the corresponding CSR demand can be reduced to 45dB, which is equal to the adjacent channel selectivity.

Spurious channels caused by VCO spurious components in the proximity of the regular VCO frequency are suppressed 10dB by the adjacent channel selectivity (Δf = 9kHz) or 40dB by the stopband selectivity of the IF bandpass filter. The resulting CSR of the VCO, has to be equal to the selectivity of the synchronous detector.

In the carrier regenerating PLL, the finite suppression of converted interfering carriers by the PLL loop filter causes phase modulation of the VCO by those carriers. The resulting spurious components in the VCO output signal convert the corresponding interfering channel signals at the input of the synchronous mixer into the passband of the subsequent low-pass filter. This effect is illustrated in Figure 1.14.

In order to prevent selectivity degradation by the finite interfering carrier suppression of the PLL, the resulting CSR of the VCO has to be at least equal to the selectivity. With A'_d the desired carrier level and A'_i the inter-

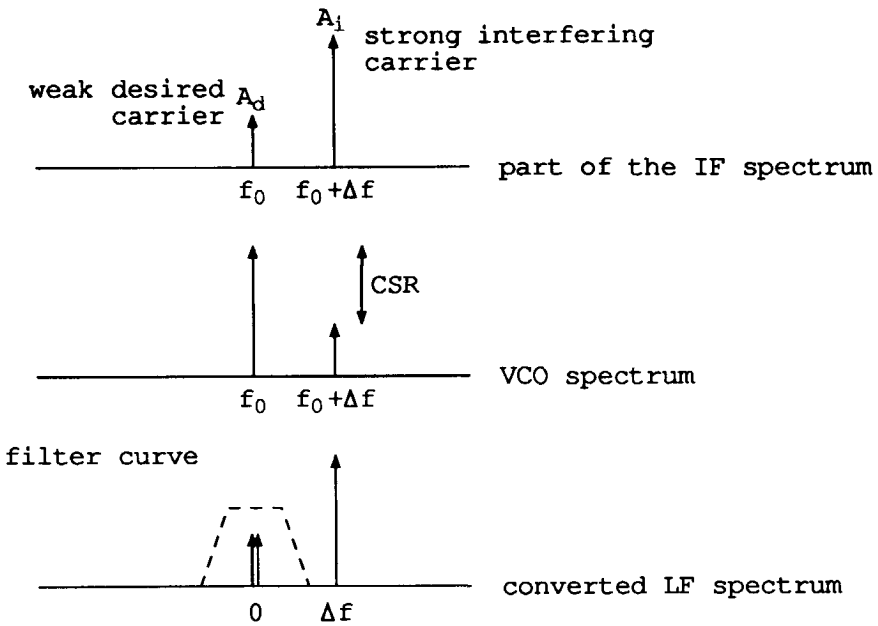

Figure 1.14: Selectivity degradation due to VCO spurious components caused by interfering carriers.

fering carrier level at the input of the synchronous detector and CSR_V the corresponding VCO output carrier-to-spurious ratio, the PLL suppression A_L (all values in dB) is defined as:

$$A_L = (A_i' - A_d') + \mathrm{CSR}_V \tag{1.46}$$

Since both the maximum $A_i' - A_d'$ and the required CSR_V are equal to the selectivity, the PLL adjacent carrier or stopband suppression has to be at least twice the synchronous detector adjacent channel or stopband selectivity:

$$\begin{aligned} A_L(9\mathrm{kHz}) &= 70\mathrm{dB} \\ A_L(45\mathrm{kHz}) &= 100\mathrm{dB} \end{aligned}$$

In analogy with the effect of oscillator spurious components, oscillator (LO or VCO) noise also converts interfering channels into the passband of the IF filter or the synchronous detector. This effect, which is called reciprocal mixing [2, Ch. 1.5] [1, Ch. 3.4], is illustrated in Figure 1.15. The

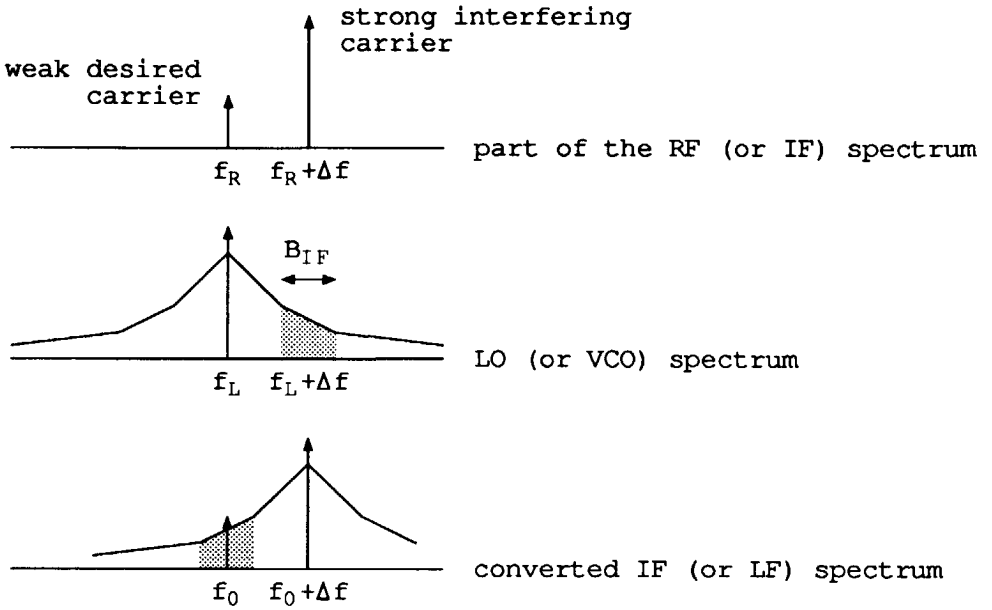

Figure 1.15: Illustration of reciprocal mixing by oscillator noise.

shaded area in the oscillator spectrum indicates the spectral part of the oscillator noise responsible for reciprocal mixing.

The single-sided phase noise spectral density of an oscillator, indicated by $\mathcal{L}(\Delta f)$ and given in dBc/Hz, is the ratio of the noise power in a 1Hz bandwidth at a frequency distance Δf from the carrier and the carrier power level, which is the power level of the oscillator fundamental frequency component. The corresponding carrier-to-noise level (CNR), given in dBc, can be approximated by:

$$\mathrm{CNR} = -\mathcal{L}(\Delta f) - 10\log(B_{IF}) \tag{1.47}$$

In this equation, Δf is the frequency distance of the corresponding interfering carrier and B_{IF} is the IF noise bandwidth of the synchronous detector, which is calculated in Section 3.1.1.

In order to prevent selectivity degradation caused by reciprocal mixing, the CNR has to be at least equal to the selectivity. For the local oscillator this results in:

$$\begin{aligned} \mathcal{L}(9\mathrm{kHz}) &= -80\mathrm{dBc/Hz} \\ \mathcal{L}(45\mathrm{kHz}) &= -125\mathrm{dBc/Hz} \end{aligned}$$

and for the VCO, this results in:

$$\begin{aligned} \mathcal{L}(9\text{kHz}) &= -70\text{dBc/Hz} \\ \mathcal{L}(45\text{kHz}) &= -85\text{dBc/Hz} \end{aligned}$$

The corresponding noise bandwidth is 2.5kHz. It is shown in [12] that these short-term stability demands can be fulfilled by using on-chip oscillators.

The direct influence of the VCO phase noise upon the signal-to-noise ratio of the desired carrier can be derived if we write the synchronous mixer conversion gain, calculated in Section 3.1.1 as:

$$G_{C\phi} = G_{C0} \cos(\phi - \phi_0 - \phi_n) \tag{1.48}$$

In this equation, ϕ is the phase of the desired IF carrier, ϕ_0 is the average VCO phase and ϕ_n indicates the VCO phase noise. A minimum sensitivity of the synchronous conversion gain for the VCO phase noise ϕ_n is obtained if the phase difference $\phi - \phi_0$ is zero. In this case, the direct influence of oscillator noise upon the signal-to-noise ratio of the desired channel signal is negligible compared with the effect of reciprocal mixing.

1.8 Summary

In this chapter, the application of synchronous detection is proposed for an AM short-wave upconversion receiver with a limited IF channel selectivity, in order to obtain the required additional selectivity without introducing additional image channels. The design of the AM upconversion receiver front end, in which the IF filter is implemented using a coupled SAW resonator on a quartz substrate, is described in [2].

The synchronous detector specifications have been derived from the front-end dynamic range and the available IF selectivity, combined with the criterion that any interfering signal has to be suppressed down to a level of 10dB below the sensitivity limit. Apart from the synchronous detector specifications, additional front-end specifications concerning the intermodulation-free dynamic range, the preselection filter suppression and the local oscillator accuracy and stability have been derived.

The interface between the front end and the synchronous detector is an IF spectrum AGC amplifier, which accommodates the output level of the IF filter to the maximum signal level of the synchronous detector. Specifications of this AGC amplifier have been given as well.

A critical aspect of this receiver is the accuracy of the local-oscillator frequency and the IF filter central frequency. The accuracy demand of the VCO initial frequency can be reduced if this initial frequency is derived from the local-oscillator reference frequency.

A lower IF frequency reduces the accuracy demand imposed upon the local oscillator and the IF filter, but increases the complexity of the preselection filter. In Section 1.4 an alternative IF frequency of 40MHz is proposed that requires a seventh-order preselection filter instead of the required fifth-order preselection filter for a 70MHz IF frequency. A 40MHz IF frequency offers the possibility of implementing the IF filter as a quartz bulk resonator filter. The accuracy of such a bulk resonator is generally higher than that of a SAW resonator. An additional advantage of a lower IF frequency, and consequently lower LO and VCO frequency, is a reduced power consumption. Although this thesis proceeds with a 70MHz IF frequency, the results can also be used for the alternative 40MHz IF frequency as well.

Chapter 2

Synchronous detector architecture

This chapter deals with the architecture design of the synchronous detector, the elementary functional implementation of which is shown in Figure 2.1. This synchronous detector has to provide for 35dB adjacent channel selectivity and 50dB stopband selectivity, while its dynamic range has to be at least 80dB (see Section 1.3). Additionally, the signal-handling dynamic range of the carrier regenerating PLL has to be at least 50dB.

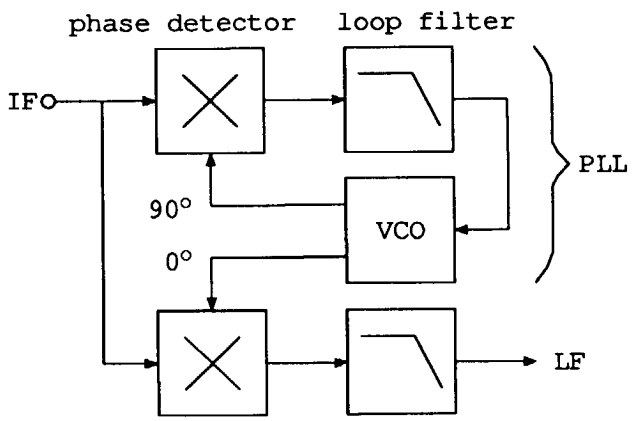

Figure 2.1: Elementary functional implementation of the synchronous detector.

In order to assure the required selectivity and dynamic range of the complete synchronous detector, the dynamic range of the mixers and the low-pass filters has to be at least 90dB (see Section 1.3), while the second- and third-order IMFDR (see Section 1.5) has to be at least 70dB and 77dB respectively. These specifications can only be fulfilled if the phase detector and the in-phase synchronous mixer are implemented as long-tailed pair switching mixers. The electronic implementation of these mixers can be found in Section 3.1. The application of a phase detector with a linear IF signal input is essential in order to prevent false lock on intermodulation components.

The phase-to-voltage transfer of a phase detector implemented as a long-

tailed pair switching mixer (see Section 3.1.1) is proportional to the level of the desired carrier at the IF phase detector input. If this phase detector gain variation is not compensated for, the loop gain of the PLL is proportional to the carrier level it is locked onto and consequently, the high dynamic range of input signals may severely endanger the stability of the loop. Although it is possible to design a high-order nested loop according to [1, Ch. 4] or [13] with a pole-zero pattern insensitive for loop-gain variations, such a design appears to be very complex. A more effective method is compensation of the phase detector gain variation by the application of an AGC amplifier [14, 15, 16]. This solution, called post-detection AGC will be developed in Section 2.1.

A second and even worse problem is caused by offset voltages in the post-detection circuitry. Especially when the desired signal is weak, offset voltages will introduce large phase errors and may even pull the PLL out of lock. If the problem concerning the phase detector gain variation has been solved, the maximum signal-handling dynamic range of the PLL will finally be limited by these offset voltages. Offset adjustments do not offer a useful solution, since they cannot solve the problem of the offset temperature drift. Techniques to perform automatic compensation of the offset including its temperature drift will be described in the Section 2.2.

A third problem, already noticed in Section 1.6, is the requirement of a VCO with an extremely accurate initial frequency. The impact of this accuracy requirement can be reduced if this VCO initial frequency is derived from the local oscillator reference frequency. In Section 2.3, a VCO system will be designed, in which the initial frequency is almost determined by this reference frequency.

Finally, Section 2.4 deals with the dynamic behaviour of the carrier regenerating PLL. The loop-filter time constants will be calculated in order to obtain the required interfering carrier suppression (see Section 1.7).

2.1 Implementation of post-detection AGC

The main purpose of post-detection AGC is the extension of the signal-handling dynamic range of the PLL by stabilising its loop gain with a controllable-gain amplifier behind the phase detector. In order to prevent saturation of that amplifier by interfering channel signals, these signals must be suppressed with a low-pass filter immediately following the phase detector. The actual loop filter containing at least one pole and one zero can be placed either in front of or behind the AGC amplifier. In order to limit the

detrimental influence of wide-band AGC amplifier noise and the resulting wide-band oscillator phase noise, the latter solution is preferred.

For a minimum static phase error of the PLL, the loop-filter pole must be situated in the origin. In combination with the inherent integration in the VCO voltage-to-phase transfer and the pole of the low-pass filter immediately following the mixer, a third-order type-2 PLL is obtained. A pole in the origin combined with a zero can easily be established with a passive RC network if the AGC amplifier has a current output. The resulting PLL is depicted in Figure 2.2. Since the mixer is implemented as a double-balanced long-tailed pair mixer, its input and output signals are drawn as balanced signals.

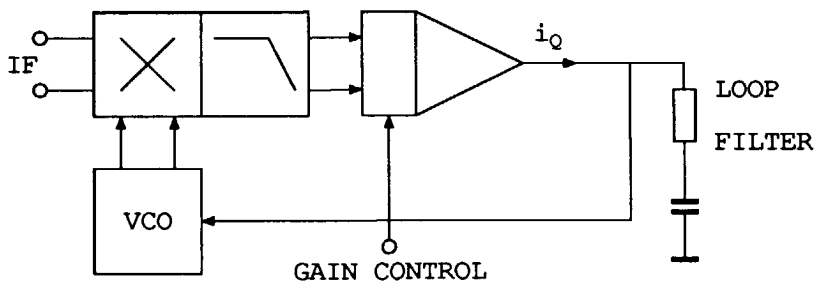

Figure 2.2: PLL with loop-gain control.

The principle of automatic gain control (AGC), in which the output level of the AGC amplifier is compared with a reference level and fed back to its gain-control input cannot be applied directly in the PLL. The signal generated by the phase detector is only a phase error signal containing no unambiguous information about the input carrier level. The control signal must be derived from the dc component of the output signal of the synchronous in-phase mixer which is proportional to the input carrier level the PLL is locked onto. This dc component, obtained with a low-pass filter, might be connected directly to the gain-control input of the AGC amplifier in the PLL loop [17]. The accuracy of this forward control method however will be rather poor over the entire dynamic range.

The accuracy of the loop-gain control can be considerably increased by the application of indirect-feedback gain control, shown in Figure 2.3. The dc component I_I of the output current of the AGC amplifier I in an additional in-phase path, which is proportional with the desired IF input carrier level, is stabilised by means of direct feedback. If the resulting control voltage is also supplied to an identical AGC amplifier Q in the PLL, its loop gain is

stabilised as well. Supplying the same control voltage to an identical AGC amplifier A in the audio path also provides for a constant audio output level. Since all AGC amplifiers are implemented on the same chip, they will be well matched. Although both in-phase paths could be combined, the implementation of offset compensation techniques, to be explained in the next section, requires the audio detection part to be separated from the carrier regeneration and gain-control part.

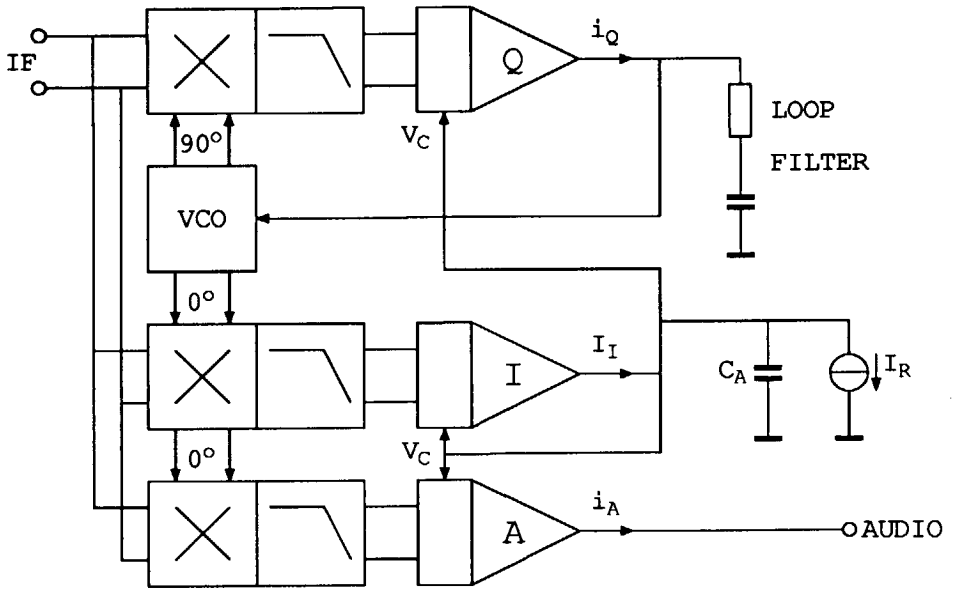

Figure 2.3: Indirect feedback AGC system.

Provided that the phase difference $(\phi_0 - \phi)$ between the VCO frequency and the desired IF input carrier frequency approaches zero, the output currents i_Q, I_I and i_A of the AGC amplifiers Q, I and A respectively can be written as:

$$i_Q = \hat{v}_i G_C G_A(\phi_0 - \phi) \quad (2.1)$$

$$I_I = \hat{v}_i G_C G_A \quad (2.2)$$

$$i_A = \hat{v}_i G_C G_A(1 + m\sin(\mu t)) \quad (2.3)$$

In these equations, $\hat{v}_i$ is the desired IF input carrier voltage amplitude, G_C is the conversion gain of the three identical synchronous mixers (see Section 3.1.1) and G_A is the controlled gain of the three identical AGC

amplifiers. The modulation component in i_Q is almost suppressed by the narrow-band PLL loop filter.

The gain-control voltage V_C can be written as a differential equation:

$$\frac{dV_C}{dt} = \frac{1}{C_A}(I_I - I_R) \tag{2.4}$$

In the steady state, I_I equals the AGC reference current I_R. The static error is negligible thanks to the pure integration in the AGC control loop. Now the output currents of the AGC amplifiers can be written as:

$$i_Q = I_R(\phi_0 - \phi) \tag{2.5}$$
$$I_I = I_R \tag{2.6}$$
$$i_A = I_R(1 + m\sin(\mu t)) \tag{2.7}$$

The resulting transfer from the mixer input to the LF AGC amplifier output according to these equations is determined by the AGC reference current I_R only! This reference current controls the effective phase detector transfer and the audio output level of the synchronous detector.

The dynamic behaviour of the AGC control loop is preferred to be independent of the received carrier level $\hat{v}_i$. Its -3dB frequency has to be lower than the lowest audio frequency in order to prevent suppression of the AM modulation by this AGC control loop. If $\hat{v}_i$ is regarded as an unknown parameter, the time derivative of I_I in Equation 2.2 is calculated as:

$$\frac{dI_I}{dt} = \hat{v}_i G_C \frac{dG_A}{dV_C}\frac{dV_C}{dt} \tag{2.8}$$

In combination with Equation 2.4, this results in the differential equation:

$$\frac{dI_I}{dt} = \frac{\hat{v}_i G_C}{C_A}\frac{dG_A}{dV_C}(I_I - I_R) \tag{2.9}$$

A constant AGC loop bandwidth independent of $\hat{v}_i$ results in the condition:

$$\frac{\hat{v}_i G_C}{C_A}\frac{dG_A}{dV_C} = k \tag{2.10}$$

in which k is an arbitrary constant. Using Equation 2.2, this equation is rewritten into:

$$\frac{dG_A}{dV_C} = G_A\frac{kC_A}{I_I} \tag{2.11}$$

In the stationary state, I_I nearly equals the AGC reference current I_R, so this equation implies an exponential gain-control function.

An exponential transfer can be implemented with a bipolar transistor in CE configuration:

$$I_C = I_S \exp(V_{BE}/V_T) \tag{2.12}$$

In this equation, I_C denotes the collector current, I_S denotes the saturation current, V_{BE} denotes the base-emitter voltage and V_T denotes the thermal voltage kT/q. If G_A is proportional with I_C and V_{BE} equals V_C, we obtain:

$$\frac{dG_A}{dV_C} = \frac{G_A}{V_T} \tag{2.13}$$

However if G_A is inversely proportional with I_C (see Chapter 5), we obtain:

$$\frac{dG_A}{dV_C} = -\frac{G_A}{V_T} \tag{2.14}$$

Now the dynamic behaviour of the AGC loop can be described with the differential equation:

$$\frac{dI_I}{dt} = \frac{I_I}{C_A V_T}(I_R - I_I) \tag{2.15}$$

Mind that the resulting dynamic behaviour is independent of the saturation current I_S and the IF input carrier level $\hat{v}_i$. As already mentioned, I_I nearly equals I_R in the stationary state, so this differential equation finally results in:

$$\frac{dI_I}{dt} = \frac{I_R}{C_A V_T}(I_R - I_I) \tag{2.16}$$

This first-order transfer has a time constant equal to:

$$\tau_A = \frac{C_A V_T}{I_R} \tag{2.17}$$

This time constant corresponds to the -3dB frequency of the AM modulation suppression by the AGC loop. In order to combine fast AGC control with a negligible suppression for audio frequencies, the AGC time constant is chosen to be 10ms, which results in an AGC -3dB bandwidth of 16Hz. The detailed electronic implementation of the AGC circuitry will be described in Chapter 5

2.2 Offset compensation techniques

In order to take profit from the dynamic range extension by the AGC system in the preceding section, offset voltages in the post-detection circuitry must be compensated for automatically. Two techniques to perform automatical offset compensation are available: the chopping technique [18] and autozero technique [15, 16].

The application of chopping techniques in the PLL is shown in Figure 2.4. The VCO signal is mixed with the low-frequency chopping signal, which is a symmetrical square wave with a frequency of some 10kHz. The resulting oscillator signal converts the desired channel signal to a low-frequency spectrum centered around the chopping frequency, so dc signals don't carry any information. After bandpass filtering and amplification of the phase detector output signal, the spectrum is converted back to the baseband. The remaining offset is caused by the last conversion and, when divided by the gain of the AGC amplifier, results in a negligible equivalent input offset voltage. An additional delay line is necessary to compensate the delay time of the bandpass filter.

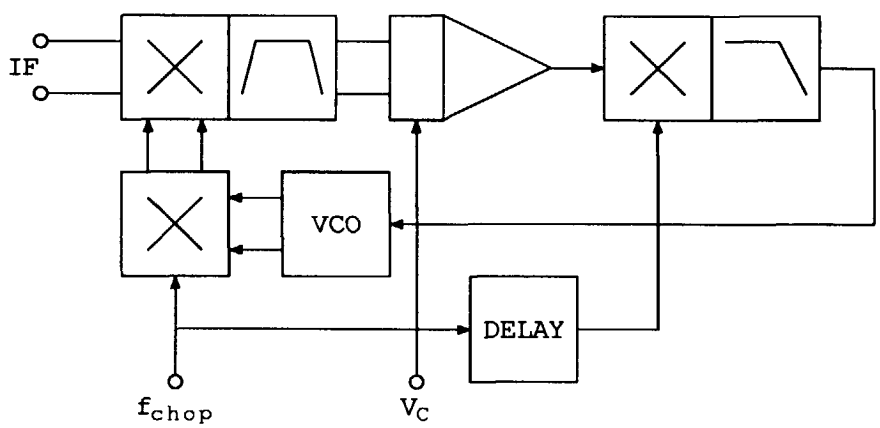

Figure 2.4: Principle of chopping.

Multiplication of the VCO signal by a low-frequency square wave (about 10kHz) of the chopping oscillator causes many spurious frequency components in the resulting oscillator signal. These spurious components will badly degrade the selectivity of the synchronous detector and may even cause false locks. If a summing loop PLL system or a single side band modulator would be applied in order to produce a spectrally pure shifted reference signal, the

indirect conversion of the chopping technique will introduce an image channel with frequency distance twice the chopping frequency. These problems make the chopping technique unattractive for automatic offset compensation in the synchronous detector.

The application of another offset compensation technique, called autozero, is shown in Figure 2.5. The switches in this figure are functioning in the operating phase. For the AGC amplifiers, the 'O' input is the offset compensation input while the 'G' input is the gain-control input. During the autozero phase, the input IF signal is switched off. The output signal of the AGC amplifier is switched to be compared with a reference voltage and fed back to the (offset adjust) input. Meanwhile, an offset adjustment voltage is generated on the autozero capacitor C_{AZ}. The VCO control voltage is hold during the autozero phase by the capacitor in the loop filter. During the operating phase, the PLL works normally as if no autozero actions were present. The offset control voltage, generated during the autozero phase, is hold by the capacitor C_{AZ}. Conform the chopping technique, the remaining offset caused by the offset comparator results in a negligible equivalent input offset voltage.

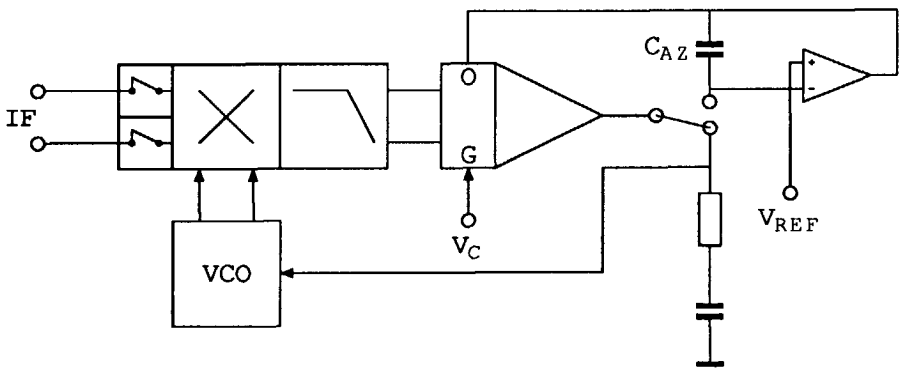

Figure 2.5: Principle of autozero.

The implementation of the low-frequency switches as CMOS transmission gates and the application of a CMOS offset comparator guarantees a minimum droop of the autozero hold capacitors C_{AZ} during the operating phase. In Section 5.4, it will be shown that the autozero hold capacitor can be implemented on-chip, while the autozero frequency can be limited to 10Hz. The minimum autozero time must be 4–5 times higher than the time constant of the low-pass filters directly following the mixer, in order to discharge the corresponding capacitor down to 1% of its voltage in the

operating phase. A time constant about 1ms (see Section 2.4) results in an autozero time of 5ms.

The autozero technique has two major advantages over the chopping technique. In the first place, the combination of a low autozero frequency of about 10Hz and a low duty cycle of about 5% results in a very small amount of spurious oscillator power and spurious channels. These spurious channels fall into the audio and sub-audio band of the desired channel, so they have no detrimental influence on the selectivity. Secondly, the autozero system does not interfere with the transfer characteristics of the PLL. Additionally, there is no need for low-frequency bandpass filters and the correcting delay line. For these reasons, autozero is largely preferred over chopping.

One critical circuit element in the autozero system is the IF switch, that has to provide for a sufficient off-state attenuation at high frequencies, apart from the required (intermodulation-free) dynamic range. A finite off-state attenuation causes an offset voltage (or current) relative to the dc component resulting from the desired IF input carrier. With A_{on} the on-state attenuation and A_{off} the off-state attenuation, this relative offset ϵ_{az} is equal to:

$$\epsilon_{az} = \frac{A_{\text{off}}}{A_{\text{on}}} \tag{2.18}$$

Assuming a 0dB on-state attenuation, a 1% relative offset resulting from a 40dB off-state attenuation of the IF autozero switch is completely negligible. Apart from these specifications, the state of the autozero switch must not have any influence of the on the mixer bias and hence the mixer offset, in order to prevent autozero switching induced offset. In Section 3.2, it will be shown that these specifications can be fulfilled with a bipolar long-tailed pair switch with on-chip ac output coupling.

In the synchronous detector, autozero is applied to compensate offset voltages in both the PLL and the AGC loop. Compensation of offset voltages in the AGC loop is necessary in order to guarantee accurate gain control for weak desired IF input carriers. The final synchronous audio detection is performed in a second in-phase path without autozero, in order to obtain an uninterrupted audio signal. Saturation of the audio AGC amplifier by offset voltages can be prevented by ac coupling or dc feedback. The complete synchronous detector with the autozero circuitry is finally shown in Figure 2.6.

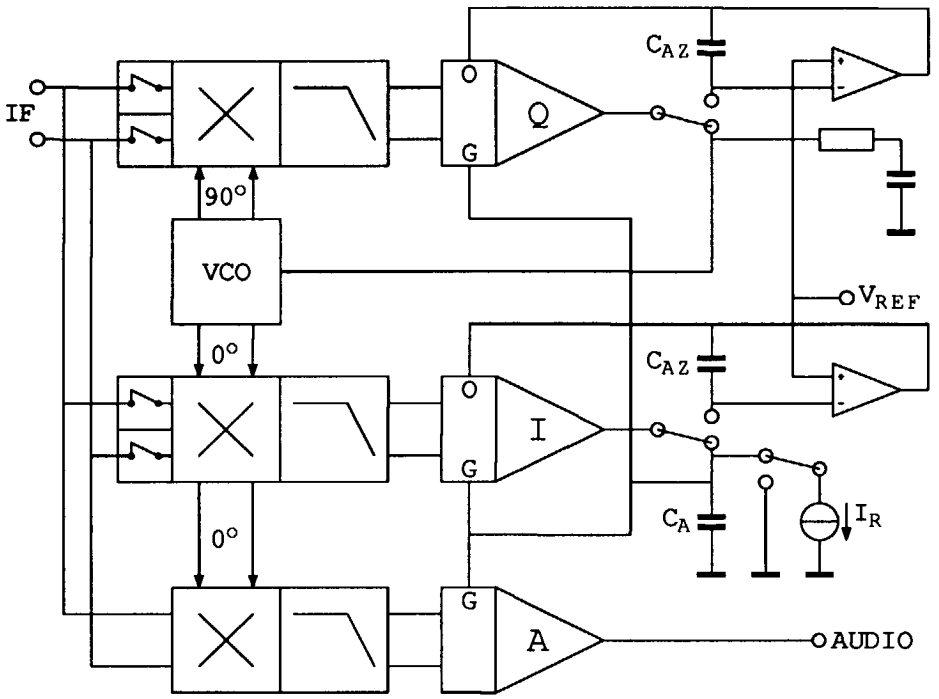

Figure 2.6: Synchronous detector architecture.

2.3 Architecture of the VCO system

In preceding sections, the voltage-controlled oscillator has been displayed as a single block. Actually, this block encloses a complete system, which is built up around a summing loop according to the right hand side of Figure 2.7. The generated output frequency is the sum of (or difference between) a relatively high, accurate and fixed reference frequency f_1 and a relatively low offset frequency f_2. The reference frequency f_1 is derived from the local oscillator reference frequency f_x by a single divide-by-N loop, which is shown in the left hand side of Figure 2.7. Besides, the first local oscillator also encloses a complete synthesiser system. The offset frequency f_2 is generated by a voltage-controlled oscillator. The summing loop provides for a minimum amount of spurious output frequency components.

The summing loop can lock both onto the sum frequency $f_1 + f_2$ and onto the difference frequency $f_1 - f_2$. For both frequencies, the absolute

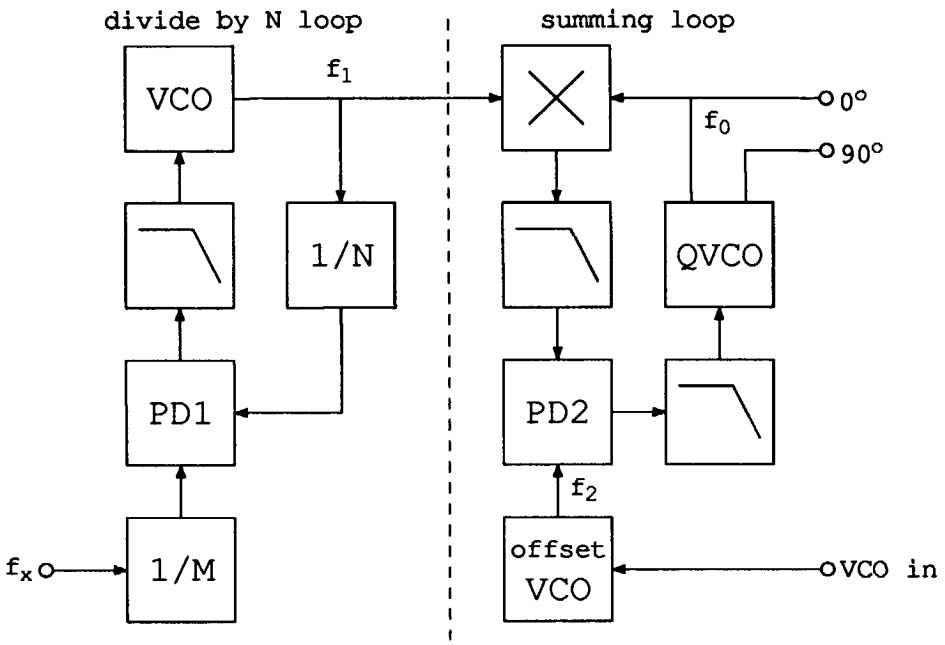

Figure 2.7: Architecture of the VCO system.

inaccuracy of the VCO output frequency is equal to:

$$|\Delta f_V| \leq |\Delta f_1| + |\Delta f_2| \tag{2.19}$$

Since the first local oscillator frequency f_L and the frequency f_1 are derived from the same reference frequency f_x, the initial beat note f_B of the carrier regenerating PLL (see Section 1.6), is calculated as:

$$f_B = |\Delta f_L - \Delta f_1| + |\Delta f_2| \tag{2.20}$$

With $f_1 \approx f_0$, the initial beat note can be written as:

$$f_B = f_R \frac{|\Delta f_x|}{f_x} + |\Delta f_2| \tag{2.21}$$

in which f_R is the received frequency. With an extended capture range of 2kHz (see Section 2.4.4) and a 10ppm tolerance of the reference frequency f_x (see Section 1.6), the maximum inaccuracy of f_2 at the highest RF frequency of 30MHz should not exceed 1.7kHz. If we take a nominal f_2 of 1MHz,

the resulting maximum tolerance of f_2 is 1700ppm. This tolerance can be obtained with a low-cost ceramic resonator.

A detailed description of a similar PLL system can be found in [19]. In that report, it has been shown that the combination of a phase-frequency detector (PFD) and a sample-and-hold phase detector enables a wide-band summing loop with a minimum of spurious output frequency components, while the summing loop can lock onto only one of both frequencies. The advantage of a wide-band summing loop is inherent to the fact that $\mathcal{L}(\Delta f)$ of the quadrature oscillator is reduced for frequencies Δf smaller than the summing loop bandwidth. The required $\mathcal{L}(\Delta f)$, however, can be obtained with on-chip regenerative oscillators [12]. A prototype regenerative quadrature oscillator is described in Section 3.3.

In conclusion, we can state that with the application of the summing loop described above, a critical quartz device for the VCO can be circumvented. The actual VCO is a ceramic resonator oscillator operating on a relatively low frequency.

2.4 Properties of the carrier regenerating PLL

2.4.1 Incremental phase transfer

The VCO tuning voltage V_v as a function of the (small) phase difference between the desired IF input carrier and the VCO output signal $\phi - \phi_0$ can be written as:

$$V_v(s) = \frac{I_R}{sC}\frac{1+sRC}{1+sR_CC_C}(\phi - \phi_0) \tag{2.22}$$

In this equation, R is the loop-filter resistor, C is the loop-filter capacitor, I_R is the AGC reference current, R_C is the mixer collector resistance and C_C is the mixer collector capacitance (see Section 3.1). With a VCO incremental phase transfer equal to:

$$\phi_0 = K_V\frac{V_v}{s}\ , \tag{2.23}$$

in which K_V is the VCO tuning constant (in rad/Vs), the incremental phase transfer of the PLL is calculated as:

$$H_L(s) = \frac{\phi_0(s)}{\phi(s)} = \frac{I_RK_V(1+sRC)}{s^2C(1+sR_CC_C)+I_RK_V(1+sRC)} \tag{2.24}$$

For the PLL incremental phase transfer, three time constants can be

defined:

$$\tau_1^2 = \frac{C}{I_R K_V} \tag{2.25}$$

$$\tau_2 = RC \tag{2.26}$$

$$\tau_3 = R_C C_C \tag{2.27}$$

Using these time constants, the PLL incremental phase transfer can be rewritten into:

$$H_L(s) = \frac{s\tau_2 + 1}{s^3\tau_1^2\tau_3 + s^2\tau_1^2 + s\tau_2 + 1} \tag{2.28}$$

The poles of the PLL can be found with the root locus equation:

$$\frac{s\tau_2 + 1}{s^2(s\tau_3 + 1)} = -\tau_1^2 \tag{2.29}$$

Since the PLL loop has two poles in the origin, the virtual loop gain is represented by the inverse of the time constant τ_1. Depending on the position of the pole represented by τ_3, three possible root loci with parameter τ_1 are drawn in Figure 2.8. The starting points at the poles refer to $\tau_1 \rightarrow \infty$, while the endpoints at the zeros refer to $\tau_1 = 0$.

One preferred pole figure is that with three coincident real poles, shown in root locus B. With τ_l the corresponding time constant, the PLL transfer can be written as:

$$H_L(s) = \frac{s\tau_2 + 1}{s^3\tau_l^3 + 3s^2\tau_l^2 + 3s\tau_l + 1} \tag{2.30}$$

The values of the time constants τ_1, τ_2 and τ_3 as a function of τ_l are calculated as:

$$\tau_1 = \sqrt{3}\tau_l \tag{2.31}$$

$$\tau_2 = 3\tau_l \tag{2.32}$$

$$\tau_3 = \frac{1}{3}\tau_l \tag{2.33}$$

The final PLL incremental phase transfer expressed in τ_l is equal to:

$$H_L(s) = \frac{3s\tau_l + 1}{(s\tau_l + 1)^3} \tag{2.34}$$

For high frequencies ($s\tau_l \gg 1$) , the incremental phase transfer can be approximated by:

$$H_{L\infty}(s) = \frac{3}{s^2\tau_l^2} \tag{2.35}$$

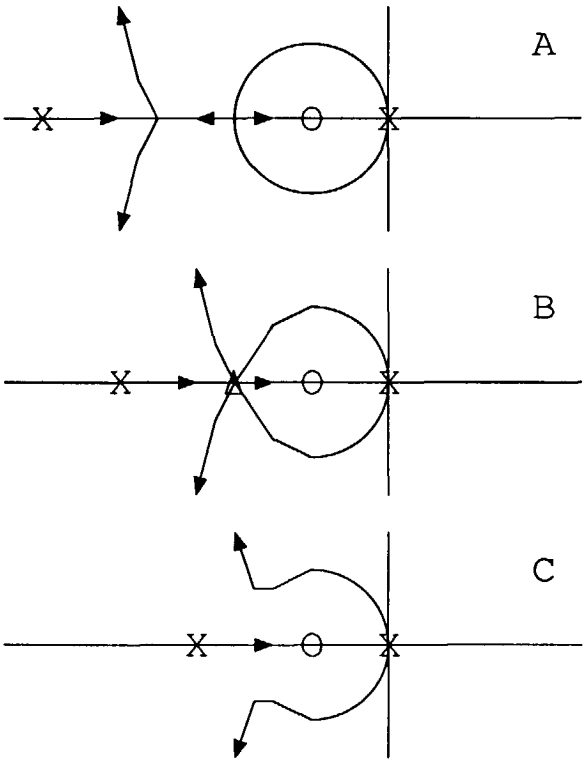

Figure 2.8: Root loci of the PLL.

The noise bandwidth B_L of a PLL is defined as:

$$B_L = \int_0^\infty \frac{|H_L(\omega)|^2}{|H_L(0)|^2} df \tag{2.36}$$

For a third-order type-2 PLL with three equal poles, the noise bandwidth is equal to:

$$B_L = \int_0^\infty \frac{9\omega^2\tau_l^2 + 1}{(\omega^2\tau_l^2 + 1)^3} df \tag{2.37}$$

substituting $\omega\tau_l = x$ results in:

$$B_L = \frac{1}{2\pi\tau_l} \int_0^\infty \frac{9x^2 + 1}{(x^2 + 1)^3} dx = \frac{3}{8\tau_l} \tag{2.38}$$

Evidently, the noise bandwidth is expressed in Hz.

An alternative desired pole figure is a third-order Butterworth configuration with root locus C. In this case, the PLL transfer can be written as:

$$H_L(s) = \frac{s\tau_2 + 1}{s^3\tau_l^3 + 2s^2\tau_l^2 + 2s\tau_l + 1} \tag{2.39}$$

and values of the time constants τ_1, τ_2 and τ_3 as a function of τ_l are calculated as:

$$\tau_1 = \sqrt{2}\tau_l \tag{2.40}$$

$$\tau_2 = 2\tau_l \tag{2.41}$$

$$\tau_3 = \frac{1}{2}\tau_l \tag{2.42}$$

The final PLL incremental phase transfer expressed in τ_l is equal to:

$$H_L(s) = \frac{2s\tau_l + 1}{(s\tau_l + 1)(s^2\tau_l^2 + s\tau_l + 1)} \tag{2.43}$$

For high frequencies ($s\tau_l \gg 1$) , the incremental phase transfer can be approximated by:

$$H_{L\infty}(s) = \frac{2}{s^2\tau_l^2} \tag{2.44}$$

Finally, the noise bandwidth (in Hz) can be calculated as:

$$B_L = \frac{1}{2\pi\tau_l}\int_0^\infty \frac{4x^2 + 1}{(x^6 + 1)}dx = \frac{1}{2\tau_l} \tag{2.45}$$

In order to avoid highly complex poles emerging from component value tolerances, a pole configuration with three coincident poles is slightly preferred over the Butterworth pole configuration.

2.4.2 Interfering carrier suppression

For the calculation of the interfering carrier suppression of the PLL, the IF input signal of the PLL is modelled with a desired and an interfering carrier with a frequency distance equal to $\Delta\omega$:

$$v_i = \hat{v}_1 \sin(\omega t + \phi) + \hat{v}_2 \sin((\omega + \Delta\omega)t) \tag{2.46}$$

Under the condition that $\Delta\omega\tau_l \gg 1$ and the phase modulation of the VCO resulting from the interfering carrier is small, the effect of this phase modulation upon the loop behaviour can be neglected and the output voltage

of the phase detector for a small phase difference $\phi - \phi_0$ (see Section 3.1.1) can be written as:

$$v_Q = \hat{v}_1 G_C(\phi - \phi_o) + \hat{v}_2 G_C \sin(\Delta\omega t) \tag{2.47}$$

The peak phase deviation $\hat{\phi}_m$ of the VCO resulting from the interfering carrier is calculated as:

$$\hat{\phi}_m = \frac{\hat{v}_2 G_C G_A K_V \Delta\omega \tau_2}{\Delta\omega^3 \tau_3 C} \tag{2.48}$$

According to Equation 2.2 in Section 2.1, $\hat{v}_1 G_C G_A = I_R$, so the peak phase deviation results in:

$$\hat{\phi}_m = \frac{\hat{v}_2}{\hat{v}_1} \frac{I_R K_V \Delta\omega \tau_2}{\Delta\omega^3 \tau_3 C} = \frac{\hat{v}_2}{\hat{v}_1} |H_{L\infty}(\Delta\omega)| \tag{2.49}$$

Obviously, the phase modulating frequency is equal to $\Delta\omega$.

The fundamental frequency component of the phase modulated VCO output signal can be written as:

$$v_0 = \hat{v}_0 \sin(\omega_0 t + \hat{\phi}_m \sin(\Delta\omega t) + \phi_0) \tag{2.50}$$

For a small phase deviation $\hat{\phi}_m$, the VCO output signal can be written as:

$$v_0 = \hat{v}_0 \left(\sin(\omega_0 t + \phi_0) - \frac{\hat{\phi}_m}{2} \sin(\omega_0 - \Delta\omega)t + \frac{\hat{\phi}_m}{2} \sin(\omega_0 + \Delta\omega)t \right) \tag{2.51}$$

and the carrier-to-spurious ratio of one spurious component in dB is equal to:

$$\mathrm{CSR}_V = -20 \log \left(\frac{\hat{\phi}_m}{2} \right) = -20 \log \left(\frac{\hat{v}_2}{\hat{v}_1} \right) - 20 \log \left(\frac{1}{2} |H_{L\infty}(\Delta\omega)| \right) \tag{2.52}$$

This results in a PLL adjacent carrier suppression in dB equal to:

$$A_L = -20 \log \left(\frac{1}{2} |H_{L\infty}(\Delta\omega)| \right) \tag{2.53}$$

For a PLL transfer with three coincident real poles and with Butterworth pole positions, the adjacent carrier suppression in terms of τ_l is written as respectively:

$$A_L = 20 \log \left(\frac{2}{3} \Delta\omega^2 \tau_l^2 \right) \tag{2.54}$$

$$A_L = 20 \log \left(\Delta\omega^2 \tau_l^2 \right) \tag{2.55}$$

2.4.3 PLL bandwidth design considerations

For the final value of the time constants, there are two demands to fulfill. The first one of course is the required adjacent carrier suppression of the PLL, that has to be at least twice the required selectivity (see Section 1.7). The second one concerns the suppression of the low-pass filter directly following the mixer. In order to prevent saturation of the AGC amplifier without a large overhead driving capability, the minimum suppression of this filter has to be equal to the desired selectivity.

In order to meet the first demand, the PLL suppression for $\Delta f = 9$kHz and $\Delta f = 45$kHz has to be at least 70dB and 100dB respectively. This results in $\tau_l = 1.4$ms for a PLL with three coincident real poles and $\tau_l = 1.1$ms for a PLL with Butterworth pole positions.

In order to meet the second demand, the suppression of the low-pass filter for $\Delta f = 9$kHz and $\Delta f = 45$kHz has to be at least 35dB and 50dB respectively. This results in $\tau_3 \geq 1.1$ms, irrespective of the PLL transfer characteristic. For a PLL with three coincident real poles, the time constants and the noise bandwidth finally result in:

$$\begin{aligned} \tau_l &= 3.3\text{ms} \\ \tau_1 &= 3.3\sqrt{3}\text{ms} \\ \tau_2 &= 9.9\text{ms} \\ \tau_3 &= 1.1\text{ms} \\ B_L &= 114\text{Hz} \end{aligned}$$

For the PLL with Butterworth pole positions, the time constants and the noise bandwidth finally result in:

$$\begin{aligned} \tau_l &= 2.2\text{ms} \\ \tau_1 &= 2.2\sqrt{2}\text{ms} \\ \tau_2 &= 4.4\text{ms} \\ \tau_3 &= 1.1\text{ms} \\ B_L &= 227\text{Hz} \end{aligned}$$

2.4.4 Extension of the PLL capture range

The small noise bandwidth of the PLL results in a small direct capture range of some 100Hz. Acquisition outside this direct capture range of a third-order PLL is almost impossible, because the required beat note is suppressed

by the low-pass filter directly following the mixer. Since a capture range of some 100Hz results in unrealistic oscillator accuracy specifications (see Section 1.6), this capture range has to be extended. The presence of possible stronger interfering channels exclude the application of many commonly used acquisition methods, like the application of a phase-frequency detector or a wider loop bandwidth during acquisition [20].

A usable acquisition method, the principle of which is shown in Figure 2.9, is based upon scanning of the VCO initial frequency. The required lock detection signal can be derived from the post-detection AGC control signal. As soon as the beat note resulting from a certain VCO initial frequency falls within the direct capture range, the PLL immediately locks and the scanning stops.

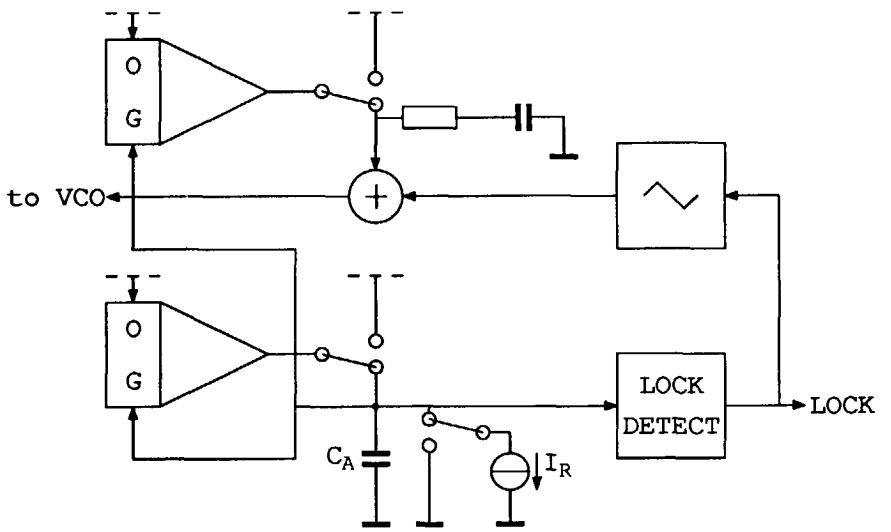

Figure 2.9: Principle of the scanning acquisition method.

The maximum scanning range and hence the maximum capture range, obtained with this scanning method is some kHz. The limitation of the scanning range is inherent to the limitation of the VCO tuning range in order to prevent pulling effects by, or even false lock onto the (possible stronger) adjacent carrier. Although no practical implementation has been made yet, an extension of the single sided capture range amounting to 2kHz may be assumed.

Chapter 3

Design of the synchronous detector HF circuits

This chapter is focussed upon the design of the synchronous mixer, the IF autozero switch and the hf quadrature oscillator.

Section 3.1 deals with the implementation of the synchronous mixer including its IF and VCO input circuitry and its LF output circuitry. The second- and third-order intermodulation free dynamic range (IMFDR) has to be at least 70dB and 77dB respectively in order to provide for the required 50dB stopband selectivity and the required 90dB dynamic range. These specifications have been calculated in Section 1.3 and Section 1.5.

Section 3.2 continues with the implementation of the IF autozero switch. It will be clear that also for the switch in its on state the minimum second- and third-order IMFDR has to be 70dB and 77dB respectively. In its off state the minimum attenuation, calculated in Section 2.2, has to be 40dB.

The implementation of the quadrature oscillator as a part of the VCO system is dealt with in Section 3.3. The elementary architecture of this VCO system can be found in Section 2.3. According to Section 1.7, the minimum CNR of the VCO signal has to be 70dBc/Hz at a frequency distance of 9kHz from the carrier and 85dBc/Hz at a frequency distance more than 45dB from the carrier.

A prototype quadrature oscillator combined with the three mixers including two switches and the driving circuitry has been silicon breadboarded in a 3GHz bipolar process. This prototype and its results will be described in Section 3.4.

3.1 The synchronous mixer

The synchronous mixer, shown in Figure 3.1, is built up around a double balanced long-tailed pair switching mixer. The IF input signal including the bias tail current is obtained from a transadmittance amplifier, which is implemented as a balanced series stage. The VCO signal is obtained from the quadrature oscillator via a single limiter stage, that provides for a square wave with sufficiently steep edges. The passive low-pass RC filter in the collector circuit of the mixer suppresses unwanted high frequency

components that might produce severe intermodulation distortion in the subsequent low-frequency circuitry.

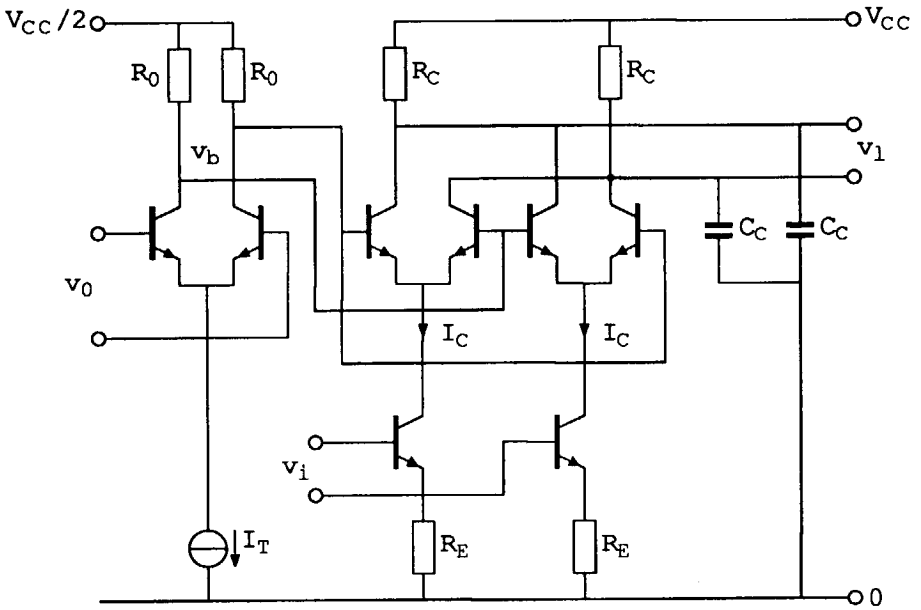

Figure 3.1: Implementation of the synchronous mixer.

The nominal conversion gain of the synchronous mixer is calculated in Subsection 3.1.1. In Subsection 3.1.2, the switching behaviour of the synchronous mixer is analysed in order to calculate the switching induced mixer distortion. The results of this analysis are also used for the calculation of the mixer noise in Subsection 3.1.3. Finally, the distortion and subsequently the IMFDR of the complete synchronous mixer is calculated in Subsection 3.1.4.

3.1.1 Synchronous mixer transfer

For an ideal switching mixer, the output signal is the product of the input IF signal and the normalised oscillator signal, being a square wave with an amplitude equal to 1. This normalised oscillator signal can be represented by its Fourier series:

$$v_b(t) = \frac{4}{\pi} \sum_{n=1}^{\infty} \frac{1}{2n-1} \cos[(2n-1)(\omega_0 t - \phi_0)] \tag{3.1}$$

For the IF input signal, an AM modulated desired carrier and an AM modulated adjacent carrier is taken:

$$\begin{aligned} v_i(t) &= \hat{v}_{i1}\{1 + m\sin(\mu_1 t)\}\cos(\omega_0 t + \phi) \\ &+ \hat{v}_{i2}\{1 + m\sin(\mu_2 t)\}\cos((\omega_0 + \Delta\omega)t) \end{aligned} \tag{3.2}$$

The modulation depths of both carriers are assumed to be equal.

The relevant low-frequency output product terms (see also Section 1.2) can be written as:

$$\begin{aligned} v_o(t) &= G_C\hat{v}_{i1}\{1 + m\sin(\mu_1 t)\}\cos(\phi - \phi_0) \\ &+ G_C\hat{v}_{i2}\{1 + m\sin(\mu_2 t)\}\cos(\Delta\omega t - \phi_0) \end{aligned} \tag{3.3}$$

The double frequency terms and the terms resulting from the oscillator harmonics are completely suppressed by the subsequent low-pass filter. The conversion gain G_C of the mixer is equal to:

$$G_C = \frac{2}{\pi}\frac{g_m R_C}{g_m R_E + 1} \tag{3.4}$$

in which $g_m = I_C/V_T$ is the transconductance of the transistor in the series stage. For $g_m R_E \gg 1$ the conversion gain can be written as:

$$G_C = \frac{2}{\pi}\frac{R_C}{R_E} \tag{3.5}$$

For the phase detector mixer, which is driven by the quadrature oscillator signal, the relevant low-frequency product terms can be written as:

$$\begin{aligned} v_o(t) &= G_C\hat{v}_{i1}\{1 + m\sin(\mu_1 t)\}\sin(\phi - \phi_0) \\ &+ G_C\hat{v}_{i2}\{1 + m\sin(\mu_2 t)\}\sin(\Delta\omega t - \phi_0) \end{aligned} \tag{3.6}$$

For small phase differences, $\sin(\phi - \phi_0) \approx \phi - \phi_0$.

The power transfer of the synchronous mixer for the desired channel can be calculated as:

$$\frac{P_o}{P_{i1}} = 2G_C^2\cos^2(\phi - \phi_0) \tag{3.7}$$

For the adjacent channel however the power transfer is equal to:

$$\frac{P_o}{P_{i2}} = G_C^2 \tag{3.8}$$

As a result of the correlation of the oscillator signal with the desired channel signal, a 3dB power gain of the desired channel can be obtained if $\phi = \phi_0$. In this case, the power ratio between the desired audio signal P_a and the (9kHz) beat note P_b resulting from the adjacent carrier is equal to:

$$\frac{P_a}{P_b} = \frac{m^2 \hat{v}_{i1}^2}{\hat{v}_{i2}^2} \tag{3.9}$$

For a modulation depth of 30%, the level ratio between the desired audio signal and the beat note is 10dB less than the level ratio between the desired and the adjacent carrier.

For the conversion of IF noise, the IF noise spectrum is assumed to be white within a certain bandwidth around ω_0 covering the input passband of the synchronous detector. The IF noise can be described as a collection of interfering carriers each with random amplitude and phase. Each noise component can be described as:

$$v_{ni}(t) = \hat{v}_n \cos(\omega_0 + \delta\omega_n t + \phi_n) \tag{3.10}$$

Both the noise component with angular frequency $\omega_0 + \delta\omega_n$ (upper sideband) and the noise component with angular frequency $\omega_0 - \delta\omega_n$ (lower sideband) are converted to a low-frequency noise component with angular frequency $\delta\omega_n$. Since both noise components are uncorrelated, their mean square values must be added, which results in the low-frequency noise component:

$$v_{no}(t) = \sqrt{2}\hat{v}_n G_C \cos(\delta\omega_n t + \phi_n - \phi_0) \tag{3.11}$$

If we describe the noise in terms of spectral densities, the LF output noise density can be written as:

$$S(V_{no}) = 2G_C^2 S(V_{ni}) \tag{3.12}$$

The noise power conversion gain is equal to the desired channel conversion gain with $\phi = \phi_0$.

In order to calculate the equivalent input noise voltage (or current) of the mixer (or another IF circuit), the effect of a 3dB power gain of the desired signal in combination with the loss of conversion gain if $\phi \neq \phi_0$ can be incorporated in an effective IF noise bandwidth B_{IF} of the synchronous detector. With a given LF noise bandwidth B_{LF}, the IF noise bandwidth is calculated as:

$$\frac{\hat{v}_{i1}^2}{2S(V_{ni})B_{IF}} = \frac{G_C^2 \cos^2(\phi - \phi_0)\hat{v}_{i1}^2}{S(V_{no})B_{LF}} \tag{3.13}$$

The left hand part of this equation expresses the IF carrier-to-noise ratio in the equivalent IF noise bandwidth B_{IF}, while the right hand part expresses the LF signal-to-noise ratio in the given LF noise bandwidth B_{LF}, in which the LF (dc) signal is the converted IF carrier. With $S(V_{no})$ calculated according to Equation 3.12, the equivalent IF noise bandwidth results in:

$$B_{IF} = \frac{B_{LF}}{\cos^2(\phi - \phi_0)} \tag{3.14}$$

which is equal to B_{LF} if $\phi = \phi_0$.

The oscillator harmonics will also convert noise into the passband of the low-pass filter. For a square wave oscillator signal, the power ratio between the harmonics and the fundamental frequency component is about 0.25. If we assume a white IF noise spectrum, the VCO harmonics increase the total LF noise power in the low-frequency noise bandwidth B_{LF} with 25% or 1dB. If this effect is incorporated in the equivalent IF noise bandwidth B_{IF}, this equivalent IF noise bandwidth is 25% larger than calculated in Equation 3.14.

3.1.2 Synchronous mixer switching behaviour

This section deals with the switching behaviour of the synchronous mixer according to Figure 3.1. The mixer switching time, during which the mixer changes its state is assumed to be much smaller than the period of the VCO signal. In this case, this transition time has no significant effect upon the nominal mixer conversion gain, calculated in the previous subsection. For high frequencies, the collectors are regarded as virtually grounded by the capacitors C_C of the subsequent low-pass filter.

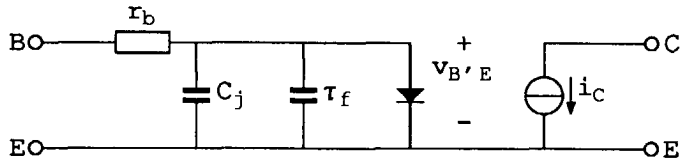

Figure 3.2: Simplified large signal model of a NPN transistor

For calculation purposes, the transistors are modelled with a simplified large signal model according to Figure 3.2. In this figure, r_b denotes the ohmic base resistance, C_j denotes the base-emitter junction capacitance and τ_f is the transit time. Since the collectors are virtually grounded for high frequencies, the collector-base junction capacitance is incorporated in the

junction capacitance C_j. With $v_{B'E}$ the instantaneous intrinsic base emitter voltage and i_C the instantaneous collector current, the instantaneous large signal base current i_B is equal to:

$$i_B = \frac{i_C}{\beta_{f0}} + \tau_f \frac{di_C}{dt} + C_j \frac{dv_{B'E}}{dt} \tag{3.15}$$

in which β_{f0} is the dc current gain. For the calculation of the mixer switching behaviour, the static base current component can be neglected. Numerical values of the main transistor parameters of the transistors used in the prototype mixer are listed in Table 3.1 on page 75.

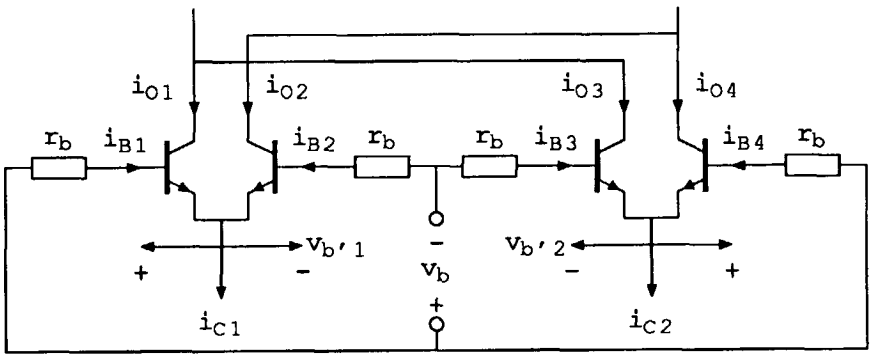

Figure 3.3: Calculation scheme for the switching behaviour of the mixer. The base resistances are drawn external to the transistors.

The dynamic behaviour of the mixer, for which the calculation scheme is shown in Figure 3.3, is described by the equations:

$$i_{B1} - i_{B2} = \tau_f \frac{d(i_{O1} - i_{O2})}{dt} + C_j \frac{dv_{b'1}}{dt} \tag{3.16}$$

$$i_{B4} - i_{B3} = \tau_f \frac{d(i_{O4} - i_{O3})}{dt} + C_j \frac{dv_{b'2}}{dt} \tag{3.17}$$

The instantaneous mixer tail currents i_{C1} and i_{C2} are the sum of a bias current I_C and a signal current i_c:

$$i_{C1} = I_C + i_c \tag{3.18}$$

$$i_{C2} = I_C - i_c \tag{3.19}$$

The voltages $v_{b'1}$ and $v_{b'2}$ denote the differential intrinsic base voltages, which can be expressed as:

$$v_{b'1} = \ln\left(\frac{i_{O1}}{i_{O2}}\right) \tag{3.20}$$

$$v_{b'2} = \ln\left(\frac{i_{O4}}{i_{O3}}\right) \tag{3.21}$$

The differential collector currents of each mixer half as a function of the differential base voltages are calculated as:

$$i_{O1} - i_{O2} = \{i_{C1} - (i_{B1} + i_{B2})\} \tanh\left(\frac{v_{b'1}}{2V_T}\right) \tag{3.22}$$

$$i_{O4} - i_{O3} = \{i_{C2} - (i_{B1} + i_{B2})\} \tanh\left(\frac{v_{b'2}}{2V_T}\right) \tag{3.23}$$

If the mixer operates in its final state, the static base currents of the mixer transistors can be neglected provided that the tail current I_T of the mixer driver for the VCO signal is sufficiently large. Generally, this tail current is in the order of magnitude of the mixer bias current I_C or even higher in order to obtain a sufficiently small switching time. In this case, the peak value of the differential extrinsic base voltage $\hat{v}_b = I_T R_0$. The differential collector currents in the final state can be written as:

$$i_{O1} - i_{O2} = i_{C1} \tanh\left(\frac{v_{b'1}}{2V_T}\right) \tag{3.24}$$

$$i_{O4} - i_{O3} = i_{C2} \tanh\left(\frac{v_{b'2}}{2V_T}\right) \tag{3.25}$$

If we temporarily disregard the influence of the junction capacitances C_j, the dynamic behaviour of the mixer is described by the equations:

$$i_{B1} - i_{B2} = \tau_f \frac{d(i_{O1} - i_{O2})}{dt} \tag{3.26}$$

$$i_{B4} - i_{B3} = \tau_f \frac{d(i_{O4} - i_{O3})}{dt} \tag{3.27}$$

Since the base currents are proportional with the slope of the collector currents, these base currents are in balance ($i_{B1} = -i_{B2}$ and $i_{B3} = -i_{B4}$), so Equation 3.24 and Equation 3.25 are also valid under dynamic operation. Provided that $I_T R_0 \gg V_T$, the differential intrinsic base voltage under dynamic operation is much smaller than $I_T R_0$ and each base current can be regarded as a constant current. The magnitude $\hat{i}_b$ of each base current under dynamic operation is calculated as:

$$\hat{i}_b = \frac{I_T}{2} \frac{R_0}{r_b + 2R_0} \tag{3.28}$$

The resulting dynamic behaviour of the mixer is described as:

$$2\hat{i}_b = \tau_f \frac{d(i_{O1} - i_{O2})}{dt} \tag{3.29}$$

$$2\hat{i}_b = \tau_f \frac{d(i_{O4} - i_{O3})}{dt} \tag{3.30}$$

The resulting collector currents of one mixer half, having a constant slope during the transition of the mixer state, are shown in the left hand part of Figure 3.4. The tail currents i_{C1} and i_{C2} are regarded as practically constant during the transition of the mixer state.

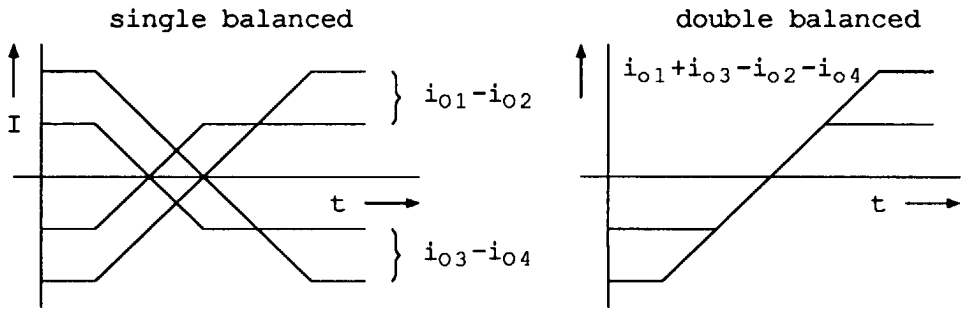

Figure 3.4: Collector currents of the mixer during transition of state if the influence the junction capacitances is disregarded. The curves are drawn for two different values of the tail current.

The switching times of both mixer halves are proportional with the corresponding tail currents. These switching times, t_{s1} of the left mixer half and t_{s2} of the right mixer half, are calculated as:

$$t_{s1} = \frac{\tau_f i_{C1}}{\hat{i}_b} = \frac{\tau_f (I_C + i_c)}{\hat{i}_b} \tag{3.31}$$

$$t_{s2} = \frac{\tau_f i_{C2}}{\hat{i}_b} = \frac{\tau_f (I_C - i_c)}{\hat{i}_b} \tag{3.32}$$

For the double balanced mixer, no effect upon the output current is observed during the time t_{s2} in which both mixer halves change their state. The output current changes during the time $t_{s1} - t_{s2}$, in which the mixer half with the lower tail current has already reached its final state, while the mixer half with the higher tail current still changes its state. The collector currents of the double balanced mixer are shown in the right hand part of

Figure 3.4. The resulting switching time t_s is calculated as:

$$t_s = t_{s1} - t_{s2} = \frac{2\tau_f |i_c|}{\hat{i}_b} \tag{3.33}$$

Figure 3.5 shows the results of a SPICE simulation of the mixer according to the calculation scheme in Figure 3.3, in which the transistors are modelled according to Figure 3.2 and the junction capacitances are omitted. The upper curves indicate the mixer output current, while the lower curves indicate the differential intrinsic base voltages for different values of the signal current i_c. The simulated slopes of the output currents are practically constant.

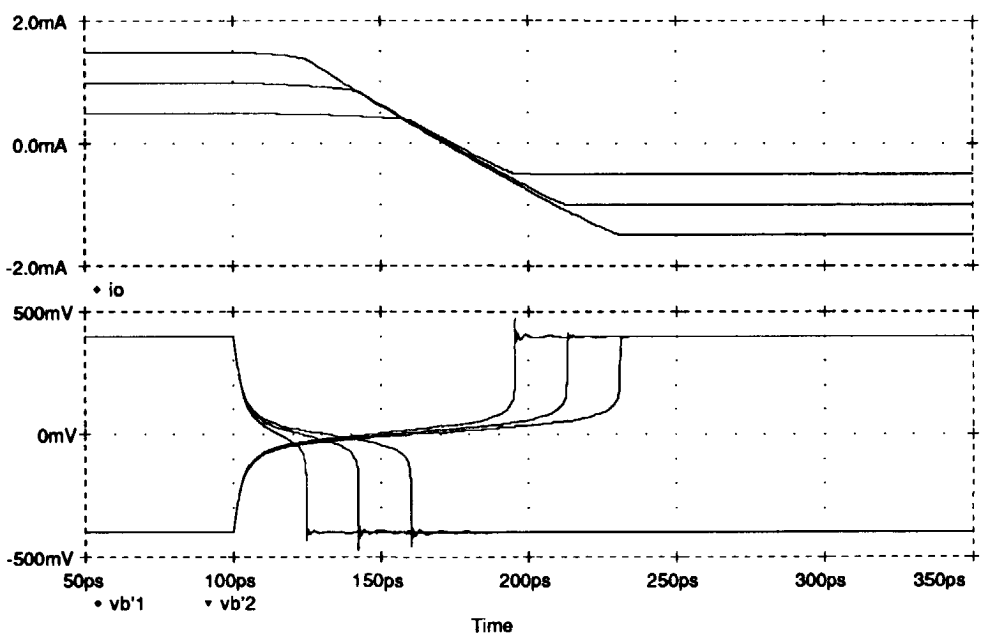

Figure 3.5: Spice simulation of the switching behaviour of the mixer in which the influence of the junction capacitances is disregarded.

In this simulation, $r_b = 300\Omega$, $\tau_f = 47$ps (see Table 3.1 on page 75) and $I_C = 1$mA. The VCO signal is obtained from a square wave voltage source with an amplitude $\hat{v}_b = 0.4$V, so $\hat{i}_b = \hat{v}_b / 2r_b = 0.67$mA. For the applied signal current i_c with values of 0.25mA, 0.5mA and 0.75mA, the switching times according to Equation 3.33 are equal to 35ps, 71ps and

106ps respectively. These calculated values of the switching time t_s are in close agreement with the simulated ones.

The dependency of the switching time resulting from τ_f on the signal current causes distortion. According to [2, Ch. 3], where a similar calculation is performed, the third-order intermodulation distortion resulting from this switching effect can be expressed as:

$$\mathrm{IM}_3 = \frac{1}{2}\left(\frac{\omega_0 \tau_f \hat{i}_c}{2\hat{i}_b}\right)^2 \tag{3.34}$$

For this equation, the instantaneous signal current $|i_c|$ is assumed to be practically equal for both the positive and for the negative edge of the oscillator signal. This assumption is valid if either the tail signal current frequency is much lower than the oscillator frequency (eg. the upconversion mixer) or the tail signal current frequency is in the close proximity of the oscillator frequency (the synchronous mixer).

At relatively low tail bias currents, the junction capacitances have a significant influence upon the switching behaviour of the mixer. Calculation of the switching behaviour under this circumstance appears to be very complex. During dynamic operation, the base currents are not in balance, so Equation 3.24 and Equation 3.25 are no longer valid. Additionally, the base currents cannot be regarded as a constant current. However, we can compare the effect of τ_f and the junction capacitances C_j by the total charge transfer during a transition of the mixer state. This total charge transfer of one mixer half is calculated as:

$$\Delta q = \tau_f i_C + \hat{v}_b C_j \tag{3.35}$$

Although the junction capacitances increase the total charge Δq to be transferred and hence the switching time, the charge transfer involved with the junction capacitances is independent of the mixer tail current. Theoretically, the dependency of Δq and also the switching time upon the tail signal current would not be effected by the junction capacitances.

Figure 3.6 shows the results of a second SPICE simulation, in which a junction capacitance $C_j = 0.1\mathrm{pF}$ is included, while all other circumstances are the same as in the previous one. The junction capacitances, for which value $r_b C_j = 30\mathrm{ps}$, have a large influence upon the switching behaviour of the mixer. Although the switching time of the mixer is increased, the dependency of this switching time upon the signal current is practically the same as that in the previous SPICE simulation. Under the condition that

the switching time is small compared with the oscillator period, the junction capacitances have no significant influence upon the switching induced mixer distortion according to Equation 3.34.

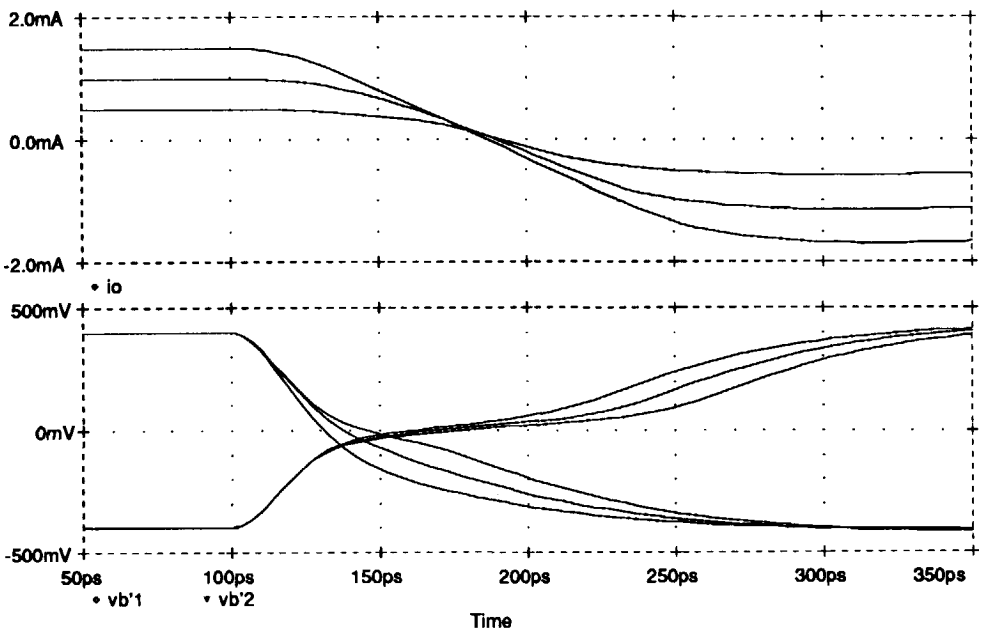

Figure 3.6: Spice simulation of the switching behaviour of the mixer including the effect of the junction capacitances.

The mixer switching behaviour in this subsection was calculated under the condition that the mixer transition time is determined by the mixer itself rather than that by the finite rise and fall time of the oscillator signal. In other words:

$$\frac{dv_b}{dt} \gg \frac{dv_{b'}}{dt} \tag{3.36}$$

The average slope of the differential intrinsic base voltage $v_{b'}$ around $v_{b'} = 0$ can be approximated by:

$$\frac{dv_{b'}}{dt} = \frac{2\hat{i}_b}{C_j + \tau_f I_C / 2V_T} \tag{3.37}$$

in which $\tau_f I_C / 2V_T$ is the so-called diffusion capacitance.

For the limiter stage driving the oscillator input of the mixer (see Figure 3.1), the slope of the collector voltage v_b at its differential intrinsic base

voltage $v_{0'} = 0$ is calculated as:

$$\frac{dv_b}{dt} = \frac{I_T}{2V_T}\frac{dv_{0'}}{dt}\frac{r_b R_0}{r_b + 2R_0} = \frac{\hat{i}_b r_b}{V_T}\frac{dv_{0'}}{dt} \tag{3.38}$$

Now the slope of $v_{0'}$ has to fulfill the relation:

$$\frac{dv_{0'}}{dt} \gg \frac{2V_T}{r_b(C_j + \tau_f i_C/2V_T)} \tag{3.39}$$

under the condition that the amplitude of the oscillator signal $\hat{v}_0 \gg V_T$.

3.1.3 Mixer noise

In this subsection, the equivalent IF input noise voltage of the complete mixer according to Figure 3.1 will be calculated.

The noise sources in the series stage, shown in Figure 3.7, are the base current shot noise, I_{nb}, the collector current shot noise I_{nc}, the thermal noise of the base resistance V_{nb} and the thermal noise of the emitter resistance V_{ne}.

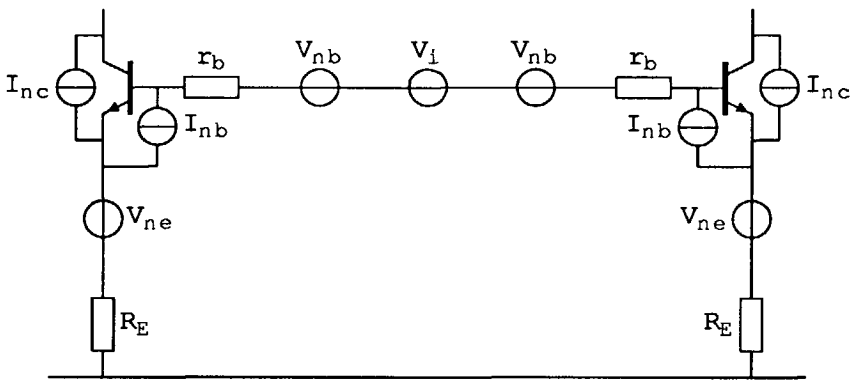

Figure 3.7: Noise sources in the series stage. The base resistances are drawn external to the transistors.

The spectral densities of the noise sources in Figure 3.7 are equal to:

$$S(I_{nb}) = 2qI_B = \frac{2kTg_m}{B_F} \tag{3.40}$$

$$S(I_{nc}) = 2qI_C = 2kTg_m \tag{3.41}$$

$$S(V_{nb}) = 4kTr_b \tag{3.42}$$

$$S(V_{ne}) = 4kTR_E \tag{3.43}$$

In these equations, g_m is the small signal transconductance, B_F is the large signal current gain and r_b is the ohmic base resistance. These noise sources can be replaced by an equivalent input noise voltage V_{ni} in series with V_i, which is calculated as (see also [21, Ch. 3]):

$$S(V_{ni}) = 8kT\left[R_E + r_b + \frac{1}{2g_m} + \frac{g_m}{2}\left(\frac{1}{B_F} + \frac{f^2}{f_T^2}\right)(r_b + R_E)^2\right] \quad (3.44)$$

in which f_T is the transit frequency. With $g_m R_E \gg 1$, $B_F = 130$, $f_T \approx$ 3GHz and $f \approx$ 70MHz the expression of the equivalent input noise voltage can be reduced to:

$$S(V_{ni}) = 8kT(R_E + r_b)\left(1 + \frac{g_m(r_b + R_E)}{2B_F}\right) \quad (3.45)$$

The noise sources in the mixer, shown in Figure 3.8, are the collector current shot noise, the base current shot noise, and the thermal noise of the base resistances.

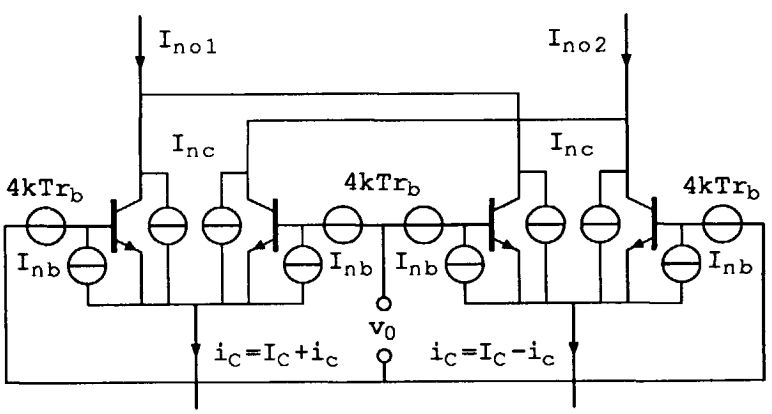

Figure 3.8: Noise sources in the mixer.

If we consider a static situation the output noise current of the mixer can be described as (see also [1, Section 3.2]):

$$S(I_{no1} - I_{no2}) = 4qI_B x^2 + 4qI_C(1 - x^2) + \frac{4qr_b I_C^2}{V_T}(1 + y^2)(1 - x^2) \quad (3.46)$$

In this equation, I_C denotes the tail bias current, I_B denotes the static base current, x is the state of the mixer determined by the intrinsic differential base voltage $v_{b'}$:

$$x = \tanh\left(\frac{v_{b'}}{2V_T}\right) \quad (3.47)$$

and y is the relative tail signal current i_c/I_C. According to [1, Section 3.2.1], the noise under dynamic operation is found by substituting the variables $x = x(t)$ and $y = y(t)$ in the noise spectrum in Equation 3.46 and taking the time average of this spectrum.

For an ideal switching mixer, $x^2 = 1$ and the output noise is caused by the base current shot noise only.

$$S(I_{no1} - I_{no2}) = 4qI_B = \frac{4qI_C}{B_F} \tag{3.48}$$

This minimum noise level corresponds to the noise of a balanced CB stage. For a practical switching mixer the output noise current during the final state is determined by the base current shot noise only, provided that the local oscillator voltage amplitude $\hat{v}_b > 8V_T$ (see also [1, Ch. 3]).

Additional output noise caused by the collector current shot noise or the thermal noise of the base resistances is generated during the transition of the mixer state. With F_m the mixer noise figure due to the nonzero transition time, the mixer noise can be written as:

$$S(I_{no1} - I_{no2}) = \frac{4qI_C}{B_F} F_m \tag{3.49}$$

If we assume a small signal level ($|y(t)| \ll 1$), the noise figure can be written as:

$$F_m = 1 + B_F \left(1 + \frac{r_b I_C}{V_T}\right) \overline{(1 - x^2(t))} \tag{3.50}$$

According to Section 3.1.2, the slope of the intrinsic oscillator voltage $v_{b'}$ around the transition point $v_{b'} = 0$ is equal to:

$$\frac{dv_{b'}}{dt} = \frac{2\hat{i}_b}{C_j + \tau_f I_C/2V_T} \tag{3.51}$$

and $1 - x^2(t)$ during a transition can be approximated by:

$$1 - x^2(t) = 1 - \tanh^2\left(\frac{2\hat{i}_b t}{2V_T C_j + \tau_f I_C}\right) = \cosh^{-2}\left(\frac{2\hat{i}_b t}{2V_T C_j + \tau_f I_C}\right) \tag{3.52}$$

During one local oscillator period, two transitions occur. If we assume a transition time smaller than the local oscillator period, each transition can be regarded as an independent event, which results in:

$$\overline{1 - x^2(t)} = 2f_0 \int_{-\infty}^{\infty} \cosh^{-2}\left(\frac{2\hat{i}_b t}{2V_T C_j + \tau_f I_C}\right) dt = \frac{2f_0(2V_T C_j + \tau_f I_C)}{\hat{i}_b} \tag{3.53}$$

Similar calculations in [1, Section 3.2.2] practically give the same result. Now the noise figure is finally written as:

$$F_m = 1 + B_F(1 + g_m r_b)\frac{2f_0(2V_T C_j + \tau_f I_C)}{\hat{i}_b} \tag{3.54}$$

The equivalent input noise voltage of the complete synchronous mixer can be calculated as:

$$V_{ni}^2 = 8kT\left[(R_E + r_b)\left(1 + \frac{g_m(r_b + R_E)}{2B_F}\right) + \frac{\pi^2 F_m g_m R_E^2}{8B_F} + \frac{\pi^2 R_E^2}{8R_C}\right] B_{IF} \tag{3.55}$$

In this equation, the last term expresses the noise caused by the collector resistors R_C. The IF noise bandwidth B_{IF} is given by Equation 3.14.

If the numerical value of the mixer noise figure $F_m \gg 1$ (see Section 3.4), the base current shot noise of the series stage can be neglected. With $R_E \gg r_b$ and $R_C \approx R_E$, Equation 3.55 can be simplified to:

$$V_{ni}^2 = 8kTR_E\left(2 + \frac{\pi^2 F_m g_m R_E}{8B_F}\right) B_{IF} \tag{3.56}$$

If also $F_m g_m R_E \gg B_F$, this equation can be further reduced to:

$$V_{ni}^2 = \frac{\pi^2 kT F_m g_m R_E^2}{B_F} B_{IF} \tag{3.57}$$

In this case, the equivalent input noise voltage is completely determined by the noise of the synchronous mixer itself.

3.1.4 Mixer distortion

In this subsection, the total distortion of the synchronous mixer is calculated as the sum of the distortion generated when the mixer operates in its final state and the distortion generated during the transition of state. In its final state, the synchronous mixer operates as a balanced common-base stage driven by a balanced series stage. The dominating distortion mechanism in these local feedback stages is caused by the fundamental exponential relation between the intrinsic base-emitter voltage and the collector current [2, Ch. 3]. The intermodulation generated by this distortion mechanism will be calculated for the series stage shown in Figure 3.9. The results are also valid for a common-base stage and an emitter follower as well.

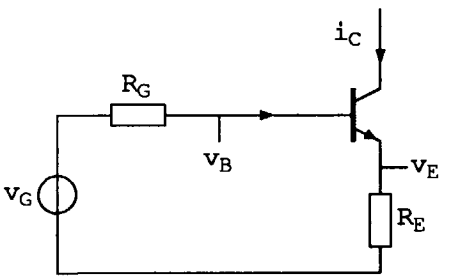

Figure 3.9: Calculation of the distortion of a series stage.

The large signal behaviour of a single ended series stage according to Figure 3.9 can be described as:

$$v_G = i_C R_E + i_B(r_b + R_G) + V_T \ln(\frac{i_C}{I_S}) \tag{3.58}$$

in which I_S denotes the saturation current of the transistor, $i_C = I_C + i_c$ denotes the instantaneous collector current and $v_G = V_G + v_g$ denotes the instantaneous input voltage. If $R_G \ll \beta_f R_E$ and $r_b \ll \beta_f R_E$, the influence of the base current can be neglected. If also $V_E = I_C R_E \gg V_T$ and $i_c < I_C$, the collector current can be approximated by a Taylor series until the third order:

$$i_C = I_C + \frac{di_C}{dv_G} v_g + \frac{1}{2}\frac{d^2 i_C}{dv_G^2} v_g^2 + \frac{1}{6}\frac{d^3 i_C}{dv_G^3} v_g^3 \tag{3.59}$$

The bias component I_C is given by:

$$V_G = I_C R_E + V_T \ln\left(\frac{I_C}{I_S}\right) \tag{3.60}$$

and the Taylor coefficients are calculated as:

$$\frac{di_C}{dv_G} = \frac{1}{R_E} \tag{3.61}$$

$$\frac{d^2 i_C}{dv_G^2} = \frac{V_T}{R_E V_E^2} \tag{3.62}$$

$$\frac{d^3 i_C}{dv_G^3} = \frac{-2V_T}{R_E V_E^3} \tag{3.63}$$

This results in the large signal transfer:

$$\frac{i_c}{I_C} = \frac{v_g}{V_E} + \left(\frac{v_g}{V_E}\right)^2 \frac{V_T}{2V_E} - \left(\frac{v_g}{V_E}\right)^3 \frac{V_T}{3V_E} \tag{3.64}$$

For a balanced series stage, the second-order distortion is cancelled out. The third-order intermodulation of the balanced series stage as a function of the collector current amplitude $\hat{i}_c$ is equal to:

$$\mathrm{IM}_{3a} = \frac{V_T}{4V_E}\frac{\hat{i}_c^2}{I_C^2} \tag{3.65}$$

The intermodulation as a function of the IF differential input voltage amplitude can be found by substituting $\hat{i}_c = \hat{v}_i/2R_E$.

The impedance at the emitters of the long-tailed pair mixer is equal to the output impedance of the series stage. At high frequencies, this output impedance is determined by the sum of collector-base capacitance and the collector-substrate capacitance, indicated by C_c. When the mixer operates in its final state, the third-order intermodulation (see also [2, Section 3.5]) can be calculated as:

$$\mathrm{IM}_{3b} = \frac{\omega_0 C_c V_T}{4I_C}\frac{\hat{i}_c^2}{I_C^2} \tag{3.66}$$

The ratio between the third-order intermodulation IM_{3b} of the mixer in its final state and the third-order intermodulation IM_{3a} of the series stage is equal to:

$$\frac{\mathrm{IM}_{3b}}{\mathrm{IM}_{3a}} = \omega_0 R_E C_c \tag{3.67}$$

According to Section 3.1.2, the third-order distortion of the mixer generated during the transitions of state was calculated as:

$$\mathrm{IM}_{3c} = \frac{1}{2}\left(\frac{\omega_0 \tau_f \hat{i}_c}{2\hat{i}_b}\right)^2 \tag{3.68}$$

If we compare the third-order intermodulation IM_{3c} of the mixer generated during the transition of state with the third-order intermodulation IM_{3b} of the mixer operating in its final state, we obtain:

$$\frac{\mathrm{IM}_{3c}}{\mathrm{IM}_{3b}} = \frac{\omega_0 \tau_f^2 I_C^3}{2V_T \hat{i}_b^2 C_c} \tag{3.69}$$

Figure 3.10 shows the three calculated intermodulation components of the complete synchronous mixer as a function of the IF central frequency f_0. Numerical calculations in Section 3.4 show that the intermodulation of the prototype synchronous mixer at the IF central frequency $f_0 = 70\mathrm{MHz}$ with a collector bias current $I_C = 0.8\mathrm{mA}$ is determined by that of the series

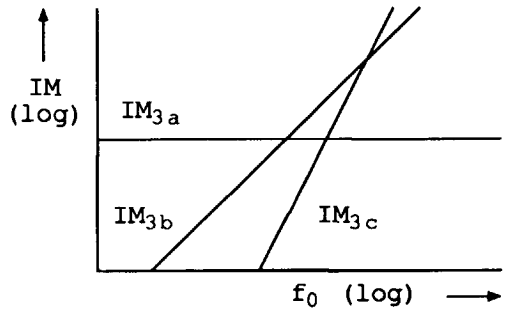

Figure 3.10: Third-order intermodulation components of the synchronous mixer including the series stage as a function of the IF central frequency f_0.

stage. Additionally, the mixer distortion generated during the transition of state is negligible compared with the mixer distortion in the final state.

According to Section 1.5, the third-order IMFDR of the synchronous mixer including the series stage is calculated as:

$$\mathrm{IMFDR_3} = -\frac{1}{3}\mathrm{IM_3} + \frac{2}{3}\mathrm{CNR} \tag{3.70}$$

Provided that the distortion generated during the transition of state can be neglected, the third-order intermodulation distortion is calculated as:

$$\mathrm{IM_{3ab}} = 20\log\left(\frac{V_T}{8V_E^3}\sqrt{(1+\omega_0^2 R_E^2 C_c^2)}\,V_i^2\right) \tag{3.71}$$

If the mixer noise according to Section 3.1.3 is determined by the synchronous mixer itself, the equivalent input noise voltage is equal to:

$$V_{ni}^2 = \frac{\pi^2 kTF_m g_m R_E^2}{B_F} B_{IF} = \frac{\pi^2 kTF_m I_C R_E^2}{B_F V_T} B_{IF} \tag{3.72}$$

The third-order IMFDR finally results in:

$$\mathrm{IMFDR_3} = 20\log\sqrt[3]{\frac{8I_C^2 R_E B_F}{\pi^2 kTF_m B_{IF}\sqrt{1+\omega_0^2 R_E^2 C_s^2}}} \tag{3.73}$$

As long as $\omega_0 R_E C_c < 1$, the distortion of the series stage dominates over the mixer distortion in the final state and the IMFDR of the mixer can be increased by increasing the emitter resistor R_E. Numerical values of the IMFDR can be found in Section 3.4.

3.2 Implementation of the IF switch

In this section, two possible implementations of the IF switch are presented. In the first one, the switching element is a bipolar long-tailed pair switch according to the left hand part of Figure 3.11. In the second one a CMOS transmission gate is applied as a switching element. The transmission gate including its driving inverters is shown in the right hand part of Figure 3.11. In two successive subsections, the off-state attenuation and the IMFDR of the IF switch built up around a bipolar long-tailed pair switch and the IF switch built up with transmission gates will be calculated.

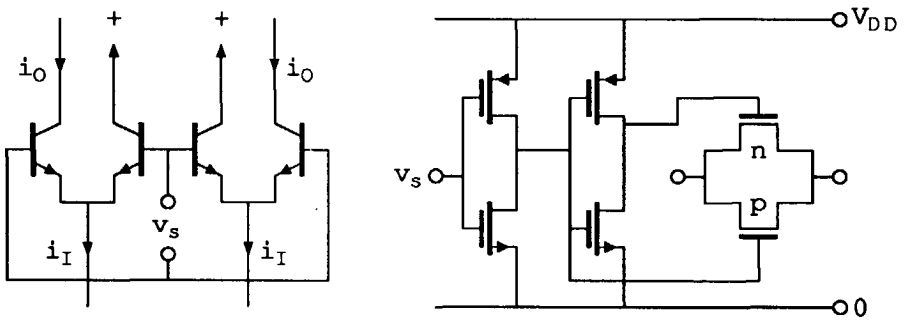

Figure 3.11: Bipolar long-tailed pair switch and CMOS transmission gate as basic switching elements.

3.2.1 The bipolar long-tailed pair switch

Figure 3.12 shows the implementation of the bipolar long-tailed pair switch in combination with the synchronous mixer. In analogy with the synchronous mixer, the IF signal input of the long-tailed pair switch is driven by a balanced series stage. The output of the switch is ac coupled to the balanced CB input stage of the synchronous mixer. This ac coupling is required by the implementation of the autozero system in order to prevent any influence of the state of the switch upon the mixer bias and hence the mixer output offset voltage.

Provided that the amplitude of the switching voltage is sufficiently large ($\hat{v}_s > 8V_T$), the switch in its on state behaves like a balanced CB stage. The intermodulation distortion generated by the switch in its on state is comparable with that of the mixer in its final state. In analogy with the

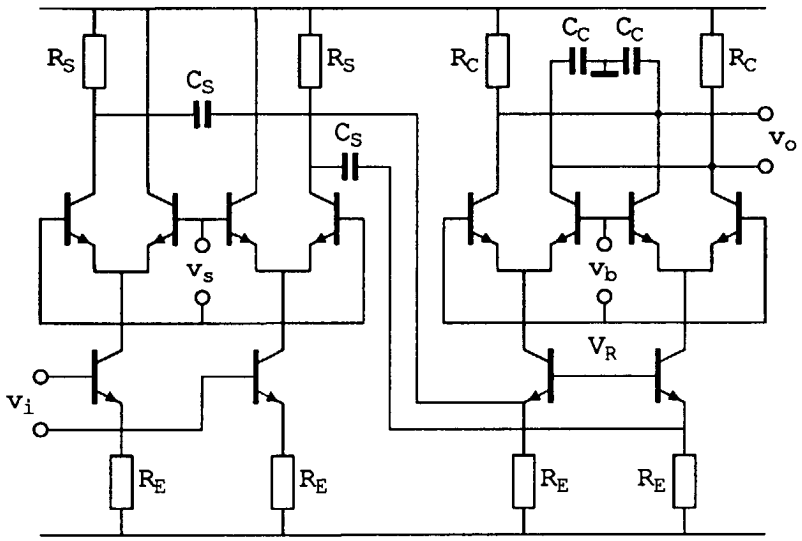

Figure 3.12: Implementation of the long-tailed pair switch including the mixer.

calculations in Subsection 3.1.4, Equation 3.71 is extended to:

$$\mathrm{IM}_{3s} = 20\log\left[\frac{V_T}{8V_E^3}\sqrt{\left(2+\frac{R_S}{R_E}\right)^2+\omega_0^2R_E^2(3C_c+C_p)^2V_i^2}\right] \qquad (3.74)$$

In this equation, which expresses the intermodulation distortion of the mixer including the series stage, the IF switch and the CB stage, R_S is the collector resistor of the long-tailed pair switch and C_p is the parasitic substrate capacitance of the coupling capacitors. The transistor types and the collector currents for both the series stage and the CB stage are taken as equal.

Because of the high mixer noise figure (see Section 3.4), the base current shot noise of the long-tailed pair switch and the CB stage, which is evidently equal to the base current shot noise of the series stage, can be neglected. Provided that $R_S \approx R_C \approx R_E$ and $R_E \gg r_b$, only the noise of the CB stage might significantly contribute to the equivalent input noise voltage. With this noise contribution taken in account, Equation 3.56 is extended to:

$$V_{ni}^2 = 8kTR_E\left(4+\omega_0^2R_Er_b(C_p+C_s)^2+\frac{\pi^2F_mg_mR_E}{8B_F}\right)B_{IF} \qquad (3.75)$$

Since the noise bandwidth of the PLL and the gain control is much smaller

than the audio noise bandwidth, a small noise contribution of the IF switch and the CB stage has no significant effect upon the detector dynamic range.

The phase shift introduced by the ac coupling can be calculated as:

$$\phi_s = \arg\left(\frac{j\omega_0 R_S C_S}{1 + j\omega_0 R_S C_S}\right) = \arctan\left(\frac{1}{\omega_0 R_S C_S}\right) \tag{3.76}$$

If $\omega_0 R_S C_S > 1$, this phase shift introduces a reduction of the conversion gain equal to:

$$1 - \cos(\phi_s) \approx \frac{\phi_s^2}{2} \approx \frac{1}{2(\omega_0 R_S C_S)^2} \tag{3.77}$$

If eg $\omega_0 R_S C_S = 4$ is taken, the phase lead $\phi_s = 0.24$rad and $\cos(\phi_s) = 0.97$. The loss of conversion gain introduced by this phase shift is about 3%. The required coupling capacitor can easily be implemented on-chip (see Section 3.4).

The off-state attenuation of the long-tailed pair switch at high frequencies is determined by the parasitic junction capacitances C_{be} and C_{bc}, the base resistance r_b and the additional cross talk capacitance C_w of the circuit. The amplitude of the switching voltage is assumed to be sufficiently large ($\hat{v}_s > 8V_T$). The on-state attenuation of the switch being the current attenuation of two CB stages including the ac coupling can be neglected (< 1dB).

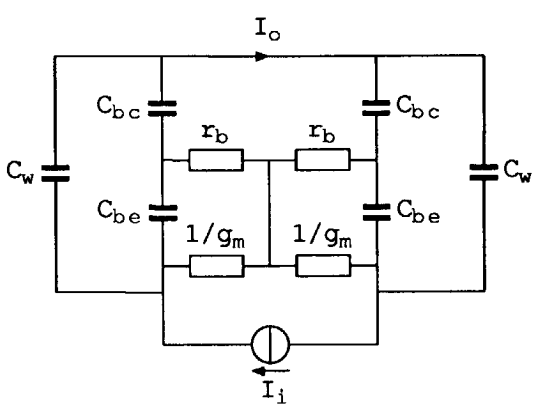

Figure 3.13: Small signal equivalent circuit of the long-tailed pair switch in its off state for frequencies $f \ll f_T$.

Figure 3.13 shows the small signal equivalent circuit of the switch in its

off state. The off-state transfer can be calculated as:

$$\frac{I_o}{I_i} = \frac{s^2 r_b r_e C_{be} C_{bc} + s r_e C_w (1 + s r_b C_j)}{s^2 r_b r_e C_{be} C_{bc} + s r_e C_w (1 + s r_b C_j) + s r_b C_j + s r_e C_{be} + 1} \tag{3.78}$$

In this equation, $r_e = 1/g_m = V_T/I_C$ and $C_j = C_{be} + C_{bc}$. Under the condition that $\omega_0 r_e C_w \ll 1$, $\omega_0 r_e C_{be} \ll 1$, $\omega_0 r_b C_{be} \ll 1$ and $\omega_0 r_b C_{bc} \ll 1$, which is generally fulfilled if $\omega_0 \ll \omega_T$, the off-state transfer can be approximated by:

$$\frac{I_o}{I_i} = \omega_0^2 r_b r_e C_{be} C_{bc} + \omega_0 r_e C_w \tag{3.79}$$

If we disregard the influence of the direct cross talk ($C_w = 0$), the off-state attenuation results in:

$$A_{\text{off}} = \frac{1}{\omega_0^2 r_e r_b C_{be} C_{bc}} \tag{3.80}$$

However, if the direct cross talk has a significant influence, the off-state attenuation can be approximated by:

$$A_{\text{off}} = \frac{1}{\omega_0 r_e C_w} \tag{3.81}$$

Numerical values of the off-state attenuation resulting from theoretical calculations, SPICE simulations and measurements of the switch can be found in Section 3.4.

3.2.2 The MOS switch

For the implementation of the IF autozero switch with transmission gates, these transmission gates can be configured as a current switch according to Figure 3.14 or as a voltage switch according to Figure 3.15.

For the current switch implementation, the additional noise and distortion introduced by the switch and the subsequent CB stage is comparable with that of the bipolar long-tailed pair switch. The on-state attenuation and the noise and distortion of the switch itself can be neglected, provided that the on-resistance of the transmission gates is lower than the collector resistors R_S. This on-resistance is equal to:

$$r_{\text{on}} = \frac{1}{\beta_n (V_{GSn} - V_{THn}) + \beta_p (V_{GSp} - V_{THp})} \tag{3.82}$$

in which β_n and β_p are the proportionality factors, while V_{THn} and V_{THp} are the threshold voltages of the NMOS and the PMOS pass transistors respectively.

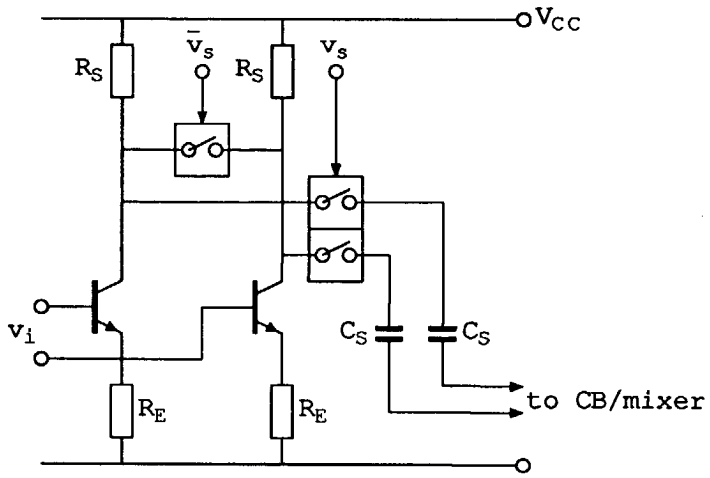

Figure 3.14: IF switch implementation with transmission gates as current switches.

In the case of a voltage switch, additional noise and distortion is generated by the emitter followers only provided that the on-resistance is lower than the ohmic base resistors. These emitter followers are used as buffers in order to prevent feedthrough of switching transients to the audio mixer.

The off-state attenuation of both switch configurations is determined by parasitic capacitive transfers over the gate and the bulk. A small signal equivalent circuit of the current switch configuration is shown in Figure 3.16. The small signal equivalent circuit of the voltage switch is just the reciprocal circuit. In this figure, C_{sb} and C_{db} are the junction capacitances of the drain and source diffusion areas respectively. The capacitances C_{gs} and C_{gd} are the gate overlap capacitances. The resistances r_{gn} and r_{gn} are the ohmic gate series resistances, while the r_{bn} and r_{bp} are the distributed bulk series resistances.

If the parasitic time constants ($r_g C_{gsn}$ etc.) are small compared with $1/\omega_0$, the off-state attenuation can be approximated by:

$$\begin{aligned}\frac{1}{A_{\text{off}}} &= \frac{1}{2}\omega_0^2 r_{on} r_{gn} C_{gsn} C_{gdn} + \frac{1}{2}\omega_0^2 r_{on} r_{gp} C_{gsp} C_{gdp} \\ &\quad + \frac{1}{2}\omega_0^2 r_{on} r_{bn} C_{sbn} C_{dbn} + \frac{1}{2}\omega_0^2 r_{on} r_{bp} C_{sbp} C_{dbp} \end{aligned} \tag{3.83}$$

For a MOS transistor, the gate resistance of a polysilicon gate is generally much smaller than the bulk resistance through the lightly doped substrate.

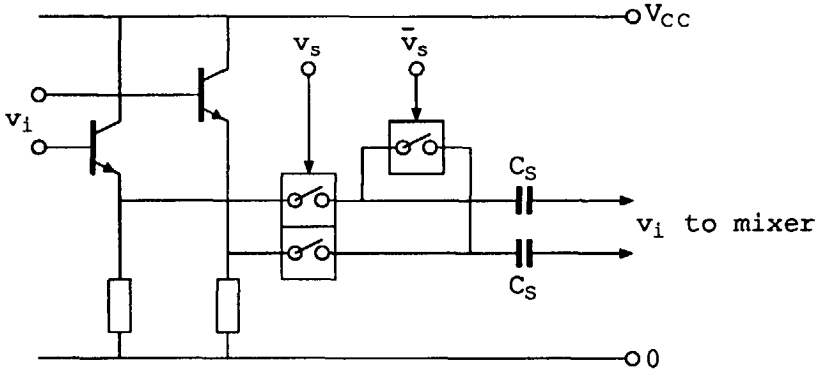

Figure 3.15: IF switch implementation with transmission gates as voltage switches.

For a self-aligned process, the gate capacitances in the off state, (the overlap capacitances) are also smaller than the bulk capacitances of the diffusion areas. Under these conditions, the off-state attenuation can be approximated by:

$$A_{\text{off}} = \frac{2}{\omega_0^2 r_{on} r_{bn} C_{sbn} C_{dbn} + \omega_0^2 r_{on} r_{bp} C_{sbp} C_{dbp}} \tag{3.84}$$

Although no MOS implementation of the IF switch has been made yet, the high bulk resistances of several kΩ make the feasibility of a 40dB off-state attenuation at an IF frequency of 70MHz doubtful. Since the required 40dB off-state attenuation can certainly be obtained with a bipolar long-tailed pair switch (see Section 3.4), the bipolar implementation is preferred over the MOS implementation.

3.3 The quadrature oscillator

For the generation of two oscillator signals in quadrature, three principal methods can be followed. The first method, shown in Figure 3.17 uses an oscillator operating at the double frequency. Under the condition that this double frequency oscillator generates a symmetrical waveform, the subsequent master slave divider provides for the desired quadrature relation.

In the second method a quadrature signal is obtained from the fundamental quadrature relation between the inductor current and the capacitor voltage in an LC oscillator. Obviously, this method requires far less circuitry and power dissipation than the former one. However, the inductor cannot be implemented on-chip.

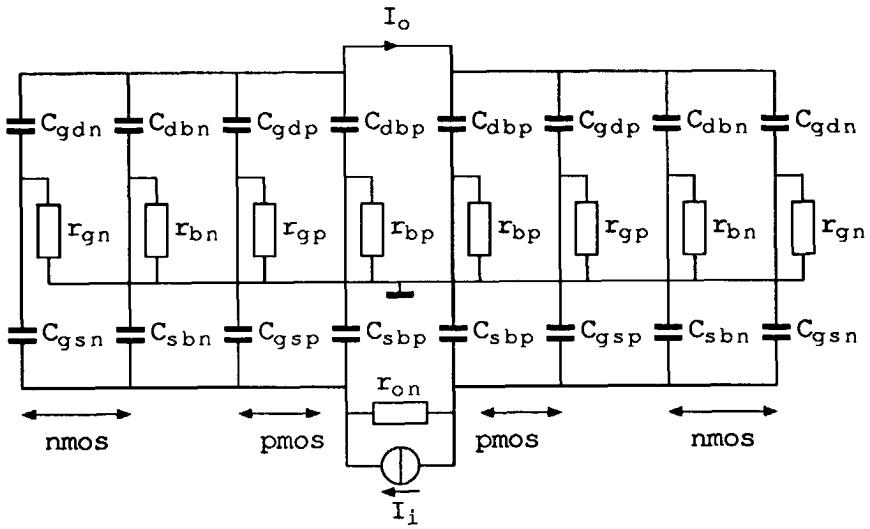

Figure 3.16: Small signal equivalent circuit of the MOS switch in its off state.

The third method uses a fully integrable first-order oscillator which principle is outlined in Figure 3.18. As we can see in the lower part of this figure, there is a fundamental quadrature relationship between the Schmitt trigger output voltage and the capacitor voltage.

An extremely accurate quadrature signal can be obtained with two coupled regenerative oscillators or with a two integrator oscillator [12]. An electronic implementation of a coupled regenerative quadrature oscillator is shown in Figure 3.19 on page 74. This coupling also provides for an improved carrier-to-noise ratio. In the rest of this section a brief calculation of the carrier-to-noise ratio of this coupled regenerative quadrature oscillator is made.

The frequency of the coupled oscillator can be calculated from the timing diagram in the lower part of Figure 3.18. From Figure 3.19, it can be seen that the capacitor charging current is equal to $I_1/2$ and that the hysteresis voltage V_{hys} is equal to $2(I_1 + I_2)R_X$. This results in an oscillator period equal to:

$$T_0 = \frac{8R_X C_X (I_1 + I_2)}{I_1} \tag{3.85}$$

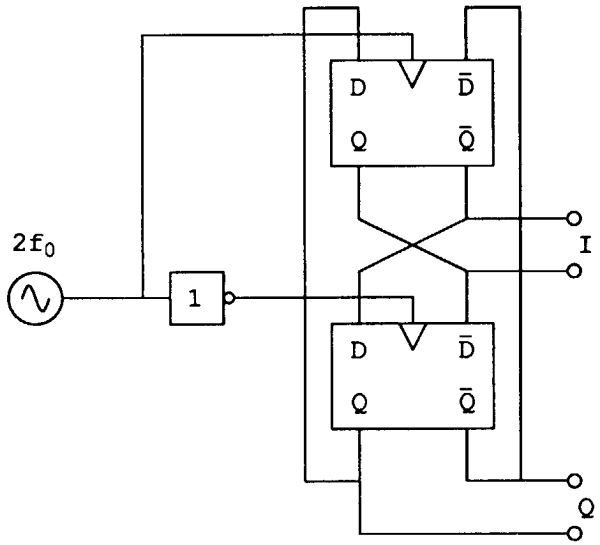

Figure 3.17: Generation of a quadrature signal with a master slave divider.

or an oscillator frequency equal to:

$$f_0 = \frac{I_1}{8R_X C_X (I_1 + I_2)} \tag{3.86}$$

The time derivatives of the oscillator frequency are calculated as:

$$\frac{df}{dI_1} = \frac{I_2}{8R_X C_X (I_1 + I_2)^2} \tag{3.87}$$

$$\frac{df}{dI_2} = \frac{-I_1}{8R_X C_X (I_1 + I_2)^2} \tag{3.88}$$

The absolute values of these derivatives are equal if $I_1 = I_2$.

The carrier-to-noise ratio of the oscillator signal is partly determined by frequency modulation caused by the noise current of the current sources $I_1/2$ and I_2. The output noise current of each of these current sources is described in terms of their equivalent parallel noise resistances $2R_{n1}$ and R_{n2} respectively:

$$S(I_1/2) = \frac{4kT}{2R_{n1}} \tag{3.89}$$

$$S(I_2) = \frac{4kT}{R_{n2}} \tag{3.90}$$

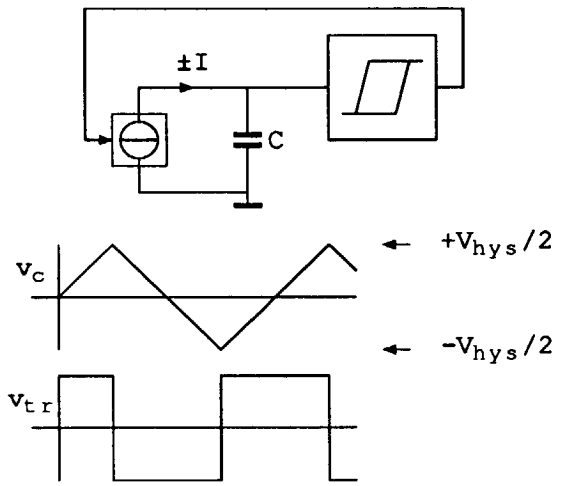

Figure 3.18: Generation of a quadrature signal with a first-order oscillator.

For low modulation frequencies, the rms frequency deviation in a 1Hz bandwidth is calculated as:

$$\overline{\Delta f_0^2} = \frac{2kT}{R_{n1}} \left(\frac{df}{dI_1}\right)^2 + \frac{2kT}{R_{n2}} \left(\frac{df}{dI_2}\right)^2 \tag{3.91}$$

At a relatively small frequency distance from the carrier, the phase noise caused by the noise of the current sources results in:

$$\mathcal{L}(\Delta f) = \frac{\overline{\Delta f_0^2}}{2\Delta f^2} = kT \left(\frac{1}{I_1^2 R_{n1}} + \frac{1}{I_2^2 R_{n2}}\right) \frac{I_2^2}{(I_1 + I_2)^2} \left(\frac{f_0}{\Delta f}\right)^2 \tag{3.92}$$

Another noise source is the noise of the hysteresis voltage, mainly caused by the thermal noise of the base resistances and the collector resistances R_X. The spectral noise density of the hysteresis voltage of the regenerative circuits is equal to:

$$S(V_{nh}) = 4kT(4r_b + 2R_X) \tag{3.93}$$

In contrast to the noise of the current sources, noise of the hysteresis voltage causes duty-cycle modulation. With a nominal duty cycle of 50%, $\mathcal{L}(\Delta f)$ for frequencies close to the carrier is calculated as [12, Ch. 6]:

$$\mathcal{L}(\Delta f) = \frac{V_{nh}^2}{2V_{hys}^2} \left(\frac{f_0}{\Delta f}\right)^2 = \frac{kT(2r_b + R_X)}{(I_1 + I_2)^2 R_X^2} \left(\frac{f_0}{\Delta f}\right)^2 \tag{3.94}$$

The sampling actions inherent to the switching behaviour of the oscillator cause aliasing of phase noise around the higher oscillator harmonics to phase noise around the fundamental frequency component. Apart from this effect, extra time jitter is caused by the regenerative circuit itself. The theoretical oscillator noise, in which this aliasing effect is included, can be written as:

$$\mathcal{L}(\Delta f) = 2kT\left(\frac{1}{I_1^2 R_{n1}} + \frac{1}{I_2^2 R_{n2}} + \frac{2r_b + R_X}{I_2^2 R_X^2}\right)\frac{I_2^2}{(I_1 + I_2)^2}\left(\frac{f_0}{\Delta f}\right)^2 n_{\text{fold}} \tag{3.95}$$

In this equation, n_{fold} is the noise folding factor caused by sampling of the noise in the active circuitry. With B_n the noise bandwidth of the active circuitry (in Hz), this folding factor [12, Sec. 6.7] is equal to:

$$n_{\text{fold}} = \frac{B_n}{2f_0} \tag{3.96}$$

The results of a prototype coupled regenerative oscillator is described in Section 3.4.

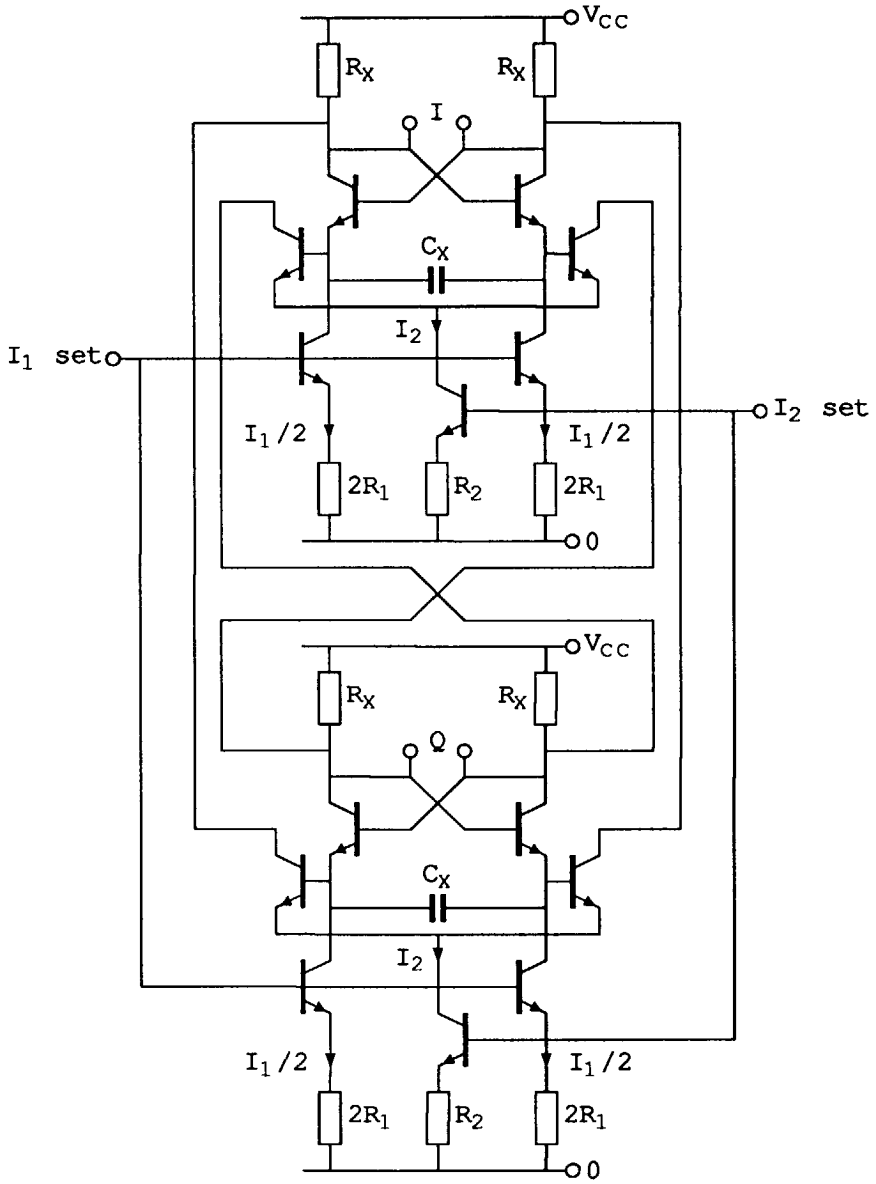

Figure 3.19: Coupled regenerative quadrature oscillator.

3.4 Results of a prototype IF system.

A monolithically integrated prototype of the IF circuitry containing the mixers, switches and the quadrature oscillator has been made in a 3GHz bipolar process. The mixers and the switches operate on a nominal supply voltage of 8V, while the oscillator buffers and the oscillator operate on a nominal supply voltage of 4V. For all transistors, the typical values of the main parameters, used for calculations in preceding sections, are listed in Table 3.1.

current gain:	B_F	130
	β_f	130
base resistance:	r_b	300Ω
base-emitter capacitance:	C_{be}	0.14pF
base-collector capacitance	C_{bc}	0.17pF
collector-substrate capacitance:	C_{cs}	0.36pF
total base junction capacitance:	C_j	0.31pF
total collector capacitance:	C_c	0.53pF
transit time:	τ_f	47ps

Table 3.1: Typical transistor parameters of the 3GHz bipolar process. The junction capacitances are specified for a zero bias voltage.

Collector current	I_C	0.8mA
Buffer tail current	I_T	1.3mA
Emitter resistor	R_E	1.6kΩ
Mixer collector resistor	R_C	2kΩ
Switch collector resistor	R_S	2kΩ
Buffer collector resistor	R_0	300Ω
Mixer collector capacitor	C_C	25nF
Coupling capacitor	C_S	6pF
Parasitic substrate capacitance	C_p	2pF

Table 3.2: Bias current and component values of the prototype mixer and the IF switch.

The numerical values of the bias currents and the component values are listed in Table 3.2. With the given transistor parameters and the given component values, the base current $\hat{i}_b$ of the mixer during the transition of

state is calculated as:

$$\hat{i}_b = \frac{I_T}{2}\frac{R_0}{r_b + 2R_0} = 0.22\text{mA} \tag{3.97}$$

With the given bias current, the ratio between the quasi-static mixer distortion IM_{3b} and the switching induced mixer distortion IM_{3c} at the IF frequency of 70MHz is calculated as:

$$\frac{IM_{3c}}{IM_{3b}} = \frac{\omega_0 \tau_f^2 I_C^3}{2V_T \hat{i}_b^2 C_c} = 0.39 \tag{3.98}$$

For this prototype mixer operating at an oscillator frequency of 70MHz, the switching induced distortion is practically negligible. The ratio between the quasi-static mixer distortion IM_{3b} and the distortion of the series stage IM_{3a} is calculated as:

$$\frac{IM_{3b}}{IM_{3a}} = \omega_0 R_E C_c = 0.37 \tag{3.99}$$

For this prototype mixer, the distortion of the series stage dominates over the distortion of the mixer for the nominal IF frequency of 70MHz.

With the given component values and transistor parameters, the mixer noise figure $F_m = 49$, which is calculated with Equation 3.54. This large noise figure, which is partly caused by the noise of the relatively large base resistances ($1 + g_m r_b = 11$), can be significantly reduced if transistors with lower base resistances are applied. Obviously, $g_m R_E = 51$, so

$$F_m g_m R_E = 2500 \gg B_F$$

and consequently, the equivalent input noise is completely determined by the noise of the synchronous mixer itself. With an IF bandwidth of 2.5kHz, the equivalent input noise voltage according to Equation 3.57 is 1.8μV. The third-order IMFDR according to Equation 3.73 is 95dB.

The additional third-order intermodulation distortion caused by the IF switch and the subsequent CB stage has been calculated in Section 3.2. The ratio between the distortion of the mixer including the IF switch according to Figure 3.12, expressed by Equation 3.74, and the distortion of the mixer without the IF switch, expressed by Equation 3.71, is calculated as:

$$\frac{IM_{3s}}{IM_{3ab}} = 10\log\left(\frac{(2 + R_S/R_E)^2 + \omega_0^2 R_E^2 (3C_c + C_p)^2}{(1 + \omega_0^2 R_E^2 C_c^2)}\right) \tag{3.100}$$

With the given transistor parameters and component values, this ratio is 12dB, so the implementation of the IF switch in the synchronous mixer causes a 12dB increase the of the third-order intermodulation distortion. The Equivalent input noise of the mixer including the IF switch according to Equation 3.75 is 1.9μV, which is nearly equal to that of the mixer without the IF switch. In Section 1.5, the IMFDR$_3$ in dB was calculated as:

$$\text{IMFDR}_3 = -\frac{1}{3}\text{IM}_3 + \frac{2}{3}\text{CNR} \tag{3.101}$$

A 12dB increase of the intermodulation distortion combined with a 0.5dB increase of the noise level results in a 4dB decrease of the IMFDR. As a result, the third-order IMFDR of the phase detector and the AGC mixer including the IF switch is 91dB.

The measured noise floor of the synchronous mixers is about 2μV for the audio mixer and 2.2μV for the the phase detector and the AGC mixer. The measured IMFDR$_3$ is about 88dB for the phase detector and the AGC mixer and at least 90dB for the audio mixer. Although the measured IMFDR is somewhat smaller than calculated, these values are more than sufficient in order to guarantee the required selectivity and dynamic range of the complete synchronous detector. These calculated and measured values are listed in Table 3.3.

	calculated	measured
V_{ni} audio mixer	1.8μV	2.0μV
V_{ni} mixer and switch	1.9μV	2.2μV
IMFDR$_3$ audio mixer	95dB	$\geq$ 90dB
IMFDR$_3$ mixer and switch	91dB	88dB

Table 3.3: Calculated and measured values of the equivalent input noise voltage and the IMFDR of the synchronous mixers.

The coupling capacitors are 6pF oxide capacitors. With the 2kΩ collector resistor, the phase lead $\phi_s = 0.19$rad and $\cos(\phi_s) = 0.98$. The effect of this phase lead, which is almost compensated by the phase lag of the CB stage, can be neglected.

The off-state attenuation of the IF switch, in which the direct cross talk is disregarded ($C_w = 0$), was calculated as:

$$A_{\text{off}} = \frac{1}{\omega_0^2 r_b r_e C_{be} C_{bc}} \tag{3.102}$$

With the transistor parameters given in Table 3.1, an off-state attenuation $A_{off} = 87$dB at 70MHz is found. A spice simulation of the on-state and the off-state transfer of the IF switch as a function of the frequency is shown in Figure 3.20. The slope of the off-state attenuation is 20dB/decade, which is in agreement with Equation 3.102. At the nominal 70MHz IF frequency, the on-state attenuation can practically be neglected and the off-state attenuation is about 100dB, which is even 13dB more than calculated. For the calculated off-state attenuation, the junction capacitances at zero bias voltage has been taken, while the junction capacitance values at the off-state bias are lower.

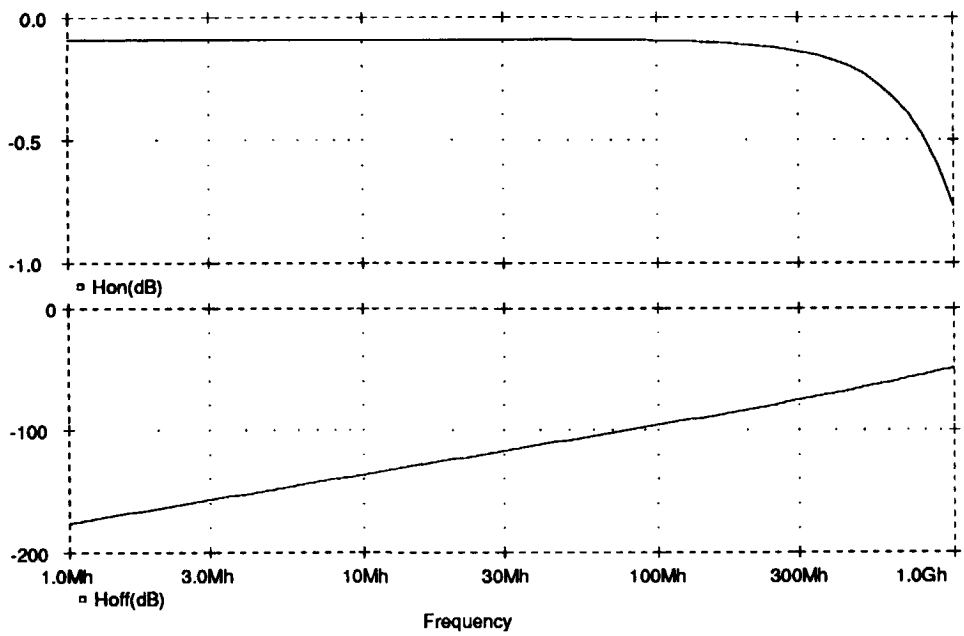

Figure 3.20: Transfer of the IF switch in its on state (upper one) and in its off state (lower one).

The measured off-state attenuation however is only 57dB, while the measured on-state attenuation is less than 1dB. This limited value of the measured off-state attenuation is completely determined by direct cross talk, which was calculated as:

$$A_{off} = \frac{1}{\omega_0 r_e C_w} \tag{3.103}$$

A 57dB off-state attenuation corresponds to a cross talk capacitance $C_w =$

0.1pF, which is determined by the suboptimal wiring structure of the semi-custom chip. However, this limited off-state attenuation is sufficient for proper operation of the autozero system.

The prototype coupled regenerative quadrature oscillator is implemented with 2.7pF on-chip junction capacitors. With collector resistors $R_X = 400\Omega$ and nominal currents I_1 =0.5mA and I_2 = 0.5mA, the hysteresis voltage is 0.8V and the theoretical initial frequency is equal to:

$$f_0 = \frac{I_1}{8R_X C_X (I_1 + I_2)} = 58\text{MHz} \tag{3.104}$$

The results of a SPICE simulation of the oscillator is shown in Figure 3.21. Both the measured initial frequency of 95MHz and the initial frequency of 110MHz obtained with the SPICE simulation deviate significantly from the theoretical one. This effect is mainly caused by leakage currents and nonlinearities of the junction capacitors and the base currents of the cross coupling transistors, which causes the capacitor voltage swing to be smaller than the hysteresis voltage at the collectors [12]. Until now, no deviation of the quadrature relation of the output signals has been measured.

The phase noise of the oscillator is expressed by Equation 3.95. With R_{n1} and R_{n2} about 2kΩ, the phase noise at the nominal currents is calculated as:

$$\mathcal{L}(\Delta f) = -159 + 10\log\left[\left(\frac{f_0}{\Delta f}\right)^2\right] \text{ dBc/Hz} \tag{3.105}$$

A noise bandwidth B_n = 500kHz is taken resulting in n_{fold} = 6dB. The calculated CNR at a carrier frequency of 70MHz is 81dBc/Hz at 9kHz from the carrier and 95dBc/Hz at 45kHz from the carrier. Phase noise measurements confirm a 20dB/decade noise characteristic, although the measured phase noise is 10dB larger than calculated (71dBc/Hz and 85dBc/Hz respectively). This oscillator hardly fulfills its CNR specifications.

The 10dB additional noise is caused by the jitter of the Schmitt triggers and by the reduced capacitor voltage swing. This jitter is further enlarged by the parasitic substrate capacitances of the junction capacitors C_X. In a BIMOS process, where linear oxide capacitors with low parasitic substrate capacitances can be implemented (less than 10% of the nominal value), a better performance can be expected.

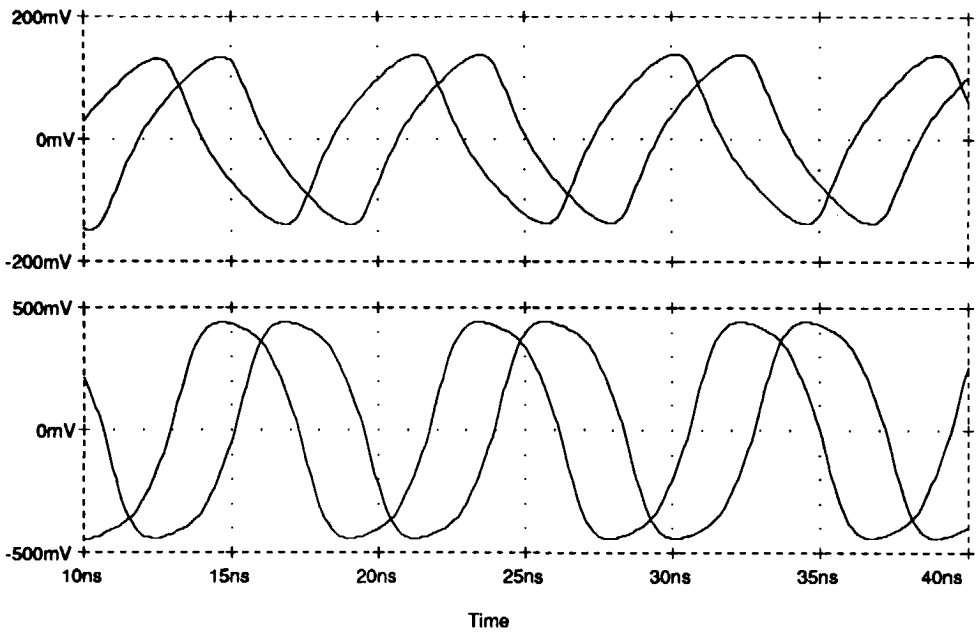

Figure 3.21: Spice simulation of the regenerative quadrature oscillator. The upper curves indicate the differential capacitor voltages, while the lower curves indicate the collector voltages.

3.5 Conclusions

The required specifications concerning the synchronous mixers and the IF switch, stated in Chapter 1 and Chapter 2, will not lead to specific implementation problems. The required IMFDR can be obtained with local feedback IF driving stages for the mixers and the switches, while the required CNR of the VCO is feasible with an on-chip oscillator.

The implementation of a completely integrable quadrature oscillator demanding a minimum amount of circuitry and power consumption is feasible with a coupled regenerative oscillator (see Figure 3.19). For proper operation of this oscillator and in order to obtain the required carrier-to-noise ratio, it is important to implement the on-chip capacitors C_X as oxide capacitors with minimum parasitic substrate capacitances.

Chapter 4

Design of the on-chip continuous-time audio low-pass filter

As we have seen in Section 3.1.1, the synchronous mixer output level ratio between the desired modulation signal and the beat note resulting from an interfering carrier is 10dB less than the IF mixer input level ratio between the desired carrier and the adjacent carrier. A modulation depth of 30% has been assumed. For adequate suppression of this beat note, the filter suppression has to be 10dB more than the selectivity, which results in a 45dB filter suppression at 9kHz and a 60dB filter suppression at 45kHz. According to Section 1.3 and Section 1.5, the dynamic range of the audio low-pass filter has to be at least 90dB, while the second- and third-order IMFDR has to be at least 70dB and 77dB respectively.

For a maximally flat amplitude response of the detected audio signal, a Butterworth characteristic is chosen. The Butterworth pole positions are shown in Figure 4.1, while the amplitude transfer is equal to:

$$|H(f)|^2 = \frac{H(0)^2}{1 + \left(\frac{f}{f_c}\right)^{2n}} \tag{4.1}$$

In this equation, f_c denotes the -3dB cut-off frequency, $H(0)$ denotes the passband gain and n denotes the order of the filter. With a -3dB frequency f_c in the range of 3.0–3.5kHz and a suppression of 45dB at 9kHz, a fifth-order Butterworth filter is required. The calculated filter suppression at 45kHz is more than 110dB, which is much more than the required stopband selectivity.

The real pole of the fifth-order Butterworth filter is implemented in the passive RC prefilter in the collector circuit of the mixer (see Section 3.1). This prefilter provides for 9dB adjacent channel selectivity and 23dB stopband selectivity and suppresses high-frequency interfering signals that may cause intermodulation and spurious detection in the active filter part. Although the intermodulation demands of the fourth-order active filter part may be reduced, the initial IMFDR requirements are maintained. For frequencies above 1MHz, the suppression of the prefilter is more than 50dB, so this prefilter completely takes over the required stopband selectivity from

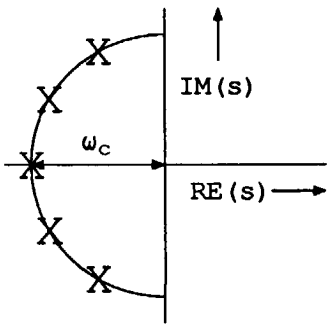

Figure 4.1: Pole pattern of a Butterworth filter.

the active filter part. Consequently, the fourth-order active filter part must be able to handle frequencies up to at least 1MHz.

The filter types described in this chapter will be limited to all pole low-pass filters for the audio frequency range. These active filters will be derived from passive LC ladder filter models, which will be described in Section 4.1. In Section 4.2, the passive LC filter models will be transformed to active filter structures by taking an active integrator as a basic building block. The implementation of such an integrator and the resulting IMFDR of the filter will be described in Section 4.3.

In continuous-time integrated filters, all filter transfer characteristics except the cut-off frequency f_c are determined by on-chip component matching. The mismatch of critical on-chip component values can be limited to a few percent. The absolute tolerance of integrated component parameter values however may be more than 30%. In order to establish an accurate filter bandwidth, Section 4.4 deals with autotuning techniques that relate the filter bandwidth to an external reference frequency.

current gain:	B_F	190
(I_D = 0.1mA, V_{CB} = 2V)	β_f	190
base resistance:	r_b	1kΩ
transit frequency	f_T	2.5GHz

Table 4.1: Typical parameter values of a minimum dimension NPN transistor in the Philips L422 process.

Finally, Section 4.5 deals with the design of, simulations of and measurements on a prototype audio filter. This filter, including test and autotuning circuitry, is integrated on a single evaluation chip using the Philips L422

proportionality factor	$\beta_\square$	$45\mu A/V^2$
threshold voltage	V_{TH}	0.75V
body coefficient	γ	$0.28V^{0.5}$
surface potential	ϕ_B	0.55V

Table 4.2: Typical parameter values of a NMOS transistor in the Philips L422 process.

proportionality factor	$\beta_\square$	$15\mu A/V^2$
threshold voltage	V_{TH}	0.85V
body coefficient	γ	$0.60V^{0.5}$
surface potential	ϕ_B	0.55V

Table 4.3: Typical parameter values of a PMOS transistor in the Philips L422 process.

BIMOS technology. Typical values of the main parameter of NPN, NMOS and PMOS transistors in this process can be found in Table 4.1, 4.2 and 4.3 respectively. These parameter values will be used for all numerical calculations throughout this chapter.

4.1 Passive LC filter models

In this section, the audio filter floor plan design is modelled with a cascade of passive all-pole LC networks. Obviously, the prefilter is modelled with a single RC section. The filter models will be normalised with respect to the -3dB angular frequency ω_c and the termination resistor. The values of the normalised filter coefficients will be used for the determination of the time constants of the active filters in the following sections.

In Figure 4.2 the audio filter is modelled with a first-order section cascaded by two second-order ladder sections. The voltage buffers provide for non-interactive transfers of the passive networks.

The transfer of a second-order ladder section is equal to:

$$H_2(s) = \frac{\omega_c^2}{\omega_c^2 + a\omega_c s + s^2} \tag{4.2}$$

In this equation,

$$\omega_c = \sqrt{\frac{1}{LC}}$$

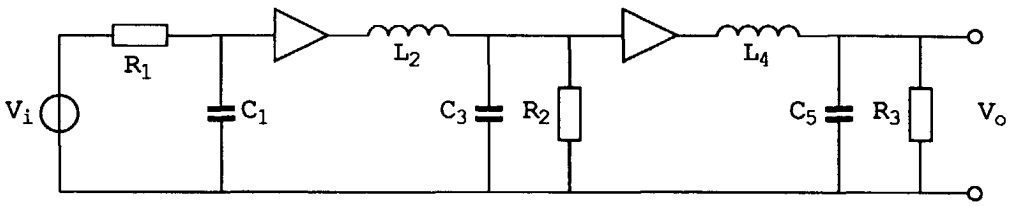

Figure 4.2: A passive audio filter model built up with a cascade of a first-order section and two second-order sections.

denotes the cut-off frequency and

$$a = \frac{1}{R}\sqrt{\frac{L}{C}}$$

denotes the relative damping. For a normalised second-order section, $\omega_c = 1\text{rad/s}$ and $R = 1\Omega$. The normalised transfer of a fifth-order Butterworth filter ($\omega_c = 1$ and $H_0 = 1$) can be derived directly from the pole pattern in Figure 4.1 as:

$$H(s) = \frac{1}{(1+s)(1+a_1 s+s^2)(1+a_2 s+s^2)}\ , \tag{4.3}$$

in which

$$a_1 = \frac{1}{2}(\sqrt{5}+1)\ ,$$

and

$$a_2 = \frac{1}{2}(\sqrt{5}-1)\ .$$

Now the normalised coefficients and the filter component values can be calculated as:

$$A_1 = \omega_c R_1 C_1 = 1 \tag{4.4}$$

$$A_2 = \omega_c L_2/R_2 = \frac{1}{2}(\sqrt{5}+1) \tag{4.5}$$

$$A_3 = \omega_c R_2 C_3 = \frac{1}{2}(\sqrt{5}-1) \tag{4.6}$$

$$A_4 = \omega_c L_4/R_3 = \frac{1}{2}(\sqrt{5}-1) \tag{4.7}$$

$$A_5 = \omega_c R_3 C_5 = \frac{1}{2}(\sqrt{5}+1) \tag{4.8}$$

Figure 4.3 shows a passive LC filter model of the audio filter, in which the prefilter is represented by the RC section R_1 and C_1 and the active filter part has to be derived from the fourth-order asymmetrical ladder filter L_2 to C_5 and R_2.

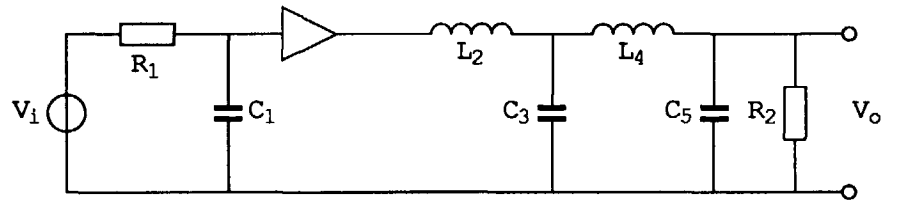

Figure 4.3: A passive audio filter model built up with a cascade of a first-order section and a fourth-order asymmetrical ladder section.

The normalised transfer of the fourth-order ladder section can be calculated as:

$$H_4(s) = \frac{1}{1 + s(A_2 + A_4) + s^2(A_2A_5 + A_2A_3 + A_4A_5) + s^3A_2A_4A_3 + s^4} \tag{4.9}$$

In this equation, the normalised coefficients are equal to:

$$A_2 = \omega_c R_2 C_2 \tag{4.10}$$

$$A_3 = \frac{\omega_c L_3}{R_2} \tag{4.11}$$

$$A_4 = \omega_c R_2 C_4 \tag{4.12}$$

$$A_5 = \frac{\omega_c L_4}{R_2} \tag{4.13}$$

The -3dB angular frequency ω_c is equal to:

$$\omega_c = \sqrt[4]{\frac{1}{L_2C_3L_4C_5}} \tag{4.14}$$

The normalised Butterworth transfer, in which the denominator is expressed as a product of a first-order and a fourth-order polynomial, can be written as:

$$H(s) = \frac{1}{(1 + s)(1 + \sqrt{5}s + 3s^2 + \sqrt{5}s^3 + s^4)} \tag{4.15}$$

Now the values of the normalised coefficients of this passive LC filter model are calculated as:

$$A_1 = \omega_c R_1 C_1 = 1 \tag{4.16}$$

$$A_2 = \omega_c L_2/R_2 = \frac{1}{2}\sqrt{5} \tag{4.17}$$

$$A_3 = \omega_c R_2 C_3 = \frac{4}{5}\sqrt{5} \tag{4.18}$$

$$A_4 = \omega_c L_3/R_2 = \frac{1}{2}\sqrt{5} \tag{4.19}$$

$$A_5 = \omega_c R_2 C_5 = \frac{1}{5}\sqrt{5} \tag{4.20}$$

As an alternative to the fourth-order asymmetrical ladder filter, also a symmetrical fourth-order ladder filter, terminated with R_2 at both the input and the output, might be used. However, the intended transfer cannot be realised with this configuration if both R_2 is normalised to 1Ω and ω_c is normalised to 1rad/s.

4.2 Active filter structures

If we look at the graph and the network equations of passive RLC networks, an inductor can be regarded as a voltage-to-current integrator and a capacitor can be regarded as a current-to-voltage integrator. In integrated filters, large inductors are not available, so a voltage-to-current integrator has to be realised with a capacitor as a current-to-voltage integrator and two real voltage-to-current transfers. Figure 4.4 shows a simulation of an inductor in which the active part, built up with two transconductances, is generally called a gyrator.

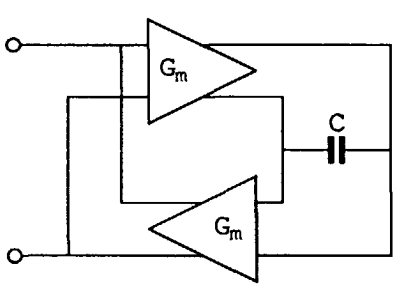

Figure 4.4: Inductor simulated with a gyrator and a capacitor.

A more systematic method applied in this chapter is based on the application of active voltage-to-voltage integrators with multiple inputs. Figure 4.5 shows the schematic representation of a two input active voltage-to-voltage integrator. This integrator is built up with a real voltage-to-current

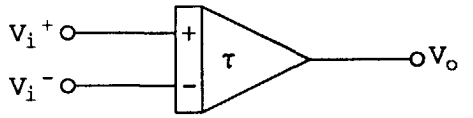

Figure 4.5: Symbol for a multiple input integrator.

transfer, represented by an equivalent resistance R, and a capacitor C as a current-to-voltage integrator. The detailed implementation will be dealt with in Section 4.3. The transfer of the integrator according to Figure 4.5 can be written as:

$$\frac{V_o(s)}{V_i^+(s) - V_i^-(s)} = \frac{1}{s\tau} = \frac{1}{sRC} \tag{4.21}$$

in which $\tau = RC$ denotes the integration time constant. Although all signals are drawn with a single wire in this section, these signals can be balanced as well.

The simplest active filter structure is a first-order active filter or a damped integrator. Its passive model is a first-order RC low-pass section. The damping is obtained by connecting the negative input of the integrator in Figure 4.5 to its output. The resulting transfer then equals:

$$\frac{V_o(s)}{V_i^+(s)} = \frac{1}{1 + s\tau} = \frac{1}{1 + sRC} \tag{4.22}$$

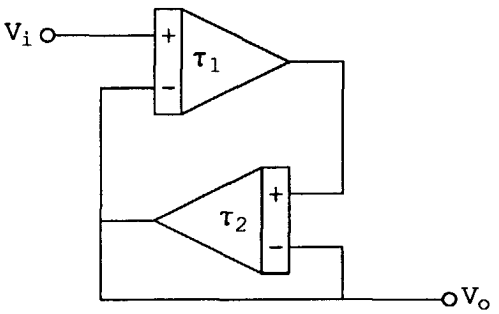

Figure 4.6: Active implementation of a second-order LC low-pass filter.

The simplest configuration to realise a low-pass transfer with complex poles is shown in Figure 4.6. This active filter configuration is derived from a second-order low-pass LC filter section, shown in Figure 4.2. The transfer of this second-order filter structure, generally called a BIQUAD, is equal to:

$$H(s) = \frac{1}{1 + s\tau_1 + s^2\tau_1\tau_2} \tag{4.23}$$

From this equation, the -3dB angular frequency ω_c and the damping a can be derived as:

$$\omega_c = \frac{1}{\sqrt{\tau_1 \tau_2}} \tag{4.24}$$

$$a = \sqrt{\frac{\tau_1}{\tau_2}} \tag{4.25}$$

The active part of the audio filter can be implemented with two cascaded BIQUADs, for which the relative dampings and the normalised filter coefficients are calculated in Section 4.1.

Equivalent to higher-order asymmetrical ladder filters terminated at the output, the BIQUAD filter structure can be extended to a higher-order active ladder structure (in fact, the first-order and the second-order structures are also ladder structures). As an example, Figure 4.7 shows the active realisation of the fourth-order ladder filter, for which the passive LC filter model was shown in Figure 4.3. Both passive and active ladder implementations are described by the same network equations, in which the normalised time constants $\omega_c \tau_i$ of the active integrators are equal to the corresponding normalised coefficients A_i calculated in Section 4.1. This one-to-one relation enables a systematic design starting with a classical passive LC filter.

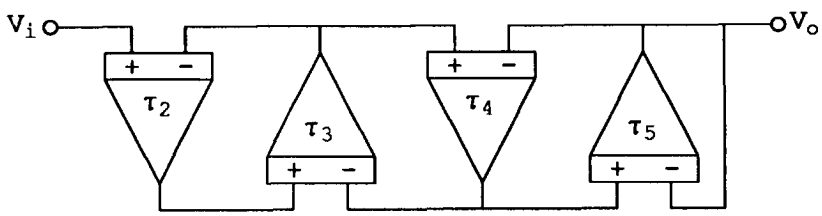

Figure 4.7: Active realisation of a fourth-order low-pass ladder filter.

The -3dB angular frequency ω_c of an active ladder filter with order n is equal to:

$$\omega_c = \frac{1}{\sqrt[n]{\tau_1 \tau_2 \ldots \tau_n}} \tag{4.26}$$

This value is determined by absolute values of time constants. The dimensionless normalised coefficients however are all ratios of time constants, so their accuracy depends upon the matching of component values. In order to enable adjustment of ω_c without affecting the normalised coefficients, all time constants must be tuned simultaneously with the same multiplicative

factor. For MOS based active filters, the capacitors are generally implemented as MOS capacitors because of their excellent linearity and matching. Consequently, adjustment of the time constants implies adjustment of the equivalent resistances R.

The noise behaviour of an active integrator will be mainly determined by its integration resistance R. The equivalent input noise voltage in a bandwidth B at *each* input can be written as:

$$V_{ni}^2 = 4kTFRB \tag{4.27}$$

In this equation, k is the Bolzman constant, T is the absolute temperature and F represents the excess noise generated by the active circuitry. For the first-order active filter, the total output noise voltage is calculated as:

$$V_{no}^2 = 8kTFR \int_0^\infty \frac{df}{1+\omega^2 R^2 C^2} = \frac{2kTF}{C} \tag{4.28}$$

The total output noise is determined by the integration capacitor C independent of the integration resistance R.

The output noise of the BIQUAD is calculated as:

$$V_{no}^2 = 8kTFR_1 \int_0^\infty |H(\omega)|^2 df + 8kTFR_2 \int_0^\infty \omega^2 \tau_1^2 |H(\omega)|^2 df \tag{4.29}$$

Using standard integrals, this equation results in:

$$V_{no}^2 = 2kTF\frac{R_1}{\tau_1} + 2kTF\frac{R_2}{\tau_2} = 2kTF\left(\frac{1}{C_1} + \frac{1}{C_2}\right) \tag{4.30}$$

Also for the second-order active ladder filter, the total output noise is determined by the value of the integration capacitors independent of the integration resistances.

For higher-order active ladder filter with a single termination at the output, it can be derived that the output noise is equal to:

$$V_{no}^2 = 2kTF\left(\frac{1}{C_1} + \cdots + \frac{1}{C_n}\right) \tag{4.31}$$

This total output noise voltage is independent of the value of the integration resistances.

If all integration resistances are taken as equal and the noise contribution of the passive prefilter is neglected, the total output noise of the audio filter can be calculated as:

$$V_{no}^2 = 2kTFR\omega_c \sum_{i=2}^{5} \frac{1}{A_i} \tag{4.32}$$

The total capacitance is equal to:

$$C_{tot} = m \sum_{j=1}^{5} A_j \tag{4.33}$$

in which m depends on the integrator implementation (see Section 4.3). The output noise as a function of the *total* capacitance is equal to:

$$V_{no}^2 = \frac{2mFkT}{C_{tot}} \sum_{i=1}^{n} \frac{1}{A_i} \sum_{j=1}^{n} A_j \tag{4.34}$$

Using the numerical values of the normalised coefficients calculated in Section 4.1, the total output noise of the audio filter built up with two cascaded BIQUADs is found to be:

$$V_{no}^2 = \frac{40mFkT}{C_{tot}} \tag{4.35}$$

For the audio filter built up with a fourth-order active ladder filter, the total output noise is found to be:

$$V_{no}^2 = \frac{41mFkT}{C_{tot}} \tag{4.36}$$

The output noise in relation to the total capacitance of both filter implementations is practically equal.

If all integration capacitors are taken as equal, the total output noise is calculated as:

$$V_{no}^2 = \frac{32mFkT}{C_{tot}} \tag{4.37}$$

This noise level is 1dB lower than that of the filter implementation with all resistance values being equal. However, the tracking accuracy of the adjustable integration resistances is expected to be better if these resistances are all equal.

4.3 Integrator implementations

The limited value of on-chip capacitors (about 100pF) combined with a low cut-off frequency (about 3kIIz) requires large integration resistances (about 1MΩ), which have to be adjustable. Such integration resistances can be implemented with MOS transconductance elements or gate controlled MOS

resistors. Using a simplified MOS model [22, p. 130], the drain current I_D in the triode region and in the saturation region is given by:

$$I_D = \beta\left((V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right) \quad \text{if} \quad V_{DS} \leq V_{GS} - V_{TH} \quad (4.38)$$

$$I_D = \frac{\beta}{2}\left((V_{GS} - V_{TH})^2\right) \quad \text{if} \quad V_{DS} > V_{GS} - V_{TH} \quad (4.39)$$

In this equation, β is the proportionality factor, V_{GS} is the gate-source voltage, V_{TH} is the threshold voltage and V_{DS} is the drain-source voltage. Due to the dominant quadratic behaviour of a MOS transistor, fully balanced circuits are applied in order to cancel out even-order nonlinearities. For proper balancing, the post-detection dc carrier has to be suppressed by ac coupling of the active filter input with the audio mixer output.

If a MOS transistor is biased in its saturation region, the small-signal transconductance can be calculated as:

$$g_m = \frac{dI_D}{dV_{GS}} = \beta(V_{GS} - V_{TH}) = \sqrt{2\beta I_D} \quad (4.40)$$

The basic implementation of an active voltage-to-voltage integrator, in which the voltage-to-current transfer is implemented with a MOS source-coupled pair applying saturated MOS transistors as transconductance elements, is shown in Figure 4.8. Additional inputs can be realised by adding additional source-coupled pairs. The small-signal transfer of this integrator is written as:

$$\frac{V_o(s)}{V_i(s)} = \frac{g_m}{2sC} = \frac{\sqrt{\beta I_T}}{2sC} \quad (4.41)$$

in which I_T is the tail current. The equivalent integration resistance R is equal to $2/g_m$. Obviously, the factor m in Equation 4.33 to 4.37 in the previous section is equal to 1.

If a MOS transistor is used as a gate controlled resistor, the small-signal channel resistance R_m is calculated as:

$$R_m = \left.\frac{dV_{DS}}{dI_D}\right|_{V_{DS}=0} = \frac{1}{\beta(V_{GS} - V_{TH})} \quad (4.42)$$

Figure 4.9 shows the basic implementation of a two-input active voltage-to-voltage integrator based on overall feedback, in which the integration resistances are implemented as gate controlled MOS resistors. Additional

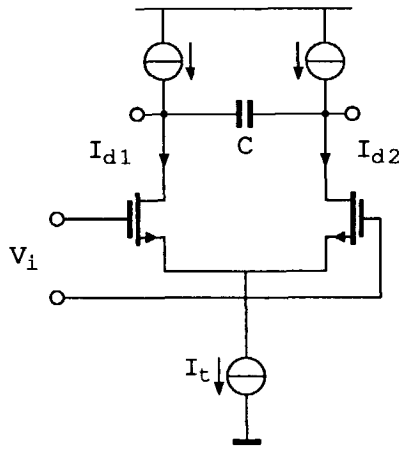

Figure 4.8: Transconductance integrator.

inputs can be realised by adding additional MOS resistors at the input. The small-signal transfer of this so-called Miller integrator is written as:

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{2sR_mC} \tag{4.43}$$

The integration resistance R is the series circuit of two MOS resistors, so $R = 2R_m$. Since the equivalent integration capacitance is the series circuit of the two feedback capacitors, the factor m in Equation 4.33 to 4.37 is equal to 4. Active filter structures built up with Miller integrators are known in the literature as active RC filters or MOSFET-C filters [23, 24].

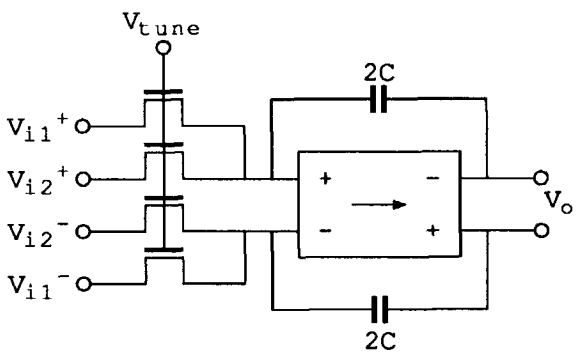

Figure 4.9: Two input Miller integrator.

In two subsequent subsections, the intermodulation-free dynamic range (IMFDR) of the audio filter implemented with transconductance integrators

and with Miller integrators will be calculated. The total filter noise has been calculated in Section 4.2. The strongest interfering signal levels appear at the input of the first integrator and consequently, the selectivity degradation by intermodulation distortion is mainly determined by the nonlinearity of the first integrator.

The drain-source noise current density $S(I_{dn})$ of a MOS transistor at low frequencies can be written as:

$$S(I_{dn}) = 4kT\beta(V_{GS} - V_{TH})\frac{2}{3}\frac{1+\alpha+\alpha^2}{1+\alpha} + \frac{K_F I_D}{WLC_{ox}}\frac{1}{f} \tag{4.44}$$

The left hand term expresses the thermal noise according to [22, p. 340], while the right hand term expresses the 1/f noise according to [25]. In this equation, W denotes the transistor length, L denotes the transistor width, K_F denotes the 1/f noise factor and C_{ox} denotes the oxide capacitance per unit area. The factor α is equal to 0 in the saturation region and approaches to 1 in the triode region for small drain-source voltages.

4.3.1 IMFDR of the audio filter using transconductance integrators

According to Equation 4.44, the drain current noise density of a MOS transistor in the saturation region is equal to:

$$S(I_{dn}) = 4kT\frac{2}{3}\beta(V_{GS} - V_{TH}) + \frac{K_F I_D}{WLC_{ox}}\frac{1}{f} \tag{4.45}$$

With g_m according to Equation 4.40, the equivalent input noise voltage of the source-coupled pair is calculated as:

$$S(V_i) = 4kT\frac{2}{3}\frac{2}{g_m}\left(1 + \frac{f_l}{f}\right) \tag{4.46}$$

In this equation, the corner frequency f_l, for which the 1/f noise is equal to the thermal noise, is equal to:

$$f_l = \frac{3g_m K_F}{16kT\beta WLC_{ox}} \tag{4.47}$$

In practice, f_l is in the order of magnitude of 300kHz for NMOS transistors and f_l is in the order of magnitude of 10kHz for PMOS transistors.

With an integration resistance equal to $2/g_m$, the integrator noise figure F results in:

$$F = \frac{2}{3}\left(1 + \frac{f_l}{f}\right) \tag{4.48}$$

This noise figure is further enlarged by additional noise generated by the bias current sources. It has been shown in [26, 27] that the noise figure resulting from the thermal noise of these current sources $F = 8$. The 1/f noise makes this noise figure even worse.

Using the drain-current formula according to Equation 4.38, the large signal nonlinear transfer of a source-coupled pair is calculated as:

$$i_{d1} - i_{d2} = v_i\sqrt{\beta I_T}\sqrt{1 - \frac{\beta v_i^2}{4I_T}} \tag{4.49}$$

This equation is valid for input voltages in the range:

$$|v_i| \leq \sqrt{\frac{2I_T}{\beta}}$$

otherwise, $|i_{d1} - i_{d2}| = I_T$. For small signals ($\beta v_i^2 \ll 4I_T$), the small-signal linearised transfer is obtained:

$$\frac{i_{d1} - i_{d2}}{v_i} = \sqrt{\beta I_T} = g_m \tag{4.50}$$

which has already been calculated in Equation 4.41.

For the calculation of the intermodulation distortion, Equation 4.49 will be approximated by a Taylor series up to the third order. If we substitute:

$$x = \sqrt{\frac{\beta}{4I_T}}v_i = \frac{v_i}{V_Y}$$

and:

$$y = \frac{i_{d1} - i_{d2}}{I_T}$$

Equation 4.49 is transformed into:

$$y = 2x\sqrt{1 - x^2} \tag{4.51}$$

and the derivatives are calculated as:

$$\frac{dy}{dx} = 2\frac{1-2x^2}{\sqrt{1-x^2}} \tag{4.52}$$

$$\frac{d^2y}{dx^2} = \frac{4x^3-6x}{(1-x^2)^{\frac{3}{2}}} \tag{4.53}$$

$$\frac{d^3y}{dx^3} = \frac{-6}{(1-x^2)^{\frac{5}{2}}} \tag{4.54}$$

The transfer from the differential input voltage to the differential output current of a source-coupled pair, written as a Taylor series up to the third order around $v_i = 0$, is finally written as:

$$i_{d1} - i_{d2} = I_T\left(2\frac{v_i}{V_Y} - 3\epsilon\left(\frac{v_i}{V_Y}\right)^2 - \left(\frac{v_i}{V_Y}\right)^3\right) \tag{4.55}$$

In this equation, ϵ denotes a small unbalance in the source-coupled pair.

The second- and third-order intermodulation distortion of two sine waves with equal amplitude $\hat{v}_i$ is equal to:

$$\mathrm{IM}_2 = \frac{3\epsilon\hat{v}_i}{2V_Y} \tag{4.56}$$

$$\mathrm{IM}_3 = \frac{3\hat{v}_i^2}{8V_Y^2} \tag{4.57}$$

With V_i the rms input voltage of one of the sine waves, the intermodulation expressed in dB is equal to:

$$\mathrm{IM}_2 = -20\log\left[\frac{3\epsilon V_i}{\sqrt{2}V_Y}\right] \tag{4.58}$$

$$\mathrm{IM}_3 = -20\log\left[\frac{3V_i^2}{4V_Y^2}\right] \tag{4.59}$$

With V_{no} the filter output noise voltage, the second- and third-order IMFDR of the complete filter, under the assumption that the intermodulation is determined by the first integrator, is finally calculated as:

$$\mathrm{IMFDR}_2 = 20\log\sqrt{\frac{\sqrt{2}V_Y}{3\epsilon V_{no}}} \tag{4.60}$$

$$\mathrm{IMFDR}_3 = 20\log\sqrt[3]{\frac{4V_Y^2}{3V_{no}^2}} \tag{4.61}$$

As a numerical example, $V_Y = 2\text{V}$, $C_{tot} = 1\text{nF}$, $F = 8$ and $\epsilon = 0.01$ is taken. The total output noise voltage V_{no} according to Equation 4.36 is $37\mu\text{V}$, which results in a second-order IMFDR of 64dB and a third-order IMFDR of 64dB.

4.3.2 IMFDR of the audio filter using Miller integrators

According to Equation 4.44, the thermal noise of a MOS transistor in the triode region is calculated as:

$$S(I_D) = 4kT\beta(V_{GS} - V_{TH}) = 4kTR_m \tag{4.62}$$

With $I_D = 0$, the 1/f noise is totally absent. If we neglect the influence of the signal induced 1/f noise, the noise of a gate controlled MOS resistance is equal to that of its equivalent ohmic resistance. If the amplifier is well designed (see Section 4.5), its noise contribution can be neglected, so $F = 1$.

For the calculation of the third-order IMFDR, the simple drain-current formula according to Equation 4.38 results in an infinite value. For this purpose, a more accurate drain-current formula according to [28] or [22, p. 120] is taken:

$$\begin{aligned} I_D &= \beta((V_{GS} - V_{FB} - \phi_B)V_{DS} - \frac{1}{2}V_{DS}^2 \\ &\quad + \frac{2}{3}\gamma(V_{SB} + \phi_B)^{\frac{3}{2}} - \frac{2}{3}\gamma(V_{SB} + V_{DS} + \phi_B)^{\frac{3}{2}}) \end{aligned} \tag{4.63}$$

In this equation, V_{SB} denotes the source-bulk voltage, V_{FB} denotes the flat band voltage, ϕ_B denotes the surface Fermi potential and γ denotes the body coefficient in $\text{V}^{0.5}$.

Because of the 3/2 powers, this drain-current formula is preferred to be simplified with a minimum loss of accuracy. This can be done by using a Taylor series expansion up to the third order around $V_{DS} = 0$. The derivatives of the drain current are calculated as:

$$I_D|_{V_{DS}=0} = 0 \tag{4.64}$$

$$\left.\frac{dI_D}{dV_{DS}}\right|_{V_{DS}=0} = V_{GS} - V_{FB} - \phi_B - \gamma(V_{SB} + \phi_B)^{\frac{1}{2}} \tag{4.65}$$

$$\left.\frac{d^2I_D}{dV_{DS}^2}\right|_{V_{DS}=0} = -1 - \frac{\gamma}{2}(V_{SB} + \phi_B)^{-\frac{1}{2}} \tag{4.66}$$

$$\left.\frac{d^3I_D}{dV_{DS}^3}\right|_{V_{DS}=0} = \frac{\gamma}{4}(V_{SB} + \phi_B)^{-\frac{3}{2}} \tag{4.67}$$

The first derivative is equal to $V_{GS} - V_{TH}$, in which the threshold voltage is equal to:

$$V_{TH} = V_{FB} + \phi_B + \gamma(V_{SB} + \phi_B)^{\frac{1}{2}} \tag{4.68}$$

Mind that the threshold voltage increases with increasing source-bulk potential, which is called the body effect.

The virtually grounded source is biased on the common-mode voltage V_{CM}. With the effective bulk potential V_B, defined as:

$$V_B = (V_{SB} + \phi_B) = (V_{CM} + \phi_B) \tag{4.69}$$

the drain-current formula is written as:

$$I_D = \beta\left((V_{GS} - V_{TH})V_{DS} - (\frac{1}{2} + \frac{\gamma}{4}V_B^{-\frac{1}{2}})V_{DS}^2 + \frac{\gamma}{24}V_B^{-\frac{3}{2}}V_{DS}^3\right) \tag{4.70}$$

If the body coefficient $\gamma \ll \sqrt{V_B}$, this equation can be reduced to:

$$I_D = \beta\left((V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2 + \frac{\gamma}{24}V_B^{-\frac{3}{2}}V_{DS}^3\right) \tag{4.71}$$

This equation is just an extension of the drain-current formula according to Equation 4.38, extended with a third-power term.

Due to the body effect, the triode region will be limited to:

$$V_{DS} < V_{GS} - V_{TD} \tag{4.72}$$

in which V_{TD} is the threshold voltage at the drain side:

$$V_{TD} = V_{FB} + \phi_B + \gamma(V_B + V_{DS})^{\frac{1}{2}} \tag{4.73}$$

For proper second-order nonlinearity cancellation, the amplifier must have a balanced voltage output [23, 24]. This implies an accurate control of the output common-mode voltage. Under this condition, the input drain current $i_{d1} - i_{d2}$ as a function of the differential input voltage v_i is equal to:

$$i_{d1} - i_{d2} = \beta\left\{V_G v_i - \frac{\epsilon}{2}v_i^2 + \frac{\gamma}{96}V_B^{-\frac{3}{2}}v_i^3\right\} \tag{4.74}$$

In this Equation, $V_{GS} - V_{TH}$ is expressed by V_G for short and ϵ denotes a small unbalance. The balanced configuration compensates even-order distortion, but has no significant effect on the first-order transfer and the odd-order distortion.

With $\hat{v}_i$ the amplitude of two input sine waves with equal amplitude, the intermodulation distortion can be calculated as:

$$\mathrm{IM}_2 = \frac{\epsilon \hat{v}_i}{2V_G} \tag{4.75}$$

$$\mathrm{IM}_3 = \frac{\gamma \hat{v}_i^2}{128 V_B^{\frac{3}{2}} V_G} \tag{4.76}$$

With V_i the rms voltage of two input sine waves, intermodulation expressed in dB is equal to:

$$\mathrm{IM}_2 = -20 \log \left[\frac{\epsilon V_i}{\sqrt{2} V_G} \right] \tag{4.77}$$

$$\mathrm{IM}_3 = -20 \log \left[\frac{\gamma V_i^2}{64 V_B^{\frac{3}{2}} V_G} \right] \tag{4.78}$$

With V_{no} the filter output noise voltage, the second- and third-order IMFDR of the complete filter, under the assumption that the intermodulation is determined by the first integrator, is finally calculated as:

$$\mathrm{IMFDR}_2 = 20 \log \sqrt{\frac{\sqrt{2} V_G}{\epsilon V_{no}}} \tag{4.79}$$

$$\mathrm{IMFDR}_3 = 20 \log \sqrt[3]{\frac{64 V_B^{\frac{3}{2}} V_G}{\gamma V_{no}^2}} \tag{4.80}$$

As a numerical example $V_G = 2\mathrm{V}$, $V_B = 3\mathrm{V}$, $C_{tot} = 1\mathrm{nF}$, $\epsilon = 0.01$ and $\gamma = 0.28\mathrm{V}^{0.5}$ is taken. The total output noise voltage according to Equation 4.36 is equal to $26\mu\mathrm{V}$, which results in the second-order IMFDR of 70dB and a third-order IMFDR of 84dB.

4.3.3 Conclusion

If we compare the performance of the audio filter built up with transconductance integrators and the audio filter built up with Miller integrators, the Miller integrator or MOSFET-C implementation has the largest IMFDR. However, we must keep in mind that the applied MOS models do not cover all higher-order effects. Although the linearity and hence the IMFDR of the transconductance integrators can be improved by the application of linearising techniques (see eg. [29, 30]), the MOSFET-C implementation is still

favoured because of the minimum 1/f noise contribution and hence a lower noise floor at low frequencies. Provided that the circuits are well balanced and the amplifiers are well designed, the MOSFET-C implementation provides for a sufficiently large IMFDR.

At the moment we can conclude that MOSFET-C filters offer the highest performance for low-frequency applications. For high-frequency applications however, where the influence of 1/f noise is negligible and the symmetrical amplifier is difficult to design properly, the transconductance integrator implementation will be preferred [31].

4.4 Autotuning techniques

The autotuning techniques presented in this section relate the absolute value of the time constants of one or more additional integrators, implemented on the same chip as the filter itself, to a reference frequency. If all equivalent resistances are simultaneously tuned, the value of the −3dB angular frequency ω_c, is related to the reference frequency as well. The accuracy of these indirect autotuning techniques is determined by the matching of the integration resistances and the capacitors, which is generally within a few percent.

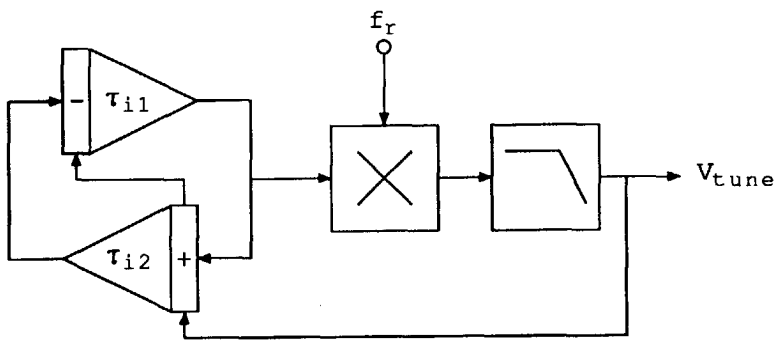

Figure 4.10: PLL autotuning principle.

Figure 4.10 shows one of the frequently used autotuning techniques [23, 31]. This autotuning technique is based upon a PLL, in which the VCO is implemented as a two-integrator oscillator. With τ_{i1} and τ_{i2} denoting the time constants of the oscillator integrators, the oscillator frequency for linear operation is equal to:

$$f_o = \frac{1}{2\pi\sqrt{\tau_1\tau_2}} \tag{4.81}$$

This oscillator frequency and hence the −3dB angular frequency f_c, are locked onto the reference frequency.

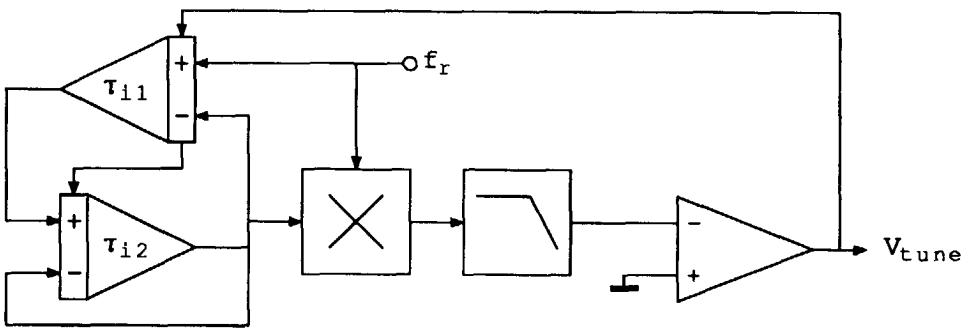

Figure 4.11: Phase discriminator autotuning principle.

Figure 4.11 shows another frequently used autotuning technique [23]. This autotuning technique is based upon a voltage controlled phase discriminator using the phase transfer of a BIQUAD. The phase transfer of the BIQUAD can be written as:

$$\arg\left(H(\omega)\right) = -\arctan\left(\frac{\omega\tau_{i1}}{1-\omega^2\tau_{i1}\tau_{i2}}\right) \tag{4.82}$$

In the stationary state, a zero mixer output corresponds to a 90° phase transfer, at which the time constants are tuned to:

$$\sqrt{\frac{1}{\tau_{i1}\tau_{i2}}} = 2\pi f_r \tag{4.83}$$

With this autotuning technique, several inherent difficulties of the two-integrator oscillator (startup problems and saturation effects) and lock-in problems of the PLL are avoided.

A principal drawback of these two autotuning techniques is the overhead of two integrators, while one integrator for autotuning purposes would be sufficient. The PLL autotuning technique can be implemented with only one integrator as a part of first-order oscillator according to Figure 4.12. Since the same reference voltage can be used for the integrator input and the Schmitt-trigger reference levels, the oscillator frequency does not depend on that reference voltage. This Schmitt trigger also provides for a stable amplitude. The oscillator frequency is equal to:

$$f_o = \frac{1}{4\tau_i} \tag{4.84}$$

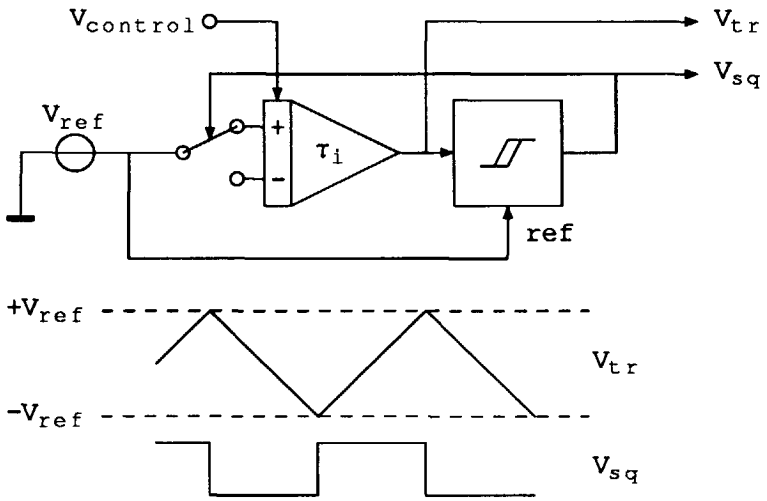

Figure 4.12: Integrator used in a first-order oscillator.

in which τ_i is the integration time constant.

Figure 4.13 shows an elegant autotuning technique, in which the integration time constant of only one additional integrator is compared with a reference time. The timing and control is performed directly with switches, which are driven by the reference timing signals φ_1, φ_2 and φ_3. Just like the phase discriminator principle, startup and lock-in problems are avoided, but this method requires only one overhead integrator. Besides, the sampling switch φ_3 provides for a minimum ripple on the gate tuning voltage. For these reasons, this autotuning technique is preferred. In the rest of this section this technique, which will be called the direct sampling tuning technique, is analysed in more detail.

The timing diagram is shown in the lower part of Figure 4.13. During the time φ_1 is active, the integrator capacitors are short circuited forcing the output differential voltage to zero. During the time interval t_2, in which φ_2 is active, a fixed differential input voltage is connected to the integrator input, which results in a ramp voltage at the integrator output. Finally, when φ_3 gets active, the integrated voltage is sampled into the capacitor C_H. This sampled voltage passes through the low-pass filter, implemented with a transconductance G_M and a capacitor C_F, to the gates of all MOS resistors.

In the stationary state, the final sampled voltage V_S is equal to the reference voltage V_R and the sampled and filtered resistor tuning voltage

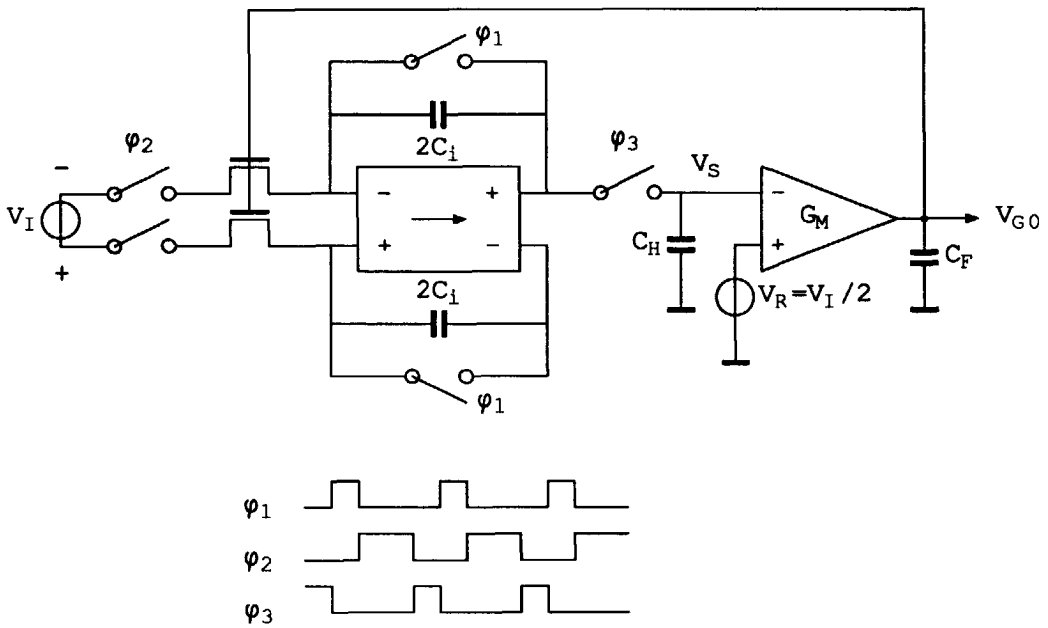

Figure 4.13: Direct sampling tuning technique.

remains constant with no ripple. If the reference voltage V_R is made half the integrator input voltage V_I, the integrator time constant is directly related to the integration time t_2, during which φ_2 is active:

$$V_S = V_I \frac{t_2}{2\tau_i} = V_R = \frac{V_I}{2} \tag{4.85}$$

This equation results in:

$$\tau_i = t_2 \tag{4.86}$$

In other words, the integration time constant τ_i, and indirectly all other integration time constants are related to a reference clock time t_2.

Figure 4.14 shows the timing circuitry, which is based upon a master-slave divider. The timing signals φ_1, φ_2 and φ_3 are derived from the output signals Q_1 and Q_2 of latch 1 and latch 2 respectively. Since Q_1 and Q_2 are in quadrature, critical race conditions are avoided and the timing signals are free of spikes.

The stability of the sampled control loop would be no problem if the time constant C_F/G_M is made much larger than the autotuning cycle time $T_r = 1/f_r$. However, if all capacitors including C_F have to be implemented

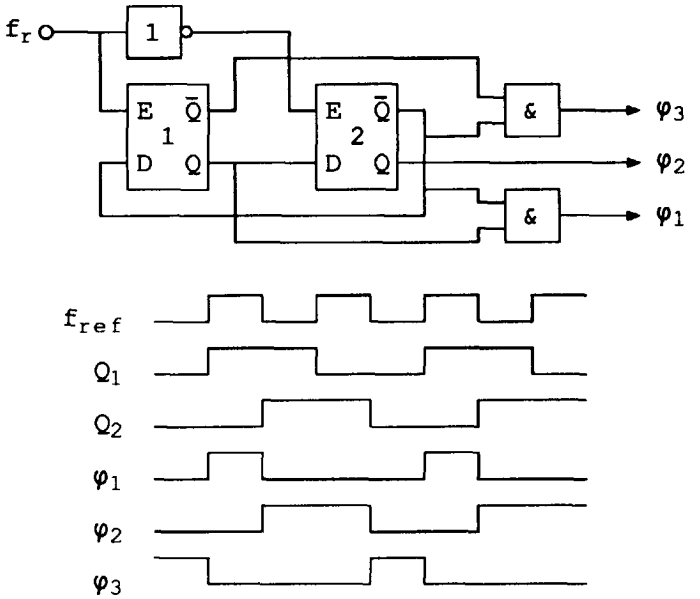

Figure 4.14: Autotuning timing circuitry.

on-chip, only a limited time constant C_F/G_M can be realised. Because the autotuning circuitry produces no inherent ripple on the resistor tuning voltage in the stationary state, the minimum C_F/G_M mainly depends on the loop stability.

The effective gate voltage $V_G = V_{GS} - V_{TH}$ of the MOS resistors is a result of an integration by G_M and C_F. This gate overdrive voltage can be written in the z-transform as:

$$V_G = \frac{1}{z-1}\frac{G_M T_r}{C_F}(V_R - V_S) \tag{4.87}$$

in which T_r denotes the autotuning cycle time. The reference time ($t = 0$) corresponds to the time ϕ_3 starts to become active.

The sampled voltage V_S can be written in the z-domain as:

$$2zV_S = \frac{\beta V_I T_r}{2C_i}V_G + \frac{3\beta V_I G_M T_r^2}{8C_i C_F}(V_R - V_S) \tag{4.88}$$

in which β denotes the proportionality factor in A/V^2 of the MOS resistors and V_I denotes the integrator input voltage.

Substituting V_G in Equation 4.88 by Equation 4.87 results in the z-transfer:

$$\frac{V_S}{V_R} = k\frac{3z+1}{8z^2+(3k-8)z+k} \tag{4.89}$$

in which:

$$k = \frac{\beta V_I G_M T_r^2}{2C_i C_F}$$

The root locus of this sampled system as a function of k is shown in Figure 4.15.

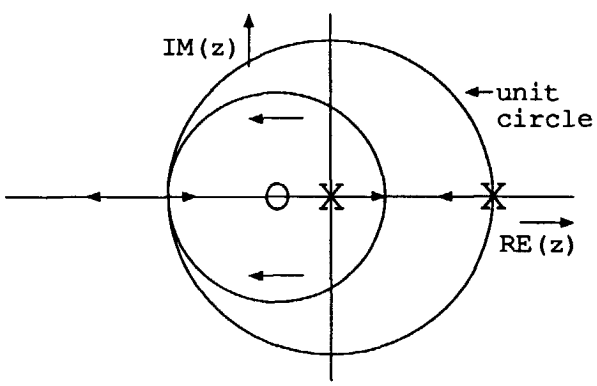

Figure 4.15: z-plane root locus of the sampling feedback loop.

The breakpoint in the root locus at the real axis occurs for $k = 8/9$ at $z = 1/3$ and for $k = 8$ at $z = -1$. For a stable autotuning system with a ripple free dynamic behaviour $k < 0.9$. However, a smaller value of k is preferred for minimum noise and ripple of the tuning voltage.

As a conclusion, we can state that the direct sampling tuning technique provides for a complete on-chip autotuning system with a minimum of overhead circuitry and a minimum ripple on the resistor tuning voltage.

4.5 Design of a prototype audio filter

This section deals with the design of a prototype audio filter on a BIMOS evaluation chip, containing a fourth-order MOSFET-C ladder filter according to Figure 4.16, a first-order MOSFET-C section according to Figure 4.17 and the autotuning circuitry based upon the direct sampling tuning method, described in Section 4.4. The first-order MOSFET-C section is included for test purposes as an active version of the prefilter.

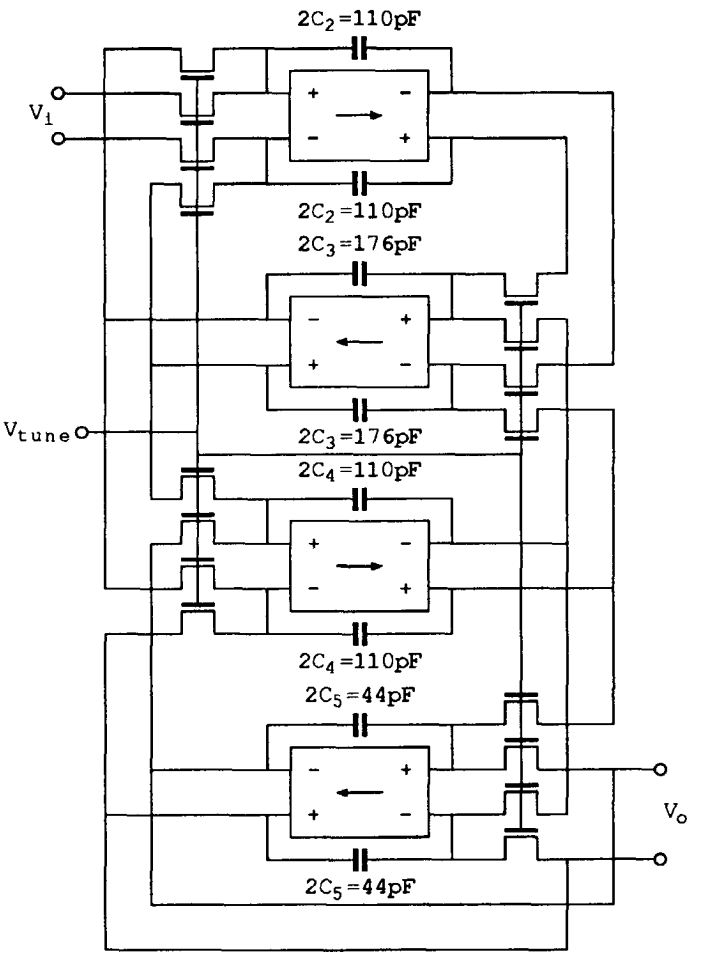

Figure 4.16: Fourth-order MOSFET-C ladder filter.

All circuits have to operate upon a single 8V supply and all MOS resistors are taken as equal for a maximum tracking accuracy. For a maximum

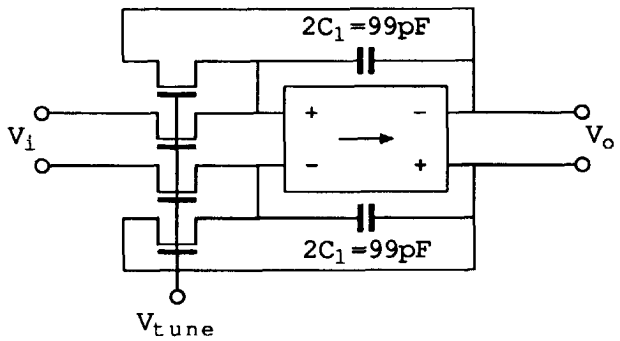

Figure 4.17: First-order MOSFET-C filter section.

IMFDR (see Equation 4.79 and 4.80), a NMOS resistor is taken, having the lowest body coefficient γ. Although a NMOS resistor is about three times longer than a PMOS resistor ($\beta_{\square n} \approx 3\beta_{\square p}$), the chip area occupied by the MOS resistors is still negligible compared with the chip area occupied by the capacitors. A maximum IMFDR also requires a maximum bulk voltage $V_B = V_{CM} + \phi_B$ and a maximum effective gate voltage $V_G = V_{GS} - V_{TH}$ within the available supply voltage and remaining a sufficient tuning range. For this reason, V_{CM} = 3V and a nominal V_G =2V has been chosen, which results in V_B = 3.55V and V_{TH} = 1.1V (see Equation 4.68). The resulting nominal gate voltage of 6.1V leaves an additional gate tuning voltage of nearly 2V and therefore a resistor tuning range of nearly 50% of its nominal value to infinity. This tuning range is sufficient for compensation of the process parameter tolerances.

For the nominal integration resistance R, a value of 1MΩ is chosen in order to keep the total capacitance of the fourth-order active filter part including the autotuning integration capacitance below 1nF. For a maximum matching of the capacitor values, all capacitors are built up with an integer number of unit capacitors. With a nominal integration resistance of 1MΩ and a nominal cut-off frequency f_c of 3.2kHz, the resulting capacitor values are calculated as:

$$2C_1 = 1/R\omega_0 = 99\text{pF} = 9C_0 \quad (4.90)$$

$$2C_2 = \tfrac{1}{2}\sqrt{5}C_1 = 110\text{pF} = 10C_0 \quad (4.91)$$

$$2C_3 = \tfrac{4}{5}\sqrt{5}C_1 = 176\text{pF} = 16C_0 \quad (4.92)$$

$$2C_4 = \tfrac{1}{2}\sqrt{5}C_1 = 110\text{pF} = 10C_0 \quad (4.93)$$

$$2C_5 = \tfrac{1}{5}\sqrt{5}C_1 = 44\text{pF} = 4C_0 \quad (4.94)$$

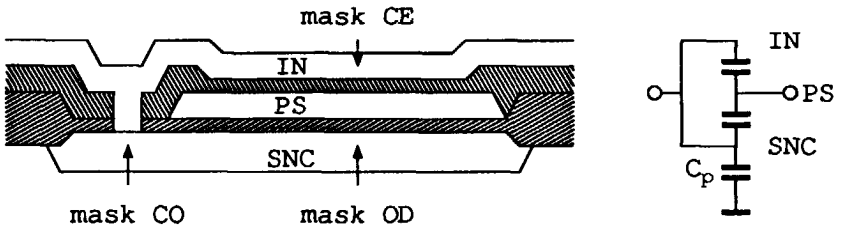

Figure 4.18: Structure of a MOS sandwich capacitor.

The unit capacitance C_0 = 11pF and the total capacitance of the fourth-order MOSFET-C ladder filter is $80C_0$ = 880pF. The resulting output noise according to Equation 4.36 is calculated as:

$$\overline{V}_{no} = \sqrt{\frac{164kT}{880.10^{-12}}} = 28\mu\text{V} \tag{4.95}$$

With an effective gate voltage V_G = 2V and a bulk voltage $V_B = 3.55V$ the IMFDR_2 according to Equation 4.79 is equal to 70dB for 1% unbalance and the IMFDR_3 according to Equation 4.80 is equal to 84dB for a body coefficient $\gamma = 0.28\text{V}^{1/2}$. The noise contribution of the amplifiers has been neglected.

The combination of a NMOS channel resistance R_m = 500kΩ and an effective gate voltage V_G = 2V requires a β equal to $1\mu\text{A/V}^2$. PHILPAC simulations show that the effective gate width of an NMOS transistor with the minimum mask width of 2.5μm is only 2μm. With a square β of 45μA/V for an NMOS resistor, the resulting mask length is 90μm.

The 11pF unit capacitance is realised as a IN1-CE-PS-SNC sandwich capacitor according to Figure 4.18. Due to the thin oxide defined by the CE mask, the total capacitance per unit area is nearly twice the ordinary gate oxide capacitance. The parasitic bottom-plate capacitance at zero bias voltage is about 1.2pF. If the bottom plate is biased to the common-mode bias voltage V_{CM}, its capacitance is reduced to:

$$C_p = \frac{C_{p0}}{(1 + \frac{V_{CM}}{\phi_j})^{m_j}} \tag{4.96}$$

in which ϕ_j denotes the junction build in voltage and m_j denotes the grading coefficient. For the SNC-to-substrate junction, ϕ_j = 0.8V and m_j = 0.5, which results in a parasitic capacitance of 0.55pF for V_{CM} = 3V. The dimension of this 11pF unit capacitor is about 110 × 110μm.

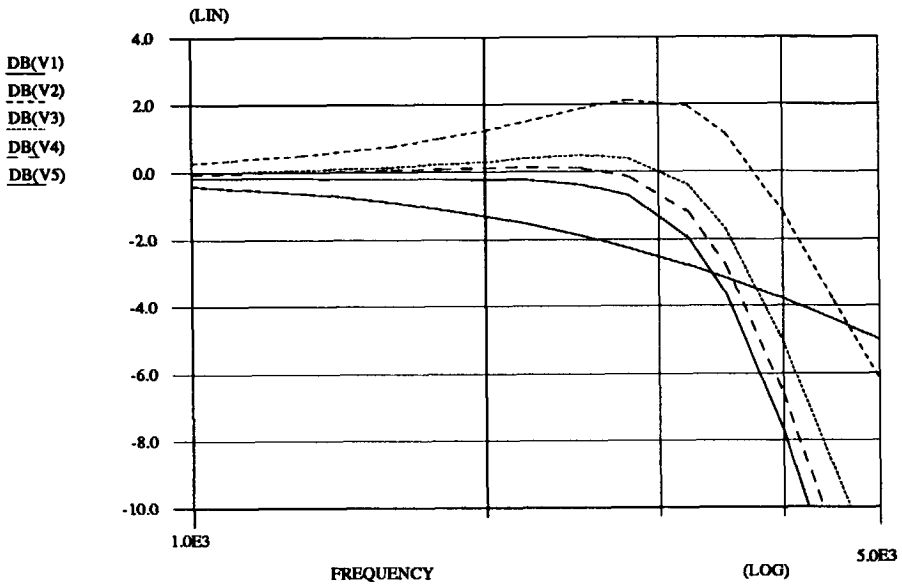

Figure 4.19: Detail of the internal transfers of the fourth-order MOSFET-C filter, preceded by the first-order prefilter from 1kHz to 5kHz.

The normalised internal amplitude transfer of the cascade of the first-order (active or passive) prefilter and the fourth-order MOSFET-C ladder filter $|H_i(\Omega)|$ is the transfer from the filter input to the output of section i. The normalised frequency Ω is equal to f/f_c or ω/ω_c. Obviously, $|H_1(\Omega)|$ is the transfer of the prefilter and $|H_5(\Omega)|$ is the overall Butterworth filter transfer. The normalised internal amplitude transfers are calculated as:

$$|H_1(\Omega)|^2 = \frac{1}{1+\Omega^2} \tag{4.97}$$

$$|H_2(\Omega)|^2 = \frac{1+\Omega^2+0.8\Omega^6}{1+\Omega^{10}} \tag{4.98}$$

$$|H_3(\Omega)|^2 = \frac{1+0.25\Omega^2+0.25\Omega^4}{1+\Omega^{10}} \tag{4.99}$$

$$|H_4(\Omega)|^2 = \frac{1+0.2\Omega^2}{1+\Omega^{10}} \tag{4.100}$$

$$|H_5(\Omega)|^2 = |H(\Omega)|^2 = \frac{1}{1+\Omega^{10}} \tag{4.101}$$

Numerical analysis of these transfers show that the maximum overshoot is about 2dB for $|H_2(\Omega)|$, about 0.5dB for $|H_3(\Omega)|$ and less than 0.2dB for $|H_4(\Omega)|$ at $\Omega \approx 1$. This overshoot has practically no effect upon the overall in-band dynamic range. The results of a PHILPAC simulation of these transfers in the frequency range of 1–5kHz is shown in Figure 4.19.

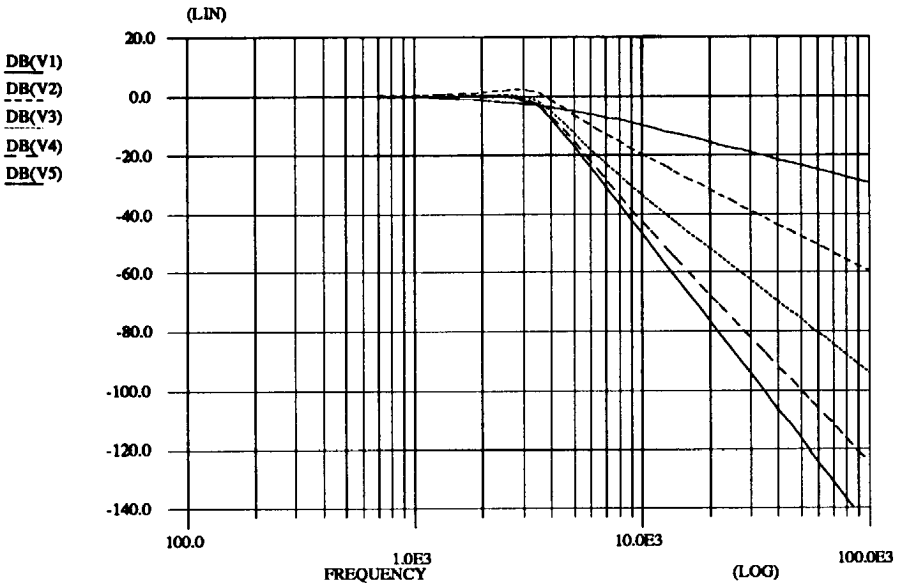

Figure 4.20: Internal transfers of the fourth-order MOSFET-C filter, preceded by the first-order prefilter.

At the adjacent channel frequency, for which $f = 9$kHz and (with $f_c = 3.2$kHz) $\Omega = 2.8$, the amplitude transfers are equal to:

$$\begin{aligned} -20\log|H_1(\Omega)| &= 9\text{dB} \\ -20\log|H_2(\Omega)| &= 18\text{dB} \\ -20\log|H_3(\Omega)| &= 33\text{dB} \\ -20\log|H_4(\Omega)| &= 40\text{dB} \\ -20\log|H(\Omega)| &= 45\text{dB} \end{aligned}$$

As we can see, the strongest interfering signals appear at the prefilter and the input MOS resistors of the fourth-order ladder filter, so selectivity degradation by intermodulation distortion in the active part of the audio filter

mainly occurs at the input MOS resistors. Results of a PHILPAC simulation of these transfers in the frequency range of 100Hz to 100kHz are shown in Figure 4.20. The measured transfers can hardly be distincted from the simulated and calculated ones.

4.5.1 Design of a symmetrical amplifier

As already mentioned at the beginning of this chapter, the filter must be able to handle signal frequencies up to 1MHz, at which frequency the prefilter takes over the complete detector selectivity. This design aspect is translated into a minimum amplifier gain-bandwidth of 1MHz.

Since optimal even-order nonlinearity cancellation requires optimal balancing, an output common-mode feedback control loop is applied, for which the loop gain nearly equals the amplifier gain. In order to keep the unbalance well below 1% even if a strong interfering 9kHz beat note resulting from a strong adjacent channel is present, the amplifier gain must be 40dB minimally at 9kHz. The differential-mode loop gain resulting from a 40dB amplifier gain for the audio frequency range is sufficient for an accurate filter response.

If the maximum signal handling capability of the entire filter has to be determined by the MOS resistors rather than by the amplifiers, the minimum output swing of the amplifiers should be larger than the signal handling capability of the MOS resistors. With a nominal effective gate voltage V_G = 2V for the MOS resistors, the minimum amplifier output swing must be $2V_p$ for each output

Amplifier configuration

The first stage must provide for a high input common-mode rejection in combination with a high gain and a minimum noise contribution. A high common-mode rejection is important for proper balancing and in order to prevent common-mode instability by parasitic common-mode loops within the filter. These demands can be fulfilled with a PMOS source-coupled pair, having much less excess noise than a NMOS source-coupled pair. As already calculated in Section 4.3, the equivalent input noise voltage of a source-coupled pair is equal to:

$$S(v_{ni}) = \frac{16kT}{3g_m}\left(1 + \frac{f_l}{f}\right) \tag{4.102}$$

For the relevant filter frequencies, the equivalent input noise current can be neglected. With a low bias current of some tens of micro amperes, the corner frequency f_l of the PMOS input transistors is limited to 10kHz or even lower. The 1/f noise can be neglected in the weighed audio spectrum if the overall corner frequency of the integrator does not exceed 500Hz, which results in $g_m > 80/3R = 27\mu A/V$. In this case, the thermal noise of the amplifier is completely negligible and the filter noise is determined by the noise of the integration resistances only.

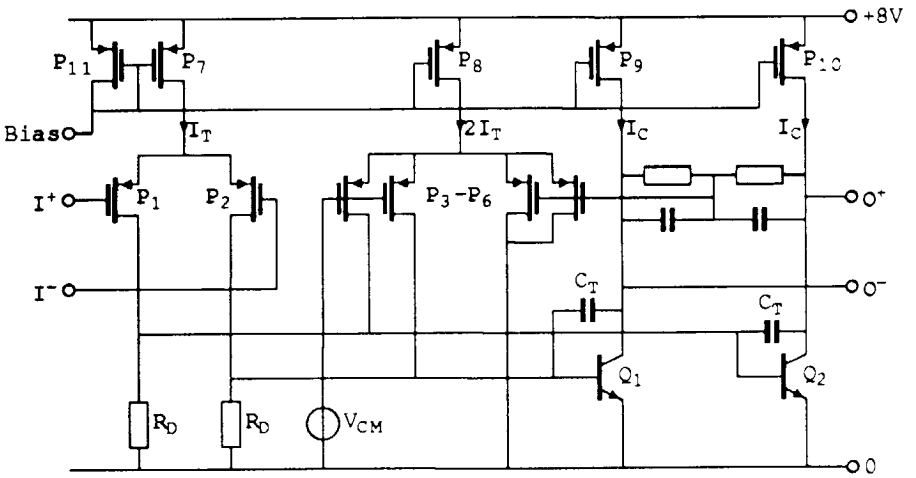

Figure 4.21: Symmetrical amplifier with common-mode feedback.

Unfortunately, the equivalent input noise voltage of the amplifier is determined by the NMOS drain current sinks as well. Consequently, the high 1/f noise of these NMOS transistors completely dominates over the total noise of the PMOS input stage. The loss of amplifier gain if these current sinks are replaced by ordinary resistors is unacceptable, unless the second stage is implemented with bipolar transistors. The amplifier configuration, in which the first stage is a PMOS source-coupled pair and the second stage is built up with two NPN transistors in CE configuration, is shown in Figure 4.21. The output voltage swing of this bipolar output stage is nearly rail-to-rail.

Accurate common-mode sensing is performed with two diffused resistors and the double source-coupled pair provides for a maximum common-mode

accuracy (see also [32]). The capacitors C_T are implemented for phase compensation.

Small-signal behaviour

The small-signal differential-mode behaviour of the two stage amplifier will be modelled with its single ended equivalent shown in Figure 4.22. In this figure, g_{mp} is the transconductance of the PMOS transistors, g_{mn} is the transconductance of the NPN transistors, R_D is drain resistor, r_π is the bipolar transistor input resistance and R_L is the load resistance. If the NPN transistor is biased on a low tail current ($\approx 100\mu$A) the influence of the base resistance can be neglected.

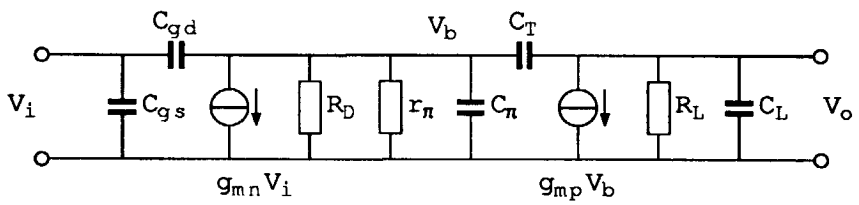

Figure 4.22: Small-signal ac differential-mode model of the amplifier.

The small-signal low-frequency differential-mode voltage gain of this amplifier according to Figure 4.22 is calculated as:

$$G_{dm} = g_{mp}\frac{R_D r_\pi}{R_D + r_\pi} g_{mn} R_L = \sqrt{\beta I_T}\frac{R_D}{R_D + \beta_f V_T/I_C}\beta_f R_L \qquad (4.103)$$

in which β is the PMOS proportionality factor, I_T is the differential input stage tail current, β_f is the NPN current gain, V_T is the thermal voltage and I_C is the collector bias current. If the tail current of the double source-coupled pair (P_3—P_6) is twice the tail current of the input source-coupled pair and if we neglect the base current, $R_D = V_{BE}/I_T$, in which V_{BE} is the base emitter voltage. For a given collector bias current I_C a maximum voltage gain is found if:

$$I_T = \frac{V_{BE} I_C}{\beta_f V_T} \qquad (4.104)$$

and consequently, $R_D = r_\pi$. This maximum voltage gain is equal to:

$$G_{dm} = \frac{g_{mp} R_L \beta_f}{2} \qquad (4.105)$$

The high-frequency behaviour of the MOS transistors is modelled with the capacitances C_{gs} and C_{gd}. For a MOS transistor biased in its saturation region, C_{gs} nearly equals 2/3 of the oxide capacitance, while C_{gd} is determined by the gate-drain overlap capacitance, which is practically negligible compared with the other capacitors. The capacitance C_π is the base emitter capacitance of the NPN transistor, while the collector base capacitance is incorporated in the compensation capacitor C_T. For high frequencies, the integration capacitor can be regarded as a unity feedback, so the influence of the gate-source capacitance and the parasitic substrate capacitance of the integration capacitors can be incorporated in the total load capacitance C_L.

Under the condition that $R_D = r_\pi$, the small-signal ac differential-mode transfer according to Figure 4.22 can be written as:

$$\frac{V_o(s)}{V_i(s)} = \frac{G_{dm}(1 - sC_T/g_{mn})}{1 + s(-1/p_1 - 1/p_2) + s^2/p_1p_2} \tag{4.106}$$

in which G_{dm} is given by Equation 4.105 and p_1 and p_2 are the poles of the amplifier, for which:

$$-\frac{1}{p_1} - \frac{1}{p_2} = r_\pi(C_\pi + C_T)/2 + R_L(C_L + C_T) + \beta_f R_L C_T/2$$

and

$$\frac{1}{p_1p_2} = R_L r_\pi(C_L C_T + C_\pi C_T + C_\pi C_L)/2$$

If the amplifier is properly phase compensated with C_T, then $p_1 \ll p_2$. With $\beta_f \gg 1$, $C_\pi \approx C_T$ and $\beta_f R_L \gg r_\pi$, these poles can be approximated by:

$$p_1 \approx -\frac{1}{R_L(C_L + \beta_f C_T/2)} \tag{4.107}$$

$$p_2 \approx -\frac{2 + \beta_f C_T/C_L}{r_\pi(C_T + C_\pi)} \tag{4.108}$$

The resulting unity-gain angular frequency ω_t is calculated as:

$$\omega_t = -G_{dm}p_1 = \frac{g_{mp}}{C_T + 2C_L/\beta_f} \tag{4.109}$$

Apart from these two poles, the transfer contains a right half plane zero located at:

$$z = +\frac{g_{mn}}{C_T} \tag{4.110}$$

This zero is shifted to infinity by taking a small resistor $R_T = 1/g_{mn}$ in series with C_T. The influence of R_T upon p_1 and p_2 is negligible. This resistor introduces a third non-dominant pole located at:

$$p_3 = -\frac{1}{R_T C_\pi} = -\frac{g_{mn}}{C_\pi} \approx -2\pi f_T \tag{4.111}$$

With f_T in the order of magnitude of 2GHz, the influence of this pole can be neglected.

The phase margin ϕ_m can be calculated as:

$$\phi_m = 180° + \arctan\left(\frac{\omega_t}{p_1}\right) + \arctan\left(\frac{\omega_t}{p_2}\right) \tag{4.112}$$

The most dominant pole p_1 gives a phase lag of 90° at ω_t. Now the phase margin can be written as:

$$\phi_m = 90° - \arctan\left(\frac{G_{dm}p_1}{p_2}\right) \tag{4.113}$$

in which:

$$\frac{G_{dm}p_1}{p_2} = \frac{g_{mp}}{g_{mn}} \frac{(C_T + C_\pi)C_L}{(C_T + 2C_L/\beta_f)^2} \tag{4.114}$$

A minimum required phase margin of 45° results in the relation:

$$\frac{g_{mn}}{g_{mp}} = \frac{(C_T + C_\pi)C_L}{(C_T + 2C_L/\beta_f)^2} \tag{4.115}$$

The small-signal behaviour of the common-mode feedback loop is similar to the unity-feedback differential-mode behaviour. The common-mode loop gain however is approximately half the differential-mode gain G_{dm}. Consequently, a 40dB common-mode loop gain requires a 46dB differential-mode voltage gain.

Dimensioning of a prototype amplifier

The amplifier of the prototype filter is dimensioned in order to handle additional resistive and capacitive output loads of test probes. For this purpose, the amplifier will be dimensioned for a load impedance $R_L \geq 50\text{k}\Omega$ and $C_L \leq 50\text{pF}$. The minimum unity-gain bandwidth has to be 1MHz with a minimum phase margin of 45°.

A collector current $I_C = 0.1\text{mA}$ is chosen in order to deliver the $60\mu\text{A}$ output current resulting from a 3V peak output voltage swing over a load

impedance $R_L = 50\text{k}\Omega$ at each output. The resulting g_{mn} is 4mA/V and V_{BE} is about 0.7V. With $\beta_f \approx 190$, $r_\pi = 48\text{k}\Omega$, so R_D has to be $48\text{k}\Omega$ as well and the tail current I_T has to be $15\mu\text{A}$ for a maximum voltage gain. The PMOS transconductance g_{mp} has to be at least $42\mu\text{A/V}$ for the required 46dB differential-mode voltage gain. With this value of g_m, the amplifier noise contribution can be neglected completely. A PMOS transistor with dimensions $W/L = 50/3\mu\text{m}$ is chosen, which results in $\beta = 250\mu\text{A/V}^2$, $g_{mp} = 61\mu\text{A/V}$ and a voltage gain $G_{dm} = 49dB$.

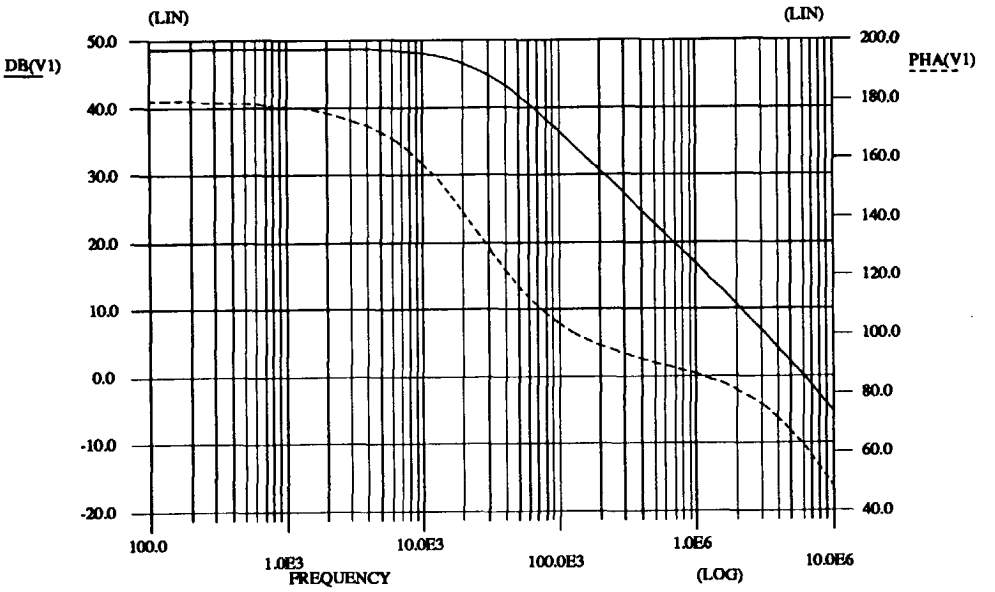

Figure 4.23: Differential-mode amplitude (straight line) and phase (dashed line) transfer of the amplifier with 50pF capacitive load at each output.

A compensation capacitor $C_T = 1\text{pF}$ is chosen, which results in a calculated unity-gain bandwidth of 6.4MHz ($C_L = 50\text{pF}$). With $C_\pi \approx 1\text{pF}$, the phase margin is calculated as:

$$\phi_m = 90^\circ - \arctan(0.66) = 57^\circ$$

and stability is guaranteed. Figure 4.23 shows a PHILPAC simulation of the amplifier differential-mode transfer with 50pF capacitive load. The effective load resistance R_L, in which the value of the common-mode sense resistors is incorporated is $50\text{k}\Omega$. The resulting simulated differential-mode gain is

48dB, while the simulated unity-gain bandwidth is 6.2MHz and the phase margin is 62°.

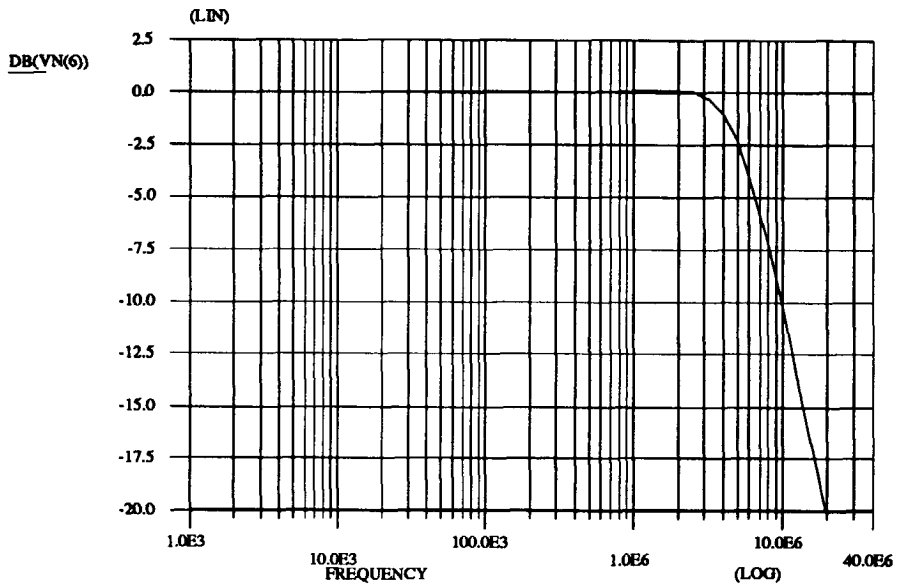

Figure 4.24: Common-mode transfer of the amplifier with 50pF capacitive load at each output.

The common-mode sense resistors are implemented as 100kΩ diffused resistors, being a compromise between the linearity, the loss of differential-mode gain and the occupied chip area. This linearity is important in order to obtain the exact common-mode output voltage independent of the differential-mode output voltage. For high frequencies, the phase lag of these diffused resistors is compensated with two parallel capacitors, of which the value of 0.3pF is determined empirically with the network simulator PHILPAC. The common-mode transfer is shown in Figure 4.24. The simulated common-mode −3dB bandwidth is 5.4MHz, obtained with a negligible overshoot. Measurement of the common-mode transfer results in a common-mode −3dB bandwidth of 6MHz with an overshoot of 1.5dB.

In conclusion, the previously stated amplifier specifications have been fulfilled with a relatively simple and uncritical two-stage BIMOS amplifier, in which the 1/f noise contribution has been minimised.

4.5.2 Implementation and dimensioning of the autotuning circuitry

The principle of autotuning, based on a direct sampling method, has been dealt with in Section 4.4. The tuned cut-off frequency of the filter as a function of the reference frequency f_r and the autotuning integration capacitor C_i was found to be:

$$f_0 = \frac{C_i}{2\pi C_1} f_r \tag{4.116}$$

The reference frequency will be derived from the synthesiser reference crystal frequency of 4MHz. In order to keep the frequency dividers as simple as possible, this frequency is preferred to be derived as a power of two from the crystal frequency. In this case, a reference frequency of 62.5kHz has been chosen. With $2C_1$ = 99pF, a 3.3kHz cut-off frequency is obtained if $2C_i$ = 33pF which is equal to 3 unit capacitances of 11pF each.

The switches are implemented as transmission gates according to Figure 4.25. The NMOS and PMOS have equal gate dimensions in order to minimise the clock feedthrough.

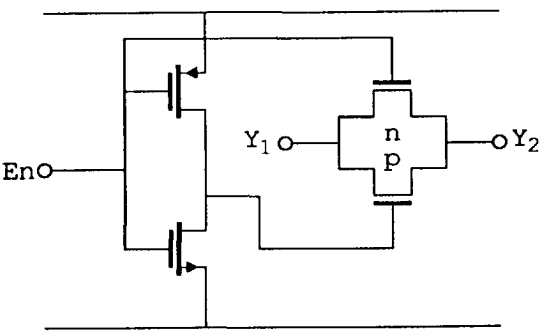

Figure 4.25: Implementation of a switch as a transmission gate.

For the capacitor C_F, a value of 200pF is chosen as a compromise between a minimum noise and ripple of the gate voltage and the required chip-area. The loop-gain factor k, calculated in Section 4.4 was found to be:

$$k = \frac{\beta V_I T_r}{2C_i} \frac{G_M T_r}{C_F} \tag{4.117}$$

In this Equation, $2C_i$ = 33pF, T_r = 32μs and β = 1μA/V^2. If k = 0.2 and V_I = 1V is chosen, the time constant C_F/G_M is calculated as:

$$\frac{C_F}{G_m} = 5T_r = 160\mu s \tag{4.118}$$

With C_F = 200pF, G_M = 1.25μA/V. The implementation of the transconductance amplifier is shown in Figure 4.26

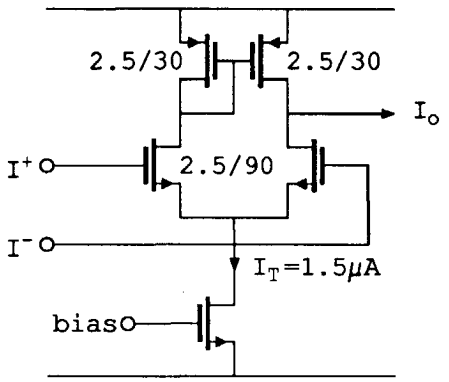

Figure 4.26: implementation of the transconductance amplifier.

4.5.3 Results and conclusions

As already noted, the measured frequency transfers can hardly be distincted from the simulated ones shown in Figure 4.19 and 4.20 (except for very high frequencies $f \gg$ 100kHz). The amplifier inputs are not connected to bonding flaps, so the amplifier transfer cannot be measured directly. The amplifier performance has been verified by measuring the common-mode −3dB bandwidth, which results in a −3dB bandwidth of 6MHz.

Measurement of the output spectral noise density results in a practically flat noise spectrum within the filter passband. This flat in-band noise floor corresponds within 1dB to the total thermal noise of all filter resistances. The overall corner frequency f_l, for which the 1/f noise dominates over the thermal noise is about 250Hz. If the audio weight function is taken in account, the 1/f noise contribution is completely negligible.

A 3.2kHz bandwidth of the prototype filter is obtained with a gate voltage of 6.5V with respect to the ground. The resulting effective gate voltage $V_G = V_{GS} - V_{TH}$ is 2.4V. Under this condition, the measured third-order intermodulation distortion of the input resistor pair is about −65dB at V_i = 1.2Vrms. The calculated intermodulation distortion according to Equation 4.78 with $\gamma = 0.28V^{0.5}$, V_G = 2.4V and V_B = 3.55V is −68dB. The measured second-order intermodulation is −58dB at V_i = 1Vrms (V_G = 2.4V and V_B = 3.55V). The calculated second-order intermodulation under this condition is −51dB for an unbalance ϵ = 0.01.

For the fourth-order MOSFET-C filter, being the active part of the audio filter, the calculated output noise calculated in Equation 4.95 is 28μV. This value is verified and confirmed by noise measurements. With a measured second-order intermodulation of -58dB at 1Vrms and a measured third-order intermodulation of -65dB at 1.2Vrms, the measured second- and third-order IMFDR is 74dB and 83dB respectively. These values correspond closely to the calculated second- and third-order IMDFR of 70dB and 84dB respectively.

At this stage, we can conclude that MOSFET-C filters provide for a sufficiently high IMFDR. The application of MOS resistors with zero bias current provide for an absolute minimum 1/f noise. With the BIMOS amplifier described in Subsection 4.5.1, both the thermal noise and the 1/f noise contribution of the amplifiers can be neglected and the filter noise is determined by that of the (MOS) resistors only [33].

The operation and the corresponding waveforms of the autotuning integrator correspond to the theory in Section 4.4. The accuracy of this autotuning system turns out to be determined by the matching of the integrator input voltage V_I and the reference voltage V_R of the transconductance amplifier (see Section 4.4) and the accuracy of the common-mode control. This implementation problem causes a systematic inaccuracy in the prototype autotuning system.

For a better accuracy, a fully balanced sample and comparator circuitry (C_H and G_M in Figure 4.13) should be applied. If properly implemented, the direct sampling tuning system provides for a sufficient accuracy (within 5%) with a minimum of overhead circuitry.

Chapter 5

Design of the synchronous detector LF circuits

This chapter is focussed upon the design of the post-detection AGC amplifier including the low-frequency autozero circuitry. The architecture of the synchronous detector can be found in Chapter 2, while the block diagram of the synchronous detector is drawn in Figure 2.6 on page 37.

In order to guarantee the required 50dB signal-handling dynamic range of the carrier regenerating PLL, the gain-control range of the AGC amplifier has to be at least 50dB. As already noticed in Section 1.5, the linearity requirement of the signal part of the AGC amplifier is based upon the maximum allowed audio distortion. A 0.5% total harmonic distortion for AM receivers is generally accepted. According to Section 1.3, the dynamic range of the amplifier has to be at least 90dB.

5.1 AGC circuit design

The LF AGC amplifier is implemented with bipolar transistors for a minimum 1/f noise contribution. Figure 5.1 shows two elementary bipolar current gain-control cells, called the AGC quad and the translinear Gilbert quad.

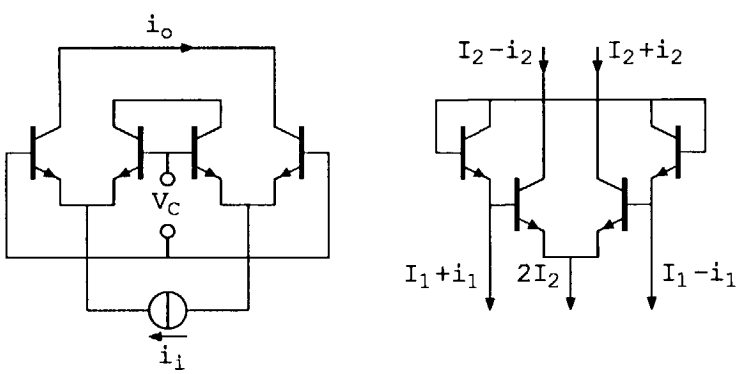

Figure 5.1: AGC quad (left) and Gilbert quad (right) as elementary bipolar current gain-control cells.

The small-signal transfer of the AGC quad in the left hand part of Fig-

ure 5.1 is equal to:

$$\frac{i_o}{i_i} = \frac{1}{2}\left[1 - \tanh\left(\frac{V_C}{2V_T}\right)\right] \tag{5.1}$$

In this equation, V_C is the gain-control voltage and V_T is the thermal voltage. The small-signal transfer of the Gilbert quad in the right hand side of Figure 5.1 can be written as:

$$\frac{i_2}{i_1} = \frac{I_2}{I_1} \tag{5.2}$$

in which I_1 and I_2 are the bias currents and i_1 and i_2 are the signal currents. In contrast to the AGC quad, the Gilbert quad can provide for both amplification and attenuation. Besides, if the bias current I_2 is kept constant and the gain of the Gilbert quad is controlled by I_1, a constant output current results in constant relative signal levels i_1/I_1 and i_2/I_2. For those reasons, the Gilbert quad is chosen as elementary gain-control cell in the LF AGC amplifier.

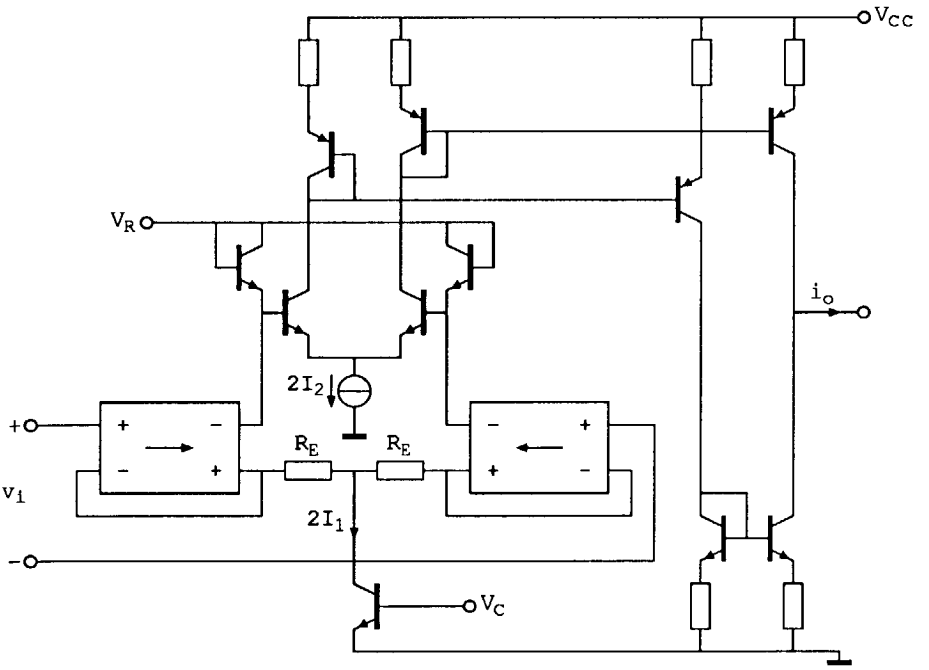

Figure 5.2: Implementation of the AGC amplifier with a Gilbert quad.

Figure 5.2 shows the implementation of the LF AGC amplifier with a Gilbert quad as elementary gain-control cell. The Gilbert quad is driven by

a balanced transadmittance amplifier, the transfer of which can be written as:

$$\frac{i_1}{v_i} = \frac{1}{2R_E} \tag{5.3}$$

The current I_1 is derived from the gain-control voltage V_C that provides for an exponential gain-control characteristic, necessary for a signal level independent AGC loop gain (See Section 2.3). A single ended output current is obtained using three current mirrors. The transfer of the complete AGC amplifier according to Figure 5.2 results in:

$$G_A = \frac{i_o}{v_i} = \frac{I_2}{R_E I_1} \tag{5.4}$$

in which I_2 is a fixed bias current and I_1 is the gain-control current.

The transadmittance amplifier might be implemented with the differential pair according to Figure 5.3. The small-signal transfer of such a differential pair however, depends on the tail current:

$$\frac{i_1}{v_i} = \frac{1}{2R_E + 2r_e} = \frac{1}{2R_E + 2V_T/I_1} \tag{5.5}$$

For small values of I_1, the nonlinear emitter impedance $r_e = 1/g_m$ introduces distortion and a significant gain error in the AGC amplifier transfer.

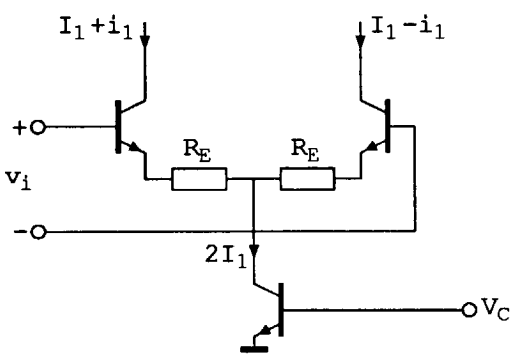

Figure 5.3: Differential pair as transadmittance amplifier.

An improved linearity and accuracy is obtained with a two-stage overall-feedback transadmittance amplifier according to Figure 5.4 [34]. The transfer of this amplifier, given by Equation 5.3, is practically independent of the tail current $2I_1$.

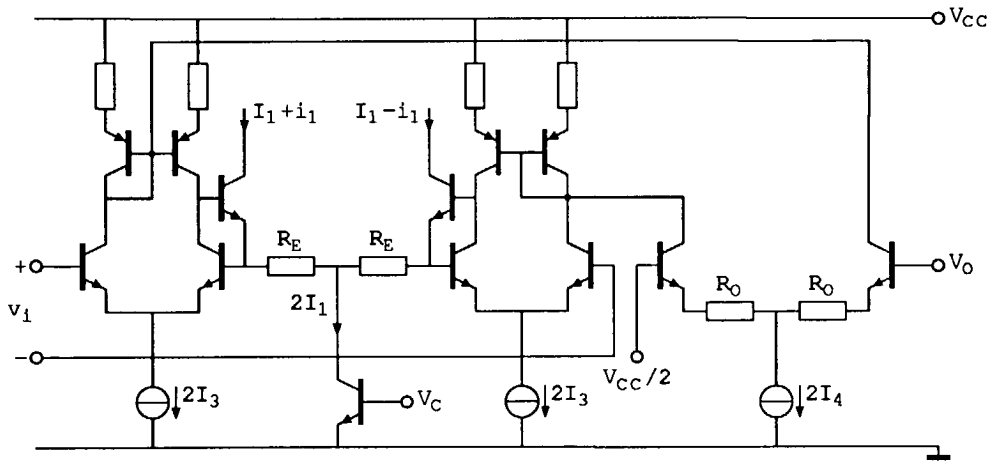

Figure 5.4: Two-stage overall-feedback transadmittance amplifier with offset correction circuitry.

If the gain-control current I_1 is zero, there is still a current flowing trough the outer transistors of the Gilbert quad. This current is determined by the base current I_2/B_F of the inner transistors of the Gilbert quad and the base current I_3/B_F of the input stage of the transadmittance amplifier. The actual gain of the AGC amplifier results in:

$$G_A = \frac{I_2}{(I_1 + I_2/B_F + I_3/B_F)R_E} \tag{5.6}$$

At high gain-control currents, the influence of these base currents can be neglected.

The input voltage V_O is the offset compensation voltage generated by the autozero system. The gain of this offset correction input should not be larger than necessary in order to limit the effect of the droop of the autozero hold capacitor (see also Section 2.2). The maximum equivalent input offset correction voltage is calculated as:

$$\tanh\left(\frac{\Delta v_i}{2V_T}\right) = \frac{I_4}{I_3} \tag{5.7}$$

in which I_3 and I_4 are the tail currents as indicated in Figure 5.4. Since the offset voltage in bipolar transistors is in the order of magnitude of 1mV, a total offset correction voltage about V_T is more than sufficient. If a tail

current $I_4 = 0.5I_3$ is taken, the offset-control gain can be written as:

$$\frac{\Delta v_i}{V_O} \approx \frac{V_T}{I_3 R_O} \tag{5.8}$$

under the condition that $R_O \gg V_T/I_4$.

5.2 AGC noise behaviour

The noise contribution of the current sources can be neglected provided that the voltage drop over the emitter resistors is much larger than V_T. In this case, the noise of the AGC amplifier is determined by the noise of the Gilbert quad, the input differential pairs and the resistors R_E.

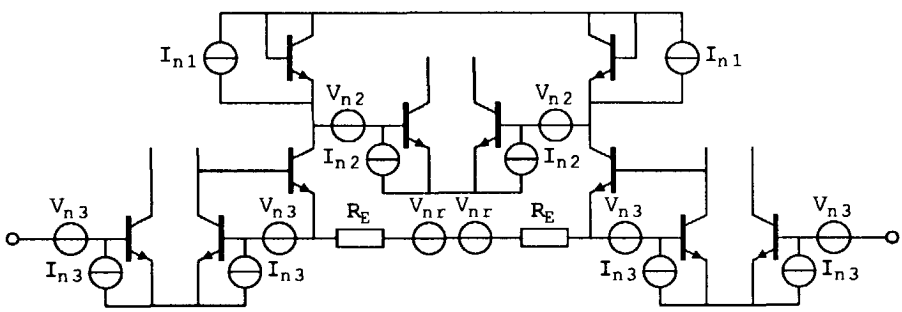

Figure 5.5: Noise model of the AGC amplifier with the relevant noise sources

Figure 5.5 shows the noise model of the AGC amplifier. The spectral densities of the relevant noise sources are equal to:

$$S(I_{n1}) = \frac{4kT}{2r_{e2}}\left(1 + 2\frac{r_{b1}}{r_{e1}}\right) \tag{5.9}$$

$$S(V_{n2}) = 4kT(r_{b2} + r_{e2}/2) \tag{5.10}$$

$$S(I_{n2}) = \frac{4kT}{2B_F r_{e2}} \tag{5.11}$$

$$S(V_{n3}) = 4kT(r_{b3} + r_{e3}/2) \tag{5.12}$$

$$S(I_{n3}) = \frac{4kT}{2B_F r_{e3}} \tag{5.13}$$

$$R(V_{nr}) = 4kTR_E \tag{5.14}$$

In these equations, $r_{e1} = V_T/I_1$, $r_{e2} = V_T/I_2$ and $r_{e3} = V_T/I_3$.

The equivalent input noise voltage V_{ni} of the AGC amplifier is calculated as:

$$S(V_{ni}) = 4S(V_{n3}) + 2S(V_{nr}) + 2R_E^2\left[S(I_{n1}) + S(I_{n2}) + S(I_{n3}) + \frac{S(V_{ni})}{r_{e1}^2}\right] \tag{5.15}$$

If the AGC amplifier is driven by a low-impedance source, the influence of the equivalent input noise current, which is equal to $2I_{n3}$ can be neglected.

Generally, $B_F r_{e2} > R_E$ and $B_F r_{e3} > R_E$, so the influence of the base current shot noise I_{n2} and I_{n3}, which are independent of the control current I_1, can be neglected. Under this assumption, the equivalent input noise voltage is calculated as:

$$S(V_{ni}) = 4kT\left[2R_E + 4r_{b3} + 2r_{e3} + \frac{R_E^2}{r_{e1}^2}(r_{e1} + r_{e2} + 2r_{b1} + 2r_{b2})\right] \tag{5.16}$$

since r_{e1} is inversely proportional with the gain-control current I_1, the equivalent input noise voltage increases with an increasing I_1 and hence a decreasing gain.

All noise sources in Figure 5.5 can also be transformed to an equivalent output noise current. This equivalent output noise current is calculated as:

$$S(I_{no}) = \frac{4kT}{r_{e2}}\left[\frac{r_{e1}^2}{r_{e2}R_E}\left(2 + \frac{4r_{b3}}{R_E} + \frac{2r_{e3}}{R_E}\right) + 1 + \frac{r_{e1}}{r_{e2}} + \frac{2r_{b1}}{r_{e2}} + \frac{2r_{b2}}{r_{e2}}\right] \tag{5.17}$$

In the signal level range, for which the output level is kept constant, the signal to noise ratio is directly related to this equivalent output noise current. At the minimum gain, for which $r_{e1} \ll r_{e2}$ and $r_{e1} \ll R_E$, the output noise current can be approximated by:

$$S(I_{no}) = \frac{4kT}{r_{e2}}\left[1 + \frac{r_{e1}}{r_{e2}} + \frac{2r_{b1}}{r_{e2}} + \frac{2r_{b2}}{r_{e2}}\right] \tag{5.18}$$

This output noise current is determined by the noise of the Gilbert quad itself. At the maximum gain, for which $r_{e1} \gg r_{e2}$ and $r_{e1} \gg R_E$, the output noise current can be approximated by:

$$S(I_{no}) = 4kT(2R_E + 2r_{e3} + 4r_{b3})\,(G_{A\max})^2 \tag{5.19}$$

This output noise current is determined by the noise of the transadmittance amplifier.

5.3 Dimensioning and results of a prototype AGC amplifier

A prototype AGC system containing three complete AGC amplifiers is implemented on a 500MHz bipolar array [35]. The main transistor parameters of the NPN transistors are given in Table 5.1. The autozero circuitry is not implemented on this chip.

current gain:	B_F	180
	β_f	180
base resistance:	r_b	300Ω

Table 5.1: Typical values of the main transistor parameters of the applied 500MHz bipolar process.

The AGC reference current I_R is chosen to be one third of the maximum output current as a compromise between the linearity and the carrier-to-noise ratio. The dc carrier in this case is the dc signal component in the gain-control path resulting from the desired carrier. In the stationary state, this dc signal component is equal to the AGC reference current:

$$i_o = 2i_2 = I_R = \frac{2}{3}I_2 \tag{5.20}$$

With an AGC amplification according to Equation 5.6, the corresponding signal current i_1 can be derived as:

$$i_1 = \frac{I_1 + I_2/B_F + I_3/B_F}{I_2} i_2 = \frac{I_1 + I_2/B_F + I_3/B_F}{3} \tag{5.21}$$

In order to prevent distortion at very low gain-control currents, I_1 is given a minimum value, for which $I_1 \geq 2i_1$. This results in a minimum gain-control current of:

$$I_{1\text{min}} = 2I_2/B_F + 2I_3/B_F \tag{5.22}$$

and a maximum gain equal to:

$$G_{A\text{max}} = \frac{I_2}{3(I_2/B_F + I_3/B_F)R_E} \tag{5.23}$$

In the prototype AGC amplifier, I_3 is chosen equal to I_2, which results in a maximum gain of $B_F/6R_E$.

Obviously, the minimum gain depends on the maximum gain-control current. For high gain-control currents, this minimum gain can be written as:

$$G_{A\min} = \frac{I_2}{I_{1\max} R_E} \tag{5.24}$$

For a certain control range $\mathcal{R}$, it can be calculated that:

$$\mathcal{R} = \frac{G_{A\max}}{G_{A\min}} = \frac{B_F I_{1\max}}{6 I_2} \tag{5.25}$$

which results in a maximum gain-control current:

$$I_{1\max} = \frac{6\mathcal{R} I_2}{B_F} \tag{5.26}$$

For a given maximum input voltage $v_{i\max}$ of the AGC amplifier, the emitter resistor R_E is calculated as:

$$R_E = \frac{3 v_{i\max}}{2 I_{1\max}} \tag{5.27}$$

For the prototype AGC amplifier, a tail current $2I_2 = 40\mu$A is chosen for a theoretical control range of 60dB with a maximum gain-control current $2I_{1\max} = 1.5$mA. The minimum gain-control current $2I_{1\min} = 0.89\mu$A is generated by an additional offset current source. A 2kΩ emitter resistor is chosen for a maximum input voltage $v_{i\max} = 1$V. Obviously, the AGC reference current is 13.3μA. The time constant of the AGC loop, calculated in Section 2.1 was found to be:

$$\tau_A = \frac{C_A V_T}{I_R} \tag{5.28}$$

An AGC time constant of 10ms is obtained with an AGC capacitor $C_A = 5.3\mu$F. This capacitor cannot be implemented on-chip because of its large value.

At the minimum gain resulting from a maximum input signal level, for which $2I_1 = 1.5$mA and hence $r_{e1} = 33\Omega$, the equivalent output noise current according to Equation 5.18 is 5.2pA/$\sqrt{\text{Hz}}$. With a 13.3μA output current, the CNR is 94dB in a 2.5kHz noise bandwidth. At the maximum gain resulting from a minimum input signal level, the equivalent output noise current according to Equation 5.19 is 0.17nA/$\sqrt{\text{Hz}}$. The resulting CNR ($i_o = 13.3\mu$A) is 64dB in a 2.5kHz noise bandwidth for a corresponding synchronous detector input signal level of -60dB.

The measured control range of the prototype amplifier under the conditions described above is about 55dB. With a signal current less than a third of the bias current, the total harmonic distortion is well below 0.5%. The measured output noise current at the maximum gain, for which the external gain-control current is zero, is about $0.2\text{nA}/\sqrt{\text{Hz}}$. At the minimum gain, the output noise current is $7\text{pA}/\sqrt{\text{Hz}}$ and the resulting CNR is 90dB in a 2.5kHz noise bandwidth.

5.4 Design considerations of the LF autozero circuitry

The most critical design aspect of the low-frequency autozero circuitry concerns the droop of the autozero capacitors. Since these autozero capacitors are intended to be implemented on-chip, their limited values require an extremely low droop in order to keep the droop of the equivalent input offset compensation voltage of the LF AGC amplifier far below its minimum input voltage using an autozero frequency not exceeding 10Hz.

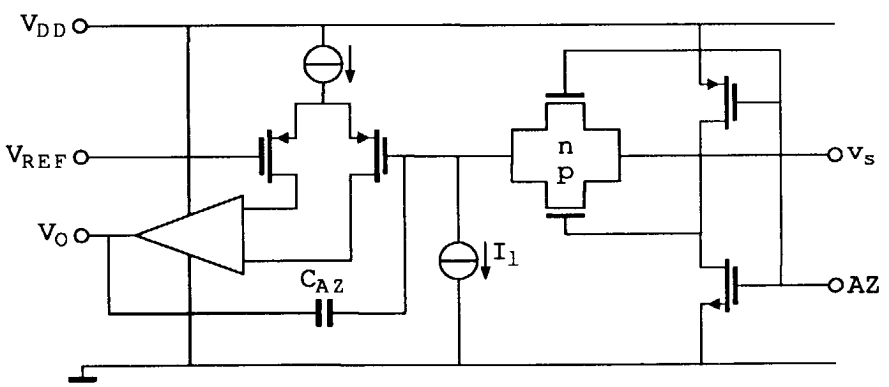

Figure 5.6: Implementation of the offset adjustment circuitry.

Figure 5.6 shows a (BI)MOS implementation of the offset adjustment circuitry, in which the cause of droop is indicated by the leakage current I_l. A minimum leakage current of the capacitor itself is obtained by the application of an oxide capacitor, for which the poly silicon plate is connected to the integrator amplifier input (see Figure 4.18 on page 107). The MOS input of the integrator amplifier also provides for a minimum leakage current. The leakage current will finally be determined by that of the diffusion areas of the transmission gates. Equal and minimum dimensions of both NMOS and PMOS pass transistors not only minimise charge over effects, but also

provide for minimum leakage currents as well. Since the leakage currents of the NMOS and the PMOS transistor have opposite signs, these leakage currents partly compensate each other.

In the stationary state, the sampled output current of the AGC amplifiers is zero (apart from the leakage current) and the sampled output voltage v_s of the AGC amplifiers nearly equals the autozero reference voltage V_{REF}. As already mentioned in Section 2.2, the remaining offset voltage $V_{\mathrm{REF}} - v_s$, caused by the offset in the input stage and the finite gain of the integrator amplifier results in a negligible input offset voltage of the LF AGC amplifiers. The autozero integrator provides for a dominant pole in the autozero control loop, so the stability over the entire gain-control range of the AGC amplifier will not cause significant problems.

The maximum input voltage of the LF AGC amplifier (see Section 5.3) is 1V. With the required 90dB dynamic range, the maximum equivalent input noise voltage has to be $30\mu\mathrm{V_{rms}}$. According to Section 5.1, an offset adjustment voltage $V_O = 1\mathrm{V}$ corresponds to an equivalent input offset compensation voltage of about 10mV. If the droop of this equivalent input offset compensation voltage should not exceed the noise floor, the droop of V_O should not exceed 3mV. This droop voltage ΔV_O can be expressed as:

$$\Delta V_O = \frac{I_l T_{AZ}}{C_{AZ}} \tag{5.29}$$

in which I_l is the leakage current, T_{AZ} is the autozero cycle time and C_{AZ} is the autozero hold capacitor. For the leakage current, a value in the order of magnitude of 1pA may me assumed. This results in $\Delta V_O = 3\mathrm{mV}$ obtained with an autozero capacitor $C_{AZ} = 33\mathrm{pF}$ and an autozero cycle time $T_{AZ} = 0.1\mathrm{s}$

In a breadboard version of a synchronous detector operating at an IF frequency of 8MHz, the LF switches are implemented with IIEF4016 transmission gates. The autozero integrators are built up with transistors in the HEF4007 and a 100pF discrete capacitor. With an autozero frequency about 10Hz, no degrading effects of the droop can be observed, while the autozero control loop is stable over the entire gain-control range of the LF AGC amplifiers. In an integrated version conform the design considerations given in this section, an improved performance with an autozero capacitor of about 10pF and an autozero frequency not exceeding 10Hz must be feasible.

Chapter 6

Conclusions

The selectivity and dynamic range of the basic implementation of a synchronous detector (conform Figure 1.3 on page 4) is limited by the signal-handling dynamic range of the carrier regenerating PLL, rather than that of the synchronous conversion itself. With the application of post-detection AGC combined with autozero techniques, the signal-handling dynamic range can be widely extended, while the output level of the detected baseband signal can be kept constant over the entire gain-control range of the AGC amplifiers. Provided that this gain-control range is sufficiently large, the selectivity and dynamic range of the extended dynamic range synchronous detector is determined by that of the synchronous conversion itself and the subsequent on-chip low-pass filter.

Fully balanced MOSFET-C filters are the preferred filter types for the audio frequency range, since they provide for a high linearity and a minimum 1/f noise contribution. In addition, both the thermal noise level and the 1/f noise level of the (BIMOS) amplifiers can essentially be kept below the unavoidable thermal noise floor of the MOS resistors. The filter output noise is inversely proportional with the total filter capacitance and hence the occupied chip area. The direct sampling tuning technique, proposed in Section 4.4 provides for a completely integrated automatic tuning system with a minimum ripple on the resistor control voltage and a minimum of overhead circuitry.

In a final conclusion, we can state that the performance concerning the selectivity and dynamic range of the extended dynamic range synchronous detector with on-chip low-pass filtering is sufficient for application as a selective detector for an AM upconversion receiver with a limited (first) IF selectivity. The major drawback of synchronous detection is the relatively large amount of overhead circuitry for carrier regeneration.

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Summary

This thesis is focussed upon the design of a synchronous detector for an integrated AM upconversion receiver with a tuning range from 150kHz to 30MHz. The design of the upconversion front end is described in the thesis of my colleague dr. ir. J.W.Th. Eikenbroek [2].

In a traditional downconversion receiver, the preselection filter is a bandpass filter, which is simultaneously tuned with the local oscillator. The large tuning range requires many band switches and adjustments. In an upconversion receiver, preselection is realised with a fixed low-pass filter, while tuning is performed with the local oscillator only. Although this low-pass filter and the IF filter cannot be implemented on-chip, the upconversion principle leads to a much more integration friendly design.

The high IF frequency emerging from the upconversion principle requires an accurate local oscillator frequency and IF filter central frequency together with a narrow IF filter relative bandwidth. Consequently, the local oscillator has to be synthesister controlled with an extremely accurate quartz reference crystal, while the IF filter has to be a quartz (SAW) device. The required (adjacent) channel selectivity cannot be established at the high (first) IF frequency (70MHz or 40MHz), so additional selectivity has to be obtained at a second and lower IF frequency. Synchronous detection is presented as an integration friendly method for the implementation of the additional selectivity by on-chip low-pass filtering, without introducing additional image channels.

According to [2], a 120dB front-end dynamic range and a 40dB stopband selectivity of the first IF filter is feasible, while the overall stopband selectivity of the reciever has to be 90dB. Consequently, the synchronous detector has to provide for the additional 50dB stopband selectivity. With an IF AGC amplifier, the signal dynamic range can be reduced down to 80dB at the input of the synchronous detector. These selectivity and dynamic range specifications result in a second- and third-order intermodulation-free dynamic range (IMFDR) specification of 105dB and 110dB respectively for the front-end circuits and 70dB and 77dB respectively for the synchronous detector circuits.

The required IMFDR of the front end and the synchronous detector can only be established if all mixers including the phase detector of the car-

rier regenerating PLL are implemented as long-tailed pair switching mixers. The implementation of the synchronous mixers and the calculation of their transfer, switching behaviour, noise behaviour and distortion is dealt with in Section 3.1.

The transfer of a long-tailed pair mixer and consequently the phase detector gain depends on the desired IF carrier level, the PLL is locked onto. In order to handle a large dynamic range of input signals, a post detection AGC system is implemented in the synchronous detector that provides for both a constant PLL loop gain and a constant audio output level. The low-frequency AGC amplifiers are built up around a single Gilbert quad. A prototype post detection AGC system (Chapter 5) has been implemented in a 500MHz bipolar analog array. The resulting 55dB gain control range and 90dB dynamic range of this prototype is sufficient in order to fulfill the specifications of the complete synchronous detector.

A second and even worse problem resulting from the high dynamic range of input signals is caused by offset in the post detection circuitry. Autozero techniques are applied in the synchronous detector in order to compensate offset voltages and their temperature drift automatically with a minimum amount of spurious oscillator power. This in contrast to offset compensation based on chopping techniques, which introduce a significant amount of spurious oscillator power, having a detrimental effect on the synchronous detector selectivity.

The specifications of the low frequency autozero circuits do not lead to specific implementation problems if these circuits, combined with the remaining circuitry, are integrated in a BIMOS technology. The specifications concerning the IMFDR and the off-state attenuation of the IF autozero switch can be fulfilled with a bipolar long-tailed pair switch. The required off-state attenuation is hard to realise with an IF switch built up with CMOS transmission gates.

The initial frequency of the VCO must be extremely accurate in order to prevent false lock on adjacent carriers. The requirement of an additional quartz reference crystal for the VCO can be circumvented if this initial frequency is derived from the local oscillator reference frequency. The required carrier-to-noise ratio of the quadrature VCO can be obtained with an on-chip oscillator.

In Chapter 3, the implementation on a 3GHz bipolar array of the synchronous detector hf circuits, containing the synchronous mixers, the IF autozero switch and the quadrature oscillator is described. This quadrature oscillator is realised with mutually coupled regenerative oscillators. Both

the calculated and the measured circuit performance of this prototype on a 3GHz bipolar array is sufficient in order to guarantee the selectivity and dynamic range of the synchronous detector.

The design of the continuous time audio low-pass filter, that has to provide for the required channel selectivity, is described in Chapter 4. For the audio frequency range, the largest dynamic range is obtained if the active filter is built up with Miller integrators, in which gate controlled MOS resistors are used as resistive elements. With these integrator types, the detrimental effect of the 1/f noise can be circumvented and the noise contribution of the amplifiers can be kept lower than the unavoidable thermal noise of the integration resistors. A novel automatic tuning technique is proposed in order to control the filter cut-off frequency with a minimum amount of overhead circuitry and a minimum ripple on the resistor control voltage. A prototype audio filter has been integrated in the PHILIPS L422 BIMOS process, which results in a 90dB dynamic range with a total chip area of about 3.5 square millimeters.

The results of the calculations in this thesis combined with the results of the prototypes confirm the technical feasibility of a synchronous detector, that guarantees at least 50dB additional channel selectivity. However, the relatively large amount of overhead circuitry for the regeneration of the carrier makes the economic feasibility for the consumer market doubtful.

Samenvatting

Het onderwerp van dit proefschrift omvat het ontwerp van een synchrone detector voor een geïntegreerde AM upconversie ontvanger met een afstembereik van 150kHz tot 30MHz. Het ontwerp van het upconversie front-end wordt beschreven in het proefschrift van mijn collega dr. ir. J.W.Th. Eikenbroek [2].

In een traditionele downconversie ontvanger is het preselectiefilter een banddoorlaat filter dat gelijktijdig met de locale oscillator wordt afgestemd. Door het grote afstembereik zijn veel bandschakelaars en afregelingen noodzakelijk. In een upconversie ontvanger daarentegen is het preselectiefilter een vast laagdoorlaat filter en wordt de ontvanger afgestemd met uitsluitend de locale oscillator. Hoewel dit laagdoorlatende preselectiefilter en het middenfrequentfilter niet op een chip te implementeren zijn, is het upconversie principe veel beter geschikt voor integratie.

De hoge middenfrequentie die samenhangt met het upconversie principe vereist een nauwkeurige locale oscillator frequentie en centrale frequentie van het middenfrequentfilter samen met een een smalle relatieve bandbreedte van dit middenfrequentfilter. Dit heeft als gevolg dat de locale oscillator synthesiser gestuurd moet zijn met een uiterst nauwkeurig referentie kristal, terwijl het middenfrequentfilter moet worden geïmplementeerd als een kwarts (oppervlaktegolf) filter. Aangezien het niet mogelijk is om de vereiste (nabuur) selectiviteit bij de eerste middenfrequentie (70MHz of 40MHz) te realiseren, dient de aanvullende selectiviteit te worden gerealiseerd in een tweede en lagere middenfrequentie. Synchrone detectie wordt voorgesteld als een integratie vriendelijke methode voor het verkrijgen van aanvullende selectiviteit met behulp van integreerbare laagdoorlaatfilters, zonder daarbij extra spiegelkanalen te introduceren.

Voor het front-end is volgens [2] een dynamisch bereik van 120dB en een stopband selectiviteit van 40dB haalbaar, terwijl een totale stopband selectiviteit van 90dB vereist is. De stopband selectiviteit van de synchrone detector dient zodoende 50dB te zijn. De signaaldynamiek kan met een middenfrequent AGC versterker worden teruggebracht tot 80dB. Deze specificaties betreffende de selectiviteit en het dynamisch bereik resulteren in een specificatie betreffende de tweede- en derde orde intermodulatievrij dynamisch bereik (IMFDR) van respectievelijk 105dB en 110dB voor de cir-

cuits in het front-end en respectievelijk 70dB en 77dB voor de circuits in de synchrone detector.

Het vereiste IMFDR van het front-end en de synchrone detector kan alleen worden bereikt indien alle mixers, inclusief de fasedetector van de draaggolf regeneratie PLL, worden geïmplementeerd als schakelende dubbelgebalanceerde long-tailed pair mixers. De implementatie van de synchrone mixers en de daarbij behorende berekeningen aangaande de overdracht, het schakelgedrag, het ruisgedrag en de distorsie worden behandeld in paragraaf 3.1.

De overdracht van een long-tailed pair mixer en daarmee de versterkingsfactor van de fasedetector is afhankelijk van het gewenste draaggolfniveau waarop de PLL staat vergrendeld. Om nu een groot dynamisch bereik van het ingangssignaal aan te kunnen wordt een post-detectie AGC systeem in de synchrone detector geïmplementeerd, die zorgt voor een constante lusversterking van de PLL en een constant uitgangsniveau van het audiosignaal. De laagfrequente AGC versterkers zijn opgebouwd rond een enkel Gilbert quad. Een prototype van dit post-detectie AGC systeem is geïmplementeerd op een 500MHz bipolaire analoge array. Het behaalde regelbereik van 55dB en het behaalde dynamisch bereik van 90dB is voldoende om aan de specificaties van de synchrone detector in zijn geheel te kunnen voldoen.

Een tweede nog veel groter probleem, inherent aan het hoge dynamisch bereik van ingangssignalen, wordt veroorzaakt door offset in de post-detectie circuits. Om offset spanningen en de temperatuurdrift daarvan automatisch te compenseren met een minimale spectrale vervuiling van het oscillatorsignaal worden autozero technieken in de synchrone detector toegepast. Dit in tegenstelling tot het compenseren van offsetspanningen met choptechnieken, die het oscillatorsignaal spectraal ernstig vervuilen en daarmee de selectiviteit verslechteren.

De specificaties van de laagfrequente autozero circuits leiden niet tot specifieke implementatieproblemen, indien deze circuits gecombineerd met de overige circuits worden geïmplementeerd in een BIMOS technologie. De specificaties aangaande het IMFDR en de demping in de uittoestand van de middenfrequentschakelaar kunnen worden bereikt met een bipolaire long-tailed pair schakelaar. Indien deze schakelaar wordt gerealiseerd met CMOS transmissie poorten kan aan de dempingseis in de uittoestand waarschijnlijk niet worden voldaan.

De rustfrequentie van de VCO moet zeer naukeuring vastliggen om onder andere foutieve vergrendelingen op nabuurdraaggolven te voorkomen. Een extra kwarts kristal voor deze VCO kan worden vermeden indien deze

rustfrequentie wordt afgeleid van de referentie frequentie van de locale oscillator. Aan de vereiste signaal ruisverhouding kan worden voldaan met een integreerbare oscillator.

In hoofdstuk 3 wordt de implementatie van het hoogfrequent gedeelte van de synchrone detector op een 3GHz bipolaire array beschreven. Dit prototype omvat de synchrone mixers, de middenfrequent autozero schakelaars en de quadratuur oscillator, waarbij de laatste is opgebouwd uit wederzijds gekoppelde regeneratieve oscillatoren. Zowel de berekende als de gemeten kwaliteitseigenschappen zijn voldoende teneinde de selectiviteit en het dynamisch bereik van de synchrone detector in zijn geheel te garanderen.

Het ontwerp van een tijdcontinu audio laagdoorlaatfilter, dat de vereiste kanaalselectiviteit moet leveren, wordt beschreven in Hoofdstuk 4. Een maximaal dynamisch bereik voor audio frequenties wordt bereikt indien het actieve filter wordt opgebouwd rond Miller integratoren, waarin gate gestuurde MOS weerstanden worden toegepast als resistieve elementen. Met dit type integratoren kunnen de nadelige effecten van 1/f ruis worden vermeden en kan het ruisniveau van de versterkers lager worden gehouden dan de onvermijdbare thermische ruisvloer van de weerstanden. Voor het vastleggen van de afsnijfrequentie wordt een nieuw type automatisch afstemsysteem voorgesteld die een minimum aan extra circuit vereist en een minimale rimpel op de stuurspanning van de MOS weerstanden introduceert. Een prototype audiofilter is geïntegreerd in het PHILIPS L422 BIMOS process, waarbij een dynamisch bereik van ruim 90dB is bereikt met een totale chip oppervlakte van ongeveer 3.5 vierkante millimeter.

De resultaten van berekeningen en metingen in dit hoofdstuk bevestigen de technische haalbaarheid van synchrone detectie voor het verkrijgen van aanvullende selectiviteit van tenminste 50dB. Echter, vanwege de extra schakelingen die nodig zijn voor het regenereren van de draaggolf lijkt dit type ontvanger economisch minder aantrekkelijk voor de consumentenmarkt.

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About the author

Jaap van der Plas was born in Leiden, the Netherlands on April 3rd, 1963. Starting his studies at Delft University of Technology, Delft, the Netherlands in 1981, he received (cum laude) his masters degree on July 3rd, 1986. The subject of his masters thesis enclosed the design of a synchronous detector for an integrated car radio receiver.

In September 1986, he joined the Electronics Research Laboratory at this university and was engaged in a Ph. D. research project on the subject of integrated AM shortwave receivers, financially supported by the Dutch Technology Foundation (Stichting voor de Technische Wetenschappen, STW). This thesis about synchronous detection, a patent pending and several publications are the results of his main research subject.