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Intermittent Undefined State Fault in RRAMs

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***Abstract*—Industry is prototyping and commercializing Resistive Random Access Memories (RRAMs). Unfortunately, RRAM devices introduce new defects and faults. Hence, high-quality test solutions are urgently needed. Based on silicon measurements, this paper identifies a new RRAM unique fault, the Intermittent Undefined State Fault (IUSF); this fault causes the RRAM device to intermittently change its switching mechanism from bipolar to complementary switching, resulting in undefined state faults. First, we characterize the IUSF by analyzing RRAM devices, and demonstrate that a single RRAM device can suffer from the IUSF up to $1.068\,\%$ of its switching cycles; we relate the IUSF to two defects: capping layer doping, and over-forming. This clearly shows the importance of detecting this fault. Second, we develop a device-aware defect model that accurately describes the physical behavior of these defects and gives essential insights into the IUSF's behavior and its detection. Third, we perform fault modeling by applying the device-aware defect model, and the results are used to develop high-quality test solutions for the IUSF. The contributions in this work improve the overall RRAM test quality, which enables mass commercialization of RRAMs.**

***Index Terms*—RRAM test, defect modeling, device-aware test**

I. Introduction

Resistive Random Access Memories (RRAMs) are a promising alternative to replace traditional memory technologies such as Flash and Dynamic RAM (DRAM) [1, 2]. RRAM devices are non-volatile and consume no static power, which makes them suitable for embedded applications. Furthermore, RRAM devices can be read and written in few nanoseconds, making them significantly faster than Flash [3]. They are relatively simple to manufacture and enable dense crossbar structures and can store multiple bits per cell [1–4] and even enable new computing paradigms [5, 6]. Although they have many benefits, some obstacles still need to be overcome. One of these is that RRAM devices introduce new defects and faults that have not been seen in traditional memories, e.g., forming defects [7]. Hence, appropriate fault modeling and high quality and efficient test solutions are needed.

Several RRAM defects and faults have been described in the literature [8–13]. The majority of the studied defects are modeled as *linear* resistors in (and at) the *terminals of the RRAM device*, i.e., opens, short and bridges [8–12]. This defect model led to the identification of several RRAM fault models, e.g., undefined write or read faults [9, 10], and deep faults [10]. However, a linear resistor does not accurately describe defects *in the RRAM device itself*, e.g., forming defects [13]. The RRAM device is non-linear by nature, and the linear resistor approach models the defects in the surrounding interconnections rather than the defects in the device itself; using this inappropriate defect model leads to test escapes and yield loss. A solution to this is device-aware defect modeling, in which the defect's impact on the RRAM device's electrical parameters is *incorporated* in the RRAM device model [13]. The resulting defect model leads to realistic fault models that can be used to develop high-quality test solutions. However, since RRAM is a new technology, unique defects and failure mechanisms will evolve, e.g., defects caused by miniaturization of the device, or complex faulty behaviors such as SET switching failure [14]. Hence, it is of prime importance to identify such defects (in an industrial environment), characterize, and accurately model them for optimal and high-quality test development.

This paper identifies and characterizes, based on measurement data, a new RRAM fault, the Intermittent Undefined State Fault (IUSF). This fault causes the RRAM device to intermittently change its switching mechanism from bipolar to complementary, which affects write operations and causes undefined state faults. We apply the device-aware approach to model the defects that cause IUSFs. Subsequently, we use this model to develop appropriate fault models and test solutions. Summarizing, in this paper we:

- Identify the IUSF in RRAMs based on silicon data.
- Determine RRAM defects that could lead to IUSFs.
- Demonstrate that the conventional defect modeling approach fails to appropriately describe these defects.
- Perform device-aware defect modeling to accurately model these defects.
- Perform device-aware fault modeling to develop realistic fault models and thereafter optimal test solutions.

The remainder of the paper is structured as follows. Section II briefly presents RRAM background information. Section III presents experimental evidence, characterization, and underlying defects of the IUSF. Section IV demonstrates the failure of the linear resistor defect model, and presents the defect model that accurately describes the behavior of a defective RRAM device. This model is used in Section V to perform fault modeling and analysis. Section VI describes a test algorithm to detect the IUSF. Section VII discusses and concludes the paper.

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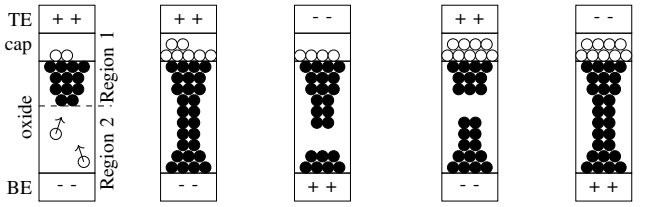
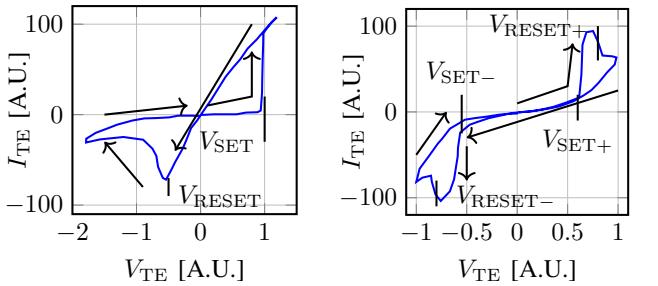


(a) Forming (b) BS SET (c) BS RESET (d) CS RESET (e) CS SET

Fig. 1: Evolution of the conductive filament



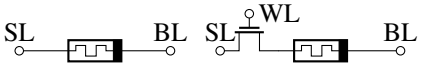
(a) Bipolar switching (BS) (b) Complementary switching (CS)

Fig. 2: Resistance switching mechanisms in RRAM.

II. Background

Fig. 1a illustrates a RRAM device; it consists of two electrodes, the top electrode (TE) and bottom electrode (BE), in between which a metallic oxide is sandwiched (commonly, HfO_x, TaO_x, or TiO_x) with an additional capping layer [1, 2, 15]. After fabrication, a voltage V_{forming} is applied to the oxide to break some of the metal and oxygen ions bonds [1, 15]. Fig. 1a shows how the (negatively charged) oxygen ions (white circles) move towards the positive electrode and enter into the capping layer (cap) under the influence of the electric field and bond there [15, 16]. This leaves behind a chain of conducting vacancies (black circles) known as *Conductive Filament (CF)*, as shown in Fig. 1b. When the voltage is removed, the CF remains, making the RRAM device non-volatile. The shape (e.g., radius) of the CF determines the resistance of the device [16]; it can be changed by applying voltages to the oxide. Note that the ability to bind oxygen ions in the capping layer determines the resistance switching mechanism of the RRAM device [17, 18]; if (almost) all of oxygen ions can be bound, then the device will be *Bipolar Switching (BS)*. Conversely, if many oxygen ions remain unbound, then the device will be *Complementary Switching (CS)*.

The BS mechanism relies on the formation and dissolution of the CF by movement of *oxygen ions* [1, 19]. Its electrical behavior is illustrated in Fig. 2a. When a negative voltage V_{TE} less than a threshold V_{RESET} is applied to the TE, then some of the oxygen ions move back into the oxide and re-oxidize the CF leaving a gap in the CF, as shown in Fig. 1c. This movement increases the resistance of the device and is called a RESET operation. When a positive voltage higher than a threshold V_{SET} is applied, the bonds between the metal and oxygen ions break again, and the CF regrows, as shown in Fig. 1b. The oxygen vacancy-rich capping layer collects the free oxygen ions [15]. This process is called a SET operation and results in a lower device resistance. The exact value of the resistance in SET (R_{SET}) and in RESET (R_{RESET}) varies per write cycle due to the random nature of the filament formation and dissolution; it is known as cycle-to-cycle variation [1, 15].



(a) 1R (b) 1T1R

Fig. 3: Two RRAM cell structures.

The CS mechanism relies on the formation and dissolution of the CF by movement of *oxygen vacancies* [17, 18]. Its electrical behavior is illustrated in Fig. 2a. After initial forming, a normal BS RESET is performed, resulting in the CF shown in Fig. 1c. Now, by applying a voltage exceeding the switching threshold $V_{\mathrm{SET+}}$, a SET operation will take place (similar to BS) that results in the breaking of the bonds between the oxygen and metal ions and the forming of the CF as shown in Fig. 1b. However, when the voltage is further increased and exceeds the threshold $V_{\mathrm{RESET+}}$, the negative oxygen ions cannot all be bound in the capping layer. Instead, they will remain in the oxide and the positive oxygen vacancies in the CF will start to move along the electric field towards the negative electrode. This disrupts the just created CF and brings the device in a RESET state, as shown in Fig. 1d. Note that both SET and RESET occur at the same voltage direction, they complement each other. When a negative voltage is applied less than the threshold $V_{\mathrm{SET-}}$, first the oxygen vacancies will move back into the oxide and form a CF, see Fig. 1e. With further decreasing of the voltage below threshold $V_{\mathrm{RESET-}}$, the CF will be broken again by the oxygen ions that move back into the oxide from the capping layer, leading to the state shown in Fig. 1c.

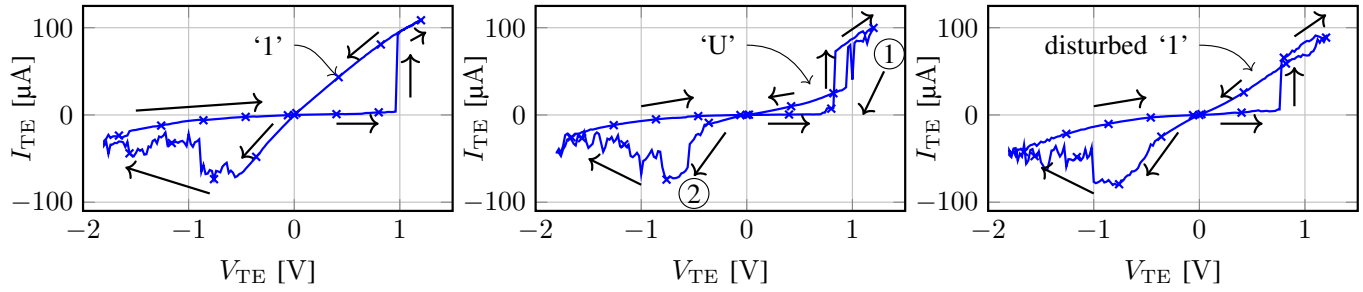
Fig. 3 shows two commonly used cell designs that consist of only one RRAM device (1R, Fig. 3a), or of one transistor and one RRAM device (1T1R, Fig. 3b); each of these cell designs can be used to build a crossbar memory cell array. In the figures, BL, WL, and SL refer to bit line, word line, and select line, respectively. The RRAM devices can be written by setting these lines to appropriate voltages. A cell is read out by applying a read voltage and sensing the resulting current through the device using a sense amplifier (SA).

III. Characterization of the Intermittent Undefined State Fault

First the results of the characterization of RRAM devices under investigation (based on which the IUSF was identified) are presented. Thereafter, a brief overview on the underlying physics and potential defects behind the IUSF is given.

A. Characterization

We measured the electrical characteristics of $7 \times 7 = 49$ 1T1R *BS* RRAM devices on a single wafer during 936 RESET-SET cycles. The RRAM devices are manufactured at ST Microelectronics and have the following structure (BE, oxide, cap, TE) = (TiN, HfO_2(10 nm), Ti(10 nm), TiN). An



(a) Defect-free device (b) Faulty device (c) Weak device

Fig. 4: Comparing defect-free, faulty, and weak devices.

TABLE I: Occurrence probability of CS (P_{CS}) in % and maximal duration suffering from CS ($D_{\max}$) in absolute numbers.

		WL 0	WL 1	WL 2	WL 3	WL 4	WL 5	WL 6
BL 0	P_{CS}	5.983	0.427	0	0	0.427	0	0
	$D_{\max}$	3	2	0	0	1	0	0
BL 1	P_{CS}	0	1.282	0	1.175	0.107	1.709	0.641
	$D_{\max}$	0	2	0	1	1	2	2
BL 2	P_{CS}	0	0	0	0.107	0.107	0	1.282
	$D_{\max}$	0	0	0	1	1	0	1
BL 3	P_{CS}	0	0.427	0	0	0	0.107	0
	$D_{\max}$	0	1	0	0	0	1	0
BL 4	P_{CS}	0	0	0.427	0.214	2.564	0.214	0.855
	$D_{\max}$	0	0	1	1	3	1	3
BL 5	P_{CS}	0	0	2.03	0	0	0.107	0
	$D_{\max}$	0	0	2	0	0	1	0
BL 6	P_{CS}	0.427	0.107	0.427	0.321	1.389	0	0
	$D_{\max}$	1	1	1	1	3	0	0

ST Microelectronics 130 nm technology NMOS high-voltage thick oxide transistor is placed in series to control the current through the device. The switching in a nominal defect-free device is bipolar, where logic '1' is represented by the SET state with R_{SET}<25 kΩ, and logic '0' by the RESET state with 100 kΩ<R_{RESET}<1 MΩ. The range [25 kΩ, 100 kΩ] is called an *undefined state* ('U'). An illustrative measured I-V graph of a defect-free device is shown in Fig. 4a. Typical nominal values for V_{SET} and V_{RESET} are 0.82 V and −0.88 V.

While analyzing the measurement data, we noticed that some of the devices showed a strange switching characteristic! After a number of cycles, the switching resembles CS when performing SET, even though the devices are BS. The observed undesired CS in all faulty devices can be classified into two groups: *faulty* and *weak* devices. Fig. 4b represents the I-V graph of the faulty devices. A SET event occurs when the voltage increases from 0 V. However, as the voltage increases even further, the current through the device suddenly decreases at ①, leading to an *undesired* RESET putting the device in an *undefined* state of R_{SET}=33 kΩ. The subsequent RESET operation at ② also differs from a nominal operation, as the current first increases before decreasing, which again resembles CS. Hence, in this group of devices, a SET operation ends in undefined state. Contrarily, Fig. 4c represents the group of weak devices that shows a similar switching behavior, but instead the operation ends in a *disturbed '1' state*.

Table I lists the occurrence probability (P_{CS}.) of undesired CS in the measured devices (using the WL and BL to indicate them); this is the percentage of cycles in which CS occurs given a total of 936 cycles, and includes both groups of faulty and weak devices. Additionally, the table lists the maximal duration ($D_{\max}$) of the undesired behavior, expressed in the maximal number of *consecutive* cycles in which the device shows this behavior. For example, if the undesired CS occurs first in cycles 54, 55 and 56, and later in cycles 141 and 142, then P_{CS}=5/936=0.534 % and $D_{\max}$=3 cycles. From the table it follows that undesired CS occurs in 25 devices, in up to 5.983 % of the cycles, and with a maximal duration of 3 cycles. Hence, the faulty behavior is *intermittent*, and it is a serious concern for BS RRAM devices. As the first group of faulty devices ends in *undefined state* after a SET operation, we will refer to this fault as *Intermittent Undefined State Fault (IUSF)*.

TABLE II: Occurrence probability (P_{IUSF}) of IUSF in %

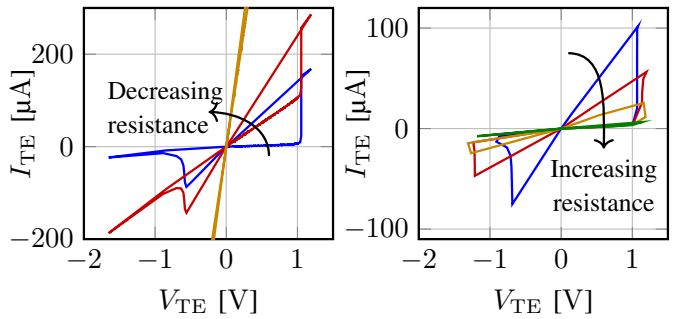
	WL 0	WL 1	WL 2	WL 3	WL 4	WL 5	WL 6
BL 0	0.962	0.427	0	0	0.107	0	0
BL 1	0	0.107	0	0.107	0	0.427	0
BL 2	0	0	0	0	0	0	0.107
BL 3	0	0.107	0	0	0	0	0
BL 4	0	0	0.107	0	1.068	0	0
BL 5	0	0	0.321	0	0	0	0
BL 6	0	0	0.321	0	0.748	0	0

Table II lists the occurrence probability (P_{IUSF}) of the IUSF in the 49 investigated devices over all 936 RESET-SET cycles. It can be seen that depending on the defect strength, the failure rate varies from 0.107 % up to 1.068 % of the cycles, all resulting in an IUSF. Also, the probability of weak CS can be easily derived using P_{weak}=P_{CS} − P_{IUSF}, and can thus be a high as 5.021 %. Note that the weak devices do not result in logic faulty behavior at time=0, but can result in reliability concerns as the weak devices may become logic faults in field, e.g., due to aging, the weak fault may become an IUSF.

B. Physical Explanation and Possible Defects

In Section II, we already distinguished between BS and CS in RRAM devices; BS devices rely on the movement of oxygen *ions* to grow and dissolve the CF, while CS devices rely on the movement of the oxygen *vacancies* due to the shortage of ions in the capping layer to bind the free oxygen ions [17, 18]. Hence, the physics behind the IUSF must involve a reduced oxygen binding capability of the device with respect to the nominal BS case. Two manufacturing defects may lead to this, individually or combined: 1) low-doping of the capping layer, and 2) over-forming; both are explained next.

*1) **Low doping of capping layer**:* The capping layer is not doped with enough positive ions that can bind the negative



(a) Parallel resistor (b) Series resistor

Fig. 5: Linear resistor defect models.

oxygen ions originating from the CF growth. This low binding capacity prevents the widening of the CF and thus favors CS. Since the formation and dissolution of a CF is a random process, the exact amount of oxygen ions varies per write cycle, and hence CS will not occur in every cycle [15].

*2) **Over-forming**:* Over-forming causes the filament to grow wider than in the nominal case. Therefore, more oxygen ions need to bind in the capping layer [15], leading more quickly to a shortage of binding capacity, thus resulting in CS. The random nature of CF growth and dissolution causes this behavior not to occur in every cycle.

IV. Defect Modeling for IUSF

Traditionally, defects in RRAMs are modeled using linear resistors injected in the netlist *at or in the terminals* of the defective device, e.g., a bridge between the device terminals. However, these models are unable to actually describe the faulty behavior *in* the defective device [13]. Next, we first show that linear resistors fail to sensitize the IUSF. Then, we use device-aware defect modeling to model the two defects discussed in the previous section with a single defect model able to sensitize IUSFs.

A. Linear Resistor Defect Models

When modeling defects in a RRAM device with linear resistors, there are only two possible options; the resistor can either be in parallel or in series with the device. Fig. 5a and Fig. 5b show how these defect models affect the behavior of the RRAM device for varying defect strength (i.e., the resistance of the resistor). Clearly none of these two defect models can describe the IUSF properly; a parallel resistor shows that the defective device behaves as a low ohmic resistor for low defect values, while a series resistor shows that the device behaves as a high ohmic resistor for high defect sizes.

B. Device-Aware Defect Model

The device-aware approach appropriately models a defect by incorporating the impact of the affected device technology parameters (e.g., filament dimensions, oxide thickness) on the electrical behavior of the defective device [13]; it consists of three steps: 1) physical defect modeling, 2) electrical defect modeling, and 3) fitting and model optimization.

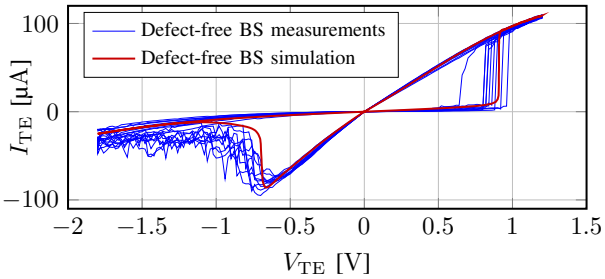
TABLE III: Model parameters for JART VCM v2 [20]

Symbol	Value	Symbol	Value
l_1	$8.75\,\mathrm{nm}$	a	$0.6\,\mathrm{nm}$
l_{cell}	$10\,\mathrm{nm}$	$R_{\mathrm{series},0}$	$2\,\mathrm{k\Omega}$
l_2	$l_{\mathrm{cell}} - l_1$	N_{max}	$3 \cdot 10^{27}\,\mathrm{m}^{-3}$
N_{init1}	$2 \cdot 10^{27}\,\mathrm{m}^{-3}$	μ_{n0}	$1.8 \cdot 10^{-5}\,\mathrm{m}^2/(\mathrm{Vs})$
N_{init2}	$3.5 \cdot 10^{25}\,\mathrm{m}^{-3}$	ν_0	$4 \cdot 10^{12}\,\mathrm{Hz}$
$e\phi_{\mathrm{Bn0,1}}$	$0.35\,\mathrm{eV}$	ΔW_{A}	$0.9\,\mathrm{eV}$
$e\phi_{\mathrm{Bn0,1}}$	$0.1\,\mathrm{eV}$	ϵ	$17 \cdot \epsilon_0$
r_{fil}	$18\,\mathrm{nm}$	$\epsilon_{\phi_{\mathrm{B}}}$	$5.5 \cdot \epsilon_0$
ΔE_{ac}	$0.04\,\mathrm{eV}$	$\alpha_{\mathrm{T,series}}$	$4 \cdot 10^{-3}\,\mathrm{K}^{-1}$
$R_{\mathrm{th,eff}}$	$6 \cdot 10^6\,\mathrm{K{\cdot}W}^{-1}$		

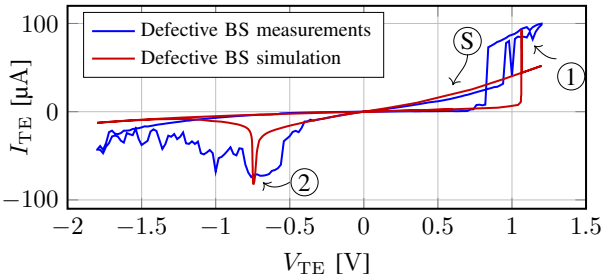
1) Physical Defect Modeling: In this step, the effects of the defect on the physical parameters of the RRAM device are analyzed and modeled. Section III showed that a shortage of ions that can bind free oxygen ions causes CS in BS devices, which leads to the IUSF. To appropriately model this phenomenon, we use the physics-based HfO_x RRAM model for CS, JART VCM v2, from [20]; the model describes CS as the exchange of oxygen vacancies between two regions (region 1 and 2, see Fig. 1a) in the oxide; the paper also describes how the model can be adapted to perform BS by introducing asymmetry between these regions via their lengths, barrier height, and electron mobility. Based on this, we adapt the model so that region 1 becomes the BS CF, and that the switching depends solely on this region. Then, we include the unwanted CS by changing two of the model parameters: the initial oxygen vacancy concentration in region 1 (parameter N_{init1}), and the maximal vacancy concentration in the oxide (parameter N_{max}). The former controls the number of oxygen vacancies that form the CF in region 1, while the latter controls the overall number of oxygen vacancies in the oxide. Since the model is based on the exchange of vacancies between region 1 and 2, the ratio $N_{\mathrm{init1}}/N_{\mathrm{max}}$ determines the number of vacancies that can be in region 2. The lower this ratio, the more vacancies can move to region 2 and thus the stronger the CS effect.

2) Electrical Defect Modeling: The next step is to incorporate the affected physical parameters of the device (e.g., the filament radius) into its electrical parameters (e.g., V_{SET}, R_{RESET}). JART VCM v2 is written in Verilog-A. Hence, it can directly be integrated in a SPICE simulator to derive the electrical behavior of the memory in the presence of the modeled defects.

3) Fitting and Model Optimization: The model is fitted to match the measurements from Section III. The parameter values used for the JART VCM v2 model are listed in Table III. Fig. 6a shows the simulation results for the BS device model as well as the measurements of defect-free devices for different SET-RESET cycles. The model matches the measurements well, except for the RESET current decrease, which is steeper than the measured current decrease. This is because the model does not include the randomness of the filament growth and rupture, and it is based on the CS model assuming that vacancies always shift between the two switching regions; in a real RRAM device, the exchange is between the capping layer and the oxide, leading to a less abrupt switching.



(a) Simulation vs. measurements for defect-free device.



(b) Simulation vs. measurements for defective device

Fig. 6: Comparing defect-free and defective device simulation model.

Fig. 6b shows the simulation results (of the calibrated model) and the measurement data for a defective BS RRAM device suffering from an IUSF; we use the same parameters as in Table III but with N_{init1}=$1.3 \cdot 10^{27}\,\mathrm{m}^{-3}$ and N_{max}=$8.0 \cdot 10^{27}\,\mathrm{m}^{-3}$ so that the ratio $N_{\mathrm{init1}}/N_{\mathrm{max}}$ is rather small while still being physically realistic. It can be seen that the simulation and the measurements match well, and the the simulation can predict the switching moments (①, ②), and the final resistance states (Ⓢ). Note that that the simulation has marginal deviations compared with the data, e.g., some shifts in SET and RESET voltages. This is again caused by the used physical model that favors the abrupt switching over the more gradual switching. Nonetheless, the obtained device model is accurate enough (e.g., accurate in the prediction of the intermediate state Ⓢ) to be used for fault modeling.

The model is also calibrated for weak devices modeling such as that shown in Fig. 4c, e.g., using N_{init1}=$1.8 \cdot 10^{27}\,\mathrm{m}^{-3}$ and N_{max}=$8.0 \cdot 10^{27}\,\mathrm{m}^{-3}$. The results (not shown here) show a very good matching between measurements and simulations.

V. Fault Modeling and Analysis

To describe the faults, we will use the fault primitive (FP) notation as $\langle \mathrm{S/F/R} \rangle$ [21]. Here, S denotes the sensitizing operation that is applied; e.g., S=1w0 denotes writing a '0' to a cell that previously stored a '1', and S=1r1 denotes reading a '1' from a cell that stores a '1'. F denotes the faulty state of the cell after the operation has completed; i.e., $\mathrm{F} \in \{0, 1, \mathrm{U}\}$. Finally, R denotes the output if the final operation in S is a read operation, where $\mathrm{R} \in \{0, 1, ?, -\}$. '?' indicates a random read output (i.e., it is unpredictable if '1' or '0') that might occur when the input of the SA is to close to its reference; '$-$' is used if there is no read output expected.

In order to analyze the IUSF effects on RRAM, a SPICE-based simulation is built; it consists of a 1T1R cell (with same dimensions as those devices used during the characterization) and the required circuitry to drive appropriate voltages in the three control lines WL, BL and SL (see Fig. 3b). The defect-free device is now replaced with the model of the defective RRAM device obtained in the previous section. The defect strength is governed by the ratio $N_{\mathrm{init1}}/N_{\mathrm{max}}$; N_{init1} is varied from $1.2 \cdot 10^{27}\,\mathrm{m}^{-3}$ to $2.0 \cdot 10^{27}\,\mathrm{m}^{-3}$, and N_{max} from $3.0 \cdot 10^{27}\,\mathrm{m}^{-3}$ to $8.0 \cdot 10^{27}\,\mathrm{m}^{-3}$ to fit within realistic physical limits [22] and ensure proper functioning of the model. Similar to the characterization, the voltages are applied via the BL and are swept from $0\,\mathrm{V}$ to $1.2\,\mathrm{V}$ back to $0\,\mathrm{V}$ for SET, as this is the only operation that can sensitize the fault. While performing SPICE simulations, we inspect both the final resulting resistance of the defective device (e.g., R_{SET} after SET operation) and the I-V graph; these are used to derive the behavior of the memory in the presence of the modeled defects. For example, if the final device resistance is outside of the R_{SET} range, then F=U, and if the undesired CS occurs but only disturbs the R_{SET} value without putting it outside the spec, then it is a weak fault.

TABLE IV: Fault Analysis Results for IUSF.

$N_{\mathrm{init1}}/N_{\mathrm{max}}$ [−]	N_{max} [$10^{27}\,\mathrm{m}^{-3}$]	N_{init1} [$10^{27}\,\mathrm{m}^{-3}$]	Fault
0.15	8.0	1.2	⟨0w1/U/−⟩
0.18	8.0	1.4	⟨0w1/U/−⟩
0.20	8.0	1.6	Weak fault
0.23	8.0	1.8	Weak fault
0.25	8.0	2.0	Weak fault
0.27	6.0	1.6	Fault free
0.30	6.0	1.8	Fault free
0.53	3.0	1.6	Fault free
0.67	3.0	2.0	Fault free

Table IV shows the obtained results. Note that observed faults can be classified into two types: *strong* and *weak* faults. Strong faults are faults causing functional errors and can always be sensitized by applying a sequence of operations. In contrast, weak faults do not cause functional errors; instead, they cause parametric deviations (e.g., disturbances in the SET state). In the table, strong faults are described with FP notation. It can be seen that faults are sensitized when the ratio $N_{\mathrm{init1}}/N_{\mathrm{max}}$ decreases; strong faults IUSFs are sensitized for ratios below 0.2, while weak faults are caused for ratio's between 0.20 and 0.25. A lower ratio gives more room for vacancies to move from region 1 into region 2. This makes it easier for the device to perform the undesired CS.

VI. Test Development

As shown in Table IV, the defect causes strong and weak faults. A straightforward test for the strong fault IUSF would be a *march test*. However, due to the nature of the faults (being intermittent and causing the cell to switch into 'U'), a march test cannot guarantee the detection of such a fault. It will rather *probabilistically* detect the fault; reading this state will sometimes result in '1' and sometimes in '0'. The following march algorithm can be used:

$$\text{March-IUSF} = \left\{ \Updownarrow (\mathrm{w0}, \mathrm{w1}, \mathrm{r1})^k \right\}$$

where $\Updownarrow$ indicates any memory addressing order, w0 denotes a RESET operation, w1 a SET operation, r1 a read 1 operation,

and k indicates the number of times the sequence is applied. If we assume that reading a cell in 'U' state results the same probability of getting '1' or '0' (i.e., $50\,\%$), and that the occurrence probability of IUSF is P_{IUSF}, then the detection probability is: P_{d}=$1-(1-(P_{\mathrm{IUSF}}\cdot 50\,\%))^{k}$. Assuming that P_{IUSF}=$1.068\,\%$ (see Section III) results in $k=560$ to realize a fault coverage (FC) of FC=$95\,\%$, and in k=1291 to realize FC=$99\,\%$. Hence, realizing high FC needs long test time; not to mention the potential impact of repeating memory accesses on the endurance. Note that the detection capabilities might be further improved by adding additional stress factors, e.g., by using back-to-back operations and special data backgrounds.

To reduce the test time while providing high fault coverage, design-for-test (DfT) schemes can be used. For example, the authors in [23] present a DfT scheme that deploys different references in the SA to perform a binary search to find the resistance of the RRAM device. This scheme can be modified to detect the IUSF by setting the reference of the SA directly at the boundary between the '1' and 'U' state, making the read operation deterministic; i.e., if IUSF occurs, then the SA will *always* output '0', and detect it. This results into P_{d}=$1-(1-P_{\mathrm{IUSF}})^{k}$. In this case realizing a FC=$95\,\%$ requires k=279 and FC=$99\,\%$ requires k=644; a reduction in test time of about $\approx$2X as compared with march test only.

To further decrease the test time while keeping high FC, specialized DfTs are required. Such schemes could aim at increasing P_{IUSF} (and thus decreasing k) by e.g., increasing the current through the device during SET. This will lead to a wider CF which increases P_{IUSF} and thus decreases P_{weak} [17]. This could be done by boosting the WL or BL voltage during SET in test mode. A drawback of this scheme is that it may lead to lower R_{SET}, which will increase power consumption. Alternatively, additional DfT schemes could be introduced that continuously monitor and verify write operations, for example by performing a read operation using the above mentioned DfT from [23] after every SET operation. This will increase the write latency and energy consumption, but it will significantly boost the FC.

VII. Discussion and Conclusion

This work has demonstrated the existence of some unique defects in RRAM that can not be modeled neither detected using traditional memory test approaches; these defects cause the Intermittent Undefined State Fault (IUSF). The Device-Aware Test approach has been put in place in order to appropriately model the defects and develop efficient test solutions. Given the nature of IUSF being intermittent, it is worth to note the following:

- **Prevention versus detection:** As the detection of this fault is hard and could be expensive, it is worth to invest in preventing it. This can be done by tightly controlling the SET current via the access transistor or by optimizing the production process of the capping layer so that always enough oxygen ions can be bound and CS is prevented.
- **Intermittent behavior modeling:** The defect model developed in this work does not consider the intermittent nature of the fault. Additional effort is now put in further extension of the model to include this behavior and cycle-to-cycle variations similar to [22].

Finally, this work has shown the importance of identifying and modeling new unique defects in RRAMs in an appropriate manner. The space of RRAM manufacturing defects is not explored completely yet, and even new defects may be introduced with further downscaling. Hence, further analysis of such space is needed especially now that the traditional memory approach is not able to guarantee the detection of unique RRAM faults, as demonstrated in this work.

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