MSc THESIS IN ELECTRICAL ENGINEERING

ANALOG FRONT-END WITH SLOW-TIME FEEDBACK FOR TRANSCRANIAL FUNCTIONAL ULTRASOUND

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ABSTRACT

Transcranial Doppler (TCD) ultrasound is a non-invasive technique for assessing cerebral blood flow, offering valuable insights for the diagnosis and monitoring of brain disorders. Despite its importance, its effectiveness is limited by the high dynamic range required at the receiver front-end due to clutter components from skull and tissue reflections. Traditional approaches rely on high-dynamic-range amplifiers and high-resolution ADCs to detect the useful blood flow signal against the clutter signal, leading to high power consumption and data throughput.

This thesis addresses this challenge by incorporating a feedback path from the receiver output directly to the transducer. This approach enables effective clutter suppression, thereby reducing the dynamic range requirements of the receiver chain. To achieve this, the system employs a slow-time integrator at the feedback path, ensuring stable tracking of the clutter component.

Key building blocks, including a boxcar integrator with micro-beamformer functionality, a slow-time delta modulator, a DAC, and a buffer, are thoroughly analyzed. The system is designed and implemented in a TSMC 180 nm BCD process, realizing an ASIC tailored for an 8-element CMUT array. MATLAB simulations demonstrate the feasibility of reducing the dynamic range requirements by up to 57 dB, while the transistor-level prototype achieves a power consumption of 1.984 mW per element. The study also provides valuable insights into the trade-offs associated with implementing clutter suppression in an ASIC ultrasound system.

Keywords: Transcranial Functional Doppler Ultrasound; Clutter Filtering; Dynamic Range Reduction; Delta Modulator;

CONTENTS

1

INTRODUCTION

1.1. CLINICAL MOTIVATION AND IMAGING TECHNIQUES

1.1.1. CLINICAL PROBLEM: BRAIN DISORDERS

Brain disorders, such as strokes and Alzheimer's disease, are among the leading causes of death globally, claiming millions of lives each year [1].

Statistics from the World Health Organization (WHO), shown in figure 1.1, depict that in 2021 stroke was the third leading cause of death worldwide, while dementia ranks seventh [2]. A striking example comes from the statistics of the Netherlands in 2019 (before the COVID-19 pandemic), when dementia was the leading cause of death (figure 1.1) [2]. Furthermore, in the Netherlands, more than a quarter of healthcare resources are dedicated to treating brain disorders [3].

It is therefore evident that brain disorders are a paramount concern demanding substantial advancements from the medical sector.

1.1.2. HEMODYNAMICS AND DIAGNOSTIC NEEDS

In the medical domain, doctors can study the blood flow of vessels and arteries inside the brain in order to diagnose certain brain disorders. The study of blood flow is called hemodynamics. It focuses on how blood moves through the heart, arteries and veins due to pressure, flow and resistance. Understanding hemodynamics helps explain how the heart pumps blood, how blood vessels regulate blood flow, and how various physiological or pathological conditions affect circulation. Furthermore, it can evaluate injuries, inflammations or cancer tumors of the targeted studied areas [4]. With the right tools such as Ultrasound scan or MRA scan, and with the knowledge of hemodynamics, doc-

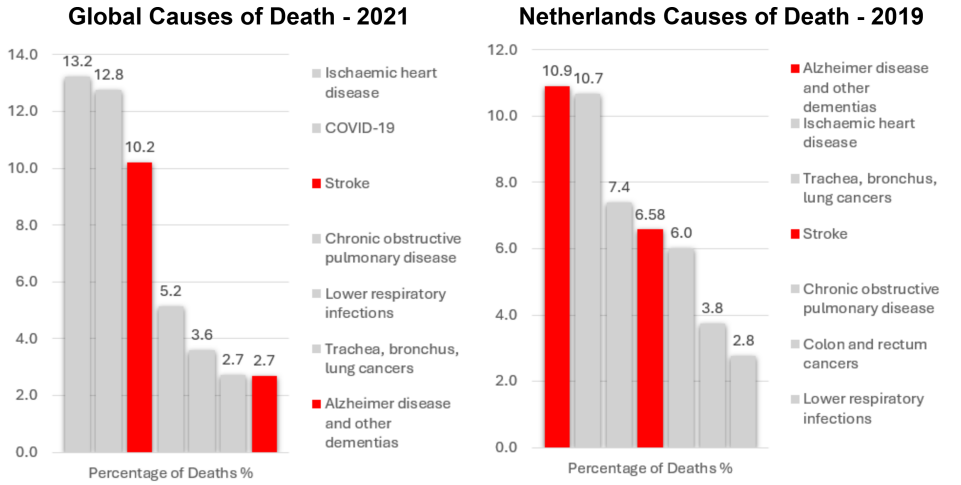


Figure 1.1: Global Causes of Death 2021 and Netherlands Causes of Death 2019. Source [2].

tors can diagnose and monitor such disorders[5]. Following the diagnosis, appropriate treatment can be provided to reduce the associated risks of the disorder [6].

1.1.3. CURRENT IMAGING MODALITIES

Several imaging techniques are available for assessing cerebral hemodynamics, including Magnetic Resonance Angiography (MRA), Computed Tomography Angiography (CTA), and Transcranial Doppler (TCD) ultrasound. MRA and CTA provide high-resolution images of cerebral vessels, while TCD offers real-time blood flow velocity measurements using ultrasound. Each modality has unique advantages and limitations that influence its suitability for specific clinical applications. A detailed comparison of these techniques, with emphasis on why TCD was chosen for this study, is presented in Section 1.2.

1.1.4. EXAMPLE - STENOSIS

A brief example is given to introduce the concept [7]. In figure 1.2 a) a sketch of a vessel with stenosis condition is depicted. Stenosis in the brain refers to the narrowing of arteries within the skull, a condition often caused by the build-up of plaque. This narrowing restricts blood flow to the brain, potentially leading to stroke or transient ischemic attacks. If a vessel becomes narrowed, the velocity of the blood will increase as the blood passes through the stenosed section of the vessel. Beyond the narrowing, a flow reversal occurs as show in figure 1.2 a). This phenomenon of blood flow changes can be observed using color flow ultrasound.

Picture 1.2 b) illustrates an image of such a vessel with a color flow image [7]. The red

illustrates the flow direction to right and the blue the flow direction to left. The color intensity illustrates the speed. It is observed that the velocity increases as the blood flows through a stenosis from left to right, with an area of flow reversal (shown as blue) beyond the narrowing. The vein lying over the artery is also seen in blue.

This example demonstrates how ultrasound imaging, combined with an understanding of hemodynamics, enables clinicians to identify and diagnose conditions such as stenosis [8], [9], [10], [11].

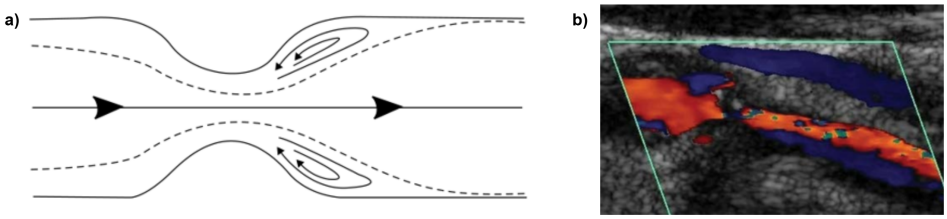


Figure 1.2: a) Sketch of Vessel with stenosis disease. b) Color flow image showing a vessel with stenosis disease. Source: [7].

1.2. TRANSCRANIAL DOPPLER ULTRASOUND

1.2.1. TRANSCRANIAL DOPPLER ULTRASOUND OVERVIEW

Transcranial Doppler (TCD) sonography is a non-invasive clinical technique that uses Doppler ultrasound to measure the characteristics of blood flow within the cerebral arteries [12]. Doppler ultrasound recording of blood flow at extracranial arteries was first reported in 1960 by Miyazaki and Kato [13]. The transcranial application of this technique was introduced later in 1982 by Aaslid, Markwalder, and Nornes [14].

Unlike conventional B-mode ultrasound 1.3.2, TCD primarily provides blood flow information through spectral waveforms (Section 1.3.4, Figure 1.10), which can also be read-out audibly [7], [14], [15], [16]. In addition, TCD can employ color flow imaging (Figure 1.2), as previously discussed at the stenosis example in Figure 1.2.

The transducer emits low-frequency ultrasound (~ 2 MHz) that penetrates the skull and reflects from intracranial vessels [14]. Reflected signals are processed via spectral analysis to estimate cerebral blood flow velocity (CBFV), providing real-time hemodynamic information [16], [17], [18]. TCD belongs to functional imaging methods, since it provides information on brain function (hemodynamics) instead of depicting structural anatomy [19], [20].

A major challenge is the attenuation of the transmitted signal by the skull which reflects most of the transmitted energy. In contrast, the echoes returning from blood vessels are much weaker[20]. To address this, TCD relies on “acoustic windows,” areas of the skull where the bone is naturally thinner, minimizing the energy from skull reflection

and improving signal penetration [6], [11], [21].

Picture 1.3 a) and b) show an example of TCD usage. In figures 1.3 a transducer is attached on the skull at an acoustic window where the bone is thinner. The ultrasound beams are sketched showing the focal point on a vessel inside the skull.

Figure 1.4 depicts a commercial TCD unit. The unit is cart-based, making the device portable.

TCD ultrasound has a wide range of clinical applications, including monitoring cerebral blood flow and detecting vascular abnormalities [10], [11], [15], stenosis detection [8], [9], [10], [11].

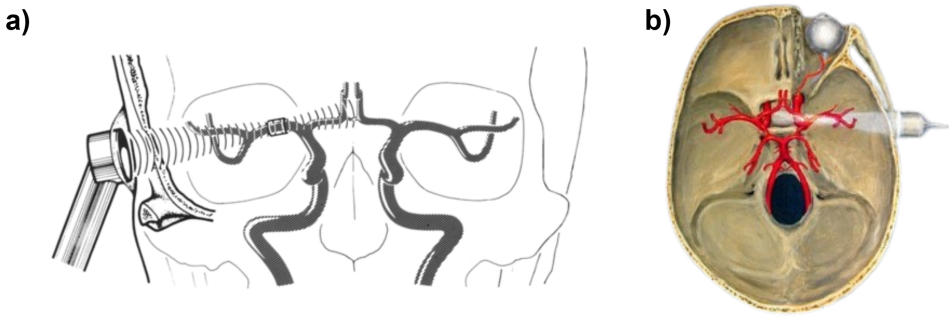


Figure 1.3: a) Frontal view of the ultrasound probe directed toward the middle cerebral artery (MCA). The cylinder around the MCA indicates the observation region (sampling volume) for the Doppler recording [14]. b) Transcranial Doppler insonation of the cerebral circulation. Rune Aaslid [15].

1.2.2. TCD ADVANTAGES AND LIMITATIONS

TCD sonography offers several advantages for cerebrovascular diagnostics. It is safe, being non-invasive and relying on non-ionizing ultrasound frequencies around 2 MHz [11]. It is also relatively inexpensive compared to CT and MRI, with lower equipment and operational costs since it does not require specialized facilities [6], [7], [11]. Beyond cost and safety, TCD enables continuous bedside assessment, providing clinically relevant information for both diagnosis and prognosis. For example, serial examinations can reveal hemodynamic changes following ischemic stroke that may be missed by a single MRA scan [21]. Its real-time capability, with delays of less than half a second, makes it particularly useful during neurosurgical procedures and emergency evaluations [5], [11]. In addition, cart-based systems are portable and well-suited for intensive care units, where patient transfer to imaging suites is often not feasible. Finally, ultrasound offers high spatial and temporal resolution, with sample rates above 100 Hz supporting dynamic and functional hemodynamic studies [11], [19], [21].

Figure 1.4: Commercial card-based TCD unit [22].

Despite these strengths, TCD also presents limitations. Because ultrasound must penetrate the skull, where most of the acoustic power is reflected, while relying on weak echoes from the vessels, its sensitivity is low, restricting measurements to large intracranial arteries (>1 mm) [11], [19]. For this reason, insonation is only possible through acoustic windows, regions of thinner skull bone [11],[6]. However, in about 10% of individuals these windows are inadequate, making the examination impossible [6]. In such cases, contrast agents or even skull-thinning may be required, but these approaches compromise the non-invasive nature of the method and are indicated only for severe pathological conditions [7], [11], [20]. Furthermore, TCD examinations are highly operator-dependent, requiring detailed anatomical knowledge and technical skill to maintain optimal insonation angles, which directly affects the consistency and quality of results [6], [11], [16], [21].

Compared with alternative imaging techniques such as CTA and MRA, TCD is far more cost-effective, portable, and suitable for bedside or continuous monitoring. CTA and MRA provide detailed vascular imaging but require large, expensive systems, involve radiation exposure or contrast-agent risks, and are unsuitable for frequent or real-time use [7], [10], [11], [19], [21], [23]. Thus, while CTA and MRA remain invaluable for detailed vessel imaging, TCD offers a unique balance of safety, affordability, and dynamic monitoring capability.

Sensitivity:
It is important to note that in the medical domain, and specifically in the context of Transcranial Doppler (TCD), *sensitivity* is referred as the ability of the device to recognize weak blood flow signals in contrast to the strong clutter signals originating from

surrounding tissues and bone structures. It is therefore related to the detection limits of the device, which are tied to the dynamic range of the system, as will be described in Section 2.1, while it does not refer to the electrical-domain sensitivity expressed in Volts per Pascal.

1.2.3. TOWARDS WEARABLE TCD SYSTEMS

Traditional TCD systems, although more portable and less expensive than CTA or MRA, remain relatively bulky, costly, and require experienced operators [11]. These limitations restrict their use, as TCD is often not available on an emergent basis and is not routinely accessible in many centers [24]. Furthermore, some clinical situations require prolonged monitoring of more than one hour, which is difficult to achieve with conventional systems [10].

To overcome these limitations, recent research has focused on miniaturizing TCD units and adapting them for wearable or handheld use [10], [11], [24]. Wearable devices enable continuous monitoring, while handheld systems allow for instantaneous bedside assessment, rapid estimation of vessel status while awaiting further imaging, and serial monitoring of patient response during therapeutic interventions [24].

An example of a wearable TCD system is shown in Figure 1.5 a) and b). In Figure a) [10], the TCD device is integrated into the side of a pair of glasses, supporting continuous monitoring during daily activities. Figure b) [24] illustrates a stethoscope-like TCD tool, demonstrating the feasibility of a compact, physician-operated device for repeated bedside measurements of cerebral hemodynamics during therapeutic procedures.

Developing user-friendly, self-fixating transducers and enhancing signal processing techniques are key steps toward advancing wearable TCD systems [10]. Wearable or handheld TCD devices are characterized by their low cost, small form factor, low power consumption, and minimal data rate requirements. This characteristic features define typical design specifications for wearable TCD systems.

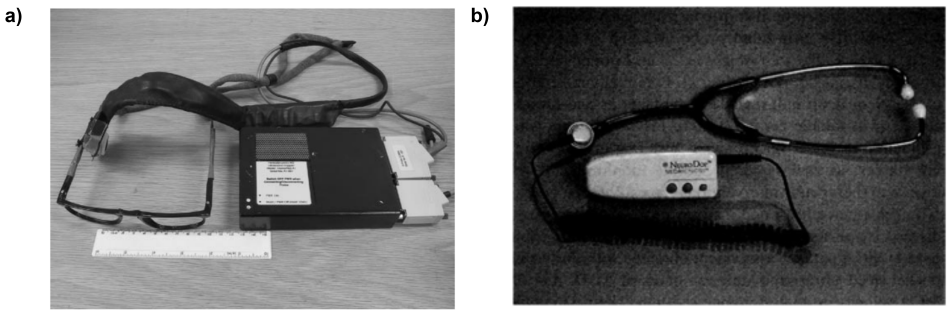


Figure 1.5: a) The ambulatory transcranial Doppler apparatus. The transducer is placed at the side of the glasses aiming the side of the head [10]. b) Pocket-Sized Transcranial Ultrasound Device [24].

1.3. DIAGNOSTIC ULTRASOUND PRINCIPLES

1.3.1. THE PULSE-ECHO PRINCIPLE

In its most basic configuration ultrasound uses the pulse-echo principle to create an image. The same principle is used in echo-sounding equipment in boats to measure the depth of water [7]. As illustrated in figure 1.6 a transducer emits a short burst of pulse of ultrasound. This travels through the water until it reached the bottom of the sea. The echo travels back through the water until it reaches the transducer where it is received. Knowing the speed of sound in the water, the distance between the boat and the bottom of the sea can be calculated by measuring the time it took from transmitting the signal until receiving it back. Figure 1.6 illustrates this example showing the time of transmit, echo and receive.

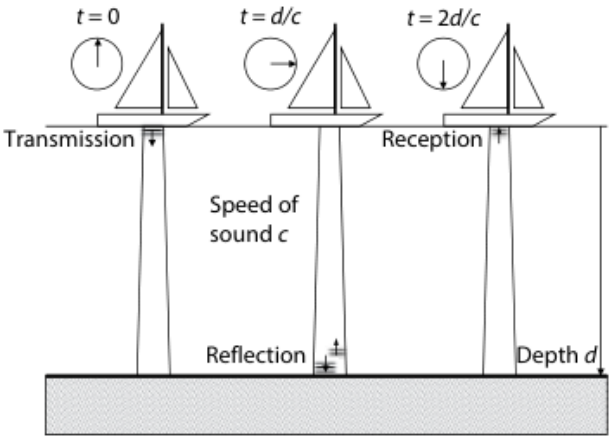


Figure 1.6: Water depth measurement using the pulse-echo principle. Where t is the time, d the distance and c the speed of sound inside the water. By knowing the speed c and measuring the time the depth can be calculated. Source [7].

The same principle is applied in medical diagnostic ultrasound to generate images of internal body structures. The transducer emits ultrasound pulses, and echoes reflected from tissues, organs, or other structures inside the body are detected. By measuring the time between transmission and reception, the system calculates the depth of each reflector, enabling the construction of a detailed image of the examined area.

1.3.2. IMAGE FORMATION - B-MODE

With one transmission of ultrasound pulse the system can receive multiple echos and form an image of one scan line [7]. The brightness of this line varies according to the amplitude or strength of the echo. A two-dimensional image of the target is created by

combining a sequence of 100 or more such lines. This image is referred to as B-mode image, where "B" stands for Brightness. Figure 1.7 a) illustrates how a sequence of lines forms a two-dimensional image, while Figure 1.7 b) shows an actual B-mode ultrasound image of a fetal head.

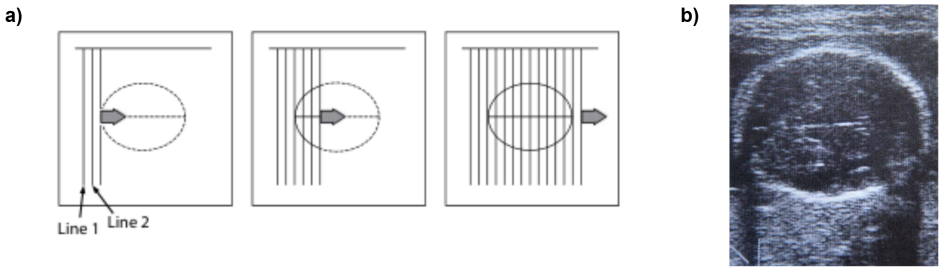


Figure 1.7: a) A B-mode image created by a sequence of received lines. b) A B-mode Ultrasound image of a head of a fetus. Source:[7].

1.3.3. DIAGNOSTIC ULTRASOUND MODES

The aforementioned B-mode imaging is just one of several techniques used in ultrasound to obtain information from inside the human body. Other common modes include A-mode (Amplitude), M-mode (Motion), spectral Doppler, and color flow Doppler imaging [25] , [7]. For example, Doppler modes are particularly useful for detecting and measuring blood flow.

The above information provides a general overview of how ultrasound systems operate. This thesis will specifically focus on Doppler ultrasound scanning.

1.3.4. DOPPLER ULTRASOUND AND DISPLAY

The Doppler effect refers to the change in the observed frequency of a wave compared to its emitted frequency, caused by the relative motion between the source and the observer. This phenomenon is commonly experienced in everyday life. For instance, the changing pitch of an ambulance siren as it moves past an observer. In Figure 1.8, the observer on the left of the ambulance perceives a lower frequency (lower pitch) as the ambulance moves away, while the observer on the right perceives a higher frequency (higher pitch) as the ambulance approaches. This effect can be expressed by the Doppler equation:

$$f_d = f_r - f_t = \frac{2 f_t v \cos\theta}{c} \tag{1.1}$$

where f_d is the Doppler frequency shift, f_r is the received frequency, f_t is the transmitted frequency, v is the velocity of the source, c is the speed of sound, and θ is the angle

between the observer and the source.

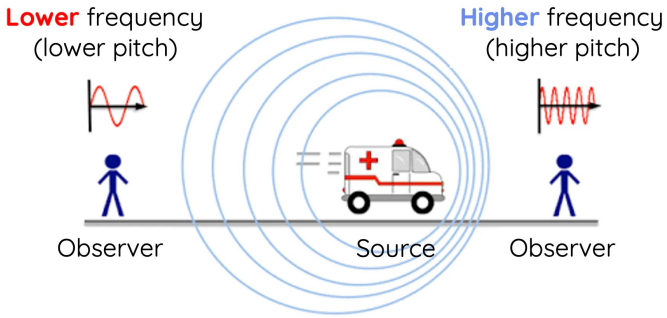


Figure 1.8: Doppler effect: an ambulance passing by an observer. Source: [26].

In diagnostic ultrasound Doppler scanning, the same principle applies to asses blood flow in vessels and arteries. A transducer emits ultrasound pulses that travel through body tissues, organs, and blood vessels. The ultrasound waves are partially reflected back to the transducer from moving blood cells. By measuring the frequency shift (Doppler shift) of these echoes, the system can determine the velocity of the blood flow, as described by the equation 1.1 [17], [7]. Figure 1.9 illustrates, on the left, a transducer above a blood vessel with moving red blood cells, and on the right, the blood flow speed and direction, the angle θ relative to the observer, and the velocity component $v\cos\theta$.

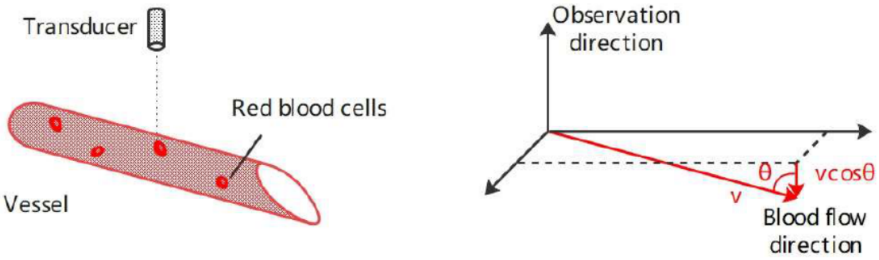


Figure 1.9: Doppler effect applied in blood flow detection. Source: [25].

Two main ways of displaying the information extracted from the ultrasound Doppler scan are ([7]):

Spectral Doppler
The velocity information detected from moving blood cells in the vessel is displayed in the form of a frequency shift-time plot [7]. The vertical axis indicates that the frequency shift is directly related to the blood velocity. The brightness of the image indicates the amplitude of the the detected ultrasound with that particular frequency. Figure 1.10 illustrates such a spectral Doppler display. The same information can also be represented

as an audible sound where pitch and loudness vary with flow velocity [7], [14], [15], [16].

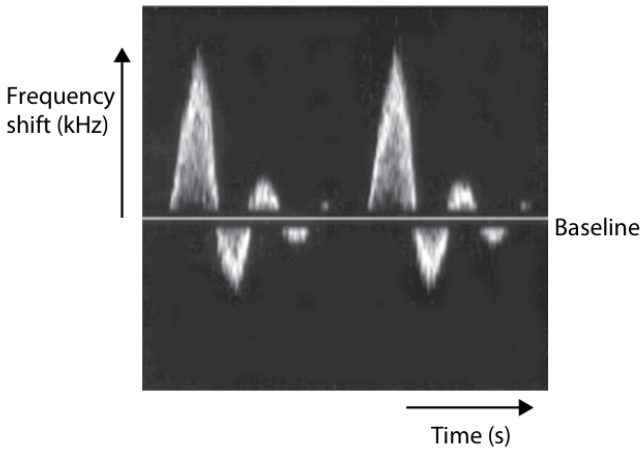


Figure 1.10: Spectral Doppler display, frequency shift vs time plot. Source: [7].

2D color flow imaging
The Doppler signal is displayed as a 2D color image superimposed on the B-mode image [7]. The color indicates the direction of blood flow, variations in the same color represent the speed, and brightness represents the amplitude of the signal. The aforementioned stenosis case in Figure 1.2 illustrates this concept.

1.3.5. RECEIVED SIGNAL IN DOPPLER ULTRASOUND – CLUTTER VS DOPPLER SIGNAL

To understand how Doppler ultrasound works, it is important to first examine the nature of the received signal. When ultrasound is emitted from the transducer, it passes through various tissues, bones, and other internal structures before reaching the target vessels and arteries. The task of the Doppler ultrasound receiver is to extract the Doppler signals originating from moving blood cells which carry the important information about blood flow velocity and direction. Any unwanted signals are referred to as clutter. Clutter from bone and tissue can be up to 60 dB stronger than the Doppler signal from blood [23].

Figure 1.11 illustrates a Doppler transducer (Transcranial Doppler Ultrasound transducer) emitting an ultrasound signal. Reflections from the artery, referred to as the Doppler signal, and reflections from the skull and tissue, referred to as clutter, travel back to the receiver. In reality, the transducer is attached to the skull without any air gap, however the illustration shows a gap for clarity of the superimposed clutter and Doppler received signals. The figure shows the transmitted and received signals in the time domain, along with their corresponding representations in the frequency domain. The frequency plot highlights the 57 dB difference between the clutter and Doppler signals, as

well as the Doppler frequency shift.

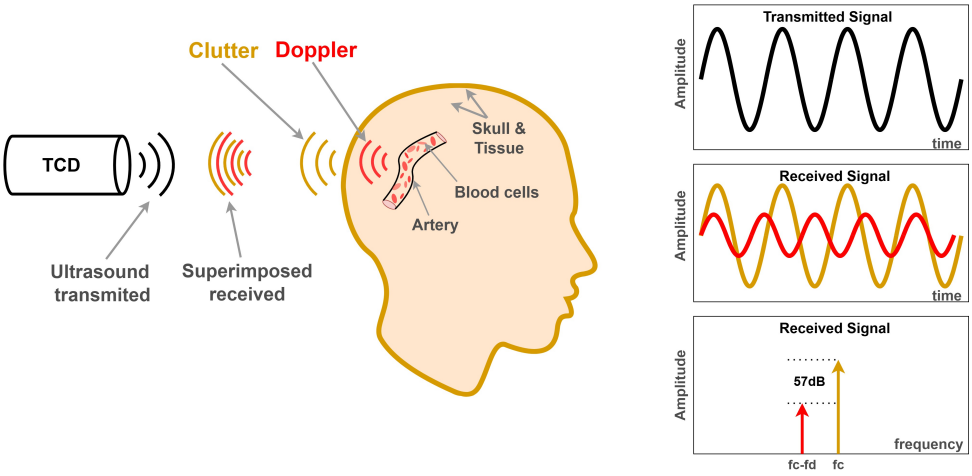


Figure 1.11: Simplified illustration of clutter and Doppler signals in a Transcranial Doppler (TCD) system, along with their transient and frequency responses.

1.4. CONTINUOUS-WAVE AND PULSED-WAVE DOPPLER

In the Doppler systems the ultrasound can be transmitted in the form of a continuous-wave (CW) or a pulse-wave (PW). In the CW the signal is transmitted continuously while in PW the system transmits short pulses of ultrasound.

The main advantage of PW Doppler is that the depth information can be assessed through the pulse-echo principle. The same transducer can be used to transmit and receive information as illustrated in figure 1.12. On the other hand, the main drawback is that there is an upper limit to the Doppler frequency shift which can be detected.

CW Doppler system needs a separate transducer to transmit and receive the ultrasound. The drawback is that the depth can not be controlled since it is related to the fixed relative position of the transmitter and receiver. Figure 1.12 highlights this. The main advantage of the CW system is that the signal processing required for extracting the Doppler signal is less complex.

1.4.1. CONTINUOUS-WAVE DOPPLER SIGNAL PROCESSING

At the CW-Doppler systems, the received ultrasound signal undergoes a three-step process to extract the Doppler frequency information.

Demodulation

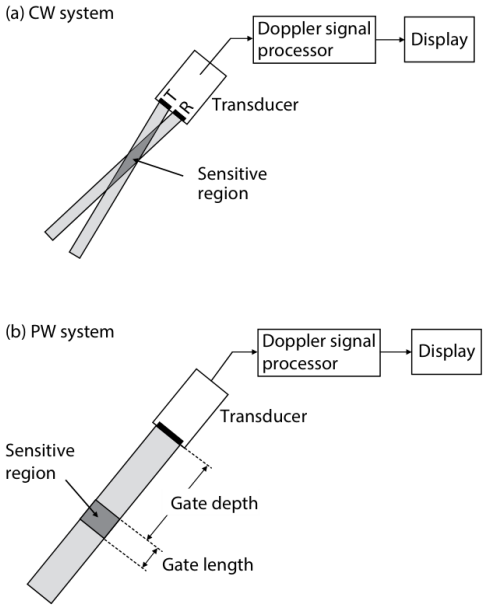


Figure 1.12: Illustration of CW and PW Doppler system. Source: [7].

The first step is demodulation, which separates the Doppler frequency components from the transmitted carrier signal. This is achieved by mixing (multiplying) the received ultrasound signal with a reference signal at the same frequency as the transmitted pulse. Since the received signal is slightly shifted in frequency due to motion, this multiplication produces two components:

- A **low-frequency component** corresponding to the Doppler shift
- A **high-frequency component** centered around twice the transmit frequency

This relationship is described by the product-to-sum equation:

$$\cos(2\pi f_1 t) \cdot \cos(2\pi f_2 t) = \frac{1}{2}\Big[\cos\big(2\pi(f_1 + f_2)t\big) + \cos\big(2\pi(f_1 - f_2)t\big)\Big] \tag{1.2}$$

Example: Figure 1.13 depicts an example of a CW signal undergoing demodulation. Consider an ultrasound system transmitting at $f_0 = 2.7$ MHz, with the speed of sound inside the body being $c = 1540$ m/s [7]. The blood inside a vessel moving at $v = 1$ m/s [7] will reflect an echo at approximately 2.7035 MHz. This is derived due to the Doppler shift of about $f_d = 3.5$ kHz from the DOppler shift equation 1.1.

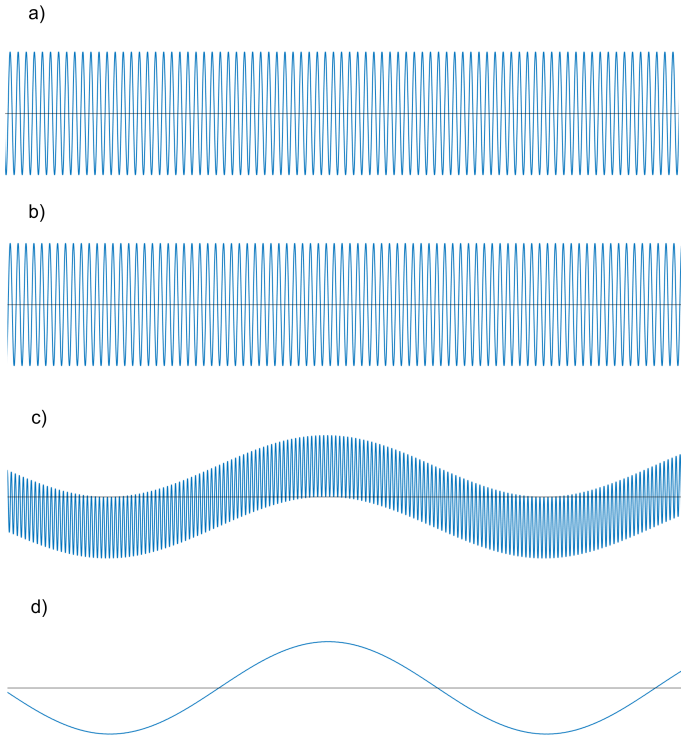


Figure 1.13: CW Doppler signal - Demodulation process.

When the received signal (2.7035 MHz) is mixed with the reference (2.7 MHz), the result from 1.2 is:

- A high-frequency component at $f_0 + (f_0 + f_d) = 5.4035$ MHz
- A low-frequency component at $|(f_0 + f_d) - f_0| = 3.5$ kHz

A low-pass filter then removes the high-frequency term, leaving the Doppler information in the baseband. At this stage, the signal contains the Doppler shift from blood flow but also clutter from slowly moving tissue and stationary structures (e.g., bone). Figure 1.14 a) and b) illustrates the process of demodulation in the frequency domain.

High-pass Filtering
The next step is clutter removal via high-pass filtering. As illustrated in Figure 1.14 c), this filter suppresses components below a certain threshold frequency, eliminating contributions from stationary and slowly moving tissues. However, a limitation of this technique

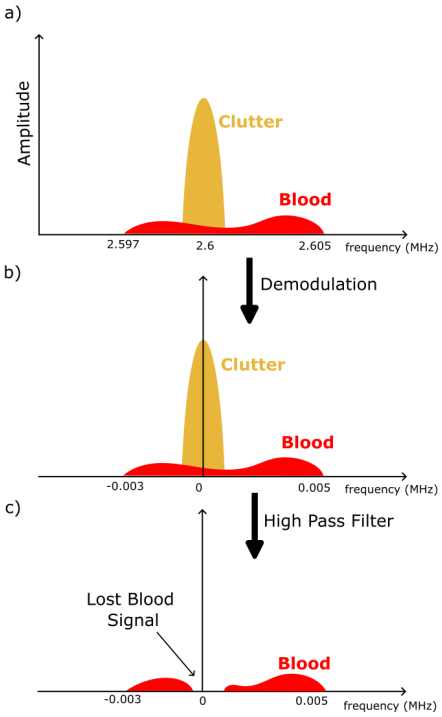


Figure 1.14: Frequency spectrum of CW Doppler.

is that Doppler frequency shifts from slowly moving blood will also be lost as illustrated in figure 1.14.

Frequency Estimation
Finally, the Doppler signal, which is still in the time domain, undergoes frequency analysis using the Fast Fourier Transform (FFT). The FFT computes a complete Doppler spectrum every 5–40 ms[7], which is then displayed as a spectrogram as previously described at 1.3.4 at figure 1.10.

1.4.2. PULSED WAVE DOPPLER

While continuous-wave (CW) Doppler is effective for detecting blood flow, it cannot provide any axial information, leading to potential signal overlap from different vessels and uncertainty in velocity estimation. Pulsed-wave (PW) Doppler was developed from *Baker 1970* [27] to overcome this issue by enabling depth-specific measurements and improved velocity profiling.

In the pulsed-wave Doppler the same principle as the CW of demodulation, high fre-

quency filter and frequency estimation could be applied [7]. However, time-domain waveform narrowing leads to spectrum broadening as depicted in figure 1.15 [23]. This causes overlap between two signals spectrum. Since the static components are much stronger in amplitude compared to Doppler-shifted components, this can introduce significant errors when estimating the Doppler shift using the aforementioned method [7], [23].

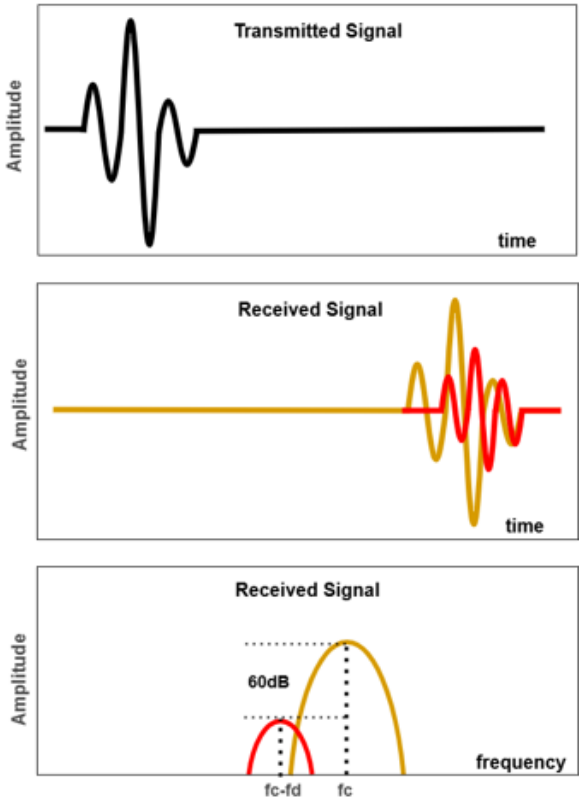


Figure 1.15: Time and frequency domain of a Pulsed Wave Doppler.

Slow-Time Sampler

To overcome this limitation, pulsed-wave Doppler employs a different approach for Doppler frequency estimation. Instead of relying on a single pulse, it utilizes sampling across multiple successive transmit-receive cycles, taking advantage of the time shift information.

To clarify and distinguish operations within a single transmit/receive (T/R) cycle from those occurring across successive cycles, this thesis adopts the following terminology:

- **Fast-time** refers to operations that occur within a single T/R cycle.
- **Slow-time** refers to operations that occur across successive T/R cycles.

An example illustrating this multi-cycle processing concept is shown in Figure 1.16. The figure depicts signals received from a single blood cell moving away from the transducer. The middle plot illustrates the fast-time received signals for five successive transmit/receive cycles. For clarity, the Doppler and clutter signals are shown separately, although in reality they are superimposed. The right plot illustrates the slow-time sampled signal where one sample is taken for each pulse emitted. Assume the pulse repetition fre-

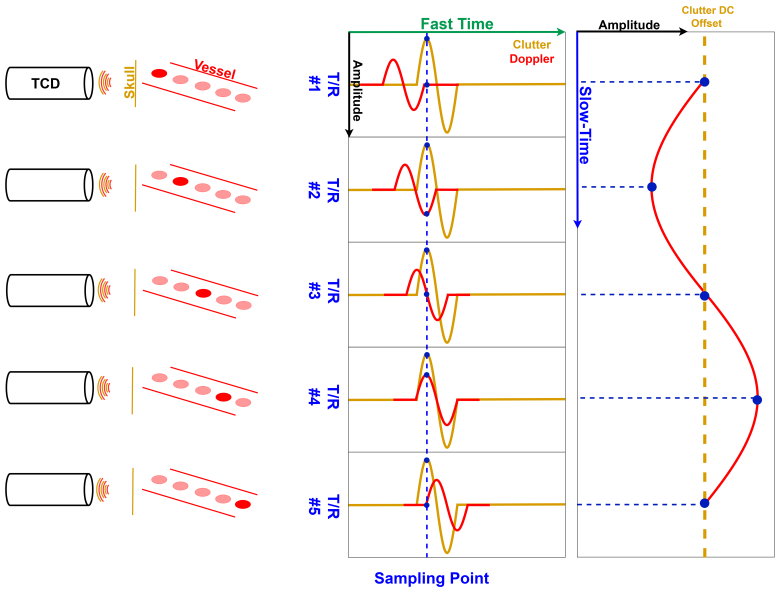


Figure 1.16: Pulsed-wave Doppler processing between successive transmit-receive cycles.

quency is f_{prf}, the carrier frequency is f_s and the Doppler shift frequency is f_d. The time delay of the reflection from a moving object between two successive T/R cycles is given by:

$$\delta t = \frac{2v\cos\theta}{c\, f_{\text{prf}}} \tag{1.3}$$

This time delay introduces a phase shift, assuming $f_d \ll f_s$, so that $f_s - f_d \approx f_s$:

$$\delta\phi = 2\pi \cdot \frac{2v\cos\theta}{c\, f_{\text{prf}}} \cdot f_s \tag{1.4}$$

Consequently, in the slow-time domain, a sinusoidal signal is obtained with frequency:

$$f_{\text{out}} = \frac{\delta\phi}{2\pi} f_{\text{prf}} = \frac{2|v|\cos\theta}{c} f_s \tag{1.5}$$

which corresponds exactly to the Doppler shift frequency, as described in Equation 1.1. A detailed derivation is provided in [17].

In contrast, for static reflections, the signal remains constant across successive T/R cycles, resulting in a fixed value in the slow-time domain. Therefore, in the slow-time spectrum, the static component appears at DC, while the Doppler component is located at the Doppler shift frequency. This separation enables clutter filtering in the slow-time domain.

High-pass Filtering and Frequency Estimation
Subsequently, the signal obtained from the slow-time sampler passes through a high-pass filter in order to remove the clutter components. Finally a frequency estimation is applied using FFT to compute the Doppler frequency and display it.

Is PW Doppler a Doppler shift detector?
This approach does not rely on the classic Doppler effect, instead it is an artifact in this approach [17] , [7]. PW Doppler measures the rate of change of phase between successive echoes received. From this phase shift the target velocity can be estimated using the same equation 1.1.

Aliasing
A key constraint of pulsed-wave (PW) Doppler is its dependence on the pulse repetition frequency (PRF). As the Doppler shift is sampled, the PRF needs to meet the Nyquist criterion to avoid aliasing. In most cases, this implies that the following condition must be met:

$$f_{PRF} > 2f_d \tag{1.6}$$

When aliasing does occur, the velocity information can often not correctly be recovered.

Conclusion
As analyzed, CW Doppler offers a straightforward method for estimating blood velocity but does not provide axial information. In contrast, PW Doppler enables estimation of axial velocities through the pulse–echo principle. Consequently, the IC architecture is designed to be compatible with PW Doppler. Furthermore the signal processing of it adopts a similar approach to PW Doppler signal processing analysis, leveraging the phase-shift characteristics of blood signals to calculate the Doppler shift frequency.

1.5. MOTIVATION AND THESIS OUTLINE

Based on the preceding analysis, it is evident that Transcranial Doppler (TCD) offers several key advantages as a clinical tool. Nevertheless, current TCD systems face two significant limitations: low sensitivity and restricted miniaturization. Enhancing sensitivity would improve reliability and broaden clinical applications, while further miniaturization could enable continuous, wearable monitoring. Together, these challenges represent critical areas of research with the potential to improve patient monitoring and expand TCD's role in modern healthcare.

To address these challenges, this thesis focuses on the analog front-end receiver unit of TCD systems, investigating how its design can improve both sensitivity and miniaturization. The work centers on the analysis and design of integrated circuits (ICs) for the analog front-end receiver, covering the signal chain from the transducer to digitization. Clinical applications and image reconstruction techniques fall outside the scope of this study.

The objective of this thesis is to leverage the *slow-time feedback* architecture initially introduced in [23], [25] and further developed in this work in order to improve:

- **Sensitivity**: mitigating low-sensitivity issues by means of the system detection limits, directly within the analog IC front-end through architectural enhancements compared to conventional architectures.
- **Efficiency**: lowering the data rate output through the optimized front-end architecture compared to conventional architectures.
- **Micro-beamforming**: expand the design to show feasibility with micro-beamforming operation as described in section 2.4.8.
- **Miniaturization**: reducing the overall area of the TCD system through architectural enhancements in the analog front-end IC.

Through these objectives, this thesis aims to demonstrate how analog front-end architecture design can overcome the sensitivity limitations of current TCD systems, improve their efficiency, and pave the way toward wearable devices.

Chapter 2 discusses the design of the TCD front-end receiver architecture. First, the project specifications are defined. Next, three possible system architectures are presented and compared, with the RF-sampling system using slow-time feedback selected as the preferred choice. Third, the chapter focuses on the system-level design of the chosen architecture and the reasoning behind the selection of each functional block. A detailed analysis is provided for the boxcar integrator and the micro-beamformer, followed by an examination of the slow-time delta modulator. Finally, the chapter presents the system-level results.

Chapter 3 describes the prototype implementation. It includes the integration of a previous design from the *Electronic Instrumentation Laboratory* for the receiver path. Furthermore, it focuses on the element-level design of the digital-to-analog converter (DAC) the buffer of the feedback path.

Chapter 4 reports the results of the project, including transient and spectrum simulations, overall power consumption, and a comparison with state-of-the-art designs.

Chapter 5 summarizes the thesis contributions, outlines the conclusions, and discusses future work. This includes remaining prototype implementation tasks and potential improvements for the system.

2

TCD Receiver Architecture

2.1. Specifications Derivation

In order to design the architecture of the TCD analog front-end receiver, it is important to first define the specifications it must meet.

Transducer

The operating frequency of the transducer is a critical parameter, influenced by the acoustic domain and the specific application. Higher frequencies provide better spatial resolution in 2-D imaging and improve the back-scattering coefficient of blood cells [28]. However, they also suffer from increased attenuation through tissue and the skull, which is a major constraint for transcranial Doppler (TCD) applications.

To balance these trade-offs, a commercial capacitive micro-machined ultrasound transducer (CMUT) array (CM5 from XIVER) was chosen [29], [30], [31], which operates at a relatively low frequency of 2.6 MHz. The CM5 consists of 64 transducer elements. A subset of eight-elements is utilized at this project, in order to simplify the architecture and demonstrate feasibility of the micro-beamformer feature which is discussed in section 2.4.8.

The transducer offers a fractional bandwidth of 93%, corresponding to an effective frequency range of approximately 1.39–3.81 MHz.

The target imaging depth for TCD applications is 5 cm. Considering the speed of sound in human tissue ($c \approx 1540\,\mathrm{m/s}$), the maximum pulse repetition frequency (PRF) is calcu-

lated as:

$$\mathrm{PRF}_{\max} = \frac{c}{2d} = \frac{1540}{2 \times 0.05} = 15.4\,\mathrm{kHz},$$

where d is the imaging depth. Based on the Nyquist criterion, the highest Doppler frequency that can be measured without aliasing is half of the Pulse Repetition Frequency (PRF), which is 7.7 kHz [32].

A CMUT is a silicon-based transducer device consisting of two plate-like electrodes. A bottom electrode attached on the silicon substrate and a top electrode formed by a thin, metalized membrane. The device is biased with a DC voltage and it is driven with an additional AC signal in order to generate ultrasonic waves [33]. In receive mode, when ultrasonic waves strike the membrane, it vibrates in response to the acoustic pressure, causing a change in the device's capacitance.

Figure 2.1 shows a simplified layout of a CMUT. A cavity is formed between the membrane (top electrode) and the silicon substrate (bottom electrode). An insulating layer is included between them to prevent electrical shorting in case of contact.

Figure 2.1: CMUT Layout

To accurately simulate the behavior of the front-end receiver circuit, an appropriate transducer model must be used. The Butterworth–Van Dyke (BVD) model is commonly employed to represent the electrical behavior of acoustic resonators, including CMUTs [34], [35].

Figure 2.2 illustrates the *Butterworth–Van Dyke (BVD) model*, which consists of two parallel branches. The first branch, known as the *motional branch*, models the mechanical behavior of the transducer and is represented by a series connection of R_m, L_m, and C_m [35]. The second branch represents the *static capacitance* C_e, which corresponds to the actual electrical capacitance between the two conductive plates of the transducer [35], [36].

This model can accurately captures how the transducer loads the input of the receiver and how it behaves as a small-signal source at the input of the low-noise amplifier (LNA). An additional source can be included in the mechanical branch to model the acoustic input as illustrated in figure 2.2. Finally, the thermal noise associated with R_m accounts for

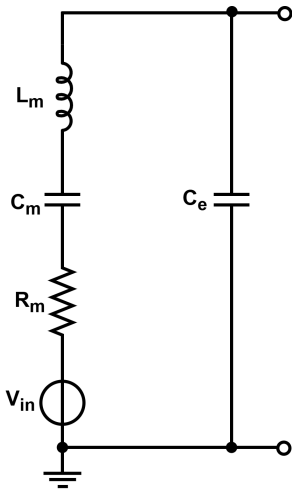


Figure 2.2: Van Dyke Model

the noise contribution of the transducer itself [35].

The impedance of the transducer can be written as:

$$Z(s) = \frac{L_m C_m s^2 + R_m C_m s + 1}{sC_e(LC_m s^2 + R_m C_m s + 1 + \frac{C_m}{C_e})} \tag{2.1}$$

Table 2.1 lists the parameters used in the transducer model.

Bias [V]	Ce [pF]	Cm [pF]	Lm [mH]	Rm [kOhm]
120	3.6	1.7	2.245	53

Table 2.1: Transducer Parameters

The current noise density can be calculated as follows:

$$I_n = \sqrt{\frac{4kT}{R_m}} = 0.56\,\text{pA}/\sqrt{\text{Hz}} \tag{2.2}$$

where $k = 1.38 \times 10^{-23}\,\text{J/K}$ is the Boltzmann constant, and $T = 300\,\text{K}$ is the nominal temperature.

The RMS noise current can be derived:

$$I_{\text{noise}} = 0.56\,\text{pA}/\sqrt{\text{Hz}} \times \sqrt{2.6 \times 10^6} \approx 0.9\,\text{nA}. \tag{2.3}$$

DOPPLER SNR

The Doppler signal-to-noise ratio (SNR) refers to the proportion of the blood-reflected signal relative to the system's inherent background noise. It is important to highlight that this measure does not include the impact of clutter. The target for this design is to achieve a Doppler SNR of 30 dB [17], [23].

DYNAMIC RANGE

The dynamic range can be defined as the ratio between the minimum detectable signal and the maximum detectable signal that the system can handle. Graph 2.3 illustrates the magnitude in dB of the system (output signal of transducer) at the y-axis and the target depth of the application at the x-axis (round-trip distance). Following the metrics are analyzed.

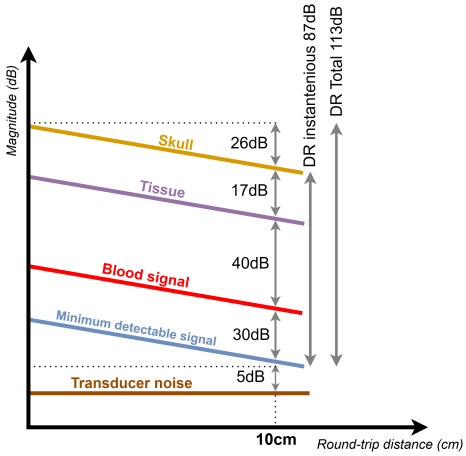


Figure 2.3: Dynamic range of receiver over round-trip distance in the human body

- **Transducer noise**
  The selected CMUT, together with the chosen input capacitor, has a current noise floor of 0.9 nA.
- **Minimum detectable signal**
  The minimum detectable signal at the distance of interest is approximately 5 dB higher than the transducer noise, to include the noise contribution of the LNA and the feedback path.
- **Blood signal**
  Blood signal is 30dB higher than the minimum detectable signal [17], [23], creating sufficient SNR for signal processing.

- **Tissue**
  Tissue echoes exceed blood echoes by about 40 dB [37].
- **Skull**
  Reflections from the skull are approximately 17 dB higher than tissue echoes [32], [38].
- **Round trip loss**
  With a target imaging depth of 5 cm and an attenuation coefficient of 1 dB/MHz/cm [39], the round-trip loss at 2.6 MHz is calculated as:

$$\text{Loss} = 2 \cdot \alpha \cdot f \cdot d = 2 \cdot (1\,\text{dB/MHz/cm}) \cdot (2.6\,\text{MHz}) \cdot (5\,\text{cm}) \approx 26\,\text{dB}.$$

Considering these factors, the dynamic range in any given moment referred as instantaneous DR is estimated at 87 dB [39], [40]. Since the system is capable of having depth control, the total dynamic range is 113dB.

AREA

Since the project employs a matrix transducer, aligning the ASIC dimensions with the transducer matrix would be advantageous, as it brings us closer to achieving compact and potentially wearable ultrasound systems.

The chosen CMUT (CM5) has a pitch of 365 μm [29]. Given the 4x2 elements matrix configuration, the resulting ASIC dimensions should be 1.46 mm × 0.73 mm.

TECHNOLOGY

Given the selection of a low-frequency transducer ($f_{\text{center}} = 2.6\,\text{MHz}$) and the benefit of leveraging existing designs from this group, the TSMC 180 nm BCD process was chosen for this design.

POWER

The goal of this design is to meet these specifications while minimizing power consumption, thereby moving a step closer to realizing wearable ultrasound devices.

TABLE OF DESIGN SPECIFICATIONS

Based on the aforementioned derived specification table 2.2 summarizes the specifications that the ASIC Receiver should meet.

Center frequency	f_c = 2.6MHz
Bandwidth of interest	1.39–3.81 MHz (93% BW/fc)
Area	1.46x0.73mm^2
Total DR	113dB
Instantaneous DR	87dB
Technology	TSMC 180nmBCD
Power	As low as possible
Transducer noise	0.9nArms
Input noise target	<1.6nArms

Table 2.2: Specifications of the ASIC Ultrasound Receiver

2.2. ULTRASOUND DOPPLER FRONT-END RECEIVER ARCHITECTURES

In this part, three PW Doppler front-end receiver architectures are explored in order to choose the most suitable one for this project.

2.2.1. MIXER BASED PW DOPPLER SYSTEM

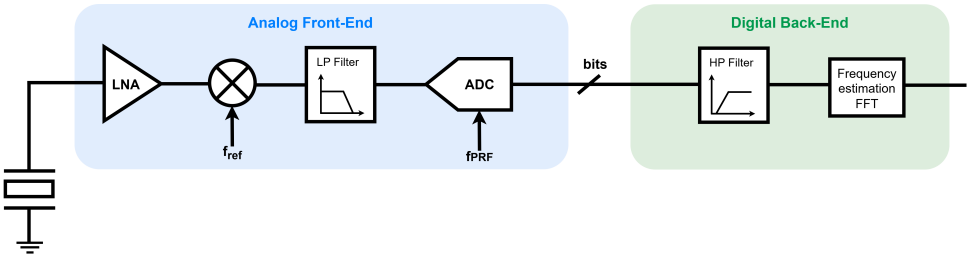


Figure 2.4: Mixer-based system

Figure 2.4 illustrates a conventional analog front-end, mixer-based PW Doppler receiver architecture[17], [27], [41], [42]. The LNA first amplifies the received signal to match the level of the reference signal. A mixer then combines the amplified signal with the reference signal, resulting in a Doppler component signal at the base-band and a high frequency component at double the carrier frequency effectively applying demodulation. Following the signal is passed through a low-pass filter to remove the high-frequency components. This step leaves only the Doppler and clutter components at base-band. Subsequently, an ADC is utilized sampling at the pulse repetition frequency (PRF) in order to implement the *slow-time sampling* operation and to digitize the signal. Finally, the data are forwarded to the back-end digital stage. The digital back-end applies a high-pass filter to suppress clutter components, followed by frequency estimation using the Fast Fourier Transform (FFT) to calculate the Doppler spectrum.

This type of design typically involve I/Q demodulation to preserve phase information. Furthermore, a mixer is required with a high dynamic range and capability of operating at low DC frequencies while maintaining linearity, which can be challenging to implement effectively [23].

2.2.2. RF-SAMPLING BASED PW DOPPLER SYSTEM

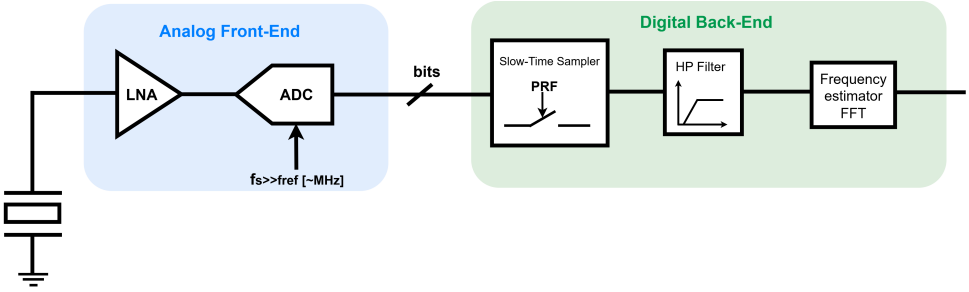


Figure 2.5: RF-sampling based system

Systems that sample the received signal directly at the carrier frequency are referred to as RF-sampling architectures [43], [44]. Figure 2.5 illustrates such a system. In this approach, an LNA amplifies the captured signal to match the dynamic range of the ADC. Subsequently the signal is passed to a high-speed ADC, operating at a sampling rate that is multiple of the ultrasound center frequency in the megahertz range.

The digitized data are then transferred to the digital back-end, where the PW Doppler signal processing is performed. As previously described, this involves sampling the signal at Pulse Repetition Frequency (PRF) between successive slow-time cycles. As a result the signal is demodulation based on the phase-shift principle. Subsequently, a high-pass filter is applied to remove clutter components, effectively isolating the Doppler frequency information, providing it to the Frequency estimator.

The main advantage of this architecture is its flexibility in digital back-end processing and compatibility with B-mode imaging for color flow applications. Consequently, it is widely adopted in many commercial Doppler ultrasound systems [43], [44].

The main disadvantage of this architecture is that it requires an LNA and ADC of high dynamic range which means that the front-end blocks needs low noise specification, usually paid in the price of increased power.

Furthermore, this architecture requires a digital back-end with higher demands on memory capacity and digital processing speed. Achieving a dynamic range of 87dB typically requires an ADC resolution exceeding 15 bits. For instance, a 15-bit ADC operating at a 10 MHz sampling rate generates a data stream of approximately 18.75 MB/s. The challenge becomes even more significant when using transducer arrays.

2.2.3. RF-SAMPLING WITH SLOW TIME FEEDBACK PW DOPPLER SYSTEM

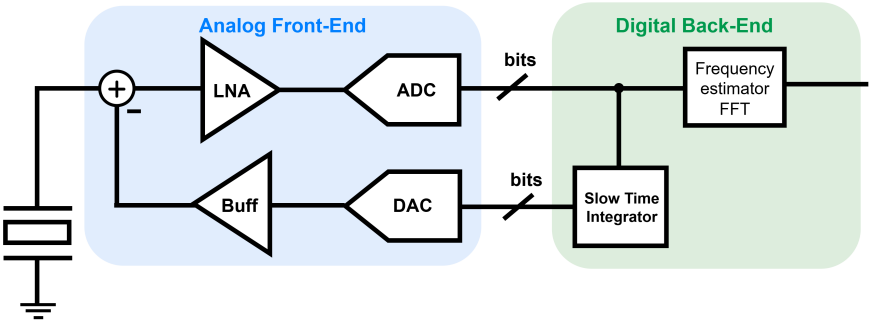


Figure 2.6: RF-sampling with Slow time integrator system

In [23], [25] an elegant approach is implemented of removing the clutter components in the analog domain utilizing a feedback loop and thus reducing the high dynamic range specifications of the front-end components. In these cases the digital domain accumulates the static clutter component and feeds them back to the analog front-end enabling clutter cancellation. The loop acts as a low-pass filter tracking slow phase changes. It is worth mentioning that a similar approach was previously presented in [45], [46]. However, in that case it was neither designed for TCD units with high dynamic range requirements nor implemented as an integrated circuit.

Figure 2.6 depicts the architecture implemented in [23]. In this case the front-end system works on the RF-sampling frequency. The LNA amplifies the signal to meet the dynamic range (DR) of the ADC. The ADC samples the signal at least a twice the frequency of the ultrasound frequency to meet the Nyquist criteria. Following, the output of the ADC is fed to a slow-time integrator which captures the static components in the digital domain after several transmit/receive cycles. Subsequently, the static component passes through a DAC to convert the digital signal to analog. Finally, the copied static signal is subtracted from the input signal of the transducer in the current domain effectively canceling the clutter-static components.

A simplified illustration of the slow-time delta modulator is shown in Figure 2.7. The modulator accumulates the input signal with a coefficient $\alpha < 1$, which allows it to gradually build up a copy of the signal over time if the same input is repeatedly applied. Since the system operates at the pulse repetition frequency (PRF), and static components such as skull reflections remain constant across cycles, the delta modulator effectively reconstructs the clutter signal. In contrast, the blood signal introduces a phase shift between successive cycles due to motion. As a result, the Doppler signal drifts between cycles and cannot be accumulated by the delta modulator. A more detailed discussion of this behavior is provided in Section 2.4.7.

At this stage, the signal remains at the carrier frequency, but the clutter components have been effectively removed. The digital back-end can now perform further signal processing, such as demodulation, a high-pass filtering and frequency estimation to extract the

desired Doppler information.

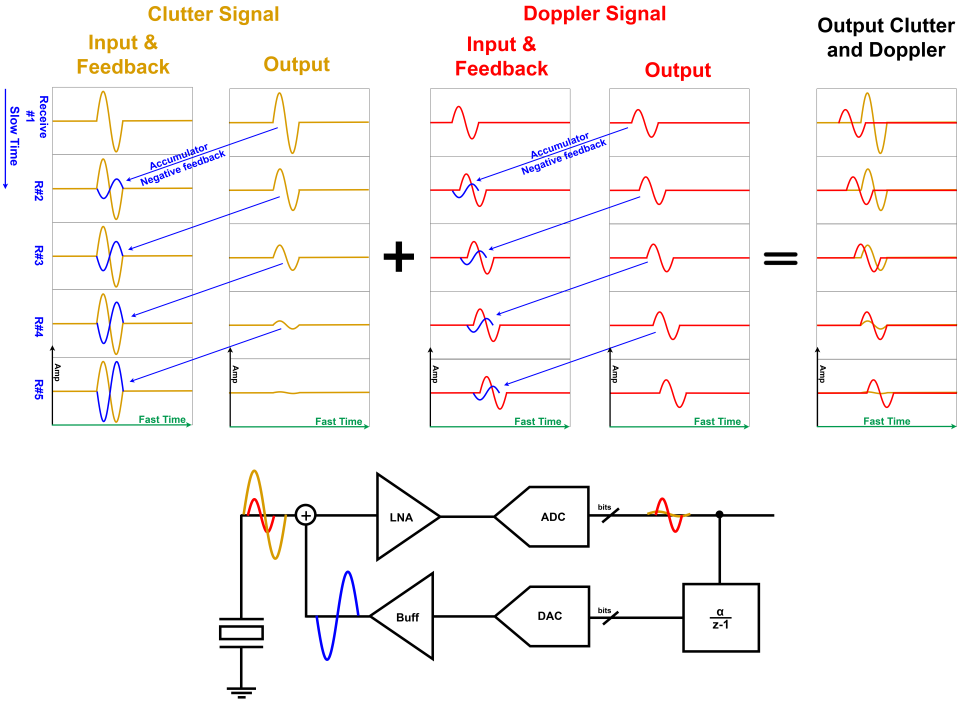


Figure 2.7: Time domain diagram of slow-time modulator and signal flow diagram of slow-time architecture.

Advantages and Drawbacks

The result is that the LNA and ADC do not need high dynamic range as in the previous architectures since the high amplitude clutter components is already removed through the feedback loop. As a result the power consumption of this system is also lower.

Furthermore the reduced dynamic range of the ADC means that the output streamed data are lower in size compered to the simple RF-sampled architecture.

The main drawback of this architecture is the requirement for additional memory to implement the delta modulator, as well as the addition of extra components such as the DAC and the DAC buffer. These components can introduce noise into the system and must therefore be carefully designed.

Given its substantial advantages over previous architectures, this design is adopted in the thesis, which further explores and evaluates its potential.

2.3. SYSTEM DESIGN APPROACH AND OVERVIEW

The design is initially considered at a high level, while the transistor-level implementation will be discussed in detail in the following chapter. Each block is first modeled as an ideal component to evaluate the overall system behavior.

At this stage, the focus is on the selection of functional blocks, the reasoning behind their selection, as well as their advantages and limitations. Based on the specifications from Section 2.1 and the functional requirements of each block, appropriate design choices are made.

Furthermore, the system is analyzed using a signal flow diagram in section 2.4.7, which provides analysis of the closed loop configuration of the system, affecting the requirements of the system and thus of the individual blocks.

The goal is to develop a MATLAB script that simulates the system behavior and overall performance of the system. This will be followed by Cadence simulations to further verify the results.

The architecture block diagram of the Pulsed Wave Doppler receiver with Slow-Time feedback is illustrated in figure 2.8.

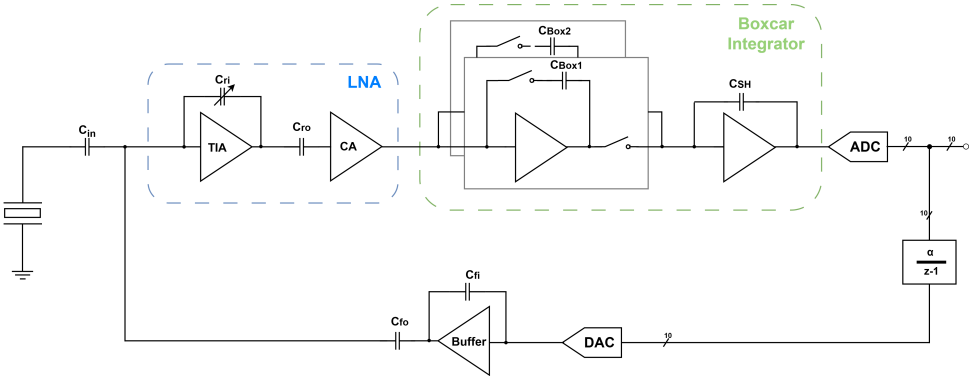


Figure 2.8: Block diagram of receiver

The transducer receives the ultrasound pulse echoes from the human body and converts the information to voltage signal. A capacitor differentiates this signal, converting the input voltage into a current. Following is the cancellation node in the current domain where the feedback signal and the input signal are summed.

The first block is a low-noise amplifier (LNA). It consists of a TIA with capacitive feedback which integrates the input current and converts it into a voltage. An output capacitor then differentiates this voltage back into current. This current is fed into a current amplifier, which presents a high output impedance to effectively drive the subsequent boxcar integrator.

The boxcar integrator performs a sample-and-hold operation by integrating the incoming current and converting it to a voltage. Additionally, it supports micro-beamforming functionality, which can be enabled when additional transducer elements are integrated into the system.

The output voltage of the boxcar integrator is digitized by an ADC and passed to the backend digital processing unit for further signal processing and frequency estimation. At this stage, a delta modulator accumulates the digitized signal over multiple slow-time (T/R) cycles, effectively capturing the clutter signal. This accumulated signal is then used as the feedback signal in the next cycles.

A DAC converts the accumulated digital signal back into an analog current using a zero-order hold operation. Finally, a buffer attenuates the DAC output to match the amplitude level of the original input signal before feeding it back to the cancellation node. At the cancellation node, the clutter component in the input signal is effectively canceled by the feedback clutter signal, leaving only the Doppler information for further processing.

2.4. FUNCTIONAL BLOCKS ANALYSIS AND DESIGN

2.4.1. INPUT COUPLING AND CANCELLATION NODE

In the pitched-matched configuration the CMUTs are monolithically integrated on top of the ASIC, allowing the captured signals to be delivered directly in the current domain. This enables a straightforward and effective implementation of a cancellation node at the transducer output, where the current from the transducer and the feedback current are summed and cancel each other.

2.4.2. LOW NOISE AMPLIFIER

After the cancellation node, the difference between the input signal and the feedback signal is received by the LNA. The purpose of the LNA is to read-out this weak signal and amplify it to the dynamic range of the following blocks without adding noise or distortion.

Based on this specification in this design a closed-loop TIA with capacitive feedback is implemented. It integrates the input current to generate an output voltage. This voltage is then differentiated by the output capacitor to produce a current output which will be passed to the current amplifier. As shown on the schematic 2.8, the gain of the amplifier is defined as:

$$A_{\mathrm{LNA}} = \frac{C_{\mathrm{ro}}}{C_{\mathrm{ri}}} \tag{2.4}$$

C_{ri} is chosen to meet the output swing of 0.9 V, while C_{ro} is chosen to minimize the input-

referred current noise. The TIA provides a low input impedance and low-noise to sense the transducer's signal current. Subsequently, the current amplifier (CA) provides the high output impedance to drive the boxcar-integrator.

Startup phase
The LNA includes a variable feedback capacitor, C_{ri}, to support the startup phase. During the initial slow-time cycles, the feedback system has not yet fully captured the clutter signal. Since the gain of the LNA is determined by the Doppler signal, and the clutter signal can be up to 57 dB stronger, directly amplifying the input during this period would lead to signal saturation. To prevent this, a startup phase is implemented in which the gain begins at a lower value and is gradually increased. Once the feedback system has sufficiently captured and suppressed the clutter signal, the gain is settled to the target value.

2.4.3. BOXCAR INTEGRATOR

The boxcar integrator plays multiple roles: it converts the input current to a sampled voltage, acts as an anti-aliasing filter, and enables micro-beamforming through delay-and-sum functionality, as will be explained in Section 2.4.8.

Figure 2.9 a) illustrates the boxcar integrator circuit together with its timing diagram [29], [47]. During each sampling window, controlled by the write switches W_i, the input current charges the boxcar capacitor, effectively integrating the signal over time. At the end of the sampling interval, the capacitor is disconnected from the input and connected to the sample-and-hold capacitor C_{SH} through the N_i switches, effectively transferring the stored charge. This provides a readout voltage to the ADC until the Q switch resets the circuit for the next sample. While one capacitor is charging in write mode, the other is being read out, resulting in a ping-pong operation that ensures a seamless stream of samples.

Anti-aliasing
An advantageous characteristic of the boxcar integrator is its inherent anti-aliasing behavior. Equation:

$$V_{out} = \frac{1}{C}\int_0^{Ts} I_{\text{in}}(t)\,dt \tag{2.5}$$

can be expressed as the convolution of the input signal with a rectangular window whose height is *1/C* and width is *Ts* as depicted in figure 2.9 b). Figure The 2.9 c) illustrates the same in the frequency domain were the normalized magnitude response of the boxcar integrator can be expressed from the equation [48], [49], [50]:

$$|H(f)| = \frac{1}{Cf_s}\left|sinc(\frac{f}{fs})\right| \tag{2.6}$$

Figure 2.9 e) illustrates the sinc response which exhibits a first-order low-pass characteristic with nulls at integer multiples of the sampling frequency f_{s}, a main lobe at DC

with a gain of $\frac{1}{f_s \cdot C}$, and a set of side lobes rolling off at 20 dB/dec [50]. This characteristic creates an effective anti-aliasing filter that suppresses unwanted frequency components above the Nyquist frequency.

Furthermore, it can effectively suppress noise caused by clock leakage, which introduces tones at multiples of f_s. Additionally, it helps to attenuate out-of-band noise coming from the LNA [48].

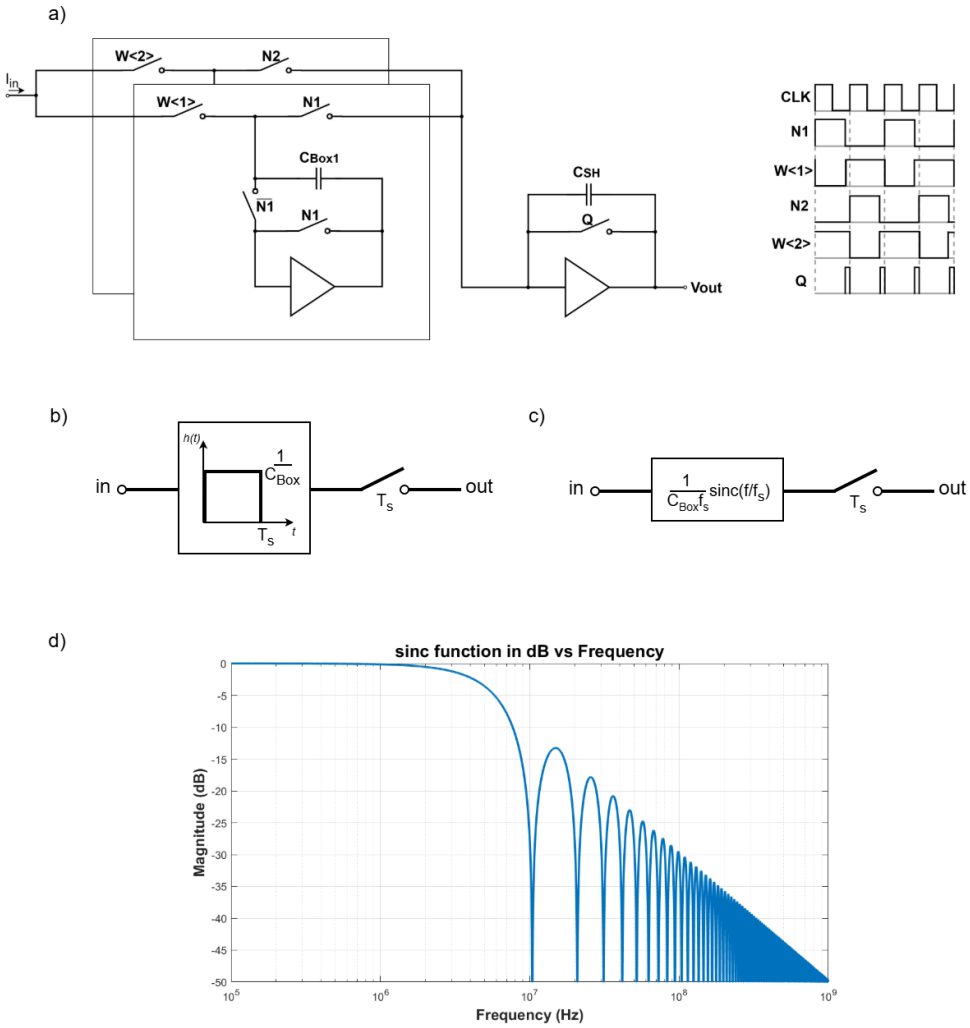


Figure 2.9: Boxcar Integrator schematic diagram along with timing diagram [29], [47]. b) Windowed integration sampler time domain c) Windowed integration sampler frequency domain d) sinc function frequency response.

2.4.4. ANALOG TO DIGITAL CONVERTER

ADC Resolution
The resolution of the ADC depends on system's dynamic range requirements. Since the system removes the clutter signal the ADC DR requirements are relaxed needing only 30dB which relates to the Doppler SNR.

The quantization noise should be at least 10 dB smaller than the thermal noise to ensure that the SNR degradation remains below 0.5 dB.

The ADC dynamic range can be calculated as:

$$DR_{\text{ADC}} = DR_{\text{instantaneous}} - DR_{\text{clutter}} + 10\,\text{dB} = 92 - 57 + 10 = 45\,\text{dB}. \tag{2.7}$$

The number of bits required is given by:

$$N = \log_2\left(10^{\frac{DR_{\text{ADC}}}{20}}\right) \approx 8\,\text{bits}. \tag{2.8}$$

In this design the ADC is set with a resolution of 10bits, considering the reuse of an existing ADC design within the EI group [47].

2.4.5. DIGITAL TO ANALOG CONVERTER

The role of the DAC is to convert the digital output of the slow-time integrator into a current signal.

DAC resolution
The feedback signal essentially replicates the clutter component but includes additional quantization noise introduced by the DAC. To ensure that this quantization noise does not limit the receiver's dynamic range, its level must remain below that of the Doppler signal.

Therefore, the dynamic range of the DAC should satisfy the condition:

$$\text{DR}_{\text{DAC}} > \text{DR}_{\text{clutter}} \implies \text{DR}_{\text{DAC}} > 57\ \text{dB}. \tag{2.9}$$

The required DAC resolution bits can be estimated as:

$$n_{\text{DAC}} > \log_2\left(10^{\frac{\text{DR}_{\text{DAC}}}{20}}\right), \tag{2.10}$$

which for $\text{DR}_{\text{DAC}} = 57$ dB gives:

$$n_{\text{DAC}} \approx 10\ \text{bits}. \tag{2.11}$$

2.4.6. DAC BUFFER

The DAC Buffer plays multipurpose role. Firstly, by providing gain to the feedback path it provides flexibility into scaling the DAC for noise specifications. Hence, it scales the mA-scale DAC current into the μA-scale of the transducer signal in order to create effective cancellation. As shown on the schematic 2.8, the gain of the amplifier is defined as:

$$A_{\text{Buff}} = \frac{C_{\text{fo}}}{C_{\text{fi}}} \tag{2.12}$$

Secondly, it buffers the resistive output of the DAC from loading the LNA and decreasing its gain.

2.4.7. SLOW-TIME DELTA MODULATOR

Delta modulator
The basic idea of a delta modulator is illustrated in figure 2.10 a). The output is based on the difference between the current input sample and a predicted value. The predicted value can be obtained by integrating the previously quantized outputs.

From its linear z-domain the transfer function can be derived:

$$y = x(1 - z^{-1}) + q(1 - z^{-1}) \tag{2.13}$$

as illustrated in figure 2.10 b), where q is the quantization error.

This scheme creates a high pass characteristic both at the signal transfer function (STF) and the noise transfer function (NTF), preventing DC or low-frequency components from entering the quantizer. The magnitude of the signal transfer function is depicted in figure 2.10 c).

Slow-time Delta Modulator
In the slow-time domain, the signal-flow diagram of an individual delta modulator can be represented as shown in Figure 2.10 d). Here, z represents slow-time sampling, in contrast to the delta modulator shown in Figure 2.10 b). Within the bandwidth of interest, the blocks in both the receiver and feedback paths can be approximated by constant gains, denoted as A_{rx} and A_{fb}, respectively. The integrator in the loop is a first-order integrator characterized by a gain factor α. A first-order implementation is considered sufficient for clutter suppression, as the dominant components such as skull reflections and low-frequency motion primarily occur near DC [23].

The signal transfer function can be derived as:

$$STF_{x\to y} = A_{rx}\frac{1 - z^{-1}}{1 - (1 - \alpha A_{rx}A_{fb})z^{-1}} \tag{2.14}$$

The magnitude diagram of the STF is depicted in Fig. 2.10 e). It exhibits a high-pass

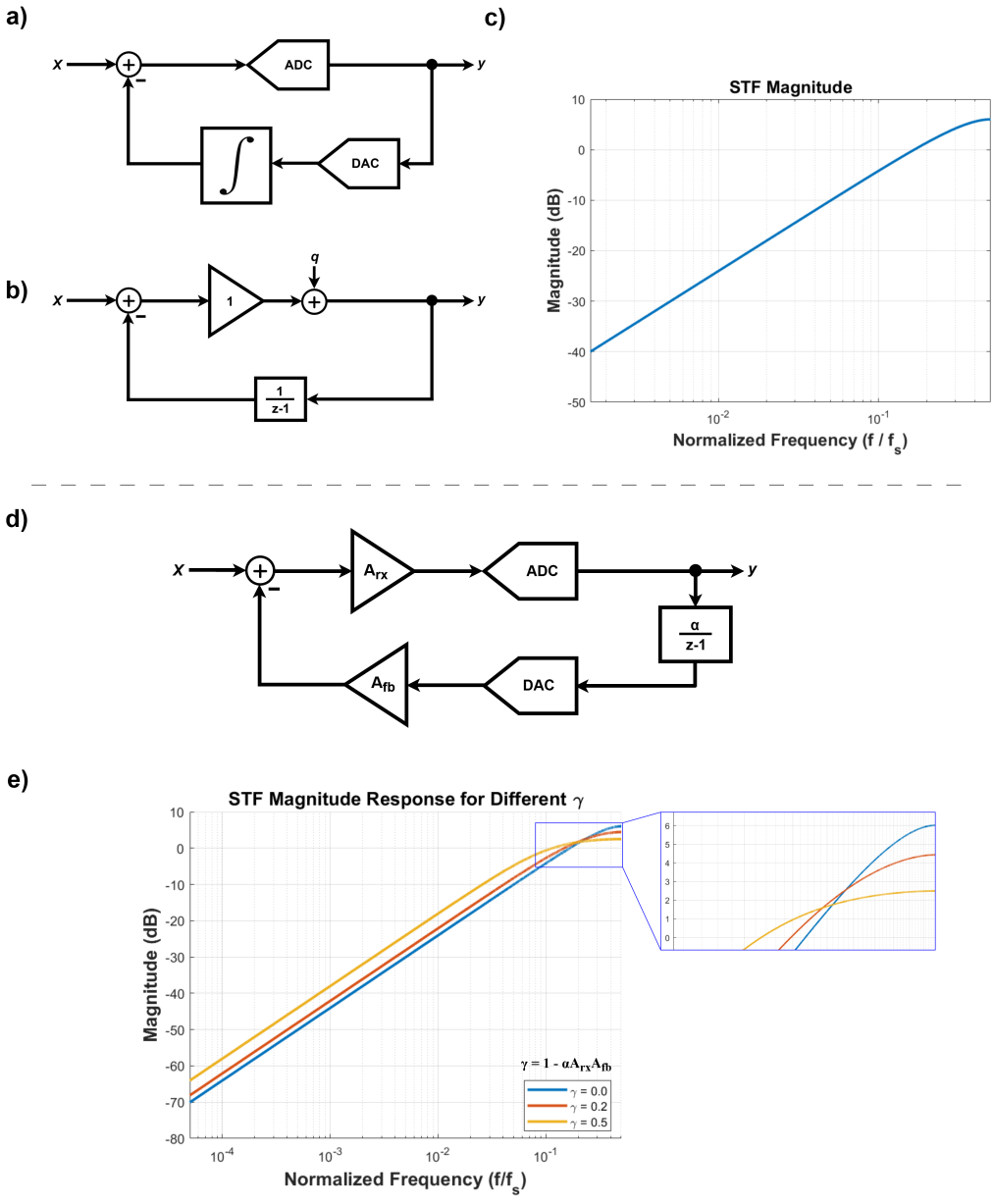


Figure 2.10: a) A Delta Modulator used as an ADC. b) Its linear z-domain model. c) Its signal transfer function (STF). d) Signal flow diagram of slow-time system e) Magnitude STF of slow-time system

characteristic with a pass-band characteristic near the f_{prf}, which can be controlled by adjusting the digital coefficient a.

Slow-Time Integrator

In the slow-time architecture the ADC samples at the fast-time domain. For each fast-time sample an individual accumulator integrates the sample over slow-time cycles. While each individual integrator functions in the slow-time domain, their combined operation forms a fast-time processing scheme, as illustrated in Figure 2.11. Since in the slow-time domain the clutter signals are at DC and base-band frequencies, whereas Doppler signals are in higher frequencies, the signal transfer function (STF) of the delta modulator effectively attenuates the former while preserving the latter.

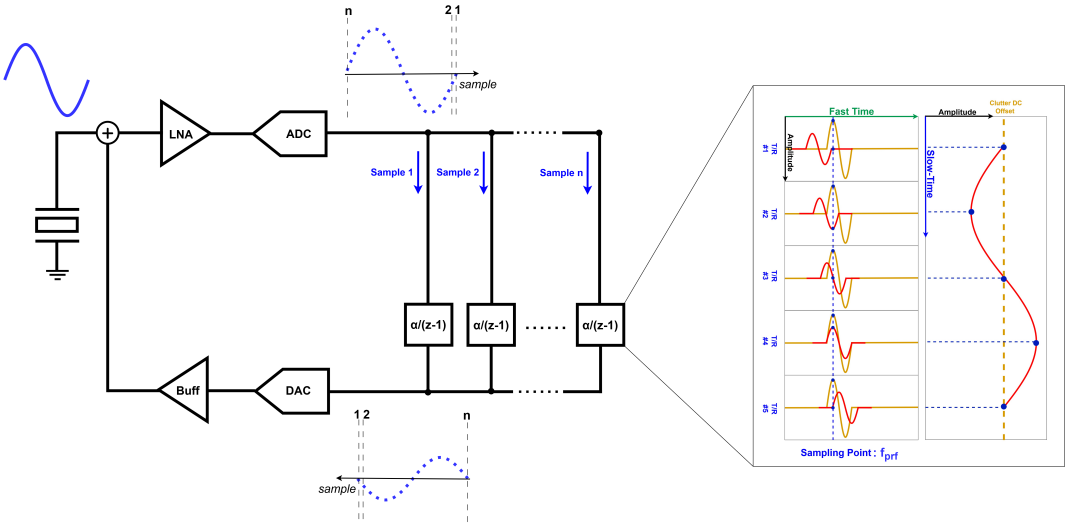


Figure 2.11: Slow Time Integrator - Delta Modulator

Stability Criteria

Since the system operates in a feedback configuration, analyzing its stability is essential. As with conventional delta modulators, instability can arise due to the finite loop bandwidth, which introduces excess delay in the feedback path. A narrower bandwidth increases the phase difference between the input and feedback signals. If this phase error becomes large enough, it may begin to reinforce itself over successive slow-time cycles, eventually causing the system to oscillate. A comprehensive stability analysis of this behavior is presented in [23].

Figure 2.12 a) shows the slow-time signal diagram, where H_{rx} and H_{fb} represent the transfer functions of the receiver and feedback paths, respectively, including the effects of sampling and zero-order hold (ZOH) operations. As mentioned in Section 2.4.3, the boxcar integrator introduces a sinc-shaped frequency response. In addition, the ZOH function of the DAC also results in a sinc response. A equivalent diagram with the magnitude operations is depicted in Figure 2.12 a). As analyzed in [23], this structure can be expanded into a fast-time sequence that passes through a chain of loop transfer functions, as illustrated in Figure 2.12 c). Consequently, system stability depends on whether

this overall loop transfer function remains bounded or diverges through the equation 2.15.

$$\lim_{n\to\infty} \left|(1-\alpha H_{fb}(s)H_{rx}(s))^n\right| < 1 \tag{2.15}$$

Hence, the stability criteria can be established as follows:

$$|1-\alpha H_{fb}(s)H_{rx}(s)| < 1 \tag{2.16}$$

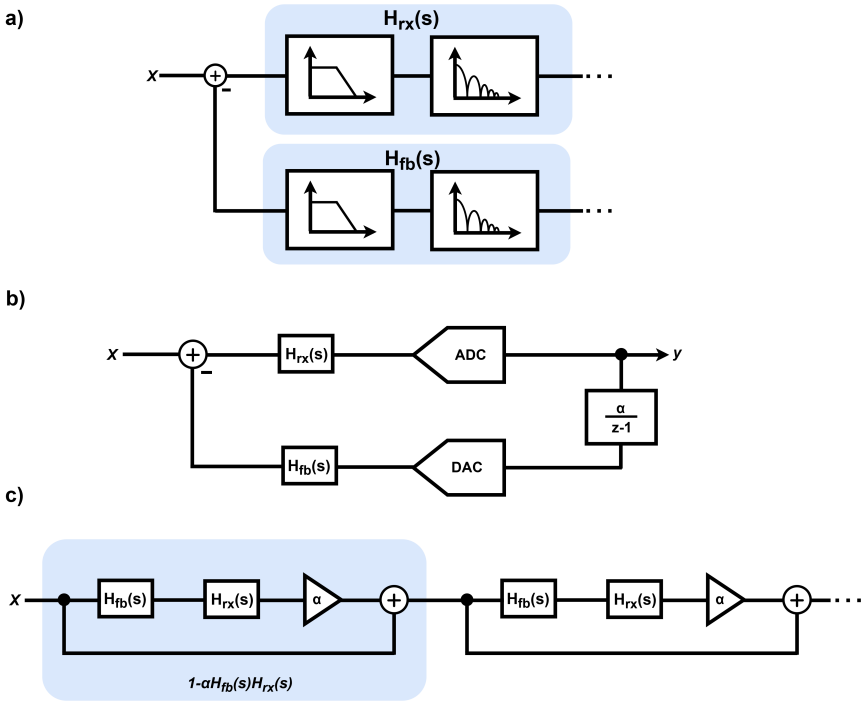


Figure 2.12: a) Equivalent model of transfer function of the receive path and feedback path. b) Signal flow diagram of slow-time system. c) Equivalent model for stability analysis.

Stability Design

By keeping in mind the aforementioned stability criteria, several design options can be implemented to keep the system stable. First, by keeping high bandwidth in the blocks the delay of the over all loop can be minimized, which can help stabilize the system. Secondly, the sampling frequency can be reduced which reduces the amplitude of the output of the boxcar integrator however this means that the dynamic range of the previous blocks should be increased. In this design a modest sampling rate is chosen of $T_s = 96ns$. Finally, the gain factor a can be reduced however the STF corner frequency comes closer to DC, which may reduce system responsiveness to the desired Doppler signals.

2.4.8. MICRO-BEAMFORMER

Delay-and-sum beamforming is the most common receive beamforming technique. As illustrated in figure 2.13 a), echoes from a focal point arrive at different times across the array elements due to different propagation distances. By applying appropriate time delays to each channel and summing the resulting signals, the contributions from the desired focal point add coherently, amplifying the signal, while off-focus signals remain incoherent and are thus not amplified as much or attenuated. This can be performed digitally using high-speed processors after element-level digitization [47].

Micro-beamforming performs the delay-and-sum (DAS) operation in the analog domain within sub-array groups, as illustrated in figure 2.13 b). Additional beamforming can then be done digitally off-chip. By dividing the transducer array into sub-arrays of N elements, the overall channel count is reduced by a factor of N, enabling a pitch-matched layout at the sub-array level. This also significantly reduces the complexity of signal routing, since fewer channels need to be processed and routed off-chip. However, conventional micro-beamformer implementations use per-element capacitive memory to realize the delay, which results in significant area consumption.

An elegant way of implementing the micro-beamformer is described in [48], where summation is applied prior to delay, using boxcar integration in the current domain. This reduces the need for per-element memory, and dense signal routing, offering a more compact implementation compared to conventional micro-beamforming techniques. Figure 2.13 c) illustrates this scheme. In this configuration the switches W_{ii} can be programmed to adjust the delay while N_1 to N_k work at a fixed time.

Slow-time system with micro-beamforming
Since the system 2.8 already employs a boxcar integrator, it can be easily extended to implement micro-beamforming for four transducer elements by appropriately programming the integrator's switches. Figure 2.16 a) illustrates a schematic of the architecture design for four transducer elements.

For each transducer, the structure of the slow-time architecture remains as previously described, with the distinction that the boxcar integrator is now also connected to the other subsystems through the programmable switches $Wi < i >$. These switches are configured to operate in a micro-beamformer fashion as shown in the time diagram 2.16 b), implementing the Sum and Delay operation.

In addition, since the signals received at each transducer element arrive with different time delays, it is important for the feedback signals to be synchronized. This can be achieved by applying an opposite delay at the slow-time integrator to compensate for the delays introduced by the micro-beamforming function as shown in figure 2.16 a).

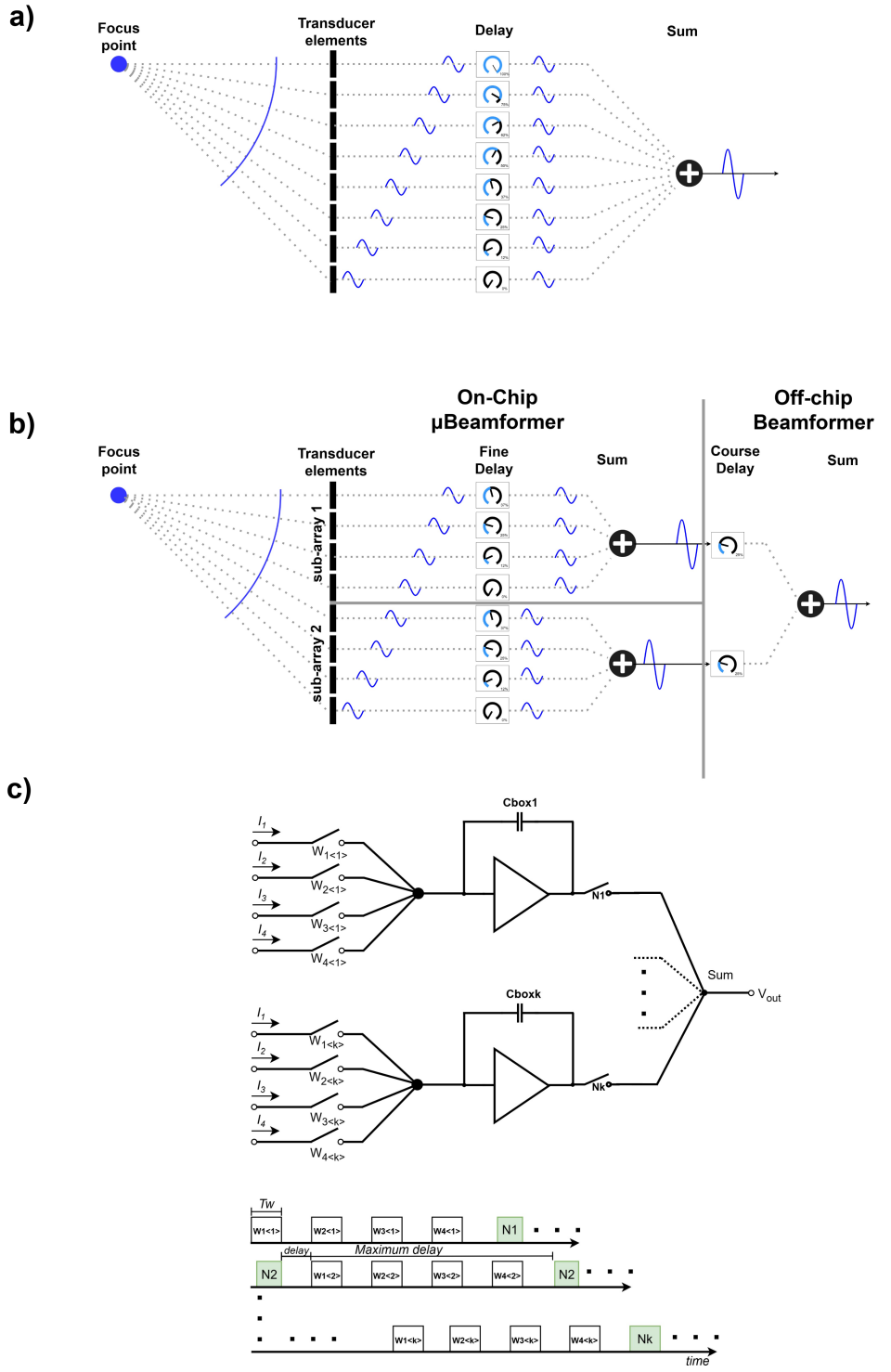


Figure 2.13: a) Beamforming with delay-and-sum (DAS). b) Micro-beamforming with two-step DAS c) Boxcar integrator based micro-beamformer schematic and time diagram. Sum and Delay scheme.

2.5. SIMULATION RESULTS

2.5.1. TRANSIENT AND SPECTRUM RESULTS

In order to evaluate the system a sinusoidal signal of continuous wave is inserted to the system which contains a clutter signal of $2.6MHz$ and a Doppler signal of $2.4MHz$ 46dB lower in amplitude. The signal is received for ten slow-time cycles. The Doppler shift frequency is exaggerated to ensure clear separation of the tones in the spectrum. In addition, the Doppler frequency exhibits phase variations in the slow-time domain. Finally, noise is added to represent the input referred noise of the system and of the transducer.

Figure 2.14 illustrates the fast-time spectrum. Figure 2.14 a) shows the input signal, where the red curve represents the clutter signal and the blue curve corresponds to the Doppler signal. Figure 2.14 b) presents the output spectrum obtained from the ADC.The clutter SNR and the Doppler SNR are defined as the ratio of the corresponding signal power to the noise background. It can be observed that the clutter signal is completely canceled transforming into quantization noise with clutter SNR = -12.25dB. In addition, the Doppler signal is 25dB higher than the noise with Doppler SNR = 8.75dB.

Figure 2.15 illustrates the transient response of the system for three different input cases. In the first simulation, only the clutter signal was applied, consisting of 6.5 cycles of a sine wave at 2.6 MHz with an amplitude of 13μA. In the second simulation, only the Doppler signal was applied, consisting of six cycles of a sine wave at 2.4 MHz with an amplitude of 0.65μA. In the third simulation, the clutter and Doppler components were superimposed to form a combined input pulse, resulting in a pulse of 2.5 μs. The response is shown over eight slow-time cycles. To clearly demonstrate the system's performance, the dynamic range between the Doppler and clutter signals has been reduced, and the frequency separation of the Doppler components has been exaggerated. It can be seen that by the last cycle, the clutter signal has been completely suppressed, leaving only the Doppler component.

At this stage, the signal remains at the carrier frequency, but the clutter components have been effectively removed. The digital back-end can now perform further signal processing to improve the SNR. This can be done such as demodulation, a high-pass filtering and frequency estimation to extract the desired Doppler information.

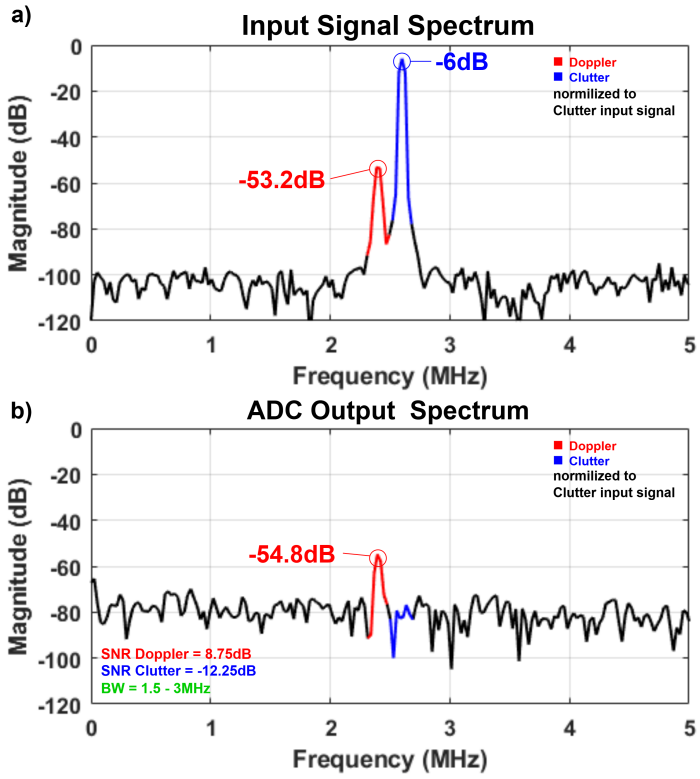


Figure 2.14: Cadence ideal model. Spectrum of a) Input signal b) ADC output at the first slow-time cycle c) ADC output at the last slow-time cycle

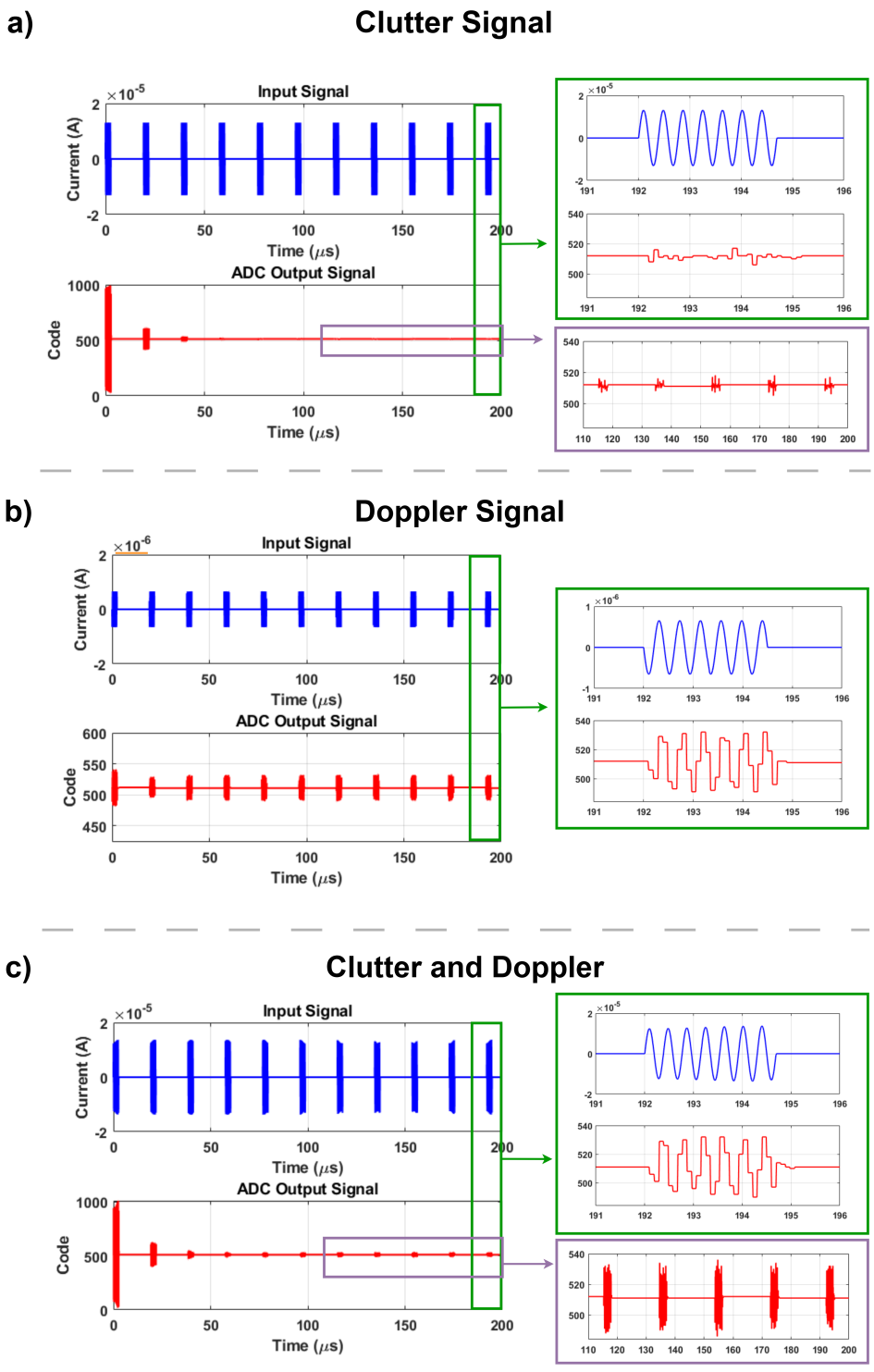


Figure 2.15: Pulsed Wave Doppler transient simulation results. a) Clutter signal only, b) Doppler signal only, and c) clutter and Doppler signal superimposed.

2.5.2. MICRO-BEAMFORMER RESULTS

The μBF directivity was evaluated by emulating acoustic waves arriving from angles between 0° and 50°. For each chosen arrival angle, the corresponding time shift between the transducer input signals was calculated, based on an assumed ultrasound propagation speed of 1540 m/s. Each input signal consisted of a 2.6 MHz clutter component and a 2.4 MHz Doppler component, superimposed. The μBF was configured to look forward at 0°. Figure 2.16 c) shows the configuration.

Figure 2.16 d) illustrates the experimental results for arrival angles up to 50°, mirrored around 0° to show the overall angular response. The results demonstrate that the system successfully forms a μBF, effectively suppressing signals arriving from directions other than the steered angle. The presented results correspond to the case where the clutter and Doppler components originate from the same direction.

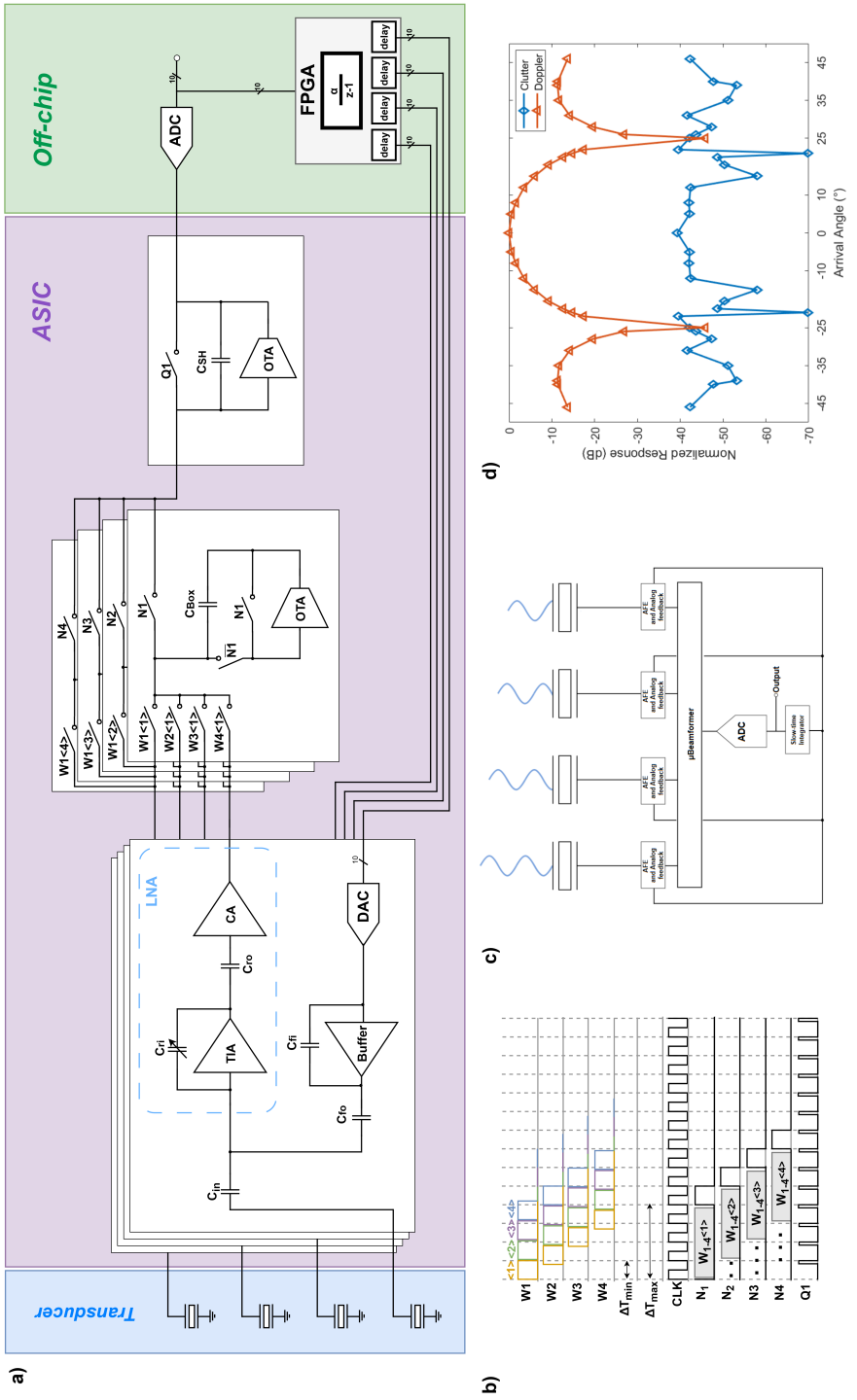


Figure 2.16: a) A four-transducer micro-beamformer slow-time architecture system b) Time diagram c) Directivity measurement with acoustic waves arriving at different angles by means of time-shifted sinusoidal signals. d) Normalized measured Clutter and Doppler signal after ten slow-time cycles as a function of arrival angles

3

PROTOTYPE IMPLEMENTATION - CIRCUIT DESIGN

In this chapter, the system design progresses toward the transistor level in order to enable the implementation of a prototype. To evaluate the overall feasibility, the front-end ultrasound receiver from a previous project in the *Electronic Instrumentation Laboratory*, [29], [47], is integrated into the system. For simulation purposes the analog-to-digital converter (ADC) is modeled in Verilog-A, although in a fabricated implementation it would be realized as an external chip. Similarly, the slow-time integrator is implemented in Verilog-A, while in hardware it would be realized on an FPGA. For the prototype, the concept is to integrate the receiver front-end with the design of the DAC and DAC buffer, both of which will be implemented at the transistor level in this chapter.

3.1. RECEIVER FRONT-END INTEGRATION

The integration of the front-end [29], [47] receiver with the Slow Time system is illustrated in Figure 3.1. The architecture employs eight transducer elements, divided into two identical sub-arrays of four elements each, enabling the implementation of the micro-beamformer operation. Every transducer element is connected to a cancellation node, which also receives the feedback signal used for clutter suppression. The output of each cancellation node is subsequently fed into the Low Noise Amplifier (LNA).

The Low Noise Amplifier (LNA) operates as a variable gain amplifier (VGA) to implement time-gain compensation (TGC). It consists of two stages: a transimpedance amplifier (TIA) with capacitive feedback, and a current amplifier (CA). The TIA output is capacitively coupled to the CA input, while the CA provides a high-impedance output in order to drive the boxcar integrator with the amplified received signal. The gain of the ana-

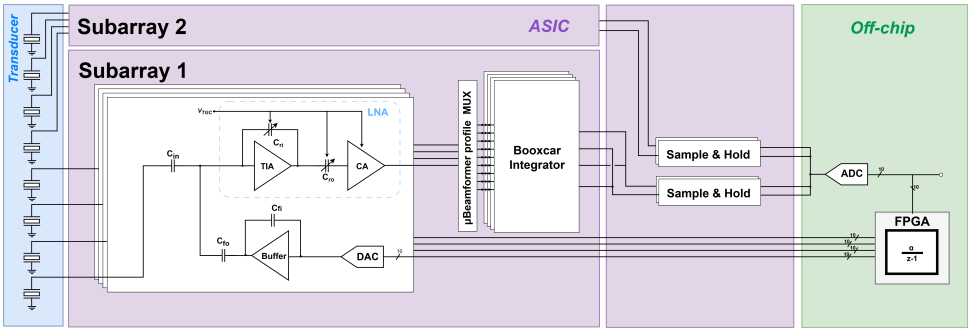


Figure 3.1: Integration of front-end ASIC from [29] with slow-time feedback.

log front-end (AFE) can be continuously adjusted across a 36 dB range via an external control voltage V_{TGC}, enabling the TGC operation.

The current output of the current amplifier is passed to four active boxcar integrators through programmable switches enabling delay control. Each two integrators operating in ping-pong fashion, are connected to a sample and hold (S/H) stage, effectively transferring the charge at a fixed timing. This scheme performs the sum-and-delay operation, thereby realizing the micro-beamforming functionality. Finally, the S/H blocks can realize time-division MUX (TDM) driving one output instead of two. A more comprehensive analysis can be found in [29], [47].

Following, the ADC samples the signal and the output is transferred to the slow-time integrator, which accumulates the clutter signal. Subsequently, the signal is passed to the DAC, where it is converted into an analog current. The DAC buffer then adjusts the signal level to match that of the input signal.

3.2. FEEDBACK NETWORK SIZING

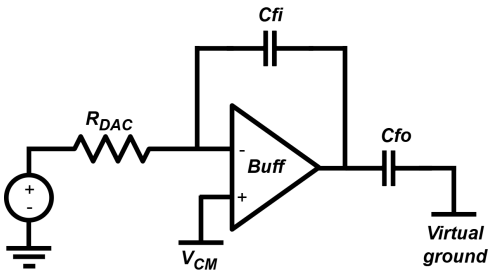


Figure 3.2: Feedback network

Before proceeding to the transistor-level design of the DAC and DAC Buffer, the required passive components are first determined. Figure 3.2 shows an equivalent representation

of the DAC as a voltage source in series with its total resistance, along with the DAC Buffer, the feedback capacitor, and the output capacitor connected to the LNA's virtual ground.

In this design step it should be taken into account the the DAC and DAC Buffer should not contribute more noise that the transducer noise in order to not increase the noise of the feedforward path of the signal.

Output Swing
In order to provide the highest possible SNR the amplifiers output voltage swing should be as close to the supply rails. In order to ensure proper operation of the output transistors a V_{ov} of 100 mV is allocated (discussed also in section 3.4). Therefore, the DAC Buffer is assumed to have an output voltage swing of:

$$V_{\text{Buffout,max}} = 1.6\,\text{V}$$

DAC Buffer Output Current
The DAC Buffer output current amplitude should match the maximum current provided by the transducer. Hence:

$$I_{\text{Buff,out,max}} = I_{\text{transducer,out,max}} = 13\,\mu\text{A}$$

Output Capacitance
From the transfer function of the DAC and DAC Buffer, the following relation can be derived:

$$\frac{C_{\text{fo}}}{C_{\text{fi}}} = \frac{I_{\text{Buff,out,max}}}{I_{\text{DAC,out,max}}} \quad \Rightarrow \quad C_{\text{fi}} \cdot R_{\text{DAC}} = \frac{V_{\text{DAC,max}} \cdot C_{\text{fo}}}{I_{\text{Buff,out,max}}} = const. \tag{3.1}$$

Power and Area vs. Noise Trade-off
This relation highlights a design trade-off between power consumption, output-referred noise and capacitor area. Reducing R_{DAC} increases the thermal current noise density of the DAC, which would normally degrade noise performance. However, because the output current must remain fixed at 13 μA, the feedback capacitor C_{fi} must be increased proportionally such that $R_{\text{DAC}} \cdot C_{fi}$ = constant. The larger capacitor attenuates the DAC's noise contribution more strongly, so that the overall output-referred noise actually decreases with smaller R_{DAC}. The penalty of this approach is higher power consumption due to the larger DAC signal swing, and increased silicon area from the larger C_{fi}.

Therefore, the following component values are chosen:

$$C_{\text{fo}} = 1\,\text{pF}, \quad R_{\text{DAC}} = 2\,\text{k}\Omega, \quad C_{\text{fi}} = 34.2\,\text{pF}$$

which create an output-referred current noise density of 0.15 nA_{rms}, referred to the buffer output. This keeps the noise contributions of the DAC and buffer lower than the transducer's current noise of 0.9 nA_{rms}.

3.3. DAC CIRCUIT DESIGN

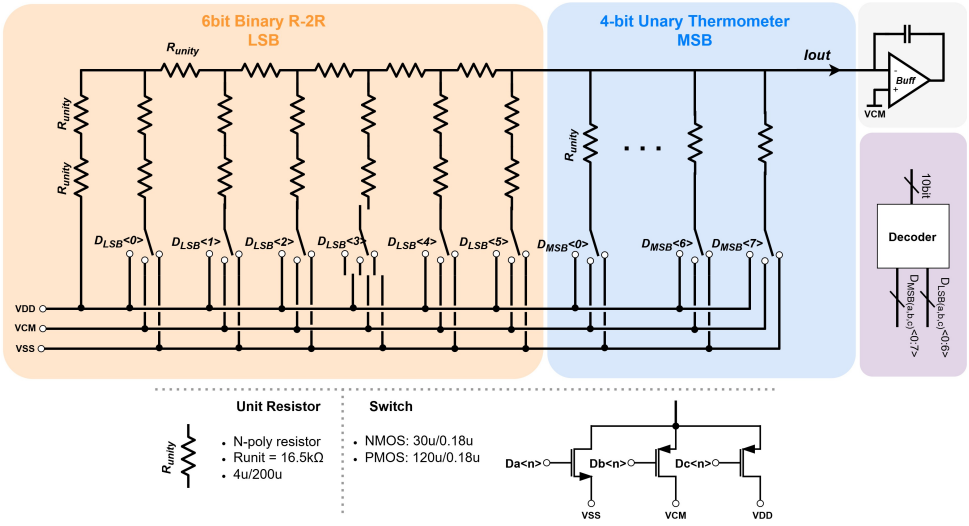


Figure 3.3: DAC Transistor level

Specifications

The design of the DAC begins with its specifications. Based on the system-level design, the DAC should operate in the current domain. Additionally, its input-referred noise should not exceed the noise floor of the transducer. Finally, the linearity and bandwidth must be designed to avoid introducing SNR degradation or stability issues.

Topology

Two common topology options for DAC are the Resistive DAC (RDAC) and the Current Steering DAC (CS-DAC) [51]. Both of this topologies can obtain low-noise performance by trading more power. Increasing the power results in a proportional increase in signal amplitude, whereas the noise grows only with the square root of the power increase. One advantage of the RDAC is that, for an equal level of power usage, it generates lower thermal noise [52]. Its drawbacks, however, include a lower output resistance, determined by its total resistance, which can load the following amplifier stage and reduce the loop gain. In addition, its operating speed is limited by the RC time constant of the switches. Considering that a buffer is used between the DAC and the LNA and the design targets a 2.6 MHz signal bandwidth, the RDAC is preferred for its consistently lower noise performance. Therefore, the RDAC is selected for this design.

Segmented thermometer and R-2R topology
Having selected the RDAC topology, the next step is to determine the code representation. A fully unary, thermometer-coded DAC structure provides excellent matching, resulting in high linearity. However, this comes at the cost of significant area usage and routing complexity, as a 10-bit implementation would require 1023 unit resistors.

An alternative is the binary structure based on the R-2R ladder topology, which is far more compact, requiring only 20 resistor elements for a 10-bit DAC. However, it suffers from poor matching, leading to degraded linearity.

To balance linearity with area efficiency, a hybrid segmented approach is adopted in this design: a 4-bit unary segment for the most significant bits (MSBs) combined with a 6-bit binary segment for the least significant bits (LSBs).

The DAC block schematic, including component sizing, is shown in Figure 3.3.

Unit Resistor
Following the component selection for noise requirements in Section 3.2, the unit resistor is set to 16.5 kΩ, with its area adjusted to mitigate mismatch. A total resistance of 2 kΩ corresponds to a maximum output current of 0.9 mApp and an LSB current of 1.75 μApp.

Switch
The system operates in a pulsed-wave mode, so the DAC remains in quiescent mode for a large fraction of the time, ideally providing zero current. To eliminate current consumption during this period, a three-switch configuration is used with supply voltages of 1.8 V, 0.9 V, and 0 V. Consequently, when no signal is applied, the DAC sits at the common-mode voltage, and no current flows, as one terminal of R_{DAC} is at V_{CM} and the other terminal is at the buffer's virtual ground, also at V_{CM}. The switches are sized with an on-resistance well below that of the unit resistor, reducing nonlinearity and enhancing speed.

Decoder
The decoder drives the switches, alternating between 0 V and V_{CM} for negative currents, and between V_{CM} and V_{DD} for positive currents. Furthermore, its contribution to power consumption and delay is negligible compared to the resistor ladder.

DAC Mismatch
Mismatch in the unit resistors can introduce distortion in the DAC output, making it necessary to define a specification to see its impact on system performance. In system-level MATLAB simulations, a non-ideal DAC with 6-bit binary and 4-bit unary segmentation was modeled. Each unit resistor was assigned a mismatch with standard deviation σ. By varying the mismatch, its effect on Doppler and Clutter SNR was evaluated, as shown in Figure 3.4. Additionally, the corresponding INL and DNL due to this mismatch were simulated. It can be observed that as the mismatch increases, the SNR of both Doppler and Clutter signals degrades, with a region where the degradation becomes much steeper. Moreover, the INL and DNL exhibit a roughly linear increase with increasing mismatch.

To ensure a Doppler SNR above 30 dB, the unit resistor mismatch must be kept below 0.67%, corresponding to a maximum DNL of $0.54LSB$.

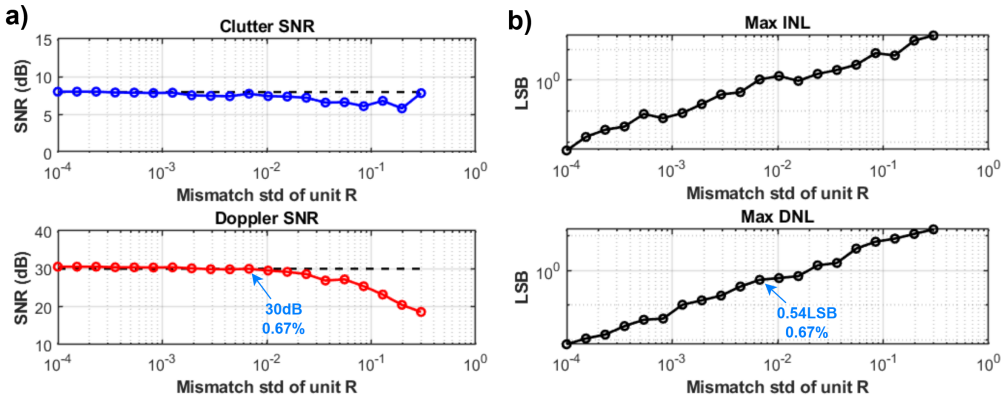


Figure 3.4: DAC Mismatch a) SNR Doppler and SNR Clutter vs mismatch. b) DNL and INL vs mismatch

Linearity and Bandwidth
With the DAC mismatch specification established, Monte Carlo simulations were performed to evaluate linearity of the element level Cadence model. The design meets the requirements, exhibiting a maximum DNL below $0.25LSB$ at 3σ across all corners. System speed was also assessed for an 80 MHz bandwidth, showing negligible phase delay.

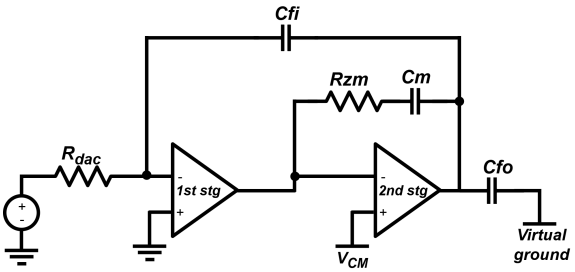
3.4. DAC BUFFER CIRCUIT DESIGN

Specifications
The DAC Buffer has the following functions. First, it scales the DAC output current from the mA-range down to the μA-range. Second, it isolates the RDAC from the LNA input, thereby preventing any loading effects that could otherwise reduce the loop gain of the LNA. In addition, the buffer architecture allows for Time Gain Compensation (TGC), where the gain can be adjusted by tuning the output capacitor.

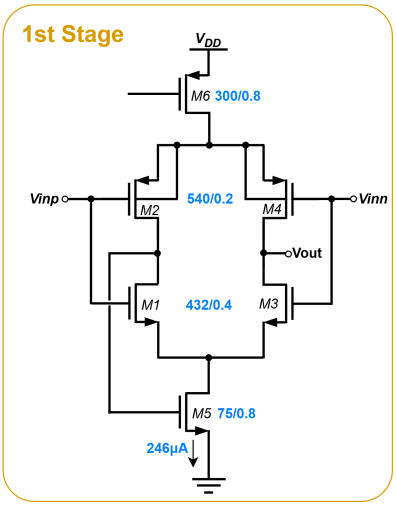
A key specification of the DAC buffer is that its noise contribution must not exceed that of the DAC itself, so as to avoid degrading the overall noise performance of the signal path.

As discussed in Section 3.2, the passive components were selected to ensure that the DAC and DAC Buffer blocks meets the required low-noise performance.

Amplifier
A two-stage amplifier is implemented creating an orthogonal design approach. The first stage is optimized for noise performance hence providing low noise specification to the overall amplifier. The second stage is optimized for high output swing.



C_{fi}	34.2pF
C_{fo}	1pF
C_m	12pF
R_{dac}	2kΩ
R_{zm}	250Ω
g_{m1}	7.26mS
g_{m2}	4.26mS



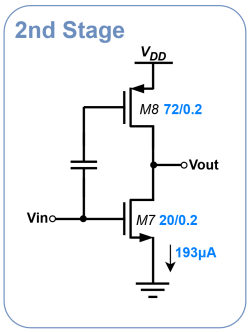


Figure 3.5: DAC Buffer Schematic with sizing and component values

First stage

The first stage employs the topology described in [53]. A current-reuse configuration is adopted to effectively double the transconductance (g_m). Furthermore, the input transistor pairs are biased in the subthreshold region to maximize the g_m/I_D efficiency.

To realize a single-ended amplifier, the output of the positive input branch is fed back to the tail transistor, forming a local feedback loop. This loop provides common-mode regulation by forcing the sources of M_1 and M_2 to follow the variations of V_{in+} and adjust the current accordingly, thereby stabilizing the common-mode level.

Finally, the input NMOS transistors are designed with a channel length larger than the minimum feature size in order to suppress $1/f$ noise.

Second stage

The second stage is a push-pull stage in order to optimize the output swing. Each transistor is biased with an overdrive voltage of 100mV allowing an output swing of 1.6V.

A Miller cap C_M is used for stability compensation and a resistor R_{zm} is introduced to cancel the right-half-plane (RHP) zero introduced by the Miller cap.

Bode plot
Figure 3.6 illustrates Bode plots of the loop of the amplifier. The Miller compensation ensures a phase margin of 60 degrees. Furthermore, while the Miller capacitor shifts the first pole to the kHz range, the loop gain remains adequate in the bandwidth of interest, guaranteeing gain accuracy and linearity.

The closed-loop transfer function exhibits a right-half-plane zero, as shown in Fig. 3.6. This zero is introduced by the feedback capacitor, which creates a feed-forward path and leads to a high-pass characteristic. Such a behavior can affect the stability of the closed-loop system. To address this, the second-stage gm is adjusted so that the right-half-plane zero is shifted farther from the sampling frequency.

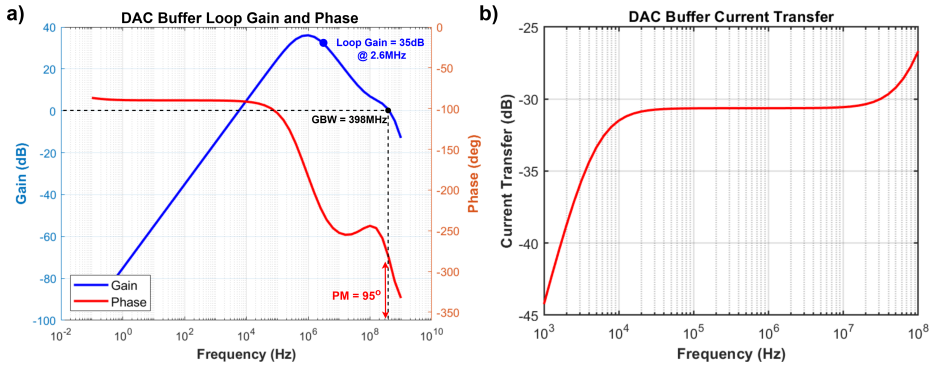


Figure 3.6: a) DAC Buffer Loop Gain and Phase. b) DAC Buffer Current Transfer

3.5. BIASING

The current reference circuit which is biasing the amplifier is illustrated in Fig.3.7 a). It is implemented as a cascode constant-gm structure that generates a reference current of 10 µA. This current is then mirrored to the amplifiers through transistors with different sizing ratios, ensuring proper biasing conditions. The total power consumption of the current reference circuit is $0.219mW$.

The biasing scheme for the second stage amplifier adopts the topology described in [54], [55]. It employs a GΩ-equivalent resistor, realized by a turned-off transistor, together with a switch that operates once every slow-time cycle as illustrated in 3.7 b). This mechanism establishes the biasing voltage for the network, after which the switch is disabled during normal operation to suppress any noise contribution from the biasing path.

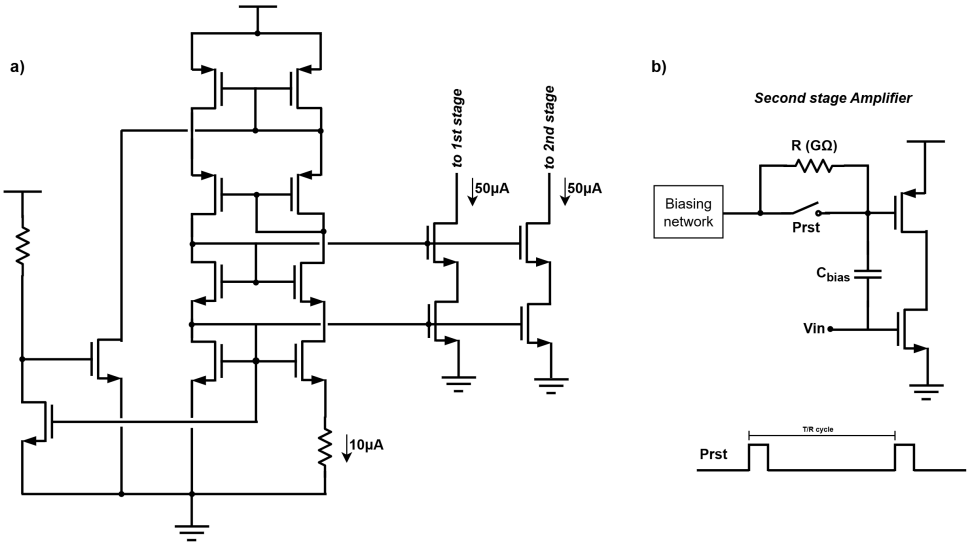


Figure 3.7: a) Current reference schematic b) Biasing scheme of second stage amplifier

4

SIMULATION RESULTS

The simulations of the system were carried out in Cadence Virtuoso. The purpose of these simulations is to demonstrate the feasibility of the slow-time system architecture at the transistor level.

4.1. TRANSIENT AND SPECTRUM RESULTS

Two types of simulations were conducted. In both cases, the clutter signal was set to 2.6 MHz and the Doppler signal to 2.4 MHz. A total of ten slow-time cycles, each consisting of 200 T_{sample}, were applied ($T_{\text{sample}} = 96ns$).

In the first simulation, a continuous-wave input was used to analyze the system response in the frequency domain. The clutter signal amplitude was set to 6.5 μA, whereas the Doppler signal amplitude was 0.065 μA.

In the second simulation, a *pulse-wave input* was applied, consisting of 6.5 clutter pulses at 2.6 MHz and 6 Doppler pulses at 2.4 MHz superimposed, resulting in a total pulse duration of 2.5 μs. For this case study, the clutter signal had a peak amplitude of 9.8 μA, while the Doppler signal had a peak amplitude of 0.65 μA. These values were intentionally increased in order to clearly demonstrate the system's transient response.

All simulations were performed under standard conditions (TT corner, room temperature).

Figure 4.1 illustrates the spectrum results of the continuous-wave (CW) simulation. Figure 4.1 a) shows the input signal, while figure 4.1 b) presents the output of the ADC at the last slow-time cycle. At the input, the clutter component is approximately $40dB$ stronger than the Doppler component. After slow-time filtering, the clutter signal is ef-

fectively suppressed, falling near the quantization noise level with clutter $SNR = 3.51dB$. Additionally, the final Doppler signal is approximately $23dB$ higher than the noise floor, with Doppler $SNR = 13.1dB$.

Figure 4.2 illustrates the transient response of the pulsed-wave experiment. It can be observed that the system gradually suppresses the clutter component across successive slow-time cycles, leaving only the Doppler signal after approximately five to six cycles.

In the case of only clutter signal, a residual noise floor remains visible. This can be attributed imperfect cancellation of the signal and charge leakage in the sample-and-hold stages.

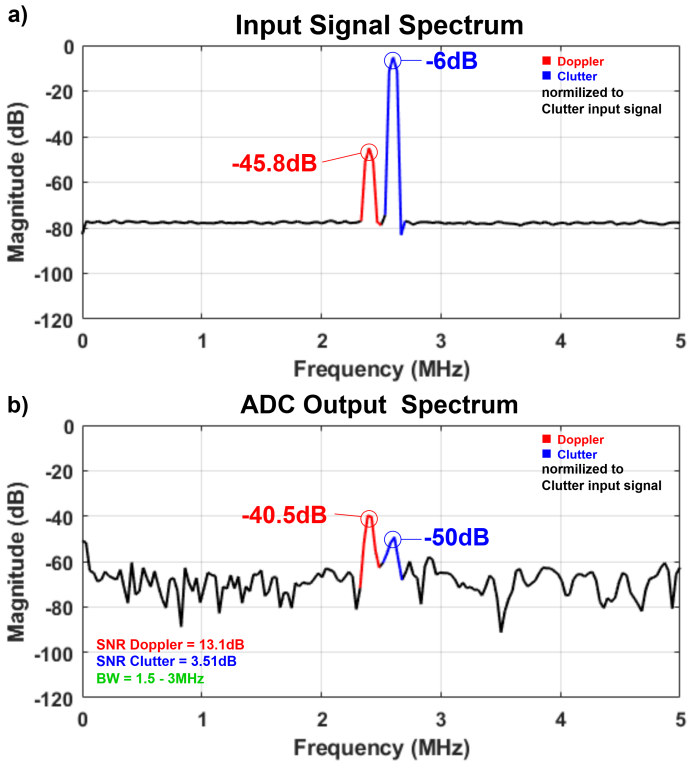


Figure 4.1: Spectrum of Input signal and ADC output at the last slow time cycle

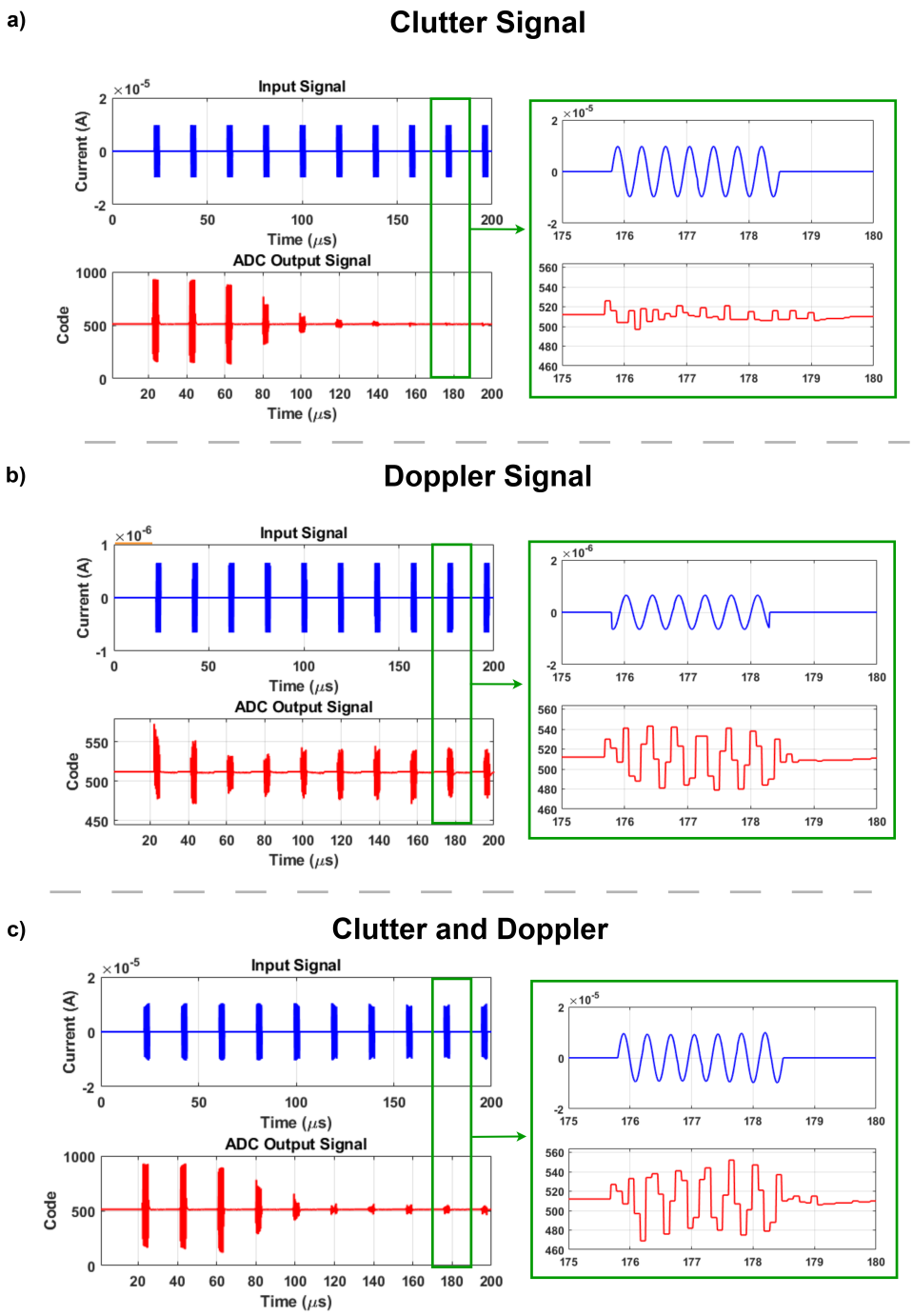


Figure 4.2: Pulsed Wave Doppler transient simulation results. Clutter signal only, Doppler signal only, and clutter and Doppler signal superimposed.

4.2. POWER AND AREA

The power distribution of the system per element is shown in Figure 4.3 (a). The power consumption for the Analog front-end together with the micro-beamformer is taken from [29].

From the chart it can be observed that the DAC consumes only a small fraction of the total power, which is consistent with the design objective of achieving very low power consumption in the quiescent state.

In contrast, the DAC Buffer accounts for a significant portion of the overall power consumption. This design choice was made in order to maintain the overall noise at a sufficiently low level, ensuring proper system performance.

However, after examining the results it can be observed that the chosen transconductance (g_m) of the buffer can also be traded for power. Reducing g_m lowers power consumption but slows down the feedback network, which in turn increases distortion. To evaluate this effect, a MATLAB model could be developed in which the distortion of the feedback network is gradually increased. The resulting SNR can then be observed to determine the acceptable level of distortion that does not compromise system performance. This analysis would allow the selection of a more suitable g_m for the buffer, potentially enabling further power savings at the cost of controlled distortion.

Figure 4.3 (b) illustrates the area occupied per element. It can be observed that the DAC and DAC Buffer together contribute approximately 30% additional area to the design. Within the DAC and Buffer, the feedback capacitor and the output capacitor of the Buffer occupy 46% of their combined area, indicating that there is potential for optimization in this part of the design. This design choice was made to ensure that the total output noise remains lower than the transducer noise.

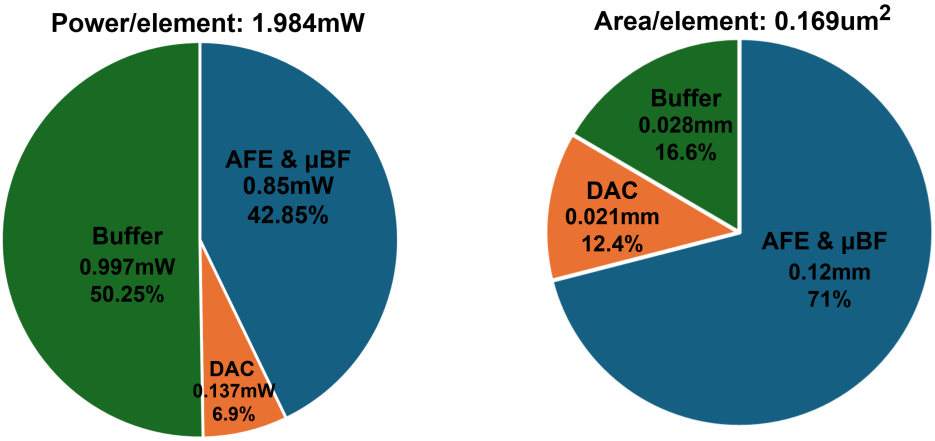


Figure 4.3: Power Consumption of slow-time architecture.

4.3. TOWARDS TARGETED SPECIFICATIONS

The simulation results indicate 53dB Instantaneous Dynamic Range with a target of 87dB and Doppler SNR of 13.1dB with a target of 30dB. Achieving this requires two necessary features: Time Gain Compensation (TGC) to reach the 57 dB difference, and a reconstruction filter to suppress DAC noise and preserve the 30 dB Doppler SNR.

Time Gain Compensation
The front-end amplifier is capable of providing up to 36 dB of Time Gain Compensation (TGC). The clutter-to-Doppler signal ratio is set to 57 dB, with the Doppler component positioned near the noise floor. At the first cycle, when no TGC is applied, the front-end captures the signal but the Doppler component does not yet achieve the target SNR of 30 dB. As the slow-time delta modulator progressively accumulates and cancels the clutter, the TGC is gradually ramped up to provide 36dB additional gain to the Doppler signal, without clipping the LNA.

For instance, the clutter signal can be 46.26 μA, whereas the Doppler signal is 0.065 μA. To suppress the clutter component under these conditions, the feedback circuit can be tuned to output a current of 46.26 μA by setting the feedback capacitor C_{fo} to 3.54 pF. Furthermore, the coefficient α of the slow-time delta modulator can be adjusted to 0.9 for the first two cycles, quickly capturing the high-amplitude clutter component. Subsequently the coefficient α is adjusted to lower values to meet the stability requirements.

Without TGC, if the front-end were set to its full gain of 104 dB, the amplifier would clip for the given clutter signal, disrupting the slow-time feedback loop and preventing stable operation. By gradually applying TGC, the dominant clutter component is suppressed before the amplifier reaches maximum gain, allowing stable operation without clipping. Consequently, the system can achieve the desired 57 dB difference between clutter and Doppler signals.

Figure 4.4 illustrates a MATLAB model of the system including the TGC function. In this simulation, the clutter component is initially about 57 dB stronger than the Doppler signal. After applying the slow-time cancellation, the clutter is suppressed to the noise floor, effectively removing its impact on the receiver dynamic range.

As a result, the required dynamic range of the receiver can be relaxed by approximately 57 dB. In the same simulation, the resulting Doppler signal-to-noise ratio (SNR) is 16.65 dB, while the residual clutter SNR is –9.53 dB, confirming that clutter is no longer the dominant limitation.

Reconstruction filter
After the clutter suppression the output signal contains a dominant quantization noise from the DAC which substantially reduces the Doppler SNR. A reconstruction filter is necessary to remove the DAC quantization noise[23].

Figure 4.5 a) illustrates the Block diagram with the reconstruction filter and 4.5 b) illustrates the equivalent signal model.

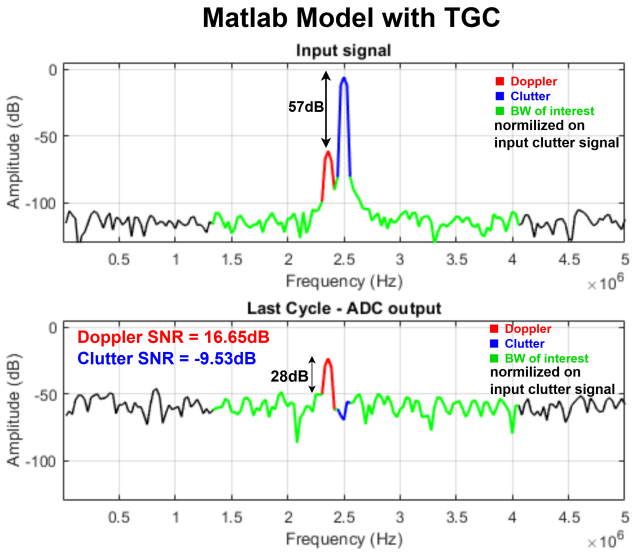


Figure 4.4: Matlab model with TGC function, effectively canceling the clutter signal with 57dB dynamic range difference

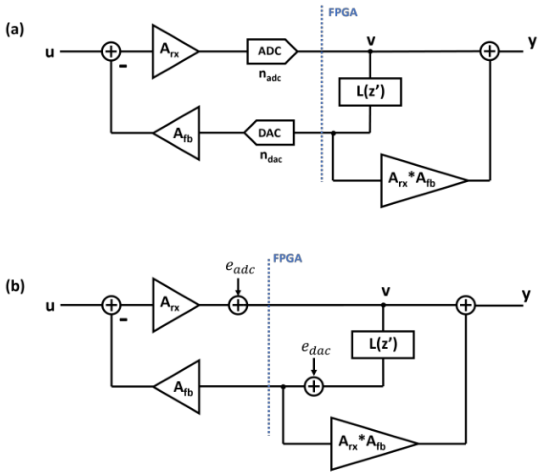


Figure 4.5: (a)Block diagram and (b)equivalent model of slow-time delta modulator with reconstructed output [23]

From there it can be derived that the NTF from u to v due to the ADC quantization error is equal to:

$$v = \frac{1}{1 + A_{fb} A_{rx} L(z')} e_{adc} \tag{4.1}$$

While the NTF from u to v due to the DAC quantization error is equal to:

$$v = -\frac{A_{rx}A_{fb}}{1 + A_{fb}A_{rx}L(z')}e_{dac} \tag{4.2}$$

Since the A_{rx} is 57dB higher than the A_{fb}, this implies that the dominant noise source comes from the quantization noise of the DAC.

To reconstruct the signal the output of the DAC needs to be multiplied by $A_{rx} * A_{fb}$ and summed to the output of the ADC as illustrated in 4.5 b). This way the NTF from DAC quantization noise to node y is effectively canceled out as follows:

$$y = \left(1 + A_{rx}A_{fb}L(z')\right)v + A_{rx}A_{fb}e_{dac} = 0 \tag{4.3}$$

while the transfer function of the system becomes:

$$y = A_{rx}u + e_{adc} \tag{4.4}$$

Consequently, the system can achieve the desired Doppler SNR of 30 dB.

4.4. COMPARISON WITH STATE-OF-THE-ART DESIGNS

Table 4.1 provides a comparison of the proposed system with state-of-the-art designs in the same 180 nm BCD technology. While the achieved Doppler SNR (13.1 dB) and input instantaneous dynamic range (53 dB) are below those reported in prior works, the expected results shows the potential to reach the targeted specifications of 30 dB SNR and 87 dB dynamic range.

The proposed design also exhibits a relatively large active area per element (0.169 mm²) and higher RX power consumption (1.98 mW/EL) compared to other implementations. These overheads result from the additional feedback and buffering circuitry required for clutter cancellation. With further refinements particularly in buffer design the power could be reduced towards state-of-the-art levels.

Overall, the architecture offers a trade-off, exchanging additional power and area for higher dynamic range, while avoiding the need for high-resolution ADCs and high-dynamic-range LNAs, making it a promising alternative for Transcranial Doppler ultrasound systems.

	This work	**Expected**	**[29]**	**[56]**	**[57]**	**[58]**
Technology	180nm BCD	180nm BCD	180nm BCD	180nm BCD	180nm BCD	180nm BCD
Center frequency	2.6	2.6	2.6	5.5	6	9
Element pitch	365µm	365µm	365µm	208µm	160µm	125µm
Channel reduction	8x	8x	8x	64x	18x	128x
Active Area/EL [mm^2]	0.169	0.169	0.12	0.043	0.03	0.016
RX Power / EL [mW]	1.984	1.984	0.85	0.66	1.12	1.31
Peak SNR [dB]	13.1	30	32	54.5	52.2	54
Instantaneous Input DR	53	87	73	N/A	91	83

Table 4.1: Comparison with state-of-the-art ultrasound receiver designs

5

CONCLUSION

5.1. THESIS CONTRIBUTIONS

This thesis contributes to the development of integrated front-end architectures for Transcranial Doppler (TCD) ultrasound by tackling the main limitations of sensitivity and miniaturization while also addressing efficiency. The key contributions are:

- **Elaboration of a novel slow-time feedback receiver architecture:** A pulsed-wave RF-sampling architecture with integrated slow-time feedback was elaborated and analyzed, enabling clutter suppression directly in the analog domain. This improves the detection limits of TCD systems, allowing weak Doppler signals to be resolved in the presence of strong tissue and skull reflections.
- **Relaxed front-end requirements:** By shifting clutter suppression to the analog front-end, the dynamic range requirements of both the LNA and the ADC are reduced by approximately 57 dB. As a result, the output data rate is lowered and the subsequent digital processing is simplified.
- **Integration of micro-beamforming to slow-time system** A micro-beamforming scheme was integrated to slow-time system. This provides on-chip directivity with reduced channel count, area, and routing complexity, making the design more scalable to larger arrays and more suitable for miniaturized systems.
- **Prototype-level circuit implementation:** Critical blocks of the feedback path, including a DAC and DAC buffer, were designed and simulated at transistor level. Their integration with a previously designed receiver from the *Electronic Instrumentation Laboratory* demonstrates the feasibility of implementing the full slow-time feedback loop in silicon.

- **Efficiency and miniaturization:** The implementation of micro-beamforming provided a four times channel reduction, meaning fewer channels need to be processed and routed off-chip, contributing to a smaller device footprint and lower data volume. Additionally, the use of slow-time feedback reduced the ADC resolution requirement from 14-bit in conventional architectures to 10-bit, further decreasing the data rate.

5.2. FUTURE WORK

While this thesis demonstrates the feasibility and advantages of a slow-time feedback architecture for Transcranial Doppler (TCD) front-ends, several aspects remain for further research and development:

- **Implementation of TGC and reconstruction filter** Implementation of TGC and reconstruction filter is required to reach the targeted specifications.
- **Test over PVT variations:** The robustness of the proposed architecture should be verified across process, voltage, and temperature (PVT) variations to ensure stable performance under realistic fabrication and operating conditions.
- **Complete prototype integration:** Future work should include the design and integration of the remaining blocks, such as the on-chip ADC and a shift-register logic block to connect the slow-time integrator with the DAC. This would allow data transfer in a compact serial manner using digital logic, reducing the number of interconnects required for each DAC.
- **Power optimization:** Other architecture for the DAC Buffer can be explored to further reduce the power consumption of the block while also maintaining the same low noise.
- **Scaling to larger arrays:** Extending the micro-beamforming concept to larger transducer arrays would enable higher image quality and improved spatial resolution.
- **Fabrication and measurements:** A critical next step involves implementing the physical layout, fabricating a prototype chip, and designing a PCB for measurement test.
- **Towards clinical translation:** Future efforts should also focus on system-level integration with transducers and user interfaces, as well as collaboration with medical partners to evaluate the potential of the proposed architecture in clinical scenarios.

5.3. CONCLUSION

This thesis has presented the analysis, design, and prototype implementation of an analog front-end receiver with slow-time feedback for Transcranial Doppler (TCD) ultra-

sound. By addressing limitations in sensitivity by means of detection limits in current TCD systems, the proposed architecture demonstrates a promising path toward improving the performance of clinical TCD devices, while also improving their efficiency and paving a direction towards wearable devices. The work combined system-level modeling, functional block design, and transistor-level implementation of critical circuits, showing both the feasibility and potential advantages of integrating clutter suppression directly in the analog domain. The results highlight how the proposed circuit architecture can enhance TCD hardware, contributing to more effective medical diagnostic and monitoring tools for critical brain disorders.

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