Evaluating the Impact of Process Variation on RRAMs

Brum, E. ; Fieback, M.; Copetti, T.S.; Jiayi, H. ; Hamdioui, S.; Vargas, F. ; Bolzani Poehls, L.M.

DOI
10.1109/LATS53581.2021.9651789

Publication date
2021

Document Version
Final published version

Published in
2021 IEEE 22nd Latin American Test Symposium, LATS 2021

Evaluating the Impact of Process Variation on RRAMs

E. Brum[1], M. Fieback[2], T. S. Copetti[3], H. Jiayi[3], S. Hamdioui[2], F. Vargas[1], L. M. Bolzani Poehls[3]
[1]EASE, PUCRS, Brazil
[2]Computer Engineering Laboratory, Delft University of Technology, The Netherlands
[3]IDS, RWTH Aachen University, Germany
Email: edulbrum@gmail.com, vargas@pucrs.br, [copetti, poehls]@ids.rwth-aachen.de

***Abstract*—Over the last fifty years Complementary Metal Oxide Semiconductor (CMOS) technology has been scaled down, making the design of high-performance applications possible. However, there is a growing concern that device scaling will become infeasible below a certain feature size. In parallel, emerging applications present high demands regarding storage and computing capability, combined with challenging constraints. In this scenario, memristive devices have become promising candidates to replace or complement CMOS technology due to their CMOS manufacturing process compatibility, zero standby power consumption as well as high scalability and density. Despite these advantages, the implementation of high-density memories based on memristive devices poses some challenges related manufacturing process variation and consequently, to their reliability during lifetime. This paper investigates the impact of manufacturing process variation on Resistive Random Access Memories (RRAMs). In more detail, an evaluation of the RRAM's functionality when considering different levels of manufacturing process variation is performed. The obtained results show that different parameters can degrade the functionality of the RRAM cell as well as that there is a relation between the performed operating sequence and the tolerated percentage of variability. Finally, it is important to mention that understanding how process variation impacts the functionality of RRAM cells is considered essential to guarantee their reliability during lifetime, also allowing to optimize manufacturing processes.**

***Index Terms*—Process Variation, RRAMs, Memory's Functionality.**

I. Introduction

Complementary Metal Oxide Semiconductor (CMOS) technology scaled down according to Moore's and Dennard's laws during the last five decades [1, 2]. Limitations on the continued transistor miniaturization and increasing demand for high-performance applications pose significant challenges to device technologies and computer architectures, increasing the necessity of novel devices and architectures able to deliver high performance systems for emerging applications. In this scenario, memristive devices represent a promising candidate to replace or complement the CMOS technology mainly due to their CMOS manufacturing process compatibility as well as high scalability and density [3]. Note that when used as a memory, ionic thin film and molecular memristors are called resistive memories, more precisely Resistive Random Access Memories (RRAMs), being classified as non-volatile memories [4, 5]. A RRAM presents some advantages with respect to Flash memories, such as, operating at higher frequencies and better cell cycle endurance [6]. RRAMs are also compatible with standard CMOS production processes and can be easily manufactured in the Back-End-Of-Line (BEOL) of a CMOS process [6]. However, as observed in CMOS technology, RRAMs are also susceptible to manufacturing defects and process variation due to their relatively immature fabrication process and inherent variability in the manufacturing flow, which can compromise their use [7]. Thus, the adoption of RRAMs in emerging applications depends on guaranteeing their quality and reliability after manufacturing, which can only be achieved by understanding the real impact of process variation on their functionality and performance. Note that even a slight parametric variation in a device, due to process variation or defects, can cause a large shift in its normal operating conditions [7]. As a result, such non-idealities may result in permanent or transient faults that have a catastrophic or parametric impact on the performance of these non-volatile memories [7]. This paper evaluates the impact of process variation on RRAMs' functionality in order to establish the tolerated variability of RRAM cells. Moreover, the proposed evaluation aims to identify the most critical manufacturing parameters, which make the optimization of the fabrication process possible. Electrical simulations considering a case study composed of a RRAM cell array and peripheral circuity were performed using CADENCE Spectre. The obtained results show that some manufacturing parameters can be considered more critical than others, since cause functional misbehavior of RRAM cells. Further, the results also demonstrate that there is a relation between the performed operating sequence and the tolerated percentage of variability. The remainder of this paper is structured as follows: Section II describes the background related to RRAMs. Section III discusses the importance of studying RRAM process variation from the point of view of different RRAM-based applications. In Section IV, the experimental setup adopted for performing the electrical simulations is detailed. Section V presents the obtained results and finally, conclusions are drawn in Section VI.

This work was supported by the Federal Ministry of Education and Research (BMBF, Germany) within the NEUROTEC project (project numbers 16ES1134 and 16ES1133K).

2021 IEEE 22nd Latin American Test Symposium (LATS) | 978-1-6654-2057-0/21/$31.00 ©2021 IEEE | DOI: 10.1109/LATS53581.2021.9651789

II. Background related to RRAMs

RRAMs are arrays of memristive devices, which are three layer devices consisting of a dielectric sandwiched between two metal electrodes. In more detail, the memory cell is based on a Metal/Insulator/Metal (MIM) structure [8]. According to [9], a memristive device is a passive element that can be described by the time integral of the current (charge q) through the time integral of the voltage (flux ϕ) across its two terminals [9]. In more detail, a memristor has at least two distinct states, the High Resistance State (HRS) and the Low Resistance State (LRS), and can switch from HRS (LRS) to LRS (HRS) by applying a voltage VSET (VRESET) with an absolute value larger than its threshold voltage (Vth). This functional characteristics of the memristive devices can be affected due to variations during the manufacturing process. Note that a certain level of variability should be tolerated, since it should not cause any faulty behavior. However, extreme variability should not only degrade the device's performance, but cause different types of faults. Finally, it is important to point out that memristive devices require an additional step after manufacturing, called forming process. This step if performed in order to switch the devices' state from their initial resistance state to the normal LRS [7]. Note that this process affects characteristics of the conductive filament, such as width and length, influencing the device's functionality [6].

III. Importance of RRAM Variations

In this section, we demonstrate the importance of understanding the impact of RRAM variations by illustrating its effects on three applications.

Neural networks require many Vector-Matrix Multiplications (VMM) to perform inference. In traditional computing architectures, this operation is costly and time consuming. However, the analog nature of RRAM devices allows to make efficient architectures that can perform this multiplication in a single cycle [10]. In such architectures, the weight matrices of the network are stored in a RRAM crossbar and the multiplication is done by applying a vector as an input voltage directly to this matrix. The current that flows out of the crossbar matrix represents the outcome of the multiplication. However, it is shown that variations in RRAMs decrease the prediction accuracy in the presence of variations [11]. This accuracy loss can be addressed by re-training the network, while taking the variations into account. This can be either done by using software on a host computer, which prevents in-field updates [11], or online, which requires additional hardware and negatively affects the write endurance of the device [10]. Hence, understanding the effect of RRAM variations allows to optimize both the networks and the hardware, while keeping the cost minimal.

Variations in a RRAM device can be used to generate random numbers [12, 13]. However, when using these generators in security applications, their performance needs to guarantee sufficient randomness, e.g., using the NIST statistical test suite [14]. The circuit may fail some of the criteria and needs to be further developed. For this aim, it is important to understand how the different components in the circuit affect the variations in RRAM devices and vice versa. Understanding RRAM variations gives handles to optimize random number generators so that they can be used in security applications.

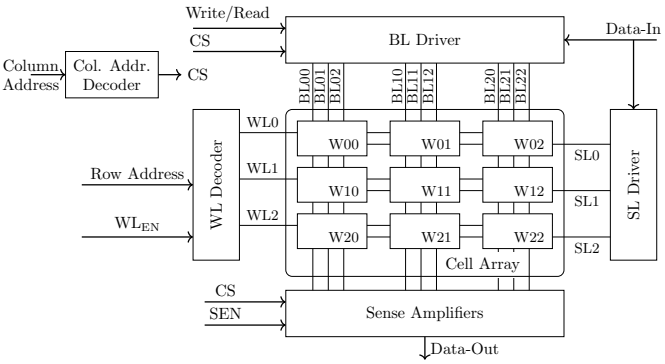

Fig. 1: Case study architecture.

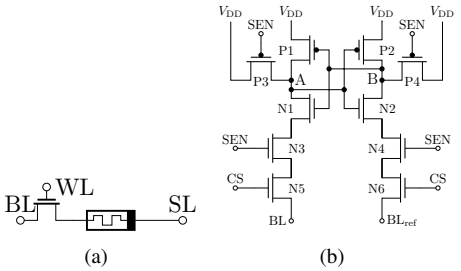

Fig. 2: (a) 1T1R RRAM cell and (b) SA.

As was stated before, RRAMs are a promising alternative to replace Flash memories, due to their small cell size, lower write latency, and lower energy consumption [15]. Unfortunately, for mass-commercialization, every part of the RRAM needs to be optimized so that no silicon area is wasted, while still having maximal performance. This means that the circuits that drive RRAM cells need be optimized to be as small as possible, while still tolerating the inherent variability of RRAMs. Hence, to understand this optimization's trade-offs, one needs to scrutinize how the complete read and write paths are affected by RRAM variations.

From the above, it becomes clear that variation impact on RRAM is an important factor that influences not only the design of the RRAM device itself, but rather the complete circuit.

IV. Experimental Setup

This section describes the complete RRAM architecture used as case study and the configurations adopted during the simulations.

A. Case Study: Circuit Description

The entire RRAM architecture adopted as case study is illustrated in Fig. 1. The case study consists of a 3x3 word cell array with peripheral circuitry. All words on one row share the Word Line (WL) and Select Line (SL), while all words in one

column share a Bit Line (BL). Every word consists of three single RRAM cells, storing one bit of data each. The single cell (1T1R) is composed of one Transistor (1T) to control the current through the memristor (1R), as shown in Fig. 2(a). The peripheral circuitry is used to write to and read back from the cell array. The column address decoder selects the desired column, column select (CS), based on the column address. Similarly, the WL decoder selects the WL that corresponds to the desired row address once the WL enable (WL_{EN}) signal is enabled. When a write operation is performed, a reset operation is performed on the selected word, i.e., every cell in the word stores only '0'. This reset operation is performed by driving the SL to V_{reset} and the corresponding BL to GND. When the data to be written to a cell (Data-in) contain a '1', a set operation is performed subsequently on that cell only. This is done by setting the BL to V_{DD} and the SL to GND. This writing scheme ensures that the cells are not over-set, which may lead to low-reliability [16]. Sense Amplifiers (SAs), one per BL, are used to read out the words, as shown in Fig. 2(b) [17]. A read operation works as follows. When the SA Enable (SEN) signal is '0', nodes A and B are precharged. Next, when SEN is '1', the SA is connected via the BL to the cell, and to a reference cell via the reference BL (BL_{ref}). The reference in the presented design is just a resistor between BL_{ref} and GND. The node that is connected to the lowest resistance will be discharged to GND, while the one with higher resistance will be charged to V_{DD}. Hence, node B will contain the value that is stored in the cell. The adopted case study was implemented using the $130\,\mathrm{nm}$ Predictive Technology Model (PTM) for the CMOS-based circuits and the RRAM (Pt/HfO_2/TiO_x/Pt) compact model from [18, 19]. Finally, the voltage adopted for performing a *write '1'* operation, or in other words a SET operation, is equal to 1.6 V. The RESET operation is performed by applying a voltage of - 1.7 V, and a READ operation requires a voltage pulse of 0.16 V.

B. Configurations Adopted During Simulations

In order perform the proposed evaluation, two different configurations were defined. The first configuration aims to identify the most relevant manufacturing parameters with respect to RRAM cell functionality. Moreover, the second one evaluates the impact of the device-to-device variations on the complete memory performance.

1) Configuration 1: Single Manufacturing Parameter Variations: In this first configuration, we analyze which manufacturing parameters will affect the RRAM cell performance the most. The results obtained from these experiments can be used to optimize the manufacturing process, aiming to minimize the variability of these parameters and, consequently, to guarantee reliable RRAMs. Note that the following parameters were individually varied during simulations [19, 20]: (1) Maximum oxygen vacancy concentration in the disc (Ndiscmax); (2) Minimum oxygen vacancy concentration in the disc (Ndiscmin); (3) Length of the disc and plug region (Ldet); and (4) Radius of the filament (Rdet) [19].

2) Configuration 2: Device-to-Device Variations: This configuration aims to evaluate the device-to-device variation impact. A total of 100 iterations were simulated for each percentage of variability (1%, 2%, 5%, 10% and 20%), while performing the following operating sequences: 0w0w0r0, 0w1w0r0, 1w0w1r1, 1w1w1r1. Here, 'w' denotes a write operation, 'r' a read operation, and '0'/'1' indicates the cell's content. These operations contain transitioning writes in every direction (e.g., 0w1), as well as non-transitioning write operations (e.g., 1w1), and read operations (e.g., 0r0). Hence, this set of operations will give insights into the RRAM performance with respect to adopted operating sequence and its transitions. After the execution of every operation, we observed the value of the following parameters: (1) The actual oxygen vacancy density of the RRAM device (Nreal) [19], (2) Resistance State (RS) of the RRAM device for write operations, and (3) the output of the SA to validate read operations.

V. Obtained Results and Discussion

This section presents the results obtained through electrical simulations using CADENCE Spectre. In the first subsection we present the nominal results when simulating the circuit without any variation. Afterwards, we present and discuss the results from the previously described experiments.

A. Validation of the Case Study

In order to validate the case study and define the reference values of Nreal and RS when performing different operating sequences, four simulations were performed, one for each sequence. Note that during this step, the manufacturing parameters were not varied and consequently, nominal values were adopted for all parameters (Ndiscmax = $20 \times 10^{26} m^{-3}$; Ndiscmin = $0.1 \times 10^{26} m^{-3}$; Ldet = 0.4 nm; and Rdet = 45 nm). Fig. 3 depicts the observed values of Nreal, RS and SA considering the execution of the four operating sequences. It is important to mention that RS is calculated by the division of voltage over current for each performed operation. However, due to the way that read operations are performed in this particular case study, it is not possible to determine the cell's RS during read operations, since the SA works as a current source over the cell, mainly when the cell is in HRS (logic '0'). Thus, the graphs include the SA logic value when performing read operations. Further, the resistance value associated to LRS (logic '1) is around 1.6 kΩ and around 60 kΩ for HRS (logic '0'), which corresponds to an Nreal of $20 \times 10^{26} m^{-3}$ and $0 \times 10^{26} m^{-3}$, respectively. Observing the graphs, it is possible to see that the SA slightly increases the Nreal value of the memristor when a *read '0'* is performed, without changing the logic value stored in the cell. Another important aspect to be noted is that the cell's resistance value after performing a 'w0' operation considering the sequence '1w0' is lower than the resistance when executing '0w0'. The RS considering the sequence '1w0' is around 52 kΩ and the sequence '0w0' 63 kΩ, which indicates that the transition from LRS to HRS impacts the resistance value of the cell. Finally, Nreal is the most accurate parameter to represent the cell's resistance state

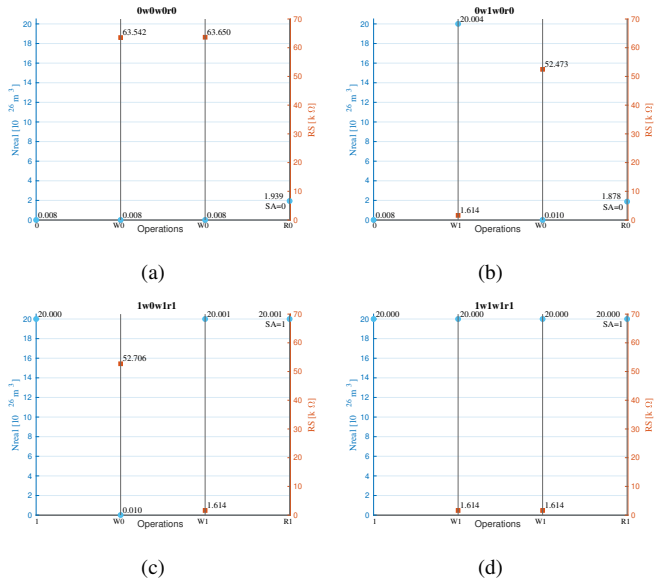

Fig. 3: Nominal values when performing the following operations: (a) 0w0w0r0, (b) 0w1w0r0, (c) 1w0w1r1, and (d) 1w1w1r1.

TABLE I: Manufacturing Parameter Variations.

Parameter	Default	Upper	Lower	Step
Rdet(nm)	45	100	5	1
Ldet(nm)	0.4	5	0.1	0.1
Ndiscmax($\times 10^{26} m^{-3}$)	20	30	10	1
Ndiscmin($\times 10^{26} m^{-3}$)	0.008	1	0.001	0.01

during the execution of write and read operations, since it represents the oxygen vacancy concentration in the disc of the cell during the operation execution time [20]. Note that according to [20], the disc of the cell represents one region of the conductive filament.

B. Evaluating the Impact of Single Manufacturing Parameter Variations

The evaluation of the impact on the RRAM cell was performed varying a single manufacturing parameter (Rdet, Ldet, Ndiscmax, and Ndiscmin) according to Table I. In more detail, Table I summarizes default value, the upper and lower limit, as well as the adopted increment factor for each parameter. The default value and limits are defined in [20]. Figures 4, 5, 6, and 7 depict the most relevant results, summarizing examples when single parameters affect the RRAM device functionality.

In Fig. 4, it is possible to see the relation between RS and Rdet when executing the first *write '1'* of the operation sequence *0w1w0r0*. In these simulations, Rdet was varied from 5 nm to 100 nm, assuming a 1 nm increment step. In more detail, when Rdet reaches a value above 20 nm, the resistance value of the cell suffers a strong drop, reaching a value close to 1.6 kΩ, and basically remains constant for a Rdet between 49 nm and 100 nm. Hence, to properly perform a *write '1'* operation, Rdet needs be larger than 20 nm, otherwise the RRAM cell would remain at logic '0'.

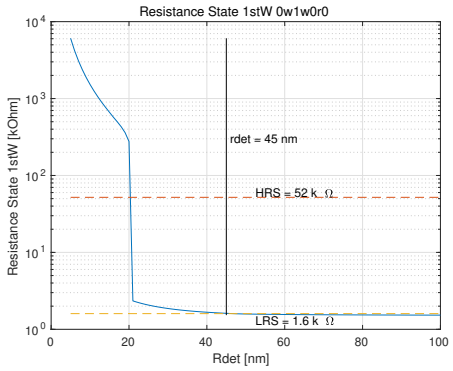

Fig. 4: Resistance observed when performing the first write operation of 0w1w0r0, varying Rdet.

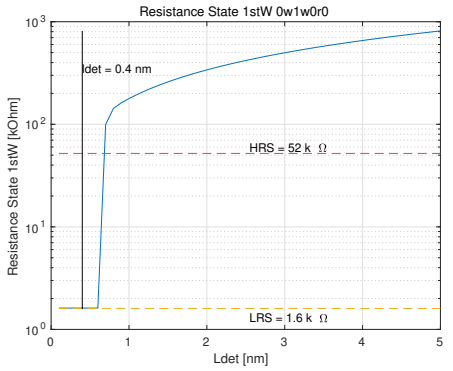

Fig. 5: Resistance value observed when performing the first write operation of 0w1w0r0, varying Ldet.

Fig. 5 presents the relation between the RS value and Ldet when performing the first *write '1'* operation the operation sequence *0w0w0r0*. Ldet was varied from 0.1 nm to 5.0 nm, assuming a step of 0.1 nm. Observing this graph, it is possible to see that RS remains almost unaltered until reaching a value of 0.6 nm. However, when Ldet assumes values beyond 0.6 nm, the resistance value of the cell is compromised and RS changes from 1.6 kΩ to nearly 100 kΩ, demonstrating a linear dependency between the two parameters (Ldet and RS). In other words, the variation of Ldet drastically impacts the behavior of the memristor, since it prevents the RRAM cell to store the logic '1' (LRS), putting the cell in a stuck-at-0.

The next two graphs show the relation between Ndiscmax and Ndiscmin with RS. Fig. 6 depicts the RS of the cell when performing the second write operation of the operation sequence *0w1w0r0*, where Ndiscmax varied from 10 to 30 $\times$ $10^{26} m^{-3}$, assuming a increment factor of $1 \times 10^{26} m^{-3}$ during each simulation. The graph shows that RS remains relatively constant, around 52 kΩ, when considering an Ndiscmax below $20 \times 10^{26} m^{-3}$. Note that from $20 \times 10^{26} m^{-3}$ to $22 \times 10^{26} m^{-3}$, the RS gradually decreases until reaching values close to LRS, which means that the cell is going to be stuck-at-1. At this point it is important to recall, observing the graph presented in Fig. 7, that the RRAM cell's correct behavior may only be guaranteed by keeping Ndiscmin smaller than $0.4 \times 10^{26} m^{-3}$,

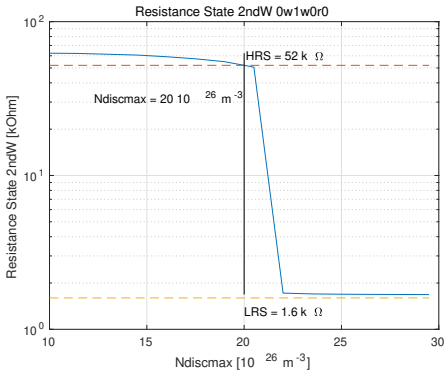

Fig. 6: Resistance observed when performing the second write operation of 0w1w0r0, varying Ndiscmax.

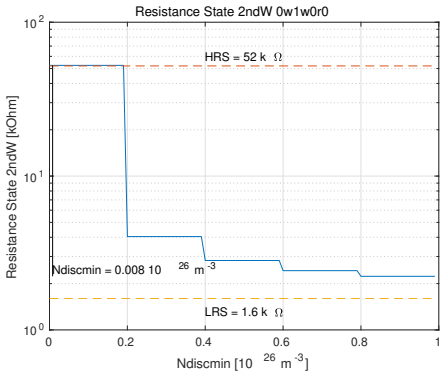

Fig. 7: Resistance observed when performing the second write operation of 1w1w0r0, varying Ndiscmin.

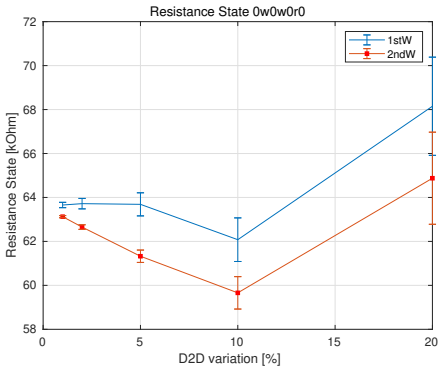

Fig. 8: Error bars related to RS when performing the write operations of the sequence 0w0w0r0.

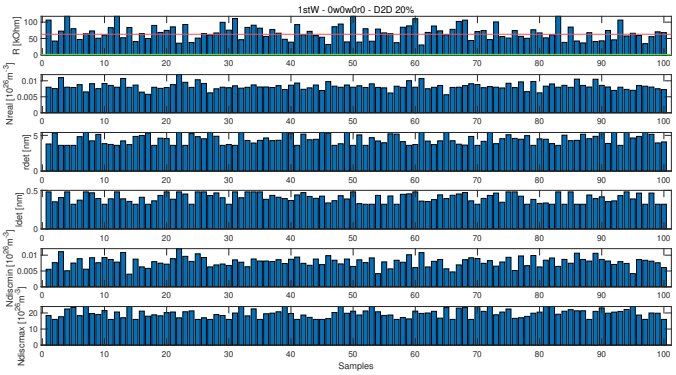

Fig. 9: 20% of variability: RS and Nreal related to all manufacturing parameters when performing the first write operation of 0w0w0r0.

otherwise, the cell remains at LRS or even switches to an undefined state.

C. Evaluating the Impact of Device-to-Device Variations

To evaluate the impact of device-to-device variations, one hundred Monte Carlo simulations, varying the four manufacturing parameters previously described, were performed. The next graphs depict the impact of process variation, assuming a relative strength varied from 1% up to 20%, on the cell's resistance value when performing different operating sequences. The graph depicted in Fig. 8 shows the average variation including error distributions when performing the operating sequence *0w0w0r0*. It demonstrates that the increase of relative strength impacts on the average value of the cell's resistance, being more significant when assuming a variation of 10% and 20% for the manufacturing parameters. In more detail, the average value of RS after performing the first write operation is around 62 kΩ, when considering 10% of variability, and around 68 kΩ when 20%. Further, after the second write operation the average value of RS is reduced from 62 kΩ to around 60 kΩ, when assuming 10 % of variability, and from 68 kΩ to around 65 kΩ when 20%. This particular situation indicate that consecutive write operations, assuming the same logic value, could affect the RRAM cell's functionality. Fig. 9 expands the data shown in Fig. 8 when assuming 20% of variability. In more detail, the bar graphs depict all values of RS, Nreal, Ldet, Rdet, Ndiscmin and Ndiscmax associated to the 100 iterations when performing the first write operation of the sequence *0w0w0r0*. Observing this figure, it is possible to see that RS assumes a value bigger than 100 kΩ in some iterations and in others values around 50 kΩ. However, even when a more relevant impact on the RS is observed, no faulty behavior is observed, since the RRAM cell still stores the logic '0' (Nreal value does not change).

In Fig. 10, when performing a write operation of '0', the average resistances are significantly smaller than the ones observed in Fig. 8. Assuming 20% of variability, the RS average values of the previous case, when performing the first and the second write operation of '0', are around 94% and 85% bigger than the one observed in Fig. 10. Regarding the write operation of '1', the RS values depicted in Fig. 10 indicate that the percentage of variability does not degrade the RRAM cell's capacity of storing LRS. The results depicted in Fig. 11 allow a further investigation regarding the significant reduction of the RS average values when performing the operating sequence of *0w1w0r0*. Observing the values related to RS it is possible to see that in around 50% of the iterations the RRAM cell were not able to switch from '1' to '0', clearly showing a faulty behavior. It is important to point out that functional faults were also observed when percentage of variability was

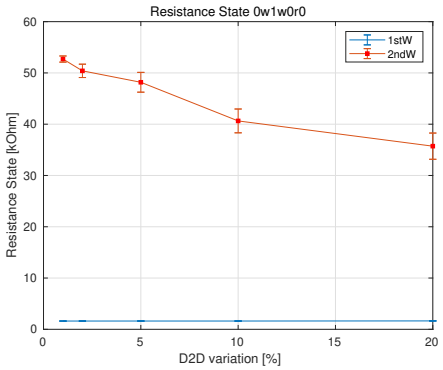

Fig. 10: Error bars related to RS when performing the write operations of the sequence 0w1w0r0.

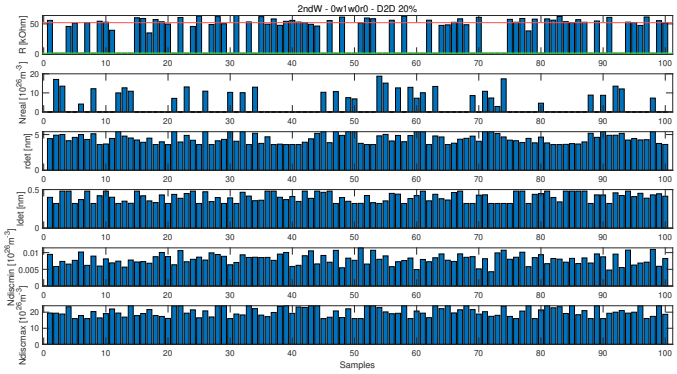

Fig. 11: 20% of variability: RS and Nreal related to all manufacturing parameters when performing the first write operation 0w1w0r0.

set to 2% as well. Finally, the analysis of all obtained results indicates that the impact of process variation is much more significant when trying to execute a *write '0'* operation. This can be justified by the fact that the RESET is more complex than the SET operation, requiring a higher voltage and much more time than the SET.

VI. Final Remarks

This paper aims to evaluate the impact of process variation on a memristor-based crossbar array. The adopted case study was simulated considering two different experiment configurations, one for analysing the impact of varying single manufacturing parameters on RRAM cell functionality, and the other for understanding the impact of device-to-device variation. Observing the obtained results related to the first set of experiments, it is possible to conclude that when the filament length (Ldet) assumes a value above 0.6 nm, a stuck-at-0 will be observed. However, the opposite situation is observed when analysing the results related to varying Rdet. In more detail, low values of the filament radius (Rdet), smaller than 20 nm, cause stuck-at-0 faults. A similar behavior is also observed when varying Ndiscmax and Ndiscmin. From the point of view of device-to-device variation, the obtained results show that transition faults can be observed during the execution of *write '0'* operations, when assuming 2% of variability (Monte Carlo simulations). Note that this particular aspect regarding *write '0'* operations indicates that the a tight manufacturing process control should be adopted, as well as that the circuit design should be optimized in order to improve the RESET operation robustness. Finally, as future work, we foresee (1) a deeper analysis of the obtained results in order to establish a relation between operating sequence and process variation impact, (2) an evaluation of the impact of cycle-to-cycle variations on the RRAMs' functionality, as well as (3) the clear definition of the tolerated manufacturing variability for RRAMs.

References

[1] G. M. Moore, "Cramming more components onto integrated circuits With unit cost," *Electronics*, vol. 38, no. 8, p. 114, 1965.

[2] R. Dennard *et al.*, "Design of Ion-Implanted Small MOSFET ' S Dimensions with Very," *IEEE Journal of Solid State Circuits*, vol. 9, no. 5, pp. 257–268, 1974.

[3] P. Mazumder *et al.*, "Memristors: Devices, models, and applications," in *Proceedings of the IEEE*, vol. 100, Jun. 2012, pp. 1911–1919.

[4] R. Waser *et al.*, "Redox-based resistive switching memories nanoionic mechanisms, prospects, and challenges," *Advanced Materials*, vol. 21, no. 25-26, pp. 2632–2663, 2009.

[5] D. Ielmini *et al.*, "Physics-based modeling approaches of resistive switching devices for memory and in-memory computing applications," *Journal of Computational Electronics*, vol. 16, no. 4, pp. 1121–1143, 2017.

[6] M. Fieback *et al.*, "Testing Resistive Memories: Where are We and What is Missing?" In *2018 IEEE Int. Test Conf.*, IEEE, Oct. 2018, pp. 1–9.

[7] A. Chaudhuri *et al.*, "Fault-Tolerant Neuromorphic Computing," pp. 1–10, 2019.

[8] R. Waser, "Electrochemical and thermochemical memories," in *Technical Digest - International Electron Devices Meeting, IEDM*, 2008.

[9] L. Chua, "Memristor-The missing circuit element," *IEEE Trans. Circuit Theory*, vol. 18, no. 5, pp. 507–519, 1971.

[10] M. Liu *et al.*, "Fault tolerance in neuromorphic computing systems," in *Proceedings of the 24th Asia and South Pacific Design Automation Conference*, ser. ASPDAC '19, Tokyo, Japan: Association for Computing Machinery, 2019, pp. 216–223.

[11] Z. Song *et al.*, "Itt-rna: Imperfection tolerable training for rram-crossbar-based deep neural-network accelerator," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 40, no. 1, pp. 129–142, 2021.

[12] H. Bazzi *et al.*, "Resistive ram set and reset switching voltage evaluation as an entropy source for random number generation," in *2020 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, 2020, pp. 1–4.

[13] S. Balatti *et al.*, "Physical unbiased generation of random numbers with coupled resistive switching devices," *IEEE Transactions on Electron Devices*, vol. 63, no. 5, pp. 2029–2035, 2016.

[14] A. Rukhin *et al.*, "A statistical test suite for random and pseudorandom number generators for cryptographic applications," Booz-allen and hamilton inc mclean va, Tech. Rep., 2001.

[15] H.-S. P. Wong *et al.*, "Metal-Oxide RRAM," *Proc. IEEE*, vol. 100, no. 6, pp. 1951–1970, Jun. 2012.

[16] D. Alfaro Robayo *et al.*, "Endurance Statistical Behavior of Resistive Memories Based on Experimental and Theoretical Investigation," *IEEE Trans. Electron Devices*, vol. 66, no. 8, pp. 3318–3325, Aug. 2019.

[17] W. Zhao *et al.*, "Synchronous Non-Volatile Logic Gate Design Based on Resistive Switching Memories," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 61, no. 2, pp. 443–454, Feb. 2014.

[18] C. Bengel *et al.*, "Variability-Aware Modeling of Filamentary VCM based Bipolar Resistive Switching Cells Using SPICE Level Compact Models," *IEEE Trans. CIRCUITS Syst.*, pp. 1–13, 2020.

[19] *Jart vcm v1b*, http://www.emrl.de/JART.html, Accessed: 2021-04-11.

[20] F. Cüppers *et al.*, "Exploiting the switching dynamics of hfo2-based reram devices for reliable analog memristive behavior," *APL materials*, vol. 7, no. 9, p. 091 105, 2019.