Battery Charger Design for the Columbus MTFF Power System

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A novel pulsewidth-modulated (PWM) dc-dc converter topology is proposed for the battery charge regulator (BCR) of the Columbus Man-Tended Free-Flyer (MTFF) power system. The system is a regulated bus system. Bus voltage control is implemented at the input of the BCR. The use of a conventional buck topology with PWM conductance control at the input results in a second-order behavior. A study of new PWM dc-dc converter topologies has been made to attain a suitable topology. The proposed converter topology is designed and a breadboard including the control loop has been built and tested. The experimental results show that the converter operates according to the design constraints.

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INTRODUCTION

The Columbus Man-Tended Free-Flyer (MTFF) laboratory is a part of the Columbus project of the European Space Agency (ESA). It is mainly an automated, self-contained space station, consisting of two parts.

The resource module will carry all resources and services necessary for its operation, such as power, communications, attitude control, and electrical support systems. The pressurized module will provide the laboratory facility for the material and life science experiments. The Free-Flyer will be able to dock to either the International Space Station or the spacecraft Hermes. Astronauts will then be able to enter the spacecraft and work in the pressurized module.

Since the MTFF will be an autonomous spacecraft, it needs to have an independent power system. A schematic overview of the power system of the Free-Flyer is shown in Fig. 1. Three different sources of power are available: the solar arrays, the nickel-hydrogen batteries, and power supplied via the external input of the system. The energy is distributed to the payloads via a regulated bus. For large systems with many payloads as in the case of the MTFF system, the regulated bus systems is the preferred approach.

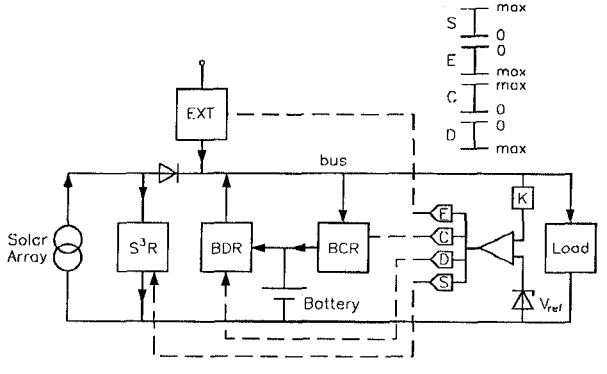

Fig. 1. Power System of the Columbus MTFF.

The method of regulating the power flow from the different energy sources is identified as *domain control*. There are four domains of regulation: (S)hunt, (C)harge, (D)ischarge and (E)xternal power source domain. The main bus voltage of the system is sequentially controlled in one domain at a time. The control system compares the bus voltage to a reference voltage and the resulting error signal determines in which domain the power system will be operating. More information on the power system is found in [1–3].

In the (C)harge domain, the charging of the batteries is controlled depending on the amount of power available from the solar array or an external power source. The battery charge regulator (BCR)

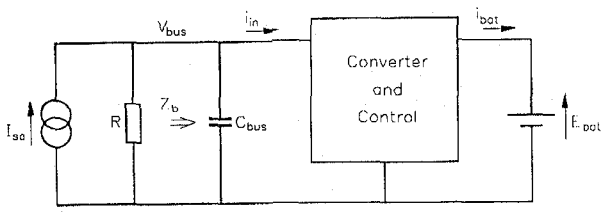

Fig. 2. Simplified system for analysis of BCR application.

directly controls the main bus voltage and at the same time charges the batteries with the surplus of electrical energy available from the solar arrays. The unusual feature of this BCR application is that the bus voltage control has to be applied at what would normally be considered the input port of the regulator.

All four controllers of the various domains regulate the bus voltage by controlling their current. The current is set by the error voltage from the error amplifier. This means that the controllers have a specific conductance. The conductances for the different controllers are made identical to simplify the stabilization of the four different control loops. The same error amplifier can be used for all four controllers.

The preferred method for controlling power regulators used in modern space power systems is pulsewidth modulated (PWM) Conductance Control [4]. This method allows a simple first-order control, perfect current sharing of parallel converters and provides inherent overload protection. To achieve the input conductance control for this application, current sensing is applied to the input port. With proper design of the current loop, the regulator acts like a voltage-controlled current sink, resulting in a first-order control of the bus voltage.

SPECIFIC REQUIREMENTS FOR THE BCR

The BCR of the MTFF power system consists of twelve units connected in parallel. These units are converters with their control loops to convert power from the main bus to the batteries. For the analysis it is not necessary to consider the twelve units in parallel. The BCR application is simplified by reducing it to one unit. This means that the solar array current, load, and bus capacitor are also scaled down. The system of one BCR unit is illustrated in Fig. 2.

The specific requirements for one BCR unit are presented in Table I. These values are presented and explained in [5]. Some of the requirements are standardized by ESA and can be found in [6].

The impedance Z_b of the voltage-regulated bus shall be below the impedance mask as presented in Fig. 3. The maximum impedance is calculated from the constraint that there shall be 1% ac bus voltage variation due to 50% current modulation:

$$Z_{b,\max} = \frac{0.01V_{\text{bus}}}{0.5P_n/V_{\text{bus}}} = 0.02\frac{V_{\text{bus}}^2}{P_n} = 320\ \text{m}\Omega. \quad (1)$$

The frequency range of the bus impedance mask is presented in Table II. The minimum required value for the bus capacitor is

$$C_{b,\min} = \frac{1}{2\pi 10^4 Z_{b,\max}} = 50\ \mu\text{F}. \quad (2)$$

TABLE I
Specific Requirements

Solar array current (I_{SA})	14.5 A
Nominal power (P_n)	900 W
Nominal bus voltage (V_{bus})	120 V
Nominal input current (I_{in})	7.5 A
Nominal load resistance (R)	17.1 Ω
Minimum battery voltage ($E_{bat,min}$)	63 V
Maximum battery voltage ($E_{bat,max}$)	105 V
Maximum battery current ($I_{bat,max}$)	15 A
Maximum battery current ripple ($\Delta I_{bat,max}$)	1.5 A
Required conductance (G)	2.5 S
Switching frequency (f_s)	100 kHz
Minimum efficiency	92%
Bus stability: minimum phase margin	60°
minimum gain margin	10 dB
Maximum bus ripple voltage	0.6 V
Maximum bus spike voltage	2.4 V
Maximum bus impedance ($Z_{b,max}$)	320 mΩ
Minimum bus capacitor	50 μF
Maximum AC bus voltage variations at 50% current modulation	1.2 V

Note: Roman symbols here correspond to italic symbols in text.

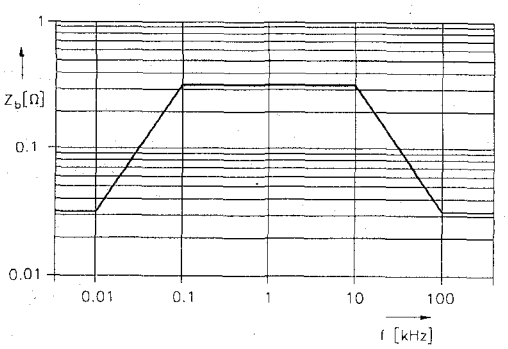

Fig. 3. Bus impedance mask.

TABLE II
Regions of Bus Impedance Mask

0.1 kHz to 10 kHz	$Z_{b,max}$
10 Hz to 100 Hz	effect of integral feedback
10 kHz to 100 kHz	experience and effect of bus capacitor
< 10 Hz > 100 kHz	0.1 $Z_{b,max}$ due to residual resistance

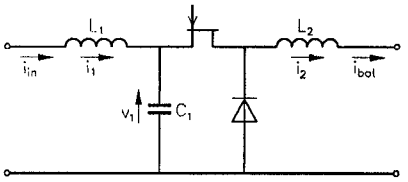

Fig. 4. Buck converter with input filter.

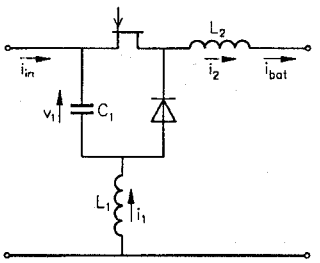

Fig. 5. Novel topology for BCR application.

A NOVEL TOPOLOGY FOR THE BCR

Because the battery voltage is always lower than the bus voltage in this application, a step-down converter must be employed. As input current sensing will be applied to regulate the input current, the input current must be continuous. This suggests the use of a conventional buck converter with an input filter as shown in Fig. 4.

In the next section it will be demonstrated that the small-signal transfer function $H(s)$ of the duty ratio to the input current i_{in} of the applied converter determines the behavior of the control loop (see (10)). It is discussed there that this function should behave as a first-order function for high frequencies, to realize a stable PWM conductance control loop.

The input current i_{in} of the buck converter with input filter flows through the input filter inductor resulting in a second-order behavior of the small-signal transfer function $H(s)$ of the duty ratio d to the input current i_{in} for high frequencies. When applying the buck converter with input filter of Fig. 4 in the BCR application of Fig. 2, this function is found as:

$$H(s)=\frac{I_2\left(\frac{L_2}{R}s+L_2C_bs^2\right)+DV_1\left(\frac{1}{R}+C_bs\right)}{D^2+\frac{D^2L_1+L_2}{R}s+(D^2L_1+L_2)C_bs^2+C_1L_2s^2+\frac{L_1L_2C_1}{R}s^3+L_1L_2C_1C_bs^4} \tag{3}$$

where s is the Laplace operator and D, V_1, I_1, and I_2 are the steady state values of the duty ratio d, the voltage v_1 across capacitor C_1 and the currents i_1 and i_2 through the inductors L_1 and L_2, respectively. This function behaves as a second-order function for high frequencies:

$$H(s\to\infty)=\frac{I_2}{L_1C_1s^2}. \tag{4}$$

This means that the buck converter with input filter cannot be used for this application. The second-order behavior of this function will result in an unstable operation of the PWM conductance control loop (see next section).

A study was performed on the use of new converter topologies for the BCR application [5]. The study proposes to use the novel topology depicted in Fig. 5. The topology of Fig. 5 is similar to the buck converter with input filter, where the input filter inductor L_1 has been relocated to the return line. This topology has been mentioned in the classifications of topologies in [7, 8]. According to [7, 8], the steady state behavior of this topology is the same as that of the buck converter with input filter.

The small-signal transfer function $H(s)$ of the duty ratio d to the input current i_{in} for this topology in the BCR application is found as

$$H(s)=\frac{\frac{D'L_1+L_2}{R}s+[(D'L_1+L_2)C_bs^2]I_2+\left[\left(\frac{1}{R}+C_bs\right)D+\frac{L_1C_1}{R}s^2+L_1C_1C_bs^3\right]V_1}{D^2+\frac{D'^2L_1+L_2}{R}s+(D'^2L_1+L_2)C_bs^2+(L_1+L_2)C_1s^2+\frac{L_1L_2C_1}{R}s^3+L_1L_2C_1C_bs^4} \tag{5}$$

where $D'=1-D$. This function behaves as a first-order function for high frequencies:

$$H(s\to\infty)=\frac{V_1}{L_2s}. \tag{6}$$

The influence of the second-order input filter on the small-signal transfer function $H(s)$ of the duty ratio d to the input current i_{in} is now completely avoided for high frequencies.

Capacitor C_1 is calculated such that the voltage ripple ΔV_1 across the capacitor is not more than 1% of the maximum voltage across it. The voltage V_1 across capacitor C_1 equals the bus voltage V_{bus}. This gives

$$C_1=\frac{I_{bat,max}}{f_S\,\Delta V_{1,max}}D_{min}(1-D_{min})=\frac{15}{100\;10^3\;1.2}0.525(1-0.525)=31\;\mu\text{F} \tag{7}$$

where D_{min} is the minimum duty ratio for the steady state operation:

$$D_{min}=\frac{E_{bat,min}}{V_{bus}}=\frac{63}{120}=0.525. \tag{8}$$

Inductor L_2 is calculated such that the battery current ripple does not exceed the maximum value presented

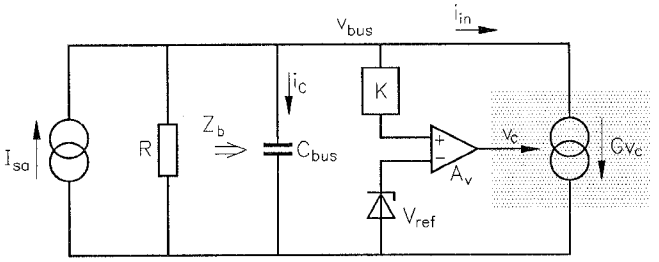

Fig. 6. PWM conductance control for BCR application.

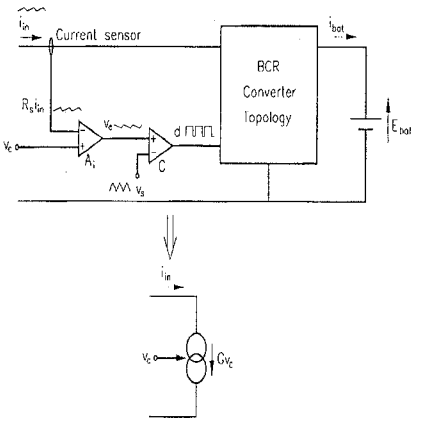

Fig. 7. Current loop for PWM conductance control.

in Table I. This gives

$$L_2 = \frac{V_{\text{bus}}}{f_S \Delta I_{\text{bat,max}}} D_{\min}(1 - D_{\min})$$

$$= \frac{120}{100\ 10^3\ 1.5} 0.525(1 - 0.525)$$

$$= 200\ \mu\text{H}. \tag{9}$$

The input filter inductor L_1 is determined at the end of the next section.

PWM CONDUCTANCE CONTROL FOR THE BCR

PWM conductance control is used by ESA in its space programs for PWM-type regulators [4]. This method is a conventional PWM modulation technique based on the averaged value of the current. The advantages compared with other techniques are its relatively simple design, the noncriticality of components, and the simple conversion to integrated-circuit technology.

The general concept of PWM conductance control is a voltage-controlled current sink which is used to control a desired output function. For the BCR application shown in Fig. 2, the desired output function is the bus voltage v_{bus} as shown in Fig. 6. The unusual feature of this type of control in the BCR application is that what would normally be considered the input port of the regulator is being controlled while the output is supplying energy to the batteries.

The BCR acts as a voltage-controlled current sink with a conductance G. The input current i_{in} of the BCR is adjusted by the control voltage v_c. This is established by a simple voltage feedback loop. The bus voltage is compared with a reference voltage V_{ref} via a voltage divider K. The resulting error signal multiplied by a gain A_v is then employed to adjust the controlled current sink. Thus, the bus voltage is regulated by controlling the current drawn from the bus by the BCR.

This type of control is a first-order control which is very uncomplicated and stable. Another benefit is the ability to employ parallel power stages. The BCR units have the same transconductance and the same control voltage and thus have the same input current. Current sharing is ensured. Another advantage is the system overload protection as a result of the inherent current limitation.

Current Loop

The control loop to convert the BCR converter topology into a controlled current sink is shown in Fig. 7. The input current i_{in} is measured with a current sensor having a characteristic R_s. The output voltage of the current sensor $R_s i_{\text{in}}$ is subtracted from the control voltage v_c and multiplied by a constant amplification A_i. The resulting error signal v_e is compared with a sawtooth voltage v_s. The comparator C provides the duty ratio modulation signal d which drives the active switch of the BCR converter.

The loop gain T_i of the current loop can be found as

$$T_i(s) = \frac{R_s A_i}{V_s} H(s). \tag{10}$$

The function $H(s)$ is the small-signal transfer function of the duty ratio to the input current of the converter, as discussed in the previous section. It is clear that this function depends on the topology used for the BCR. V_s is the peak-to-peak value of the sawtooth voltage.

The transconductance G_i of the current loop is given by

$$G_i(s) = \frac{i_{\text{in}}}{v_c} = \frac{T_i(s)}{R_s(1 + T_i(s))} = \frac{G}{1 + \dfrac{1}{T_i(s)}} \tag{11}$$

where

$$G = \frac{1}{R_s} \tag{12}$$

is the conductance of the regulator. Equation (11) shows that for a large loop gain T_i, the transconductance G_i equals the conductance G while for a small loop gain the transconductance equals G times the loop gain. The behavior of the loop gain is

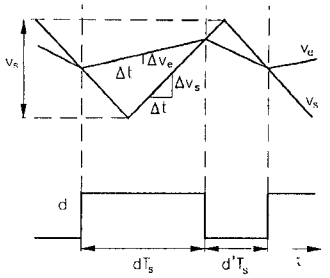

Fig. 8. Signals at inputs and output of comparator.

completely established by the transfer function $H(s)$. To obtain a stable current loop, this function should behave as a first-order system around the bandwidth of the transconductance. The best way to achieve this is to have a transfer function with n poles (the order of the converter) and $n-1$ zeros. The poles and zeros should be located at least one decade below the transconductance bandwidth. The function behaves then as a first-order function for frequencies around the bandwidth and higher, because of the extra pole. The result is a phase margin of almost 90°. As shown by (6), the transfer function $H(s)$ of the topology of Fig. 5 behaves as a first-order function for high frequencies. Applying this topology with the current loop as shown in Fig. 7, the transconductance $G_i(s)$ can be described as a first-order function. Thus the current loop modifies the 4th-order converter topology into a first-order current sink.

When the current amplifier gain A_i is increased, the bandwidth of the current loop increases. However, the amplifier gain is limited and so is the bandwidth. This is due to the fact that the amplifier amplifies the current ripple, resulting in a ripple on the error voltage. Fig. 8 shows the error signal v_e and the sawtooth voltage v_s and the resulting duty ratio signal d. We can see in Fig. 8 that the slew rate of the error signal should not exceed the slew rate of the sawtooth, otherwise the intersection between both signals will be undefined, resulting in unstable operation.

The slew rate of the symmetrical sawtooth signal is

$$\frac{\Delta v_s}{\Delta t} = 2 f_s V_s. \tag{13}$$

The slew rate of the error voltage is

$$\frac{\Delta v_s}{\Delta t} = R_s A_i \frac{\Delta i_{\text{in}}}{\Delta t} \tag{14}$$

where $\Delta i_{\text{in}}/\Delta t$ is the slew rate of the input current. Comparing (13) and (14) results in the maximum value for the current amplification:

$$A_i = \frac{2 f_s V_s}{R_s \dfrac{\Delta i_{\text{in}}}{\Delta t}}. \tag{15}$$

The maximum value is dependent on the worst case slew rate of the input current. In the case of a conventional ramped sawtooth its slew rate would be $f_s V_s$ resulting in a maximum amplification of half the one given by (15). The bandwidth of the current loop is then half of the bandwidth obtained with a symmetrical sawtooth.

The worst case current slope of the input current i_{in} of the novel topology of Fig. 7 is found as

$$\frac{\Delta i_{\text{in}}}{\Delta t} = \frac{\Delta i_2}{\Delta t} - \frac{\Delta i_1}{\Delta t} = \frac{\Delta i_2}{\Delta t} = \frac{E_{\text{bat,max}}}{L_2} \tag{16}$$

since inductor L_1 is a filter inductor having no current ripple and thus the slope of current i_1 is zero. The amplification of the amplifier of the current loop is found with (12), (15), and (16):

$$A_i = \frac{2 f_s V_s}{R_s \dfrac{\Delta i_{\text{in}}}{\Delta t}} = \frac{2 f_s V_s L_2 G}{E_{\text{bat,max}}}$$

$$= \frac{2 \; 100 \; 10^3 \; 5 \; 200 \; 10^{-6} \; 2.5}{105} = 4.76 \tag{17}$$

where the peak-to-peak voltage of the sawtooth signal $V_s = 5$ V. For high frequencies, the transfer function $H(s)$ is approximated by (6). The bandwidth $f_{\text{bw},i}$ of the current loop can be calculated from (6), (10), (11), and (17) as

$$f_{\text{bw},i} = \frac{f_s}{\pi} \frac{V_{\text{bus}}}{E_{\text{bat,max}}} = \frac{100 \; 10^3 \; 120}{\pi 105} = 36.4 \text{ kHz}. \tag{18}$$

An integrator is added to the current amplifier to increase the gain for low frequencies.

Voltage Loop

The voltage loop has already been described at the beginning of this section and is shown in Fig. 6. The voltage loop gain T_v is

$$T_v(s) = \frac{K A_v G R}{1 + s R C_{\text{bus}}}. \tag{19}$$

The voltage amplification K_v is

$$K_v(s) = \frac{v_{\text{bus}}}{V_{\text{ref}}} = \frac{T_v(s)}{K(1 + T_v(s))} = \frac{A_v G R}{1 + K A_v G R + s R C_{\text{bus}}}. \tag{20}$$

Since $K A_v G R$ is usually larger than one, the term of one in (20) can be neglected. This results in

$$K_v(s) = \frac{1/K}{1 + s \dfrac{C_{\text{bus}}}{K A_v G}}. \tag{21}$$

The bandwidth of the voltage loop is

$$f_{\text{bw},v} = \frac{K A_v G}{2 \pi C_{\text{bus}}}. \tag{22}$$

From (21), it follows that the system behaves like a first-order system, provided that the transconductance $G_i(s)$ is constant and can be replaced by G. As (11) shows, this is not the case. To reduce the effect of the pole of the current loop, the bandwidth frequency of the voltage loop should be selected one decade lower than the bandwidth frequency of the current loop.

The input or bus impedance of the regulator is derived from Fig. 6 and (22) as

$$Z_b = \frac{v_{\text{bus}}}{i_c + i_{\text{in}}} = \frac{1}{sC_{\text{bus}} + KA_vG} = \frac{1}{KA_vG} \frac{1}{1 + \dfrac{s}{2\pi f_{\text{bw},v}}}. \tag{23}$$

This impedance should comply with the impedance mask given in Fig. 3. Therefore an integrator is added to the voltage amplifier. This results in a bus impedance of

$$Z_b = \frac{1}{KA_vG} \frac{\dfrac{s}{2\pi f_{zv}}}{\left(\dfrac{s}{2\pi f_{zv}} + 1\right)\left(\dfrac{s}{2\pi f_{\text{bw},v}} + 1\right)} \tag{24}$$

where f_{zv} is the frequency of the integrator zero.

Comparing (24) with the bus impedance mask shown in Fig. 3, it shows that the zero of the integrator must be higher than 100 Hz, the bandwidth of the voltage loop lower than 10 kHz, and:

$$\frac{1}{KA_vG} \leq Z_{b,\max}. \tag{25}$$

This gives the minimum gain of the voltage amplifier as

$$A_v \geq \frac{1}{KZ_{b,\max}G}. \tag{26}$$

The conductance G is provided in Table I. The feedback factor K depends on the reference voltage used. The reference voltage is usually created by a Zener diode. A Zener diode of 6.4 V is used. This gives

$$K = \frac{V_{\text{ref}}}{V_{\text{bus}}} = \frac{6.4}{120} = 0.053. \tag{27}$$

The minimum amplifier gain is then:

$$A_v = \frac{1}{KZ_{b,\max}G} = \frac{1}{0.053\ 0.32\ 2.5} = 23.4. \tag{28}$$

The integrator in the voltage loop improves the static and dynamic response of the system. The steady state error is reduced to zero. The response will be faster for a smaller time constant or a higher frequency of the integrator zero. The frequency of the zero should be a decade lower than the bandwidth frequency of the voltage loop. The effect of the zero on the phase margin is then less than 6°. The minimum phase margin of the voltage loop is given by the design constraints as 60°. When the phase margin is larger, the response of the voltage loop can be made faster by increasing the frequency of the integrator zero until the phase margin reaches 60°.

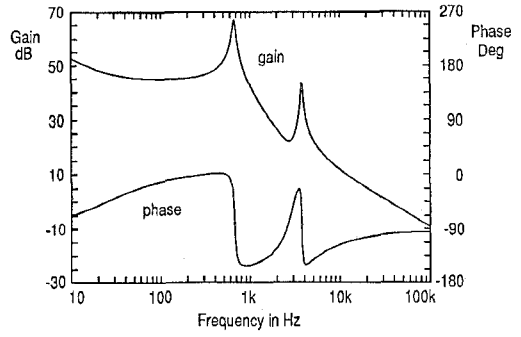

Fig. 9. Simulation of current loop gain T_i.

The bandwidth of the voltage loop is chosen a decade below the bandwidth of the current loop to make sure that the transconductance $G_i(s)$ can be considered ideal for the voltage loop. The bandwidth in combination with (18) is then:

$$f_{\text{bw},v} = \frac{f_{\text{bw},i}}{10} = 3.64 \text{ kHz}. \tag{29}$$

The bus capacitor is calculated from (22), (28), and (29) as

$$C_{\text{bus}} = \frac{KA_vG}{2\pi f_{\text{bw},v}} = \frac{0.053\ 23.4\ 2.5}{2\ \pi\ 3.64\ 10^3} = 135\ \mu\text{F}. \tag{30}$$

This value is a larger value than the minimum required as given in Table I.

Filter inductor L_1 has no current ripple. Therefore its inductance cannot be easily determined as with inductor L_2. The value of the inductance is determined with the use of simulations [9]. Fig. 9 shows a simulation of the current loop gain. The peak in the loop gain at higher frequencies shifts to the right when the inductance of inductor L_1 is decreased. The inductance has been chosen such that this peak occurs at a frequency a decade below the bandwidth of the current loop, so that the phase margin of the current loop gain is not decreased by more than 5°. This resulted in $L_1 = 80\ \mu$F.

EXPERIMENTAL RESULTS

A breadboard of the novel topology including the complete PWM conductance control loop has been built. A metal-oxide semiconductor field effect transistor (MOSFET) of the type IRF 250 is used for the active switch. The passive switch consists of two 1N5826 diodes in series for reasons of redundancy. The solar array is simulated by a High Power Solar Array Simulator from Brentec/Eolas, with a maximum current capability of 10 A. The battery is simulated by a High Power Battery Simulator also from Brentec/Eolas. It can either deliver or sink a maximum current of 20 A for a voltage between 30 V and 100 V. The

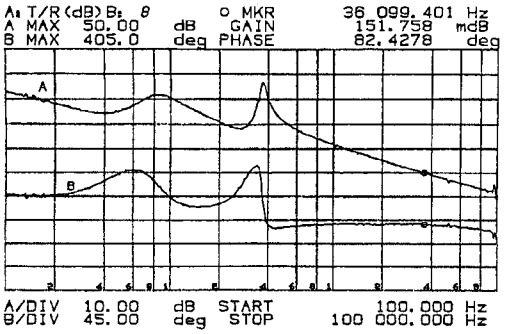

Fig. 10. Current loop gain T_i without integrator (100 Hz ... 100 kHz). Trace A: gain (10 dB/div). Trace B: phase (45°/div).

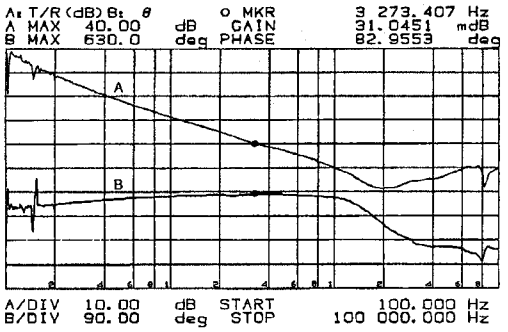

Fig. 11. Voltage loop gain T_v (100 Hz ... 100 kHz). Trace A: gain (10 dB/div). Trace B: phase (90°/div).

bus load is simulated by a Hewlett Packard 6051A electronic load. The measurements are established under nominal conditions. The solar array simulator is set at its maximum of 10 A. The electronic load is set at a resistance of 48 Ω, dissipating a current of 120/48 = 2.5 A. The nominal input current is then 7.5 A.

The bus ripple voltage was measured to be below 10 mV, much lower than specified in Table I. The peak-to-peak spike voltage due to the switching was measured to be around 1 V.

The current and voltage loop gains are measured with a Hewlett Packard 4194A impedance/gain-phase analyzer. They are shown in Figs. 10 and 11.

The current loop response is measured without the integrator at the current amplifier A_i. It appears to be very difficult to measure it with the integrator. The bandwidth of the current loop is the same as the cross-over or 0 dB frequency of the open current loop. The marker in Fig. 10, shows that the bandwidth is 36.1 kHz, which is close to the calculated value of (18). The phase margin is 82.4°.

The voltage loop response in Fig. 11 is measured with the integrators at both the current and the voltage amplifier. The bandwidth is 3.3 kHz, which is lower than the value resulting from (29). The phase margin is 82°, ensuring a stable first-order control.

The bus impedance is measured by applying a sine modulation of 1 A to the load current. The measured impedance is shown in Fig. 12. The impedance mask

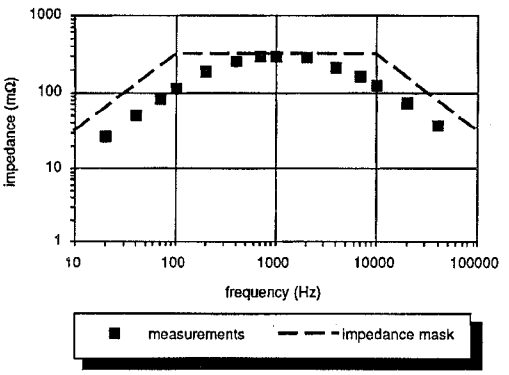

Fig. 12. Measured bus impedance.

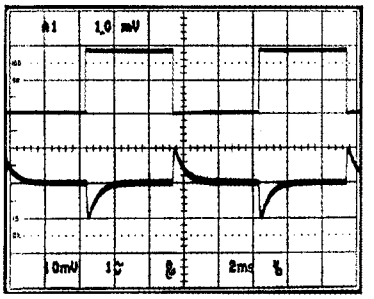

Fig. 13. Measured transient response of bus voltage (time: 2 ms/div). Upper trace: load current (2 A/div). Lower trace: bus voltage (1 V/div).

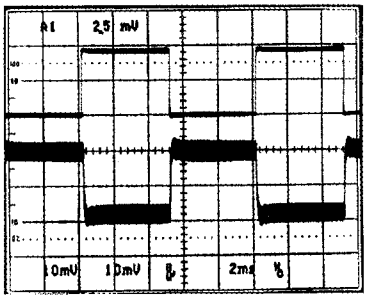

Fig. 14. Measured transient response of input current (time: 2 ms/div). Upper trace: load current (2 A/div). Lower trace: input current (1 V/div).

shown in Fig. 3 is also indicated in Fig. 12. The bus impedance of the regulator stays below the impedance mask. The maximum measured impedance is 310 mΩ.

The responses of some transients in the time domain are shown in Figs. 13 and 14. A 50% current modulation (3.75 A) is applied at the load current with a frequency of 100 Hz. Fig. 13 shows the response of the bus voltage and Fig. 14 shows the response of the input current. The bus voltage variation is 1 V, which is less than 1% of the bus voltage (1.2 V). The responses demonstrate the first-order behavior of the control.

The efficiency of the converter has been measured and is shown in Fig. 15. The efficiency of the converter is higher than the required efficiency of

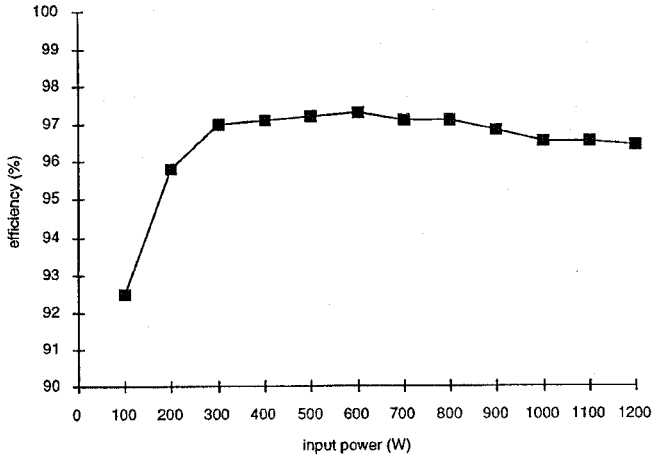

Fig. 15. Measured efficiency.

92%. No snubber circuits for the switches and no additional damping circuits have been used. The power dissipation of the control circuitry has not been taken into account either. The power consumption of the control circuitry is less than 3 W.

CONCLUSIONS

A BCR has been designed and built for the Columbus MTFF power system. Because this application has the unusual feature of input conductance control, a conventional buck converter with an input filter as shown in Fig. 4, could not be used. This resulted in a unstable current loop. A study was made to find an alternative suitable topology which is shown in Fig. 5. This topology is an elementary modification of the buck converter with input filter where the filter inductor is relocated to the return or ground line. PWM conductance control can be applied at the input of the converter. The current loop is stable and the overall behavior of this converter is of the first order.

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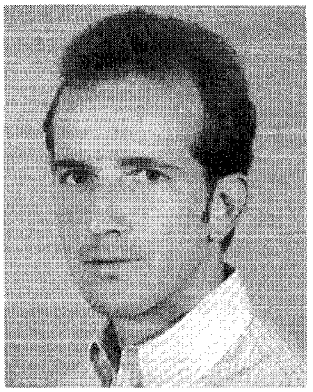

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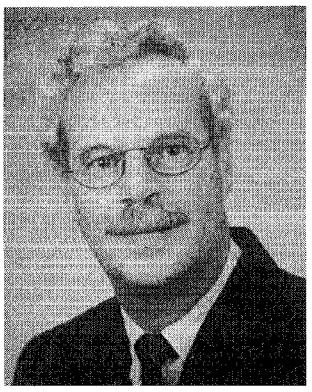
During his study in 1991 and 1992, he worked on the modeling and the application of dc-dc converter topologies in space power systems at the Power and Energy Conversion Division of the European Space Research and Technology Centre (ESTEC), Noordwijk, The Netherlands. Since 1992, he is working as a Ph.D. student at the Laboratory for Power Electronics and Electrical Machines of the Delft University of Technology.



Herman Spruijt was born in Wassenaar, The Netherlands in 1940.

He has worked at the European Space Agency in Noordwijk, The Netherlands since 1966. The first 6 years as a satellite project engineer dealing with the HEOS-1, HEOS-2, GEOS-1 and GEOS-2 scientific satellites. The last 23 years as a power subsystem engineer in the Power & Energy Conversion Division. He is presently involved in the support of the ESA moon program.

He is the holder of two ESA patents. One on the battery charge termination using the TDT (temperature derivative termination). The other one on 16 new dc/dc PWM converter topologies.

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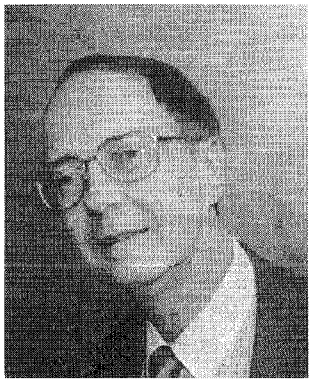

J. Ben Klaassens was born in Assen, The Netherlands in 1942. He received his B.S., M.S., and Ph.D. degrees in electrical engineering from the Delft University of Technology in The Netherlands, where he is currently Associate Professor.

His work has been concerned with inverter circuits, pulsewidth modulation, and the control of electrical machinery. His research work and professional publications are in the area of converter systems with high internal pulse frequencies for sub-megawatt power levels employing thyristors, power transistors and IGBTs. His current interest is in the area of control of converters and electrical drives.

Dr. Klaassens has published a variety of papers on series-resonant converters for low and high power applications. He has designed and built prototypes of the early dc-dc to the recent ac-ac series-resonant converters for a wide variety of applications such as electric motors and generators, communication power supplies, radar signal generators, arc welders, and space applications.