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Multiport Hybrid Converter for Electrified Transportation Systems

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***Abstract*—Compact and efficient power converter solutions are seen to be the backbone of future transportation systems in order to cope with the ongoing transition toward greener systems. Such systems usually comprise a main load section, in which one or more propulsion or traction motors are connected, in addition to an auxiliary load, which might comprise the hotels and air conditioning for example. This auxiliary load can be as low as 5–10% of the main load power. Therefore, it can be challenging to drive this power from a typical high-power system that employs a medium-voltage (MV) dc (MVDC) grid, which is typical in high-power systems. In such MVDC-integrated systems, neutral-point-clamped and active neutral-point-clamped (ANPC) converters are commonly used, where the auxiliary load converter is overrated in this case, resulting in a bulky and inefficient power system. Thus, in order to enable a lighter and efficient transportation power system, a multiport hybrid converter (MHC) is presented in this article. This converter can feed the main MV motor, in addition to two auxiliary low-voltage loads. Compared with the state-of-the-art ANPC converter, the proposed MHC utilizes only two extra switches per phase leg in order to achieve this multiport operation along with increasing the voltage rating of another two switches. The proposed MHC is analyzed in this article, where its operation, modulation, and mathematical derivation are presented. These analyses are supported by simulation and experimental results utilizing a reduced-scale 5-kW system.**

***Index Terms*—Electric vehicle, energy storage, fuel cell, locomotive, low voltage (LV), marine, medium voltage (MV), multilevel, multiport, ships, space vector modulation (SVM), trains, vessels, zero emission.**

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I. Introduction

ENVIRONMENTAL sustainability is representing a significant policy concern nowadays in the different transportation segments. In 2019, this segment has accounted for more than 24% of the global carbon dioxide emissions, and this percentage is expected to significantly increase if no changes are adapted [1]. For example, the global greenhouse gas (GHG) emissions from the shipbuilding industry are predicted to increase from less than 3% nowadays to 17% by 2050 if no changes are adapted [2]. Hence, the International Maritime Organization has imposed a target of 50% reduction in shipbuilding industry's associated GHG emissions by 2050 compared to 2008 [3]. Moreover, around 20% of the railway traffic and 40% of its mainline network are still being served by diesel technology despite the significantly electrified portion of this transportation segment [4]. Such environmental regulations are imposing new and extra requirements and challenges, and as a consequence, zero-emission-based energy sources, such as batteries and hydrogen-fed fuel cells, shall be utilized and are currently gaining higher attention.

Batteries and fuel cells are electric energy sources, where their output is a dc voltage that requires to be regulated in order to meet the load requirements. This is different from the diesel technology, in which an alternator is utilized and the output voltage is ac in this case. In addition to that, batteries and fuel cells introduce direct paths from chemical energy to an electrical one, unlike the diesel technology that goes from chemical energy to an electrical one through thermal and mechanical energy conversions. On the other hand, unlike fuel cells, batteries are commonly used in different transportation systems as a main or auxiliary energy source in hybrid power systems with diesel technology for dynamic support, peak shaving, or spinning reserve [5].

These energy sources are characterized by their dc output voltage, and as a consequence, dc integration schemes are seen to be attractive due to their simplicity and increased efficiency, since a reduced number of power conditioning stages (PCSs) is needed [6]. In addition to that, medium-voltage dc (MVDC) is seen to be efficient and promising in higher power transportation systems despite the main protection challenge in the MVDC integration schemes compared to the ac counterparts. However, these high-power transportation systems still need low-voltage (LV) ac power for the installed auxiliary loads, where the required power is usually a fraction of the installed main power.

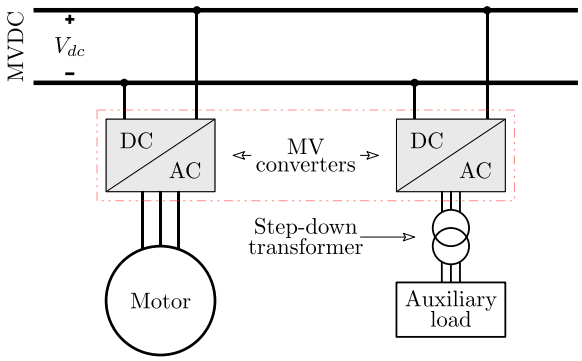

Fig. 1. State-of-the-art simplified configuration for MVDC integration in the high-power transportation system. Note that the power sources are taken out for simplicity.

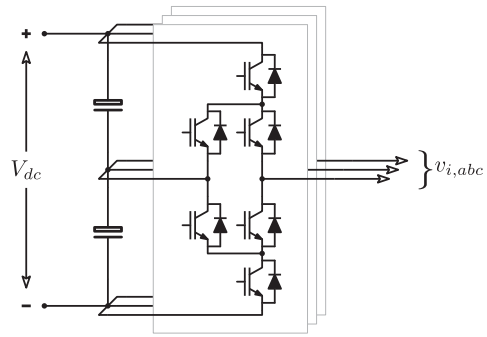

Fig. 2. Three-phase ANPC converter.

This power is typically below 20% of the main load power and can be as low as 5%. As a consequence, an additional MV dc–ac converter shall be utilized with a step-down transformer in order to feed these LV auxiliary loads, as depicted in Fig. 1. This implementation can be challenging if the motor power is in the range of 5–10 MW, while the auxiliary power is lower than 0.5 MW, particularly because an extra MV converter dedicated to this auxiliary load will increase the system footprint and cost.

In such MV systems, multilevel converters are commonly used since they can enable higher voltage and power operation with reduced output filter requirements, where most of these multilevel configurations are reviewed in [7]. Among these multilevel topologies, the three-level configurations are widely used in different renewable energy and transportation systems, where the neutral-point-clamped (NPC) and active neutral-point-clamped (ANPC) topologies are the most common configurations in general motor drive systems, as in the PCS 8000 family from ABB [8], [9]. Note that the equivalent circuit of the three-phase ANPC is shown in Fig. 2.

The three-level ANPC topology has been presented for the first time in [10] as an improved version of the traditional NPC structure in order to balance the loss distribution among the semiconductor switches. These clamping diodes in the conventional NPC converter have been replaced with active switches in the ANPC. This topology has been widely investigated for different applications, such as different transportation systems in [11], [12], and [13], wind power generation in [14], [15], and [16], and general motor drive systems in [17], [18], and [19].

Hence, the ANPC converter is seen as the state-of-the-art candidate for the prior described MVDC-based high-power transportation systems. However, such a solution with dedicated converters for the main and auxiliary loads will constitute a bulky solution since the auxiliary load is a fraction of the main load as explained before. Hence, multiport converters with multiple ac outputs are seen to be attractive in such cases. The commonly used multiport converter, in which more than one ac load can be fed, is the nine-switch inverter (NSI) [20], [21], [22]. This NSI has been studied for different applications, such as power quality improvements in [23], wind power generation in [24], and motor drives systems in [25]. Moreover, the dc-link side of this NSI has been modified in [26] and [27] in order to embrace the boosting capability within the inversion operation. This topology has been further explored in [28] and [29] for MV motor drive systems, where the employed single switches in the conventional NSI have been replaced with a cascaded connection of half-bridge converters.

Although there are extensive studies and evaluations of the multiport NSI in the literature, its MV utilization has been investigated using the cascaded connection of half-bridge circuits, in which high capacitance requirement is the main demerit since single-phase currents will flow in these half-bridges. On the other hand, an extended version of the NSI has been presented in [30] utilizing a T-type module instead of the middle switch, which is called dual-output T-type converter (DO-TC). Over and above that, another extended version of the prior mentioned DO-TC has been proposed in [31] utilizing NPC modules, which is called dual-output neutral-point clamped converter (DO-NPCC). The main challenge behind these two configurations is that the three-level operation is possible only when both the ac loads have the same fundamental frequency and phase. Moreover, the conduction losses are expected to be relatively higher in those topologies since the number of series conducting semiconductor devices during some switching states is three, where two of these devices are rated at half of the dc-link voltage and one is rated at the full dc-link voltage in the DO-TC. On the other hand, balancing the dc-link capacitors is quite challenging in both the DO-TC and the DO-NPCC.

Hence, for the sake of reducing the system footprint, flexible load operation, enhancing the system power conversion efficiency and density, and reducing the number of series conducting semiconductor devices in each switching state, this article proposes a multiport hybrid converter (MHC) for integrating such systems, as shown in Fig. 3. This converter has the following merits.

1) It has an extended structure from the ANPC, where only two extra switches are utilized in each phase leg.
2) It has a simpler structure with reduced footprint and cost compared to the conventional solution, in which two ANPC converters have to be utilized for the main and auxiliary loads.
3) It has a multiport operation with up to three ac ports.

TABLE I
COMPARATIVE ASSESSMENT BETWEEN THE PROPOSED MHC AND THE STATE-OF-THE-ART SOLUTIONS

	Two ANPC converters	DO-TC [30]	DO-NPCC [31]	Proposed MHC
Number of ac loads(1)	2x3L	2x2L(2)	2x2L(2)	2x2L + 1x3L
Number of semiconductor devices	3x2x6=36	3x6=18	3x10+2=32	3x8=24
Device voltage stress	$36x V_{dc}/2$	$12x V_{dc}/2+6x V_{dc}$(3)	$32x V_{dc}/2$	$18 V_{dc}/2+6x V_{dc}$
Maximum number of series switches(4)	2	3	3	2
Cost(5)	High	Low	Medium	Low

(1) 2L and 3L stand for two-level and three-level-operated loads, respectively.
(2) No three-level operation is assumed, where the generic case with different frequencies and phases are considered.
(3) Six devices shall see the whole dc-link voltage while balancing the dc-link capacitors.
(4) The maximum number of series conducting semiconductor devices in a certain switching state.
(5) The cost is an indication of the device count, their voltage class, and associated gate drive circuitries.

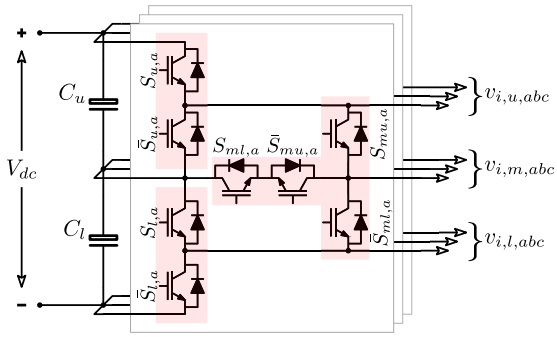

Fig. 3. Proposed three-phase MHC configuration. Note that transformers shall be used with the upper and lower auxiliary outputs according to the system requirements.

On the other hand, two semiconductor devices in each phase leg are rated at the full dc-link voltage.

The rest of this article is organized as follows. Section II describes the structure and operation of the proposed MHC. Then, Section III presents the modulation of the three-phase MHC along with its mathematical derivation. In addition, Section IV presents the obtained simulation results of the proposed MHC using PLECS and considering a reduced-scale three-phase MHC of 5 kW in order to verify its functionality and the reported analysis in the prior sections. Moreover, Section V introduces an experimental validation of the reported simulation results in the previous section. Finally, Section VI concludes this article.

II. STRUCTURE AND OPERATION OF THE PROPOSED MHC

Fig. 3 shows the proposed three-phase MHC structure. As can be seen, this converter can be fed from a single dc source (V_{dc}) and can supply power to three independent ac loads ($v_{i,u,abc}$, $v_{i,m,abc}$, and $v_{i,l,abc}$). These loads are called here: upper auxiliary load $v_{i,u,abc}$, main load $v_{i,m,abc}$, and lower auxiliary load $v_{i,l,abc}$. Note that the upper and lower auxiliary loads can be combined together using line-frequency transformers to feed a single-auxiliary load, which is the case for the considered application in this article.

Compared to the conventional ANPC converter, shown in Fig. 2, the proposed MHC utilizes two extra switches per phase leg in order to obtain the prior described multiport operation. Hence, the total number of semiconductor switches will be less, as shown in Table I, compared to the equivalent state-of-the-art case, in which two ANPC converters shall be utilized to feed two independent ac loads. On the other hand, the proposed MHC shows better characteristics compared to the DO-TC and the DO-NPCC, where the number of semiconductors devices is lower compared to the DO-NPCC. Moreover, compared to the DO-TC and the DO-NPCC, the proposed MHC has three ac ports, where one of them is three-level operated. Finally, the efficiency of the proposed MHC is expected to be higher since less series conducting semiconductor devices are ON during all the switching states.

Each phase leg in the MHC can be seen as a combination of two half-bridge modules and one T-type module, as illustrated in Fig. 3. The upper auxiliary load is fed from the upper dc-link capacitor (C_u) and modulated through $S_{u,x}$ and $\bar{S}_{u,x}$, as illustrated in Fig. 4, where x is a, b, or c, while the lower auxiliary load is fed from the lower dc-link capacitor (C_l) and modulated through $S_{l,x}$ and $\bar{S}_{l,x}$, as illustrated in Fig. 5. This shows that the upper and lower auxiliary loads are two-level modulated utilizing half of the total dc-link voltage (V_{dc}) for each load. On the other hand, the main load is modulated through the T-type module's switches, i.e., using $S_{mu,x}$, $\bar{S}_{mu,x}$, $S_{ml,x}$, and $\bar{S}_{ml,x}$, in combination with $S_{u,x}$, and $\bar{S}_{l,x}$, as illustrated in Fig. 6. Hence, the main load is three-level modulated utilizing the entire dc-link voltage (V_{dc}).

It is worth noting that the main positive state for the main load, as shown in Fig. 6(a), is sharing one switch with the upper positive state for the upper load, as shown in Fig. 4(a). Similarly, the main negative state for the main load, as shown in Fig. 6(c), is sharing one switch with the lower negative state for the lower load, as shown in Fig. 5(b). Hence, the upper negative state for the upper load, as shown in Fig. 4(b), and the lower positive state for the lower load, as shown in Fig. 5(a), have to be placed when the main load is in the main zero state that is shown in Fig. 6(b) in order not to impact its operation. However, the upper positive state for the upper load, as shown in Fig. 4(a), and the lower negative state for the lower load, as shown in Fig. 5(b), can be placed during any of the main load states that are shown in Fig. 6. Finally, it is worth noting the voltage stress across $S_{mu,a}$ and $\bar{S}_{ml,a}$ in Fig. 6(a) and (c), which is equal to the full dc-link voltage.

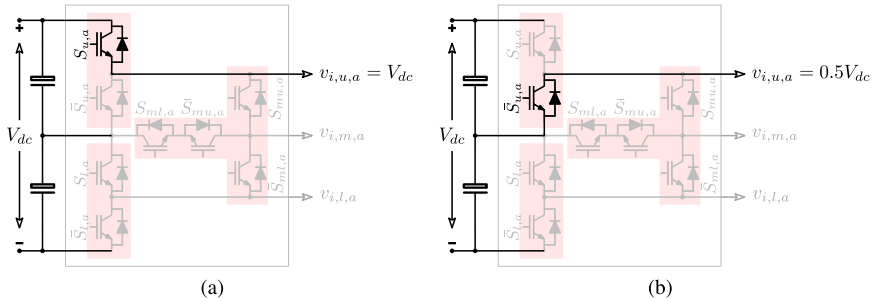

Fig. 4. Switching states of the proposed MHC, considering phase leg a for the upper load. (a) Upper positive state when $S_{u,a}$ is turned ON and $v_{i,u,a} = V_{dc}$. (b) Upper negative state when $\bar{S}_{u,a}$ is turned ON and $v_{i,u,a} = 0.5\,V_{dc}$. Note that the switching states of the remaining switches are not considered in this circuit diagram.

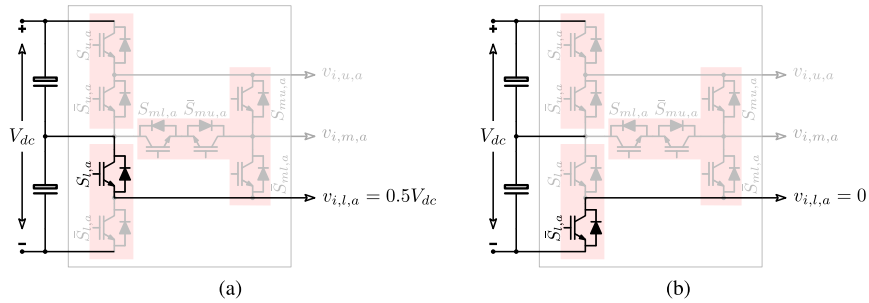

Fig. 5. Switching states of the proposed MHC considering phase leg a for the lower auxiliary load. (a) Lower positive state when $S_{l,a}$ is turned ON and $v_{i,l,a} = 0.5\,V_{dc}$. (b) Lower negative state $\bar{S}_{l,a}$ is turned ON and $v_{i,l,a} = 0$. Note that the switching states of the remaining switches are not considered in this circuit diagram.

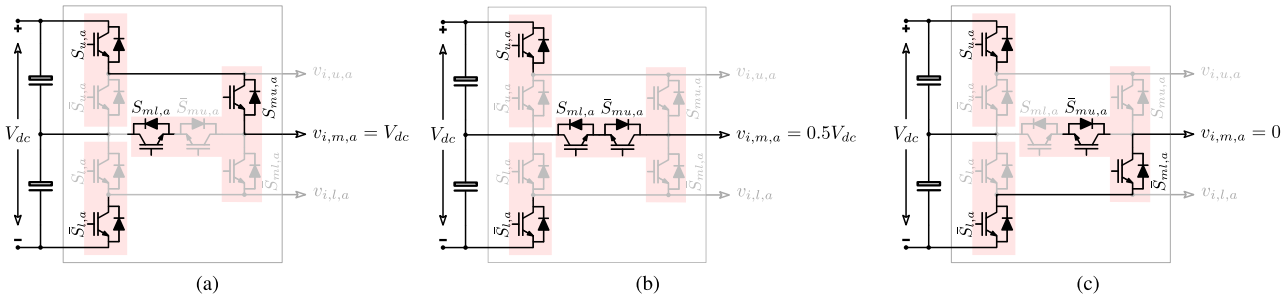

Fig. 6. Switching states of the proposed MHC considering phase a for the main load. (a) Main positive state when $S_{u,a}$ and $S_{mu,a}$ are turned ON and $v_{i,m,a} = V_{dc}$. (b) Main zero state when $S_{ml,a}$ and $S_{mu,a}$ are turned ON and $v_{i,m,a} = 0$. (c) Main negative state when $\bar{S}_{ml,a}$ and $\bar{S}_{l,a}$ are turned ON and $v_{i,m,a} = 0$. Note that the switching states of the remaining switches are randomly shown, where $S_{u,a}$ and $\bar{S}_{l,a}$ are kept ON in order to show that $S_{mu,a}$ and $\bar{S}_{ml,a}$ can see the full dc-link voltage.

III. Modulation and Mathematical Derivation of the Three-Phase MHC

The proposed MHC can be modulated using any of the standard modulation schemes that are suited for the conventional ANPC converter, where two extra sets of reference signals have to be utilized for the upper and lower auxiliary loads, as illustrated in Fig. 7. In this figure, the standard space vector modulation (SVM) reference signals are used for the upper, main, and auxiliary loads.

Note that the reference signals of the upper auxiliary load, i.e., $v^*_{u,abc}$, are placed on top of the reference signals of the main load, i.e., $v^*_{m,abc}$, as shown in Fig. 7. On the other hand, the reference signals of the lower auxiliary load, i.e., $v^*_{l,abc}$, are placed under the reference signals of the main load, i.e., $v^*_{m,abc}$, as shown in Fig. 7. In other words, $v^*_{u,abc}$ are larger than $v^*_{m,abc}$, while $v^*_{l,abc}$ are smaller than $v^*_{m,abc}$ all the time. This is followed and mandatory in any modulation scheme in order to guarantee that $S_{u,x}$ or $S_{l,x}$ is ON whenever needed by the main load, where x is a, b, or c. Hence, when $v^*_{m,abc}$ is larger than $Carrier_u$, $v^*_{u,abc}$ is also larger than $Carrier_u$. Similarly, when $v^*_{m,abc}$ is smaller than $Carrier_l$, $v^*_{l,abc}$ is also smaller than $Carrier_l$, resulting in no impacts on the main load's operation. This has to be maintained in any closed-loop control scheme, where saturation blocks have to be utilized to avoid the intersection of these reference waveforms.

Under the shown SVM scheme in Fig. 7, the three-phase MHC can be modulated as follows: $v^*_{u,abc}$ and $Carrier_u$ are used to modulate $S_{u,x}$ and $\bar{S}_{u,x}$, while $v^*_{l,abc}$ and $Carrier_l$ are used to

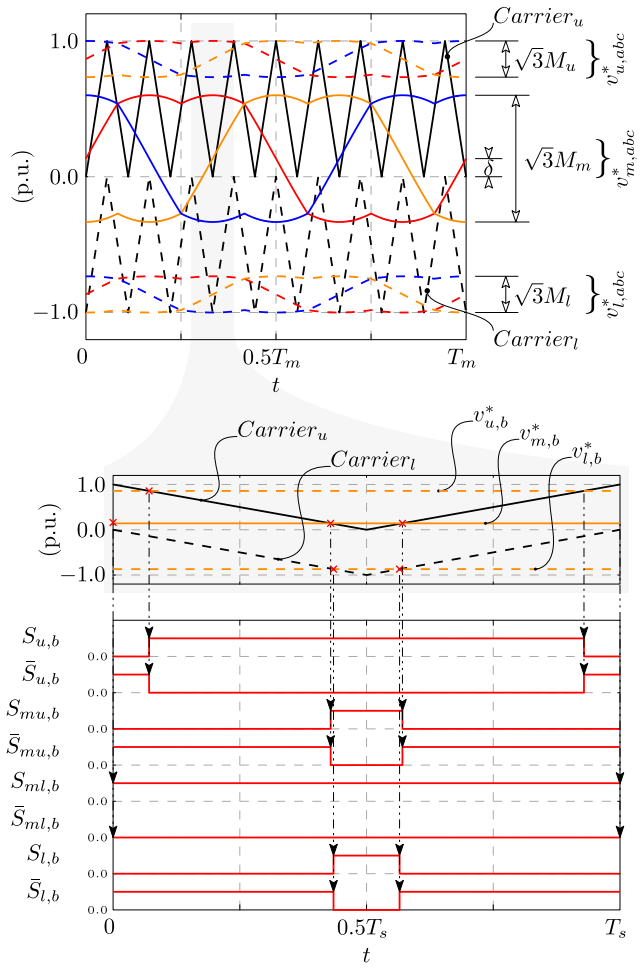

Fig. 7. SVM scheme of the proposed three-phase MHC. Note that this modulation scheme is shown for one fundamental cycle of the main load of time T_m, and the modulation-to-main load frequency index (M_f) is set to 9, which is low for the sake of illustration. Moreover, an approximate zoom for one switching cycle of time T_s is shown, where the reference signals of phase b and the switching states are shown.

modulate $S_{l,x}$ and $\bar{S}_{l,x}$ as follows:

$$S_{u,x} \rightarrow \begin{cases} 1, & v^*_{u,x} \geq Carrier_u \\ 0, & v^*_{u,x} < Carrier_u \end{cases} \tag{1}$$

$$S_{l,x} \rightarrow \begin{cases} 1, & v^*_{l,x} \geq Carrier_l \\ 0, & v^*_{l,x} < Carrier_l \end{cases} \tag{2}$$

where $\bar{S}_{u,x}$ operates in a complementary manner of $S_{u,x}$, while $\bar{S}_{l,x}$ operates in a complementary manner of $S_{l,x}$.

On the other hand, $v^*_{m,abc}$ and $Carrier_u$ are used to modulate $S_{mu,x}$ and $\bar{S}_{mu,x}$, while $v^*_{m,abc}$ and $Carrier_l$ are used to modulate $S_{ml,x}$ and $\bar{S}_{ml,x}$ as follows:

$$S_{mu,x} \rightarrow \begin{cases} 1, & v^*_{m,x} \geq Carrier_u \\ 0, & v^*_{m,x} < Carrier_u \end{cases} \tag{3}$$

$$S_{ml,x} \rightarrow \begin{cases} 1, & v^*_{m,x} \geq Carrier_l \\ 0, & v^*_{m,x} < Carrier_l \end{cases} \tag{4}$$

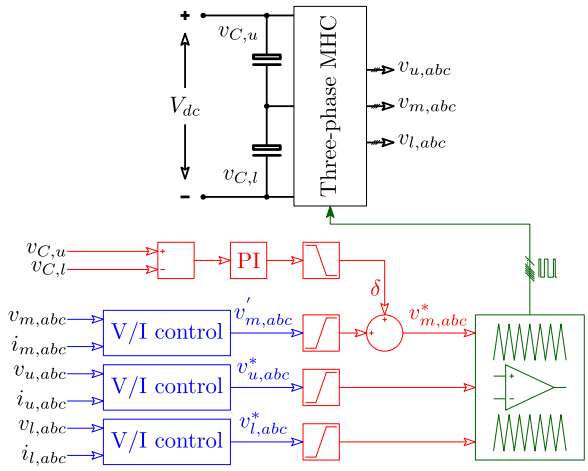

Fig. 8. Simplified schematic diagram showing the PI controller that can be used to balance the voltages across the dc-link capacitors. Note that the V/I control block can utilize any of the possible control schemes based on the targeted application.

where $\bar{S}_{mu,x}$ operates in a complementary manner of $S_{mu,x}$, while $\bar{S}_{ml,x}$ operates in a complementary manner of $S_{ml,x}$.

Utilizing this SVM scheme, the output RMS line-to-line voltages of the three loads can be obtained using

$$V_u = \frac{\sqrt{3}M_u \cdot V_{\text{dc}}}{2\sqrt{2}} \tag{5}$$

$$V_l = \frac{\sqrt{3}M_l \cdot V_{\text{dc}}}{2\sqrt{2}} \tag{6}$$

$$V_m = \frac{\sqrt{3}M_m \cdot V_{\text{dc}}}{2\sqrt{2}} \tag{7}$$

where V_u, V_l, and V_m are the output RMS line-to-line voltages of the upper auxiliary, lower auxiliary, and main loads, respectively. M_u, M_l, and M_m are the modulation indexes of the upper auxiliary, lower auxiliary, and main loads, respectively, that are defined in Fig. 7, while V_{dc} is the dc-link voltage. Note that in order to avoid any disturbance in the MHC operation, which might occur if the reference signals intersect with each other, the following constraint has to be guaranteed:

$$(M_m + M_l + M_u) \leq \frac{2}{\sqrt{3}}. \tag{8}$$

It is worth noting that the auxiliary loads can consume different powers, which results in unbalance between the dc-link capacitors. Hence, a biasing factor (δ) is introduced with the main reference signals ($v^*_{m,abc}$), as shown in Fig. 7, in order to balance the voltages across the dc-link capacitors. This factor can be simply controlled by measuring the voltages of the dc-link capacitors and using a proportional–integral (PI) controller to set its value and equalize the two voltages, as illustrated in Fig. 8.

The prior highlighted constraint of the modulation indexes in (8) shall be modified in case of biasing the main reference waveforms as follows:

$$(M_m + M_l + M_u + 2\delta_{\max}) \leq \frac{2}{\sqrt{3}} \tag{9}$$

TABLE II
PARAMETERS OF THE 5-kW THREE-PHASE MHC

DC-link voltage (V_{dc})	800 V
Upper dc-link capacitance (C_u)	738 μF
Lower dc-link capacitance (C_l)	738 μF
Upper load fundamental frequency	50 Hz
Lower load fundamental frequency	50 Hz
Main load fundamental frequency	50 Hz
Converter switching frequency	18 kHz
Upper load modulation index (M_u)	0.16 p.u.
Lower load modulation index (M_u)	0.16 p.u.
Main load modulation index (M_m)	0.77 p.u.
Upper auxiliary load RMS voltage (V_u)	80 V
Lower auxiliary load RMS voltage (V_l)	80 V
Main load RMS voltage (V_m)	380 V
LCL filters	340 μH, 5 μF, and 340 μH

where δ_{max} is the maximum allowable biasing factor considering a worst-case scenario of unbalance between the auxiliary loads.

Note that this biasing factor is not needed if these auxiliary loads are combined through line-frequency transformers to feed a single load. However, if the auxiliary loads are independent, this biasing factor has to be considered or an external balancing circuit might be needed in case the main load is not working in some specific scenarios.

IV. SIMULATION RESULTS

In order to verify the operation of the proposed MHC, which is shown in Fig. 3, a reduced-scale three-phase model of 5 kW is simulated, where the used parameters are listed in Table II. This converter is fed from a dc source of 800 V and is feeding the three sets of three-phase resistive loads through an LCL filter for each load, where the auxiliary loads are rated 0.27 kW each, and the main load is rated 4.34 kW.

This model has been utilized in order to validate the functionality of the proposed MHC, where the obtained steady-state simulation results are shown in Fig. 9. Note that these results are shown for one fundamental cycle, where the three loads are assumed to have the same fundamental frequency of 50 Hz. In this figure, the voltages and currents before and after the LCL filter of the three loads are shown in Fig. 9(a). In addition, Fig. 9(b) shows the spectrum of the voltages of these loads before the filter.

These results validate the functionality of the proposed MHC. Fig. 9(a) shows that the upper and lower auxiliary loads are two-level operated, while the main load is three-level modulated. On the other hand, Fig. 9(c) shows the currents in the different switches of phase a. This figure shows that the proposed MHC suffers from unequal current stresses among the different switches, where $S_{u,x}$ and $\bar{S}_{l,x}$ suffer the highest stresses since they are common between one of the auxiliary loads and the main load. On the other hand, $\bar{S}_{u,x}$ and $S_{l,x}$ suffer the lowest current stresses since they are feeding only the auxiliary loads, and these loads are assumed to be a fraction of the main one. Hence, different current ratings of the devices can be selected in order to optimize its performance.

It is worth noting that the proposed MHC can operate with different load frequencies as well, where the steady-state simulation results with a 50-Hz fundamental frequency for the auxiliary loads and a 25-Hz fundamental frequency for the main one are shown in Fig. 10. In this figure, the voltages before the filter along with the currents after the filter of the auxiliary and main loads are shown for one fundamental main load cycle.

In addition to the prior results, the switching and conduction losses have been simulated utilizing the loss model of the C3M0120090J SiC MOSFET from Cree, and the obtained losses are shown in Fig. 11. This figure also shows the distribution of the switching and conduction losses among the different switches of phase a, where the conduction losses are the highest in $S_{u,a}$ and $\bar{S}_{l,a}$, and the lowest in $\bar{S}_{u,a}$ and $S_{l,a}$. On the other hand, $S_{mu,a}$ and $\bar{S}_{ml,a}$ suffers the highest switching losses since they are switched ON higher current from the main load, while $\bar{S}_{mu,a}$ and $S_{ml,a}$ suffers the lowest switching losses since they are mostly freewheeling or continuously turned ON under high-power-factor loads. Note that the auxiliary loads are fixed at full load, while the main load is varied.

It is worth noting that the prior shown switching and conduction losses are considered for one case, where the three loads are in phase and having the same frequency. However, since some devices are sharing different loads, the phase of the loads' currents will impact the conversion efficiency, where higher efficiency would occur when the currents are out of phase. On the other hand, this difference in efficiency is not expected to be very high since the auxiliary loads are much smaller than the main one, where less than 0.05% increase in the efficiency can be obtained in this case at full load.

V. EXPERIMENTAL RESULTS

In order to verify the reported analysis and simulation results of the proposed MHC and experimentally test its functionality, the prior simulated 5-kW MHC model is built experimentally, where the same parameters that are reported in Table II are used in this prototype. Fig. 12 shows the MHC prototype, where two three-phase two-level modules are utilized in combination with three single-phase T-type modules to build this three-phase MHC.

Fig. 13 shows the steady-state experimental results under the same conditions as the prior shown simulation results in Fig. 9. In addition to that, a step change in the main load's power is applied, where the load power is increased from 50% to 100% and the obtained results are shown in Fig. 14. On the other hand, Fig. 15 shows the operation of the proposed MHC under different fundamental frequencies, where the upper auxiliary load is operating at 40 Hz, the main load is operating at 100 Hz, and the lower auxiliary load is operating at 60 Hz. Finally, the starting of the converter is presented in Fig. 16. These figures

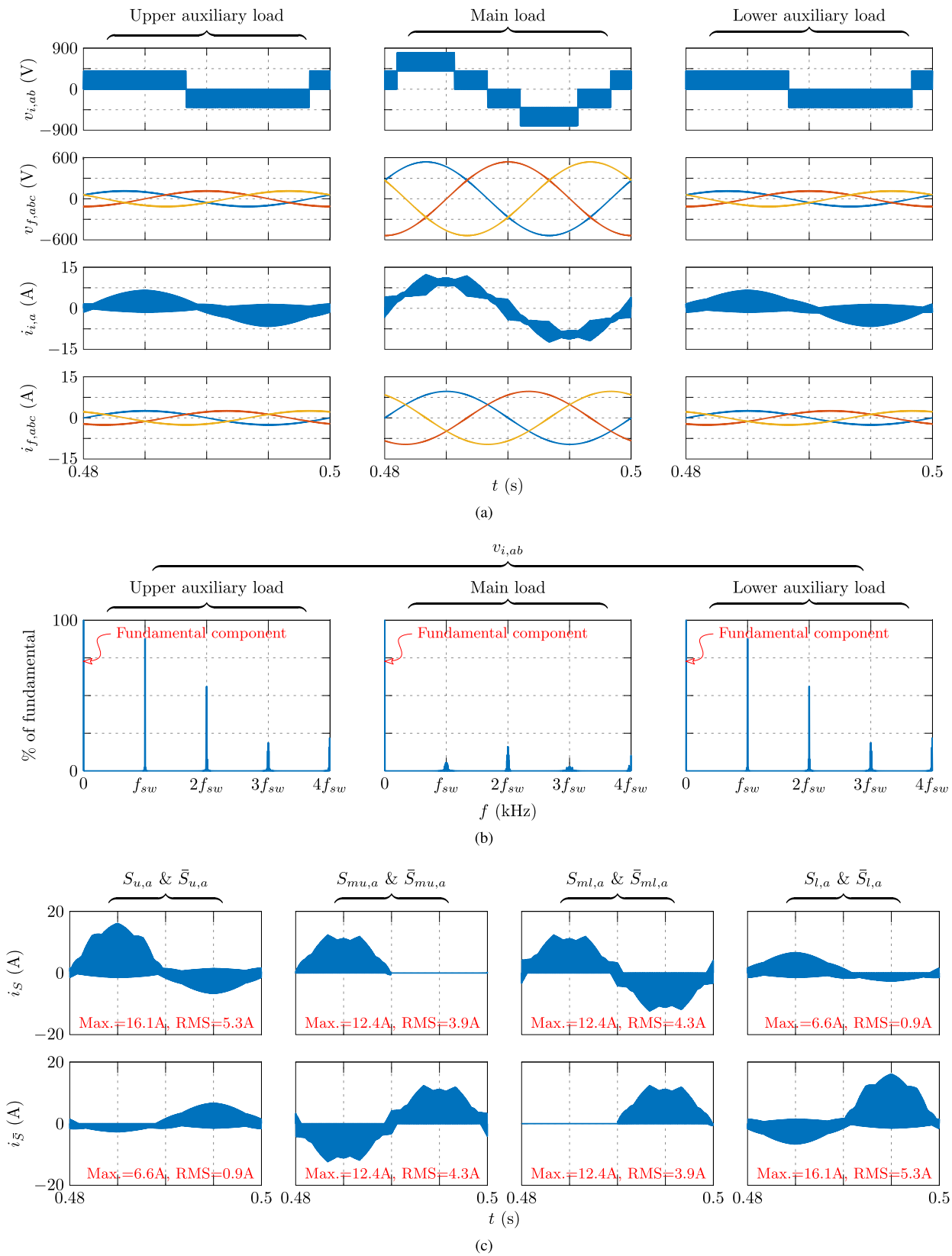

Fig. 9. Obtained steady-state simulation results of the proposed three-phase MHC. (a) Voltages and currents before and after the filter of the auxiliary and main loads for one fundamental cycle of the main load whose fundamental frequency is 50 Hz, where $v_{i,ab}$ is the line-to-line voltage before the filter, $v_{f,abc}$ is the three-phase line-to-line voltage after the LCL filter, $i_{i,a}$ is the line current before the filter, and $i_{f,abc}$ is the three-phase current after the filter. (b) Spectrum of the output line-to-line voltage as a percentage of the fundamental of each load, where f_{sw} is the switching frequency. (c) Currents through the different switches of phase leg a.

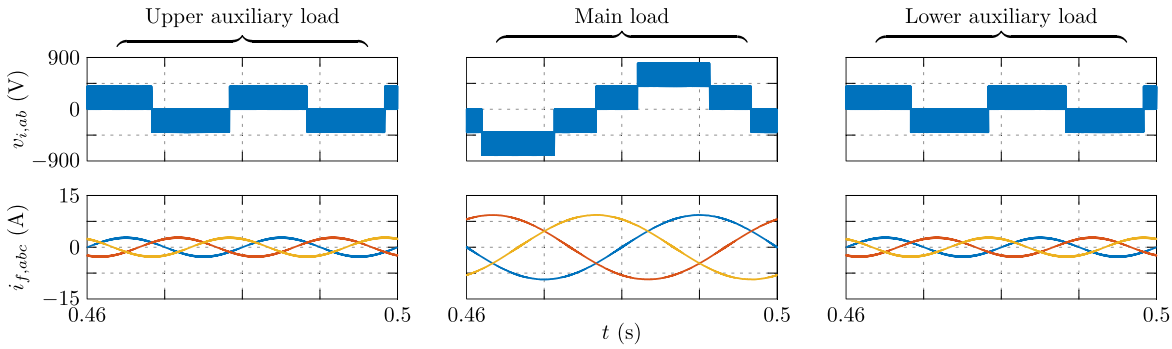

Fig. 10. Obtained steady-state simulation results of the proposed three-phase MHC under different frequency for the main load, where the auxiliary loads are operating at 50 Hz, while the main is operating at 25 Hz. Note that the voltages before the filter along with the currents after the filter of the auxiliary and main loads are shown for one fundamental main load cycle, where $v_{i,ab}$ is the line-to-line voltage before the filter and $i_{f,abc}$ is the three-phase current after the filter.

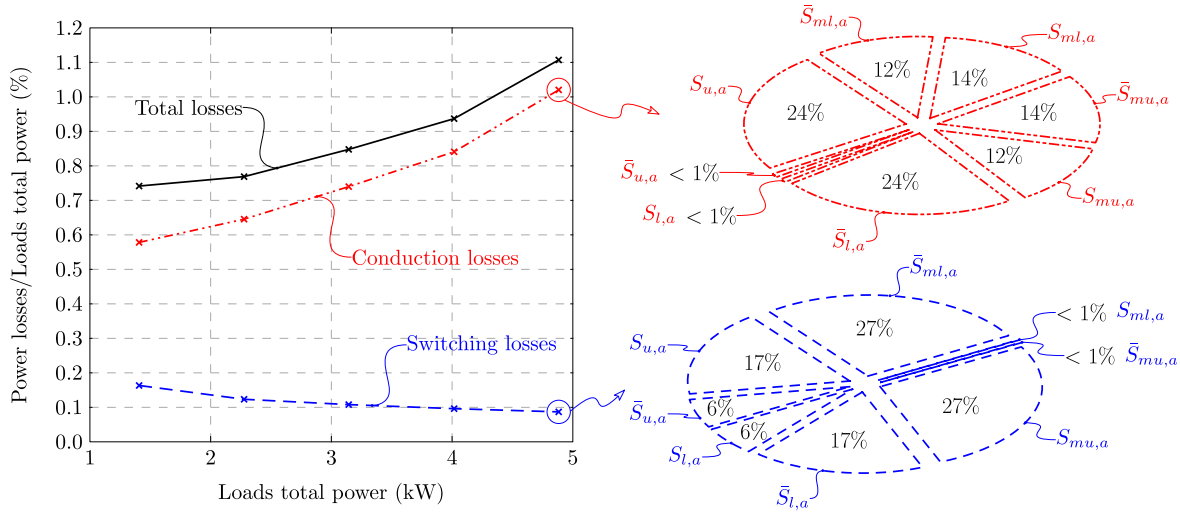

Fig. 11. Simulated switching and conduction losses of the proposed three-phase MHC, where the losses distribution among the different switches of phase leg a is shown for the full-load point. Note that the loss model of the C3M0120090J SiC MOSFET from Cree is used in PLECS to obtain these results.

show the voltage and currents of the three loads before and after the filter for the upper auxiliary and main loads. In addition, the voltage after the filter for the lower auxiliary load is also shown. These results verify the simulation results and prior analysis, which, in turn, validate the functionality of the proposed MHC along with its modulation.

In addition, Fig. 17 shows the measured efficiency of the MHC prototype. The efficiency is measured by fixing the nominal load for the auxiliary outputs and using the main output as a running parameter. This efficiency also includes the losses in the three output filters and parasitics in the whole circuit. As can be seen, a maximum efficiency of 98.22% is obtained, which is in a good agreement with the switching and conduction losses in the semiconductors, LCL filter, and hardware losses.

Finally, the auxiliary outputs can be loaded with different power levels, which will definitely impact the balance of the dc-link capacitors, as shown in Fig. 18. This can be compensated by properly adjusting the parameter δ, which is defined in Fig. 7. In this particular example, as shown in Fig. 18, a step change is applied in δ in order to balance the two dc-link capacitors.

VI. Conclusion

In this article, a three-phase MHC was proposed in order to enhance the system conversion efficiency, footprint, and cost of the state-of-the-art power supply system and future MVDC-integrated systems. This converter can be utilized in transportation systems, especially under higher power requirements, where MV is favored and the auxiliary loads can be as low as 5–10% of the main load power, which is the typical case in large ship vessels in maritime application.

The proposed MHC can feed one main load through a three-level operation, and two auxiliary loads through a two-level operation, where those two main loads can be combined through means of line-frequency transformers. This converter has the following merits: it has a simpler structure with reduced footprint and cost compared to the conventional solution in which two

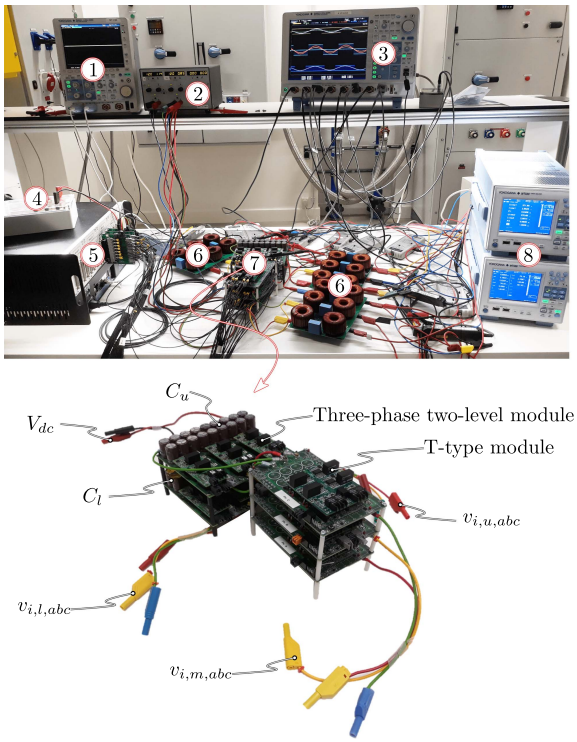

Fig. 12. Three-phase 5-kW MHC prototype. Note that the components in the figure are as follows: ①→Oscilloscope, ②→Gate drives power supply, ③→Oscilloscope, ④→DC power supply terminals, ⑤→Controller, ⑥→Loads' LCL filters, ⑦→MHC, and ⑧→Power analyzers.

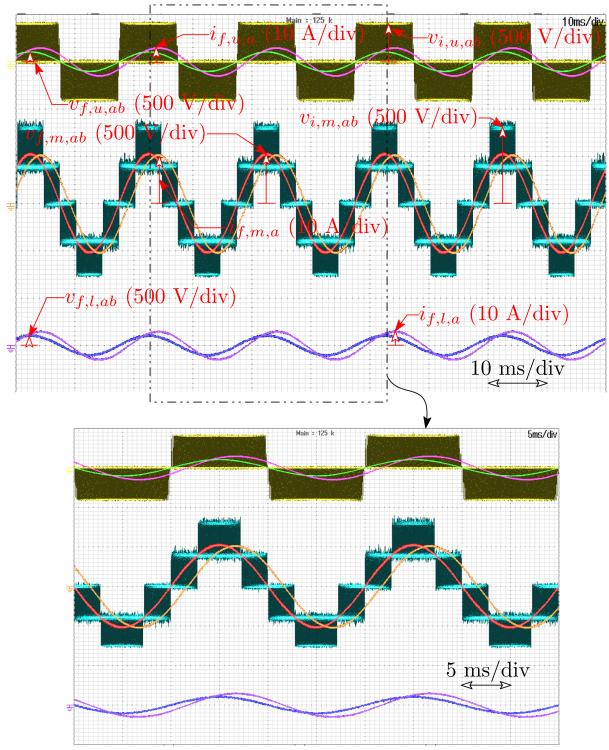

Fig. 13. Steady-state experimental results of the three-phase 5-kW MHC under full-load conditions, in which the voltages and currents of the three loads are shown, with a zoom for one fundamental cycle. Note that the three loads are operating with the same fundamental frequency of 50 Hz.

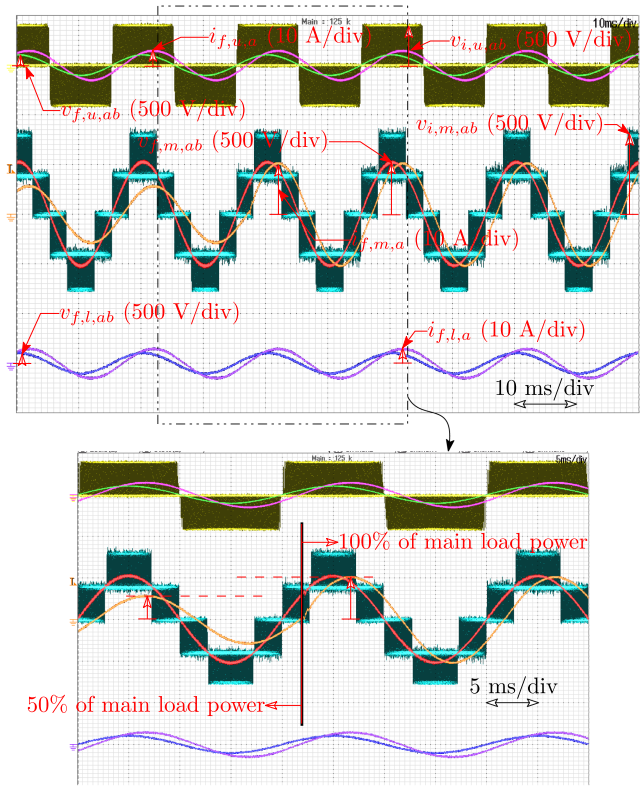

Fig. 14. Steady-state experimental results of the three-phase 5-kW MHC with a step change in the main load power from half-load to full load, in which the voltages and currents of the three loads are shown, with a zoom for one fundamental cycle. Note that the three loads are operating with the same fundamental frequency of 50 Hz.

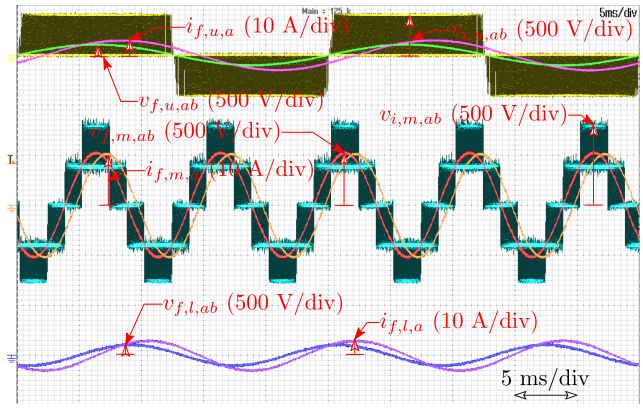

Fig. 15. Steady-state experimental results of the three-phase 5-kW MHC under full-load conditions and different fundamental frequencies, in which the voltages and currents of the three loads are shown. Note that the upper auxiliary load is operating at 40 Hz, the main load is operating at 100 Hz, and the lower auxiliary load is operating at 60 Hz.

ANPC converters have to be utilized for the main and auxiliary loads; it has a multiport operation with up to three ac ports; and it has an extended structure from the ANPC, where two extra switches are utilized in each phase leg. On the other hand, two semiconductor devices in each phase leg are rated at the full dc-link voltage. It is worth noting that the presented converter can be widely utilized in different applications where different loads exist and compact solutions are needed.

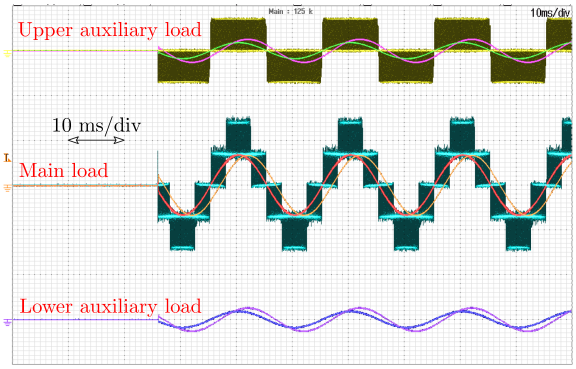

Fig. 16. Experimental results of the three-phase 5-kW MHC during starting-up, in which the voltages and currents of the three loads are shown. Note that the three loads are operating with the same fundamental frequency of 50 Hz.

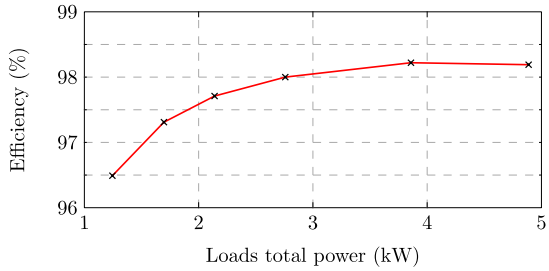

Fig. 17. Experimental efficiency of the three-phase 5-kW MHC. Note that the power of the auxiliary loads is fixed at their rated powers, while the main load power is changed to obtain this efficiency curve.

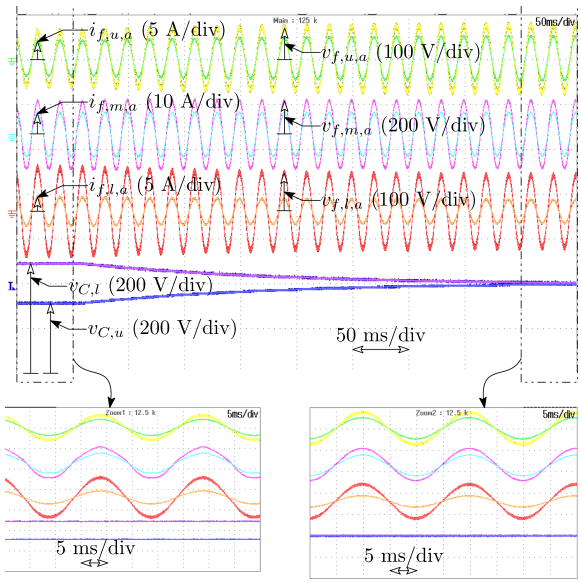

Fig. 18. Applying different auxiliary loads and introducing a step change in the δ parameter, which is defined in Fig. 7, in order to balance the dc-link capacitors' voltages. Note that the three loads are operating with the same fundamental frequency of 50 Hz.

In this article, the basic operation of the proposed three-phase MHC was presented and analyzed, showing the different switching states of the converter. Moreover, the modulation of the proposed converter was presented, where the standard SVM was used with the different loads. In this modulation, a biasing factor with the reference signals of the main load was presented in order to balance the dc-link capacitors. Finally, simulation and experimental results considering a 5-kW three-phase MHC model and prototype were presented, where a peak efficiency of 98.22% was achieved.

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