Power-efficient, Precise Discriminator for a High Time Resolution, Low-Noise Charge Detection ROIC

by

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Abstract

Pixel charge detectors are responsible for counting the number of collected electrons and converting it into an electrical signal. The proposed charge detector pixel readout integrated circuit (ROIC), implemented in 40nm TSMC technology, should be able to detect an amount of charge as low as 160aC, with a high time resolution of 2.5ns, using limited power consumption and area occupation. The discriminator, as the ROIC's last block, should distinguish the analog information of the previous block called "signal shaper", from a certain noise level, and convert it into 1-bit binary code. The mode of operation is named as an event counting.

In this thesis, two versions of the discriminator are studied and compared: with an active and passive shaper (filter). The goal is to find the optimal solution with respect to performance and power efficiency. The discriminator with an active filter (which provides an output pulse with an amplitude of 225mV and power consumption of 170μW, achieves an offset of 5mV and a noise voltage of 290$\mu Vrms$ referred to the input, and consumes a power of 36μW. Its speed performance and temperature stability have been experimentally verified. The discriminator with a passive shaper (which consumes no power) can detect an input signal with 10mV amplitude, with 240$\mu Vrms$ input noise, and a power consumption of 88μW. Its performance is partly tested through the post-layout simulation.

The achieved SNR with the active filter is 14.6, and the passive filter is 15.1. Both solutions (discriminator for active and passive filter) demonstrate an acceptable SNR. The solution with a passive filter provides a better overall power efficiency but cannot detect incoming events during the calibration period which lasts 10ns and occurs every 90μs.

Contents

1 Introduction

1.1. Application Background

In order to observe and analyze items with higher resolution, various imaging instruments have been invented. The scanning electron microscope (SEM) is an instrument that produces images of the surface of the specimen with nanometer resolution [3]. The basic configuration of SEM usually involves a vacuum system, an electron beam generator, and an electron detector (as shown in Fig.1.1). A focused beam of energetic electrons produced by the electron beam generator will be launched onto the surface of the specimen. During the interaction, the energy of the beam electrons will be transferred to specimen atoms. Then backscattered electrons (BSEs) and secondary electrons (SEs) will be generated due to a series of scattering reactions [3]. BSEs originate from deeper regions of the specimen, while SEs provide more detailed surface information [15].

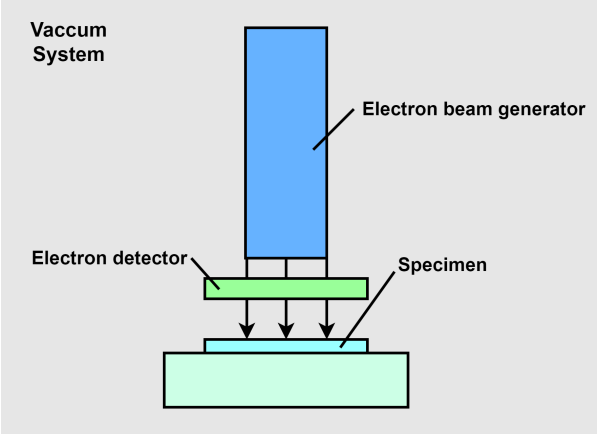


Figure 1.1: Basic configuration of SEM

The electron detector, as a key part of the SEM, will collect and process the signals coming from the specimen. By counting the number of collected electrons and converting them into electrical signals, images will be created [3]. For this project, semiconductor PIN diodes are used as electron detectors for SEM. They could be fabricated and integrated with existing CMOS technology [6]. When the PIN diode is in zero-biased condition, a space-charge region will be formed at the interface of the n-type region and the intrinsic region. Electron-hole pairs will be generated in the intrinsic region once electrons in the beam with enough energy (should be higher than the bandgap of diode material) interact with the diode. Under the application of the reverse-biased electric field, the newly generated free charge carriers in the intrinsic region will be moved towards the electrodes, which induces a current flowing from the n-type to the p-type region of the diode and the junction capacitor of the diode detector will be charged (as shown in Figure.1.2 (a)). Figure.1.2 (b) shows the equivalent circuit model of the reverse-biased diode, where the current source I_s represents the generated electron-hole pairs induced current and the

capacitor C_d represents the depletion capacitor. The following readout integrated circuit (ROIC) will

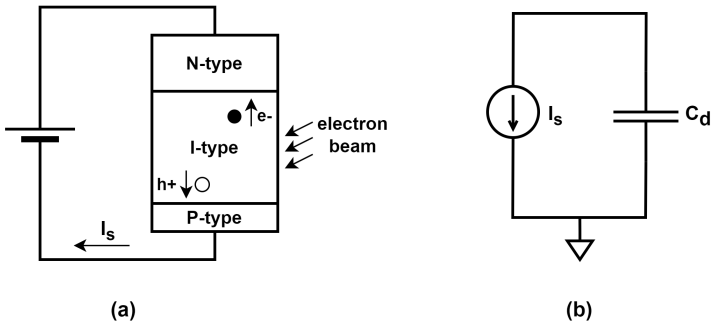


Figure 1.2: (a) Diode configuration and (b) equivalent circuit model

further process the signal and finally convert it into digital binary code. This project focused on the analog ROIC of the electron detector interface.

1.2. Characteristics of Charge Detection ROIC

The physical properties of semiconductor materials and the application requirements of the SEM put high demands on the design specification for the detector ROIC. To improve the SNR of the ROIC and to improve the counting capability, the charge detector surface is divided into pixels each with a micrometer-level size, as shown in Fig.1.3 [17]. To ensure accurate electron detection, the sampling rate

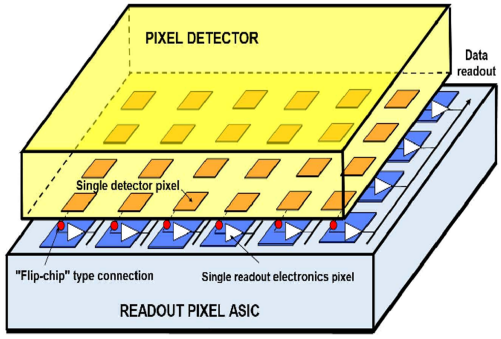


Figure 1.3: Hybrid pixel detector[5]

of the detector should be high enough that as many electron arrival events can be captured effectively [17]. For this project, the detection sampling rate is set to $400MHz$, which corresponds to a clock period of $2.5ns$. This means that the electron arrival event is assigned to a time interval of $2.5ns$.

Only electron-hole pairs generated in the depletion region of the diode can be collected and contribute to the effective current signal. Each hit will lead to a generated charge of $160aC$ (equivalent to $1000e^-$). Transit time t_c is the time the generated carriers take to move between the electrodes of the PIN diode detector under the applied electric field. It is related to the mobility of the charge carriers μ, the electric field due to the applied reverse biasing E, and the width of the diode's depletion region W_{dep} as expressed by Eq.1.1. For this project, the transit time t_c is set to $1.8ns$.

$$t_c = \frac{W_{dep}}{v_d} = \frac{W_{dep}}{\mu \cdot E} \tag{1.1}$$

The properties of the diode detector used for this project are shown in Table.1.1.

Based on the discussion about the characteristics of the semiconductor diode detector, the essential performance specifications for the ROIC are a high count rate, high accuracy with a small size as well as a low power consumption per pixel. The target specifications for the detector readout pixel ASIC are summarized in Table.1.2.

For this project, two assumptions are made regarding the behaviors of incoming electrons:

Table 1.1: Diode characteristics

Specification	Target
Carrier transit time t_c	$1.8ns$
Collected charge Q_c	$160aC(1000e-)$
Equivalent diode capacitance C_d	$50fF$

Table 1.2: Readout pixel ASIC target specification

Specification	Target
Pixel Size	$0.04mm^2$
Max.Event Rate	$4 \times 10^8 Events/s$
Time Resolution	$2.5ns$
Power Consumption Budget	$0.35mW$/Pixel
Detection Error Rate	$< 2\%$

- One pixel would only be hit by a maximum of 1 electron in every $2.5ns$;
- One pixel will be hit by 1 electron in a maximum of 3 consecutive time frames;

1.3. Motivation

The ROIC for SEM is designed to detect small amounts of charge, equivalent to one electron penetrating in the diode detector, with high time resolution as well as with limited area and power budget. How to guarantee the readout accuracy is the principal consideration for the ROIC design. Thus, the architecture and design specifications should be set carefully.

In this project, the reverse-biased diode detector is modeled as a current source I_s paralleled with a capacitor C_d, as shown in Fig.1.2 (b). The current I_s is a pulse signal representing the detection of charge carriers in the depletion region when an energy beam is incoming. The amplitude of the current pulse is determined by the collected charge Q_c and carrier transit time t_c based on Eq.1.2.

$$I_s = \frac{Q_c}{t_c} = \frac{160aC}{1.8ns} = 89nA \tag{1.2}$$

The capacitor C_d represents the depletion capacitance of the diode. For this project, it is set to $50fF$.

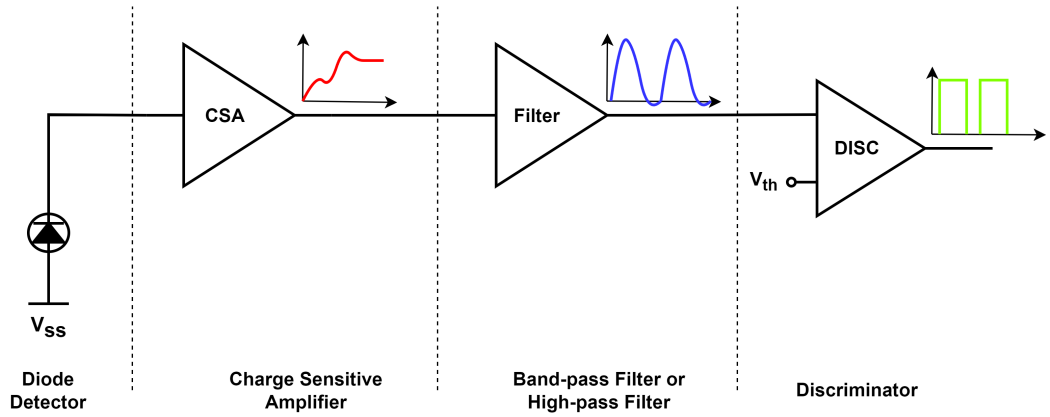


Figure 1.4: Proposed electron detector ROIC [22]

The proposed ROIC, as illustrated in Fig.1.4, has the following functional blocks: a charge-sensitive amplifier (CSA), followed by a band-pass filter (BPF) or a high-pass filter (HPF), and a discriminator (DISC). The CSA keeps ideally the detector diode in the short-circuit mode with respect to the signal pulse, and converts every current pulse of the diode into a voltage signal. It is designed to reduce the noise level through limited bandwidth. This, however, leads to a pileup of signals at the output (shown in Fig.1.5), known as inter-symbol interference (ISI) [2]. The detailed performance of the CSA is reported

in [22]. The task of the following BPF or HPF is to reduce the ISI-induced errors by shortening the time width of the signal in order to guarantee detection accuracy. Finally, the discriminator converts the analog signal coming out of the filter into a digital pulse signal with a voltage level of $1.1V$.

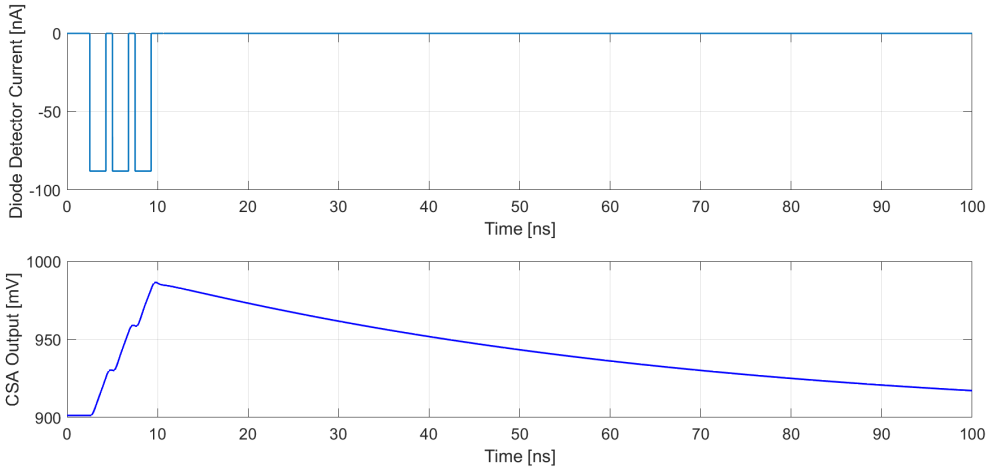


Figure 1.5: Signal pile-up at the CSA's output when responses to 3 continuous events

Based on the description in Section.1.2, the detector is segmented of a number of pixels. Thus, the power budget of each pixel should be limited. The CSA, as the first block, is the bottleneck for the ROIC design. The power consumption of the reported CSA takes 50% of the budget. Thus, the limited power budget for the remaining blocks in the ROIC would be a challenge.

The filter should be able to eliminate the signal pile-up at the CSA's output by attenuating the low-frequency band. There are two solutions to realize the desired filter. One method, named the "active filter", is by building an amplifier with feedback that achieves a band-pass frequency response. The other method, named the "passive filter", is composed of a capacitor and resistor. The advantage of the active filter is that a gain could be realized in the band of interest, which relaxes the requirements of the discriminator. However, unlike the passive filter, the active filter unavoidably consumes additional power. On the other hand, the passive filter, not only does not amplify the signal, but causes its attenuation. This poses a challenge for the discriminator design and leads to a more power-hungry solution.

One of the goals of this thesis project is to analyze the different design specifications of the discriminator for ROIC with an active or a passive filter. Another goal is to design two power-efficient discriminators that could precisely digitize the analog signal from the previous block, the active or passive filter, within every $2.5ns$, for an electron detector ROIC in $40nm$ CMOS technology. The performance of the discriminator with active or passive filter, as well as the ROIC, will be compared at the end of the thesis.

1.4. Thesis Organization

The main task of this project focused on the discriminator design and verification. In this thesis, other blocks in the ROIC will also be introduced in order to provide a complete view. The discriminator with active filter has been taped out and experimentally qualified. While the discriminator with passive filter is tested at the simulation level. The thesis is organized as follows. Chapter 1 gives a brief introduction to the application background and proposes the motivation for discriminator design. Chapter 2 presents the architecture of the ROIC with active or passive filter, and emphasizes on the filter and discriminator block. In Chapter 3, each block's transistor-level circuit implementation and the achieved performance are presented. Chapter 4 provides the testbench design and measurement setup for the discriminator with active filter. The performance of the two proposed discriminators with active or passive filter is presented in this chapter. A comparison is discussed in Chapter 5. The thesis ends with conclusions.

2

Discriminator Design Requirements with Active and Passive Filter

Design considerations and specifications are discussed in this chapter. This chapter begins by introducing characteristics of the active filter and the discriminator in Section 2.1. Threshold selection topology is described in this section. Then, the ROIC with a passive filter is presented in Section 2.2. In this section, the passive filter is proposed and challenges towards the discriminator with passive filter are analyzed. Design parameter selection for the passive filter is discussed in Section.2.2.1. Detailed methodology for designing a pre-amplifier with input offset cancellation technique as the gain stage for the proposed discriminator is presented in Section.2.2.2. This chapter ends with a summary of design specifications for discriminator with active and passive filter.

2.1. ROIC with Active Filter

The diagram of the proposed ROIC with an active filter is shown in Fig.2.1.

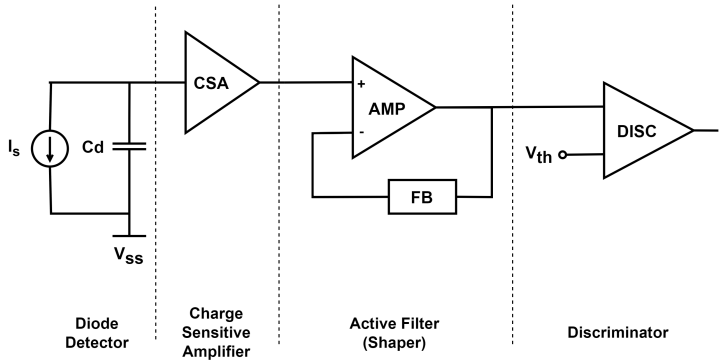


Figure 2.1: Proposed ROIC with active filter

2.1.1. Active Filter

The design of the active filter is not included in the work of this thesis project. Detailed implementation and performance of the active filter are reported in [9]. This section will briefly describe its characteristics to provide a background for the discriminator design.

The active filter is composed of an amplifier with feedback. The amplifier in the forward path has a wide bandwidth and the feedback path has an attenuation in the low-frequency band. They together lead to a band-pass filter whose transfer function is shown in Fig.2.2.

Post-layout simulation shows the active filter consumes $125\mu W$. So the remaining power budget for the last block in the ROIC, the discriminator, is $50\mu W$. When reacting to a single input event, it generates an output signal with an amplitude of $225mV$ and time width of $3ns$, as shown in Fig.2.3. The active

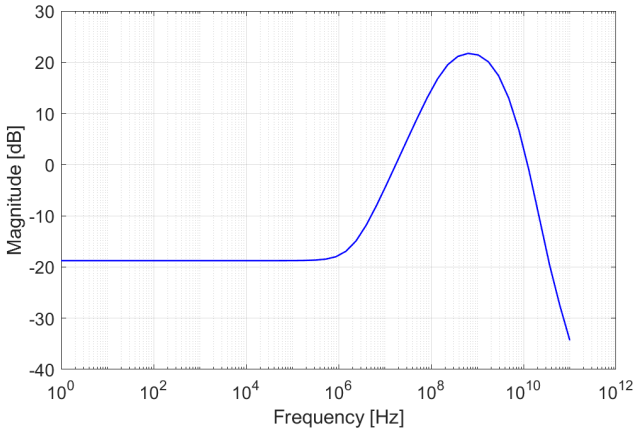


Figure 2.2: Frequency response of the active filter

filter's response for three continuous input events is shown in Fig.2.4. The noise voltage $\sigma_{n,rms}$ referred to the output is $15mV$. Monte-Carlo simulation shows that it has an output-referred offset of $18.9mV$.

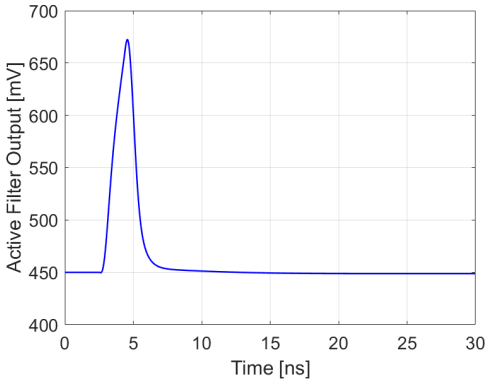


Figure 2.3: Active filter's transient response for single input event

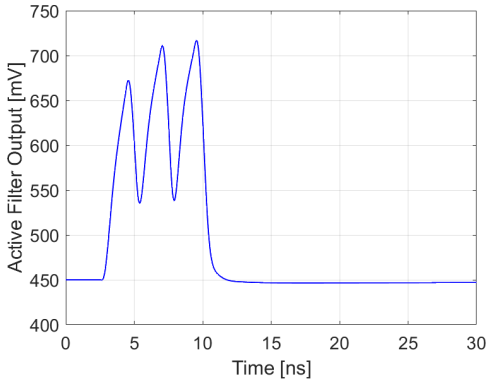


Figure 2.4: Active filter's transient response for '111' pattern

2.1.2. Basic Discriminator

The common structure for the discriminator may include 1) high-gain amplifier with differential input and single-ended output, or 2) differential input pair with a latched load. They can be classified as 1) the continuous-time discriminator, or 2) the dynamic discriminator, depending on if sampling is involved during signal processing. Dynamic discriminators usually have lower power consumption and higher operation speed. However, for the targeted electron detection ROIC design, using the dynamic discriminator could lead to a rise in detection error rate due to the asynchronous sampling [8]. While the continuous-time discriminator, which reacts to any occurrence moment of the events, is the better solution for this application.

The proposed discriminator has a gain stage and a decision stage, as shown in Fig.2.5. The gain stage is an amplifier with differential analog input and single-ended output. The signal coming out of the filter is compared with a specific DC voltage level, which is defined as the threshold of the discriminator. The difference between them is amplified and sent to the decision stage to consolidate the logic levels. Besides, the differential amplifier is chosen for the gain stage because it could usually better reject the noise from the supply source than the amplifier with single-ended configuration[14]. Considering the speed, power and area aspect, an implementation as simple as two series inverters is chosen for the decision stage.

The threshold level selection is critical for the accurate detection of the discriminator as well as the ROIC. The noise in the ROIC is the most significant factor which affects the detection results. The noise

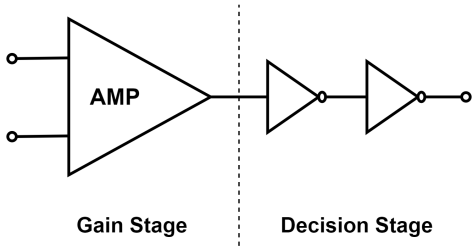


Figure 2.5: Two-stage structure for discriminator

voltage in each readout channel has a Gaussian distribution with a standard deviation of $\sigma_{n,rms}$ [8]. Setting the threshold voltage of the discriminator larger than $8 \cdot \sigma_{n,rms}$ could guarantee that at least 99.99% of the samples are within the effective detection range. This way, the minimum SNR, defined as the ratio between the threshold level of the discriminator and one standard deviation of the noise voltage, equals 8.

The offset and noise of the discriminator have a negative impact on the operation accuracy. The specifications of the offset and noise of the discriminator will be defined by the SNR and the output signal characteristic of the previous block, the filter. To avoid degrading the SNR, the input-referred noise and offset of the discriminator should not exceed the output-referred noise of the filter. The active filter produces a noise voltage of $15mVrms$ at its output.

2.2. ROIC with Passive Filter

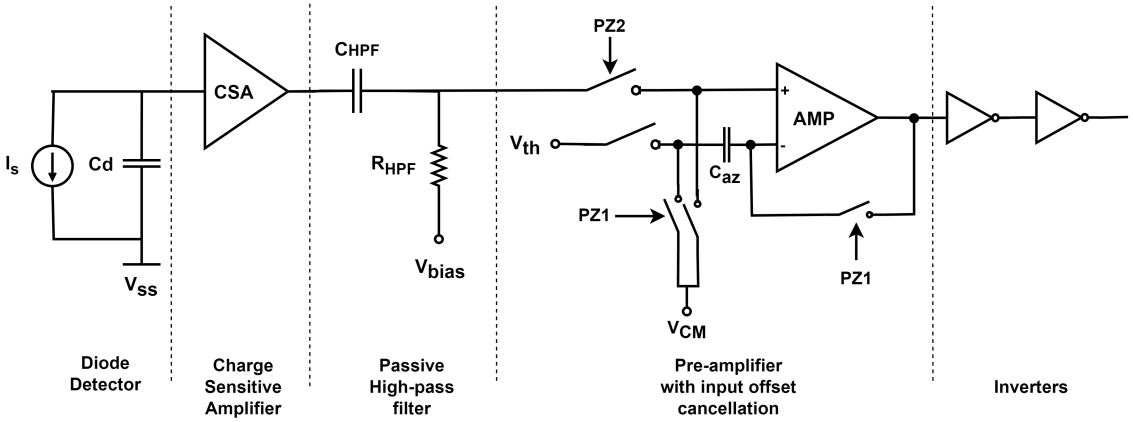


Figure 2.6: Proposed ROIC with passive filter

To save power and eliminate the signal pileup at the CSA's output, the active filter (shaper) in the first version of ROIC is substituted by a passive high-pass filter built with a resistor and a capacitor. This architecture of the ROIC with passive filter is shown in Fig.2.6. However, the passive filter on the other hand reduces the amplitude of the voltage signal received by the discriminator by around 30%, which poses new challenges for the discriminator design.

2.2.1. Passive Filter

The high-pass filter (HPF) passes signal with a frequency higher than a certain cut-off frequency f_c while attenuating signal with a frequency lower than this cut-off frequency f_c. There is no amplification for the CSA's output signal compared with the active filter. For the proposed application, the passive high-pass filter eliminates the signal pileup at CSA's output terminal by filtering the DC level and reduces the discharging time. It is a first-order filter that consists of a capacitor and a resistor in series as shown in Fig.2.7. The transfer function is shown in Fig.2.7 (b), and the cut-off frequency f_c of the HPF can be expressed as Eq.2.1.

$$f_c = \frac{1}{2\pi\tau_{HPF}} = \frac{1}{2\pi R_{HPF} C_{HPF}} \tag{2.1}$$

The attenuation in the low-frequency band also conduces to degradation in offset and noise. The passive high-pass filter usually could achieve a lower offset and noise value than the active band-pass filter by setting a proper cut-off frequency f_c.

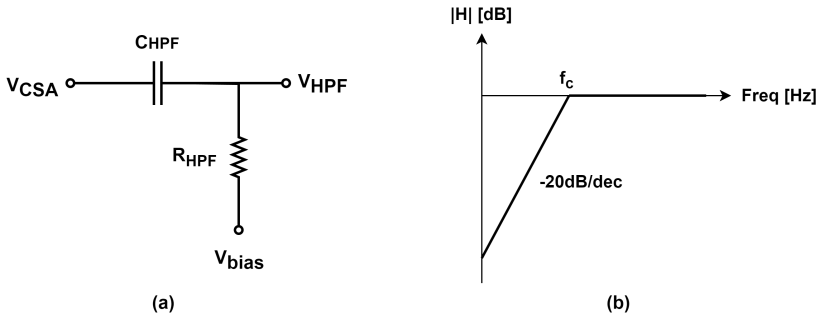


Figure 2.7: First-order passive HPF (a) diagram and (b) AC response

The transient response of the passive HPF with different time constant τ_{HPF} is shown in Fig.2.8. One of the drawbacks of replacing the active filter with a passive filter is that it leads to a certain extent of undershooting. Undershoot means the signal drops below the DC baseline at the falling edge and then increases back slowly. This could cause interference with the subsequent input events. As shown in Fig.2.9, the peak of HPF's output drops when continuous events come. In the worst case, the HPF's output wave can not exceed the threshold level of the discriminator and leads to a detection error.

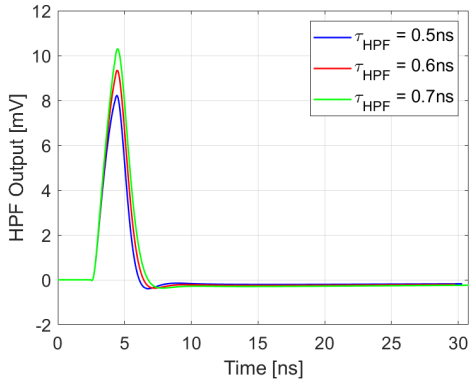


Figure 2.8: Effects of time constant τ_{HPF} on the passive HPF's transient response

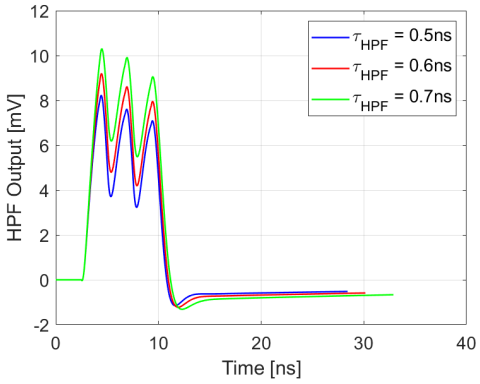


Figure 2.9: Passive HPF's transient response for '111' pattern

The characteristics of the passive HPF's output signal versus its time constant τ_{HPF} is shown in Fig.2.10. The amplitude and undershoot of the passive HPF's output both show an increasing trend with an increasing time constant τ_{HPF}. The selection of the time constant τ_{HPF} is critical. Firstly, adding this passive HPF load should not affect the stability of the CSA. Secondly, the fall time of the filter's output should be comparable with the rise time so that the time width at the discriminator's threshold level could fit into one time frame of $2.5ns$. Concerning the presented simulation results, the passive high-pass filter can fulfill the desired requirements in terms of speed and SNR with a time constant τ_{HPF} of $0.7ns$.

2.2.2. Discriminator with Offset Reduction

The discriminator for ROIC with the passive filter sticks to the two-stage structure shown in Fig.2.5. The equivalent error source referred to the input of the decision stage and the requirement for SNR puts requirement towards the gain of the preamplifier. The deviation of the decision stage's threshold level with standard deviation σ_{th} and the noise voltage referred to the preamplifier's output is σ_n both contribute to the error source of the decision stage. To make sure the decision stage could achieve an SNR above 14, its threshold level should reach $7 \cdot \sqrt{\sigma_{th}^2 + \sigma_n^2}$ above the baseline level. Assuming

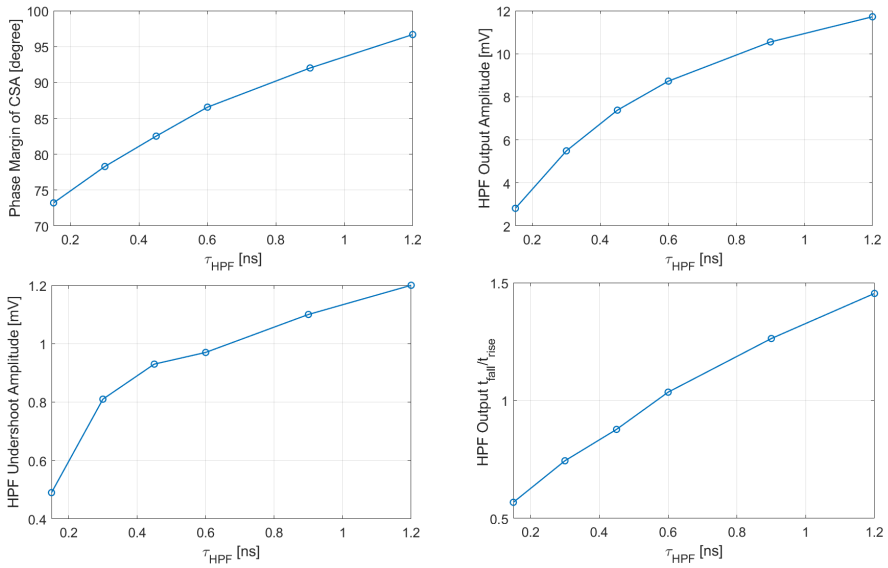


Figure 2.10: Passive HPF's performance versus time constant τ_{HPF}

the threshold level of the decision stage lies at 75% of the preamplifier's output amplitude, then the preamplifier should produce a signal with an amplitude of at least $\frac{7\cdot\sqrt{\sigma_{th}^2+\sigma_n^2}}{75\%}$.

Input Offset Storage and Cancellation

Replacing the active band-pass filter with a passive high-pass filter results in a much smaller signal received by the discriminator. According to Fig.2.10, the signal which needs to be distinguished has an amplitude less than $12mV$ depending on the selected time constant of the passive HPF. This means that the input-referred offset of the discriminator will become comparable in magnitude to its input signal levels. Therefore, the offset could drive the discriminator's output into saturation which would affect the operation accuracy. Thus, offset reduction is the main task for the design of the discriminator for ROIC with a passive filter.

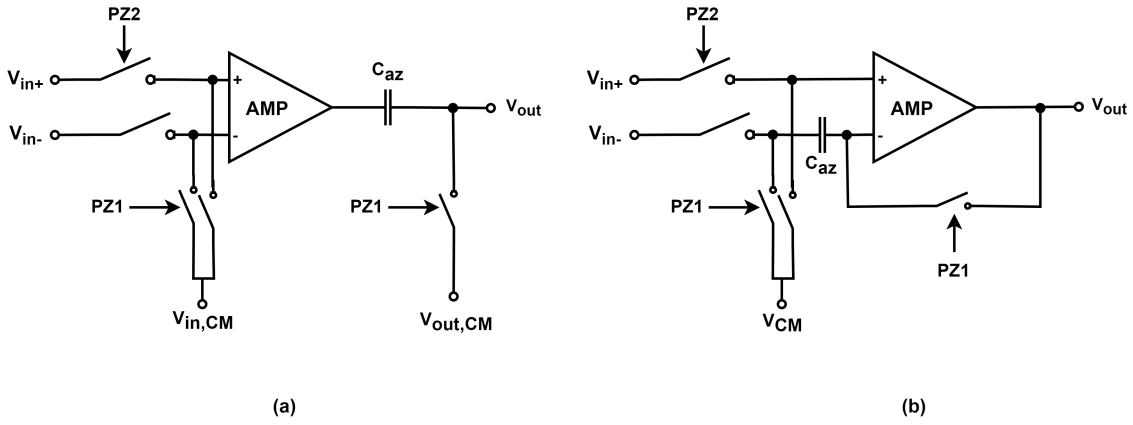


Figure 2.11: (a) Output offset cancellation, (b) Input offset cancellation

For the designed continuous-time discriminator with a two-stage structure shown in Fig.2.5, the offset from the decision stage can be dismissed due to the high gain of the pre-amplifier. The offset of the pre-amplifier could be represented by an equivalent DC voltage source referred to its input terminal. The offset of the pre-amplifier is caused by transistor mismatching including dimensions and threshold voltage V_{th}, due to manufacturing uncertainty [19]. Increasing the size of symmetrical devices [11] or applying dynamic offset reduction techniques helps to reduce the offset. Commonly used dynamic offset reduction techniques include autozeroing and chopping [19]. However, for the

targeted application with a high count rate chopping is not an option due to the required very high chopping frequency. The autozeroing technique involves sampling the offset and subtracting it from the total signal. During the offset storage phase, the differential input terminals are shorted to the AC ground. During the amplification phase, the discriminator is connected to the filter and processes the signal.

According to the offset storage and cancellation occurs at the input or the output terminal, it could be divided into closed-loop offset cancellation and open-loop offset cancellation. For the open-loop offset cancellation technique shown in Fig.2.11 (a), an amplified offset voltage $A \cdot V_{os}$ is stored on the capacitor at the output. To avoid this voltage saturating the amplifier, the gain should be limited to 50, which can't satisfy the requirement for this design based on the previous analysis. Besides, due to the large output impedance of the pre-amplifier (which is necessary to achieve a high gain), the setting time of the capacitor usually takes a time duration of more than 10 time-frames (equals to $10 \times 2.5ns = 25ns$), which leads to an increase in the number of missed events. For these reasons, the closed-loop offset cancellation technique which involves storing and compensating the offset at the input is applied for this project, shown in Fig.2.11 (b). A capacitor C_{az} is connected to the inverting input to record the offset. The configuration for the offset storage phase and amplification phase is shown in Fig.2.12. During the first clock phase, the differential inputs and output terminal are shorted together, and the voltage stored on the capacitor C_{az} equals to $\frac{A}{A+1} \cdot V_{os}$, where A is the DC gain of the pre-amplifier. Neglecting the error caused by charge injection, etc., the residual input-referred offset would be $\frac{1}{A+1} \cdot V_{os}$.

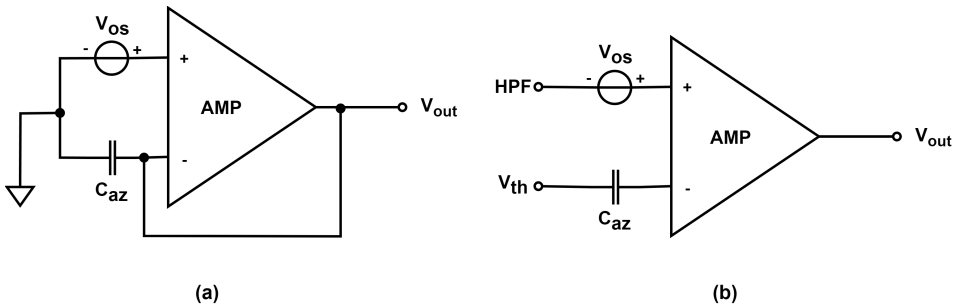


Figure 2.12: Configuration of the pre-amplifier during (a) Offset storage phase, (b) amplification phase

Offset Storage and Amplification Duration

During the offset storage phase, the discriminator is blind to the incoming events because it is disconnected from the previous stage. To reduce the number of possible missed events during this phase, the time duration of the offset storage phase t_1 should be as short as possible. During the offset storage phase, the pre-amplifier senses the offset and the capacitor C_{az} is charged. The voltage across the capacitor C_{az} is given by:

$$V_{C_{az}} = \frac{A}{A+1} \cdot V_{os} \cdot (1 - e^{-\frac{t}{\tau_1}}) \tag{2.2}$$

When $t_1 = 5 \cdot \tau_1$, $V_{C_{az}}$ equals 99.33% of the final value, and the offset could be considered as stored completely. The time duration of the offset storage phase t_1 is proportional to the charging constant τ_1, which depends on the value of C_{az} and its series resistance. A smaller capacitance leads to a smaller t_1 as shown in Fig.2.13.

During the amplification phase, the non-inverting input terminal is connected to the previous block, the passive high-pass filter, while the inverting input terminal is connected to the threshold voltage. The capacitor C_{az} is discharged and the stored voltage drops, which means the offset cannot be fully compensated anymore. A reset is necessary when the voltage variation across the capacitor C_{az} reaches the limitation $\Delta V_{C_{az}}$. The time duration of the amplification phase t_2 is related to the value of C_{az} and the current $i_{C_{az}}$ flowing onto it, given by:

$$t_2 = \frac{\Delta V_{C_{az}}}{i_{C_{az}}/C_{az}} \tag{2.3}$$

The gate leakage current of the input transistor of the pre-amplifier contributes the most to the $i_{C_{az}}$. While the less dominant current, the leakage of the capacitor C_{az} and switches should also be taken

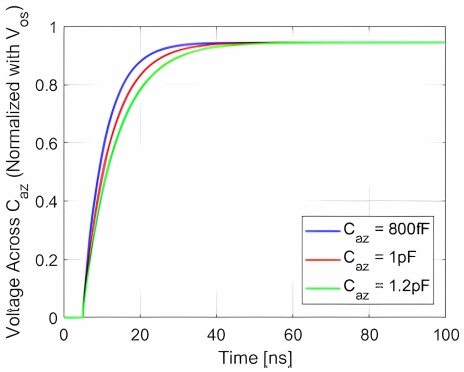


Figure 2.13: Voltage across the C_{az} during the offset storage phase

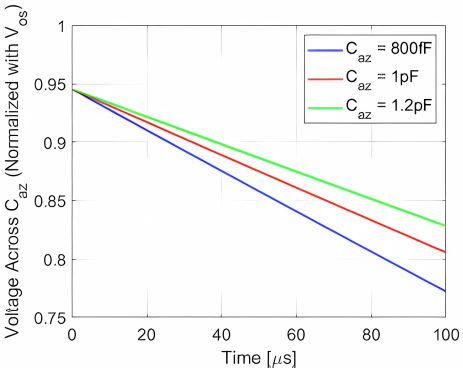


Figure 2.14: Voltage across the C_{az} during the amplification phase

into consideration. Based on Eq.2.3, limiting the gate leakage current of the input transistor is key to extending the amplification phase duration t_2 and reducing the autozeroing frequency f_{az} (which could be expressed as Eq.2.4). A lower autozeroing frequency f_{az} also leads to a smaller switching power loss.

$$f_{az} = \frac{1}{t_1 + t_2} \tag{2.4}$$

The gate leakage current of the MOS transistor mainly depends on the selected size and threshold voltage, as well as the technology used. The development of CMOS technology leads to a reduction in the oxide thickness and this causes a rise in oxide leakage current density [20]. Besides, the current is proportional to the gate area according to the equation $I = J \cdot WL$. Using input transistors with smaller sizes helps to decrease the current flowing on the capacitor C_{az}, as shown in Fig.2.15. However, this also leads to a higher offset of the pre-amplifier, as shown in Fig.2.16.

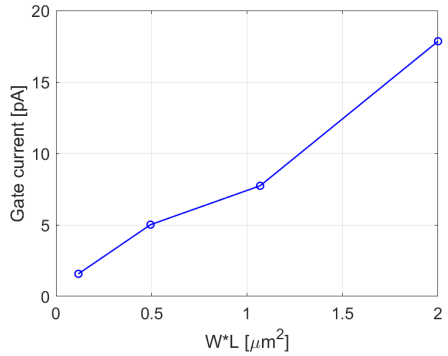


Figure 2.15: Pre-amplifier's input transistor's gate current versus size

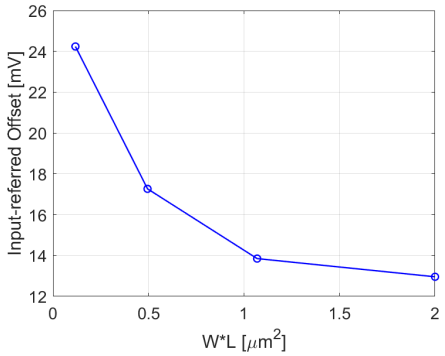


Figure 2.16: Pre-amplifier's input-referred offset versus input transistor's size

2.3. Summary

The design requirements for the discriminator closely relate to the performance of the previous block, the filter. The active and passive filter will provide different design specifications for the discriminator:

Table 2.1: Design specification for discriminator

(a) Discriminator with active filter

Specification	Target
Power	$< 50\mu W$
Input Amplitude Range	$450mV - 675mV$
Input-referred Noise	$< 3mVrms$
Input-referred Offset	$< 15mV$
Pulse Width	$< 2.5ns$
Propagation Delay	$< 2.5ns$

(b) Discriminator with passive filter

Specification	Target
Power	$< 150\mu W$
Input Amplitude Range	$544mV - 554mV$
Input-referred Noise	$< 200\mu Vrms$
Input-referred Offset	$< 1mV$
Pulse Width	$< 2.5ns$
Propagation Delay	$< 2.5ns$

3

Circuit Implementation

Based on the analysis made in the last chapter with respect to the power and accuracy aspect, circuits are designed in TSMC 40nm CMOS technology. The chapter presents the implementation of the discriminator with active or passive filter as well as auxiliary blocks at the transistor level. The performance of each block given by simulation is summarized to verify the specifications brought out in Chapter 2.

3.1. ROIC with Active Filter

The active filter relaxes the requirements for the discriminator design on the noise and offset aspect. Considering the requirements on area occupation and power consumption, a basic discriminator consisting of a five-transistor operational transconductance amplifier (OTA) and two inverters is implemented (shown in Fig.3.1).

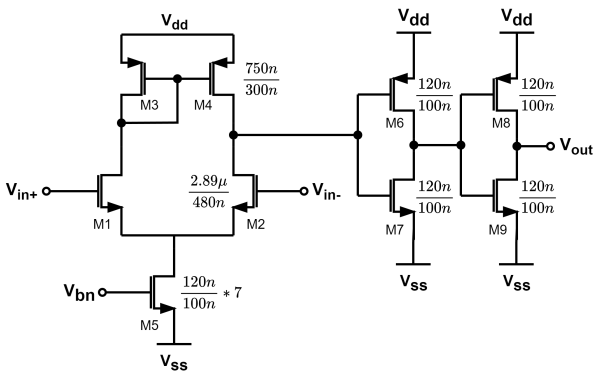


Figure 3.1: Schematic of the basic discriminator

The five-transistor OTA, as the pre-amplifier, has an NMOS differential input pair and a PMOS mirrored load. The non-inverting input is connected to the output of the active filter and the inverting input is connected to the DC threshold voltage. The threshold reference is set to $8\sigma = 120mV$ above the baseline level. The input transistor pair M1 and M2 is biased to meet the baseline level of the active filter's output. The power consumption is mainly determined by the tail current generated by M5. Tuning the tail current and keeping the power consumption within the budget of $50\mu W$, the change of offset and noise performance is observed through simulation (shown in Fig.3.2 and Fig.3.3). The final selected tail current is $20.1\mu A$, which leads to the discriminator's power consumption of $30\mu W$ (including the biasing). The OTA's frequency response is shown in Fig.3.4.

The layout of the designed basic discriminator for ROIC with active filter is shown in Fig.3.5. The transistors (M1, M2, M3, M4) on the symmetric branches of the pre-amplifier are placed in the same direction and as close as possible to minimize the device mismatching error. Deep N-well devices are

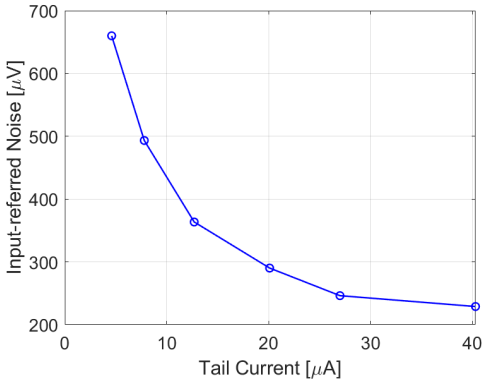


Figure 3.2: OTA's input-referred noise versus the tail current

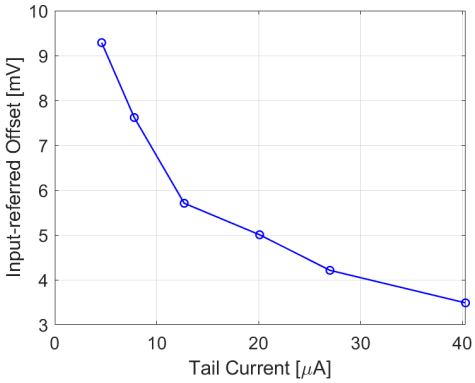


Figure 3.3: OTA's input-referred offset versus the tail current

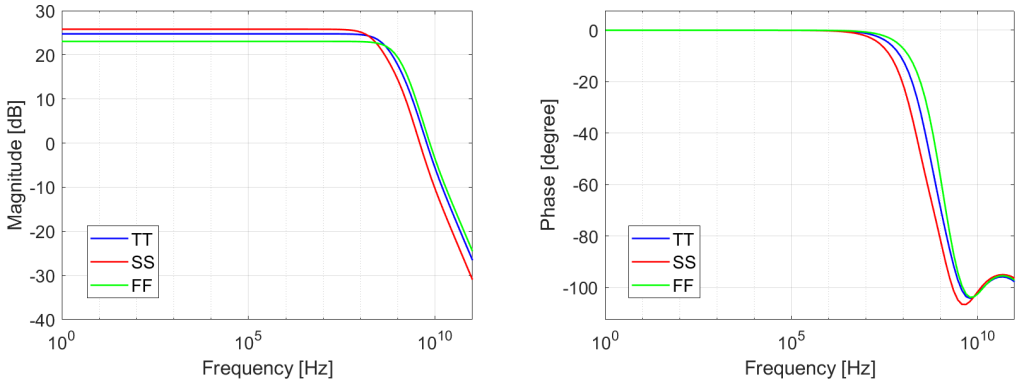


Figure 3.4: Frequency response of the implemented OTA across critical corners

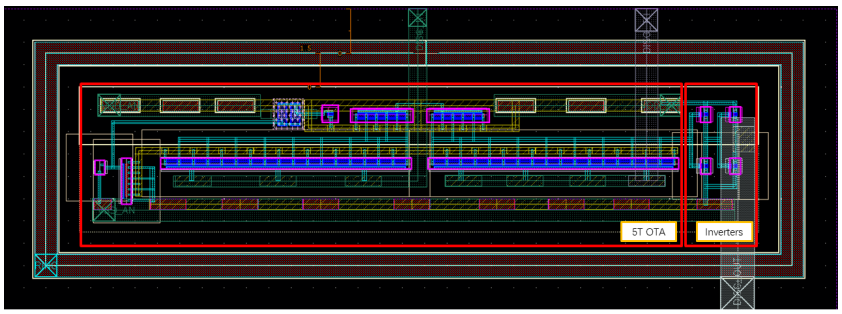


Figure 3.5: Layout of the basic discriminator

used to isolate the NMOS devices and a guard ring is implemented to further reduce the noise from the substrate caused by minority carrier injection and ensure the detection accuracy.

The achieved performance of the designed basic discriminator through schematic and post-layout simulation is summarized in Table.3.1 and Table.3.2. Note that the propagation delay is with respect to the PIN diode detector's current pulse.

Table 3.1: Summary of the basic discriminator's performance (schematic)

Specification	Min.	Max.
Input referred Noise	$260.39\mu Vrms$	$295.33\mu Vrms$
Input-referred Offset	$4.31mV$	
Propagation Delay	$1.42ns$	$2.09ns$
Pulse Width	$378ps$	$1.67ns$
Power Consumption	$30.02\mu W$	$57.47\mu W$

Table 3.2: Summary of the basic discriminator's performance across TT corner (post-layout simulation)

Specification	Schematic	Post-layout
Input referred Noise	$260.39\mu Vrms$	$295.33\mu Vrms$
Input-referred Offset	$4.31mV$	$5.76mV$
SNR	14.6	14.6
Propagation Delay	$1.8ns$	$1.9ns$
Power Consumption	$36.44\mu W$	$36.43\mu W$

3.2. ROIC with Passive Filter

Section.3.2.1 shows the implementation of the passive filter and the achieved performance. The implementation of each part of the discriminator with passive filter will be described in each subsection (from Section.3.2.2 to Section.3.2.5). The passive high-pass filter and the main discriminator (not including the switches and capacitor) are tested through post-layout simulation. A summary of the discriminator with passive filter will be presented at the end of this section.

3.2.1. Passive High-pass Filter

Based on the analysis in Section.2.2.1, the selected time constant τ_{HPF} is $0.7ns$. For the same time constant, a larger resistive R_{HPF} and a smaller capacitive C_{HPF} could get a smaller undershoot amplitude, as shown in Fig.3.7. However, the price to pay is a rise in the noise and a drop in the SNR as shown in Figure.3.6. The final selected value is resistance R_{HPF} of $20k\Omega$ and capacitance C_{HPF} of $35fF$.

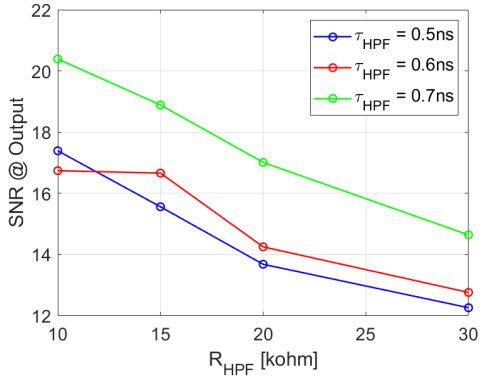


Figure 3.6: Passive HPF's SNR versus R_{HPF}

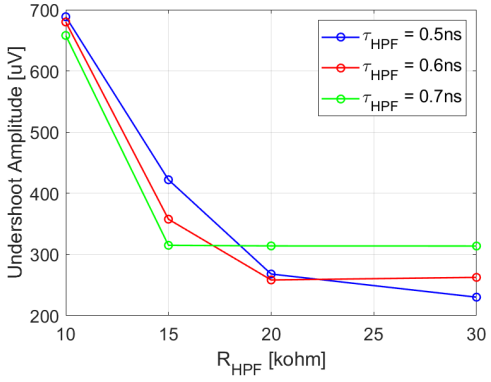


Figure 3.7: Passive HPF's undershoot versus R_{HPF}

Fig.3.8 and Fig.3.9 show the transient response of the proposed passive HPF. From the response for continuous events shown in Fig.3.9, it could be observed that the passive HPF's output amplitude

drops for the second and third incoming events. The first reason is that there is an undershoot of $300\mu V$ for every event at the passive HPF's output. To completely recover from this undershoot takes around $229ns$. So for continuous incoming events, the passive HPF's output usually rises from a lower level, which causes a drop in amplitude. Secondly, the amplitude of the signal generated by the CSA, which is the previous block before the passive HPF, drops 7% for each event. For example, for three continuous incoming events, the CSA produces a signal amplitude of $25.5mV$ for the third event and $30mV$ for the first event. Fig.3.10 presents the layout of the designed passive HPF. Table.3.3 and Table.3.4 summarize the achieved performance of the passive high-pass filter.

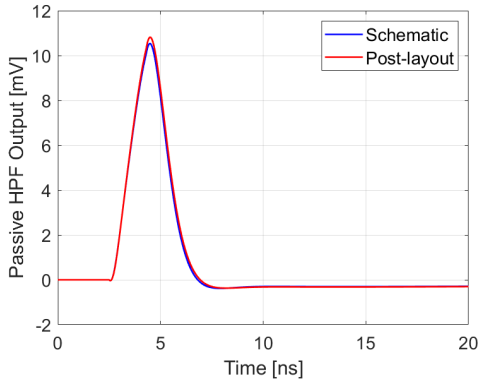


Figure 3.8: Transient response of the implemented passive HPF across TT corner for single input event

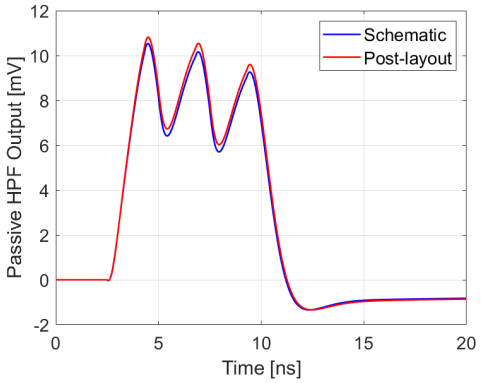


Figure 3.9: Transient response of the implemented passive HPF across TT corner for '111' pattern

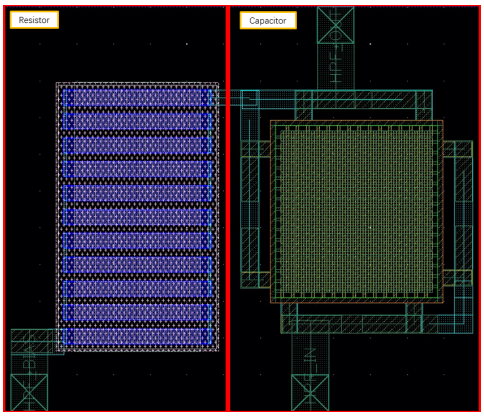


Figure 3.10: Layout of the passive high-pass filter

Table 3.3: Summary of the passive HPF's performance (schematic simulation)

Specification	Min.	Max.
SNR	13.94	16.21
Output Amplitude	$9.19mV$	$11.16mV$
Output-referred Noise	$658.8\mu Vrms$	$688.3\mu Vrms$
Time Width @ $7\sigma_n$	$1.95ns$	$1.97ns$
Undershoot	$288.4\mu V$	$633.0\mu V$

3.2.2. Gain stage: Pre-amplifier

The pre-amplifier is the core of the continuous-time 2-stage discriminator. Its target characteristics should be high-gain, low input-referred offset and low gate current of the input transistors. Accounting for the threshold variation of the decision stage of $20mV$ and leaving an amplitude margin for the

Table 3.4: Summary of the passive HPF's performance across TT corner (post-layout simulation)

Specification	Schematic	Post-layout
SNR	15.59	16.08
Output Amplitude	$10.53mV$	$10.82mV$
Output-referred Noise	$675.3\mu Vrms$	$672.8\mu Vrms$
Time Width @ $7\sigma_n$	$1.96ns$	$2.09ns$
Undershoot	$378.7\mu V$	$368.1\mu V$

decision, the pre-amplifier should provide a minimum gain of $31dB$. Based on Table.3.3, to ensure the pre-amplifier could correctly distinguish the passive HPF's output signal, its input-referred offset after compensation should be limited below $500\mu V$.

Based on the analysis in Chapter 2, the pre-amplifier should achieve a minimum DC gain of $31dB$. Furthermore, the input transistor pair should be sized properly to decrease the discharging speed of the offset storage capacitor C_{az} based on the analysis in Section.2.2.2.2. Besides, because the pre-amplifier will be in the unity-feedback configuration during the offset storage phase (as shown in Fig.2.12(a)), its input and output terminal should be biased at the same voltage. To fulfill these three requirements, a 2-stage pre-amplifier as shown in Fig.3.11 is implemented. The first stage (M1-M13) is a fully differential amplifier with an error amplifier (M6-M13) to provide common-mode feedback (CMFB). The CMFB is necessary for the fully differential amplifier to stabilize its common-mode operation point. The current following through the symmetrical branches and the tail current determine the output common-mode voltage of the fully differential amplifier and they should balance with each other. However, due to the mismatching, the current unbalance will result in a dramatic change in the output common-mode voltage[14].

Input transistors (M8, M11) of the error amplifier sense the common-mode output voltage $V_{out,CM}$ of the fully differential amplifier and compare it with a desired reference voltage $V_{CM,ref}$. The common-mode voltage deviation reflects a change in the branch currents, which is the current flowing on M12 and M13. Assume $V_{out,CM}$ is larger than $V_{CM,ref}$, the over-drive voltage of M9 and M10 will be larger than the over-drive voltage of M8 and M11, which leads to a larger drain current of M12 than M13. The current flowing on M12 will be mirrored to M5, which determines the tail current of the fully differential amplifier. An increase of the drain current of M12, also the M5, results in a decrease of the $V_{out,CM}$. Thus, a negative feedback loop to stabilize the common-mode operation point of the fully differential amplifier is formed. Simulation shows that the phase margin of the CMFB loop is 80°. The second stage is an OTA to convert the differential output of the first stage into a single-ended signal and to further amplify the signal with a gain of $23.99dB$.

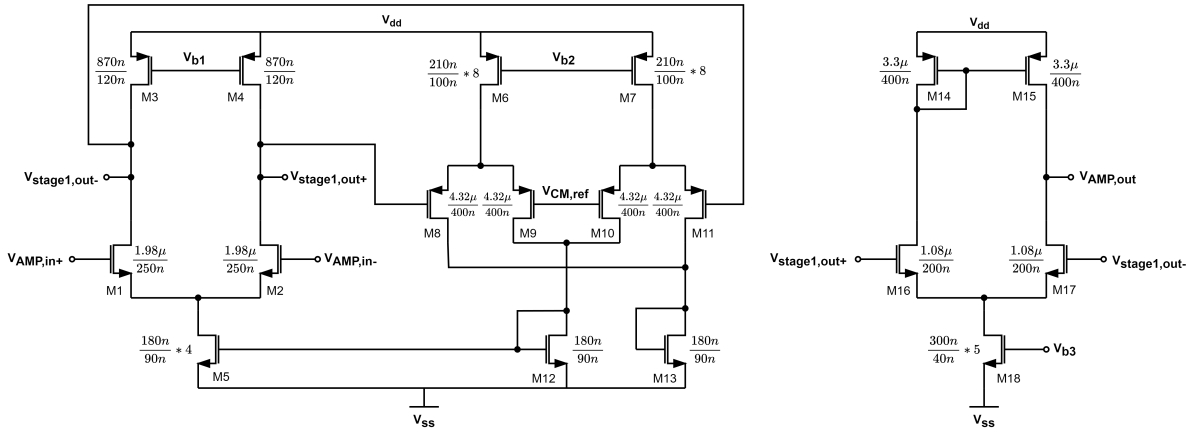
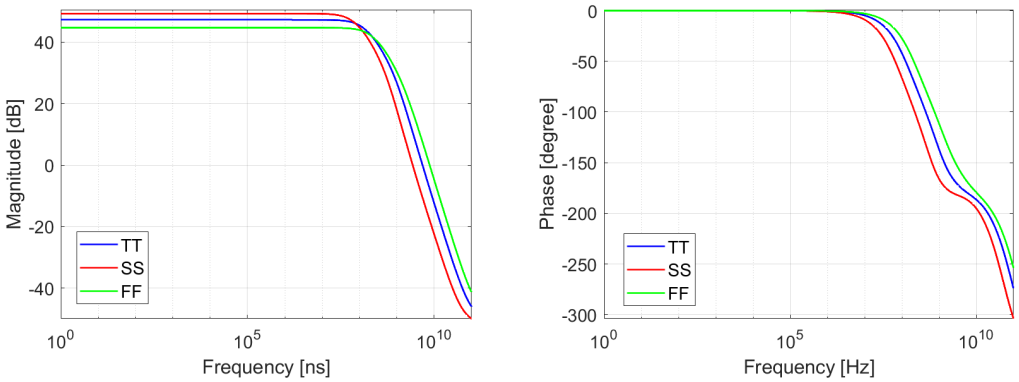


Figure 3.11: Schematic of the 2-stage pre-amplifier

The frequency response of the implemented pre-amplifier is shown in Fig.3.12. The layout of the proposed pre-amplifier is shown in Fig.3.13. Schematic simulation results of the proposed pre-amplifier (before introducing the offset cancellation technique) are summarized in Table.3.5. Table.3.6 shows the achieved performance by post-layout simulation across the TT corner.

Figure 3.12: Frequency response of the implemented 2-stage pre-amplifier across critical corners



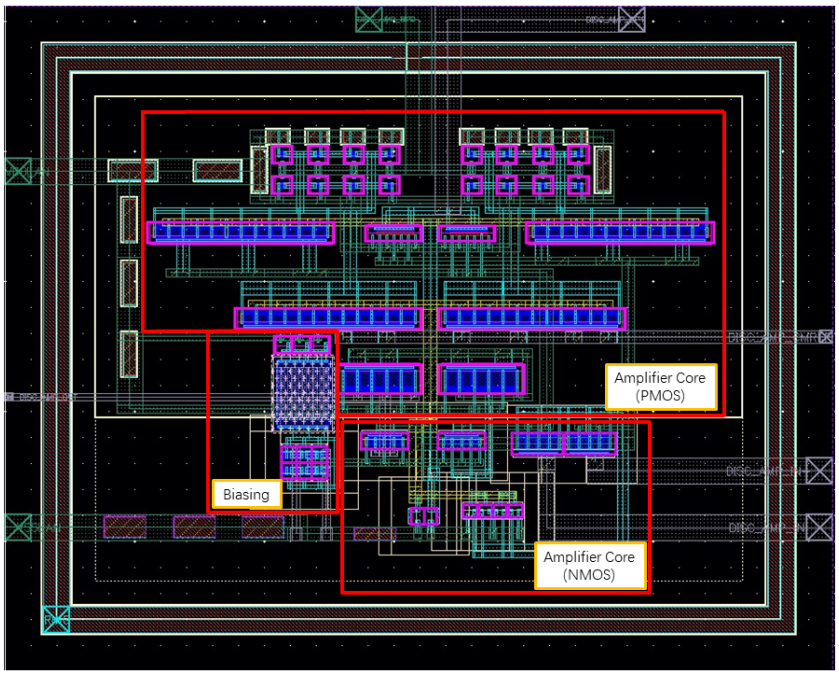


Figure 3.13: Layout of the 2-stage pre-amplifier

Table 3.5: Summary of the implemented pre-amplifier's performance (schematic simulation)

Specification	Min.	Max.
Gain	$44.65dB$	$49.24dB$
BW	$54.7MHz$	$181.4MHz$
Input-referred Noise	$109.31\mu Vrms$	$326.28\mu Vrms$
Input-referred Offset	$15.37mV$	
Power Consumption	$68\mu W$	$103.6\mu W$

Table 3.6: Summary of the implemented pre-amplifier's performance (post-layout simulation)

Specification	Schematic	Post-layout
Gain	$47.22dB$	$46.19dB$
BW	$138.29MHz$	$72.13MHz$
Input-referred Noise	$255.01\mu Vrms$	$155.73\mu Vrms$
Input-referred Offset	$16.36mV$	$14.80mV$
Power Consumption	$80.08\mu W$	$88\mu W$

3.2.3. Offset Storage Capacitance

A capacitor C_{az} is connected to the non-inverting terminal of the pre-amplifier to store its offset voltage. Because of the limited area budget of each pixel, the offset storage capacitor's value and its area should also be limited. Based on the analysis in Section.2.2.2.2, the capacitance C_{az} relates to the offset cancellation efficiency.

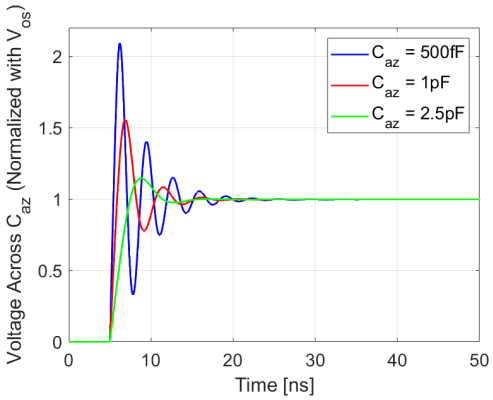


Figure 3.14: Voltage across the offset storage capacitor C_{az} during the offset storage phase

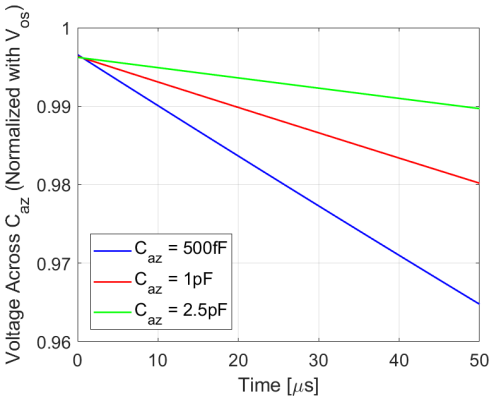


Figure 3.15: Voltage across the offset storage capacitor C_{az} during the amplification phase

During the offset storage phase, the capacitance C_{az} influences the slewing behavior of the pre-amplifier in the closed-loop configuration. Increasing the C_{az} will move the pole related to the output terminal of the pre-amplifier to a lower frequency band, which results in an increase in phase margin and stability. The output signal of the pre-amplifier, and also the voltage across the C_{az}, will respond from 'underdamping' to 'overdamping', as shown in Fig.3.14. Thus, the capacitance C_{az} should be set to a moderate value to avoid the instability problem and to achieve a relatively short charging time. During the amplification phase, it could be seen from Fig.3.15 that the larger the C_{az}, the slower the discharging speed, and the longer time that the offset could be compensated. Based on the analysis and simulation results, the capacitance C_{az} is set to $1pF$. The achieved offset storage phase duration t_1 is $10ns$ and amplification phase duration t_2 is $90\mu s$.

3.2.4. Decision Stage: Inverters

Two inverters connected in series are implemented as the decision stage, as shown in Fig.3.16. The switching threshold is related to the size and threshold voltage of the PMOS and NMOS transistor [13]. The switching threshold for the implemented inverter is set to 7σ above the baseline of the preamplifier's output signal, where σ is the standard deviation of the noise referred to the preamplifier's output. The voltage transfer characteristic (VTC) curve of the implemented series inverters is shown in Fig.3.17. The achieved performance of the implemented decision inverters is summarized in Table.3.7.

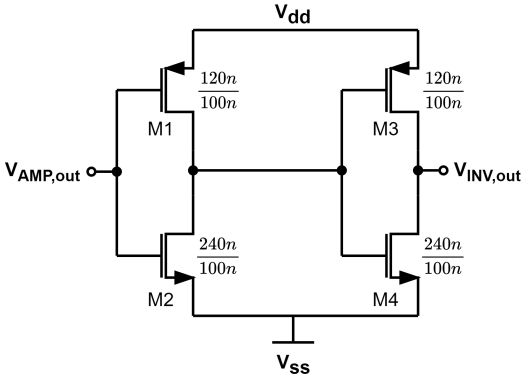


Figure 3.16: Schematic of the decision inverters

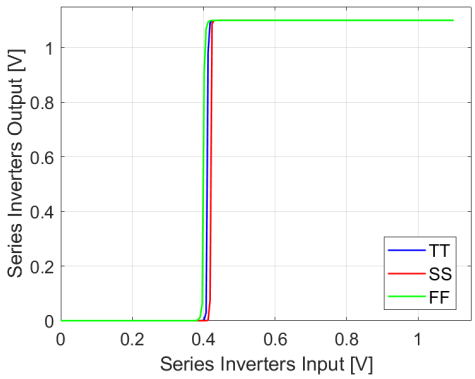


Figure 3.17: VTC of the implemented inverters across critical corners

Table 3.7: Summary of the implemented decision stage performance

Specification	Min.	Max.
Switching Threshold	$399.16mV$	$420.58mV$
Input-referred Offset	$14.36mV$	
Power Consumption	$100.6pW$	$171.9pW$

3.2.5. Switches and Complementary Clock Generator

Switches in the forward path and the feedback loop affect the performance of the offset cancellation. To minimize the additional offset voltage stored on the capacitor C_{az} due to charge injection, complementary switches are implemented (shown in Fig.3.18). The length of the transistors in the switch is selected to reach a lower equivalent on-resistance. Based on Fig.3.19 and Eq.3.1, the MOS transistor with a smaller channel length gives the smallest equivalent resistance for the same width during conduction. The width of the transistors is set to the minimum value to reduce the injected channel charge based on Eq.3.2.

$$R_{on} = \frac{V_{DS}}{I_D} = \frac{1}{\frac{\mu_n C_{ox} W}{L}(V_{GS} - V_{th})} \tag{3.1}$$

$$Q_{ch} = WLC_{ox}(V_{GS} - V_{th}) \tag{3.2}$$

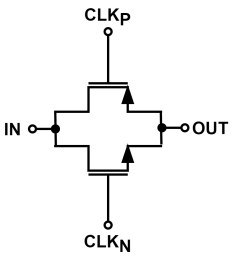


Figure 3.18: Complementary switches

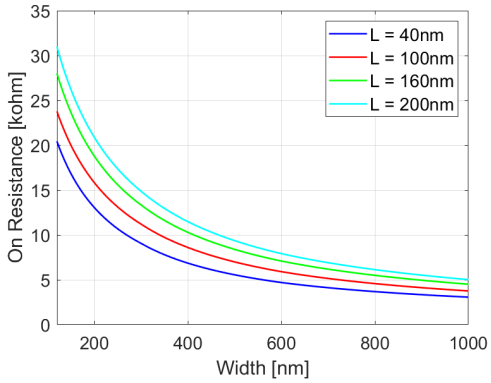


Figure 3.19: Transistor's on-resistance versus size

A complementary clock generator is implemented to control the complementary switches. The schematic of the complementary clock generator that controls the switches in the feedback loop is shown in Fig.3.20. The transmitting gate T1 passes the clock signal when the inverted clock signal reaches its gate terminal. The transmitting gate T2 passes the inverted clock signal when the clock signal reaches its gate terminal. The wave behavior of the input and output clock signal is shown in Fig.3.21. The achieved performance is summarized in Table.3.8.

Table 3.8: Summary of the complementary clock generator's performance

Specification	Min.	Max.
Rise/fall time	$4.61ps$	$8.01ps$
Delay	$7.92ps$	$12.85ps$
Power Consumption	$1.15nW$	$1.22nW$

3.2.6. Summary

The input offset cancellation technique is applied to the designed pre-amplifier to reduce its input-referred offset voltage. The theoretical residual offset after offset cancellation could be calculated based

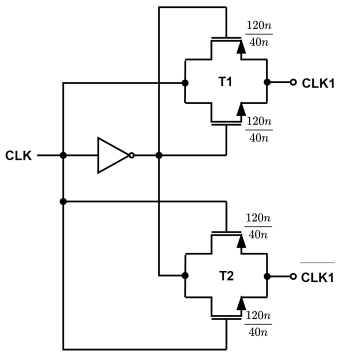


Figure 3.20: Schematic of the complementary clock generator

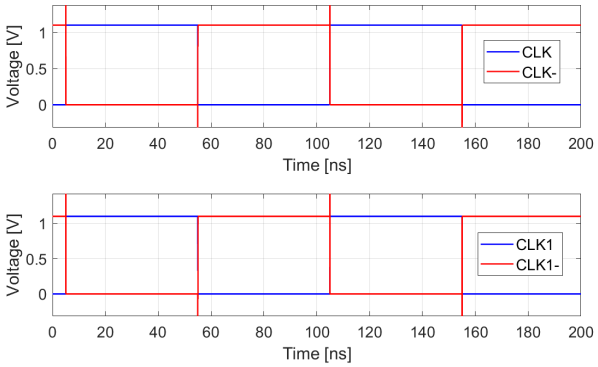


Figure 3.21: Transient response of the complementary clock generator

on the achieved performance of the pre-amplifier, shown in Eq.3.3.

$$V_{os,res} = \frac{V_{os}}{A+1} = \frac{15.37mV}{223.9+1} = 66.67\mu V \tag{3.3}$$

However, due to switches' charge injection, etc., the simulated residual offset is $69.24\mu V$. The achieved performance of the discriminator with input offset cancellation for the ROIC with passive filter is summarized in Table.3.9.

Table 3.9: Summary of the discriminator with input offset cancellation performance

Specification	Min.	Max.
Offset Storage Phase Duration	$10ns$	
Amplification Phase Duration	$90\mu s$	
Input referred Noise	$109.31\mu Vrms$	$326.28\mu Vrms$
Input-referred Offset	$69.24\mu V$	
Propagation Delay	$1.86ns$	$2.24ns$
Pulse Width	$1.37ns$	$1.70ns$
Power Consumption	$68.35\mu W$	$103.86\mu W$

4

Performance

In this chapter, the performance of the designed discriminators is presented and the signal processing of the proposed ROIC with active or passive filter is shown. The discriminator for ROIC with active filter was taped out and physically verified. While the discriminator for ROIC with passive filter was tested through simulation. Section.4.1 describes the testbench design and measurement setup for the discriminator's speed performance evaluation. The design of few functional blocks facilitating for qualification tests and the measurement results are included in this section. Section.4.2 describes the operation and performance of the designed discriminator with input offset cancellation.

4.1. Discriminator for ROIC with Active Filter

The transient response of the ROIC with active filter for various input event patterns is shown in Fig.4.2. The input events follow the Poisson distribution [8]. It could be observed from Fig.4.2 that the OTA (the gain stage of the proposed discriminator) generates a smaller signal in the FF corner due to the active filter producing a smaller input signal for it. This could be compensated by trimming the threshold level properly.

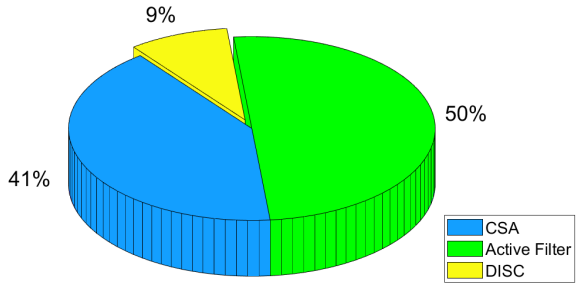


Figure 4.1: Power consumption breakdown in the proposed ROIC with active filter

The total power consumed by one pixel ROIC with active filter is $340\mu W$ and the power consumption of each function block is shown in Fig.4.1. The discriminator only takes 9% of the total power consumption and 8% of the total area occupation.

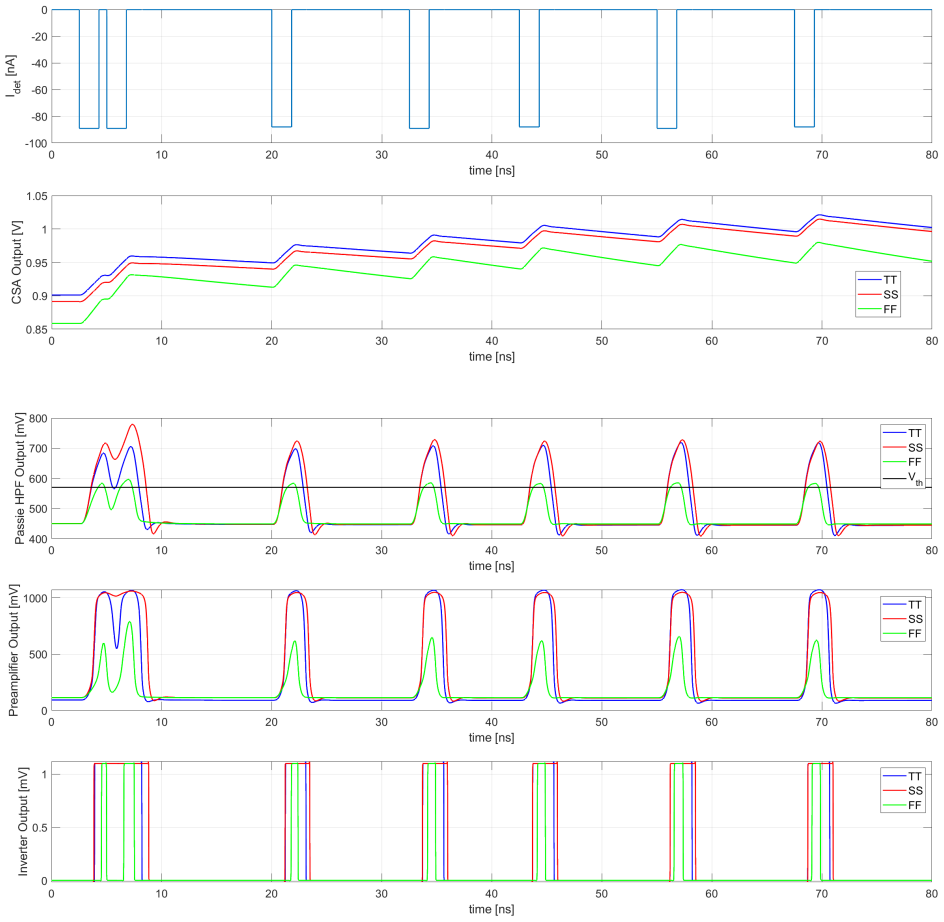


Figure 4.2: Signal processing in the ROIC with active filter across critical corners, from top to bottom namely corresponds to the current pulse generated by the reverse-biased PIN diode detector, CSA's output signal, active filter's output signal and discriminator's threshold level, preamplifier's output signal, decision stage's output signal

4.1.1. Design for Test

A separate testbench is designed and implemented to test the discriminator's transient response. The propagation delay of the designed continuous-time discriminator is a critical specification to evaluate its speed performance. To avoid miss-counting in the applied high-count rate ROIC, the propagation delay should be limited below one detection clock period of 2.5ns. A lower sampling delay could lead to a lower detection error rate [8]. Besides, carrying the measurement over a range of temperatures is necessary for the target application. As described in Chapter 1, the charge detector may consist of max.8000 pixels with each having a power consumption of 350μW (for the proposed ROIC with active filter), which leads to a total power consumption of at least 2.8W. In this case, the chip would be driven to a higher temperature during operation. Besides, the SEM usually contains a heating stage and a cooling stage to adjust the operation temperature [16]. To make sure each pixel ROIC could still achieve the desired performance under a higher temperature level, the measurement is performed over a range of temperatures from 23°C to 70°C. The block diagram of the proposed measurement setup

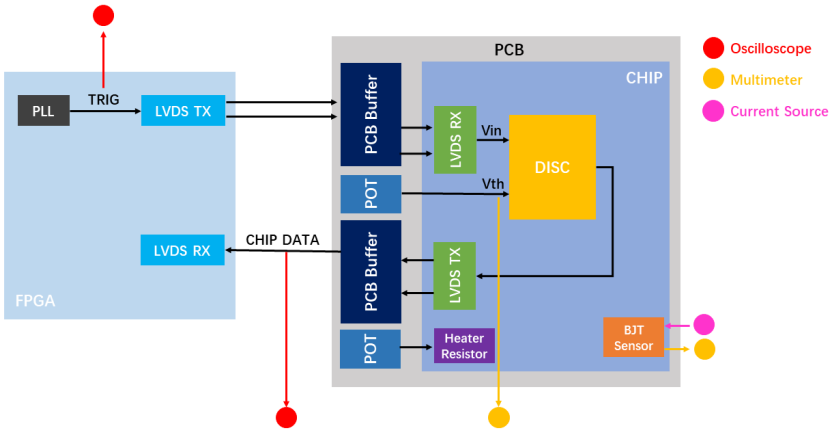


Figure 4.3: Block diagram of the proposed measurement setup

is shown in Fig.4.3. A trigger pulse signal produced by the phase-locked loop (PLL) implemented in FPGA is sent to the discriminator's non-inverting input via LVDS transmitter on FPGA, PCB buffer and on-chip LVDS receiver. The discriminator's output signal is sent back to the FPGA. An oscilloscope with 1GHz bandwidth and an active probe with 2.5GHz sampling rate is used to monitor the trigger signal and the output signal. The threshold of the discriminator with a range from 0 to 1.1V is generated by a potentiometer (POT) on PCB and could be monitored by the multimeter. There is another POT implemented to adjust the voltage applied on the on-chip heater resistor in order to tune the temperature of the chip. A BJT sensor is implemented to sense the temperature of the chip. Biasing currents are injected into the BJT and its voltage, which reflects the chip's temperature, is measured by the multimeter.

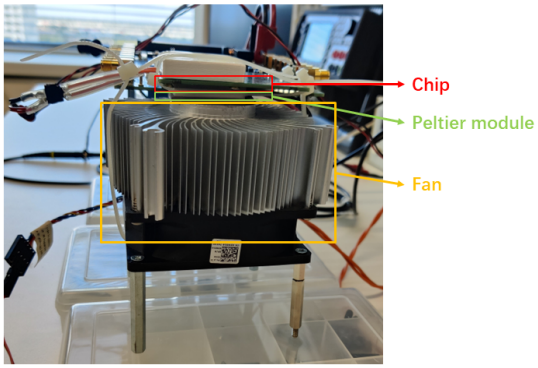


Figure 4.4: Cooling configuration

By applying different voltages across the on-chip heater POT, the chip's temperature could reach a

max 74°C. To cool the chip down to room temperature of 23°C, a Peltier module and a fan are used. The Peltier module is a passive thermoelectric element that can be used to transfer heat from a colder place to a warmer place with the help of electric energy [18]. It is glued with the chip and powered by a current source as a cooling element. A fan is used to speed up the thermal flow. The configuration is shown in Fig.4.4. Note that the producer and model type of equipment involved in the measurement are listed in the Appendix.

LVDS Transceiver
LVDS (low voltage differential signal) is a technical standard that specifies the electrical characteristics of a differential, serial signal standard which is usually applied in high-speed data transfer between chip and board [4]. A pair of High-speed LVDS transceivers (shown in Fig.4.5) has been designed and implemented to send input data and clock with a maximum data rate of 400*MHz* from the FPGA (Field Programmable Gate Arrays) to the chip and transmit the chip's output data to the FPGA. The core of the transmitter behaves like a switched-polarity current generator while the receiver's task is to convert current into voltage through a loaded resistor between its differential input terminals.

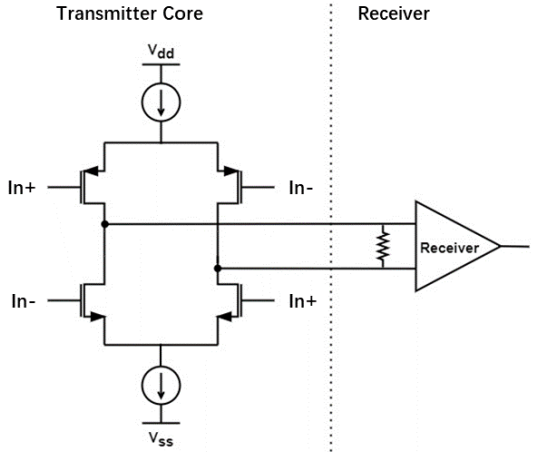


Figure 4.5: Schematic of a general LVDS transceiver circuit

LVDS Transmitter The transmitter circuit contains a level-up shifter, a control signal generator, and a switched-polarity current generator with common-mode feedback (CMFB) as shown in Fig.4.6. The

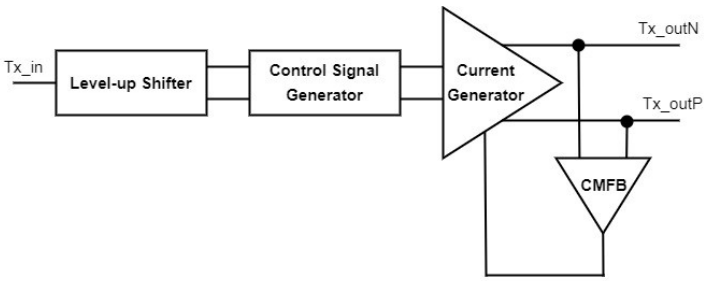


Figure 4.6: Structure of the LVDS transmitter

level-up shifter (shown in Fig.4.7) is composed of a common-source (CS) differential input transistor pair (M1, M2) with a positive feedback load (M3, M4). The role of the level-up shifter is to lift up the core logic supply level of 1.1*V* to the I/O logic supply level of 2.5*V*. A higher gain and a faster speed can be provided by the positive feedback latch transistor load than the resistive load. However, the size of the input NMOS transistors (M1, M2) should be larger than the size of the loaded PMOS transistors (M3, M4) to ensure the stability of the loop. The control signal generator (shown in Fig.4.8) comprises four cascaded inverters to provide a pair of inverse-phase control signals for the following current generator.

The size factor is set to 4 to minimize the propagation delay. The schematic of the switched-polarity current generator of the LVDS transmitter is shown in Fig.4.9. The current switching bridge is built of two current sources (M1, M6) and MOS-based switches (M2, M3, M4, M5). To set proper output common-mode voltage, a common-mode feedback circuit (M7-M14) is implemented.

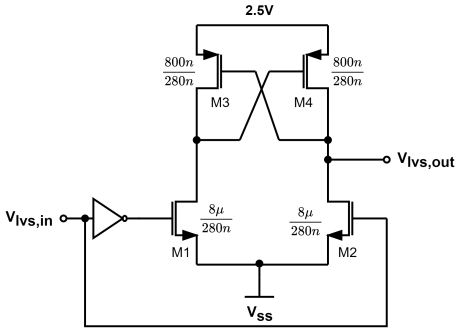


Figure 4.7: Schematic of the level-up shifter

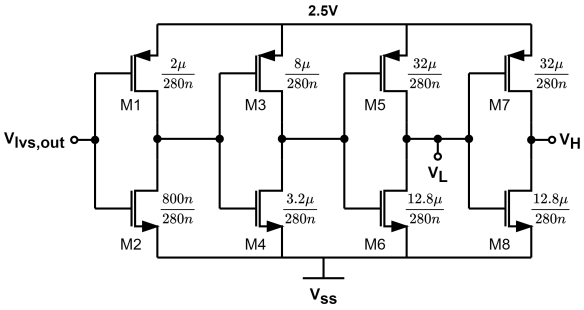


Figure 4.8: Schematic of the control signal generator

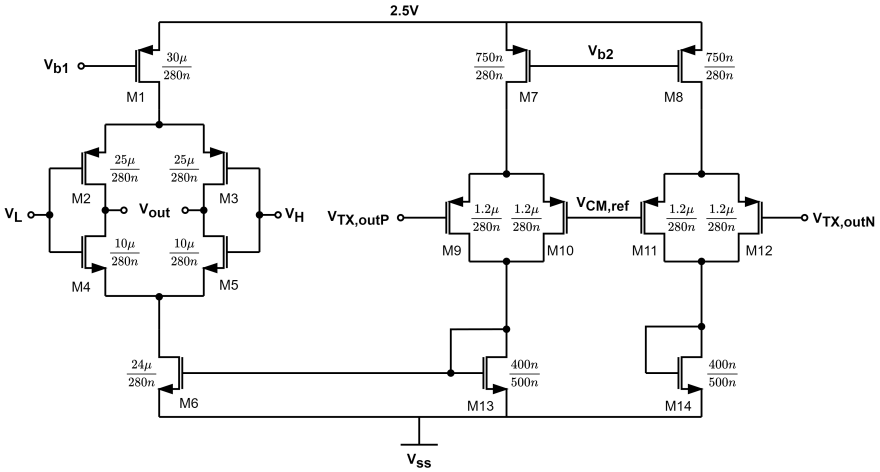


Figure 4.9: Schematic of the switched-polarity current generator

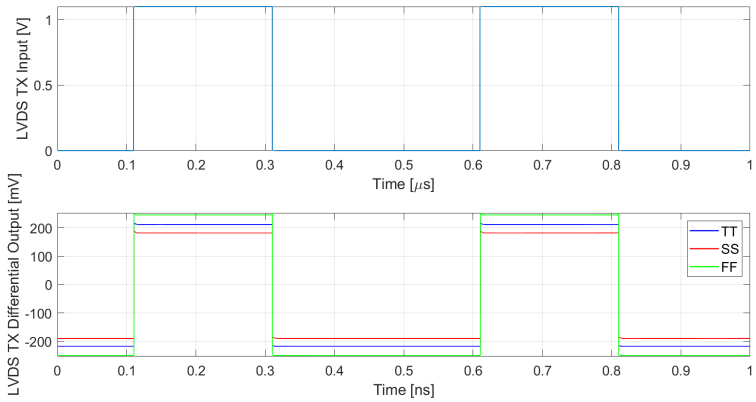


Figure 4.10: Transient response of the LVDS transmitter across critical corners

During the simulation, a resistor of 100Ω, and two equivalent pad parasitic capacitors of 200*fF* are loaded between two differential output terminals of the transmitter. The transient simulation result

of the proposed LVDS transmitter across the critical corners is shown in Fig.4.10. It has a low-voltage swing of 180mV - 215mV at the output.

LVDS Receiver The LVDS receiver circuit contains a hysteresis comparator, a differential amplifier, and an inverter as shown in Fig.4.11. The comparator with hysteresis is designed to be immune to the input noise and to increase switching speed using a positive feedback load (shown in Fig.4.12). The following differential amplifier is responsible for providing extra gain and shifting down the logic level from 2.5V to 1.1V (shown in Fig.4.13). An inverter is added at the output of the amplifier to get the desired logic output.

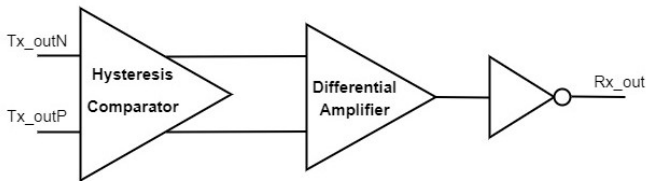


Figure 4.11: Structure of the LVDS receiver

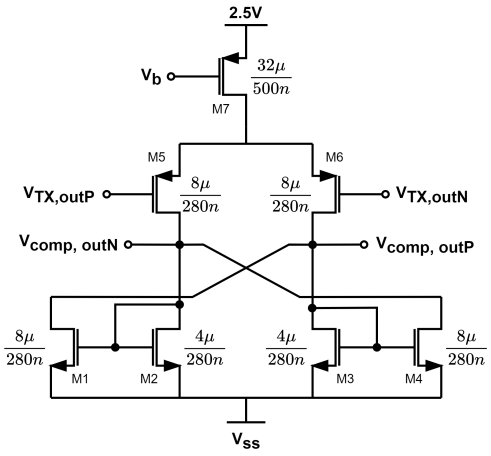


Figure 4.12: Schematic of hysteresis comparator

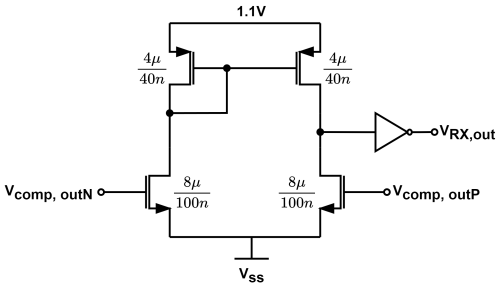


Figure 4.13: Schematic of differential amplifier with inverter

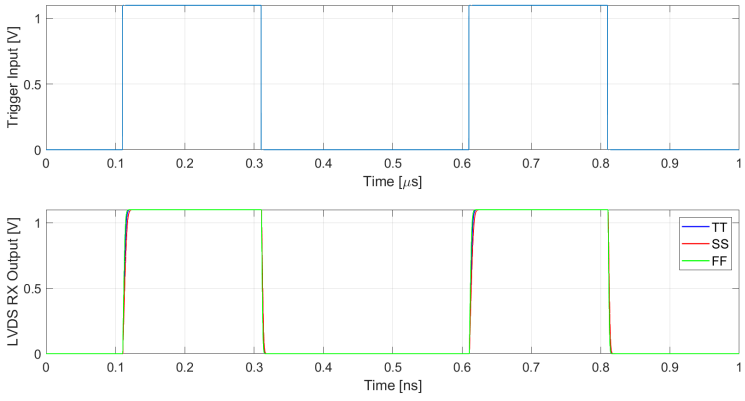


Figure 4.14: Transient response of the LVDS receiver across critical corners

Temperature Sensor

A basic on-chip temperature sensor is implemented. Since temperature measurement is not the prior aim of the project and the resolution requirement is relatively relaxed, the basic structure comprised of one BJT is chosen. The schematic is shown in Fig.4.15 and the layout is shown in Fig.4.16.

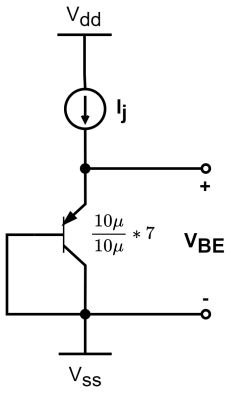


Figure 4.15: Schematic of the BJT temperature sensor

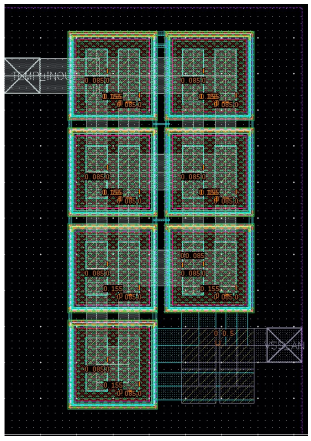


Figure 4.16: Layout of the BJT temperature sensor

The BJT has a temperature-dependent characteristic and a PTAT (proportional to absolute temperature) voltage could be generated by injecting at least two currents into the emitter terminal of the BJT. The voltage across the BJT's base-emitter junction V_{BE} (expressed as Eq.4.1) has a negative temperature coefficient. When injecting two sets of current into the emitter terminal of the BJT, the difference between its voltage across the base-emitter junction (expressed as Eq.4.2) shows a negative temperature coefficient.

$$V_{BE} = \frac{kT}{q} ln(\frac{I_c}{I_s}) \tag{4.1}$$

$$\Delta V_{BE} = \frac{kT}{q} ln(\frac{I_{c2}}{I_{c1}} \cdot \frac{I_{s1}}{I_{s2}}) \tag{4.2}$$

The selection of the range of the injected current I_j is important. There are two criteria to decide the minimum injected current value. Firstly, the minimum injected current should be selected to keep the $V_{BE} - I$ curve (shown in Fig.4.17) in the linear range to avoid minimizing the inaccuracy caused by operation point drift. Based on Fig.4.17, the slope of the $V_{BE} - I$ curve is closed to zero when the injected current I_j is larger than $50\mu A$. Secondly, the minimum injected current should be large enough to keep the $ln(I_c) - V_{BE}$ curve away from the low injection region (grey region shown in Fig.4.18) where the impact of the minority carrier concentration in the base can't be dismissed [12]. For the maximum injected current value, three criteria should be taken into consideration. Firstly, the ratio between two sets of injected current $\frac{I_{j1}}{I_{j2}}$ should be at least 10 to minimize the error in ΔV_{BE}[12]. Secondly, the maximum injected current should be small enough to keep the $ln(I_c) - V_{BE}$ curve away from the high injection region (yellow region shown in Fig.4.18) [12]. Finally, the maximum injected current should be able to keep the current gain $\beta = I_c/I_b$ independent of the injected current. To sum up, the injected current range for the proposed temperature sensor is selected from $50\mu A$ to $890\mu A$.

Three injected current I_{j1}, I_{j2} and I_{j3} are successively applied to the BJT to compensate for the error caused by the series resistor at the emitter terminal [12]. The chosen I_{j1}, $I_{j2} = 10I_{j1}$ and $I_{j3} = 16I_{j1}$ namely equals to $50\mu A$, $500\mu A$ and $800\mu A$, the resulting PTAT voltage ΔV_{BE} is expressed as Eq.4.3 [12].

$$\Delta V_{BE} = (\frac{ln10}{10-1} - \frac{ln16}{16-1}) \cdot \frac{kT}{q} = -\frac{2}{45} V_{BE}(I_1) - \frac{1}{15} V_{BE}(I_3) + \frac{1}{9} V_{BE}(I_2) \tag{4.3}$$

Before measuring the chip's temperature with the implemented on-chip BJT sensor, it is calibrated by a calibrated thermistor with a negative temperature coefficient (NTC). The thermistor is thermally glued with the chip to make sure it experiences the same temperature environment as the on-chip BJT

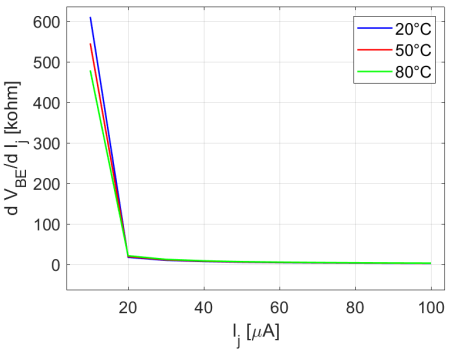


Figure 4.17: Slope of the $V_{BE} - Ij$ curve versus injected current under a range of temperatures

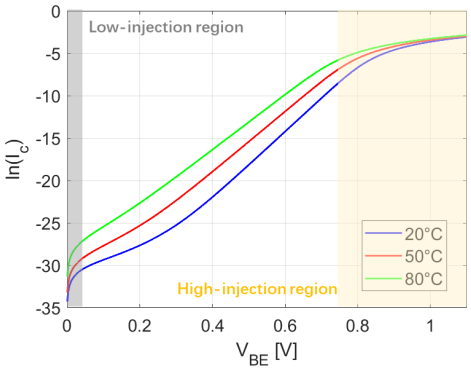


Figure 4.18: $ln(I_c)$ versus V_{BE} under a range of temperature

temperature sensor. The PTAT voltage ΔV_{BE} generated by the BJT sensor responses with a range of temperature is shown in Fig.4.19.

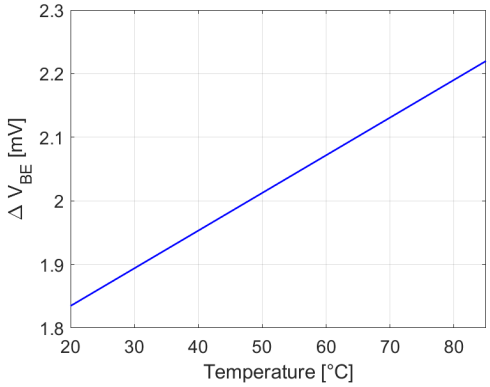


Figure 4.19: ΔV_{BE} versus temperature of the calibrated BJT sensor

4.1.2. Measurement Results

Based on the implemented testbench described in Section.4.1.1. The propagation delay of the discriminator reacting to a range of threshold levels under different temperatures is measured. The input signal and output signal of the discriminator are both digital signals with relatively sharp rise/fall edges. A pair of LVDS transceivers is required to communicate with the FPGA board. Signals are monitored through the general-purpose input/output (GPIO) pins on the FPGA board. The delay of the on-chip blocks can not be measured directly, but needs to be obtained by the subtraction from the total delay $t_{tot,mea}$ and the intrinsic delay $t_{int,mea}$ which comes from the FPGA and PCB. The intrinsic delay t_{int} is measured by shorting the input and output terminals of the on-chip LVDS transceivers so that the input signal generated by the FPGA will not pass the chip but return to the FPGA through PCB buffers. The measured intrinsic delay is 29.94ns with a standard deviation of 28.473ps. It is related to the characteristics of the FPGA and PCB. The measured chip's total delay $t_{tot,mea}$ is in the range of 32ns to 35ns and varies with the applied threshold level and temperature.

The designed testbench schematic shown in Fig.4.20 is used to obtain the simulated delay of the implemented discriminator with active filter for a range of threshold levels under a range of temperatures. The capacitor (C_{p1}, C_{p2}, C_{p3}) represents the equivalent parasitic capacitance of the trace based on the extracted cadence calibre file. Note that C_{p1} = 139.4fF, C_{p2} = 197.2fF, C_{p3} = 41.6fF, C_{pad} = 200fF, R_{load} = 100Ω. Running the post-layout simulation with the proposed design testbench, the total delay of all the on-chip blocks from LVDS receiver to LVDS transmitter is obtained and marked as $t_{p,tot,sim}$. The delay of the discriminator itself is obtained and marked as $t_{p,disc,sim}$.

The measured delay of the discriminator could be obtained based on Eq.4.4.

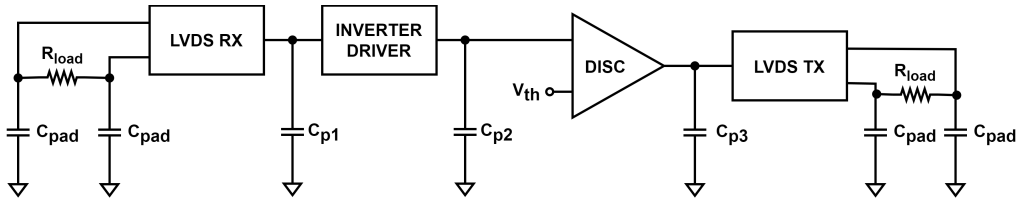


Figure 4.20: Design testbench schematic for obtaining the simulated delay of the implemented discriminator

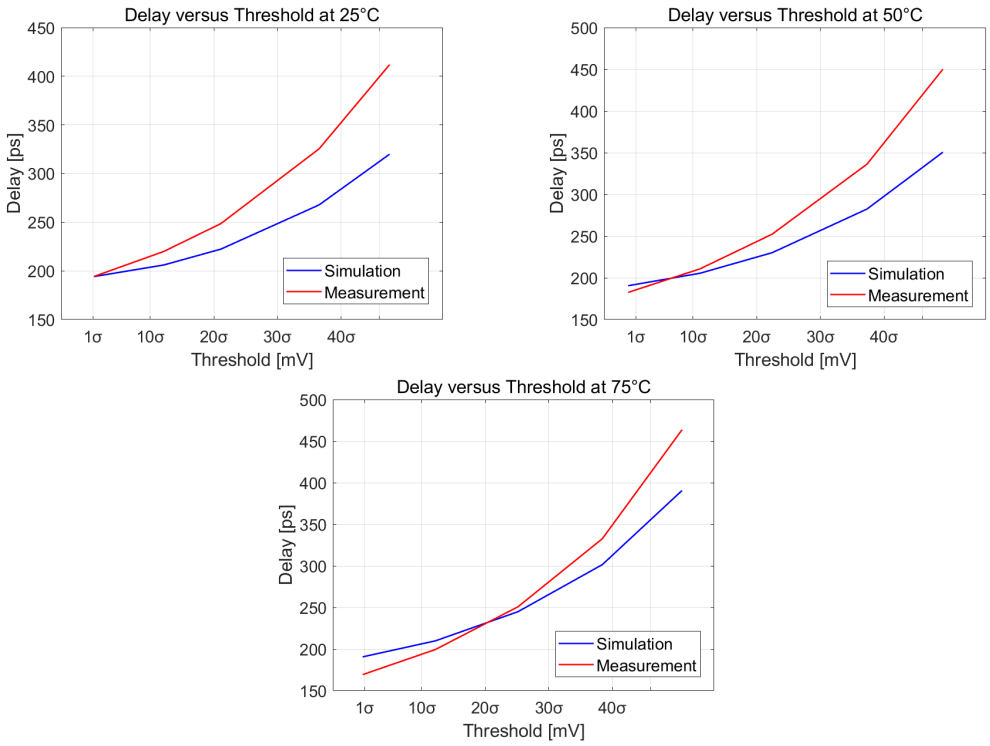


Figure 4.21: Discriminator's simulated and measured delay versus threshold at 25°C, 50°C and 75°C

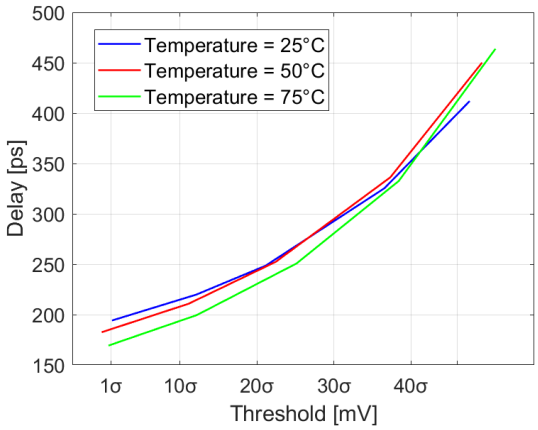


Figure 4.22: Discriminator's measured delay versus threshold at 25°C, 50°C and 75°C

$$t_{p,disc,mea} = (t_{tot,mea} - t_{int,mea}) \cdot \frac{t_{p,disc,sim}}{t_{p,tot,sim}} \tag{4.4}$$

Fig.4.21 and Fig.4.22 show how the delay of the discriminator changes with its threshold level at 25°C, 50°C and 75°C in post-layout simulation and measurement, where $\sigma = 5mV$ is one standard deviation of discriminator's input voltage variation. For example, "1σ" means that the threshold is set at 1σ above the biasing level of 520mV. The discriminator compares the pulse signal with the threshold. The higher the threshold voltage means the smaller the overdrive (note that the overdrive of the comparator is defined as the amount of voltage that exceeds the switching threshold). Simulation and measurement both verify that a lower threshold voltage leads to a smaller delay and a faster response. The maximum absolute measurement error is 90ps and it corresponds to the maximum relative measurement error of 22%. One of the error sources is the testbench schematic shown in Fig.4.20 used to obtain the simulation results. There is a difference between the extracted parasitic capacitance (C_{p1}, C_{p2}, C_{p3}) and the wire's real equivalent capacitance. The error could also come from the sample rate limitation of the oscilloscope (1GHz sample rate) and its probe (1GHz sample rate and 2.5GHz sample rate). To qualify the amount of this error, the measurement is repeated with another oscilloscope with a higher sample rate of 8GHz. A comparison between the measured delay with two oscilloscopes is shown in Fig.4.23. The measured delay versus threshold obtained by two different oscilloscopes follows the same trend. And the oscilloscope with an 8GHz sample rate gives a smaller measured delay. The absolute difference is between 5.7ps and 10ps, which means the oscilloscope's sample rate limitation contributes 3% to 4% of the total error. Besides, supply voltage variation, etc., could also be the reason for the error.

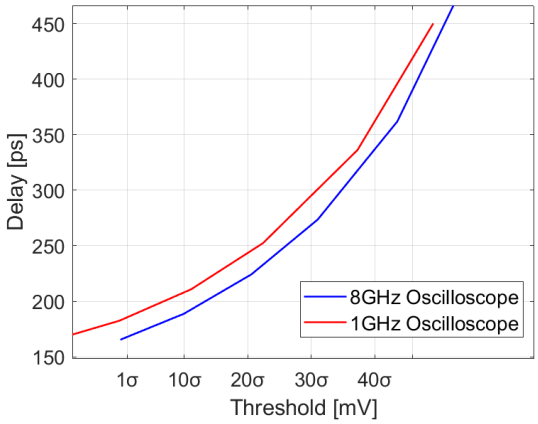


Figure 4.23: Measured delay versus threshold at 50°C obtained by oscilloscope with 1GHz and 8GHz sample rate

The maximum absolute deviation of the delay due to the change of temperature when applying the same threshold level is 25ps based on the measurement results shown in Fig.4.22. Considering the minimum delay is around 200ps at a threshold of 1σ above the biasing level, this means that temperature variation in the range of 25°C to 75°C only brings a maximum change of 12.5% for the delay. Based on the analysis described and specifications brought out in Chapter 2, this performance variation due to temperature could be tolerated for the application. It could be also observed that a higher environmental temperature leads to a faster response.

4.2. ROIC with Passive Filter

The total static power consumed by the ROIC with passive filter is 221μW per pixel, which is 65% of the power consumption of the ROIC with active filter. The power consumption of each functional block is shown in Fig.4.24. The discriminator with input offset cancellation takes 36% of the total power consumption. The transient response of the ROIC with passive filter for input patterns with Poisson distribution is shown in Fig.4.25. The input pattern is the same as the one collected for the ROIC with active filter as shown in Fig.4.2.

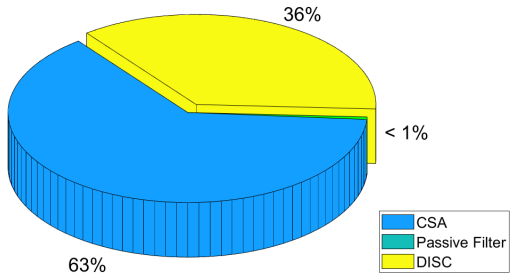


Figure 4.24: Power consumption breakdown in the proposed ROIC with passive filter

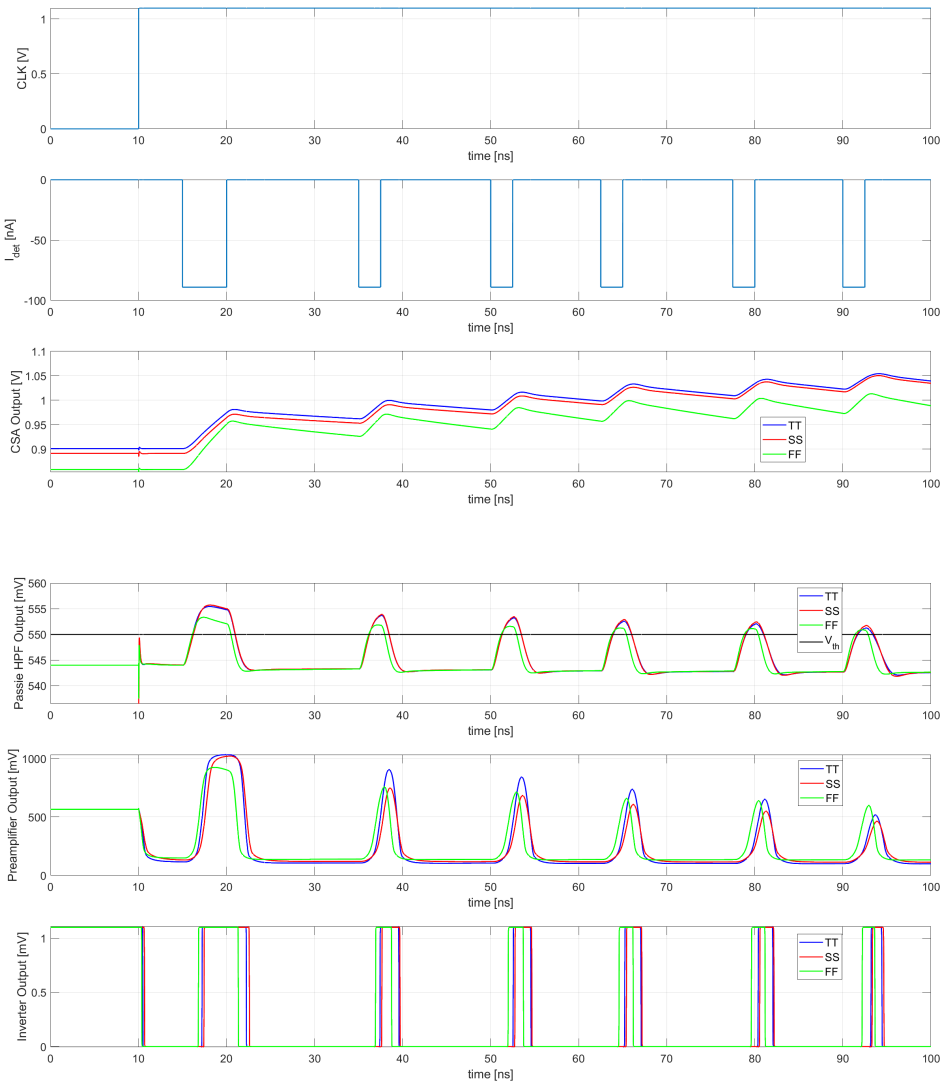


Figure 4.25: Signal processing in the ROIC with passive filter across critical corners, from top to bottom namely corresponds to the clock signal for discriminator's offset cancellation, the current pulse generated by the reverse-biased PIN diode detector, CSA's output signal, passive filter's output signal and discriminator's threshold level, preamplifier's output signal, decision stage's output signal

5 Conclusion

5.1. Comparison and Discussion

Charge detection ROIC that could realize fast and accurate particle acquisition is applied as an essential part of the SEM. The ROIC consists of three functional blocks with each playing an important role in the signal shaping. The CSA converts the charge pulse into a voltage signal with limited bandwidth. The filter with band-pass or high-pass frequency characteristic reduces the ISI error by attenuating the low-frequency band. The discriminator distinguishes the voltage from the noise level and produces a digital pulse signal that reflects the detection results. To meet the limited power budget and ensure the readout accuracy, two solutions for the filter and discriminator design came up. One of the solutions involves an active band-pass filter and a basic continuous-time discriminator with a 5T OTA as the gain stage and two inverters as the decision stage. Another solution involves a first-order high-pass passive filter built by a resistor and a capacitor, and a discriminator with periodic input offset cancellation. Design specifications are analyzed and circuit implementations are posed.

Table 5.1: Performance summary of the proposed ROIC and comparison with relevant work

	Proposed ROIC with active filter	**Proposed ROIC with passive filter**
Technology	$40nm$ CMOS	
Generated charge	$160aC$	
Detector capacitance	$50fF$	
Time resolution	$2.5ns$	
Max. event rate	$400MHz$	
Power per pixel	$320\mu W$ ($V_{sup} = 1.1V$)	$221\mu W$ ($V_{sup} = 1.1V$)
Area per pixel	$6314\mu m^2$	-

	SERCuit [2]	**SPC ROIC [5]**	**PADI-8 [1]**
Technology	$65nm$ CMOS	$40nm$ CMOS	$0.18\mu m$ CMOS
Generated charge	$160aC$	$350aC$	$1fC$
Detector capacitance	$300fF$	-	-
Time resolution	$2.5ns$	-	-
Max. event rate	$400MHz$	-	$300kHz$
Power per pixel	$2.85mW$ ($V_{sup} = 1.2V$)	$100\mu W$	$17mW$ ($V_{sup} = 1.8V$)
Area per pixel	$8000\mu m^2$	-	$15cm^2$

Table.5.1 summarizes the achieved performance of the proposed ROIC realized by two different solutions as described above and compares it to the relevant ROIC. Table.5.2 summarizes the achieved performance of the designed discriminator for ROIC with active or passive filter and compares it to the relevant work. The proposed ROIC with active filter achieves a maximum error rate of $1.47ppm$ in experimental verification[21]. The discriminator with passive filer takes less power consumption in the ROIC. However, there will be a period of $10ns$ in every $90\mu s$ that the ROIC with passive filter fails to

detect and process the input event. On the other hand, the discriminator with active filter can respond to the input event synchronously and no event will be missed. To sum up, the discriminator with passive filter is a more power-saving solution for the charge detection ROIC, while the discriminator with active filter could achieve better accuracy.

Table 5.2: Performance summary of the proposed discriminator and comparison with relevant work

	Proposed DISC with active filter	**Proposed DISC with passive filter**
Technology	$40nm$ CMOS	
SNR	14.6	15.1
Input-referred noise	$270\mu Vrms$	$255.01\mu Vrms$
Input-referred offset	$4.49mV$	$69.24\mu V$
Propagation delay	$348ps$	$995ps$
Power consumption	$36\mu W$ ($V_{sup} = 1.1V$)	$88\mu W$ ($V_{sup} = 1.1V$)
Area occupation	$350\mu m^2$	$640\mu m^2$

	[7]	**[10]**
Technology	$40nm$ LP CMOS	$0.35\mu m$ CMOS
SNR	-	-
Input-referred noise	$131mVrms$	-
Input-referred offset	$< 3mV$	-
Propagation delay	$99ps$	$15ns$
Power consumption	$1.2mW$ ($V_{sup} = 1.1V$)	$30\mu W$ ($V_{sup} = 1V$)
Area occupation	$700\mu m^2$	$900\mu m^2$

5.2. Future Work

- Fifty event samples with Poisson distribution have been collected to test the error rate of the proposed ROIC with passive filter. To get a more trustable result, testing the detection error rate of the proposed ROIC by feeding more input events with Poisson distribution should be done.
- Simulation shows that the discriminator for ROIC with passive filter experiences a slower speed at the SS corner and almost can't fulfill the requirements. Future work could focus on improving the reliability of the proposed discriminator at different process corners by improving the biasing circuit design.
- The threshold of the discriminator is externally generated for the current design. It is convenient to trim the threshold manually through the POT that is biased by the supply voltage. However, the fluctuation of the power supply due to environmental factors will directly reflect the threshold, which results in a change of SNR of the discriminator and may impact the detection accuracy. For future improvement, the threshold could be generated by a bandgap reference or a DAC.
- The current passive filter is the simplest implementation which contains a poly resistor and capacitor. It is able to attenuate the pileup effectively.
- A differential amplifier is used as the gain stage of the current discriminator. Compared to the single-ended amplifier, it could better suppress the noise from the supply. However, it also occupies more area and increases the complexity. For future work, the possibility of using the single-ended configuration as the gain stage could also be explored.

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A

Appendix

Essential equipment involved in the measurement is summarized in Table.A.1.

Table A.1: Essential equipment model number

Name	Productor	Type
NTC thermistor	TDK	B57540G1
Oscilloscope	Tektronix	MSO66B
FPGA board	terasic	DE10-Standard
Multimeter	Keithely	2002
Current source	Keysight	B2912