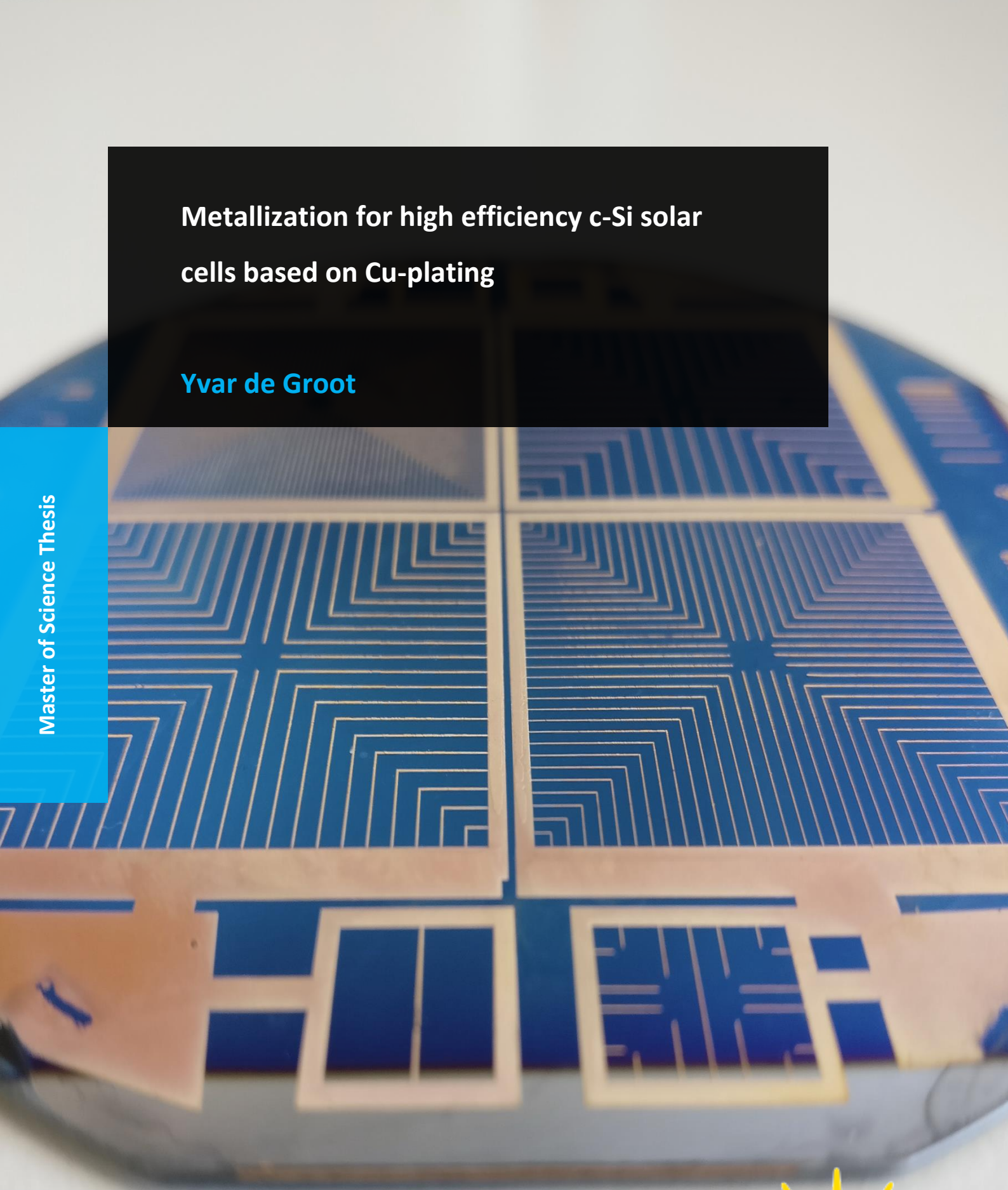
Metallization for high efficiency c-Si solar cells based on Cu-plating

Yvar de Groot

Master of Science Thesis



TU Delft Delft University of Technology

PVMD Delft University of Technology

Metallization for high efficiency c-Si solar cells based on Cu-plating

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Abstract

To improve the performance of the high efficiency c-Si solar cells within the PVMD group several front metallization methods were investigated. The objective was to decrease the series resistance, which would lead to an increase in FF and thus efficiency. Three different cell structure are examined; i) a poly-poly cell with SiN¬x as an ARC, ii) a hybrid solar cell and iii) a silicon heterojunction (SHJ) device. Last two structures have a conductive TCO layer as a top layer.

For the poly-poly device four sorts of front metallization were examined; Al e-beam evaporation, DC Cu-plating, pulse Cu-plating and Al sputtering. Because Al evaporation was the most commonly used metallization method within the group, this will be the reference cell. The best reference cell had as external parameters a VOC of 689 mV, JSC of 38.3 mA/cm2 and a FF of 73.0%, resulting in a efficiency of 19.3%. With DC Cu-plating fingers with significantly higher aspect ratios (up to 0.28 compared to 0.02 of reference), but unwanted growth of Cu was also detected. Nevertheless, it gave an average increase of 2.3% absolute in FF, which resulted in a higher efficiency of 19.6%. In order to remove the unwanted Cu-growth, pulse Cu-plating was done. When pulse plating was done, no unwanted growth of Cu was detected. The efficiency of the pulse plating device was slightly lower than the other two devices. An efficiency of 18.7%. Sputtering of Al proves to have the same result as Al e-beam evaporation, when the same thickness is used.

Regarding the hybrid solar cells the best results was achieved with Al e-beam evaporation, with a VOC of 704 mV, JSC¬ of 40.7 mA/cm2 and FF of 73.8%. This results in a device with a efficiency of 21.0%. With Cu-plating technique and Ag-paste screen printing, these results were not reached. The Cu-plating technique did show an average increase in FF of 1.8% absolute, due to a lower series resistance. Cu contamination however lowered the VOC and JSC.

For SHJ solar cells the reference solar cell had a maximum efficiency of 17.7%, with an average FF of only 61.0%. Cu-plating on SHJ solar cell had de same contamination problems (low VOC and JSC), but because of the 10.9% absolute increase in FF, it showed higher efficiencies (with a maximum of 18.4%. Ag paste screen printing showed a smaller increase in FF (3.4% absolute).

Optical measurements for the rear reflector were done as well. This resulted in an advised rear contact of 100 nm thermally evaporated Ag and 6 µm of screen printed Ag paste.

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1 Introduction

1.1 Crystalline silicon solar cells technology

Although some powerful people still deny the global warming as a result of human activity [1], scientists believe with a probability verging on certainty that the change in climate is truly caused by human activities, especially by the production of carbon dioxide. In order to stop this global warming of the earth, it is from vital importance that the CO_2-production is reduced a lot. This can be done by replacing fossil fuels, which has a big impact on the production of CO_2, by more ecofriendly power sources. Besides the environmental impact of the use of fossil fuels, the growing population and energy demand and decrease in fossil fuel reservoirs, also necessitates us to search for other ways of producing power, whereas the fossil fuel supplies will not meet this growing demand in the future [2] [3].

One of the fastest growing technologies on the sustainable energy market is the photovoltaics (PV) market [4] [5]. The cumulative installation of PV modules grew up to 306 GW_p by the end of 2016 [4]. Most of this installed power is made by PV panels based on mono- or poly crystalline silicon (c-Si) solar cells, as illustrated by in Figure 1.1.

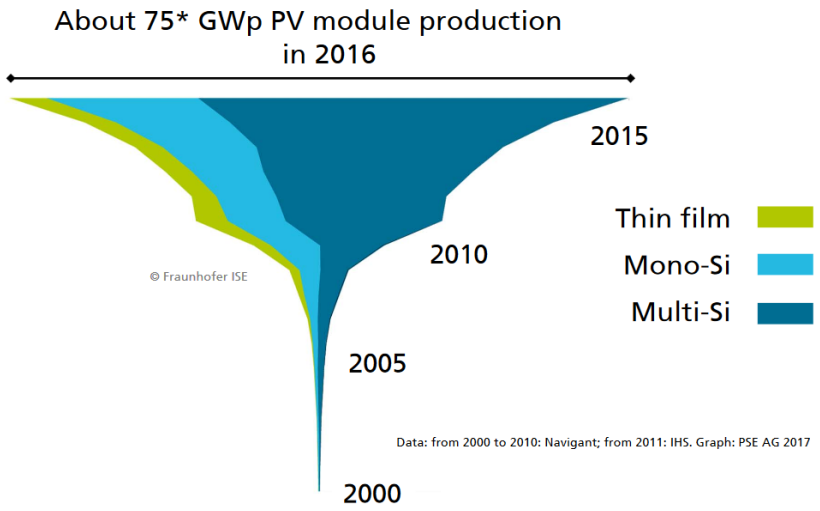


Figure 1.1 Annual PV production worldwide in GW_p. Note: The 75 GW_p in 2016 is an approximation [6]

The working principle of a c-Si solar cell, or any solar cell for that matter, is that photon, which are particles of light, can have enough energy to excite an electron (a negatively charged particle) for a full band (the valence band) to an empty band (called the conduction band). This leaves a space in the valence band what is called a hole, which is positively charged. So, in other words, a photon

creates an electron/hole pair. By making junctions in the design of the semiconductor, the created hole and electrons are both collected on the opposite side of the cell, as is shown in Figure 1.2.

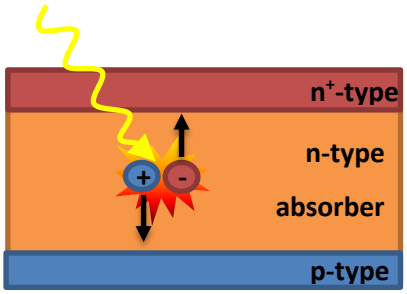


Figure 1.2. Electron (-) and hole (+) separation after a e^-/h^+ pair was created by a photon

If these opposite sides are then connected to an external circuit, they will use this circuit to recombine and thus make a current. The height of the difference between the valence and conduction band is called the band gap. This is a material property of the semiconductor and will affect the potential difference. It will also have influence on the amount of photons that are suitable to excite an electron; The bigger the bandgap, the bigger energy needed for exciting an electron, the less photons are suitable for creating such an electron/hole pair. Metal contacts on the front and rear are placed to collect these carriers (electrons or holes), so the connection with the external circuit can be made. A PV module consists of an amount of solar cells that are connected with each other.

This metallization of solar cells is, in industry, mostly done by screen printing of a silver (Ag) paste. This technique will be further discussed in chapter 2. The raw material that is used for this metallization is very conductive silver. The downside however is that the silver is also quite expensive. So, in order to decrease the price of solar cells, scientists are looking into other metallization techniques which will not harm the efficiency of the cells, but do decrease the price [7]. One of these possible solutions is copper (Cu). Copper is almost as conductive as silver, but is al lot cheaper [8] . This research will also focus on the metallization of c-Si wafer based solar cells. The goal of this project is to develop new metallization schemes to improve performances of devices at PVMD.

1.2 External parameters

Some figures of merit are used to evaluate a solar cell performance. They are commonly called external parameters. Usually efficiency is defined as fraction of incoming light that is transformed into electrical energy. To calculate efficiency, open-circuit voltage (V_{OC}), short-circuit current density (J_{SC}) and Fill Factor (FF) need to be evaluated as well. Since a solar cell is basically a diode working in forward-bias, the current-voltage equation that is regulating this device is;

$$J = J_0(\exp\left(\frac{V}{V_t}\right) - 1) - J_{ph} \quad (1.1)$$

Where J_{ph} is the photo-generated current, J_0 saturation current density and Vt is thermal voltage. The following paragraphs will describe in detail the definition and the physical meaning of external parameters.

1.2.1 Open circuit voltage

Open circuit voltage (V_{oc}) is the maximum potential that the solar device has. This maximum voltage occurs at open circuit situation, so when no current is flowing through the external circuit. The V_{oc} can be calculated when the current is set to zero. This results in the following equation for calculating the open circuit voltage;

$$V_{OC} = V_t \ln\left(\frac{J_{ph}}{J_0} + 1\right) \quad (1.2)$$

in which V_t is nKT/q and n is the ideality factor, k is the Boltzmann's constant, q is the elementary charge, J_{ph} is the photo-generated current density and J_0 is the dark saturation current density. It shows that V_{oc} depends on the photo-generated current and the saturation current. The saturation current plays an important role, whereas it can vary by orders of magnitude. This saturation current, or dark current, is a part of the reverse current in a p-n junction caused by minority carriers diffusion from the neutral regions to the bulk. The bulk will therefore have a lower concentration of majority carriers, due to recombination with the minority carriers. To have a high V_{oc}, this saturation current should be as low as possible, which means that the recombination in the solar cell should be as low as possible. And vice versa a low V_{oc} means that the recombination within the cell is (too) high. Lab-scale crystalline silicon solar cells have achieved V_{oc} up to 730 mV under standard AM1.5 conditions, while a commercially available cell has a V_{oc} that can exceed 600 mV. [9]

1.2.2 Short circuit current density

The short circuit current density, J_{sc}, is the maximum current that can be drawn from the solar cell. This occurs when the electrodes of the solar cell are short circuited, which results in a voltage of zero. The J_{sc} depends on a number of factors, like the power of the incident light source, the spectrum of the incident light source and optical properties and collection probability of the solar cell. For commercially available solar cell, a general measurement criteria is given as STC (Standard test condition). In this condition the AM1.5 spectrum is used with an intensity of 1000 W/m^2 at 25° C. The optical properties, like reflection and absorption, depend on the design of the solar cell. The collection probability depends mainly on the surface passivation and the minority carrier lifetime in the base of the cell. These last two material parameters are most critical when comparing Silicon

solar cells, whereas the bandgap and spectrum remain the same for the measurements. Crystalline silicon solar cells can deliver a maximum theoretical J_{sc} of 46 mA/cm^2 under STC. So far, in laboratory the maximum measured J_{sc} is above 42 mA/cm^2, while industrial produced cell exceed 35 mA/cm^2 [9].

1.2.3 Fill factor

Although both the open circuit voltage and the short circuit current density are the maximum of respectively the potential and the current, it is not possible to extract any power for the cell at these points. At J_{sc} the voltage is zero and at V_{oc} the current is zero. Power is best extracted at the maximum power point; the point where the product of the voltage and the current is maximum. The corresponding current density and voltage are called J_{mpp} and V_{mmp}, respectively. The product of these parameters is the maximum power (P_{mpp}). The Fill Factor, or FF, is the ratio between the product of the two maximum power points of the solar cell and the V_{oc} and J_{sc} and can be calculated with the following equation;

$$FF = \frac{J_{mpp}V_{mpp}}{J_{sc}V_{OC}} \qquad (1.3)$$

The FF says something about the 'squareness' of the J-V curve, which will be discussed in more detail in the following paragraph. A high FF means that the J-V curve is rather squared which means that the P_{mpp} is close to the product of the J_{sc} and V_{oc}.

When it is assumed that the solar cell behaves like an ideal diode, the maximum FF can be expressed as a function of open circuit voltage V_{oc},

$$FF = \frac{v_{oc} - \ln(v_{oc}+0.72)}{v_{oc}+1} \quad (1.4)\ [10]$$

With

$$v_{oc} = V_{OC}\frac{q}{k_B T} \quad (1.5)$$

The

$voc - \ln(voc+0.72)voc+1$ (1.4 is a good approximation of the maximum value of the fill factor.

1.3 Characterization techniques

1.3.1 Illuminated J-V

The performance of a solar cell and its external parameter are determined by an J-V curve of an illuminated solar cell. This J-V curve follows the J-V relation given in the equation 1.1. In this equation the J_0 term describes the dark diode current density. The J_{ph} is the photo generated current density. However, the influence of the FF is not taken into account. In order to make the relationship more fitting to reality, the two components that influence the fill factor must be included; the series

resistance, R_s, and the shunt resistance, R_{sh}. This results in the one diode equivalent circuit, shown in Figure 1.3, which, after flipping the polarity of the current, results in the following relationship

$$J(V) = J_{ph} - J_0\left[\exp\frac{q(V-AJR_S)}{k_BT} - 1\right] - \frac{V-AJR_S}{R_{sh}} \qquad (1.6)$$

where A is the area of the solar cell. When one also wants to include the additional recombination that occurs in real solar cells, a two-diode circuit can be used to simulate the working of the cell. For this research however, the one diode equivalent circuit is enough to understand the effects of the experiments.

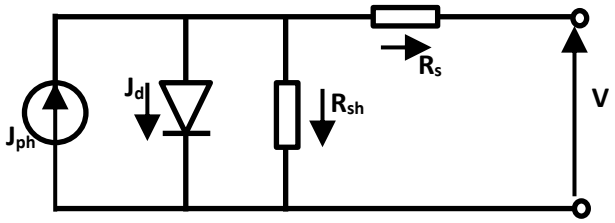


Figure 1.3. The one diode equivalent circuit.

In

Figure 1.4 a typical J-V curve (blue line) can be found. The red line shows the power curve. The blue area represents the power that is extracted from the solar cell when working at maximum power point. An increasing FF will result in a smaller difference between the V_{oc}/J_{sc} and V_{mpp}/J_{mpp}, which will increase the 'squareness' of the J-V curve. This will increasing the blue area which means an increase in power.

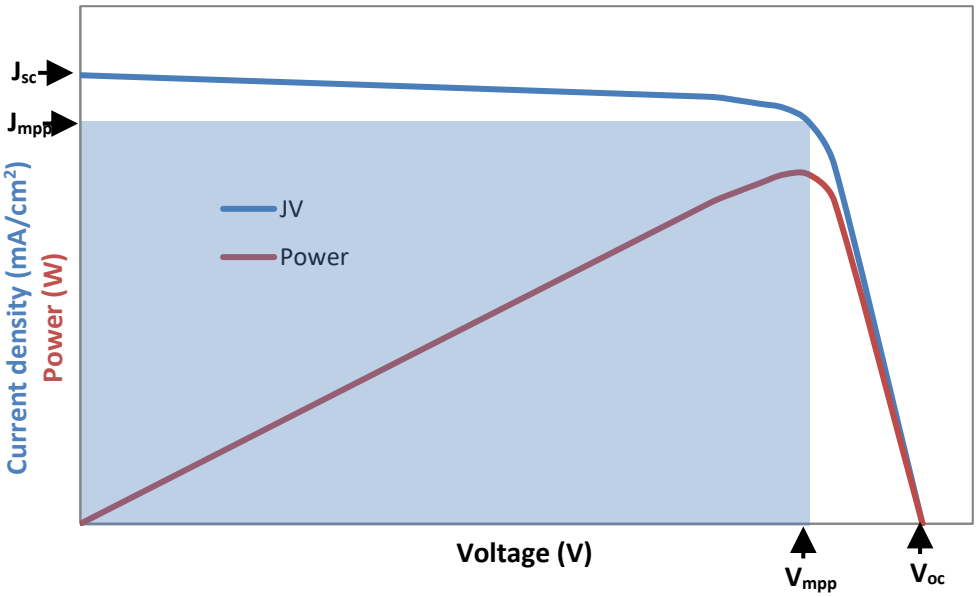


Figure 1.4. A typical JV and power curve with a V_{OC}, V_{mpp}, J_{sc} and J_{mpp}

1.3.2 External quantum efficiency

The external quantum efficiency (EQE) is the fraction of photons that successfully creates a collected electron-hole pair in the absorber layer for a certain wavelength. Because the EQE is wavelength dependent it is mostly measured by illuminating the cell with monochromatic light (a light that only emits photons with one particular wavelength). The photo generated current is then measured and the EQE is calculated with the following equation

$$EQE(\lambda) = \frac{I_{ph}(\lambda)}{q\psi_{ph,\lambda}} \qquad (1.7)$$

In which q is the elementary charge and $\psi_{ph,\lambda}$ the spectral photon flow incident on the solar cell. The shape of the EQE-λ curve depends on the optical and electrical losses. The optical losses are determined by parasitic absorption and reflection and the electrical losses caused by recombination. Parasitic absorption consist of photons absorbed by an inactive layer, such as the anti-reflection coating on top of the wafer or highly doped layers. A EQE-λ curve of a high-quality c-Si based solar cell is shown in Figure 1.5. Here it is shown that in the short and long wavelengths range, the EQE is relatively low. Parasitic absorption of the top layers is the mean reason for the EQE losses in the short wavelengths range. In longer wavelengths, the penetration depth of the photon exceeds the optical thickness of the bulk layer. This means that the bulk layer becomes more or less transparent for the photon and the photon will therefore leave the cell before it successfully creates an electron-hole pair that can be collected. Photons with λ > 1100 nm have smaller energy than the silicon bandgap ($\lambda_{bandgapSi}$ = 1100 nm), so it is less likely that they are absorbed.

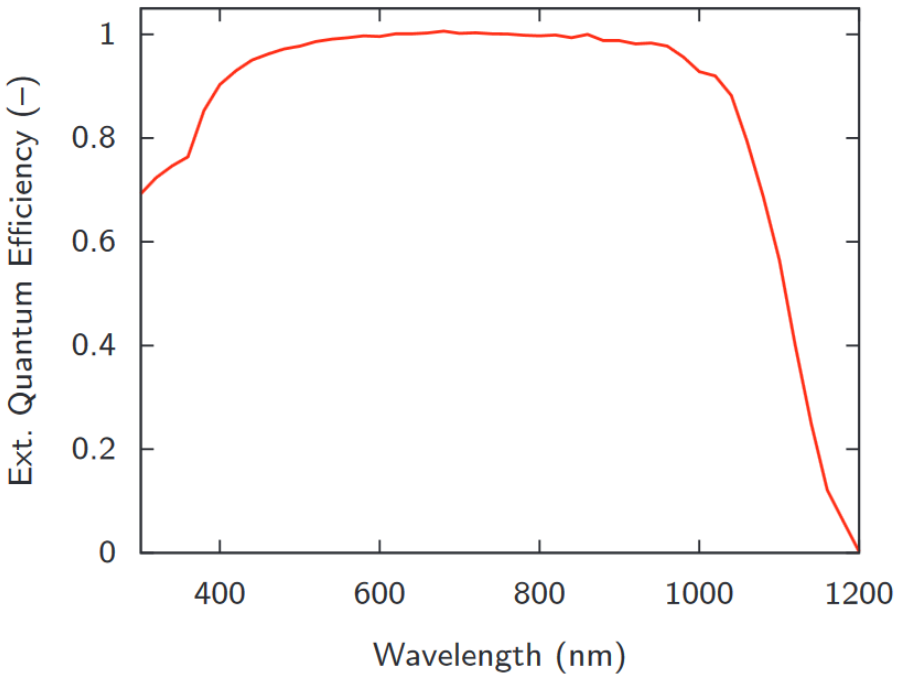


Figure 1.5. The external quantum efficiency of a high-quality c-Si solar cell [9]

1.3.3 Reflectance, transmittance and absorption

In order to have as high as possible absorption of photons with $\lambda < 1100$ nm, the absorption of the absorber layer should be as high as possible. Texturing at the front surface of the solar cell is one of the ways to increase light-trapping. Texturing means that random pyramids of micrometric size are made on the front surface. These pyramids ensure that less light is reflected back into the air when it hits the cell, as is shown in Figure.1.6 a). Another way of reduce the reflectance and thus increasing the light trapping is by using an anti-reflection coating (ARC). This coating has two important parameters; the refractive index and the thickness. The refractive index of the ARC depends on the refractive indexes of both the surrounding material (like air or glass) and the Silicon. The thickness of the ARC is chosen so that the wavelength in the coating is one quarter of the wavelength of the incoming wave. There are dielectric coating, like e.g. SiO_2 and SiN_x, but also conducting anti-reflection coatings, which are called Transparent Conducting Oxides (TCO).

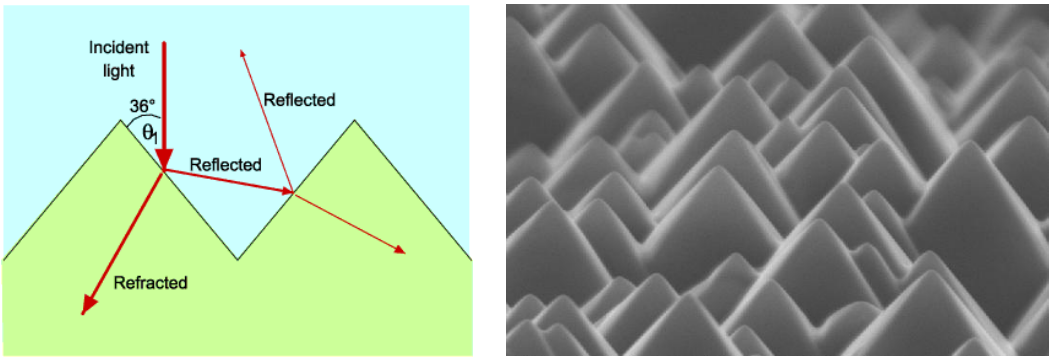


Figure.1.6. a) Pyramids ensure a higher light trapping b) Pyramids on Silicon surface, photographed by a Scanning Electron Microscope [11]

For mono-facial solar cells, i.e. cells with a fully metalized rear, rear-reflectance is also important. With rear-reflection, photons that traveled through the entire bulk without creating an electron-hole pair are reflected back into the bulk, so it again has a chance to create an electron-hole pair. An ideal rear-metal, optically-wise, should have a very high reflectance, and therefore a low parasitic absorption. The rear-reflectance is especially important for the photons in the long wavelengths range. The absorption depth, which describes how deeply light penetrates into the semiconductor before being absorbed, is larger for photons with longer wavelengths; blue light will be absorbed at the top of the bulk, whereas red light will most likely be absorbed at the bottom of the bulk.

Even with all these tricks to trap light, the absorption of crystalline Silicon is quite low when compared to other semiconductor materials. This is because c-Si is an indirect band gap material. This means that the lowest point of the conduction band is vertically not aligned with the highest point of the valence band. This means that when a photon excites an electron in the highest point of the valence band, it needs an additional horizontal *push* to get to the lowest point of the conduction band, otherwise the exited electron will just *fall* back to the valence band. This *push* is given by the

vibrations of the crystal lattice and is called a phonon. A semiconductor with a direct bandgap has the highest point of the valence band and the lowest point of the conduction band vertically aligned and therefore does not need a phonon. Therefore the chance of successfully collecting an electron-hole pair is much higher in a direct bandgap material when compared to indirect bandgap material. The upside of having an indirect bandgap material is that the radiative recombination is also very low [9]. The absorption coefficients of several semiconductor materials are given in Figure 1.7. The red Si-line shows the rather low absorption coefficient compared to other semiconductor materials. This is the reason why crystalline Silicon based solar cells need to be relatively thick.

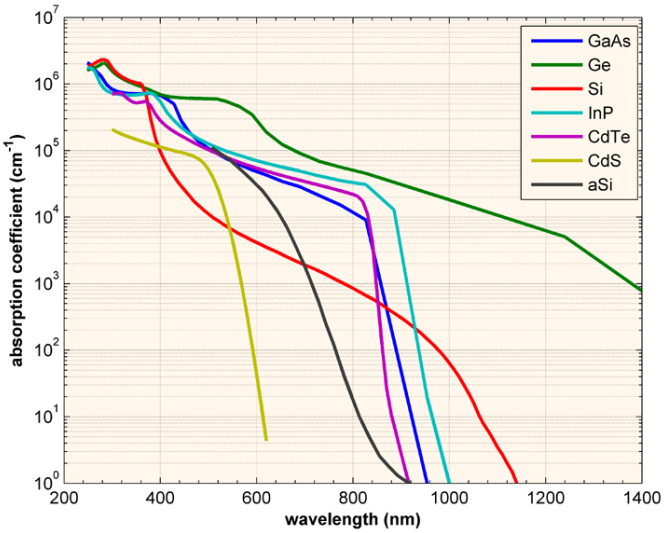


Figure 1.7. The absorption coefficients of several semiconductor materials [11]

1.3.4 SunsV$_{OC}$ and pFF

The SunsV$_{oc}$ is a measurement method for the J-V-curve of a solar cell without the influence of series resistance. The SunsV$_{oc}$ measurement uses a separate solar cell to monitor the illumination intensity. This separate cell, or monitor cell, simplifies the measurement electronics because only the cell voltage needs to be measured, which is easier than the cell current. A flash lamp with slow decay is used for the SunsV$_{oc}$ measurement. This measurement can be taken very fast. With this method the SunsV$_{oc}$ can be measured, as well as the pseudo Fill factor (pFF). Both these parameters are the V$_{oc}$ and the FF values when series resistance would not play a role; the V$_{oc}$ and FF of a cell with a R$_s$ of zero. These SunsV$_{oc}$ and pFF show the potential of the solar cell and, when compared to the real V$_{oc}$ and FF, show the influence of the series resistance.

1.4 Analysis of Fill factor

1.4.1 Shunt resistance

The shunt resistance is one of the factors that has a large influence on the fill factor. It is the resistance that the solar cell has to shunt and, as shown in Figure 1.3, can be seen as a parallel resistance in the circuit. This means that a higher resistance will benefit a good FF. A shunt in a solar cell can be seen as an alternative path for the current with respect to the p-n junction. Instead of following the external circuit, part of the photo generated current stays within the cell and will therefore not contribute to the drawn power of the solar cell. The influence of the shunt resistance is mainly visible in the lower voltages regions, where the effective resistance of the solar cell is high. The slope of the J-V-curve at short-circuit current condition (V=0 V) indicates how important is the effect of shunt resistance. If the horizontal part of the J-V-curve is flat, the shunt resistance is very high, whereas a titled line indicates a low shunt resistance, as visualized in Figure 1.8.

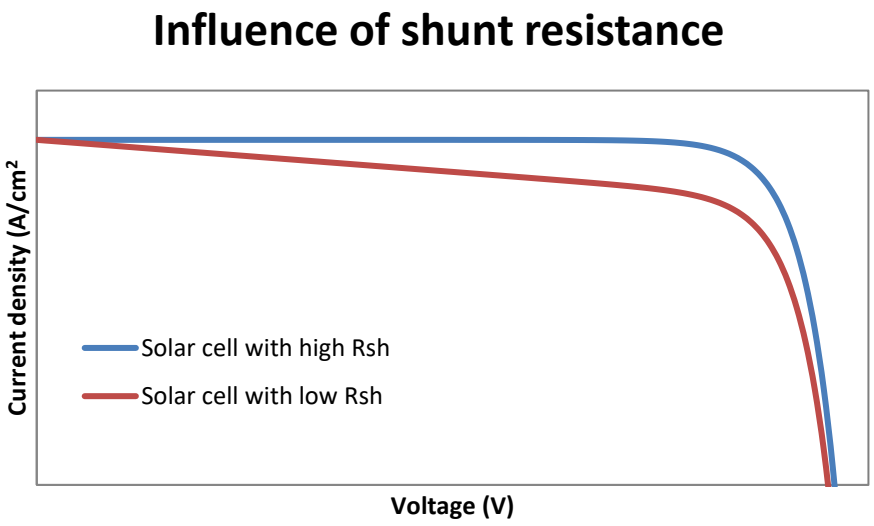


Figure 1.8. The difference between a solar cell with a very high (blue) and low (red) shunt resistance, if R_s is assumed zero.

Typically a significant power loss because of a low shunt resistance is caused by a manufacturing fault and not so much by poor cell design.

1.4.2 Series resistance

The other factor that influences the Fill factor is the series resistance, R_s. As shown in Figure 1.3, the series resistance acts like an, as the name already says, resistance in series. This means that the FF would benefit from a very low series resistance. The series resistance consists of three components; The lateral resistance, the contact resistance and the metal resistance. All components will be further discussed in more detail in the coming paragraphs.

The series resistance does not affect the solar cell at open circuit voltage condition, because there is no current. Close to the open circuit voltage however, the influence of the R_s is quite large. By looking at the slope of the vertical line in the J-V-curve at open-circuit voltage condition, the influence of the R_s can be analyzed; the more vertical the right side of the curve (or more steep), the less the influence of the series resistance, as is visualized in Figure 1.9.

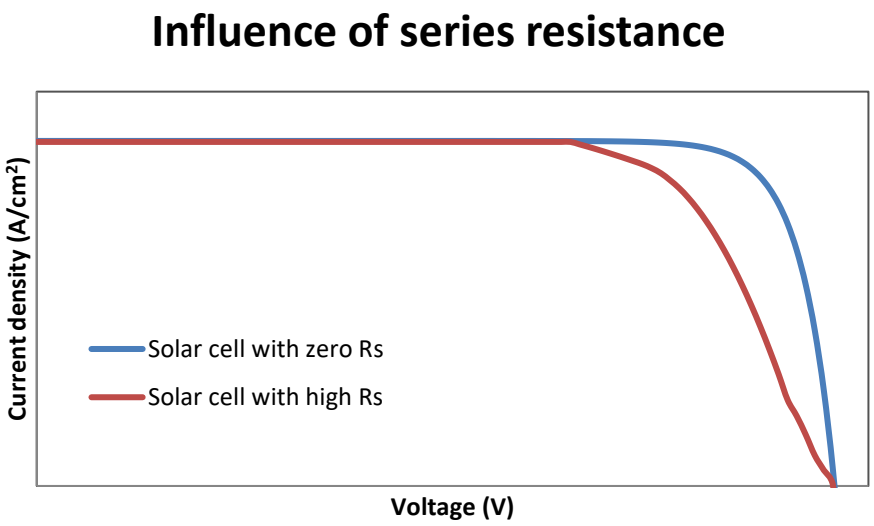


Figure 1.9 The difference between a solar cell with a very low (blue) and high (red) series resistance, if R_{sh} is assumed 10^4 Ohm/cm^2.

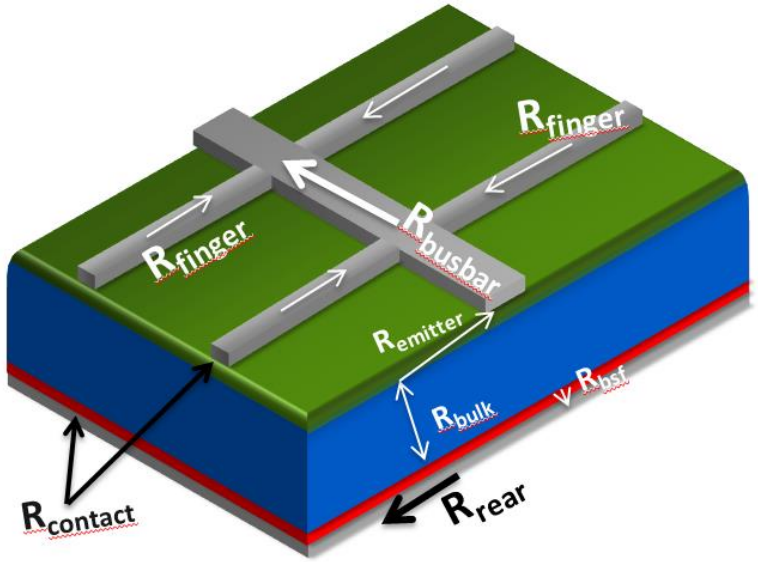


Figure 1.10 The components that contribute to the series resistance

1.4.2.1 Metal resistance

The metal resistance is the resistance that the current will undergo when it travels through the metal of the fingers of busbar. It is a specific property of metal used for solar cell application. In Figure 1.10

the components are shown as R_{busbar}, R_{finger} and R_{rear}. The resistance of a metal bar can be calculated with

$$R_m = \frac{\rho L}{A} \qquad (1.8)$$

With

$$\rho = \frac{1}{\sigma} \qquad (1.9)$$

In which R is the resistance, σ the electrical conductivity, l is the length and A is the area of the section of the finger, busbar or rear. It shows that the area of the section, which is the product of the height and width of the finger or busbar, should be as big as possible to reduce the resistance of the metal. This is especially important for the front contacts, because the area of the rear contact is already very large and thus the metal resistance low. The length of the path that the carries need to travel to the electrode increases the resistance. The last parameter is the electrical conductivity, which is a material property. In Table 1.1 the conductivity of several metals can be found. A high conductivity decreases the resistance within the metal, so metals with a high conductivity are preferred for metallization of solar cells, although more factors play a role when a metal needs to be chosen.

Table 1.1 The electrical conductivity of several metals

Metal	**Conductivity at 20° C [x10^7 S/m] [12]**
Carbon (graphene)	10.0
Silver	6.30
Copper	5.96
Annealed copper	5.80
Gold	4.10
Aluminum	3.50
Nickel	1.43
Titanium	0.24

1.4.2.2 Contact resistance

The contact resistance, R_c, is the resistance a current has to flow from one layer to another. The contact resistance can be measured with a Transfer Length Method, which will be discussed in more detail in chapter 2.2.5. The contact resistance can be calculated with the following equation

$$R_c = \frac{\rho_c}{L \times W} \qquad 1.10 \text{ [13]}$$

In which L x W is the contact area of the two layers and ρ_c is the specific contact resistance between the two layers. This the two layers. This contact resistivity depends for a large part on the band diagram of junction between the metal and

between the metal and the semiconductor. There are two types of metal/semiconductor junctions; The rectifying and non-rectifying type. The first theory about metal-semiconductor contacts that was generally accepted was decribed by Schottky, who introduced a notion of a potential barrier at the interface [14]. According to the Schottky model, the Fermi levels of both the semiconductor and metal need to be equalized via charge transfer. This results in a bending of the energy band diagram, as is shown for an n-type semiconductor in

Figure 1.11. The Schottky barrier, ϕ_{Bn} for n-type, can be calculated with the equation

$$\varphi_{Bn} = \varphi_m - \chi \qquad (1.11)$$

with ϕ_m is the metal work function and χ the electron affinity, which is the distance between the vacuum level and the edge of the conduction band. The difference between the metal work function and the work function of the semiconductor, ϕ_s, gives the built-in voltage;

$$V_{bi} = \varphi_m - \varphi_s \qquad (1.12)$$

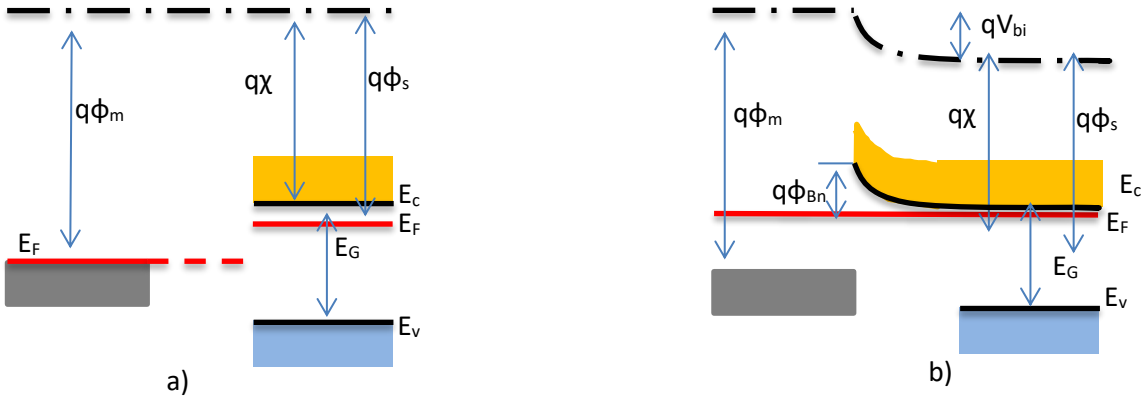


Figure 1.11. The Metal-semiconductor junction before (a) and after (b) contact.

For p-type materials the Schottky barrier can be calculated with

$$\varphi_{Bn} = \frac{E_G}{q} - (\varphi_m - \chi) \qquad (1.13)$$

Where the E_G stands for the band gap energy of the semiconductor. In order to have an as low as possible contact resistivity, one should try to make an ohmic contact. In this case, the resistance of the metal-semiconductor is negligible with respect to the bulk resistance in the semiconductor. A figure of merit for the specific contact resistance at zero bias voltage is

$$\rho_c := \left(\frac{\partial J}{\partial V}\right)^{-1}_{V=0} \qquad (1.14)$$

When there is a (low) doping concentration up to $1*10^{17}$ cm^{-3}, the thermionic emission is dominant [15]. The specific contact resistance can be calculated with$\rho_c = \frac{k}{eA^*T}\exp\left(\frac{q\varphi_{Bn}}{k_B T}\right)$ (1.15. This equation shows that the Schottky barrier should be as low as possible in order to keep the resistivity as low as possible.

$$\rho_c = \frac{k}{eA^*T}\exp\left(\frac{q\varphi_{Bn}}{k_B T}\right) \qquad (1.15)\ [16]$$

When the doping concentration is higher than $1\cdot10^{17}$ cm^{-3}, the width of the depletion region will decrease and the probability for quantum tunneling become significant. In this cause, tunneling can

become the major current transport mechanism. When this is implemented in the previous equations, the specific contact resistance becomes

$$\rho_c \propto \exp\left(\frac{4\sqrt{m_n^*}\varepsilon_s\varphi_{Bn}}{\sqrt{N_D}\hbar}\right) \quad (1.16)$$

It

1.4.2.3 Lateral resistance

The lateral resistance is the third major contributor to the series resistance. It consists of the emitter, bulk and back surface field resistance. Where bulk and back surface field resistances are 1-diminsional (carrier only need to travel vertically), carriers in the emitter need to travel 2-diminsional in order to reach the metal fingers. These resistances depend on the diffusion length in the layer. The longer the diffusion length, the smaller the chance of recombination, thus the lower the resistance. The resistance of the bulk and BSF can be calculated with $Rm = \frac{\rho L}{A}$ (1.8, in which the l is now the width (or thickness) of the layer and the ρ is the resistivity of the semiconductor, which in case of Silicon is between 0.5 – 5 Ω cm for a typical solar cell. [11] Because of the two dimensional flow of carriers in the emitter, the length that they need to overcome is bigger than the width of the layer. The total length is depending on the space between two fingers; the more *finger spacing* the longer the transport length, thus the higher the emitter resistance.

1.5 Limiting factors for low series resistance

1.5.1 Front contacts

Front contacts are the contacts on the front of the wafer. Because the front of the solar cell is illuminated, the front contacts reflect the light before it can enter the absorber layer. This is called shading, which will be discussed in more detail in the next paragraph.

1.5.1.1 Shading

As is discussed in previous paragraphs, a high coverage on the front side (> 10%) of thick metal will have a positive influence on the FF of the solar cell. However, a large area of metal decreases the illuminated area of the silicon itself, because the metal reflects light back into the air. This is illustrated in Figure 1.12. Although the metal raises the fill factor, it decreases the illuminated area and therefore the current density of the solar cell. Therefore a metal grid is always a tradeoff between a maximum fill factor and a maximum current density. This tradeoff is illustrated in the graphs of Figure 1.13, in which (a) shows that an increase in the distance between two fingers gives lower shading (and thus higher J_{sc}), but it also increases the emitter resistance (and thus the lateral resistance). Graph (b) shows the effect of the finger width; an increase in width causes a decrease in contact/metal resistance, but an increase in shading. Typical industrial front grids consist of small

fingers to collect the carriers from the emitter and thicker busbars, which collect the current from the fingers and transport it to the electrode of the external circuit or to connect the cell in series with the next one.

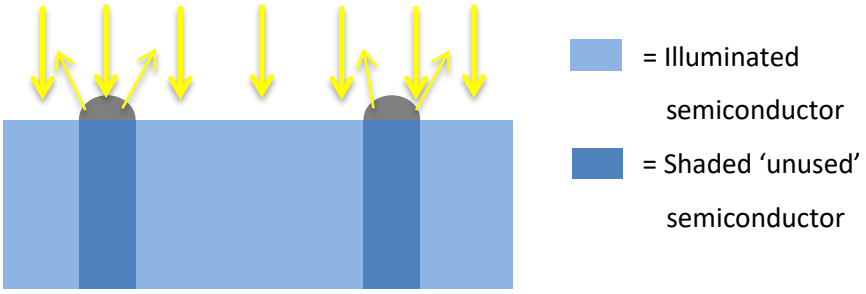


Figure 1.12. Metal front contacts cause shade in the semiconductor layer

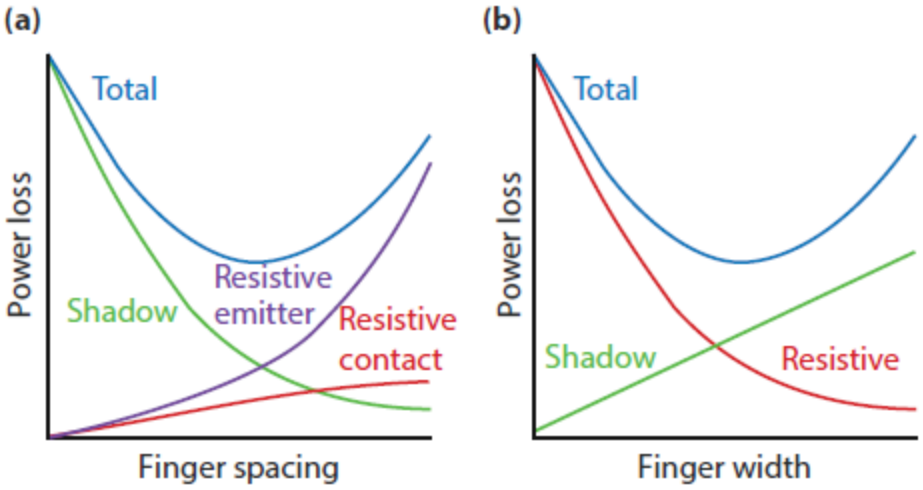


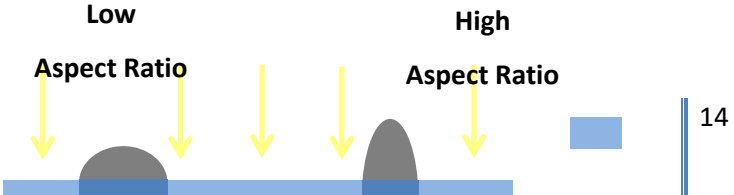
Figure 1.13. Power loss due to (a) finger spacing and (b) widths of the metallic fingers on top of a c-Si solar cell [9]

1.5.1.2 Aspect ratio

One way to decrease the resistive of the metal without increase the shading (so push the red line of Figure 1.13 b) to the left), is to increase the aspect ratio of the metal. The aspect ratio is the ratio between the height and the width of the finger and can be calculated with the follow equation

$$\text{Aspect ratio} = \frac{\text{Height}}{\text{Width}} \qquad (1.17)$$

By



= Illuminated

semiconductor

= Shaded 'unused'

semiconductor

Figure 1.14. The impact of a low (left contact) and high (right contact) aspect ratio

1.5.2 Rear contacts

Because shading is not an issue at the rear for mono-facial solar cells, the back can be fully metallized. Therefore the area of the semiconductor-metal junction is quite large and so the specific contact resistance of the junction is less important, as can be concluded from $Rc = \frac{\rho_c}{L \times W}$ 1.10; the contact area (the denominator of the equation) of the metal-semiconductor junction is very big, so the influence of the ρ_c (the numerator) is smaller than for front contacts. However, it is still important to have an a low as possible build-in voltage at the rear of the cell. This is done by choosing a metal with a work function that is close to the work function of the contacting layer.

Besides collecting and transporting carriers, the rear contact has another function; it can act like a back reflector which reflects unused photons back into the bulk, as shown in Figure 1.15. A photon that did not succeed to make a success electron-hole pair, is reflected back into the bulk and can try to excite an electron again. An ideal rear metal has a high reflectance and low parasitic absorption and transmittance.

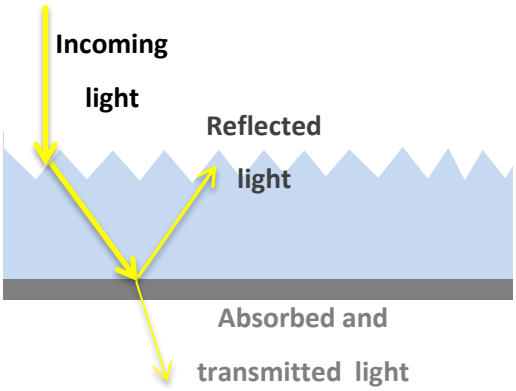


Figure 1.15. The reflecting properties of the rear metal

1.6 State of the art in metallization techniques

In industry, the most common metallization technique is screen printing with firing silver paste [17]. This technique is very fast and can be done on the non-conducting ARC layers that are used in

industry. By annealing ('firing') the paste following a very specific temperature swing, the paste etches the ARC layer (typically SiO_2/SiN_x stack) and makes contact with the emitter. The problem with the screen printing of silver paste is that it has a rather low aspect ratio, which is mainly caused rheology of the chosen paste [18]. Screen printing has also an issue with contacting poly-Se, as explained in [19], in which poly-Si can be penetrated if too thin. By dispensing the silver paste with a dispenser instead of screen printing, the aspect ratio of the fingers can be increased, which leads to an absolute efficiency increase of maximum 0.3% [20]. The rear p-type solar cells is mostly done by an aluminum paste in commercial application [21]. This method is preferred because the aluminum can be used to create a back surface field when it is annealed. [22] The aluminum rear will have some silver busbars as well, for soldering purposes. The rear can also be done with full area silver paste, although this cannot be used to dope the rear as well.

Another metallization process for the front is light induced copper plating (LICP) on a electroless plated seed layer, most commonly Nickel (Ni). For this concept, first a Nickel seed layer is plated in an alkaline nickel plating bath. This process is an autocatalytic process which will only require an temperature of 35-50° C and a pH of around 10 [23]. After depositing the Ni, the substrate is annealed for 30 seconds at 350° C to form a nickelsilicide contact. This nickelsilicide has a very low contact resistance with highly doped n-type silicon. After annealing, the solar cell is placed in a copper plating bath and is illuminated. The electricity production of the solar cell is then used to plate copper on nickel. Although this process is not yet fully controllable, it does have a high potential to be implemented in industry whereas it has a production cost which is much lower than silver screen printing.

1.7 Scientific questions

The aim of this thesis is to further improve the performances of solar cell devices made within the PVMD group by finding and (re-)introducing more optimum ways of metallization. Several front contact metallization methods on different top layers will be examined and compared, which will result in an advise for every different top layer. The four metallization methods that will be investigated will be:

1. *Standard* Aluminum e-beam evaporation,
2. Aluminum sputtering,
3. Silver paste screen printing,
4. Copper plating on a seed layer.

The ultimate goal of this research will be to find an as high as possible fill factor without decreasing the other parameters of the cell. In order to reduce the use of expensive evaporated Silver on the back, a rear reflection test will also be done.

That results in the following research question:

- **Which metallization method is preferred for metallization with a non-conductive anti-reflection coating on a n-type layer?**
- **Which metallization method is preferred for metallization on a conduction top-layer?**
- **Which rear metal stack has the best reflection properties?**

1.8 Outline of this thesis

This thesis will consist of six chapters. In Chapter 1 an introduction into crystalline solar cells will be given and the theoretical background of solar cell parameters will be discussed, as well as the State of the art techniques in metallization and the aim and scientific questions for this thesis.

Chapter 2 will discuss the techniques that have been used to fabricate different solar cells. It is assumed that this thesis starts after the fabrication of the working layers of the cells, so only the metallization steps will be discussed.

Chapter 3 will give the results of the different metallization methods on a poly/poly solar cell with an non-conductive ARC. The three metallization methods that will be examined are Al evaporation, Al sputtering and copper plating on titanium.

In chapter 4 poly/poly devices with a conductive top layer will be metallized. The two different top-layers are IOH and ITO and the metallization techniques that will be examined are Al evaporation, Ag screen printing and Cu plating on Ti.

Chapter 5 will give the results of a reflectance test. The reflectance of several different metal stacks will be examined and compared.

The last chapter, chapter 6, will give the conclusions of this work, answer the research questions and will also give some recommendations for future work.

2 Experimental setup

2.1 Fabrication process

This research will mainly focus on the metallization part of the solar cell. Because of this only the processes that are used to metallize will be discussed in the chapter. It is assumed that the experiments start with a working device with an anti-reflection coating, also known as solar cell precursor.

2.1.1 Photolithography

In research, photolithography is used to define the position of the fingers and bus bar and/or to protect layers against copper diffusion during the copper plating process. This photolithography process deals with transferring geometric patterns on a mask to a thin photo-sensitive organic material called photoresist. There are two different types of photoresist, positive and negative. Positive photoresist will become more soluble when exposed to light with small wavelengths, whereas negative photoresist needs a light treatment to not be dissolved in the developer. Photolithography takes place in a *Yellow room* (a room with yellow light), because the photoresist is not harmed by low energy photons. The process is illustrated in Figure 2.1. The process begins with putting the wafer on a spinner (a), dispensing some photoresist on the wafer and let it spin at various speeds to get a homogenous distribution of the photoresist (b). Next, the wafer is baked for 5 minutes at 100° C to remove the solvents and harden the photoresist (c). Thereafter, a mask with a transparent geometric pattern is placed on top of the wafer and it is being illuminated by UV-light

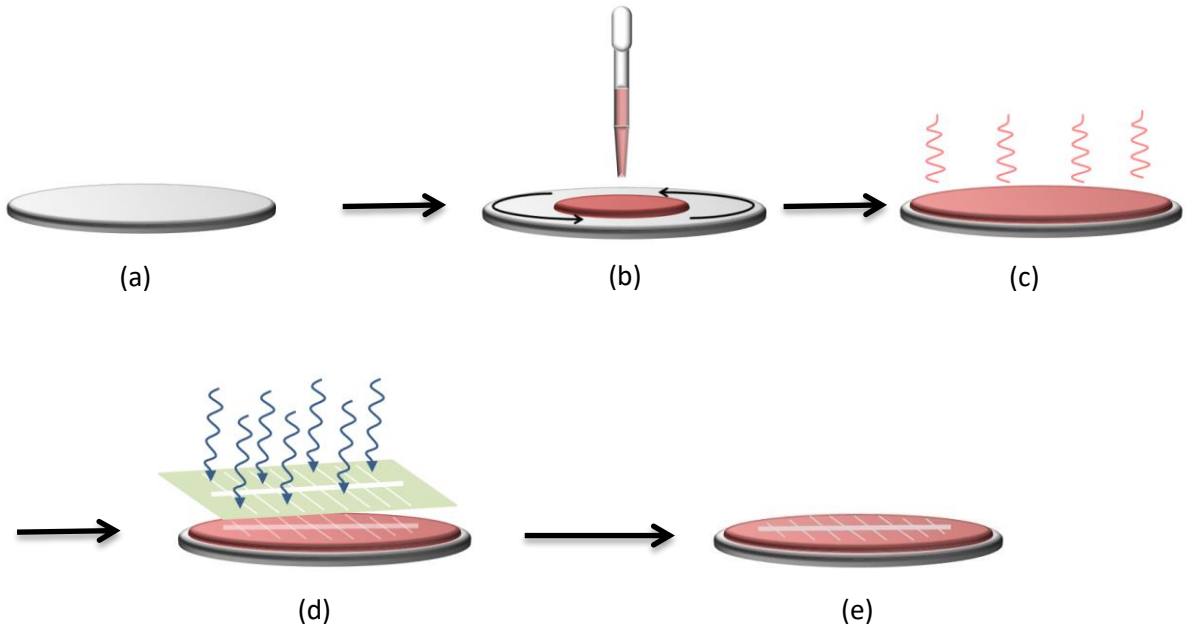


Figure 2.1. The photolithography process of positive resist; (a) the wafer (b) spin coating of photoresist (c) Baking of the photoresist (d) exposure under UV light (e) Development dissolves the illuminated photoresist

(d). The time of exposure depends on the thickness of the photoresist layer. During the last step the photoresist is developed. During this process the illuminated photoresist is being dissolved in the developer solution.

During this research two different types of photolithography were used; The automatic EVG 120 Coater-developer for steps a, b, c and e and the EVG 420 Contact Aligner for step d. This is in the Cleanroom of the *Else Kooi Laboratory (EKL)*. The other type is manual photolithography, this is done in the MEMSlab. Here a Convac Spinner is used for spin coating, a hotplate for baking and the Karl Suss MA6 contact Aligner for the alignment and exposure. The used positive photoresist is Shipley SPR3012 and the developer solution was a mixture (ratio 1:3) of AZ 400K developer and water.
For the photolithography two different masks can be used, of which the result is shown in Figure 2.2.

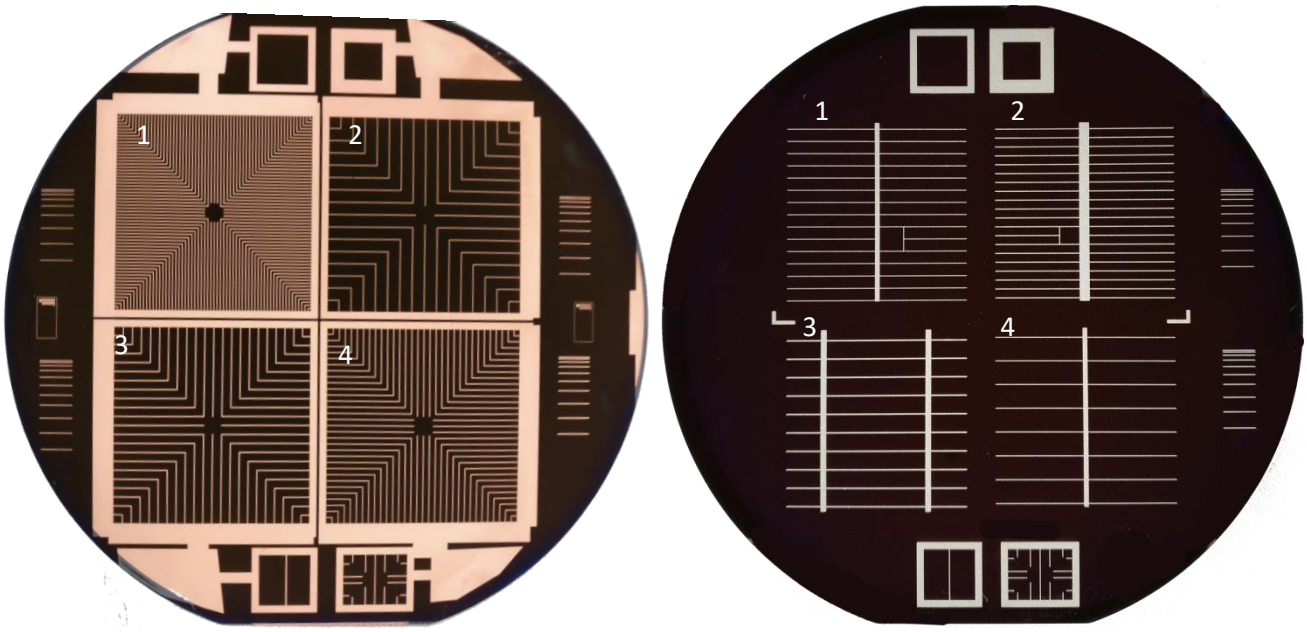


Figure 2.2 The result of two different mask designs. The left is referred to as the 3x3 cm²-large design, the right as the H-grid design.

The left design is called the 3x3 cm²-large mask, because the four big cells all have an area of 3x3 cm². One cell, which is cm². One cell, which is called a DIE, has fingers on the illuminated area to collect the carriers and a thick busbar outside thick busbar outside of the illuminated area to transport the current to the electrode. The shading percentage of the percentage of the fingers is different for every DIE and can be found in

Table 2.1. The right design is referred to as the H-grid design. In this design the busbar is on the illuminated area. One DIE has an area of 2.8x2.8 cm². The shading percentage of these DIEs can also be found in

Table 2.1.

Table 2.1 The shading percentages for different DIEs

	3x3 design	H-grid design
DIE 1	4.9%	5%
DIE 2	2.0%	12%
DIE 3	3.64%	11.5%
DIE 4	2.64%	3%

2.1.2 Metal evaporation

There are two ways to do a metal evaporation that are based on the same principle, thermal and e-beam evaporation. E-beam evaporation is a method in which a metallic source is heated above its melting point by striking it with an electron beam at very low pressure. The metallic source is loaded into a water cooled pocket. By heating it above its melting point, the metallic source becomes a vapor and will evaporate. The electrons of the beam is emitted by a filament and are directed into the pocket with metal by a strong magnetic field. The targeted wafer is placed in a rotation wafer-holder, which hangs above the pocket with the metallic source. The evaporated metallic particles will go up and will then condense on the wafer. The working principle is illustrated in Figure 2.3. E-beam evaporation is mainly used to deposit metals with high temperatures, like chromium (melting temperature 1860° C [24]), Titanium (1670° C [24]) and Nickel (1453° C [24]).

In the EKL there are two different e-beam evaporators; The Provac, which is used for Aluminum and Chromium and the CHA Opdamper, which is used to evaporate Nickel and Titanium. The difference between the two is the pressure it is pumped down to. The pump down pressure of the Provac is around $2.5 \cdot 10^{-5}$ mTorr, whereas the CHA goes down to $4 \cdot 10^{-7}$ mTorr.

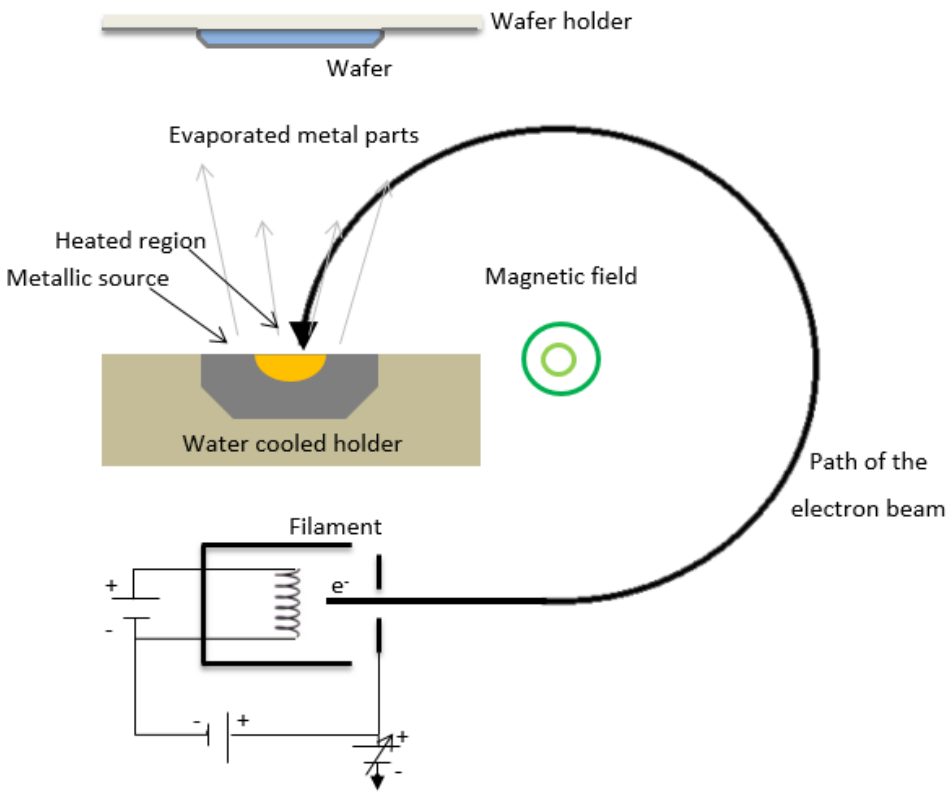


Figure 2.3. A schematic overview of e-beam evaporation of metal

Thermal, or resistive, evaporation is based on the same principle, only the metal is not heated by an electron beam, but by heating the pocket which holds the metal by running a high electrical power through it. This evaporation is also done under low pressures. The process is designed for metals with a relatively low melting point. Silver has a melting point of 961° C and is therefore suited for thermal evaporation. The melting point of Aluminum, 660° C, is also very suitable for thermal evaporation. However, Al forms an alloy with the tungsten boat and with that will eat the boat. As a consequence only silver is evaporated this way in Provac.

It is possible to put a wafer with developed photoresist in the evaporator. In this way, only on the open areas in the photoresist metal will grow on the wafer. The rest of the wafer is protected by the photoresist. After the evaporation, one should do a lift off of the photoresist with the metal on top. This lift off is done in a trilling bath of acetone until all photoresist (with metal on top) is dissolved. This process is illustrated in Figure 2.4.

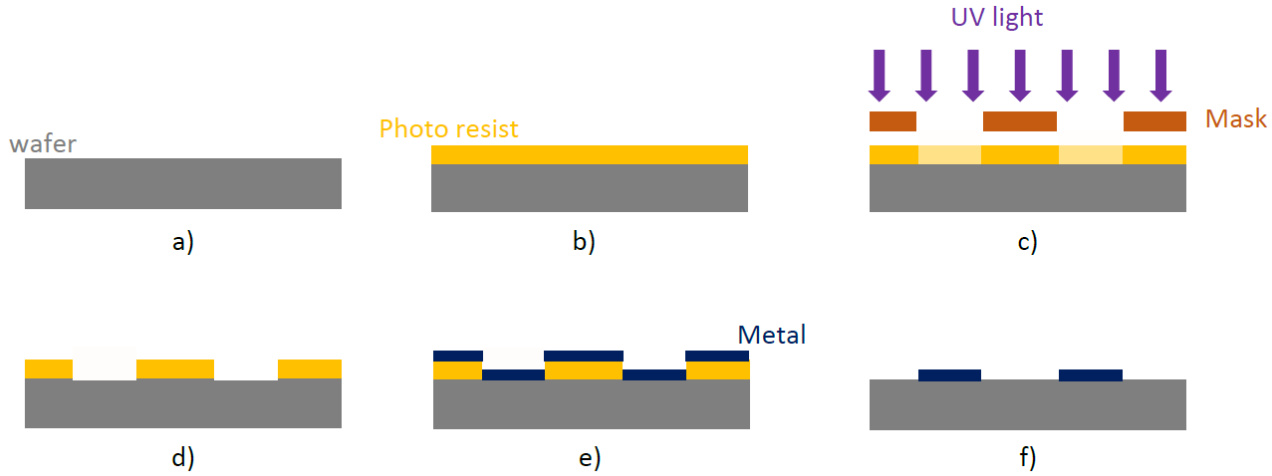


Figure 2.4 Flowchart of metal evaporation and lift off process. Step a; preparing the wafer. Step b; photo resist application. Step c; UV exposure through mask. Step d; Development. Step e; Thermal or e-beam evaporation of metal. Step f; Lift-off in acetone.

2.1.3 Cu electroplating

Cu electroplating is an electrochemical reaction with involves the transfer of electrons between two electrodes and the electrolyte-solution, which contains metal ions. When electrons are transferred, a 'redox'-reaction takes place; metal ions within the electrolyte can be oxidized (the loss of one or more electrons) or reduced (acceptance of one or more electrons), which can be expressed in the following equation

$$\mathrm{Ox}_{\mathrm{ion}}^{z+} + \mathrm{ze}^{-} \leftrightarrow \mathrm{Red}_{\mathrm{atom}} \qquad (2.1)$$

Where z is the number of electrons that are transferred during the reaction, Ox is the oxidized metal and Red is the reduced metal.

The electrochemical potential, E_{redox}, that fits this reaction is given by the Nernst equation:

$$E_{redox} = E_0 + \frac{RT}{zF}\ln\left(\frac{C_O}{C_R}\right) \qquad (2.2)$$

In which E_0 is the standard potential of the reaction, R the universal gas constant, T the temperature, z is the numbers of electrons transferred during the reaction, F the Faraday constant and C_O and C_R the concentrations of the oxidized and reduced ions. The potentials are always given versus a reference, which is most of the time is the "normal hydrogen electrode" (NHE). The standard potential of this electrode is 0 V and all other electrodes are tabulated against this reference. For copper plating, the standard potential vs the NHE is 0.35 V [15].

A electrochemical process can only run when there is a polarization at one electrode. However, to close the circuit, a oppositely polarized process is needed on the other electrode. The electrode at which the oxidation process takes place, in this case the wafer, is called the cathode. At other electrode, a plate of pure copper, a reduction reaction takes place. This electrode is called the anode. There are two different kind of electrochemical reactions. When a reaction runs spontaneously, the

system is called a galvanic cell. An example of a galvanic cell is a battery that is discharged; The system delivers a current and a potential between the cathode and the anode. A system that needs a voltage and a current from an external power source is called an electrolytic cell. This is also the case for the copper plating process.

The reactions that take place at the electrodes are the following ones:

Anode: $Cu(s) \rightarrow Cu^{2+}(aq) + 2e^{-}$ (2.3)

Cathode: $Cu^{2+}(aq) + 2e^{-} \rightarrow Cu\ (s)$ (2.4)

The electrolyte in which the wafers are plated is a solution of $Cu^{2+}(SO_4)^{2-}$.

The installation that is used for this thesis is the standard *homemade* copper plating set-up in the

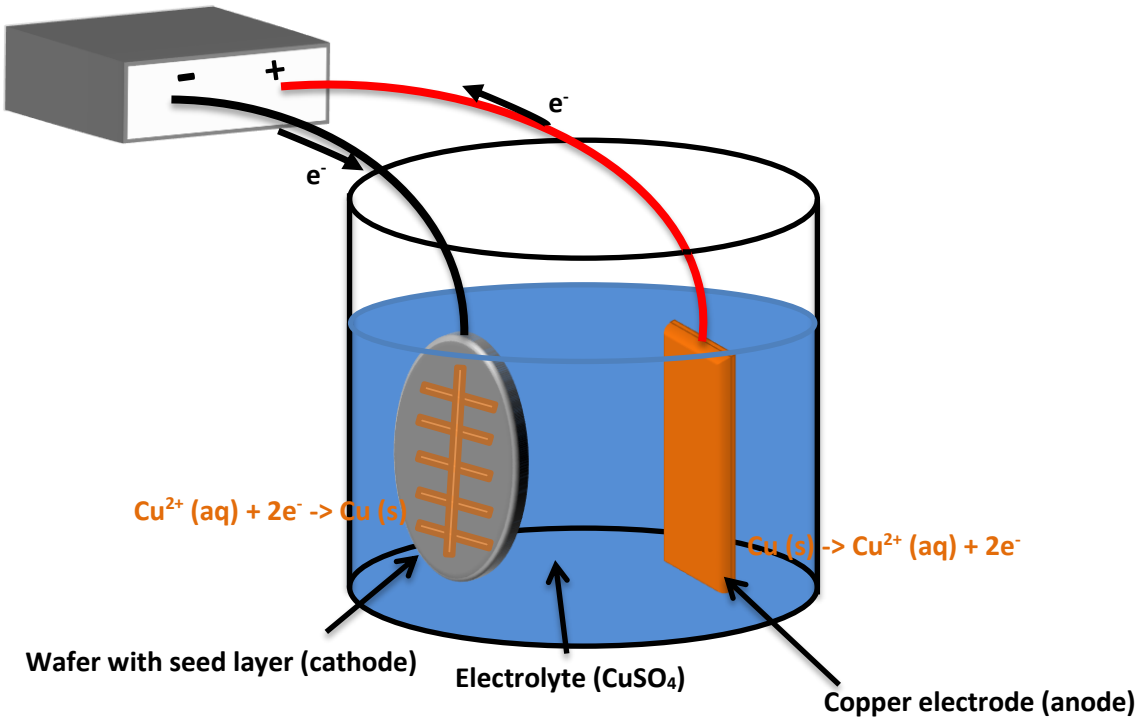


Figure 2.5. A schematic overview of the copper plating process.

MEMS-lab of the EKL. The wafer is loaded on a horizontally wafer holder and pinned down with four clamps on the edges of the wafer. These clamps are conductive and are connected to the bar of the holder. The wafer holder is then placed in the plating bath. The solution in the bath is pumped in circles through a filter and back in the bath. The solution is kept at a steady 28,0° C by an aquarium heater. A horizontally placed bar above the wafer is moving back and forth to steer the solution. The copper plate (Anode) is placed above the this bar and into the solution to close the system. There will not be any light on the wafer because of this construction. The bar of the wafer holder and the copper plate are then connected to the external power booster. Because the wafer holder is connected to the plus and the copper plate to the minus, a negative current should be given by the source to have the wanted reaction. The external power source is the Metrohm Autolab PGSTAT101

with a connected (10A) Booster, also from Metrohm. The source acts like a galvanostat, which means it can push a controlled and constant current through the system. The voltage can change during the reaction and is not controlled. Figure 2.5 shows a schematic overview of the copper plating process. Because of the high diffusion speed of copper into silicon, which causes deep level impurities, the process can be quite challenging [25]. These impurities will act as recombination-centers and will decrease the minority carrier lifetime resulting in a decrease of cell performance. This is the reason why copper should be plated on a barrier layer. In this cause, the silicon is protected against copper diffusion. This barrier layer will also act as a seed layer for the current that is used for the electroplating process.

2.1.4 Aluminum sputtering

Sputtering of Aluminum is a physical vapour deposition method, (PVD method). Sputtering can be done by direct current (DC) or radio frequency (RF) sputtering. In this research the substrate (the solar cell) is conductive and so DC sputtering will be used. The process starts with a pump down of the sputtering room to remove unwanted parts in the atmosphere. After a vacuum level is reached, the chamber is filled with a chosen gas, in this case argon. Then a negative potential is set over the cathode of the magnetron, which will case free electrons to accelerate away from the cathode. When such an electron collides with a argon atom, the argon atom is stripped from an electron (ionized), leaving a positively charged argon ion. This Argon ion is then attracted by the negative polarization of the cathode/target and will bombard the target. This bombardment will have enough energy to knock off atoms of the metal target. These metal ions will then *follow* the path of the magnetron to the anode and will sputter the substrate. By allocating magnets underneath the cathode, the process is even more efficient. A schematic overview of the process is shown in Figure 2.6.

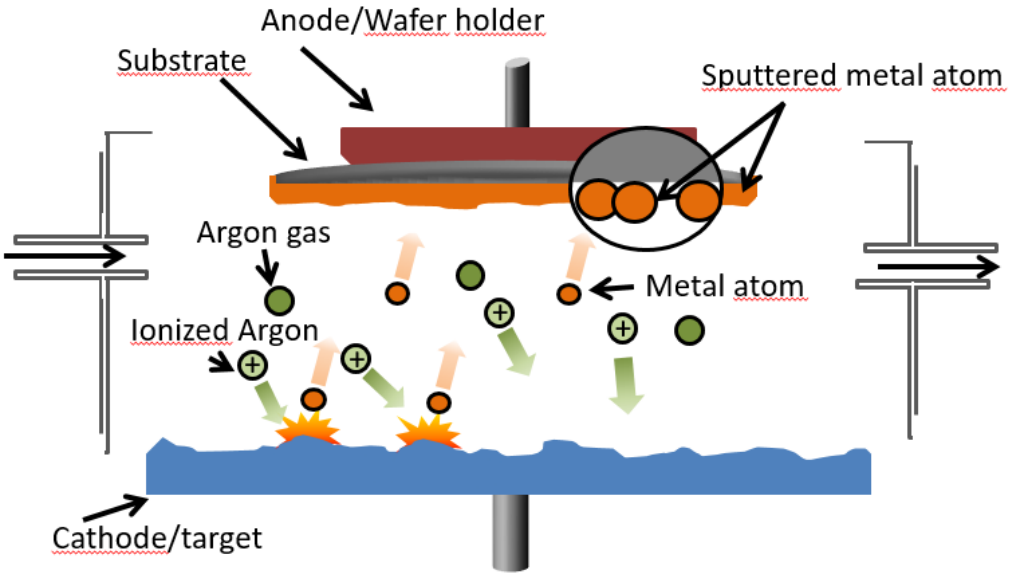


Figure 2.6. A schematic overview of metal sputtering

The machine that was used for aluminium sputtering was the Trikon Sigma sputter machine, located in the clean room of the EKL. Because photo resist is not suitable for this machine, only full area depositions can be done.

2.1.5 Screen printing (Ag-based paste)

Screen printing of Silver paste is the most commonly used metallization technique in the solar module industry. The process is well established, reliable, robust and fast. For this method a viscous paste of metal is used. Then the wafer is placed underneath a screen that consists of an interwoven thin-wire mesh, see Figure 2.8, with openings in the shape of the grid. Next, a squeegee presses the screen on the wafer and moves forward over the screen, so that the openings will be filled with the paste. The paste in these openings is put down on the wafer and after the squeegee got back and forth, the paste will be on the wafer in the shape of the chosen metal grid. This technique is illustrated in Figure 2.7. After the screen printing, the paste should be annealed to harden it and to improve the contact formation. It is also possible to etch the ARC while annealing when an etchant is included in the paste, these pastes are called firing-pastes. However, this is only necessary for non-conductive ARC-layers. The downside of these firing-pastes is that they have a difficult temperature-path to follow during the annealing and this equipment is not available within the EKL. Therefore, the paste that is been used was the low-temperature Ag based polymer paste Dupont PV416, which is especially for TCO layers. The annealing temperature and time for this paste is 170° C and 60 minutes, which is a safe temperature to avoid degradation of an a-Si layer [26].

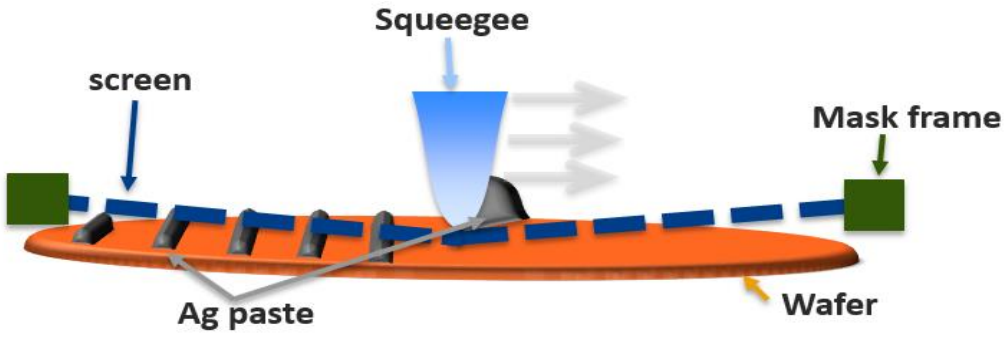


Figure 2.7. A schematic overview of the Screen printing process of silver paste

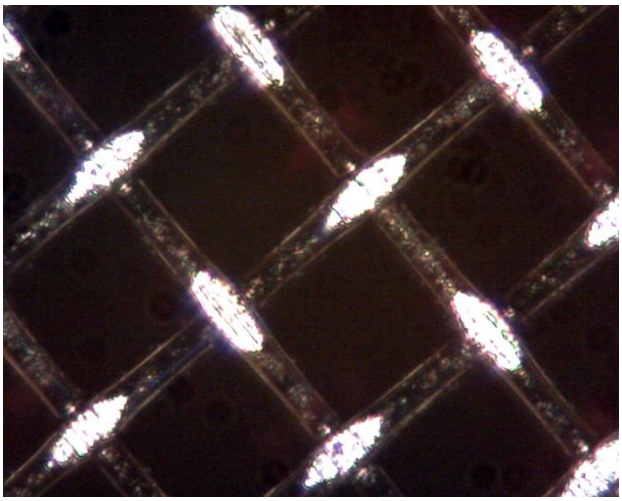


Figure 2.8. The interwoven thin-wire mesh of the screen.

2.1.6 Wet etching

For several deposition techniques only full area depositions are possible. In order to have a only a grid consisting of fingers and busbars, metal should be etched. The composition of the different etching baths that have been used for nickel and titanium are given in Table 2.2 and Table 2.3. The etching of aluminum was done in a commercially available etching bath of PES 77-19-04. The etching times for Ti and Ni is around 7 minutes for 300 nm. The etching time of aluminum is 100 nm per minute.

Table 2.2. The composition of the etching bath for titanium

	H_2O (ml)	25% NH_4OH (ml)	30% H_2O_2 (ml)
Ti/TiN etching	200	25	100

Table 2.3. The composition of the etching bath for nickel

	H_2O (ml)	HNO_3 (ml)	CH_3COOH (ml)	H_2SO_4 (ml)
Ni etching	200	50	50	20

2.2 Characterization techniques

In order keep improving solar cells, characterization of vital importance. By finding the limiting parameter of a cell, optimization can be made to improve this parameter, so that the solar cell efficiency will further improve. The characterization methods that are used in this thesis will be discussed in the coming sections.

2.2.1 1D-profiling

With 1D-profiling the height of a material can be measured. This is done with a profilometer, which measures the thickness across a horizontal length. The system uses a sensitive stylus (needle), under which the wafer is moved in a horizontal way. The stylus can move in a vertical direction and follows

the surface of the horizontal plane. The computer software records the vertical movement of the stylus (and horizontal movement of the wafer), which will result in a graph of height versus length. The stylus applies a very low force on the surface, so it will not damage the top layer. This technique is used to measure the height and width of the metal contacts. The profilometer in MEMS lab is the Dektak 150 from Veeco.

2.2.2 Illuminated J-V

In order to characterize the important external parameters, the illuminated J-V curve is measured with a solar simulator. This measurement is done under *Standard Test Conditions* (STC). This STC include a AM1.5 spectrum with 1000 W/m^2 of power and a temperature of 25° C. Usually a halogen lamp is combined with a xenon lamp to reproduces the AM1.5 spectrum. An overview is given in Figure 2.9**Fout! Verwijzingsbron niet gevonden.**.

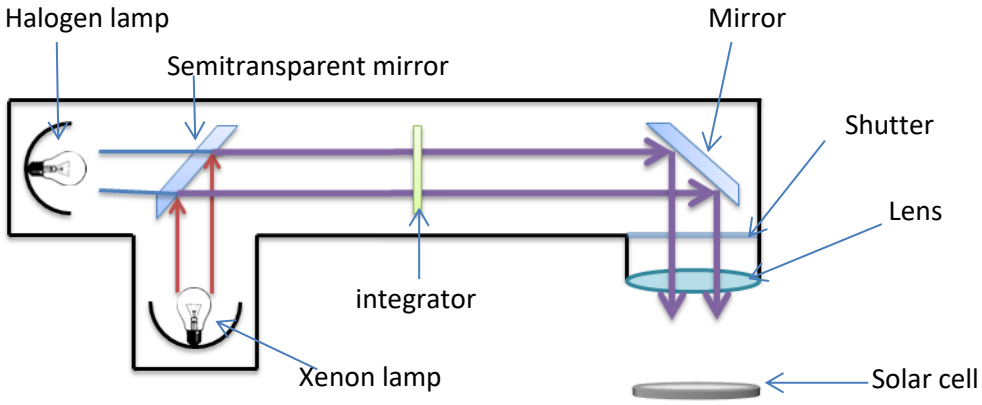


Figure 2.9. A schematic overview of a typical technique to make an illuminated J-V curve. Note: The colors of the light are for illustration purposes only, they do not represent the real spectrum of the lamps.

The J-V curve is made by connecting the illuminated solar cell to a load with various resistance. By varying this resistance (voltage applied to the load), the current is measured during the voltage sweep.

For this research an AAA class Wacom WXS-156S-L2 solar simulator is used.

2.2.3 External quantum efficiency measurement

The external quantum efficiency is measured by an in-house EQE setup of the PVMD group. A 300 W Xenon lamp is used to emit a broad wavelength spectrum. This light is passed through an optical chopper to modulate the intensity of the beam. This light is then sent through filters and into an Oriel monochromator to filter this beam. This results in a monochromatic light beam (a light beam with photons of one specific wavelength). This beam is then focused by lenses to a 3 mm^2 area which illuminates the solar cell. The generated current is measured and with that the amount of excited

electrons can be calculated. When compared to the amount of photons in the light beam, the EQE will be given. Before the in-house EQE can be used, first a calibration will be done on a reference Si photodiode. For the solar cells in this research, a range of wavelengths from 300 nm till 1200 nm is chosen. This is because the solar spectrum has hardly any photons with a smaller wavelength than 300 nm and photons with a bandgap higher than 1200 nm do not possess enough energy to create a successful electron-hole pair.

When the measured EQE (λ) is combined with the photon flux, ϕ_{ph}, at a certain wavelength (the amount of photons in the AM1.5 spectrum for a specific wavelength) the J_{sc} can be calculated as well following the equation

$$J_{sc} = q \int_{300}^{1200} EQE(\lambda) * \phi_{ph}(\lambda) \quad (2.5)$$

With

$$\phi_{ph}(\lambda) = P(\lambda) \frac{\lambda}{hc} \quad (2.6)$$

In which P(λ) is the spectral power density and h and c are constants (respectively Planck's constant and the speed of light).

Because of an internal bias voltage of the equipment of 0,23 V, a standard -0,23 V of bias voltage is set in the computer software, to nullify this internal bias voltage. The rear bias voltage is therefore zero. The step size of the wavelength is taken as 10 nm per measurement, which means that in total 91 measuring points are made. The J_{sc} calculated with the EQE equipment was calculated on a unshaded part of the solar cell, so has to be corrected with the shading percentage before it is accurate.

2.2.4 Suns-V_{oc} measurement

The Suns-V_{oc} is the value of the V_{oc} of a cell when series resistance effects are not included. This is done by using a separate reference cell to detect the intensity of the light. The illuminated J-V curve without series resistance is made by measuring the V_{oc} under different light intensities [27]. With this illuminated J-V curve the pseudo fill factor and the pseudo efficiency are also calculated. The measurement is done by using a flash lamp with a slow decay, so it will only take a second. The SunsV_{oc} measurements for this research were done with the Sinton Suns-V_{oc} instrument, see Figure 2.10, from the PVMD group.

Figure 2.10. The Sinton Suns-V_{oc} instrument

2.2.5 Transfer Length Method

The transfer length method (TLM) is a method to find the contact resistance between two layers. For the TLM a wafer needs a row of metal lines which are not connected, an example is shown in Figure 2.12. Two probes are then placed on two different lines with a distance x in between. A dark I-V curve is made, which will give the resistance. This resistance is a function of distance x. If this is done, for several distances x, a R-x graph can be made, as shown in Figure 2.11. A resistance versus distance graphs as a result of the TLM

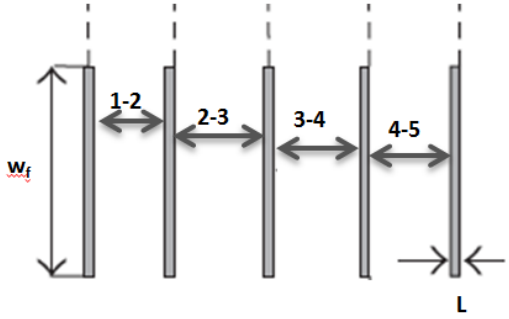


Figure 2.12. Metal lines that are used for the TLM. L is the length of the line and w_f the width.

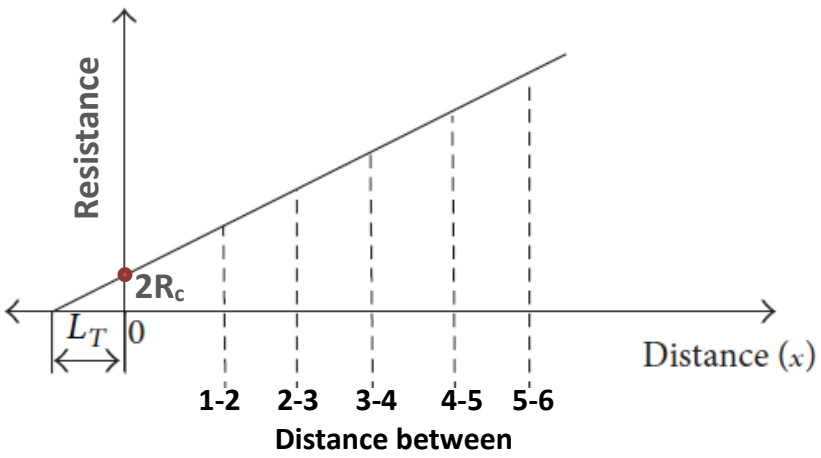


Figure 2.11. A resistance versus distance graphs as a result of the TLM

The equation of the trend that this line follows, is an indicator for the resistance build up. The slope of the trend line is a function of the distance and thus of the sheet resistance of the lower layer(s). At the junction with the y-axis, the distance is zero and so the sheet resistance is zero. The remaining resistance is therefore equal to twice the contact resistance (one for the first interface and one for the second). With this contact resistance, the contact resistivity can be calculated;

$$\rho_c = R_c * L * W_f \qquad (2.7)$$

Where L is the length of one line and W_f is the width of the line. If the L_T (the cross section with the x-axis) is smaller than L, the L_T is used instead of L. [13]

2.2.6 Scanning Electron Microscopy

With a scanning electron microscope (SEM) magnified images can be taken. A SEM has more or less the same principle as an optical microscope, with the mean difference that electrons are used instead of photons. With these electrons more magnification can be reached than with photons. The SEM consists of an electron filament (tungsten or LaB_6), a lens system, scanning coils, an electron collector and a cathode ray tube (CRT). The chamber of the SEM should be in vacuum conditions to prevent the collision of the electrons with particles from the air. An electron beam is emitted by the filament and with the lens system and scanning coils directed on the surface of the substrate. The backscattering of these electrons are detected and an image is made.

The SEM is used in this work to exam the surface topography. The SEM that was used was the SEM JEOL JSM-6360 in the MEMS laboratory of the EKL.

2.2.7 Spectrophotometry for optical measurement

With a spectrophotometer optical properties of materials can be measured, like the reflectance and transmittance. With tungsten-halogen and deuterium lamps a monochromatic light within the spectrum of photons of 175 nm till 3300 nm can be provided. The design of a spectrophotometer is shown in Figure 2.13. By placing the sample in the transmittance sample holder the transmittance can be measured and when the sample is placed in the reflectance sample holder, the reflectance can be measured through the integrated sphere. Because the reflectance, transmittance and absorption together is one, the absorption can be calculated when reflectance and transmittance are known.

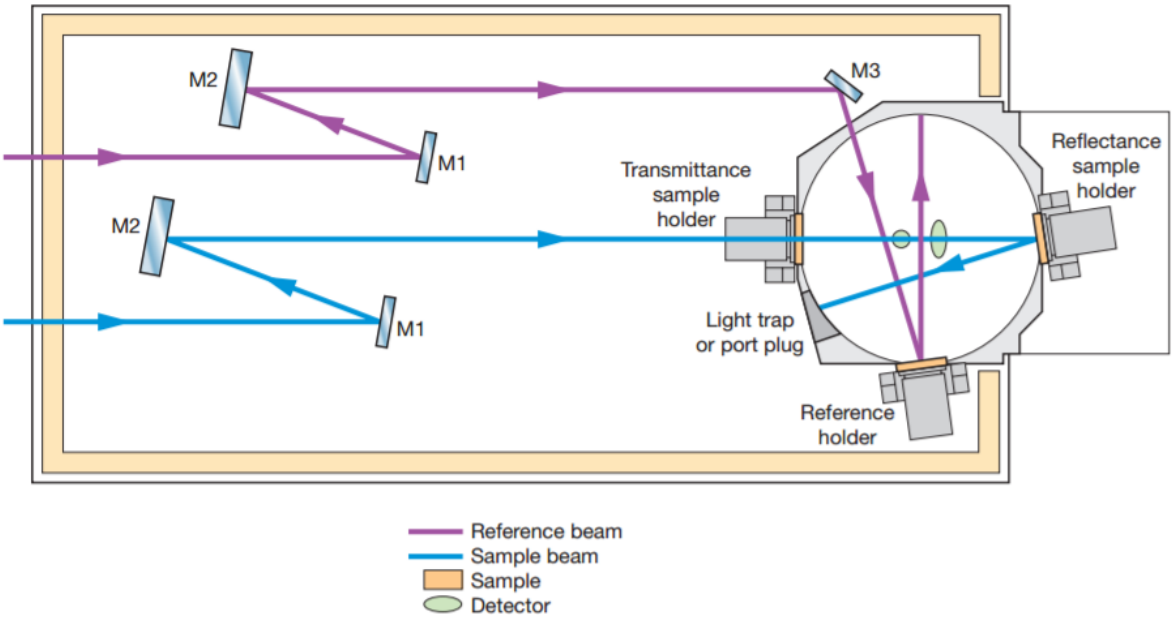


Figure 2.13. The optical design of a spectrophotometer [28]

The spectrophotometer that was used for measuring the back reflectance in this research was the PerkinElmer Lambda 950.

3 Metallization on poly/poly devices with a non-conductive ARC

3.1 Introduction

In this chapter, three metallization methods on a solar cell device with a non-conductive antireflection coating will be examined. These solar cells will have a 280 µm thick FZ n-type c-Si bulk, two passivating layers of SiO_2 on both front and rear, 20 nm n-type poly-Si at the front and 250 nm p-type Poly-Si at the rear. The non-conductive antireflection coating that is used is 75 nm of SiN_x. This structure is visualized in Figure 3.1. This type of solar cell will be referred to as a 'poly/poly device'.

The fabrication of the device starts with a flat n-type crystalline silicon wafer of 280 µm. On the rear a SiN_x layer will be deposited. Next, the wafer is textured in a texturing solution. Because the SiN_x layer protects the rear, only the front is being textured. After the texturing, the SiN_x is etched and the wafer is cleaned. Thin silicon oxide layer (approximately 1.5 nm-thick) was grown from a wet chemical solution of HNO_3, called NAOS (Native Acid Oxidation of Silicon) procedure. After the SiO_x

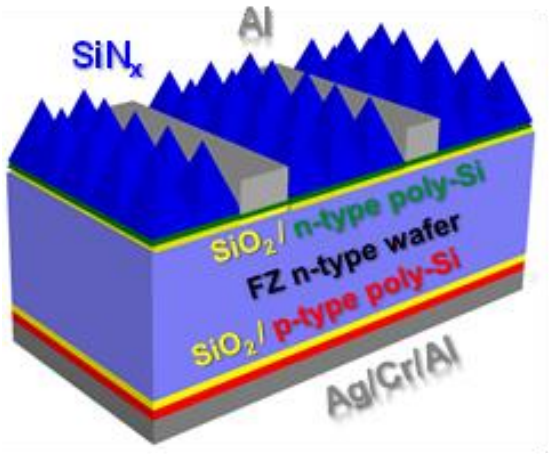


Figure 3.1. The structure of a SiN_x-poly/poly solar cell

deposition, a 250 nm thick poly-Si is deposited on both sides in an LPCVD furnace. After this deposition, the front has to be etched, because the layer is too thick and it will give too much parasitic absorption. This is done by protecting the rear with SiN_x. After poly-etching the front, the wafer is again cleaned and the SiO_x layer is again made with the NAOS procedure. Then the wafer is placed in the furnace for depositing a 20 nm thick poly-Si layer. At the rear, the SiN_x remains. After the deposition, now the 20 nm of poly-Si needs to be etched from the SiN_x at the rear. The front poly-Si is protected with a deposited layer of SiN_x. After etching the poly-Si on the rear, the wafer now has two layers of poly-Si; on the front 20 nm, on the rear 250 nm. Both layers are protected by a SiN_x layer. Before implantation of the layers, the SiN_x is removed by dry and wet etching. The

implantation dose of the rear (Boron) is $5 \cdot 10^{15}$ ions/cm^2 with an energy of 5 keV. After the implantation, the wafer is cleaned and annealed at 950° C for 5 minutes. After annealing, the front is implanted with Phosphorous with an energy of 10 keV and a dose of 10^{16} ions/cm^2. The wafer is again annealed at 850° C for 90 minutes. The device is finished by depositing 75 nm-thick layer of SiN_x as anti-reflection coating. The last step is the lithography and etching of ARC to define the front metal grid. This will be the starting point of the metallization process. The next steps for the front metallization will be explained for each metallization technique individually in the coming sections. The rear metallization will be the same for all the cells; First a layer of 200 nm of thermally evaporated Ag, then 30 nm of e-beam evaporated chromium and as a bulk layer 2000 nm of e-beam evaporated aluminum. To reduce shunt paths, backside metal stack is evaporated via hard mask and therefore localized in the active areas.

3.2 Aluminum e-beam evaporation

Aluminum e-beam evaporation is a standard process within the PVMD group. It is mainly used for metallization of c-Si wafer-based solar cell. This is because it is a rather easy process. The wafer with the opened photo resist is placed in the evaporator, the chamber is pumped down to pressure of $2.5 \cdot 10^{-5}$ mTorr and the metal is being deposited automatically at a speed of 1 nm/s. The total height of the deposited aluminum is 2 µm. After the deposition and venting of the chamber, the wafer is put in an ultra-sonic acetone bath. After a few minutes, depending on the thickness of the metal and photo resist, the wafer is stripped from the photo resist and thus also the metal that was on top of the photo resist. After rinsing and cleaning with isopropanol (IPA) the front metallization is finished. Aluminum is used because it is a relatively cheap metal, has an acceptable conductivity, a low work function and a good adhesion on silicon. Especially the last two reasons makes aluminum a far more suitable metal for front contact on a n-type silicon cell; the work function of Ag (4.26-4.73 eV [29]) is higher than the work function of Al (4.08 eV [30]), which would lead to an increase in built in voltage and the adhesion of silver on silicon is not good enough to survive the lift-off procedure.

3.2.1 Results and discussion

The width, height and aspect ratio of the Al e-beam evaporated fingers are quite steady, whereas the finger opening in the photo resist is exactly the width of the remaining finger after liftoff. The physical parameters of the fingers of the different DIEs are shown in Table 3.1. The external parameters following from the J-V measurement are given in Table 3.2. The best solar cell was DIE 1, with an efficiency of 19.3% considering aperture-area efficiency. The other DIEs performed worse and together with DIE 1 have an average of 16.75%.

Table 3.1. The width, height and aspect ratio of the fingers of the different DIEs. All DIEs have one busbar, expect DIE 3, which has two.

	Width of finger (µm)	Height of finger (µm)	Aspect ratio of finger
DIE 1	95	2.0	0.021
DIE 2	120	2.0	0.016
DIE 3	170	2.0	0.012
DIE 4	100	2.0	0.020

Table 3.2. The external parameters of the aluminum evaporated solar cell with H-grid mask.

	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	R_{sh} (kΩ·cm^2)	R_s (Ω·cm^2)	η (%)
Average (4 cells)	670.5	34.32	73.8	2.62	1.93	16.97
Best	689	38.3	73.0	1.98	1.81	19.3

3.3 Cu-electroplating

Before Cu can be plated on the wafer, a barrier layer must be deposited to protect the (poly-) silicon from the diffusion of copper. Indeed, Cu is a heavy metal atom that easily diffuses in Si bulk and acts as a recombination center. This barrier layer has a double function, i) protecting Si form contamination and ii) a seed layer for the electro plating. The seed layer that is used is e-beam evaporated titanium. This layer is deposited at a speed of 1 Å/s and a pressure of $4 \cdot 10^{-7}$ mTorr. Then, metal and photoresist are lifted-off in the ultra-sonic acetone bath. At this point, the top layer of the device consists of two materials; the SiN_x and Ti. The cell is then attached on the wafer holder with the four clamp. The clamps should be in contact with the Ti, which explains the metal areas on the outside of the cell. These clamps conduct the current from the connection bar of the holder to the seed layer. When the wafer holder is placed in the bath, the stirrer is running and both the connection bar from the wafer holder (positive pole) and the copper plate (negative pole) are connected to the external power source, the electro plating is started. The current and plating time that were used are different for the DC and pulse plating and will therefore discussed below.

3.3.1 DC copper plating on n-type SiO_2/poly-Si layer

DC copper plating is plating with only one constant current and plating time. First this technique was tested on a textured, 500 nm thick n-type test wafer. The test wafer only had 300 nm of Ti in the form of the grid and had no top layer. This way the right current and corresponding plating time was

found. In the search for the optimum plating conditions, three parameters were studied; The adhesion of the copper and/or titanium with office tape, the height of the fingers and the equality of the height in one DIE.

3.3.1.1 Results and discussion

A lot of different combinations of current and plating time were tested. Following the work of Papakonstantinou [31], who started with a current of 0.37 A for 900 seconds, which lead to a detaching of the fingers. Papakonstantinou used a seed layer stack of 10 nm Ti, 40 nm TiN and 300 nm sputtered Cu on TCO, which detached after plating 900 seconds. The 300 nm Ti seed layer on c-Si showed a stronger adhesion. Fingers with thicknesses up to 120 µm on the fingers width the most width where produced without detaching, although homogeneity and good adhesion on the other DIEs at the same run were not reached.

When low current (0.1-0.3 A) was used, it showed inhomogeneous growth, whereas the area close to the contact clamps was higher than the grid further from the clamp. Higher current (0.5 A) gave a more homogenous results, but was slow and had a maximum height of around 20 µm on DIE 1. Further increasing the current (0.7 A) gives a more homogenous height result per DIE, but still takes a rather long time. When this current is doubled, the plating time can be halved, while having the same result. This results in a plating time of 1500 seconds at a current of 1.4 A. A microscopic picture is shown in Figure 3.2 a). When the current is again doubled to 2.8 A with a plating time of 750 s, the average height is higher than with the previous recipe, with the exception of one DIE. Figure 3.2 b) shows a picture of the plated Cu under these conditions. It shows a more rough and less dense finger. A current of 5.6 A gives only a lot of plating on the clamps itself and cannot be used for Cu plating on the wafer. For the following experiments, the 1.4 A and 1500 seconds are chosen as the plating recipe.

Figure 3.2. (a) Copper plated at a current of 1.4 A (b) Copper plated at a current of 2.8 A

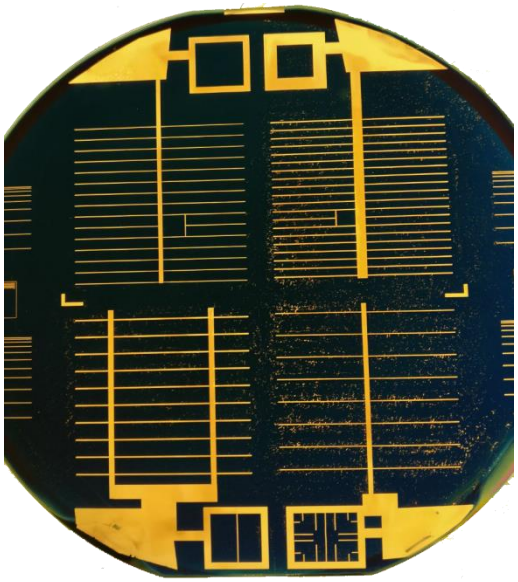


Figure 3.3. A DC plated solar cell with H-grid mask. It shows a lot of 'dirty' growth.

The first test on a real solar cell device, the poly/poly, shows a lot of unwanted growth of Cu points, as is shown in Figure 3.3. These unwanted particles are plated through gaps in the SiN_x, but are not present when plated on a test wafer, without SiN_x. These unwanted particles are most likely caused by the n-type poly (the FSF) of the solar cell, which is conductive enough to lead electrons to the gaps in the SiN_x and can also grow Cu particles. Previous research [32] shows that this problem does not occur on a p-type c-Si emitter. This unwanted growth of Cu leads to an increase in shading and thus a decrease in sheet resistance. Nevertheless, the solar cell does work. The 1D-profiling of one finger of each DIE is shown in Figure 3.4. The width, height and corresponding aspect ratio are given in Table 3.3. The width of the fingers that is given is the measure width, not the width of the lithography mask. The widths of the fingers of the lithography mask are the same as the widths given in Table 3.1.

Table 3.3. The average width, height and aspect ratio of the fingers of the DC plated H-grid mask

	Width of finger (µm)	Height of finger (µm)	Aspect ratio of finger
DIE 1	119	10.7	0.09
DIE 2	237	41.0	0.17
DIE 3	239	31.0	0.13
DIE 4	181	51.0	0.28

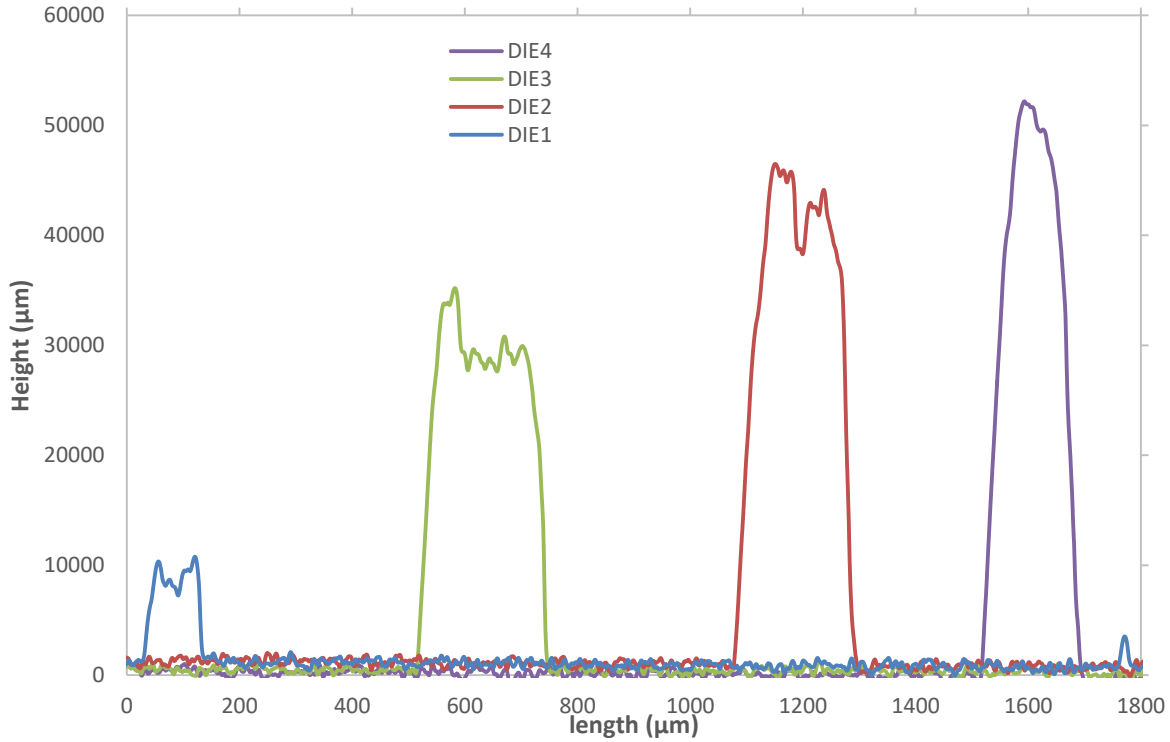


Figure 3.4. A graph of a 1D-profil of a finger from the different DIEs on a DC plated solar cell with H-grid mask

The parameters of the J-V measurements are shown in Table 3.4. The best DIE, DIE 1, has an efficiency of 19.6%, whereas the average of all the cell is 18.0%. This is mainly because the V_{oc} of both right DIEs, DIE 2 and 4, are rather low (668 and 662 mV, respectively). The FF of DIE 4 however is very high; 78.0 % (compared to the pFF of 82.8%).

Table 3.4. the external parameters of the DC plated solar cell with H-grid mask.

	V_{oc} (mV)	Suns-V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	pFF (%)	R_{sh} (kΩ·cm^2)	R_s (Ω·cm^2)	Efficiency (%)
Average (4 cells)	674.5	695.2	35.60	76.2	83.45	10.3	1.15	18.2
Best	682	697	38.1	75.2	83.3	3.12	1.20	19.6

The plating on the 3x3 cm^2-large mask gave even more unwanted growth of Cu particles, as is shown in Figure 3.5. Experiments with a lower current did not solve this issue. The physical results of the 1D-profiling of the solar cell with the 3x3 mask are shown in Table 3.5. The external parameters of the poly/poly solar cell with this grid are given in Table 3.6. DIEs 2, 3 and 4 show significantly lower values for the parameters than the H-grid, whereas DIE1 did not work at all. This is probably caused

by the amount of unwanted Cu particles in the cell. The best DIE was DIE 2. The lower parameters were not caused by the precursor cell, which is proven in the next section.

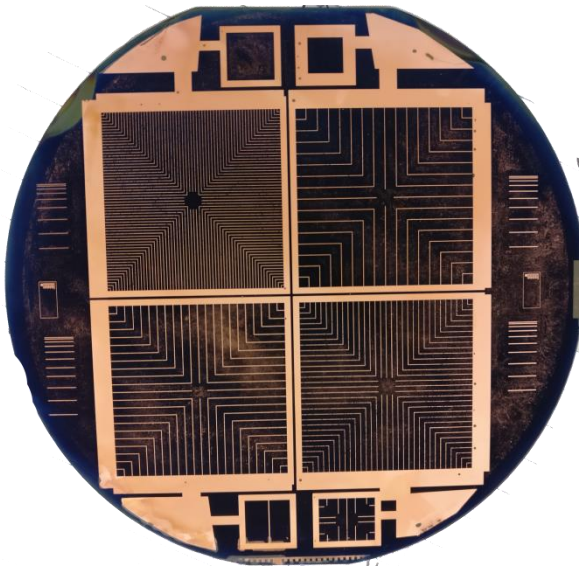


Figure 3.5. A DC plated 3x3 mask solar cell with unwanted Cu growth between the fingers.

Table 3.5. The width, height and aspect ratio of the fingers of the DC plated 3x3 mask.

	Width of finger (µm)	Height of finger (µm)	Aspect ratio of finger
DIE 1	245	29.3	0.122
DIE 2	180	26.0	0.144
DIE 3	236	46.3	0.196
DIE 4	263	34.0	0.129

Table 3.6. The external parameters of the DC plated solar cell with 3x3 mask.

	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	R_{sh} (kΩ·cm^2)	R_s (Ω·cm^2)	Efficiency (%)
Average (3 cells)	648.6	32.97	71.1	42.0	1.85	15.19
Best	649	32.30	75.85	4.53	1.55	15.89

3.3.2 Pulse copper plating on n-type SiO_2/poly-Si layer

In order to remove the unwanted growth of Cu spots on the device, pulse plating is introduced. With this method the polarity is switched for a short period, so the cathode becomes the anode and vice versa. During this reserve plating, Cu will grow on the Cu plate and Cu will be dissolved from the

wafer. Because the spots are only a thin layer of Cu, the spots will be dissolved completely, before the Cu of the fingers is gone. Again, the forward plating is started. These steps are continued for several cycles. The process is illustrated in Figure 3.6. Because unwanted growth only occurs on real devices, pulse plating was tested on a poly/poly device. The same wafer of the DC plated 3x3 cm^2-large device was used. Cu of the previous solar cell was etched in a solution of 69,5% HNO_3:H2O 1:1. The Ti seed layer, SiN_x and poly-Si on the rear were not etched or damaged during this etching. This made it possible to recycle the cell.

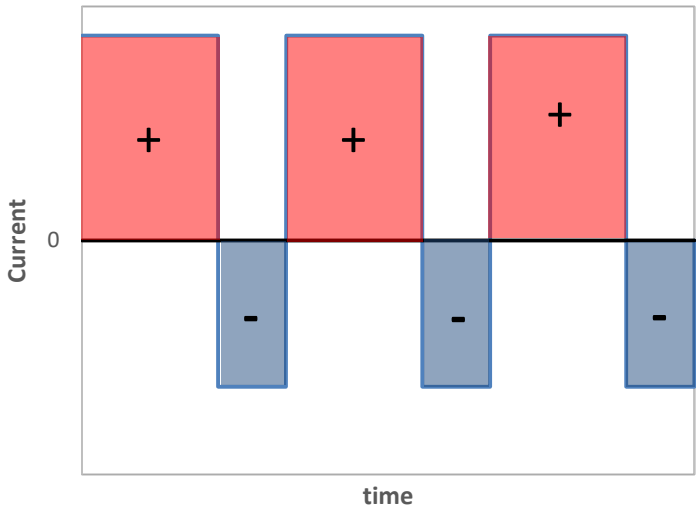


Figure 3.6. Illustration of the pulse plating technique

3.3.2.1 Results and discussion

Pulse plating is proved to be more difficult than DC plating, because the adhesion is less good. When pulse plating is done with high currents, the fingers already detach after reaching 10 micron. When the current of both forward as reversed plating are lowered, the adhesion of the copper is good and the unwanted Cu growth is not present anymore. A suitable plating recipe for the 3x3 cm^2-mask is illustrated in Figure 3.7.

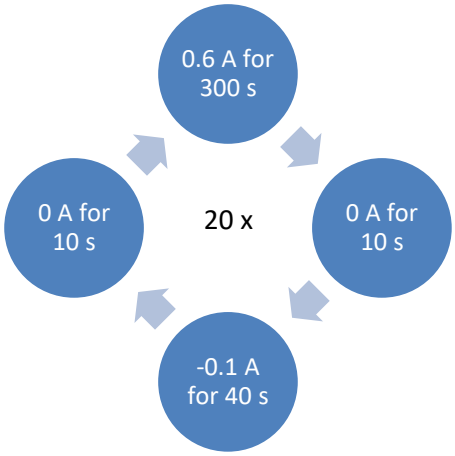


Figure 3.7. The pulse plating cycle for a poly/poly cell with 3x3 mask

The physical results of the pulse plating on the poly/poly with 3x3 mask are shown in Figure 3.8 and Table 3.7. Beside the fingers of DIE 2, the aspect ratios are comparable with the aspect ratios of the DC plating 3x3 cm^2-large fingers. The holding clamp of the wafer of DIE1 was probably not connected properly, which leaded to a relatively poor plating of Cu.

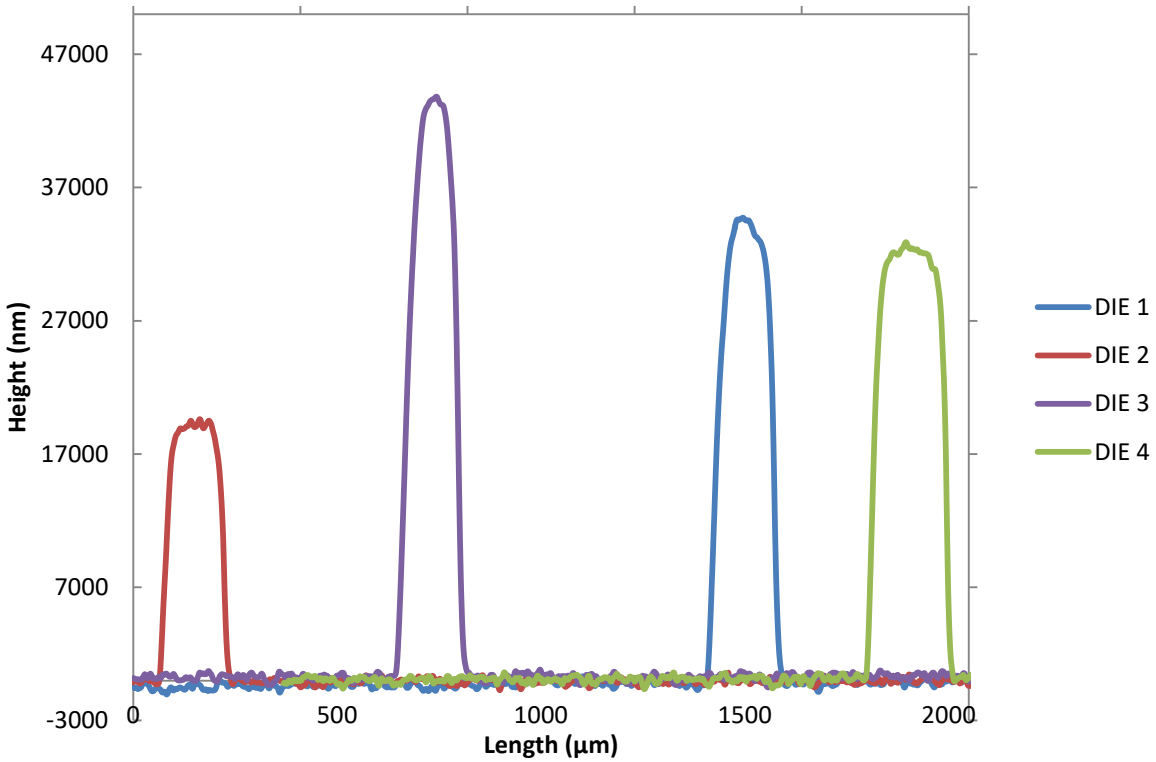


Figure 3.8. The 1D profiling of the fingers for different DIEs of the 3x3 cm^2-large mask after pulse plating

Table 3.7. The average width, height and aspect ratio of the fingers of the different DIEs of the 3x3 cm^2-large mask.

	Width of finger (µm)	Height of finger (µm)	Aspect ratio of finger
DIE 1	233	34.6	0.148
DIE 2	195	19.0	0.097
DIE 3	234	44.1	0.188
DIE 4	260	32.7	0.126

The results of the J-V measurements are shown in Table 3.8. It shows higher V_{OC} and J_{SC} than the DC plated 3x3 cm^2-large device. Because the same wafer was used, this means that the low V_{OC} and J_{SC} from the DC plated device were caused by the unwanted growth of Cu. Pulse plating shows an increase in efficiency when compared to DC plated devices. Although the plating on DIE 2 was not done perfectly, the FF was still high (75.7%). The efficiency of DIE 2 (16.6%) on the other hand was

significantly less than the efficiencies of the other DIEs (18.5% on average). This is mainly because the J_{SC} is lower. This indicates that there is an error in the working layers of the cell, because DIE 2 has the lowest shading factor and should therefore have the highest short circuit density.

Table 3.8. The external parameters of the pulse plated solar cell with 3x3 mask

	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	R_{sh} (kΩ·cm^2)	R_s (Ω·cm^2)	Efficiency (%)
Average (4 cells)	686	35.05	75.3	3.10	1.23	18.1
Best	688	36.15	75.0	3.85	1.26	18.7

3.4 Aluminum sputtering

Aluminum sputtering has the possibility to be a substitute for the evaporation with an e-beam, whereas there is the possibility that e-beam damages the semiconductor material of the solar cell [33]. The practical limit of the height of the metal, circa 20 µm, is also higher than the limit of the evaporator, circa 6 micron. The downside of this method is that during sputtering there is also an electron beam involved. This beam has a different power and goal than the e-beam of the evaporator, but still could damage the solar cell layers. Another downside is that photo resist releases too many gasses and is therefore not allowed in the sputtering chambers. Therefore, a more difficult and extensive fabrication is done. The precursor with the openings in the ARC and photo resist on top is the starting point. Firstly, the photo resist is dissolved from the device with acetone. Then, the wafer is placed in the sputtering chamber and the aluminum is sputtered in two steps. The first step is with a low deposition rate. This is so the deposited metal atoms do not destroy the surface of the solar cell. After a first protection layer is deposited, the deposition rate is raised. After the full area deposition a lithography takes place with negative photo resist. When the same mask is used, this means that after development only photo resist remains on the illuminated area. It is important that the remaining negative photo resist layer is well aligned with the grid that was etched away in the SiN_x layer. This is accomplished via alignment markers. The alignment markers are only visible when they are flat. This can be done by having some SiN_x on the alignment markers during texturing. However, because this technique is only being compared to the e-beam evaporation of Aluminum, the front of the cells is flat. The height of the deposited aluminum is 1.6 µm and the rear is thermal evaporated silver of 200 nm, 30 nm of e-beam evaporated chromium and 1.4 µm of e-beam evaporated aluminum. The reference solar cell is the same cell, with only 1.6 µm of e-beam evaporated aluminum at the front instead of sputtered aluminum.

3.4.1 Results and discussion

Because both devices have a chosen thickness and widths of the fingers (both directly dependent of the lithography), the aspect ratio is the same as well. The aspect ratios of both devices are shown in Table 3.9. The aspect ratios for both devices can be higher, whereas the chosen height is for both methods not the practical limit, but is chosen for comparison purposes. The external parameters of the e-beam Al evaporated and sputtered poly/poly devices are shown in Table 3.10 and Table 3.11, respectively.

Table 3.9. The width, height and aspect ratio of the fingers of both the sputtered and the e-beam evaporated device.

	Width of finger (µm)	Height of finger (µm)	Aspect ratio of finger
DIE 1	95	1.6	0.017
DIE 2	120	1.6	0.013
DIE 3	170	1.6	0.009
DIE 4	100	1.6	0.016

Table 3.10. The external parameters of the e-beam Al evaporated planar poly/poly device.

	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	R_{sh} (kΩ·cm^2)	R_s (Ω·cm^2)	Efficiency (%)
Average (4 cells)	699.5	28.31	68.8	37.59	3.16	13.55
Best	705	28.99	70.8	78.4	2.34	14.46

Table 3.11. The external parameters of the Al sputtered planar poly/poly device.

	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	R_{sh} (kΩ·cm^2)	R_s (Ω·cm^2)	Efficiency (%)
Average (4 cells)	694.25	28.84	69.6	8.30	2.85	13.92
Best	687	28.22	72.1	11.83	2.19	13.98

The devices show some small differences. The e-beam evaporated device has a slightly higher V_{OC} than the sputtered device, whereas the sputtered device shows a higher FF, due to a lower series resistance. However, the differences are too small to really draw conclusions, besides the fact that sputtered Al does not inflict more damage to the cell than the e-beam evaporated device. Because

the rear of both devices is done by e-beam evaporation, no conclusions can be drawn about the potential damage that is done by the e-beam.

3.5 Conclusions

The results show that Cu-electroplating can increase the fill factor of a solar cell. This is done by decreasing the series resistance. The average fill factor increases from 73.8% to 76.2% for DC plating and 75.3% for pulse plating, as shown in Figure 3.9. The higher fill factor of the DC plated is probably caused by the high shunt resistance of the DC plated device (10.3 kΩ·cm^2 versus 3.10 kΩ·cm^2 of the pulse plated device), because the difference series resistance is very small. However, because of the unwanted Cu growth between the fingers, the V_{oc} of the DC plated device is relatively low and therefore has a lower overall efficiency of the DIEs. The best poly/poly cell is DIE 1 of the DC-plated device with 2.8x2.8 cm^2-large H-grid mask. This cell has an efficiency of 19.6%, which is a record for poly/poly devices within the PVMD group.

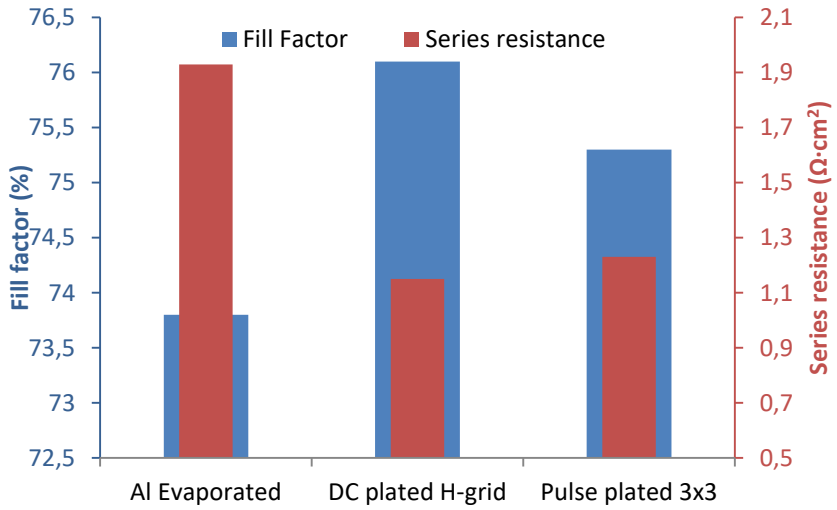


Figure 3.9. The Fill factor and series resistance of the Al evaporated, DC plated H-grid and Pulse plated 3x3 solar cell.

The comparison between the device with e-beam evaporated Al and sputtered Al as a front contact metal shows a slightly higher V_{OC} for e-beam evaporated Al and a slightly higher fill factor for the sputtered Al. Because the rear was evaporated for both sides, no conclusions can be drawn about the potential damage that is inflicted by the e-beam. The results only show that it is safe to sputter Al instead of evaporating it. This method has the advantage that the maximum wanted thickness is larger than the e-beam evaporated (practical) limit.

4 Metallization on devices with a conducting layer

4.1 Introduction

In this chapter, three metallization techniques will be used to metallize the front grid of a solar cell device with a transparent conductive oxide (TCO) layer. This TCO layer acts like an anti-reflection coating, but is also conductive (R_{SH} < 100 Ω/□) and thus can collect and transport carriers. A transparent conductive oxide layer is used on amorphous silicon layer (a-Si) in silicon heterojunction (SHJ) solar cells. This is because the conductivity of the doped a-Si layer is rather poor.

This TCO layer will, at least in theory, increase the lateral conductivity at the top of the cell. A decrease in lateral resistance is expected and thus a decrease of the series resistance as well. A good TCO layer is characterized by a low parasitic absorption and a high conductivity. The resistivity (ρ) of a TCO layer is calculated with

$$\rho = \frac{1}{\sigma} = \frac{1}{qN\mu} \quad (4.1)$$

in which N is the carrier density and μ is the mobility of the carriers. As the equation shows, the resistivity of the TCO layer decreases with an increase in carrier density and mobility of carriers. A high carrier density will therefore result in a low resistivity of the layer and should therefore increase the performance of the TCO layer. However, the carrier density also increases the plasma frequency, which is the natural frequency of oscillation of the electron gas. This will result in more reflectance, because a larger amount of photons has a frequency that is smaller than the plasma frequency. Therefore, TCO layers commonly have a low or moderate carrier density and is the mobility as high as possible.

For this experiment two different types of solar cell devices with a TCO layer were metallized. The first one is called a *Hybrid cell*. This cell has a rear fabricated at high temperature (> 900° C) and the front is processed at moderate/low temperatures (<200 °C). The cell is a combination of the TOPCon cell of Fraunhofer ISE (efficiency 25.3% [34]) and SHJ solar cells with efficiencies over 25% [35].

This cell has a FZ n-type c-Si bulk layer. The rear has a tunneling oxide SiO_x layer and a p-type poly-Si rear emitter. The textured front has an intrinsic a-Si layer and a n-type a-Si:H layer as a front surface field and a stack of IOH/ITO as a TCO layer. The solar cell overview is given in Figure 4.1.

The fabrication of this cell starts with a n-type FZ wafer of 280 µm and <100> orientation. After a Maragoni dip to remove native oxides, SiO_x is grown with the NAOS procedure. Then, a 250 nm-thick LPCVD poly-silicon layer is deposited in a furnace at 950° C. After this deposition the rear poly-Si layer

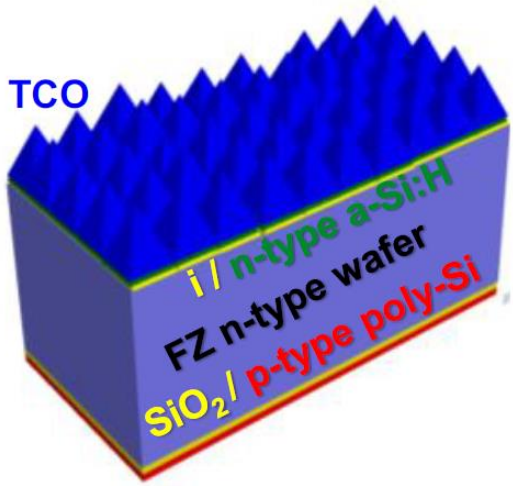


Figure 4.2. The schematic overview of the precursor of a hybrid solar cell

is implanted with Boron with a dose of $5 \cdot 10^{15}$ cm^{-2} and an energy of 5 keV. After implantation a SiN_x is deposited on the rear of the wafer to protect it during texturing of the front. The texturing will also etch the poly-Si and SiO_2 layers on the front. After texturing the SiN_x is etched from the rear in BHF (1:7) and after this the wafer is cleaned using the Nitric Acid Oxidation Cycle (NAOC) cleaning. Now the wafer is ready for the deposition of the intrinsic and n-type a-Si:H layers using radio frequency plasma enhanced chemical vapor deposition (RF-PECVD). It is important that the wafer is transferred into the vacuum chamber of Amor (the RF-PECVD of the PVMD group) to prevent surface oxidation. The wafer is first preheated for 30 minutes and then a layer of 4.5 nm of intrinsic a-Si:H and a layer of 6 nm of n-type a-Si:H are deposited. After this deposition the TCO layer is sputtered with a Radio Frequency magnetron sputtering machine, named *Zorro*. The TCO consists of two layers; 65 nm Indium Oxide Hydrogenated (IO:H) and 10 nm of Indium Tin Oxide (ITO). This will be the starting point for the metallization process, whereas the following step depends on the chosen metallization technique. The ITO top layer has an work function in the range between 4.6 and 5.2 eV [36].

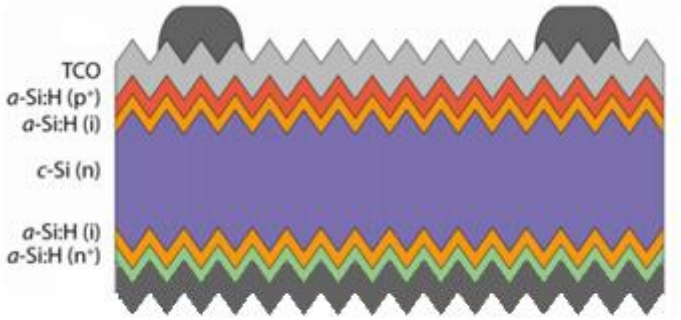


Figure 4.1. The structure of a SHJ solar cell.

The rear metallization is done after the front metallization, due to the poor of adhesion of the silver metal and is the same for all devices; 200 nm silver, 30 nm chromium and 2000 nm aluminum.

The other solar cell type that is used is the silicon hetero junction (SHJ) solar cell. This cell has an a-Si stack on both the rear and the front and, in opposition to the hybrid, has a front emitter and a back surface field, which means that the front is p-type. The FZ n-type wafer has an i/n a-Si:H stack at the rear and a i/p a-Si stack at the front, as shown in Figure 4.2. On the i/p stack there is a TCO top layer as an ARC and conductive layer.

The cell fabrication begins with the texturing of a flat n-type FZ wafer. After the texturing, the NAOC cleaning is done. After the NAOC cleaning the wafer is placed in the same RF-PECVD reactor as is used for the hybrid cell. In this reactor, first the intrinsic a-Si:H layers are deposited on the front and rear of the c-Si absorber layer in order provide chemical passivation of the c-Si. Next, the n-type doped a-Si:H layer is deposited in one chamber. The p-type doped a-Si:H is deposited after that in another chamber, in order to avoid contamination. After the p-layer deposition the wafer is transferred to the *Zorro* to sputter the TCO layer. The TCO layer is exactly the same as for the hybrid cell; 65 nm of IO:H and 10 nm of ITO. After this step, the metallization starts.

The rear is done by thermal evaporation of 200 nm of Silver and e-beam evaporation of 30 nm chromium and 2000 nm aluminum.

4.2 Aluminum e-beam evaporation

Aluminum e-beam evaporation on TCO layers is the standard metallization method within the PVMD group. After the TCO layer is deposited, the photo resist layer with the grid openings is deposited on the front with the lithography step. Then, the wafer is placed in the evaporator under the same conditions as the e-beam evaporation on the poly-poly device from chapter 3. A pressure of $2.5 \cdot 10^{-5}$ mTorr and growing speed of 1 nm/s. After the evaporation, the unwanted metal is removed with the lift-off procedure, which is describe in chapter 3. The aluminum is directly deposited on the TCO layer of the cell. The desired height on the hybrid was set on 6 µm and the height on the SHJ was set to 2 µm.

4.2.1 Results and discussion for hybrid cells

The width, height and aspect ratio of the Al e-beam evaporated fingers are quite steady, whereas the finger opening in the photo resist is exactly the width of the remaining finger after liftoff. The physical parameters of the fingers of the different DIEs of the hybrid cell are shown in Table 4.1Table 3.1. The 3x3 mask was used for lithography of this device. The external parameters following from the J-V measurement are given in Table 4.2. The best solar cell was DIE 4, with a efficiency of 21.0%. The other DIEs performed less and have an average of 19.84%.

Table 4.1. The average width, height and aspect ratio of the fingers of the different DIEs of a hybrid device with 3x3 mask.

	Width of finger (µm)	Height of finger (µm)	Aspect ratio of finger
DIE 1	115	6.0	0.05
DIE 2	120	6.0	0.05
DIE 3	230	6.0	0.03
DIE 4	190	6.0	0.03

Table 4.2. The external parameters of the different DIEs from a hybrid solar cell with 3x3 cm^2-large mask.

	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	R_{sh} ($k\Omega \cdot cm^2$)	R_s ($\Omega \cdot cm^2$)	η (%)
Average (4 cells)	697.5	39.14	72.7	13.51	1.995	19.84
Best	704	40.7	73.8	18.0	1.84	21.0

4.2.2 Results and discussion for SHJ cells

The physical parameters of the metal fingers of the SHJ solar cell are shown in Table 4.3. The external parameters of the device after the J-V-measurement are shown in Table 4.4. The best DIE is DIE 1. The device shows a rather high series and low shunt resistance, which leads to a low fill factor.

Table 4.3 The average width, height and aspect ratio of the fingers of the different DIEs of a SHJ device with 3x3 cm^2-large mask.

	Width of finger (µm)	Height of finger (µm)	Aspect ratio of finger
DIE 1	115	2.0	0.017
DIE 2	120	2.0	0.016
DIE 3	230	2.0	0.009
DIE 4	190	2.0	0.010

Table 4.4. The external parameters of the different DIEs from a SHJ solar cell with 3x3 cm^2-large mask.

	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	R_{sh} ($k\Omega \cdot cm^2$)	R_s ($\Omega \cdot cm^2$)	Efficiency (%)
Average (4 cells)	685	39.48	61.0	0.41	3.63	16.50
Best	694	39.10	65.0	3.16	5.56	17.71

4.3 Cu plating

The copper electroplating process needs more steps than the e-beam evaporation of aluminum. Because IO:H dissolves directly in the copper plating solution and ITO dissolves when a negative current is fed to it (so electrons are delivered to the ITO layer), the front TCO layer that is not being metallized, needs to be protected from the solution. The most efficient method would be to first do a evaporation of titanium on a with photo resist covered wafer and the subsequent lift-off procedure. Then Ti is only there were it should be. By covering the device with a second layer of photo resist, the geometrical design of the mask could be aligned with the first one. This is achieved through alignment markers. However, on a textured wafer these alignment markers are not visible and therefore an alignment cannot be done. Therefore a full area deposition of Ti is chosen as the seed layer. The layer is 300 nm thick and is evaporated by e-beam with the *CHA opdamper*. The pressure during evaporation was $4 \cdot 10^{-7}$ mTorr and the deposition rate was 1 Å/s. After the evaporation a photo resist layer with openings is made with the lithography method in the MEMS lab. The mask that is used for the plating is the mask with the 3x3 cm^2-large DIEs. After the lithography the device is attached on the wafer holder with four clamps. The clamps conduct the current from the connection bar of the holder to the seed layer on the device. When the wafer holder is placed in the bath, the stirrer is running and both the connection bar from the wafer holder (positive pole) and the copper plate (negative pole) are connected to the external power source, the electro plating is started. The copper plating process is done under a constant current of 1.4 A for a time of 1500 seconds. The voltage is not constant. Because of the protection of the photo resist, pulse plating is not necessary for these devices. After plating, the height of the copper is checked with 1D-profiling and if the height is satisfying, the photo resist is removed by acetone rinsing. The last step is the wet etching of the 300 nm of seed layer. The etching is done in several minutes. The etching bath does not etch copper or the ITO top layer. The rear is protected with a thin layer of photo resist during the etching.

4.3.1 Results and discussion for hybrid cells

The height, width and aspect ratio of the hybrid solar cell are shown in

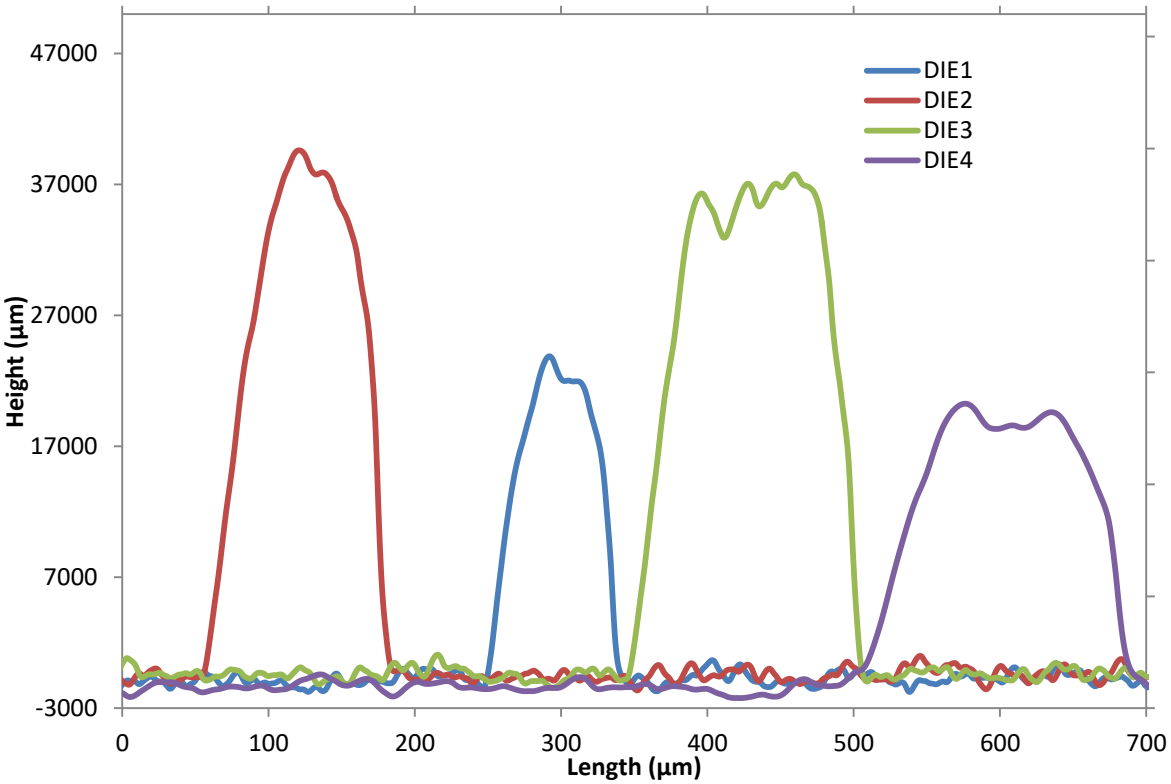


Figure 4.3 and Table 4.5. The results show that the aspect ratio of DIE 4 is somewhat less than the other DIEs. This is probably caused by a not perfectly connected clamp near this DIE. Nevertheless the aspect ratio is still very reasonable. The results of the J-V-measurement are shown in Table 4.6. The best DIE from this wafer was DIE 2, with an efficiency of 19.55%. The short current density is given by the EQE measurement and then corrected for the shading losses.

Table 4.5. The average width, height and aspect ratio of the fingers of the different DIEs of a hybrid device with 3x3 mask.

	Width of finger (µm)	Height of finger (µm)	Aspect ratio of finger
DIE 1	115	27.4	0.238
DIE 2	120	35.0	0.287
DIE 3	230	45.1	0.266
DIE 4	190	24.4	0.126

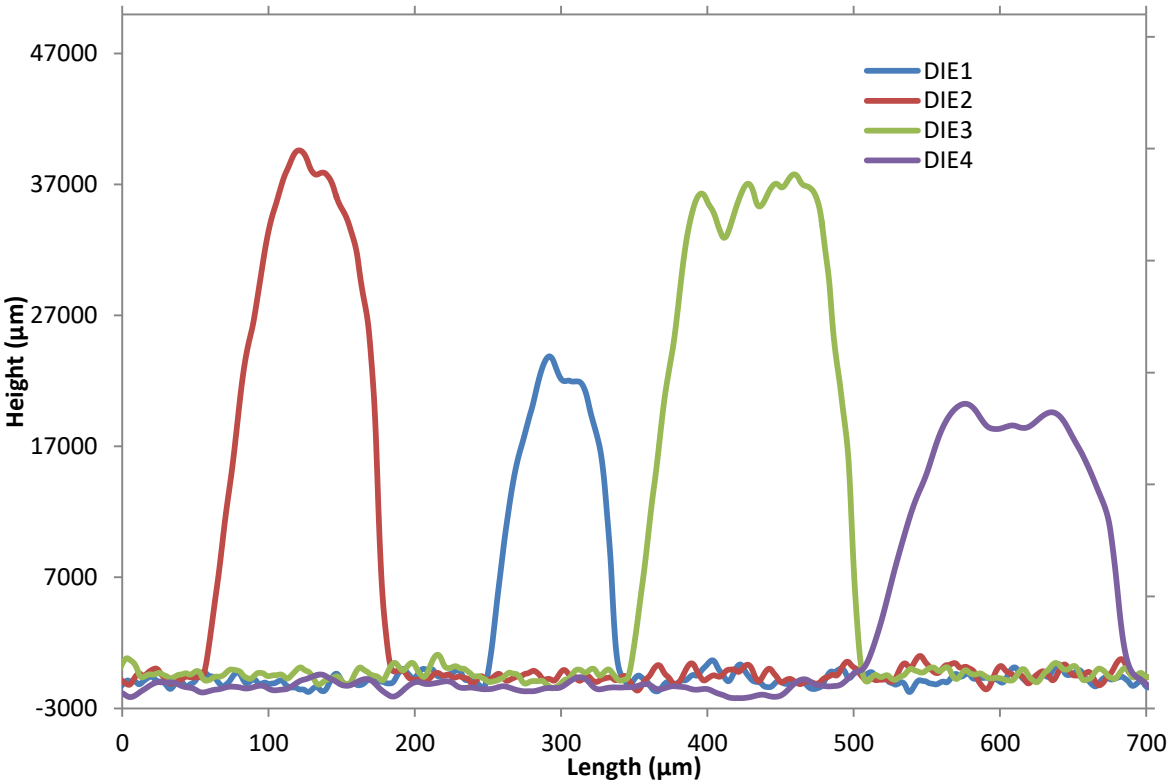


Figure 4.3. The height and aspect ratio of the fingers of the four DIEs

Table 4.6. The external parameters of the hybrid cell for the different DIEs

	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	R_{sh} (kΩ·cm^2)	R_s (Ω·cm^2)	η (%)
Average (4 cells)	692.25	37.37	74.5	2.4	1.64	19.27
Best	690	37.79	75.0	2.73	1.58	19.55

4.3.2 Results and discussion for SHJ cells

The plating time for this device was 1800 seconds to further increase the height of the fingers. The height, width and height, width and aspect ratio of the hybrid solar cell are shown in Table 4.7. The results of the J-V-measurement are shown in

Table 4.8. The best DIE from this wafer was DIE 2, with an efficiency of 18.40%. The short current density is given by the EQE measurement and then corrected for the shading losses.

Table 4.7. The average width, height and aspect ratio of the fingers of the different DIEs of a SHJ device with 3x3

	Width of finger (µm)	Height of finger (µm)	Aspect ratio of finger
DIE 1	115	33.4	0.290
DIE 2	120	50.0	0.417
DIE 3	230	38.3	0.167
DIE 4	190	42.8	0.225

Table 4.8 The external parameters of the SHJ cell for the different DIEs

	V_{oc} (mV)	Suns-V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	pFF (%)	R_{sh} (kΩ·cm^2)	R_s (Ω·cm^2)	η (%)
Average (4 cells)	672	707	36.84	71.9	80.5	1.81	2.09	17.79
Best	672	706	38.39	71.5	80.5	1.20	2.07	18.40

The results show a rather dramatic decline in V_{OC} when compared to the Suns-V_{OC}. This can be caused by Cu particles that diffused into the rear. This will lower increase the J_0 and thus decrease the V_{OC}.

4.4 Ag screen printing

Where for other metallization techniques the TCO layer is sputtered over the full area of the wafer, the TCO layer for Ag screen printed wafers can be sputtered via hard mask. This will reduce shunt paths. After sputtering, the device is taken outside of the laboratory for screen printing. With a Matlab-written script and a webcam, the grid can be aligned on the isolated, active areas. Before the

paste is put on the screen, it is stirred for more viscosity. The paste is put in front of the squeegee and the wafer is placed under the screen by an air-pressure driven movement of the table. The squeegee is then moved automatically over the screen/wafer back and forth. After printing, the wafer is put in a Heraeus forced air oven at 170° C for one hour to dry the paste and decrease the contact resistivity [31] [37]. After annealing, the rear of the wafer is metallized with the Ag/Cr/Al stack. The screen for screen printing full area Ag paste was tested as well. However, this was only done on a flat test wafer and so only the physical results will be examined. No solar cell device with a screen printed rear was made.

4.4.1 Results and discussion screen printing

In order to examine if the old paste was still usable, the contact resistivity (ρ_c) of the paste on ITO was measured. Because the measured ρ_c was higher (32.09 $m\Omega \cdot cm^2$) than ρ_c found in literature (up to 12.78 $m\Omega \cdot cm^2$ [38]), the paste was thinned by the use of an organic solvent. This solvent was also used to clean the screens after printing. This made the paste more viscous and this lowered the contact resistivity to 7.54 $m\Omega \cdot cm^2$, which is in line with literature. Therefore, this diluted paste was used for screen printing on a hybrid solar cell. The external parameters of the J-V-measurement, which will be shown in the next section, show that the conductivity was very poor and thus that the paste needed to be replaced. Screen printing on the SHJ cell was therefore done with a new fresh paste. The physical results of the screen printing are shown in Table 4.9. The two wires of the screen are each 7 micron thick, which will result in an average thickness of 14 micron for each DIE. The height of the full area rear was measured from the unprinted edge of the wafer to the center. Although printing was done on a flat wafer, the 1D-profiling shows a wave-like height pattern. This is caused by the wires of the screen. Nevertheless the bulk area is quite high and shows an average thickness of 6 micron.

Table 4.9 The average width, height and aspect ratio of the fingers of the different DIEs of a screen printed device with H-grid mask

	Width of finger (µm)	Height of finger (µm)	Aspect ratio of finger
DIE 1	105	14.0	0.133
DIE 2	100	14.0	0.140
DIE 3	110	14.0	0.127
DIE 4	150	14.0	0.093

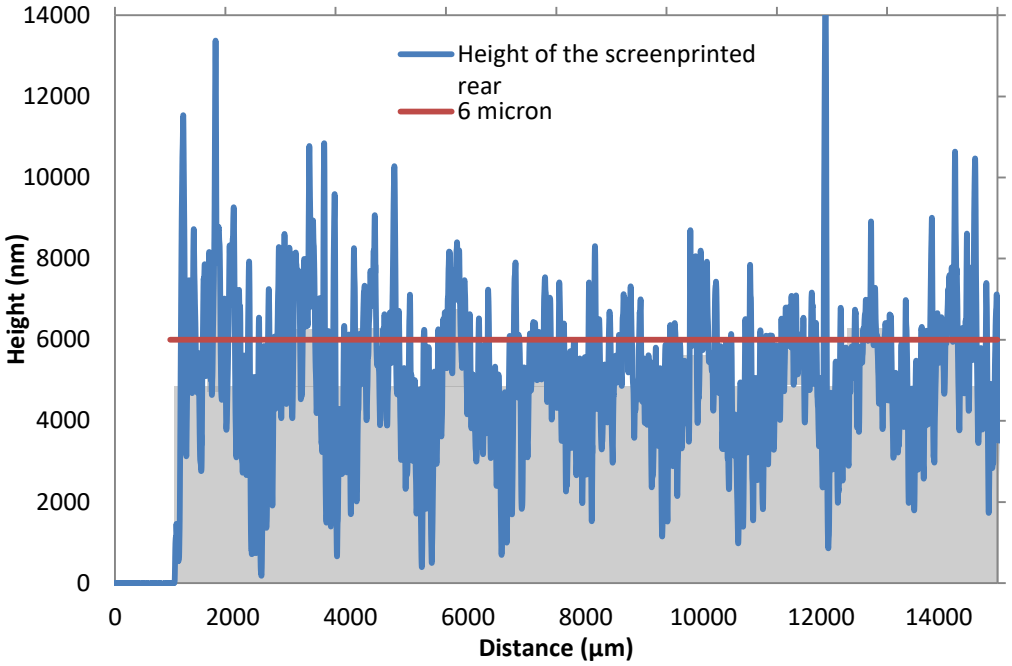


Figure 4.4. 1D-profiling of the screen printed rear on a flat wafer.

4.4.2 Results and discussion for hybrid cells

The results of the J-V-measurement of the screen printed hybrid cell are shown Table 4.10. it shows a poorly working device with only the shunt resistance as expected. The best DIE was DIE 2. The poor results are caused by the poor state of the old paste. Due to long delivery time of the paste, the hybrid cell could not be tested with fresh paste.

Table 4.10. The external parameters of the different DIEs from a Ag screen printed SHJ solar cell with H-grid mask.

	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	R_{sh} (kΩ·cm^2)	R_s (Ω·cm^2)	η (%)
Average (4 cells)	643.5	29.08	55.3	4.462	6.94	10.17
Best	676	30.35	54.0	1.43	8.06	11.15

4.4.3 Results and discussion for SHJ cells

The results of the screen printed SHJ cell is shown in Table 4.11. This wafer was printed with fresh paste. The new paste shows results which are closer to the expected performances than with the old paste. The best DIE was DIE 2.

Table 4.11. The external parameters of the different DIEs from a Ag screen printed SHJ solar cell with H-grid mask.

	V_{oc} (mV)	Suns-V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	pFF (%)	R_{sh} (kΩ·cm^2)	R_s (Ω·cm^2)	Efficiency (%)
Average (4 cells)	695	709	36.86	64.4	80.4	6.65	4.00	16.5
Best	699	712	37.71	69.2	80.4	3.06	3.36	17.4

4.5 Conclusions

4.5.1 Conclusions for hybrid cells

The best performance of a hybrid cell is given by the reference cell with the e-beam evaporated Al as a front contact. This is caused by the better open circuit voltage and short circuit current density. However, the metallization through Cu-plating shows that an increase in FF is possible. As Figure 4.5 shows, the fill factor is on average 1.8 % absolute higher than the average FF of the Al evaporated Al, caused by the decrease of series resistance. The decrease of the other two external parameters, the V_{OC} and J_{SC} is probably caused by contamination of Cu particles. Copper has, as a deep level impurity, a negative influence on the diffusion length of the minority carrier in both emitter and bulk [39]. This will lead to an increase in recombination and therefore to a decrease in V_{OC} and J_{SC}. Whereas the front of the wafer is covered with both Ti and photo resist, the contamination is probably caused through the rear of the device. It is expected that protection of the rear with photo resist will protect the rear from penetration of Cu particles. Another possible explanation for the decrease of the external parameters is the loss of passivation during etching. Although both optical and conductivity properties of the ITO are unchanged during etching, it is possible that etchant diffuses through the ITO and damages the passivation of the c-Si surface. To overcome this, and decreasing the difficulty of the Cu-plating method itself, it is possible to skip the etching part completely by introducing flat alignment markers. More about this technique will be explained in the outlook of this thesis.

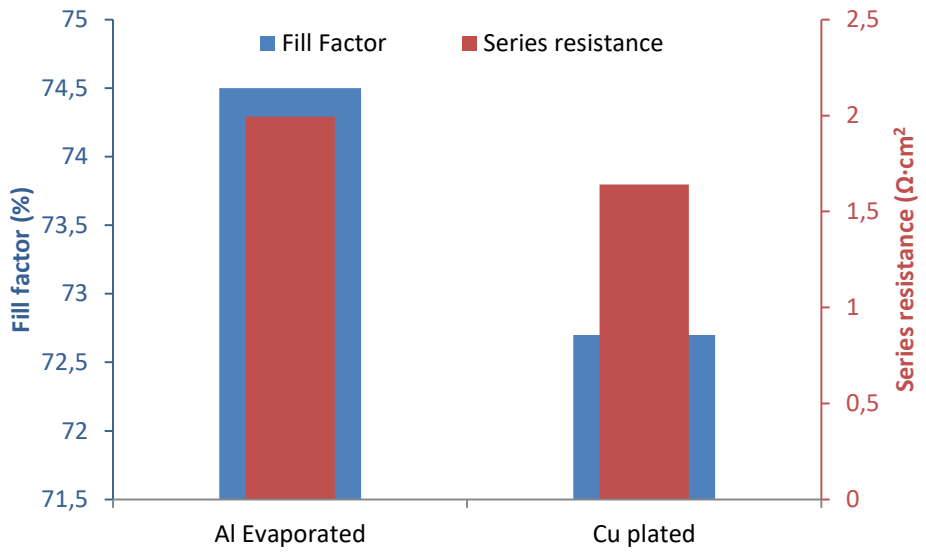


Figure 4.5. The FF and R_s of the Al evaporated (left) and Cu-plated (right) hybrid device.

4.5.2 Conclusions for SHJ solar cells

As can be seen by the results of the reference cell, the FF is the lacking parameter for this device, with only 61.0% as an average FF. The Cu-plating technique results in a significant increase in FF of 10.9% absolute, as is shown in Figure 4.6. V_{OC} and J_{SC}, however, have the same decrease as was seen by hybrid cells which is probably caused by the same contamination as describe in previous section. Although the series resistance of the Ag paste printed device is higher than the reference cell, the overall FF is still higher for the screen printed device. This is mainly due to the higher shunt resistance, which is a result of improved processing of the cell. Because both the aspect ratio and conductivity of the screen printed fingers are higher than the Al evaporated fingers, the difference in series resistance is probably caused by the contact resistance and difference in mask.

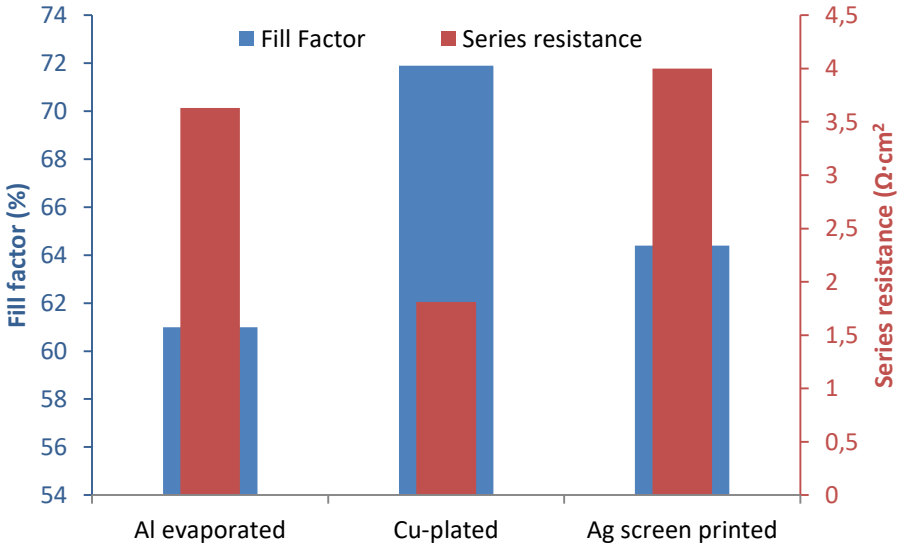


Figure 4.6. The FF and R_s of the Al evaporated (left), Cu-plated (middle) and Ag screen printed SHJ device.

5 Optical measurements of rear contacts

In this chapter the optical properties of several different metal back reflector stacks will be measured. The metal stacks are deposited on a flat glass plate. This glass plate is then measured for reflectance properties. The influence of a lower evaporation pressure and a lower deposition speed will also be investigated.

5.1 Influence of contact metal thickness

The standard metal stack for metallization of the rear of a solar cell consists of 200 nm of silver as a reflector, 30 nm of chromium to prevent aluminum particles to penetrate the silver and a bulk layer of aluminum with a thickness of several micrometer to extract the carriers. This will be the reference stack. First, different types of metals will be tested. The different stacks are shown in Table 5.1. Next, the silver layer thickness was varied, in order to possible reduce the use of expensive silver. The different samples that were tested are shown in Table 5.2. The different surroundings that the light passes are illustrated in Figure 5.1.

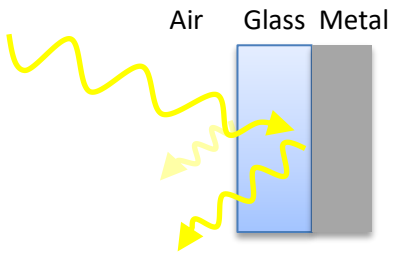


Figure 5.1. The different layers of the sample.

Table 5.1. Metal stacks with different metals at the front.

Sample name	Metal stack
Ag/Cr/Al	200 nm Ag, 30 nm Cr, 300 nm
Al	300 nm Al
Al/Ag/Cr/Al	5 nm Al, 100 Ag, 15 nm Cr, 300 nm Al
SPAg	6 µm screen printed Ag
Evaporated Ag/SPAg	200 nm evaporated Ag, 6 µm screen printed Ag

The results are shown in Figure 5.2. The results show that all metals have a poor reflection in the small wavelengths range. For silver this can be explained because the plasma frequency of the metals is lower than the frequency of the photon in this range [40].

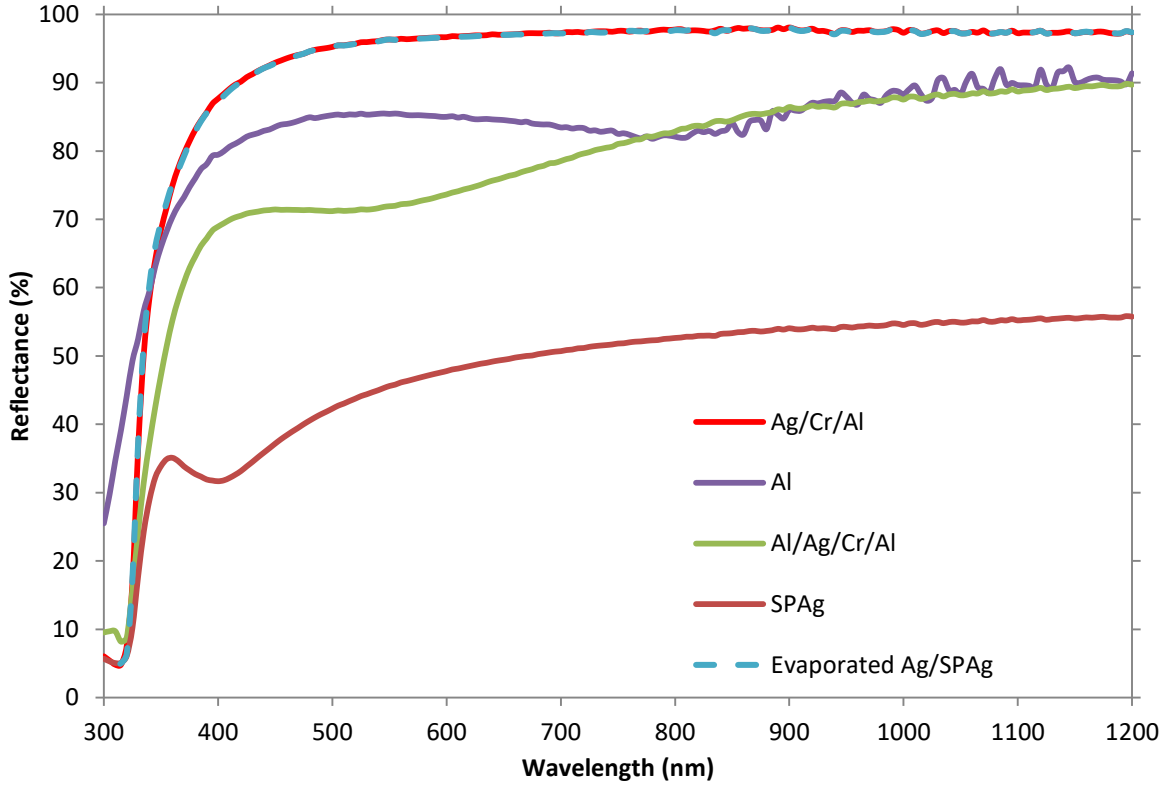


Figure 5.2 The reflectance versus wavelength for stacks with different types of metal on the front.

This results in a transparency of the metal and thus a lack of reflectance. The plasma frequency of Al (82 nm [40]), is higher than the frequency of the photon at 300 nm, so one should expect more reflectance in the lower wavelengths range for aluminum.

From the results it follows that most light is reflected by the rear that has evaporated Ag red and blue dotted line). The screen printed silver (dark red line) has a really weak reflectance. This is mainly because the screen printed rear is very transparent by a lack of dense paste, as can be seen in Figure 5.3. This is caused by the mesh of wires of the screen, as shown in Figure 2.8. However, when silver is screen printed on a layer of evaporated silver, the reflectance is optimal and there is also a high bulk metal for conduction. The Al/Ag/Cr/Al (green line) stack was made with the hypothesis that optically the light would not be influenced by the thin aluminum layer and would therefore have the same reflectance of the Ag/Cr/Al stack. The semiconductor-metal junction would be with the lower work function of Al when compared to the work function of Ag. This could be beneficial for a n-type rear. However, the reflectance pattern of this stack is lower than the reflectance of either a thick layer of only Ag or Al as first metal. Especially in the short wavelength range the Al/Ag/Cr/Al stack performance significantly worse than the normal Al stack. In the long wavelength range the reflectance of this stack is equal to the reflectance of a stack with only Al.

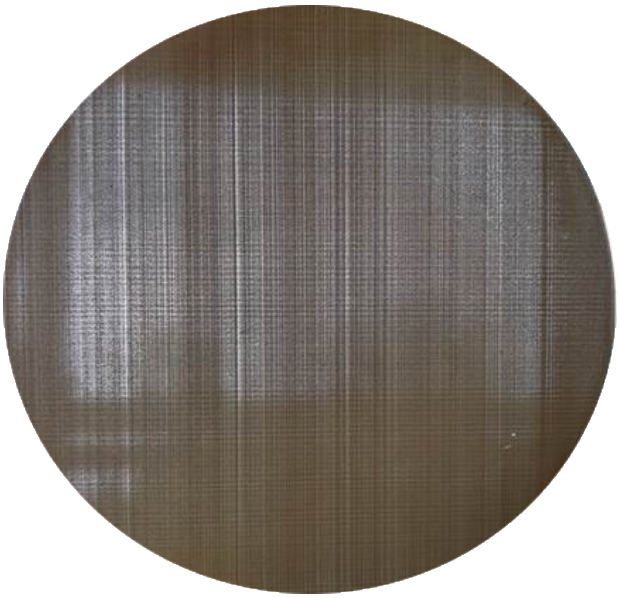


Figure 5.3. Screen printed silver on a glass plate in front of daylight.

Table 5.2. Metal stacks with different thicknesses of silver at the front.

Sample name	Metal stack
25AgCrAl	25 nm Ag, 15 nm Cr, 300 nm Al
50AgCrAl	50 nm Ag, 15 nm Cr, 300 nm Al
75AgCrAl	75 nm Ag, 15 nm Cr, 300 nm Al
100AgCrAl	100 nm Ag, 15 nm Cr, 300 nm Al
200AgCrAl	200 nm Ag, 15 nm Cr, 300 nm Al

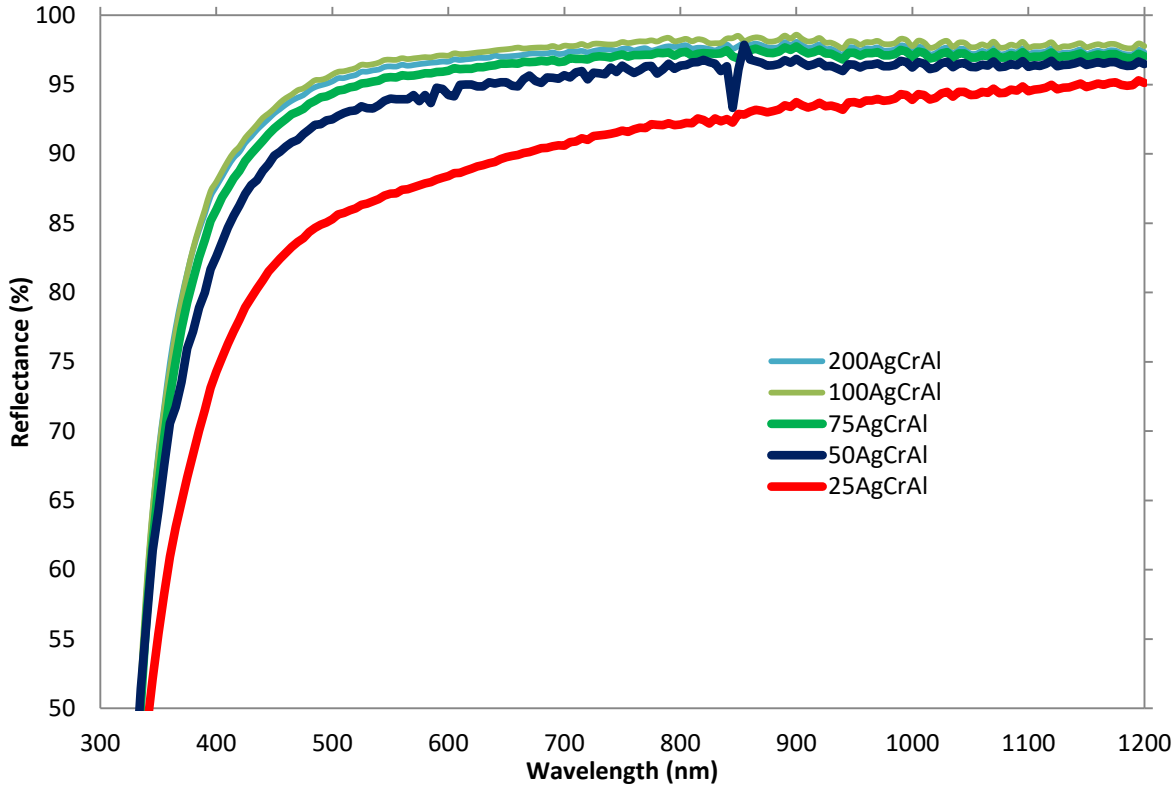


Figure 5.4. The reflectance versus wavelength for stacks with different thicknesses of silver

Figure 5.4 shows the reflection graph for the different thicknesses of silver. The strange peak in the 50AgCrAl (blue) is probably caused by the switching from one lamp to the other. The graph shows that the reflectance increases with an increase of the thickness of the silver layer until a thickness of 100 nm. This means that a thickness of 100 nm is enough for having the optimal reflectance.

As a last test, the same stack of metals was used, but the evaporation was under different conditions; one reference stack (100 nm Ag, 15 nm Cr, 500 nm Al), one slow deposition stack (same metal thicknesses, but with a lower deposition rate) and one low pressure stack (same metal thicknesses, but evaporated under lower pressure). The results are shown in Figure 5.5 and do not show any differences between the different conditions.

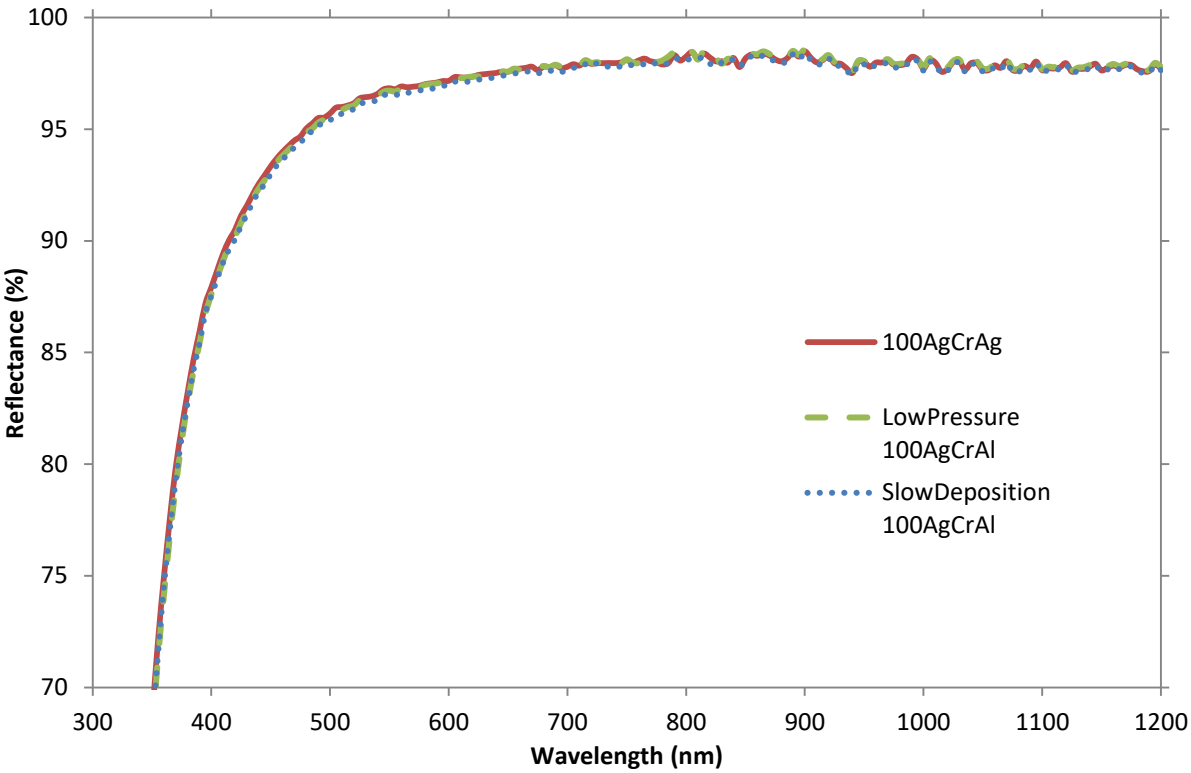


Figure 5.5. The reflectance of stacks made under different conditions

5.2 Conclusions

The results from the optical measurements show that a metal stack with evaporated silver as the first metal gives the best reflection performance. The screen printed rear has a rather high transparency caused by the wires of the screen. It has however a large volume of metal, which have a beneficial influence on the conductivity of the rear metal. The lack of reflectance can be solved by first thermal Ag evaporating on the rear and then make the screen printing. This will result in a highly reflective and conductive rear. An extra positive point is that no e-beam evaporation is used by the fabrication of this stack, so possible damage to the layers by the electron beam can be ruled out. A thickness of 100 nm of Ag is already enough to have an optimal reflection of the metal. When compared to the standard recipe for the rear, 200 nm of Silver, this could save up to 50% of the costs of expensive silver. The conditions of the evaporation, such as deposition rate and pressure in the chamber, do not have any significant influence on the optical characteristics of the metal.

6 General conclusions and Outlook

6.1 General conclusions

The aim of this thesis was to optimize metallization step in solar cells fabrication to further improve their performance. The objective was to increase the fill factor of the devices, mainly by lowering the series resistance. This was done for three different architectures of solar cells, i) a poly/poly with a non-conductive layer, ii) a hybrid solar cell with TCO toplayer and iii) a silicon heterojunction (SHJ) solar cell with TCO toplayer.

The reference metallization technique was e-beam evaporated Aluminum. This technique is mostly used within the PVMD-group. The downside of this technique is that it has a rather limited maximum height. Therefore other techniques are experiment, which, theoretically, can achieve thicker metal than e-beam evaporation technique.

For the first type of solar cell, the poly/poly with non-conductive anti-reflection coating (SiN_x), the highest efficiency is reached with the DC Cu-plated device with H-grid design (an increase of 0.3% absolute when compared to reference Al evaporation, with a 2.3% absolute higher FF). However, there was some unwanted growth of Cu between the fingers, which would have a negative influence on the current density (ΔJ_{sc}=-0.2 mA/cm^2). Therefore, pulse Cu-plating on Ti is recommended for front metallization of a poly/poly device. Another possibility is sputtering of Al instead of evaporating. In this way, a thicker layer can be made, although it does need some addition steps.

For the hybrid cell with TCO as anti-reflection coating, the reference device gave the highest efficiency. This was mainly because the V_{OC} and J_{SC} of this device were higher than the V_{OC} and J_{SC} of the Cu-plated device. The FF of the Cu-plated device did show an increase with 1.8% absolute in comparison with the FF of the evaporated device. This was caused by the decrease of the series resistance, because of the higher conductivity of the metal. The decrease of V_{OC} and J_{SC} is caused by the deep level impurity of Cu. This results in a higher recombination rate and therefore lower J_{SC} and V_{OC}. Most likely this can be prevented by shielding the rear with a layer of photo resist during the Cu-plating, which will probably lead to a device with a good V_{OC}, J_{SC} and FF. Therefore it is recommended to use Cu-plating as a metallization for record breaking devices. Because the metallization method of Cu-plating is quite difficult and has changes for contamination, it is recommended to use Ag-paste screen printing for devices which only need to be compared to each other, e.g. for finding an optimum thickness of a layer. It is expected that the new paste will give at least the same FF as evaporated Al and the process is easier than the evaporation of Al or Cu-plating, because no lithography or lift-off is needed. This is especially true when multiple devices need to be metallized, whereas the screen printing does have some time-consuming. Another advantage of Ag-paste screen

printing is that no e-beam evaporation is needed at all, which will prevent any possible damage inflicted by the e-beam.

For SHJ solar cell devices the Cu-plating embodiment gave the highest efficiency. Although the V_{OC} and J_{SC} suffer from the same problem as the hybrid cell (lower because of Cu contamination), the increase of FF, 10.9% absolute, is so high that the overall efficiency is still higher than the reference device. By shielding the rear, it is expected that the J_{SC} and V_{OC} are higher and thus the efficiency can be further increased. The recommendation for SHJ cells is therefore the same as for the hybrid device; Cu-plating for record-breaking devices, Ag-based screen printing as easy metallization method.

Optical measurements show that thermally evaporated Ag has the highest reflectance of when compared to e-beam evaporated Al and screen printed Ag. It shows that 100 nm of Ag is already enough to have an optimum reflectance, which is halve of the thickness that is now used as a standard recipe for rear metallization. The entire standard recipe is 200 nm Ag, 30 nm Cr and 1.4 µm of Al. Al is used as a bulk. By screen printing Ag on top of 100 nm Ag, an highly reflective and conductive rear is achieved, with the side benefit that no e-beam evaporation is needed at all. The 100 nm evaporated Ag/6 µm screen printed Ag stack is therefore recommended as rear metallization.

6.2 Outlook

6.2.1 Rear protection

For further research on metallization the rear should be protected by a layer of photo resist during plating. This can be done by first doing a standard lithography on the front and then putting some photo resist on the rear. The photo resist can be heated on a hotplate when a blue laboratory wipe is placed between the wafer and the hotplate to avoid melting of the photo resist on the down faced side. Results from a J-V-measurement should then show is the protection was sufficient enough to prevent Cu contamination.

6.2.2 Aligning with flat alignment markers

In order to skip the Ti-etching step, one could use flat alignment markers, as shown in Figure 6.1. By protecting these alignment markers with SiN_x before texturing, the alignment markers remain flat and thus visible. After texturing, the SiN_x is etched and the process is the same until the metallization. Then photo resist is deposited and an aligned lithography is done. Ti is evaporated and a lift-off is done. A second deposition and aligned lithography is done to protect the TCO layer from dissolving in the plating solution. After plating, the cell is ready and does not need any etching.

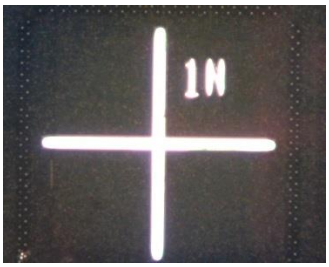


Figure 6.1. Flat alignment markers are visible on textured wafers.

6.2.3 Deposition of a capping layer

Because Copper oxidizes rather fast in air, as shown in Figure 6.2 a), a capping layer is needed for long term stability. When flat alignment markers are used, the photo resist that is used to protect the TCO, can also be used when a small layer of Ag is thermally evaporated on top of the Cu. Optically 50 nm of Ag looks to be enough to cap the Cu, see Figure 6.2 b), although further research is needed. For capping a poly/poly device, most likely wet plating of Ag or Sn is necessary to make a capping layer on the Cu.

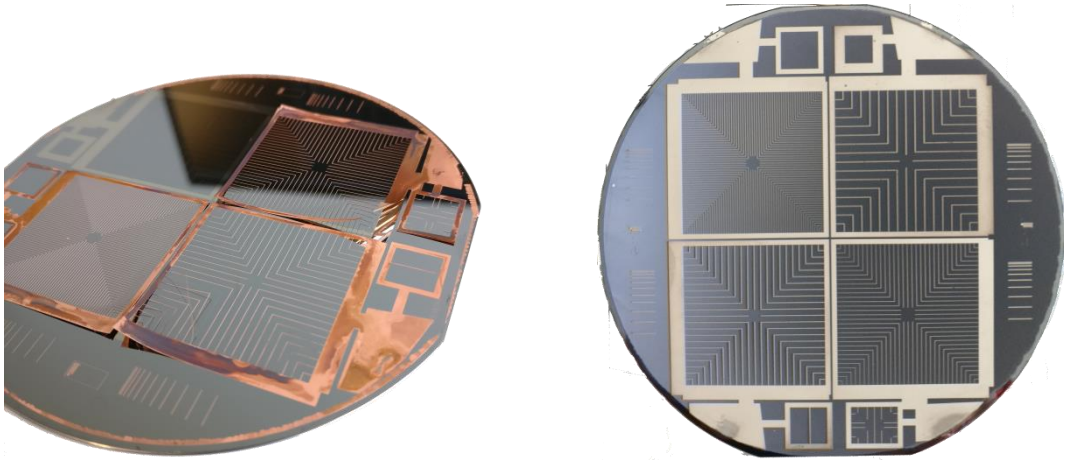


Figure 6.2. (a) oxidized Copper of a flat wafer after 30 min in oven and (b) Thermal evaporated Ag capping layer.

7 References

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