Energy-Efficient Readout of Resonant Sensors

Zeng Zeng
4046064

Supervisor: Dr. M.A.P.Pertijs

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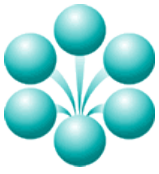

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Committee members:

Prof. K.A.A. Makinwa	(TU Delft: Electronic Instrumentation Laboratory)
Dr. M.A.P. Pertijs	(TU Delft: Electronic Instrumentation Laboratory)
Dr. W.A. Serdijn	(TU Delft: Electronics Research Laboratory)
Dr. D.M. Karabacak	(Holst Centre)

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Abstract

This thesis discusses the theory, architecture and circuit design and measurements of an ultra-low-energy prototype interface circuit for a resonant gas sensor in standard 0.35-µm CMOS technology.

A transient measurement method is used here. The resonant sensor is driven at a frequency close to its resonance frequency by an excitation source that can be intermittently disconnected causing the sensor oscillation amplitude to decay exponentially. From the ring-down signal, the frequency of the freely oscillating sensor and the quality factor are obtained. Test chips are fabricated to measure the resonance frequency and quality factor of the resonant sensor using ring-down measurement approach. The obtained results(resonance frequency and quality factor) show good consistency compared with what we obtained using an alternative approach (impedance analysis). The circuit consumes an energy of 237nJ per measurement.

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Chapter 1

Introduction

Very high aspect (length/thickness) ratio doubly clamped beam resonators with integrated piezoelectric transducers have been provided by Holst Centre. These resonators are great candidates for application in wireless autonomous sensor systems, owning to their low power consumption, high integratability and high sensitivity. By applying appropriate coatings to these resonators, they can be used to sense concentration of volatile organic compounds like ethanol, benzene etc, by measuring shifts in resonance frequency f_{res} and quality factor Q. But they can only live up to the promise of being highly energy-efficient if energy-efficient readout circuits are available to read them out. This thesis describes the design and characterization of such a readout circuit.
In this chapter, a brief introduction to resonant sensors, including their operating principle, electrical model and power-efficiency potential is presented in section 1.1. After that, readout approaches for resonant sensors, including their principles, advantages and disadvantages are introduced in section 1.2. Finally, an outline of this report is given in section 1.3.

1.1 Resonant sensors

1.1.1 Operating principle

These integrated sensor chips (Fig. 1-1 (a)), consist of very high aspect ratio (length/thickness) beam resonators with integrated piezoelectric transducers (Fig. 1-1(b)) and can be used for chemical sensing applications. These polymer-coated resonators are sensitive to volatile compounds, and require a small amplitude signal (sinusoid for instance) to excite. Thus, the volatile absorption induced swelling of the length-restricted structures, and the resultant stress formation in the structures can be measured as a shift in resonance frequency (f_{res}) or quality factor (Q). Hence, volatile concentration can be derived.
A typical number for the resonant sensitivity to absorption of ethanol has been reported to be 3.6×10^{-6}/ppm [1].

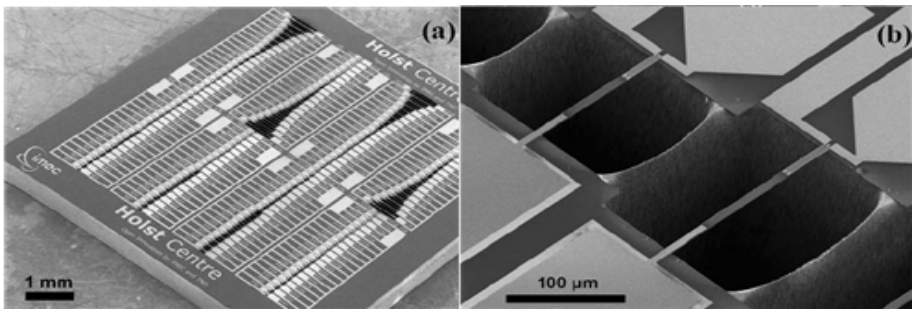

Fig. 1-1: (a) The completed sensor chip consisting of 160 resonators and (b) close-up view of suspended beams [1].

1.1.2 Electrical model

A resonator provides both series and parallel resonance, which can be modeled as an electrical network with a low impedance (series resonance) and a high impedance (parallel resonance) resonance point spaced closely together (Fig. 1-4). In this work, we focus on the series resonance mode. Figure 1-2 depicts the electrical model of the resonator in series mode.

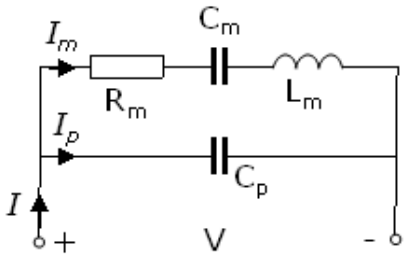

Fig. 1-2: Electrical model of the resonator

The electrical model of the resonator involves two branches: a parallel capacitor (C_p), and a series RLC branch composed of a resistor (R_m), a capacitor (C_m) and an inductor (L_m). The parallel capacitor (C_p) is an indication of the actual capacitance of the piezoelectric patch; while the resistor (R_m) models the losses in the resonator, which cause any oscillation induced in the circuit to die away over time if it is not kept going by a source. The serial motional capacitor (C_m) and inductor (L_m), act as an electrical resonator, storing electrical energy oscillating at the circuit's resonance frequency.

In fact, the complete model contains an infinite number of RLC branches in parallel, each with their own RLC constants that represent the different resonance modes.

At resonance, the series impedance of the RLC tank is at a minimum value, the inductive reactance and the capacitive reactance are of equal magnitude ($\omega \cdot L_m = 1/(C_m \cdot \omega)$, where $\omega = 2 \cdot \pi \cdot f_{res}$). Hence, the resonance frequency(f_{res}) can be calculated by:

$$f_{res} = \frac{1}{2\pi\sqrt{L_m C_m}} \qquad (1\text{-}1)$$

The quality factor is approximately the number of oscillations required for a freely oscillating system's energy to fall off to 1 / $e^{2\pi}$ (or about 1/535), of its original energy [2]. For a series resonator, the quality factor is given by [3]:

$$Q = \frac{1}{R_m}\sqrt{\frac{L_m}{C_m}} \qquad (1\text{-}2)$$

Some typical values of the model parameters for Holst resonators can be found in section 2.1 (Table 2-1).

In some works, damping factor (ζ) or dissipation factor (D) are also used to represent the power loss-rate of oscillation in a dissipative system. The dissipation factor is the reciprocal of quality factor,

$$D = \frac{1}{Q} \qquad (1\text{-}3)$$

and the damping factor is related to quality factor by:

$$\zeta = \frac{1}{2 \cdot Q} \qquad (1\text{-}4)$$

1.1.3 Energy-efficiency

According to [1], the high frequency-selectivity of the resonator enables high frequency sensitivity at low power levels.
For example, the transducer power consumption per device is reported to be less than 100nW, with a low measurement voltage (50–250 mV_{rms}) [1].
Hence, the resonant sensors hold the promise of being highly energy-efficient. But, they can only live up to this promise if energy-efficient readout circuits are available to read them out.

1.2 Readout approaches

There are mainly three readout approaches circuit to measure f_{res} and Q of the resonator: oscillator-based readout, impedance analysis and ring-down measurement.

1.2.1 Oscillator-based readout

1.2.1.1 Basic principles

The basic principle of the oscillator-based readout method (Fig. 1-3) is that the oscillator circuitry maintains the oscillation using a feed-back loop. To sustain the oscillation, two conditions need be satisfied:

- The gain in the feedback loop is larger than one.
- The phase shift around the loop is an integer multiple of 2π.

As a result, the output of the feedback loop is a sustained oscillation signal with a frequency equal to the resonance frequency. Thus, the information about resonance frequency can be extracted. Information about the quality factor is not readily available, but can in principle be extracted as it relates to the energy provided by the oscillator circuit to the resonator [4].

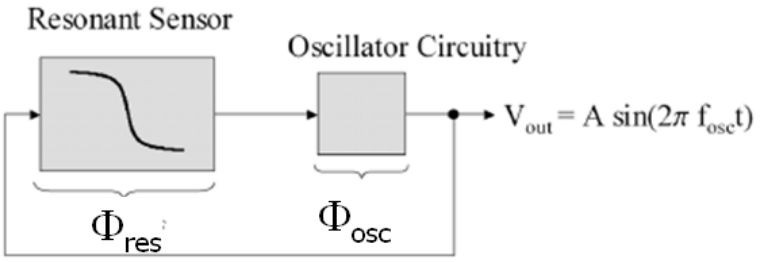

Fig. 1-3: Principle of oscillator-based readout method [5]

1.2.1.2 Advantages and disadvantages

Disadvantages

The output frequency of an oscillator-based readout circuit depends on the phase of the oscillator circuitry (Φ_{osc} in Fig. 1-3); hence, power is needed to ensure a well-defined phase condition of the oscillator circuitry, thus the output resonance frequency is only defined by the resonator.
Although the quality factor can be extracted, for instance, by using automatic gain control (AGC) circuits to derive the energy loss information, it is not so straight forward to extract Q with this readout approach.
Another problem arises in the presence of a large parasitic capacitance C_p (Fig. 1-4).

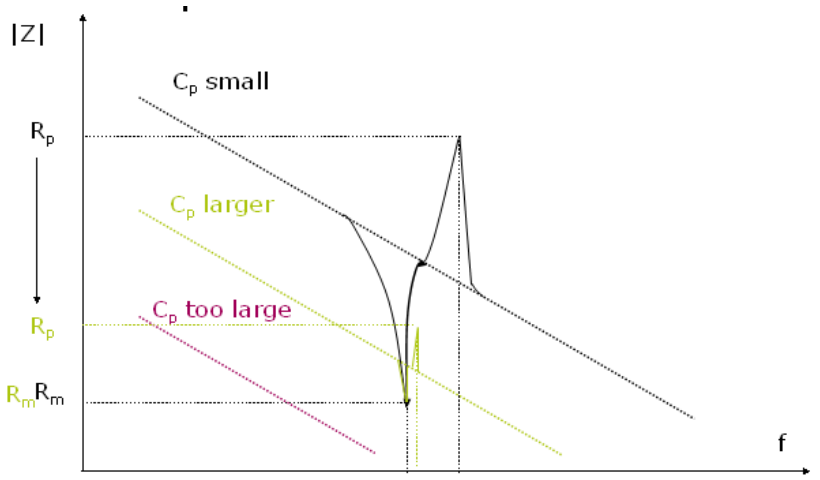

Fig. 1-4: The effect of parasitic capacitance on the impedance of the resonator

Figure 1-4 shows the impedance of the resonator versus frequency for different C_p. A larger parasitic capacitance (C_p) means series and parallel resonance shift closer. If C_p is too large, series and parallel resonance will eventually disappear.
With a large C_p, the phase shift of the resonator at the resonance frequency becomes so small and poorly defined that the oscillator-based readout is hard to implement without cancellation of C_p .
In order to use this method, the following criterion needs to be satisfied [5]:

$$R_m << \frac{1}{2\pi f_{res} C_p} \quad (1\text{-}5)$$

where R_m is the series resistance in the RLC tank, and f_{res} is the resonance frequency. Unfortunately, this condition is not true for Holst resonators.

Advantages

In spite of the drawbacks of the oscillator-based readout method mentioned above, the low cost of the circuitry as well as the integration capability are some features which make this method to be chosen for some sensor applications.

1.2.2 Impedance analysis

Nowadays impedance analysis technique is mainly used for sensor analysis under laboratory conditions, because of the costly and large dimensions of the required equipment. There are also examples of integrated implementations, like the lock-in technique [6]. In this report, if not mentioned, impedance analysis refers to the traditional impedance analysis with bench-top equipment.

1.2.1.1 Basic principles

In this method, impedance or network analyzers measure the electrical impedance or admittance of the resonant sensor over a range of frequencies near resonance for a complete characterization of the device's amplitude and phase response. Figure 1-5 demonstrates the principle of impedance analysis method.

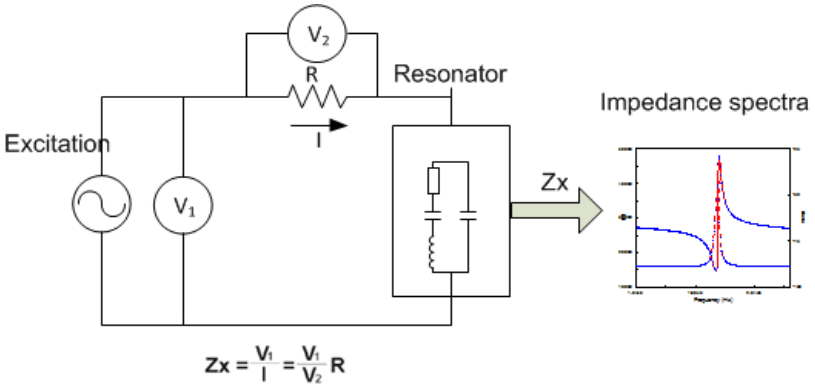

Fig. 1-5: Principle of impedance analysis method

The way to derive the resonance frequency and quality factor is to apply impedance curve-fitting using the resonator model (Fig. 1-2). The values of the model parameters can then be extracted by means of impedance curve fitting. Hence, f_{res} and Q can be calculated by equation (1-1) and (1-2) respectively.

1.2.2.2 Advantages and disadvantages

Disadvantages

- Big and complex equipment is needed in this measurement which results in high cost and poor integration.
- A frequency sweep is required, which implies a relatively long time and an associated high energy consumption.
- The extraction of the resonance frequency and quality factor by means of curve-fitting is relatively computationally intensive.

Advantages

Impedance analysis can be easily implemented with an impedance analyzer.

1.2.3 Ring-down measurement

1.2.3.1 Basic principles

Figure 1-6 displays the block diagram of the ring-down measurement.

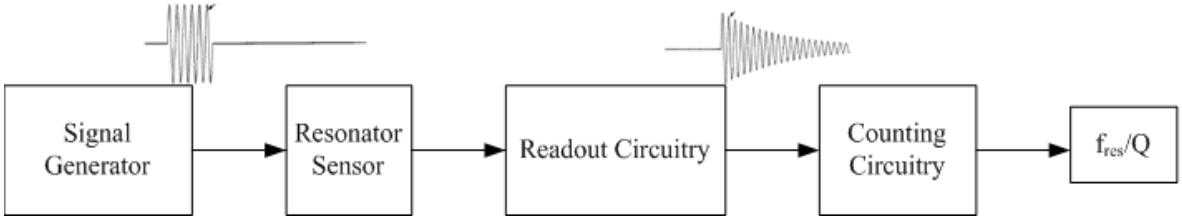

Fig. 1-6: Block diagram of the ring-down measurement

In this technique, the resonator is excited with a signal generator approximately tuned to a frequency of the desired resonance mode. After some time, the excitation signal stops; at this moment, the voltage or current, depending on whether the parallel or series resonant frequency is excited (series resonant frequency in our case), decays as an exponentially-damped sinusoidal signal [7]. From this damped output signal, resonance frequency and quality factor can be extracted, for instance by means of the frequency-counting technique (chapter 2, section 2.2.3).

1.2.3.2 Prior art

Some approaches based on the ring-down measurement have been published before. In this sub-section, we introduce some of the prior work, with a summary in the end.

- [Rodahl, Rev. Sci. Inst. 1996][8]

Figure 1-7 shows the experimental setup of this work.

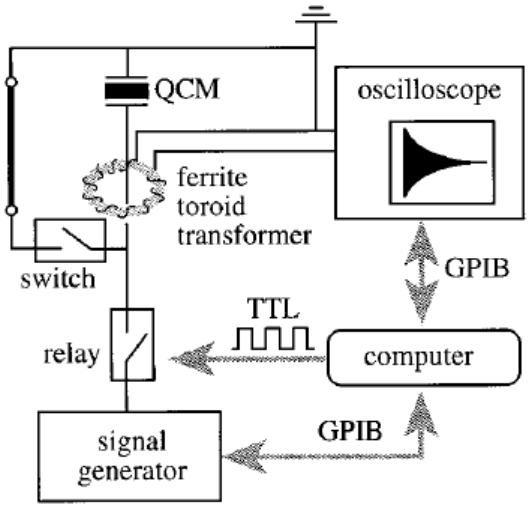

Fig. 1-7: A schematic illustration of the experimental setup used in [8].

The quartz crystal microbalance (QCM in Fig. 1-7) is excited by a signal generator approximately at its resonance frequency. Series resonance can be measured by shorting the resonator, which is controlled by a switch and a relay (Fig. 1-7). The ring-down current is measured using a ferrite toroid transformer and displayed on an oscilloscope. The exponential decay of the resulting waveform is measured and used to determine the resonance frequency and dissipation factor (D=1/Q).

- [Zeng, Rev. Sci. Inst. 2002][9]

To determine the resonance frequency, the resonator is excited with a signal burst of controllable frequency, close to the resonance frequency (Fig. 1-8(a)). After termination of this excitation signal, the sensor oscillates at its characteristic frequency with decaying amplitude (Fig. 1-8(b)). The zero point crossings of the captured transient response are converted to a square-wave (Fig. 1-8(c)). Frequency counting technique is used to measure the resonance frequency.

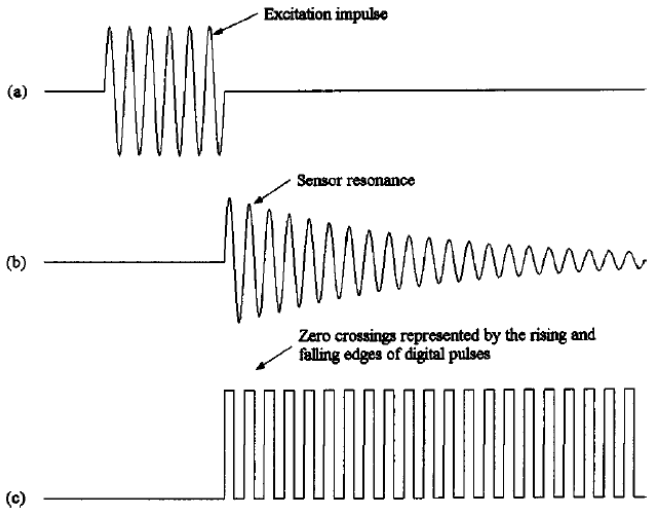

Fig. 1-8: Illustration of frequency counting process for determining the resonance frequency [9]

- [Zeng, Rev. Sci. Inst. 2004][10]

This work is an extension of the previous work. In this work, a method to determine the damping factor/quality factor is introduced.
Two digital pulse-sequences can be generated from threshold comparisons; if two threshold-levels (a_1 and a_2), are applied to the exponentially decaying oscillation. The number of pulses obtained by threshold-level a_1 is N_1, and the number of pulses obtained by threshold-level a_2 is N_2 (Fig. 1-9). Thus the damping factor, as well as quality factor, can be calculated by:

$$\zeta = \frac{1}{2Q} = \frac{\ln(a_1 / a_2)}{2\pi\Delta N} \qquad (1\text{-}6)$$

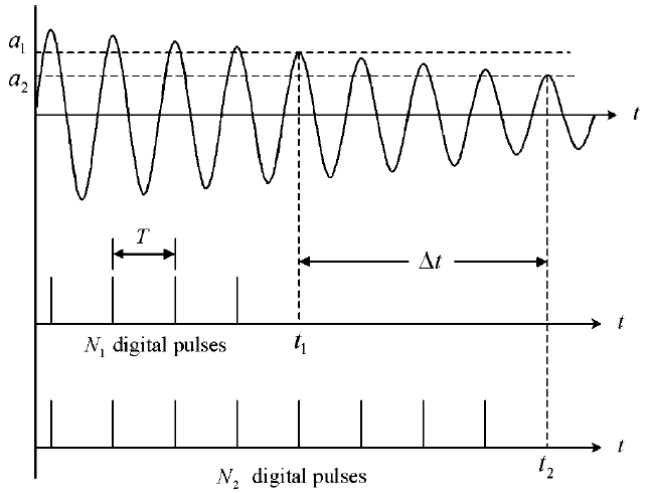

Fig. 1-9: Illustration of damping ratio measurement by threshold-crossing counting [10]

- [Q-Sense E1]

Q-Sense (Gothenburg, Sweden) sells bench-top instruments based on QCM-D technology: Quartz Crystal Microbalance with Dissipation monitoring. Figure 1-9 shows the Q-Sense E1 entry-level system.

Fig. 1-10: Q-Sense E1 entry-level system

The E1 enables accurate and simple QCM-D measurements of real-time molecular interactions, includes sensor chamber, sensor, electronics, flow module, software etc. The QCM-D systems characterize the interface in terms of structure and mass: mass changes are measured as changes in resonance frequency; structural properties are measured as changes in dissipation, which is determined from the time it takes for the oscillation to stop when the power is disconnected (ring-down measurement).

Summary of Prior Art

To conclude, the basic measurement principles for measuring f_{res} and Q based on ring-down are known. The introduced techniques have mainly been implemented using PCBs or bench-top instruments.
There are also some points that have not yet been investigated:

- Integrated implementation of the technique
- Advantages in terms of energy consumption
- Advantages in ability to cancel the effect of C_p

These aspects will be addressed in this thesis.

1.2.3.3 Advantages and disadvantages

Advantages

- Quality factor can be derived easily using threshold-counting technique.

- Potentially energy-efficient since the sensor only needs to be excited briefly at the beginning of a measurement (during which the readout circuit can be powered off); while during the rest of the measurement, the sensor does not have to be driven and only the readout circuit consumes power (chapter 2, section 2.2.1.1).

- Ability to cancel the effect of C_p (chapter 2, section 2.2.1.1).

Disadvantages

This technique has never been demonstrated in an integrated energy-efficient implementation.

1.2.4 Comparison and our solution

Compared with the oscillator-based readout method, the ring-down measurement has the advantages of low energy consumption, ability to measure Q and insensitivity to C_p.
Compared with impedance analysis, the ring-down measurement has the advantages of low energy consumption and possibilities to integrate.
Hence, we choose the ring-down measurement as our approach. In this work, we have developed an energy-efficient integrated implementation, using AMS 0.35μm CMOS technology, to read-out the resonator sensor.

1.3 Outline of the Thesis

The thesis report is divided into five chapters, presenting different aspects of the investigation and the design process.
Following this introduction chapter, chapter two mainly deals with the architecture-level analysis and design of the proposed readout approach. Target specifications, operating principles of different sub-blocks (front-end circuit, comparator and counting circuitry), proposed architectures, error analysis in several aspects and finally, sub-block design requirements will be given in chapter two.
The circuit-level analysis and design of the resonator interface is presented in chapter three. The proposed circuit will be discussed in several sub-sections, including the front-end circuit and the auto-zeroed comparator. The simulation results are also presented and analyzed in this chapter. Apart from the analog design and the simulation results, the digital design is also introduced.
In chapter four, the emphasis is on the measurement results of the system, including the fabricated chip, measurement setup and the analysis of the measurement results.
Finally, in chapter five, conclusions and recommendations are given, including highlights of this work and suggestions for future performance improvements.

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Chapter 2

Architecture-level Analysis and Design

In this chapter, architecture-level analysis and design of the proposed approach are presented in five parts, starting with sensor characteristics and target specifications; followed by operating principles, including front-end operation, comparator operation and counting circuitry operation. Then, error analysis is discussed in four aspects. Based on all these, simulation results and conclusions are given in the end. This chapter gives the information needed (design requirements) for the circuit-level design.

2.1 Sensor characteristics

As with any mechanical structures, each resonator has many modes of vibration. Figure 2-1 shows some different vibration modes of the beam resonator.

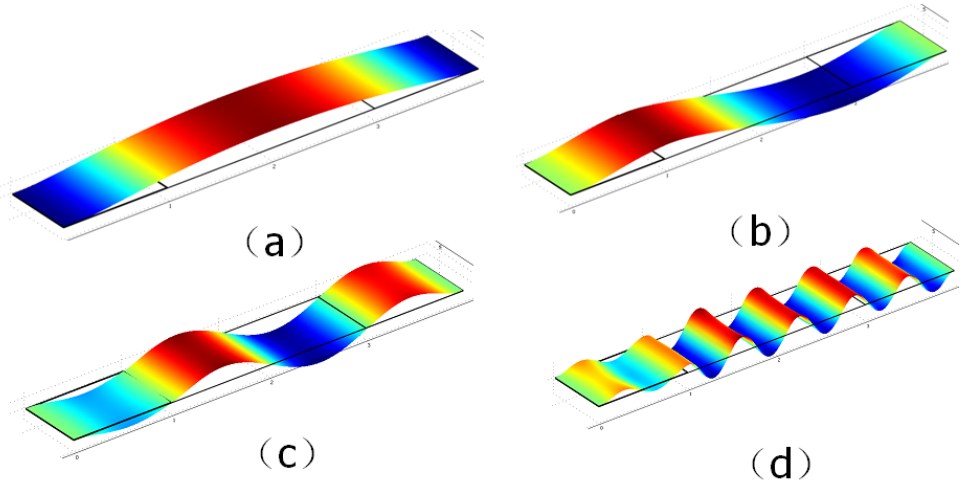

Fig. 2-1: Four different vibration modes of the resonator [1]

The resonator can be modeled as a RLC tank in parallel with a parasitic capacitor (C_p) (chapter 1, Fig. 1-2), and each vibration mode of the resonator can be modeled by different parameters. Figure 2-1 demonstrates the 3D vibration models of a resonator in

fundamental mode (Fig. 2-1(a)) and higher-order modes (Fig. 2-1(b),(c) and (d)). Table 2-1 gives an example with typical values of the model parameters in fundamental mode and a higher-order mode (with lowest R_m value). The resonance frequency is around 80kHz for the fundamental mode and around 2MHz for the chosen higher-order mode.

Table 2-1: Model parameters for two different resonance modes (from a 500µm-length beam) [1]

Model parameters	Fundamental mode	Higher-order mode
R_m	161MOhm	126kOhm
L_m	9.27kH	3.01H
C_m	386aF	2.16fF
C_p	5.73pF	5.48pF
f_{res}	84.1kHz	1.977MHz
Q	30.4	297

The resistance (R_m) in the higher-order mode is much smaller (three-orders of magnitude) than which in the fundamental mode. We can do a rough calculation based on the fundamental mode to see the effect of a large R_m.
If we apply an excitation signal (V_s) with a frequency equal to the resonance frequency, the ring-down current through the RLC tank can be expressed by V_s/R_m (section 2.2.1.2). Hence, we get a typical ring-down current of 1.25nA for the fundamental mode (with a 200mV excitation). To obtain a readable ring-down voltage of $1V_{p-p}$ after integration, a feedback impedance of 5GΩ (feedback capacitance of around 5fF) is required, which is not feasible to implement on chip. While for the higher-order mode, this value is around 0.3MΩ(250fF). We assuming all the ring-down current gets integrated on the feedback capacitor in the above calculations (an assumption that will be discussed in more detail in section 2.2.1.2).
Another point worth to mention in the table is the quality factor (Q). A higher Q indicates a lower rate of energy loss relative to the stored energy of the resonator: the oscillations die out more slowly [2]; hence, more ring-down cycles can be detected with a higher Q device. In this aspect, the higher-order mode also is to be preferred.
Since the fundamental mode is not feasible to implement, we choose the higher-order mode in this project. All the calculations in architecture-level design and circuit-level design are based on the following parameters for the higher-order mode:

- R_m = 126kOhm
- L_m = 3.01H
- C_m = 2.16fF
- C_p = 5.48pF
- f_{res} = 1.977MHz
- Q = 300

2.1.1 Target specifications

In this project, we extract the resonance frequency and the quality factor of the resonator, from which information about the volatile concentration can be derived. The sensitivity of the chosen higher-order mode is expected to have a similar sensitivity for ethanol concentration of 3.6×10^{-6}/ppm (reported in [3]). Hence, to achieve a desired detection limit in terms of ethanol concentration of at least 25ppm, we derive a minimum requirement (0.9×10^{-4}) on the detection limit for the frequency measurement. As a result, we have our detection limit for the interface circuit:

$$\frac{\delta f_{res}}{f_{res}} < 10^{-4} \quad (2\text{-}1)$$

Apart from the detection limit for the resonance frequency, we also define a detection limit for the quality factor measurement:

$$\frac{\delta Q}{Q} < 1\% \quad (2\text{-}2)$$

This detection limit for the quality factor (Eq. 2-2) will not be explicitly considered in our design phase to simplify the analysis.
The main target is to keep the energy per measurement as low as possible while maintaining the above detection limits.

2.2 Operating principles

This section describes the operating principles of the proposed architecture for the interface circuit (Fig. 2-2). We choose capacitive feedback for the integrator in this first approach because resistive feedback (in megaohm) needs large area to implement on chip (can be considered in further work). The whole system consists of: a front-end consisting of a switched excitation source, the resonator with parasitic, and a current-to-voltage converter (also mentioned as “integrator”), and a back-end consisting of an auto-zeroed comparator and counting circuitry. The operation of the read-out circuit will be introduced in three parts: front-end operation, comparator operation and counting circuitry operation.

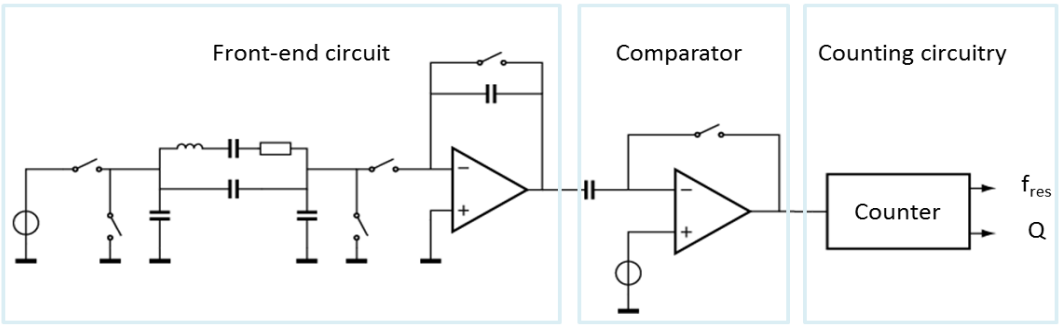

Fig. 2-2: Proposed architecture

2.2.1 Front-end operation

2.2.1.1 Operating principle

The front-end circuit includes three parts: the excitation source, the resonator and the current-to-voltage converter. To make the story clear, we divide the front-end operation into three phases:

- Phase 1: energizing the resonator

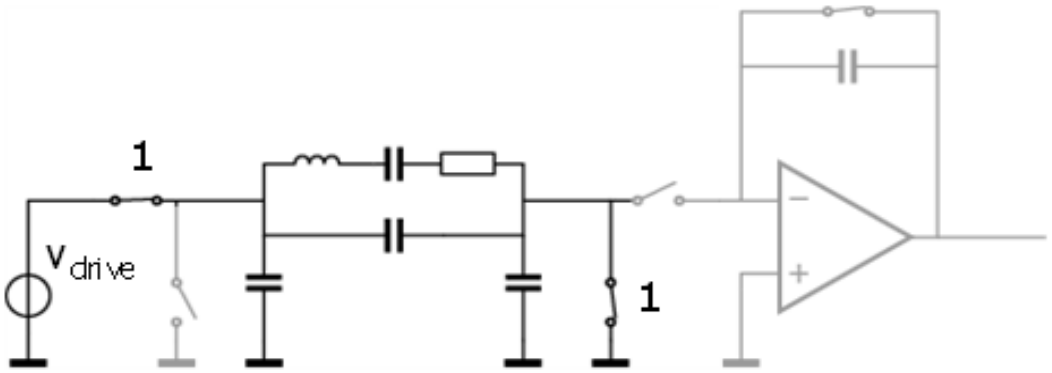

Fig. 2-3: Front-end operation in phase 1

In phase 1, the excitation signal (V_{drive}) is connected to the resonator with a frequency (f_{dr}) close to the resonance frequency (f_{res}) to energize the resonator; while the other side of the resonator is shorted to ground. The remaining circuitry can be powered down to save energy(shown in a lighter color in Fig. 2-3)

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- Phase 2: dissipating the charge on C_p

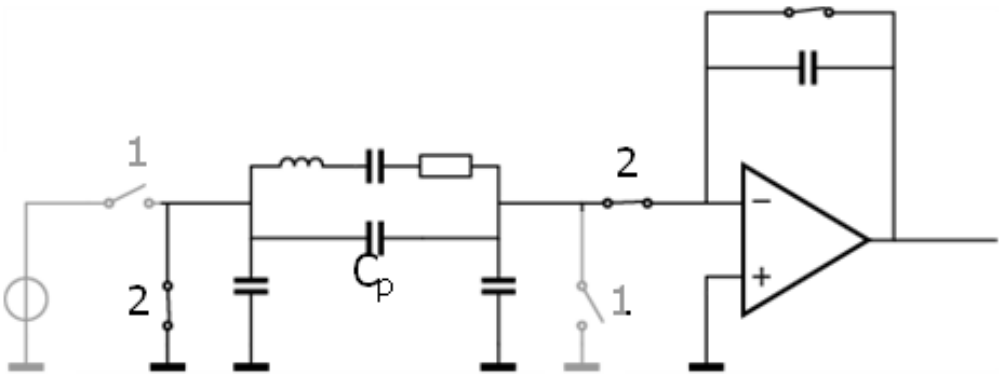

Fig. 2-4: Front-end operation in phase 2

In phase 2, the resonator is shorted to ground on one side with the excitation source powered down to save energy. On the other side, the resonator is shorted to the virtual

ground of the integrator which is in unity gain (Fig. 2-4). As a result, the initial transient current due to the parasitic capacitance (C_p) is dissipated.

- Phase 3: amplifying the ring-down current

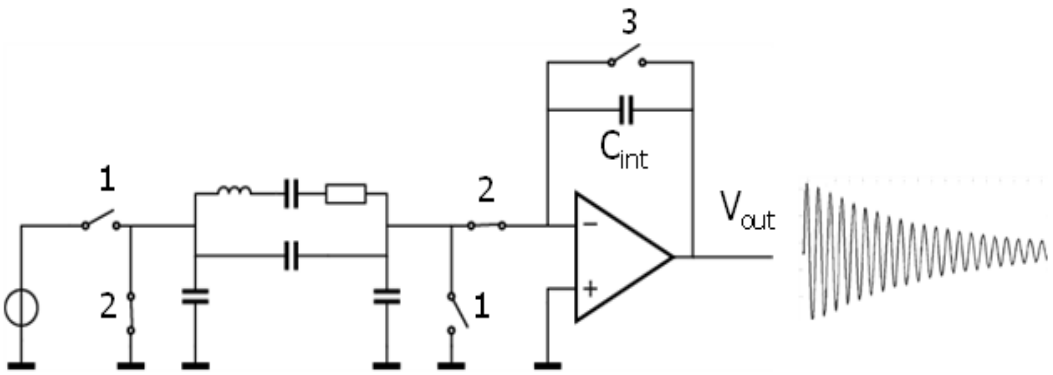

Fig. 2-5: Front-end operation in phase 3

Figure 2-5 depicts the last phase of the front-end operation. In this stage, switch 3 opens, and the ring-down current through the RLC tank gets integrated on the feedback capacitor (C_{int}). Thus, a ring-down voltage (V_{out} in Fig. 2-5) is generated at the output, from which zero-crossings can be detected by the comparator.

2.2.1.2 Output signal amplitude analysis

In this sub-section, an analysis of the output signal amplitude is presented. We assume the integrator amplifier has an infinite DC gain in the calculations.
Since the output signal is a ring-down voltage with exponentially decaying amplitude, we first determine the initial amplitude of the ring-down signal (A_0), from which the amplitude during the ring-down can then be easily calculated (section 2.3.2.1). In this report, signal amplitude refers to the initial ring-down amplitude (A_0).
The calculation of A_0 can be divided into three steps: calculation of the ring-down current through the RLC tank (i_{RLC}), calculation of the ring-down current through C_{int} (i_0) and calculation of A_0.

- Step 1: calculation of i_{RLC}

We assume that the driving frequency of the excitation source is exactly equal to the resonance frequency, which implies that the impedance of the RLC circuit is at minimum with a purely real value equal to R_m, because the impedance (reactance) of the inductor and capacitor are equivalent but of opposite sign and cancel out [4]. Hence, we have:

$$i_{RLC} = \frac{V_{dr}}{R_m} \qquad (2\text{-}3)$$

where V_{dr} is the amplitude of the driving source.

- Step 2: calculation of i_0

In order to calculate i_0, we model the integrator as a resistor with a value of $1/g_m$ (input impedance of the integrator), where g_m is the trans-conductance of the amplifier. Hence, we have the equivalent circuit (Fig. 2-6) shown below.

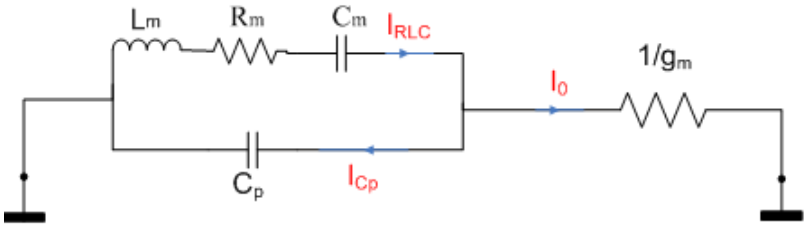

Fig. 2-6: Current divider model

From this equivalent circuit, we can see clearly that the ring-down current through the RLC tank divides into two paths: one path i_0 goes to the integrator, the other path i_{Cp} goes to the parasitic capacitor. Only i_0 contributes to the output signal, which can be calculated by:

$$i_0 = i_{RLC} \cdot \frac{g_m}{\sqrt{g_m^2 + (2 \cdot \pi \cdot f_{res} \cdot C_p)^2}} \qquad (2\text{-}4)$$

Equation 2-4 describes only the amplitude of the current, but there is also a phase shift associated to the current divider (section 2.3.3.2).
Combining with equation 2-3 results in:

$$i_0 = \frac{V_{dr}}{R_m} \cdot \frac{g_m}{\sqrt{g_m^2 + (2 \cdot \pi \cdot f_{res} \cdot C_p)^2}} \qquad (2\text{-}5)$$

- Step 3: calculation of A_0

i_0 gets integrated by the feedback capacitor (C_{int}), producing the output ring-down voltage. A_0 can be calculated by:

$$A_0 = \frac{i_0}{2 \cdot \pi \cdot f_{res} \cdot C_{int}} \qquad (2\text{-}6)$$

Substituting in equation 2-5, we obtain:

$$A_0 = \frac{V_{dr}}{2 \cdot \pi \cdot f_{res} \cdot C_{int} \cdot R_m} \cdot \frac{g_m}{\sqrt{g_m^2 + (2 \cdot \pi \cdot f_{res} \cdot C_p)^2}} \qquad (2\text{-}7)$$

2.2.2 Comparator operation

To determine the resonance frequency, the comparator is used for zero-crossing detection, with the reference voltage at zero level.
To determine the quality factor, the comparator is used for threshold-level detection, with the reference voltages at non-zero levels (section 2.2.3).
Hence, a programmable threshold voltage is applied to generate the reference levels using a multiplexer (chapter 4, section 4.2).

- Resonance frequency measurement: zero-crossing detection

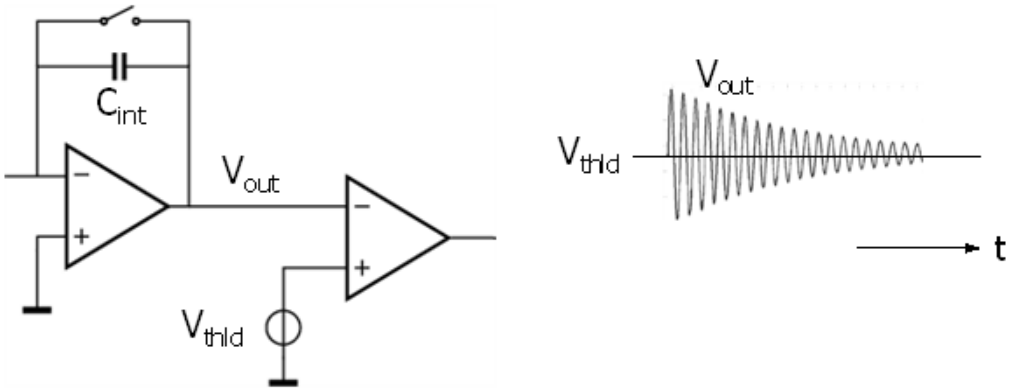

Fig. 2-7: Resonance frequency measurement

To measure the resonance frequency of the ring-down voltage (V_{out}), the reference voltage (V_{thld}) is set to zero (Fig. 2-7). The resonance frequency can then be calculated by the counting circuitry.

- Quality factor measurement: threshold-level detection

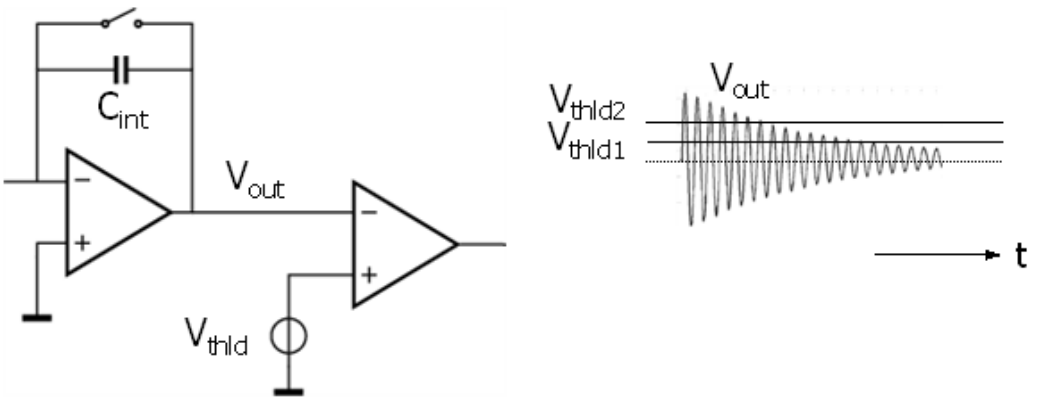

Fig. 2-8: Quality factor measurement

As depicted in Figure 2-8, the programmable reference voltage is set to two different non-zero values (V_{thld1} and V_{thld2}) when measuring the quality factor. Using the method

described in section 2.2.3, the quality factor can then also be calculated by the counting circuitry.

2.2.3 Counting Circuitry Operation

The counting circuitry is used to determine the resonance frequency (f_{res}) and quality factor (Q) of the resonator. The basic principle used here is the frequency counting technique [5] and threshold-crossing counting technique [6].

- Resonance frequency calculation

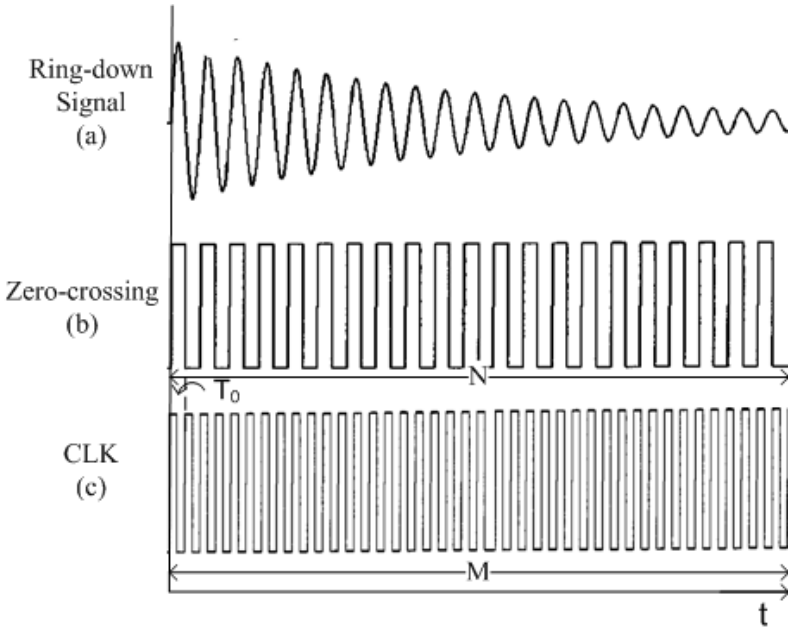

Fig. 2-9: Illustration of the frequency counting process for determining the resonance frequency. (a) Ring-down signal generated by the integrator. (b) The zero point crossings of the ring-down are converted to a square-wave. (c) Reference clock signal.

By counting the number of consecutive transitions across a given threshold point within a known measurement time, the frequency of an unknown signal can be determined. In order to calculate f_{res} of a ring-down signal (Fig. 2-9(a)), a reference clock (Fig. 2-9(c)), with a certain frequency f_0 is applied. Figure 2-9(b) shows a series of square-wave after zero-crossing detection. The resonance frequency can be calculated by:

$$f_{res} = \frac{N}{T} = \frac{N}{M \cdot T_0} \qquad (2\text{-}8)$$

where N is the number of ring-down cycles counted, T is the measurement time, which equals M clock cycles times the clock period T_0 ($T_0=1/f_0$).
The frequency determined by equation 2-8 is exact only when the measurement time (T) is an integer multiple of the signal period. When this is not the case, a quantization error will be introduced.

Equation 2-8 implies two methods to calculate f_{res} [5]:

- Method A: measure the number of clock ticks (M) for a specified number of zero-crossings (N), thus the error is within M and M+1 clock cycles.

- Method B: count N for a fixed time interval, as a result, the quantization error is smaller for large values of N.

The maximum number of ring-down cycles relates to Q and is thus on the order of a few hundred; hence, method B would result in a resolution that is too low. Thus, we choose method A for determining the resonance frequency of the resonator.

- Quality factor calculation

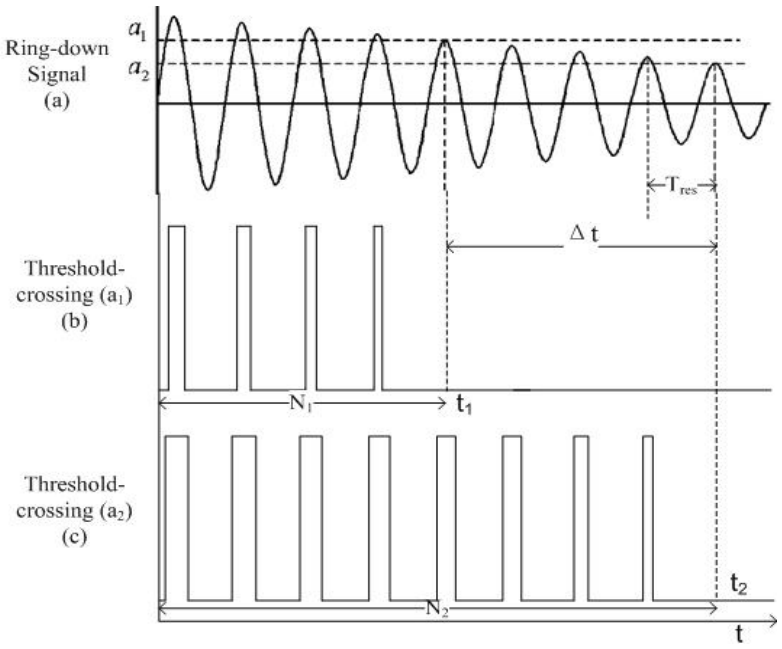

Fig. 2-10: Illustration of quality factor measurement by threshold-crossing counting. (a) Ring-down signal generated by the integrator. (b) The threshold-level (a_1) crossings of the ring-down are converted to a square-wave. (c) The threshold-level (a_2) crossings of the ring-down are converted to a square-wave.

Figure 2-10 illustrates the measurement of the quality factor. If we apply two threshold-levels, a_1 and a_2, to the exponentially decaying ring-down signal (Fig. 2-10(a)), two series of square-waves (Fig. 2-10(b) and (c)) are generated from the threshold-level comparisons. The number of cycles obtained by threshold-level a_1 is N_1, and the number of cycles obtained by a_2 is N_2. We can calculate the time t_1 and t_2 using the following approximations:

$$t_1 \approx N_1 \cdot T_{res} = \frac{N_1}{f_{res}} \qquad (2\text{-}9)$$

$$t_2 \approx N_2 \cdot T_{res} = \frac{N_2}{f_{res}} \qquad (2\text{-}10)$$

where the signal period $T_{res}=1/f_{res}$. Hence, we have:

$$\Delta t = t_2 - t_1 = (N_2 - N_1) \cdot T_{res} = \frac{N_2 - N_1}{f_{res}} \qquad (2\text{-}11)$$

According to [6], the damping factor is calculated by:

$$\zeta = \frac{\ln(a_1 / a_2)}{\Delta t \cdot 2 \cdot \pi \cdot f_{res}} \qquad (2\text{-}12)$$

Together with equation 2-11 and 1-4 (chapter 1, section 1.1.2), we obtain the quality factor by:

$$Q = \frac{\pi \cdot \Delta N}{\ln(a_1 / a_2)} \qquad (2\text{-}13)$$

2.3 Error analysis

In this section, non-idealities which affect the detection limits are discussed in four aspects: quantization error, thermal noise, offset and comparator delay.

2.3.1 Quantization error

We take the resonance frequency as an example to analyze the effect of quantization error. From the introduction of the frequency counting technique (see section 2.2.3) , we know that in the time interval of N ring-down cycles, there could be M or M+1 clock ticks (M>>1), thus resulting in a frequency uncertainty δf_{res} :

$$\delta f_{res} = \frac{N}{M \cdot T_0} - \frac{N}{(M+1) \cdot T_0} = \frac{f_{res}}{M+1} \approx \frac{f_{res}}{M} = {f_{res}}^2 \cdot \frac{T_0}{N} \qquad (2\text{-}14)$$

Using $f_0=1/T_0$ and dividing by f_{res} on both sides, we have an equation for the detection limit:

$$\frac{\delta f_{res}}{f_{res}} = \frac{f_{res}}{N \cdot f_0} \qquad (2\text{-}15)$$

Equation 2-15 implies that for a fixed number N, higher clock frequency (f_0) results less quantization error.
The choice of N is limited by the quality factor of the ring-down. There is a trade-off here:

- When N is large, the ring-down amplitude becomes too small to be detected at the end of the time interval.
- When N is small, a higher clock frequency f_0 is required to maintain the requirement for the detection limit (Eq. 2-15).

In this report, we choose N=Q=300 as a compromise. Hence, for a resonance frequency around 2MHz, to achieve the required detection limit of 10^{-4}, a minimum value for the clock frequency is 67MHz.

2.3.2 Thermal Noise

To analyze thermal noise, we start with an introduction of timing jitter. Together with the output amplitude analysis (section 2.2.1.2), a requirement for signal-to-noise ratio (SNR) is then derived to achieve the detection limit. In the end, a trans-conductance requirement for the amplifier (consider only SNR) is derived.

2.3.2.1 Timing jitter

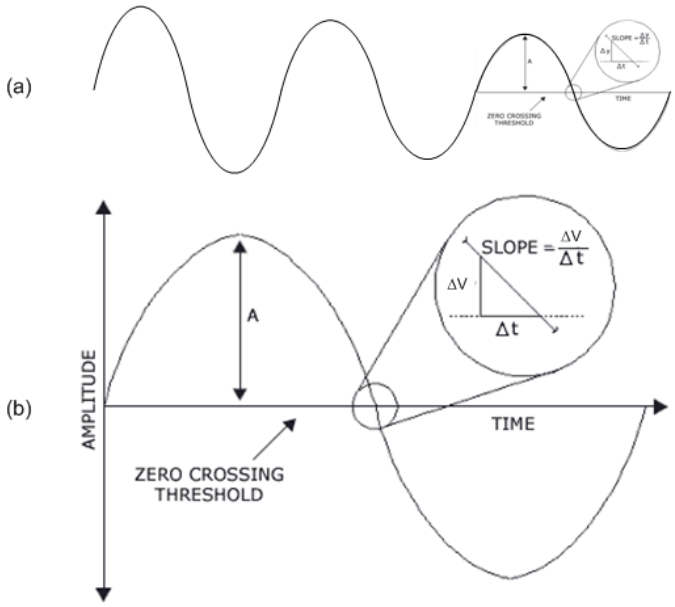

Fig. 2-11: Cause of timing jitter. (a) Output ring-down signal. (b) Zoom-in view of the last ring-down cycle.

Figure 2-11 demonstrates the cause of timing jitter: noise voltage (ΔV in Fig. 2-11) at the input of the comparator causes the ring-down signal to reach the threshold voltage Δt earlier or later, thus producing timing jitter [7].
The ring-down voltage is a sine-wave with exponentially decaying amplitude (Fig. 2-11(a)). Mathematically, we can represent this sinusoid (Fig. 2-11(b)) with the following equation:

$$V = A(t) \cdot \sin(2 \cdot \pi \cdot f_{res} \cdot t) \quad (2\text{-}16)$$

where $A(t)$ is the ring-down amplitude, which can be written as:

$$A(t) = A_0 \cdot e^{-\alpha \cdot t} \quad (2\text{-}17)$$

where α is the attenuation parameter, which can be expressed in terms of the quality factor:

$$\alpha = \frac{\omega}{2 \cdot Q} = \frac{2 \cdot \pi \cdot f_{res}}{2 \cdot Q} \quad (2\text{-}18)$$

where ω is the angular frequency: $\omega = 2\pi f_{res}$.
The derivative of equation 2-16 shows the slope of the sine-wave at its zero crossings:

$$\frac{\Delta V}{\Delta t} = 2 \cdot \pi \cdot f_{res} \cdot A(t) \quad (2\text{-}19)$$

Substituting the RMS noise voltage ($V_{n,RMS}$) for ΔV, we get the expression for the RMS timing jitter (Δt) in terms of the signal amplitude ($A(t)$) and the RMS noise voltage:

$$\Delta t = \frac{V_{n,RMS}}{2 \cdot \pi \cdot f_{res} \cdot A(t)} \quad (2\text{-}20)$$

Combining with equation 2-17 and 2-18 results in:

$$A(t) = A_0 \cdot e^{-\left(\frac{2 \cdot \pi \cdot f_{res}}{2 \cdot Q}\right)} \quad (2\text{-}21)$$

In the ring-down signal, each zero crossing produces timing jitter, but only the timing jitter corresponding to the last zero crossing in the measurement time (see section 2.2.3) is relevant. This is because the measurement time (T) is determined by the last zero-crossing; while the other N-1 ring-down cycles are always counted as one cycle. The time when the last sine-wave occurs is:

$$t = \frac{N}{f_{res}} \quad (2\text{-}22)$$

Together with equation 2-21 and the assumption $N = Q$, we now have:

$$A(t) = A_0 \cdot e^{-\pi} \quad (2\text{-}23)$$

Substituting into equation 2-20, we obtain the equation for the timing jitter:

$$\Delta t = \frac{V_{n,RMS}}{2 \cdot \pi \cdot f \cdot A_0 \cdot e^{-\pi}} \quad (2\text{-}24)$$

2.3.2.2 Signal-to-noise ratio requirement

We use $A_0/V_{n,RMS}$ (the initial ring-down amplitude divided by the RMS thermal noise voltage at the input of the comparator), to represent the signal-to-noise ratio (SNR).
To calculate the design requirement for SNR, we need to translate noise and signal amplitude into a resulting frequency detection limit. The relative detection limit of the resonance frequency, which equals the uncertainty in the measured frequency divided by the resonance frequency, can be interpreted in the time domain: RMS timing jitter (Δt) divided by measurement time (T):

$$\frac{\delta f_{res}}{f_{res}} \approx \frac{\Delta t}{T} \qquad (2\text{-}25)$$

where $T = N/f_{res}$ (from Eq. 2-8).
Combining with equation 2-24 results in:

$$\frac{\delta f_{res}}{f_{res}} \approx \frac{\Delta t}{T} = \frac{V_{n,RMS}}{2 \cdot \pi \cdot N \cdot A_0 \cdot e^{-\pi}} \qquad (2\text{-}26)$$

Equation 2-26 describes that for a given N, the resonance frequency detection limit defines a SNR requirement. If we again apply Q=N=300, we obtain the design requirement for signal-to- noise ratio: $A_0 / V_{n,RMS}$ >130.

2.3.2.3 Trans-conductance requirement

In order to understand in detail how thermal noise affects the detection limit, and derive the resulting requirement for the trans-conductance (g_m) of the amplifier, we have done some analysis to derive the equations for detection limit based on SNR consideration (Appendix A). All the calculations assume the amplifier has infinite DC gain.
The thermal noise for a MOSFET can be modeled by a current source in parallel with the channel. The noise currents of the input device can be represented by an equivalent noise voltage source at its gate terminal, with a power spectral density (PSD) of $(8/3)kT/g_m$ [8]. If we assume the amplifier has a differential pair as its input, thus, the input thermal noise may be represented by a single equivalent noise voltage source at the gate with a PSD of $(16/3)kT/g_m$.
For clarity, we rewrite the final equations here:

$$\frac{\delta f_{res}}{f_{res}} = \frac{f_{res} \cdot R_m \cdot \sqrt{\frac{4 \cdot k \cdot T \cdot C_p \cdot C_{\text{int}}}{3 \cdot (C_{AZ} + C_{\text{int}})}} \cdot \sqrt{(\frac{2 \cdot \pi \cdot f_{res} \cdot C_p}{g_m})^2 + 1}}{N \cdot e^{-\pi} \cdot V_{dr}} \qquad (2\text{-}27)$$

where g_m represents the trans-conductance of the input device of the amplifier, C_{int} is the feedback capacitance, and C_{AZ} represents the auto-zeroing capacitor (section 2.3.3.3, load capacitance of the integrator).

Equation 2-27 provides the requirement for detection limit. With the parameters given in section 2.1, the minimum value needed for g_m is around 12μS to achieve the required detection limit (Eq. 2-1).
We also derived the equation of detection limit in terms of the resonator parameters:

$$\frac{\delta f_{res}}{f_{res}} = \frac{R_m^{\,2} \cdot \sqrt{\frac{4 \cdot k \cdot T \cdot C_p \cdot C_{\text{int}}}{3 \cdot (C_{AZ} + C_{\text{int}})}} \cdot \sqrt{(\frac{2 \cdot \pi \cdot f_{res} \cdot C_p}{g_m})^2 + 1}}{2 \cdot \pi \cdot L_m \cdot e^{-\pi} \cdot V_{dr}} \qquad (2\text{-}28)$$

Equation 2-28 shows that the detection limit is proportional to R_m^2, which supports our choice to use the higher-order resonance mode with the smaller R_m (section 2.1).

2.3.3 Offset

To calculate the resonance frequency, the comparator detects the zero-crossings of the ring-down signal, but the results hold accurate only when the ring-down dies out at 0V level. We refer to the steady-state voltage level at which the (ring-down) signal rings down completely as the output DC level. If there are issues like: remaining charge on C_p in phase 3, or mismatch between f_{res} and f_{dr} (see section 2.3.3.2), the output DC level will no longer remain at 0V, thus an offset occurs.

2.3.3.1 Consequences of offset

There are two errors due to offset:

- Fewer ring-down cycles and increased measurement errors.

In frequency counting, zero-crossing detection is applied. With an offset in the output ring-down signal, the effective threshold level is not zero anymore.

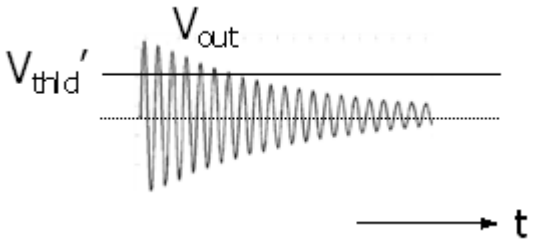

Fig. 2-12: Ring-down signal with offset

In figure 2-12, V_{out} is the ring-down signal at the output of the integrator, V_{thld}' represents the effective threshold voltage in the presence of offset. With offset, fewer signal cycles can be detected due to the decaying amplitude. Furthermore, the time interval of N signal cycles with offset is bigger or smaller than the ideal case, depending on the direction of the offset. The resulting error in the measurement time (T) gives rise to an error in the final result (Eq. 2-8).

- Smaller output swing.

The maximum swing of the ring-down signal is limited by the supply power of the integrator. If the offset is too big, the output amplitude might exceed the maximum swing; hence, clipping occurs. So, offset reduces the available output swing, and thus the maximum initial amplitude (A_0) of the ring-down signal.

2.3.3.2 Offset sources

There are mainly three offset sources, assuming the offset of the amplifier and that of the comparator negligible:

- Initial transient current through C_p

The initial transient current through C_p, as a result of energizing the resonator in phase 1, would appear as an offset at the output after integration. This issue is solved by the way we operate the front-end circuit (section 2.2.1.1), as long as phase 2, during which the charge on C_p is dissipated, is sufficiently long. Charge remaining on C_p after phase 2 will still give rise to offset.

- Mismatch between f_{res} and f_{dr}

As described in phase 3 of front-end operation (section 2.2.1.1), when switch 3 opens, the ring-down current through the RLC tank gets integrated on the feedback capacitor (C_{int}). Thus, a ring-down voltage (V_{out}) is generated at the output. The switching moment of switch 3 plays an important role in the offset analysis. Here, we give two examples of extreme cases (Fig. 2-13 and 2-14). In both figures below, the ring-down signal in the left represents the ring-down current that flows into the integrator, and the ring-down signal in the right represents the output voltage after integration.

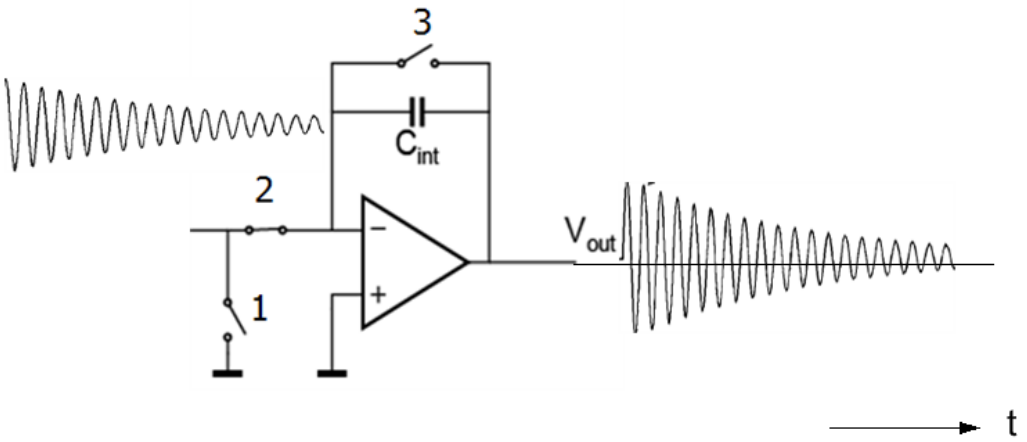

Fig. 2-13: Switch 3 opens at peak of the ring-down current

In figure 2-13, switch 3 opens at the peak of the ring-down current, after integration, a 90 degree phase shift shows up at the output due to the feedback capacitor; as a result, the output starts to ring down at zero level. In this situation, no offset occurs.

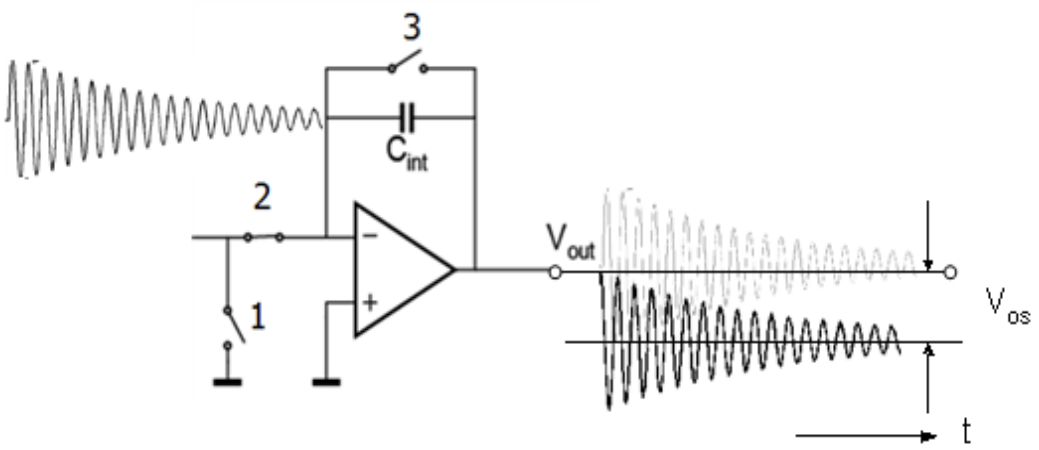

Fig. 2-14: Switch 3 opens at zero level of the ring-down current

Figure 2-14 depicts the situation when switch 3 opens at zero level of the ring-down current. Hence, the output starts to ring down at the peak, resulting in an offset (V_{os} in Fig. 2-14). In this case, we have the maximum offset due to this reason, which equals the ring-down amplitude (A_0).
From the above analysis, we know that to avoid offset, switch 3 should open at the peak of the ring-down current. This can be implemented only when the driving frequency (f_{dr}) is equal to the resonance frequency (f_{res}). Since the resonance frequency is not known a priori; hence, the mismatch between f_{res} and f_{dr} will inevitably introduce offset.

- Finite trans-conductance g_m of the integrator.

The ring-down current through the RLC tank (i_{RLC}) divides into two paths: one path i_0 goes to the integrator, the other path i_{Cp} goes to the parasitic capacitor (Fig. 2-6). i_0 gets integrated and becomes output voltage. This current divider model brings two effects: loss of amplitude (see section 2.2.1.2) and a phase shift. The phase shift due to C_p results in offset at the output.
With some simple calculations of the current divider model (Fig. 2-6), we derive the phase shift (φ) of i_0:

$$\varphi = \text{atan}\left(\frac{2\cdot\pi\cdot f_{res}\cdot C_p}{g_m}\right) \quad (2\text{-}29)$$

The phase shift is between 0 degree to 90 degree, and reduces with an increasing g_m. Hence, to make sure the majority (80%) of the ring-down current goes to the integrator:

$$i_0 \geq 80\% \cdot i_{RLC} \quad (2\text{-}30)$$

and the phase shift is less than 15 degree:

$$\varphi < 15° \quad (2\text{-}31)$$

substituted by equation 2-4 and 2-29, thus we derive a minimum value (requirement) for g_m is 300µS. With this g_m, the signal-to-noise requirement is also met (section 2.3.2.2).

2.3.3.3 Offset Compensation

We implement auto-zeroing to compensate this offset issue. There are two steps involved:

- First auto-zeroing step.

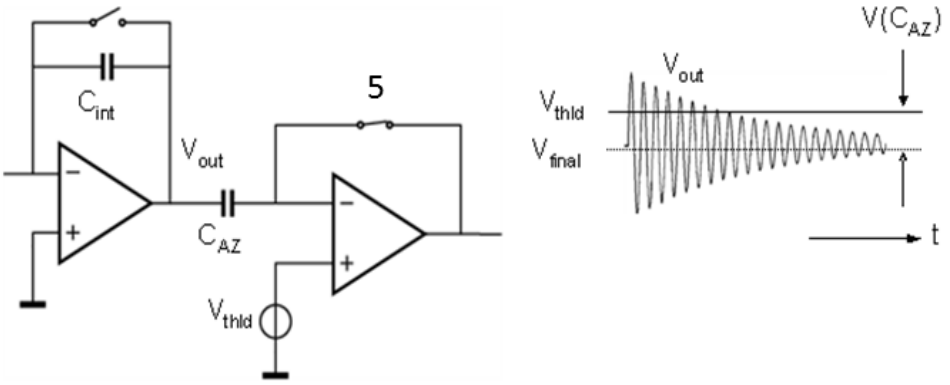

Fig. 2-15: First step of offset compensation

In this step, the comparator is configured as unity-gain buffer (Fig. 2-15). If the operation described in section 2.2.1 is applied, we obtain a ring-down voltage (V_{out}) at the output of the integrator. V_{final} is the output DC level when V_{out} rings down completely. Hence, the voltage difference (V_{final}-V_{thld}) is sampled on the auto-zeroing capacitor C_{AZ}.

- Second measurement step

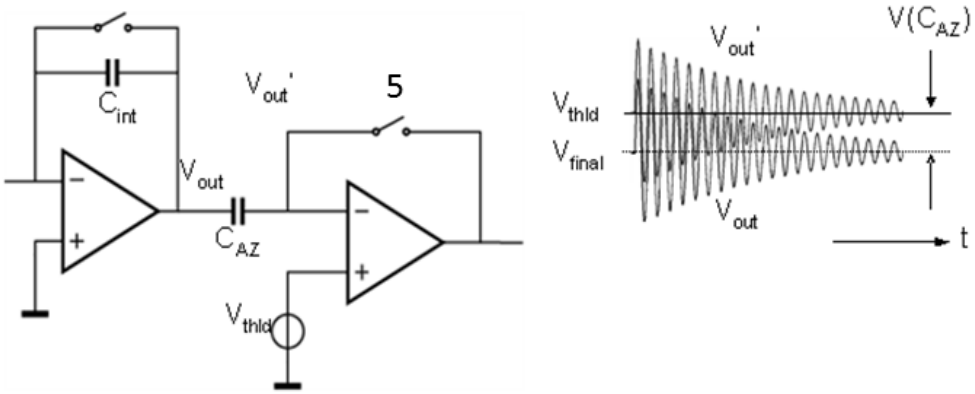

Fig. 2-16: Second step of offset compensation

In the figure 2-16, V_{out}' is the ring-down voltage after auto-zeroing, compared with the ring-down voltage with offset V_{out}.
In this step, the comparator operates as a regular comparator. We repeat the operation in step one, V_{out} rings down for the second time, the voltage difference stored on C_{AZ} level-shifts V_{out} to V_{out}', brings V_{final} to V_{thld} and thus cancels the offset error.
Compare these two steps, the auto-zeroing capacitor (C_{AZ}) and the unity gain buffer are both loading the integrator in the first step, while only C_{AZ} is loading the integrator during the second measurement. Hence, in order to keep the integrator in the same situation (output load) during the integration phase, we close the auto-zeroing switch (switch 5) only at the final moment of the first measurement step (Fig. 2-15) and then open it before the second measurement (Fig. 2-16) starts to keep the charge sampled on C_{AZ}.
To conclude, in order to detect the resonance frequency and quality factor with offset compensation, there are four excitation & ring-down steps:

- One auto-zeroing step to eliminate offset errors
- One zero-crossing step to determine f_{res}
- Two non-zero level-crossing steps to determine Q

2.3.4 Comparator delay time

Another non-ideality which affects the detection limit is the comparator delay. A delay in the comparator causes an error in the measurement time (T). This resulting error gives rise to an error in final result.
The comparator is used as a level detector in terms of signal amplitude. The key design parameter is the propagation delay (Δt_d). As long as the first and last ring-down cycles experience the same delay, no error occurs in the measurement time. Since the propagation delay typically depends on the overdrive applied to the input of the comparator [9], with exponentially decaying amplitude of the ring-down voltage, we have different delay time for the first and last cycle. We assume the delay of the first cycle is much smaller than of the last cycle due to a larger overdrive; hence, the delay time corresponding to the last sine-wave matters.
Similar to the analysis of SNR (see section 2.3.2.2), after some calculations, we obtain:

$$\frac{\delta f_{res}}{f_{res}} \approx \frac{\Delta t_d}{T} = \frac{\Delta t_d \cdot f_{res}}{N} \qquad (2\text{-}32)$$

Equation 2-32 shows how comparator delay time affects the detection limit. Again, if we apply N = 300, we obtain a minimum value for Δt_d:

$$\Delta t_d = 15ns \qquad (2\text{-}33)$$

2.4 Simulation results

To do the architecture-level simulation, we use a voltage-controlled-current-source (vccs) with a trans-conductance of 300µS as an ideal OTA; and a voltage-controlled-voltage-source (vcvs) with a high voltage gain and a 3.3V output voltage range as an ideal comparator. We apply a sine-wave with 200mV amplitude, and 1.977MHz frequency as the excitation source. All the switches are ideal, with the control signals shown in figure 2-17.

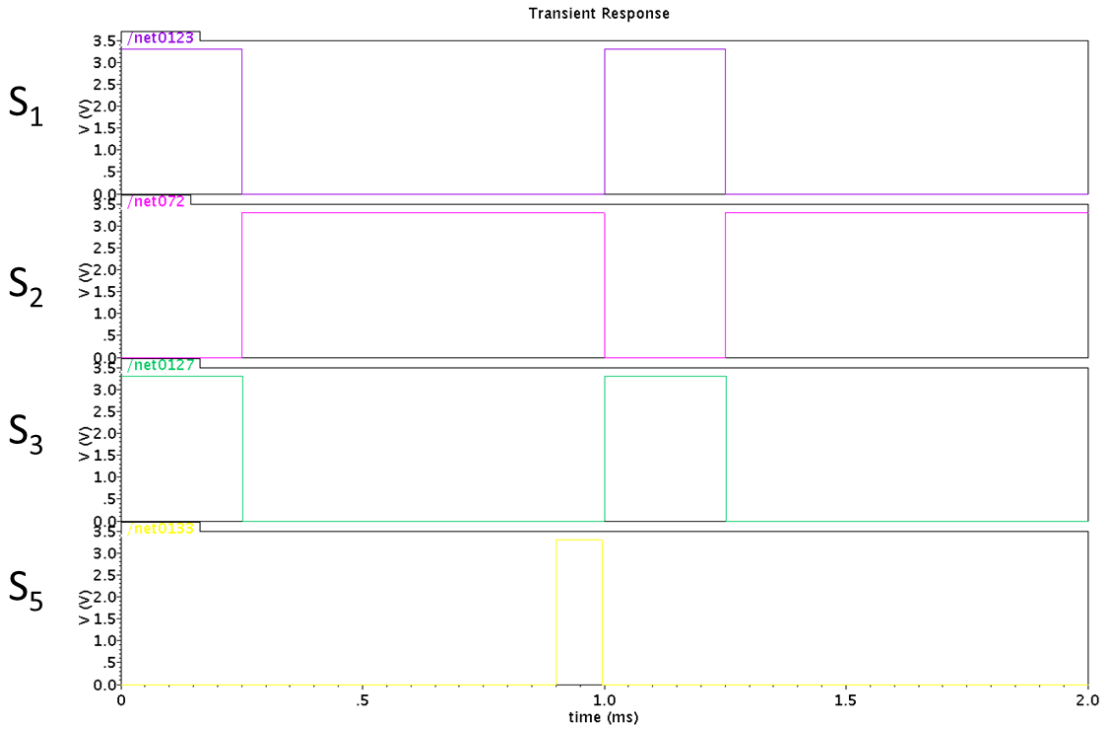

Fig 2-17: Timing of the control signals

The simulation results are demonstrated in figure 2-18. In the excitation phase, the resonator is energized by the driving signal (Fig 2-18(a)). While in the integration phase, the ring-down signal is generated (Fig 2-18(b)); and the comparator starts to detect the zero-crossings, producing square waves at the output (Fig 2-18(c)). Figure 2-18(b) plots the signals at the output of the integrator and at the input of the comparator after auto-zeroing, which explains the offset compensation (see section 2.3.3.3) .

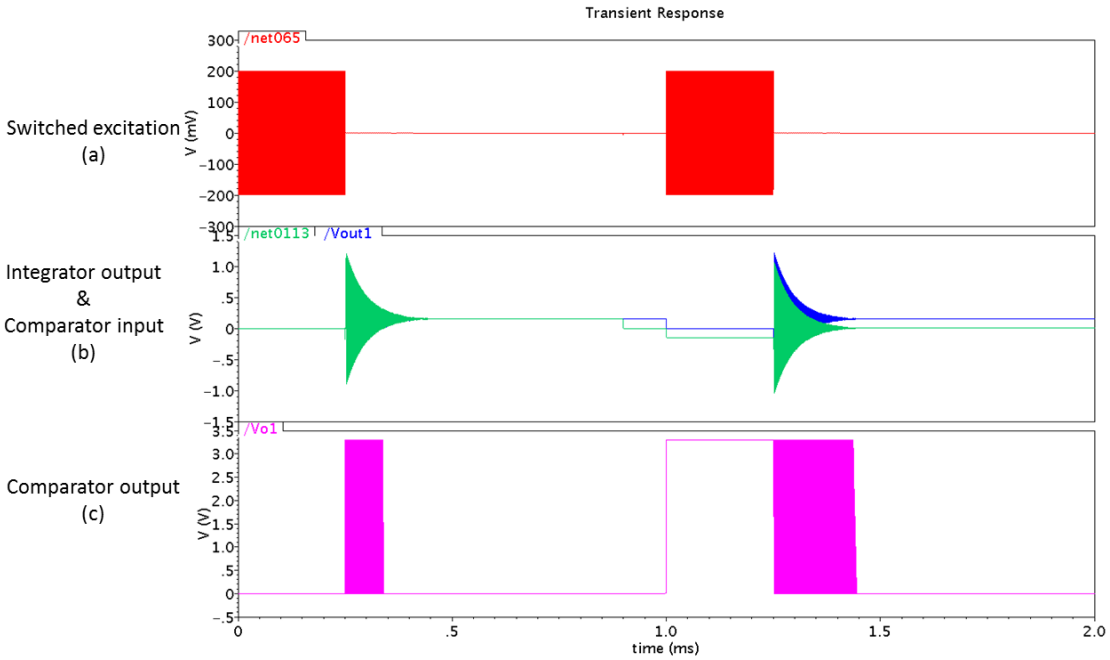

Fig 2-18: Simulation results

2.5 Conclusion

In this chapter, the architecture-level analysis and design of the read-out circuit have been presented. A motivation for using a higher-order resonance mode (with small resistance and large quality factor) rather than the fundamental mode has been presented. The operating principles of the front-end circuit, the comparator and the frequency counting circuit have been introduced. To arrive at the requirements for the detection limits, the major error sources have been analyzed, including quantization error, signal amplitude together with thermal noise, offset and comparator delay.
To conclude, our design requirement for trans-conductance g_m is 300μS, considering signal amplitude, thermal noise and offset. The delay time of the comparator is 15ns.

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Chapter 3

Circuit-level Analysis and Design

In this chapter, circuit-level analysis and design of the interface circuit are presented mainly in three parts: front-end circuit, auto-zeroed comparator and simulation results. After that, a brief introduction to the digital design is given , with a conclusion in the end.

3.1 Front-end design

We divide the front-end circuit design into several sub-sections: the integrator, switches , feedback capacitor and the output buffer.

3.1.1 A single transistor

We start with the integrator (main part) design. The integrator converts the small ring-down current produced by the resonator into a readable output ring-down voltage. Initially, we use ideal switches and an ideal biasing circuit. To make energy consumption as low as possible, we try to design the integrator as simple as possible by starting with a single transistor (Fig. 3-1).

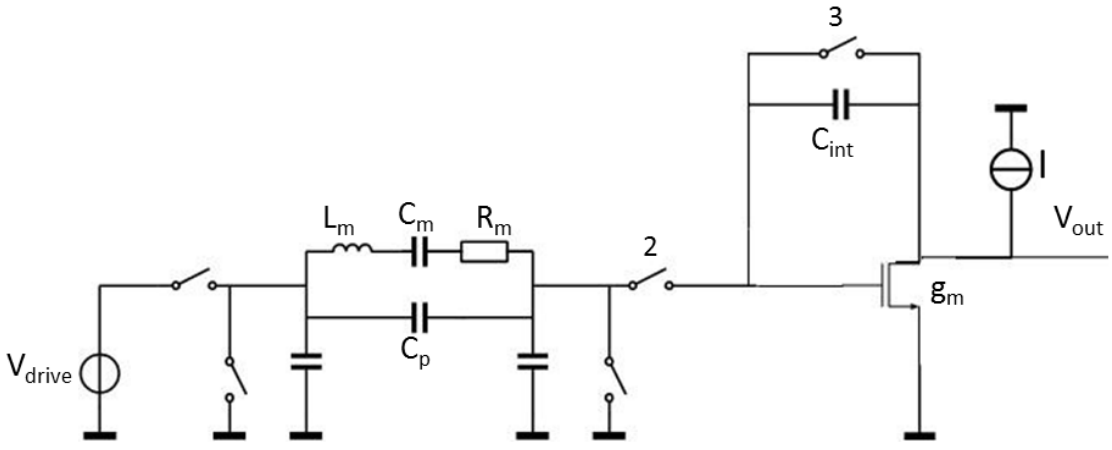

Fig. 3-1: Front-end circuit with a single transistor

To simulate the above configuration (Fig. 3-1), we use the resonator parameters (L_m, C_m, R_m and C_p) from chapter two (section 2.1). To make a power-efficient interface circuit, we design this single transistor to work in weak-inversion mode with a highest possible trans-conductance-to-current ratio: g_m/I_D=20. Thus, we derive our supply current (I in Fig. 3-1) of 15µA to achieve the g_m requirement (g_m=300µS, chapter 2, section 2.3.3.2). We apply a sine-wave (V_{drive} in Fig. 3-1) with 200mV amplitude, and 1.977MHz frequency as the excitation source.
Since there is no offset compensation in figure 3-1, we simulate only one excitation & ring-down step, within the time of 1ms.
The output signal (V_{out}) is the ring-down voltage with offset. The simulation results are shown in figure 3-2.

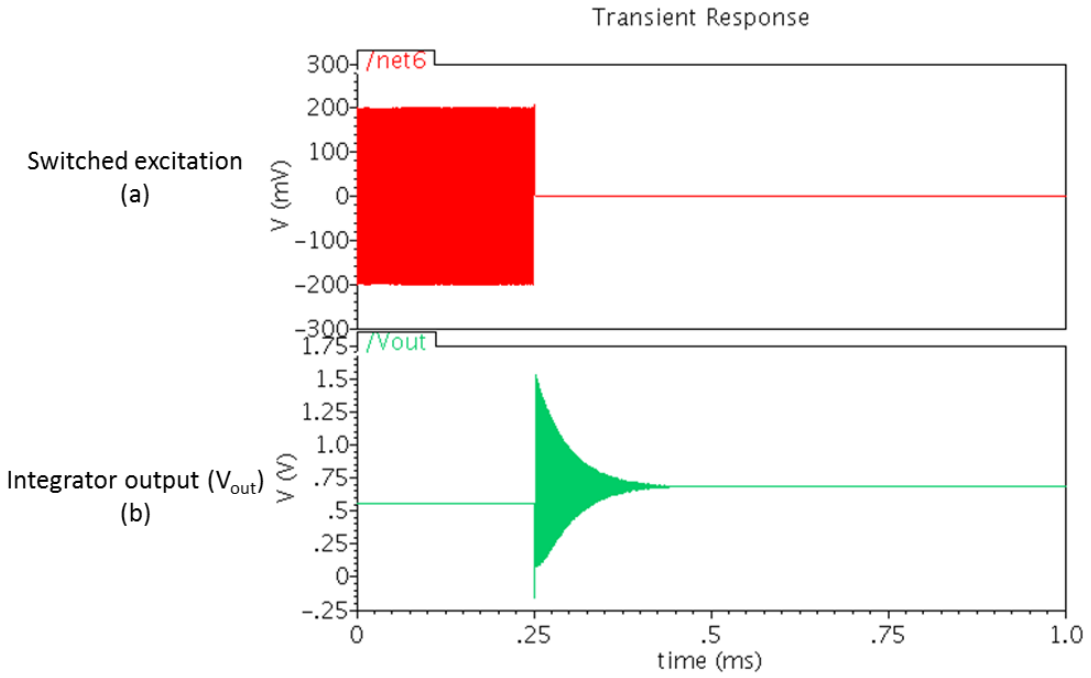

Fig. 3-2: Simulation results for a single transistor amplifier

In the excitation phase, switch 3 is closed (chapter 2, section 2.2.1.1), which diode-connects the transistor. The current source (I) defines the biasing of the transistor with a gate-source voltage of around 0.55V, which can be seen at the initial part of the output signal (Fig. 3-2 (b)). At the moment when switch 2 closes, the voltage at the right side of the resonator changes from 0V to 0.55V, which explains the voltage step at 0.25ms (Fig. 3-2 (b)). Then, during the integration phase, the ring-down signal is generated. The ring-down amplitude here is around 0.8V; while the circuit provides less than 0.55V output swing in the negative direction. As a result, clipping might happen at the negative side of the ring-down signal, depending on the direction of the offset. Figure 3-2 shows the situation when clipping occurs.

3.1.2 Cascode amplifier

To solve the above-mentioned problem (clipping), we have two solutions:

- Reduce the output signal amplitude
- Enlarge the output headroom of the circuit

Reducing the signal swing implies that a smaller thermal noise level is required to keep the SNR requirement (chapter 2, section 2.3.2.2); hence, more power might be needed for the noise reduction. Also, the ring-down output might be not readable if the amplitude is too small. As a result, to enlarge the output headroom is a better idea. With the 3.3V supply, we would like to have an output DC level at 1.65V to obtain the best output swing in both directions. Thus, we add a cascode configuration to increase the output DC level (Fig. 3-3).

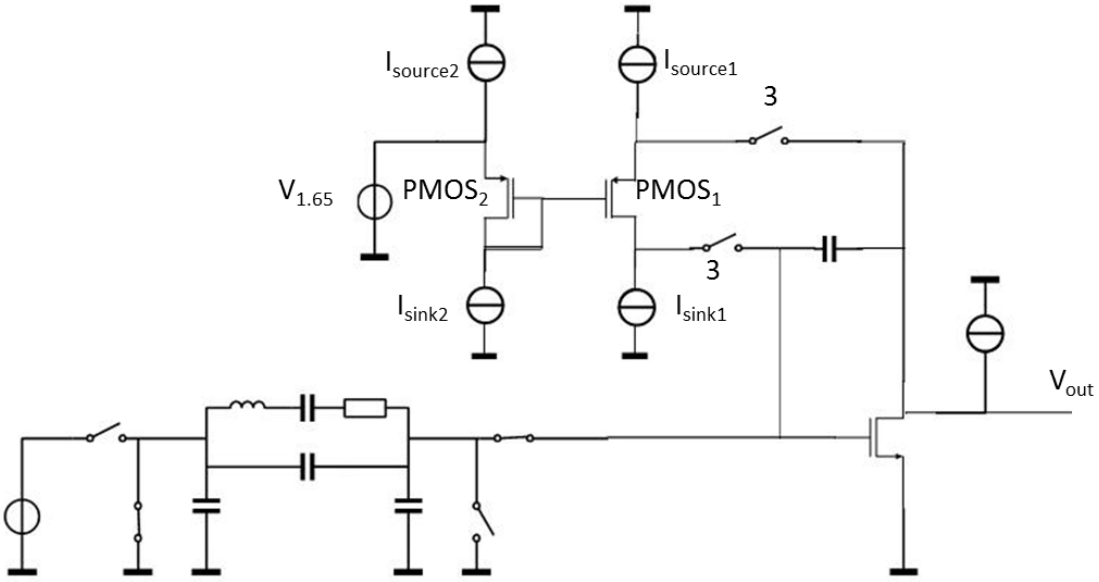

Fig. 3-3: Front-end circuit with a cascode configuration

Two PMOS transistors (with the same size) are added here: $PMOS_1$ and $PMOS_2$. When switches 3 closes, the output DC level is defined by the gate voltage of $PMOS_1$ plus the gate-source voltage of $PMOS_1$. The mirrored $PMOS_2$ transistor is connected to an external voltage supply ($V_{1.65}$) at the source. The bias-current sources of these two transistors have the same value which makes the output DC level equals to $V_{1.65}$. As a result, we can control the output DC level externally.
During the integration phase, switches 3 opens (chapter 2, Fig. 2-5), disconnecting the cascode circuit from the integrator. Hence, the bias-current sources ($I_{source1}$, I_{sink1}, $I_{source2}$, I_{sink2}) of the PMOS transistors can be switched off in the integration phase to save energy. We design these PMOS transistors to have the same trans-conductance-to-current ratio: g_m/I_D=20, as the main NMOS; but the supply current is three times less (5µA) to save energy.

We do the simulation under the same conditions (section 3.1.1). The simulation results are demonstrated in figure 3-4.

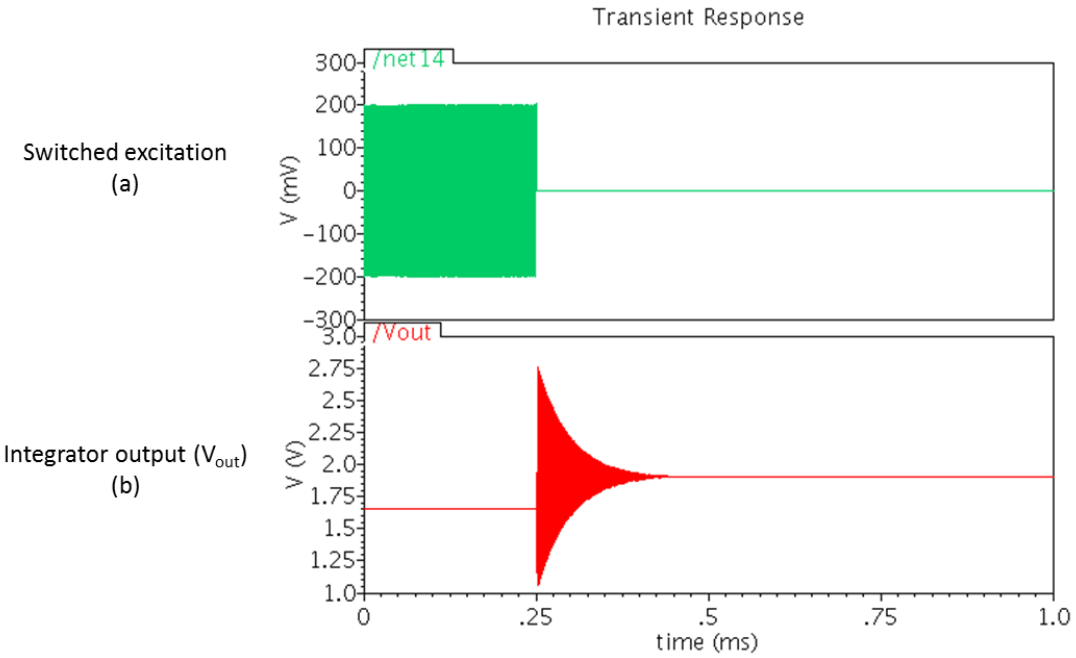

Fig. 3-4: Simulation results with cascode configuration

The integrator output (Fig. 3-4(b)) stays at 1.65V initially during the excitation phase; the output DC level might differ from 1.65V level depending on the offset issue (chapter 2, section 2.3.3). By applying cascode amplifier, we have a bigger output swing to avoid clipping.

3.1.3 Switchable feedback capacitors

So far, the integrator circuit is implemented with a fixed feedback capacitor. In order to make our circuit to operate with different devices and resonance modes, we design the feedback path with three switchable capacitors with different values in parallel (Fig.3-5). From [1], we know the resistance of the resonators ranges from 12kΩ to 2MΩ. Hence, to obtain a readable output ring-down voltage ($1V_{p-p}$ or so) with the excitation amplitude up to 200mV, we choose the following values for the integration capacitors (chapter 2, Eq. 2-7):

- C_{int1} = 150fF
- C_{int2} = 300fF
- C_{int3} = 600fF

Therefore, we have eight combinations of feedback capacitance, from 150fF to 950fF.

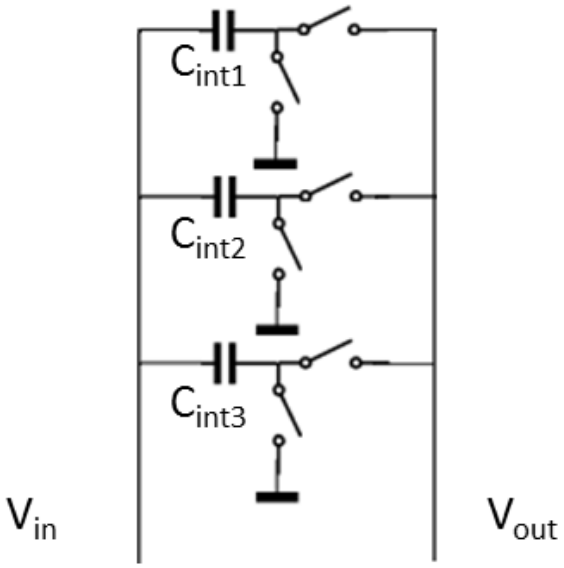

Fig. 3-5: Switchable feedback capacitors

We use two switches with complementary control signals to select the capacitor of each path. We implement the switches at the output (V_{out} in Fig. 3-5) side of the integrator. Hence, when the capacitors are not selected, they load the input node (V_{in}) of the integrator; which further adds to the big C_p (chapter 1, Fig. 1-2), without changing the output capacitance (bandwidth).

3.1.4 Switches

So far, we assumed ideal switches with infinite off-resistance (no leakage); however, there is always some leakage current flowing through a switch due to the finite off-resistance, particularly at higher temperatures.
During the integration phase, any DC leakage path through the integrator capacitor (C_{int}) will cause a droop (offset) at the ring-down output.
Similar to the analysis of timing jitter (chapter 2, section 2.3.2.1): an offset voltage (ΔV_{out}) causes the ring-down signal to reach the threshold voltage Δt earlier or later, thus producing error (chapter 2, Fig. 2-11); together with equation 2-19 and 2-33 (requirement for Δt), we derive that: to achieve the required detection limit, the maximum acceptable output offset is about 4mV (for a $1V_{p-p}$ ring-down output).
The output offset (ΔV_{out}) and the DC leakage current (I_{leak}) are linked by equation 3-1:

$$\Delta V_{out} = \frac{1}{C_{int}} \cdot \int_0^t i(\tau) d\tau \quad (3\text{-}1)$$

With a feedback capacitance of 250fF (chapter2, section 2.1) and a measurement time of 1ms (t = 1ms), we conclude that to keep the output offset up to 4mV, the maximum leakage current is:

$$I_{leak} = 1pA \quad (3\text{-}2)$$

Figure 3-6 depicts the front-end circuit (with switchable feedback capacitors) during the integration phase.

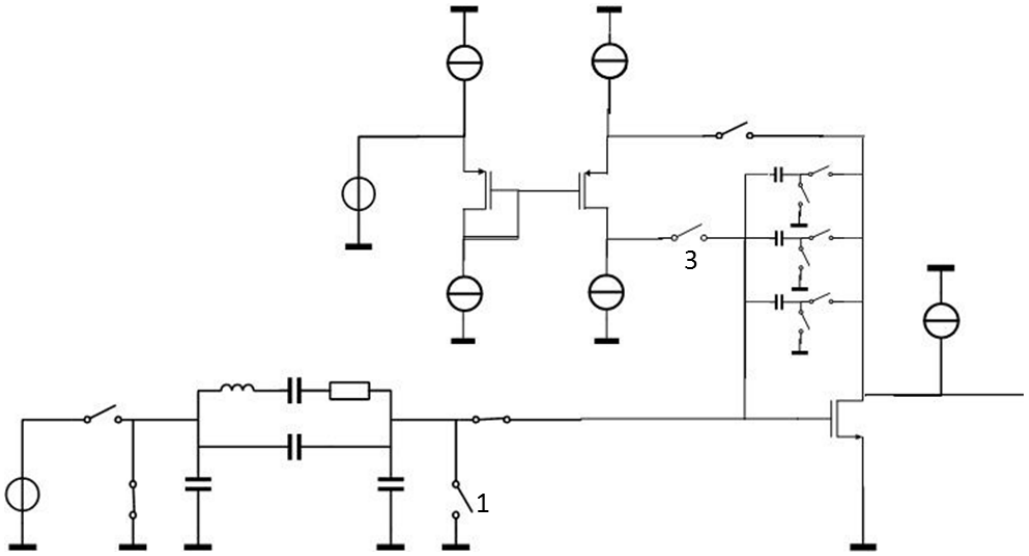

Fig. 3-6: Front-end circuit during the integration phase

Switch 1 and 3 (shown in Fig. 3-6) are tuned off ,and connected to the input of the integrator; hence, any voltage difference across these two switches would introduce a leakage current due to their finite off-resistance. For instance, the voltage across switch 1 is about 0.55V; together with a typically few gigaohm off-resistance gives a leakage of few nanoamp.

To meet the requirement (equation 3-2), we implement switch 1 and 3 in such a way (Fig. 3-7) to solve this leakage problem.

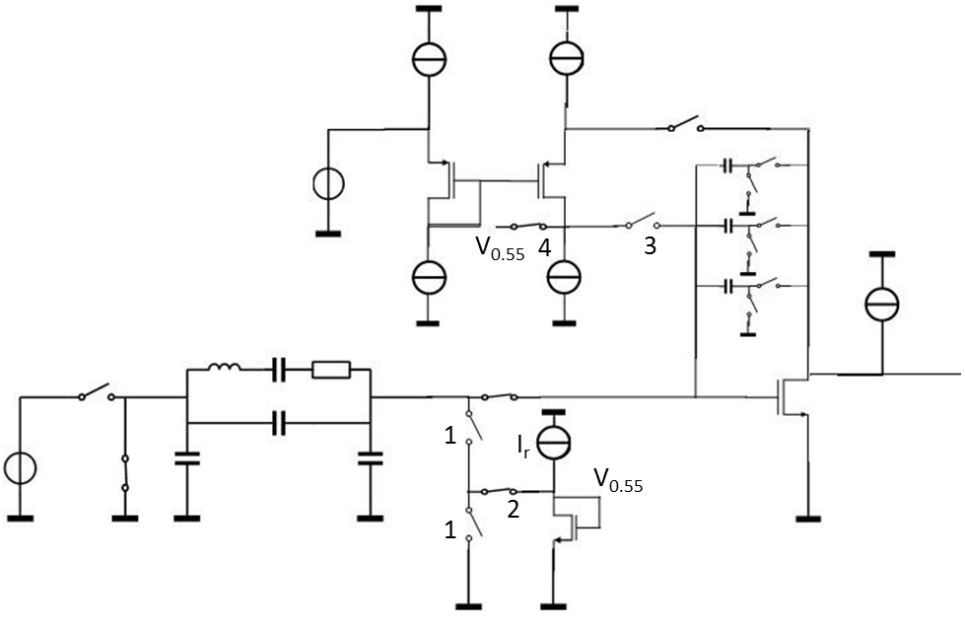

Fig. 3-7: Low leakage front-end circuit implementation

We generate a voltage source ($V_{0.55}$) to replicate the gate-source voltage of the main NMOS. Some additional switches are applied: switch 2 is complementary to switch 1; switch 4 is complementary to switch 3 (Fig. 3-7). The implementation of the replica voltage sources ($V_{0.55}$), together with complementary switches, make the voltage across swich1 and 3 become zero; hence reduce the leakage current.
To generate this replica voltage ($V_{0.55}$), we apply a diode connected NMOS transistor with a W/L proportional to the main NMOS transistor (15 times less). In the meantime, to obtain the same current density, the supply current (I_r) is also 15 times less, with a value of 1μA.

3.1.5 Source follower

In order to read-out the ring-down signal in our measurement, we use an I/O pad at the integrator output. With this large (several picofarad) pad capacitance loading the integrator, the resultant reduced bandwidth would affect the performance of the front-end circuit. Hence, we use a output buffer (source follower) at the output. To make our circuit flexible, we apply two complementary switches to select this buffer stage (Fig. 3-8).

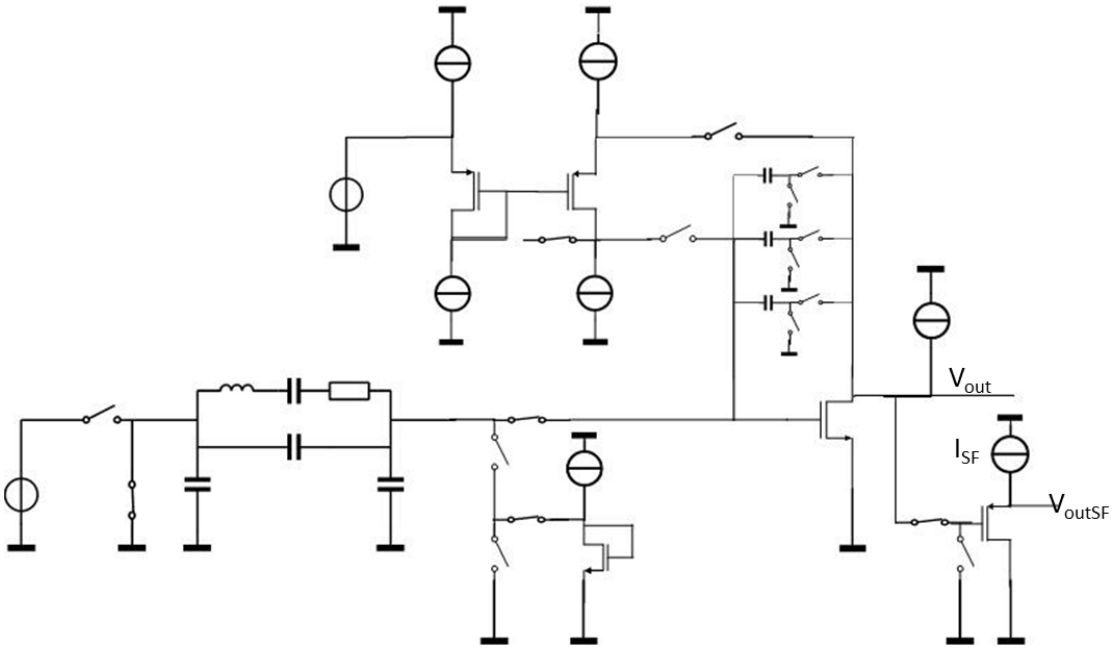

Fig. 3-8: Front-end circuit with source follower read-out

Since the voltage gain of the source follower is a bit less than one, we have the read-out signal (V_{outSF}) amplitude smaller than V_{out}. The supply of this PMOS source follower (I_{SF}) is applied off-chip (tunable), which is able to provide big headroom for the level-shifted ring-down output.

3.2 Auto-zeroed comparator design

As we described in chapter two (section 2.3.4), the main design requirement of the comparator is the delay time. The propagation delay of the last ring-down cycle should be smaller than 15ns (for a minimum overdrive).
For a first approach design, we choose a two-stage comparator with a preamp and a gain stage (Fig. 3-9) for simplicity.

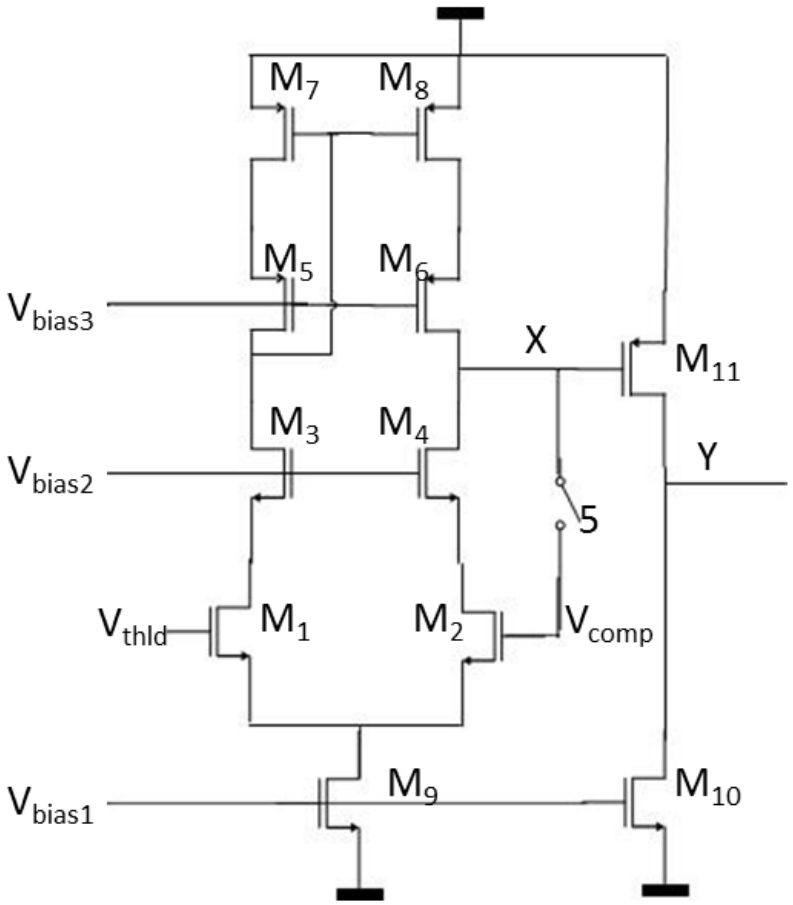

Fig. 3-9: Two-stage auto-zeroed comparator circuit

For a two-stage, open-loop comparator, the propagation delay is limited by either the bandwidth or the slew rate [2]. The open-loop comparator (Fig. 3-9) is loading an inverter-bank (several stages of inverters, to drive the large pad capacitance); hence, the output capacitance (C_Y) can be estimated by input capacitance of the inverter, together with $C_{DB10,}$ C_{DB11} and the miller capacitance of $C_{GD10,}$ $C_{GD11,}$ with a value of few tens of femtofarad. As a results, the small output capacitance, together with a big supply current (I_{10} =9µA) result a big slew rate (I_{10}/C_Y). Thus, the propagation delay is limited by the bandwidth.
The two-stage, open-loop comparator circuit (Fig. 3-9) mainly has two poles: $\omega_{p,X}$, at the output of the first stage (X) and $\omega_{p,Y}$, at the output of the second stage (Y).

- $\omega_{p,X} = (R_X \cdot C_X)^{-1}$, $R_X = (g_{m4} \cdot r_{O2} \cdot r_{O4}) // (g_{m6} \cdot r_{O6} \cdot r_{O8})$ and C_X is the total capacitance at node X to ground (C_{GS11}, C_{DB4}, C_{DB6}), with a value of few tens of femtofarad.

- $\omega_{p,Y} = (R_Y \cdot C_Y)^{-1}$, $R_Y = r_{O10} // r_{O11}$ and C_Y is the total capacitance at node Y to ground (C_{DB10}, C_{DB11}, C_{GD10}, C_{GD11}), with a value of few tens of femtofarad.

Here, we ignore the non-dominate poles introduced by the cascade stage (far away from origin). Hence, the pole at node X is the dominate one due to the large impedance (R_X), which determines the bandwidth. To design the comparator with high bandwidth, we dimension transistors M_3~M_5 with short width to push $\omega_{p,X}$ away from origin. We use longer devices for M_1 and M_2 to obtain sufficient gain.
For a ring-down signal with a 1V initial amplitude, the amplitude reduces to 40mV after 300 (N) cycles. By properly sizing the transistors, we can obtain a delay less than 12ns with a 40mV overdrive. To achieve this performance, we applied 11μA current for each branch of the first stage and 9 μA current for the second stage.
As described in section 2.3.3.3, we implement an auto-zeroing capacitor C_{AZ} (chapter 2, Fig. 2-15) and switch 5 (Fig. 3-9) to compensate the offset. Since we choose the two-stage amplifier without compensation, hence, stability of the comparator need to be ensured during the first auto-zeroing step; as a result, we only put the first stage in unity-gain. The offset introduced by the second stage is attenuated by the high gain of the first stage, which can be ignored.
The ring-down signal generated by the front-end circuit is attenuated by the factor $C_{AZ}/(C_{AZ} + C_{in})$, where $C_{in} = C_{GS2}$, is the input capacitance of the comparator. In order to reduce this signal attenuation and the charge-injection offset ($Q/(C_{AZ} + C_{in})$), we choose C_{AZ} much larger than C_{in}. Since the value of input capacitance is few tens of femtofarad, we make our design choice:

$$C_{AZ} = 300fF \quad (3\text{-}3)$$

The threshold-level (V_{thld}) will be generated off-chip (see section 4.2).

3.3 Simulation results

3.3.1 Simulation test bench

To simulate the circuit-level design, we use the excitation source with the same amplitude and frequency (200mV, 1.977MHz). In order to have a big ring-down amplitude for our resonator (with 126kΩ resistance) , we choose 150fF feedback capacitance in the simulation.
We set the output DC level ($V_{1.65}$) at 1.65V; the threshold-level (V_{thld}) is also 1.65V to detect the resonance frequency.
The control signals remain the same (chapter 2, Fig. 2-17). We add switch 4 due to the leakage issue (see section 3.1.4). Figure 3-10 plots all the control signals, with a total measurement time of 2ms.

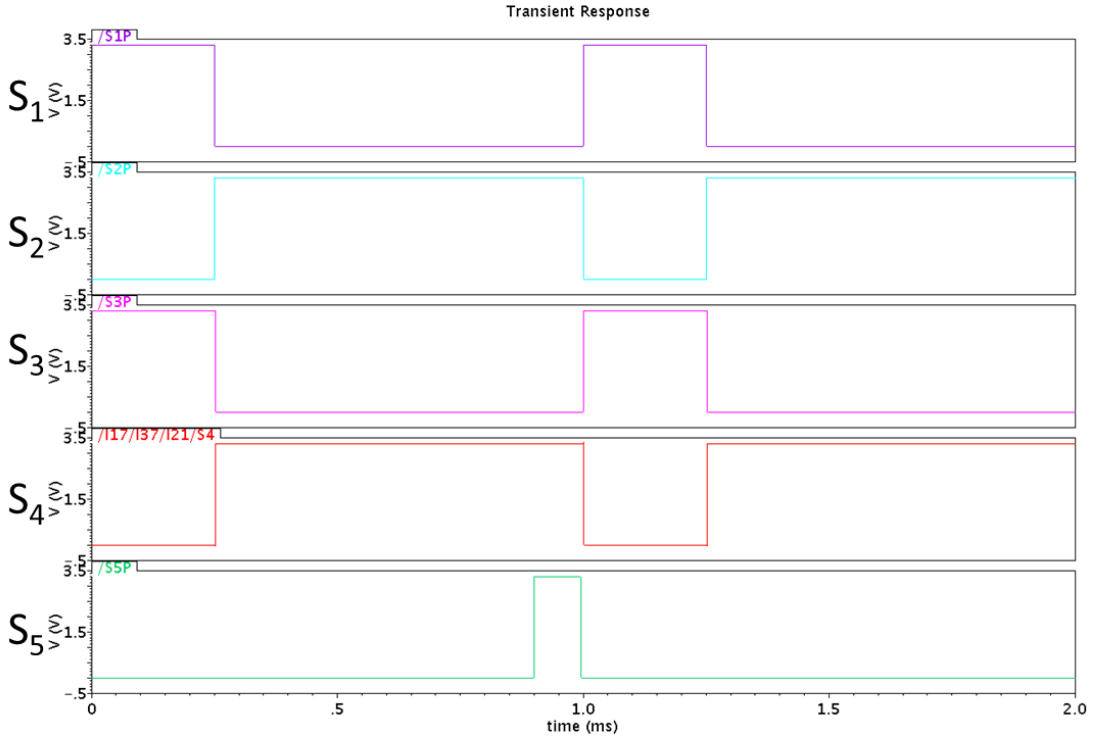

Fig. 3-10: Timing of the control signals

The simulation results are demonstrated in figure 3-11: the switched driving signal with 200mV amplitude and 1.977MHz frequency (Fig. 3-11(a)), the ring-down signal at the output of the integrator (Fig. 3-11(b)), and the comparator output signal for frequency counting (Fig. 3-11(c)).

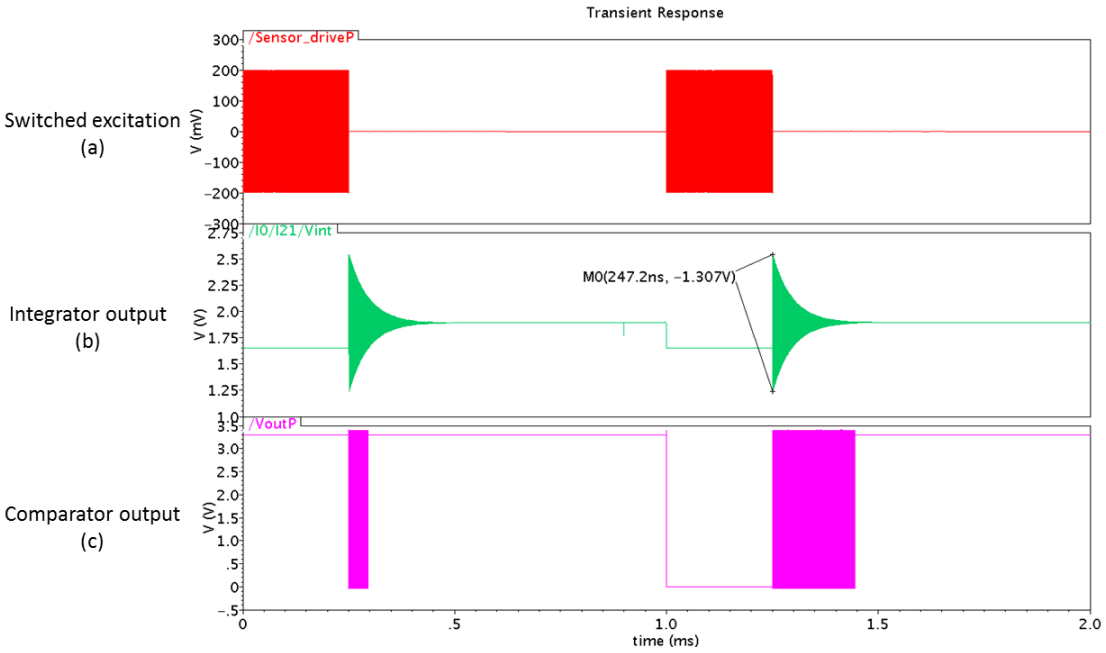

Fig. 3-11: Simulation results

During the first measurement step (1ms), the comparator detects few ring-down cycles (Fig. 3-11(c)) due to the offset issue (chapter 2, section 2.3.3). After auto-zeroing, we obtain useful comparison results in the second measurement, from which the frequency counting can be done to calculate the resonance frequency (f_{res}).

3.3.2 Ring-down amplitude

We point out the peak-to-peak difference of the first ring-down cycle (Fig. 3-11(b)), which shows that the ring-down amplitude ($A_{0(p\text{-}p)}$) is around 1.31V.
In the simulation, we choose capacitor C_{int1} (150fF) as the feedback capacitance; hence, the other capacitors ($C_{int2,}$ C_{int3}) load the input node (V_{in} in Fig. 3-5) of the integrator which further adds to the big C_p (section 3.1.3). As a result, the equivalent C_p has a value of its original value (5.5pF) plus the value of C_{int2} (300fF) and C_{int1} (600fF), plus the parasitic from the input node to ground.
Hence, we can calculate the ring-down amplitude by equation 2-7 (chapter 2, section 2.2.1.2). With all the parameters listed below:

- V_{dr} = 0.2V
- f_{res} = 1.977MHz
- C_{int} = 150fF
- R_m = 126kOhm
- C_p = 6.5pF
- g_m=300uS

we obtain the peak-to-peak ring-down amplitude:

$$A_{0(p-p)} = 1.35V \quad (3\text{-}4)$$

This value is a bit bigger than what we get in the simulation. The reasons are:

- We assume the amplifier has an infinite DC gain in equation 2-7, which is not true in our actual amplifier design.
- The energy stored in the resonator gets lost a bit in operation phase 2 (dissipating the charge on C_p) before the ring-down output generated (chapter 2, section 2.2.1.1).

3.3.3 Noise

In this section, we check the thermal noise. The NMOS of the integrator is the majority noise source. To simulate the thermal noise, we apply ac & noise simulation of the equivalent AC circuit (Fig. 3-12).

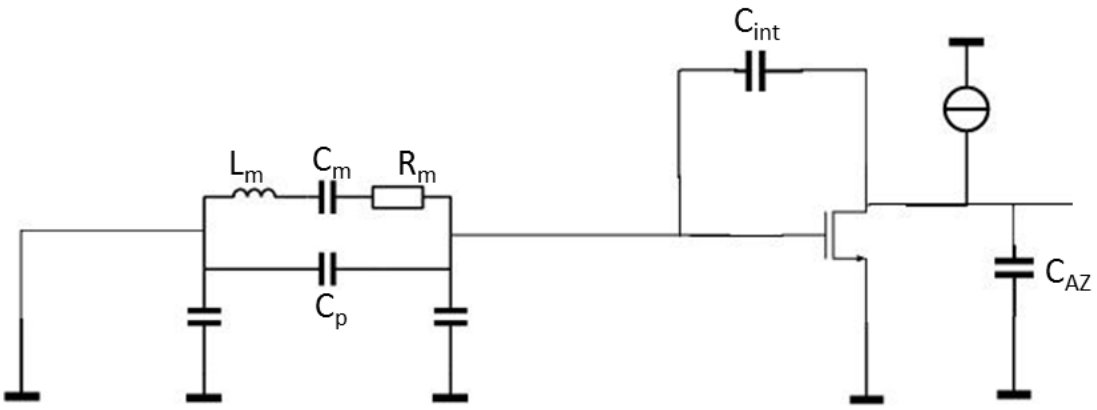

Fig. 3-12: AC equivalent circuit for noise simulation

Figure 3-13 demonstrates the RMS noise value integrated over 110MHz (bandwidth: estimated by g_m/C_0, Appendix A).

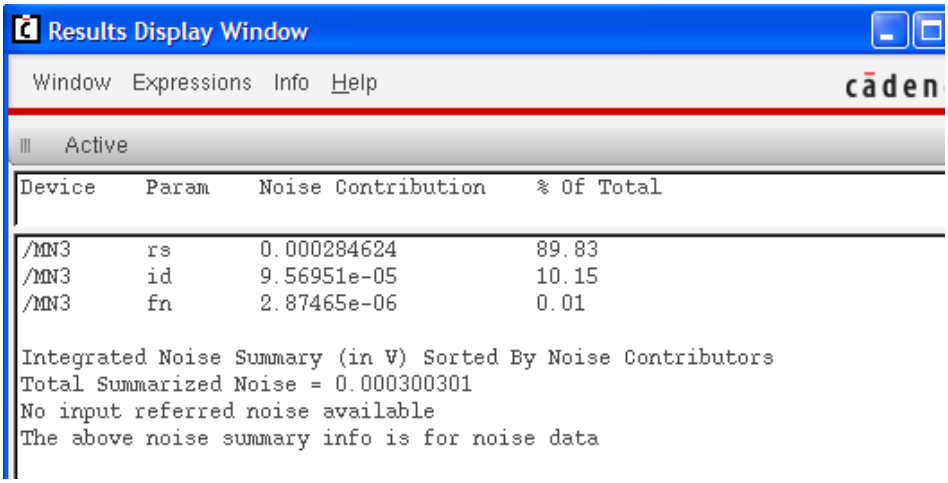

Fig. 3-13: Thermal noise simulation results

The output referred RMS noise is about 3×10^{-4} V.
The analysis of thermal noise is in appendix A, we re-write the equation (8) (appendix A) here:

$$V_{n,RMS} = \sqrt{\frac{4 \cdot k \cdot T \cdot C_p}{3 \cdot C_{int} \cdot (C_{int} + C_{AZ})}} \quad (3\text{-}5)$$

With the following parameters:

- C_{int} = 150fF

- C_{AZ} = 300fF
- C_p = 5.5pF

We derive the expected RMS noise is 6.6×10^{-4} V. To achieve equation (3-5), we assume the amplifier has a differential pair as its input; we use a single transistor for the amplifier in fact, hence, we have the RMS noise in half:

$$V_{n,RMS} = 3.3 \times 10^{-4}\ V \quad (3\text{-}6)$$

This value is a bit bigger than what we get from the simulation results. This is because: to derive equation (3-5), we assume the amplifier has an infinite DC gain, hence, the DC gain of the integrator (Appendix A, Fig. A1) is :

$$G_0 = \frac{1}{\beta+1/A} = \frac{1}{\beta} \quad (3\text{-}7)$$

where β is the feedback factor, and A is the DC gain of the amplifier.
While in reality, the finite DC gain (A) of the amplifier causes $G_0 < 1/\beta$; hence, the affected transfer function brings the smaller RMS noise in the simulation.

3.3.4 Offset

As we described, the offset is cancelled by auto-zero technique. To check the offset compensation, we plot the signals at both sides of the auto-zeroing capacitor (C_{AZ}).

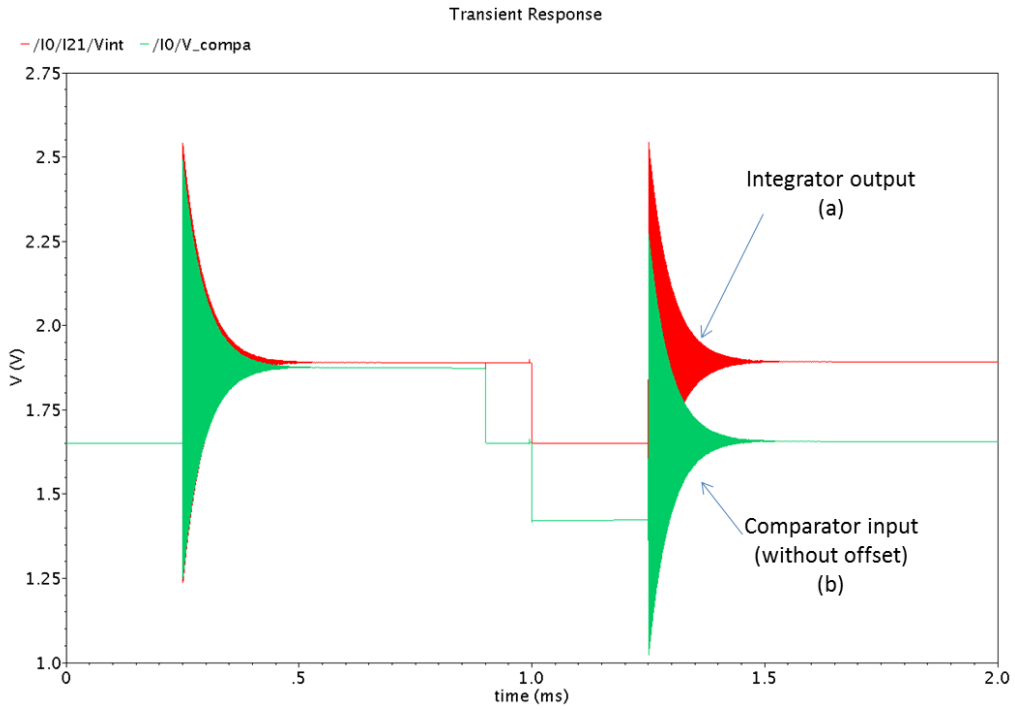

Fig. 3-14: Simulation results of offset cancellation

Figure 3-14(a) refers to the output signal of the integrator, while Figure 3-14(b) represents the input signal of the comparator. The figure depicts that the offset voltage is hold on C_{AZ} at the end of the first measurement and level-shifts the ring-down signal to 1.65V output DC-level during the second measurement.

3.3.5 Energy consumption

We summarize the energy consumption in table 3-1:

Table 3-1: Energy consumption in simulation

Components	Supply voltage	Supply current	Time	Energy consumption
Integrator	3.3V	19µA	2ms	125.4nJ
Cascode circuit	3.3V	10µA	0.25ms × 2	16.5nJ
Comparator	3.3V	36µA	1.1ms	130.68nJ

The cascode circuit is powered on only during the excitation phase (see section 3.1.2), with a total time of around 0.5ms; and the comparator is powered on only from the auto-zeroing phase (at the end of the first measurement). Hence, we have the total energy consumption of 272nJ per measurement.
If we check the ring-down signals (Fig. 3-11(b)), the signal rings down till its steady stage at about 0.5ms. Thus, we can make the measurement time shorter to save energy. If we apply a measurement time of 0.5ms, we have the total energy consumption reduced to half of its original value (136nJ per measurement).

3.4 Digital design

The digital part mainly has three functions:

1. Control signals generation:
   - Control signals for switch 1,2,3,4 and 5 (see section 3.3.1)
   - Control signal to select the source follower (see section 3.1.5)
   - Control signal to select the cascode circuit supply (see section 3.1.2)
   - Control signals to select the feedback capacitance (see section 3.1.3)
2. Excitation signal generation:

Generate a squire-wave with an amplitude of 3.3V and a frequency close to the resonance frequency

3. Counting circuitry operation to calculate f_{res} and Q

Figure 3-15 depicts the block diagram of FPGA implementation to calculate the resonance frequency (including control signals and excitation signal generation).

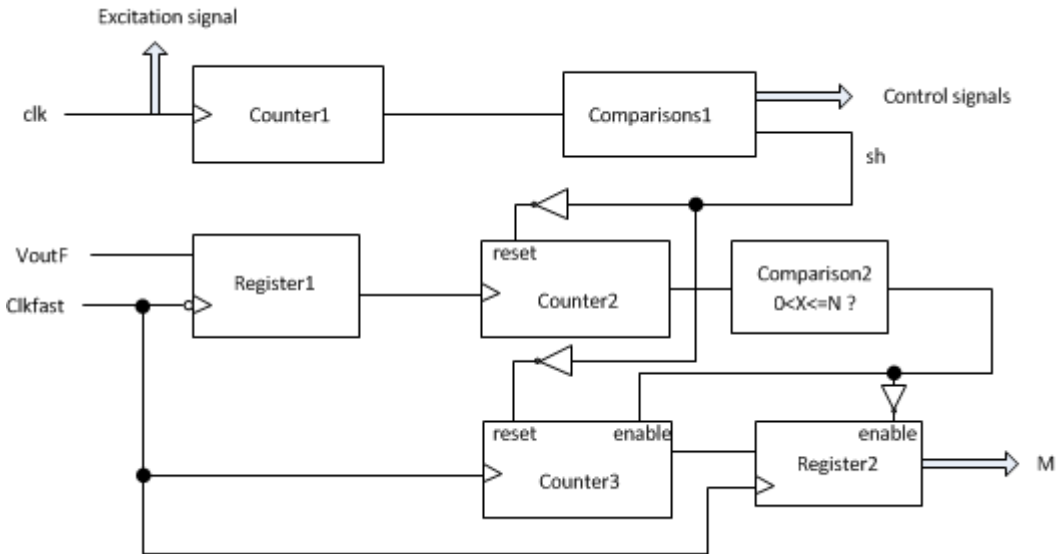

Fig. 3-15: Block diagram of f_{res} detection (all signals are active high)

'clk' is an external clock generated by a function generator, with a frequency close to the resonance frequency; 'Clkfast' represents a fast clock (50MHz) produced by the FPGA development board; 'VoutF' is the output square-wave used for counting. 'Counter2' counts the output until N cycles (chapter 2, Fig. 2-9); while in the meantime, 'Counter3' counts the fast clock (reference clock f_0). Both counters are reset by signal 'sh', which is active in the second measurement. The final output is the cycles of reference clock M. Thus, the resonance frequency can be calculated by equation 2-8, with T_0=20ns.
The verilog code of f_{res} can be found in Appendix B.
Figure 3-16 depicts the block diagram of FPGA implementation to calculate the quality factor (including control signals and excitation signal generation).

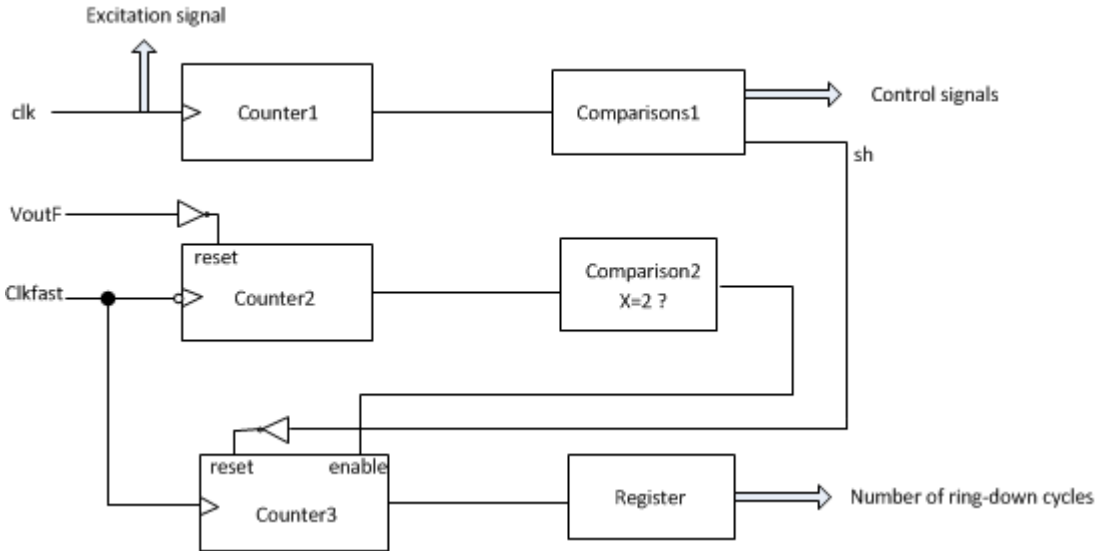

Fig. 3-16: Block diagram of *Q* detection (all signals are active high)

With a certain threshold-level, we need to calculate the total number of ring-down cycles. 'Counter3' counts the ring-down cycles, while 'Counter2' and 'Comparison2' are implemented to avoid multiple transitions: only when 'VoutF' remains high for at least two cycles of 'Clkfast', we consider that we have a valid pulse at the output. We apply negative-edge of 'Clkfast' to trigger 'Counter2' is to make sure a steady enable of 'Counter3' when it is triggered.
The verilog code of f_{res} can be found in Appendix C.

3.5 Conclusions

In this chapter, we have introduced the circuit-level analysis and design of the interface circuit. In the front-end circuit design, we have mainly discussed the integrator implementation using a single NMOS transistor, the approach to bias the integrator's output such that the headroom is maximized, the measures taken to minimize leakage in the switches, the programmable feedback capacitors, and the output buffer. For the auto-zeroed comparator, we use a simple two-stage configuration (bandwidth limited) to obtain a propagation delay of 12ns. Furthermore, we have analyzed the simulation results in several aspects: ring-down amplitude, thermal noise and offset. Also, the digital design has been briefly introduced. Finally, we have calculated the total energy consumption of 272nJ (which can be further reduced to 136nJ by applying shorter measurement time).

References

[1] D. M. Karabacak, Private Communication.

[2] P.E.Allen, "Open-loop comparators", lecture note, lecture 310.
http://www.aicdesign.org/SCNOTES/2010notes/Lect2UP310_%28100328%29.pdf

Chapter 4

Measurement Results

In this chapter, measurement results of the ring-down based resonant sensor interface chip are presented. First, the fabricated chip and the measurement setup, including the circuit layout, test board design and measurement equipment are introduced. After that, we present measurement results obtained using both conventional impedance measurements, and the ring-down technique. In the end, conclusions of the measurement are presented.

4.1 Fabricated chip

4.1.1 Circuit layout

A good analog layout plays a vital role in extracting the maximum performance from an analog circuit. To improve the performance of the interface circuit, the simplest way is to make a better layout. Figure 4-1 shows the chip layout without pad ring.

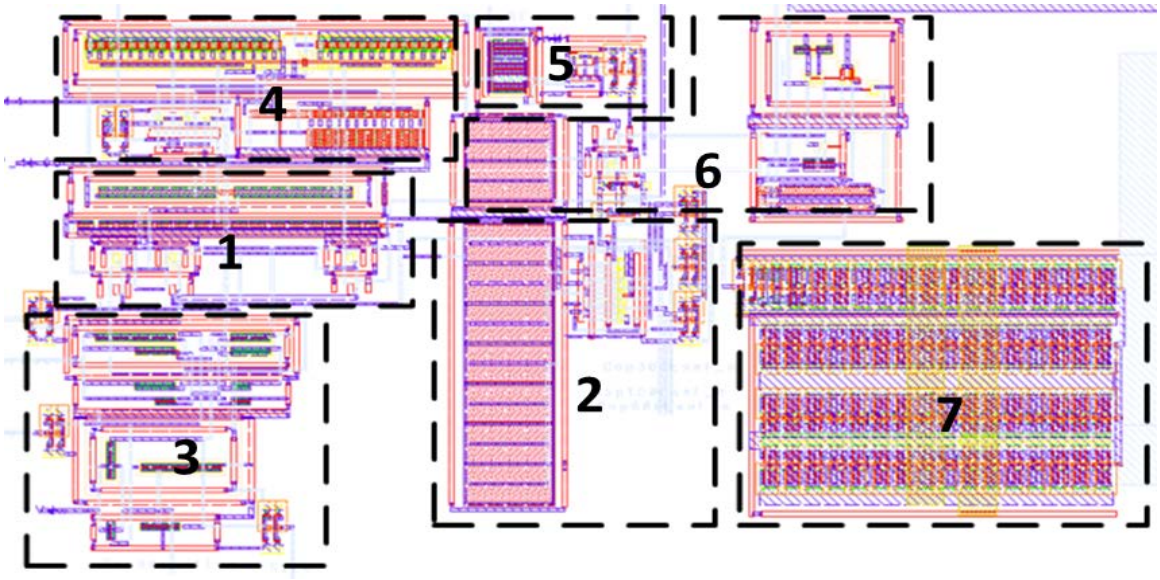

Fig. 4-1: Chip layout without pad ring

The different functional blocks in the layout are represented by the black dotted box surrounding it. Each box has a unique number from 1 to 7corresponding to a unique functionality in the circuit, which is listed below:

- 1: Cascode amplifier circuit
- 2: Switchable feedback capacitors
- 3: Analog switches
- 4: Biasing circuit for the integrator
- 5: Source follower circuit to read-out the ring-down signal
- 6: Auto-zeroed comparator circuit.
- 7: Invertor-bank circuit.

The core circuit (Fig. 4-1) area is 0.16mm×0.28mm.
Figure 4-2 shows the compete chip layout, including pad ring.

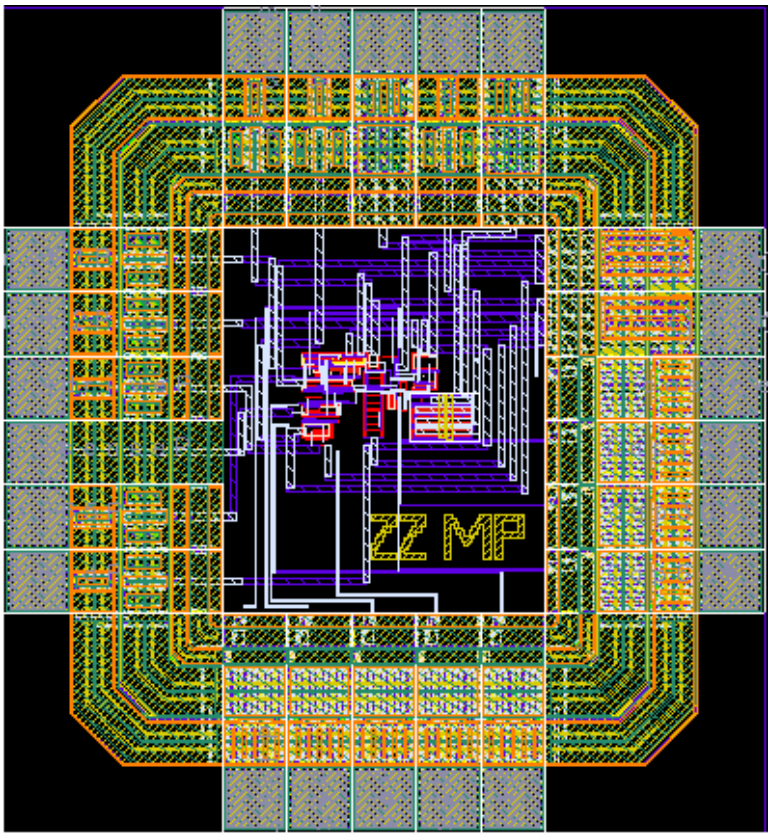

Fig. 4-2: Layout of the compete chip

4.1.2 Chip micrograph

The design is implemented in a 0.35-μm CMOS process, and the chip micrograph is shown in figure 4-3. The chip area is 1.2mm×1.3mm.

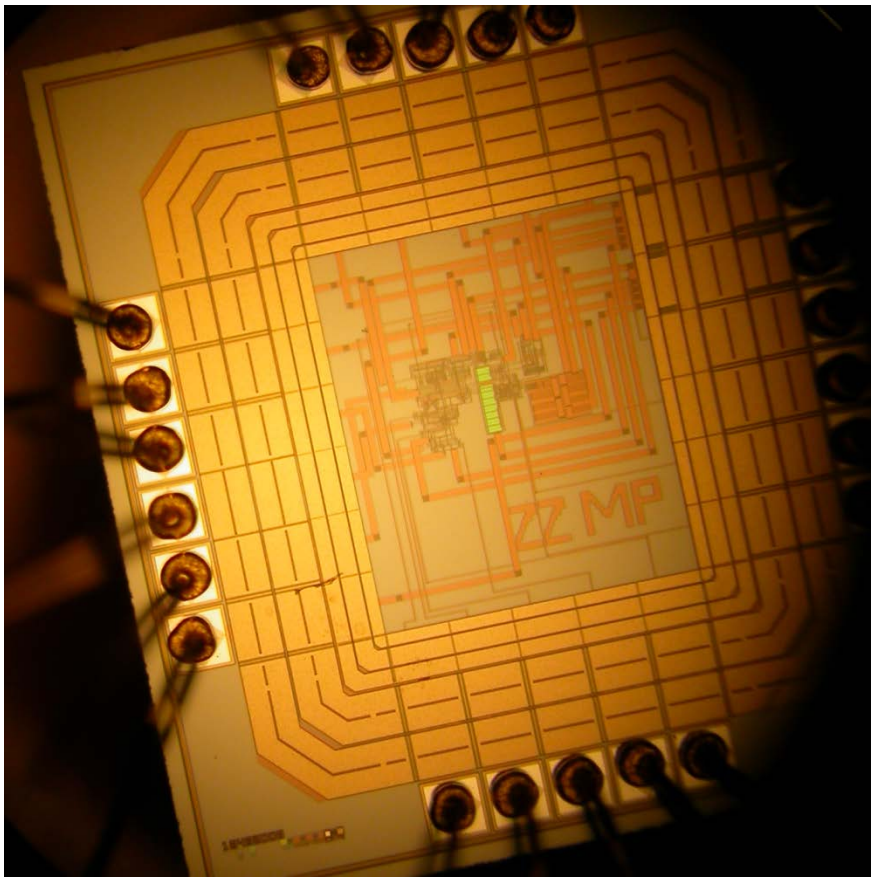

Fig. 4-3: Chip micrograph.

4.2 Measurement setup

To start our measurement, we need to build the measurement setup. A printed circuit board (PCB) is designed and fabricated as a test board for the measurement. The PCB design is described in detail in Appendix D. An overview figure of the test board is depicted in figure 4-4.

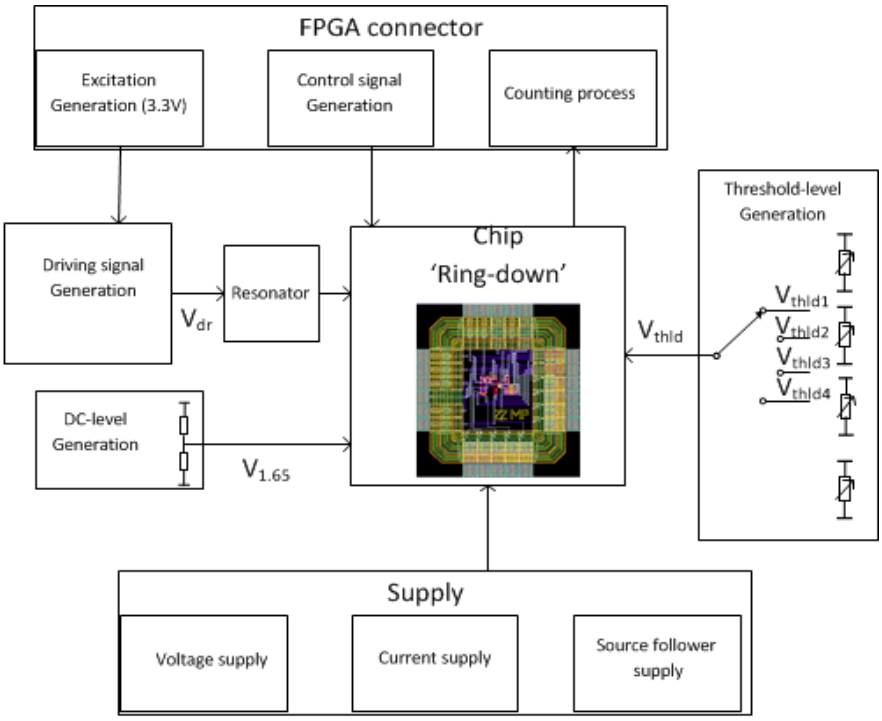

Fig. 4-4: Test board overview

Figure 4-4 shows that several parts are included in the test board:

1. FPGA development board connector (chapter 3, section 3.4)

2. Driving signal (V_{dr}) generation:

The excitation signal generated by FPGA development board is a square-wave with $3.3V_{p\text{-}p}$ amplitude, which is too large to excite the resonator. Hence, we use figure 4-5 to generate a proper driving signal (less than 200mV).

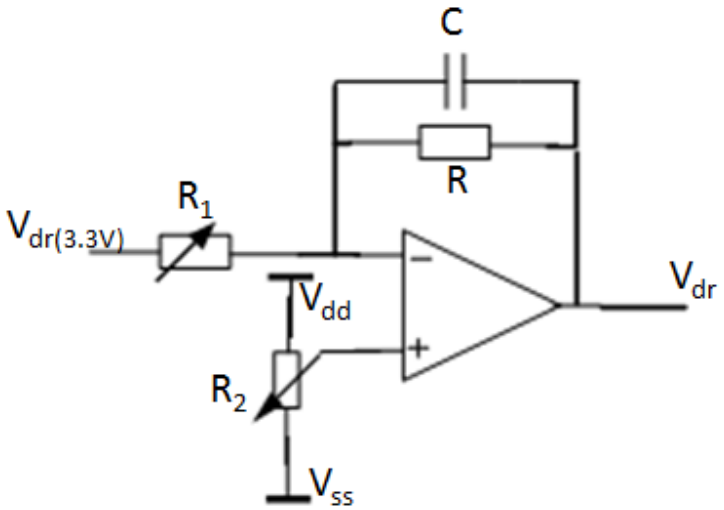

Fig. 4-5: Driving signal generation circuit

This circuit mainly has two functions:

- Reduce the input signal ($V_{dr(3.3V)}$), from FPGA) amplitude

The signal gain of the stage is :

$$\frac{V_{dr}}{V_{dr(3.3V)}} = -\frac{R}{R_1(\omega \cdot R \cdot C + 1)} \quad (4\text{-}1)$$

where ω is the angular frequency of the input signal. We choose a potentiometer for resistor R_1 to produce an output signal with a flexible amplitude.

- Low-pass filter the input square-wave.

The low-pass filter has a cut-off frequency:

$$f = \frac{1}{2 \cdot \pi \cdot R \cdot C} \quad (4\text{-}2)$$

We design the circuit with a gain of -0.1, and a cut-off frequency of 8MHz (around four times of input signal frequency); hence, we obtain the design parameters:

- C = 8.2pF
- R = 2.4kΩ
- R_1 = 200kΩ

The potentiometer R_2 is connected between the positive supply (V_{dd}) and the negative supply (V_{ss}) to obtain a programmable DC level for the excitation signal (section 4.4.1.2).

3. Output DC-level ($V_{1.65}$) generation:

A resistor-divider (two resistors with the same value in series) between 3.3V supply and ground is applied to generate the 1.65V output DC level (Fig. 4-4).

4. Threshold-level (V_{thld}) generation:

At least two threshold-levels are needed for the quality factor detection (chapter 2, section 2.2.3), and one voltage level is required for the resonance frequency detection; hence, we use a 4-channel multiplexer to provide four choices for V_{thld} . In this way, we can switch the threshold-levels easily by programming the multiplexer. To generate these voltage levels (V_{thld1}, V_{thld2}, V_{thld3} and V_{thld4}) , we implement resistor dividers with potentiometers for the flexibility (Fig. 4-4).

5. Supply:

   - Positive and negative DC voltage supply
   - DC current supply for the integrator and the comparator
   - Supply of the source follower (I_{SF}) with 5V voltage to provide a big headroom (chapter 3, section 3.1.5)

4.2.1 Equipment

An overview of the equipment setup is depicted in figure 4-6.

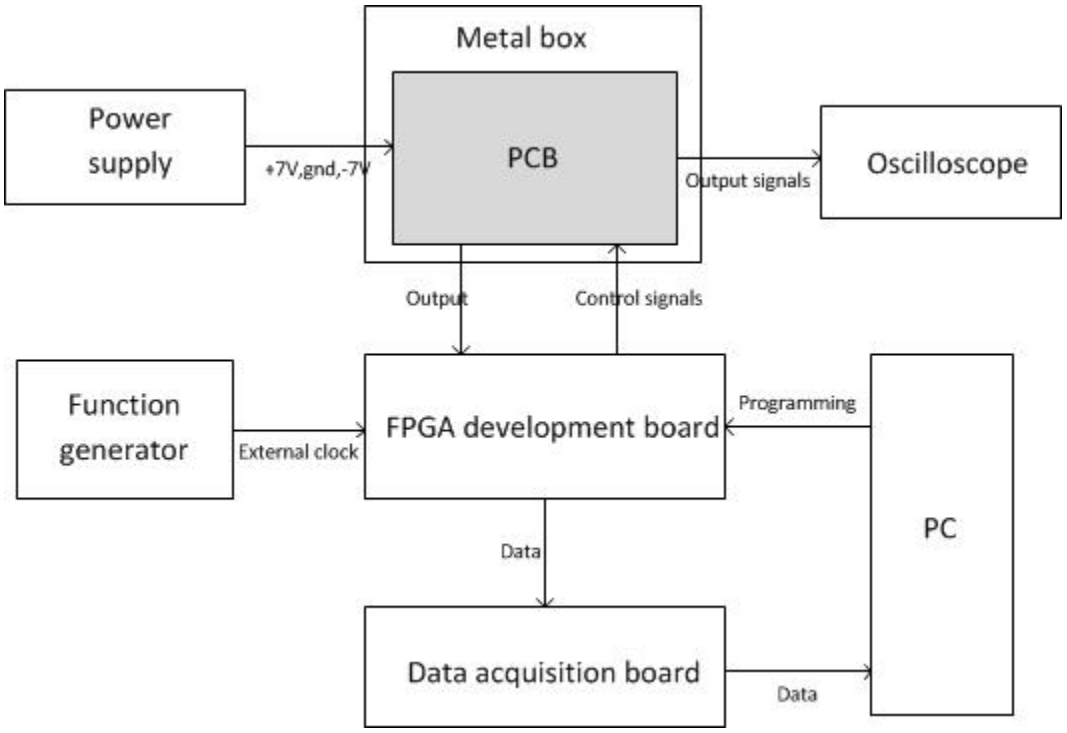

Fig. 4-6: Equipment setup overview

In the ring-down measurement, several equipment have been used (Fig. 4-6): power supply, function generator, oscilloscope, metal box, FPGA development board and data acquisition board:

- The power supply provides positive supply (+7V), negative supply (-7V) and ground (gnd) for the test board (Fig. 4-4).
- The function generator provides an external clock (a $3.3V_{p\text{-}p}$ square-wave with a frequency close to f_{res}) for the FPGA development board (chapter 3, section 3.4).
- The oscilloscope displays the level-shifted ring-down signal (read-out using the source follower) and the output signal of the comparator.

- The Metal box is used for shielding of the test PCB during measurement.
- The FPGA development board provides the control signals and the excitation for the test chip, and performs the frequency counting (chapter 3, section 3.4).
- The data acquisition board reads-out the results from the FPGA board and transfers them to the PC.
- The PC processes the measurement results and provides final f_{res} and Q values.

A photo including all the measurement equipment is shown in figure 4-7.

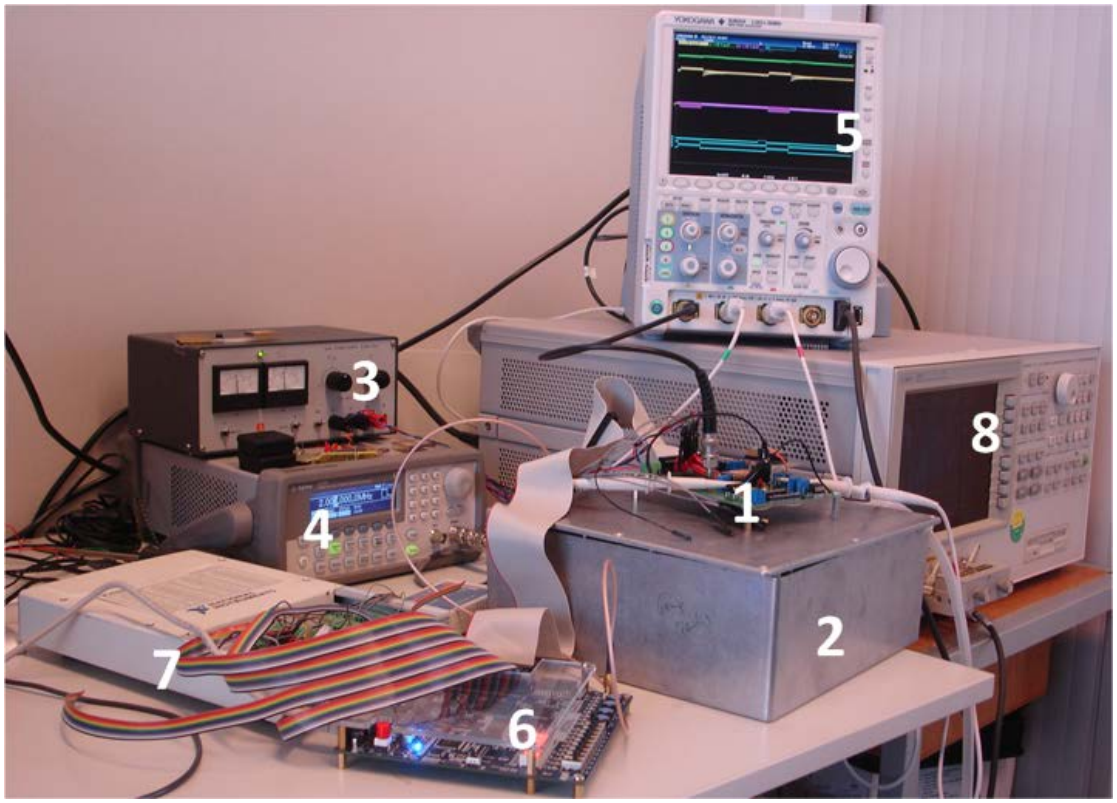

Fig. 4-7: A photo of the measurement equipment. 1: test board; 2: metal box; 3: power supply; 4: function generator; 5: oscilloscope; 6: FPGA development board; 7: data acquisition board; 8: impedance analyzer.

Equipment number 1 to 7 are used for the ring-down measurement (in Fig. 4-6); while equipment number 8 is applied for the impedance measurement (section 4.3).

4.3 Impedance measurement results

We use the impedance analysis approach (chapter1, section 1.2.2) to measure the resonance frequency and the quality factor of a sample resonator in this section. An impedance analyzer (number 8 in Fig. 4-7) is applied in this approach.
The excitation applied has a small amplitude of 100mV (to avoid non-linearity of the resonator); we sweep the frequency in a range close to 2MHz. The magnitude and phase of the impedance are plotted in figure 4-8.

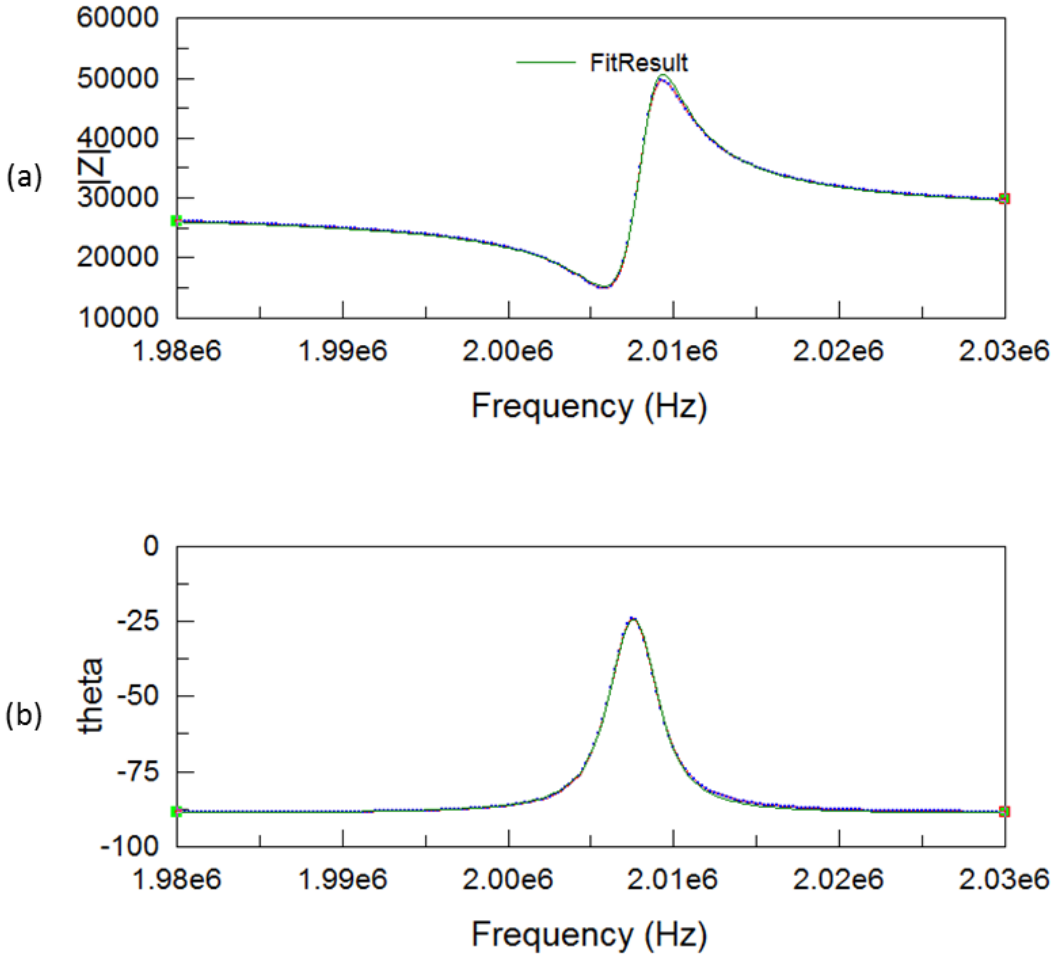

Fig. 4-8: Results of impedance measurement. (a) Magnitude of the impedance. (b) Phase of the impedance.

To calculate f_{res} and Q, we apply curve-fitting to extract the values of the model parameters (chapter 1, Fig. 1-2). The fitting lines are also shown in figure 4-8. Thus, we obtain the results shown in figure 4-9.

Element	Freedom	Value	Error	Error%
Rc	± Free(±)	450.3	13.486	2.9949
Cp	± Free(±)	2.882E-12	1.3473E-15	0.046749
Rm	± Free(±)	21369	45.129	0.21119
Lm	± Free(±)	1.148	0.0022159	0.19302
C1	± Free(±)	5.482E-15	1.0576E-17	0.19293

Fig. 4-9: Fitting results

The R_c used in figure 4-9 is to compensate for background resistance of the resonator. It has a value of few hundredohm (way less than R_m), which is neglected in our design and analysis. Hence, we have the values of each component in the resonator model:

- C_p = 2.882 pF
- R_m = 21.4 kΩ
- C_m = 5.48 fF
- L_m = 1.148 H

These values are different from what we used in simulations due to different resonator samples. With equation 1-1 and 1-2, we conclude:

$$f_{res} = 2.0062MHz \quad (4\text{-}3)$$

$$Q = 677.2 \quad (4\text{-}4)$$

Thus, we obtain a resonance frequency and quality factor value that will be used as a benchmark to compare the results obtained with ring-down based measurements (section 4.4). According to [1], DC voltage biasing of the resonator leads to resonance frequency shift. To check the bias dependency of the resonator, we repeat the above measurement with different DC bias voltages (V_{DC}).
We apply the same excitation (100mV), and calculate the resonance frequency under different bias (from -5V to +5V). The results are shown in table 4-1 and figure 4-10.

Table 4-1: Bias dependency

V_{DC} (V)	5	3	1	0	-1	-3	-5
f_{res}(MHz)	2.0099	2.0088	2.0070	2.0062	2.0058	2.0047	2.0038

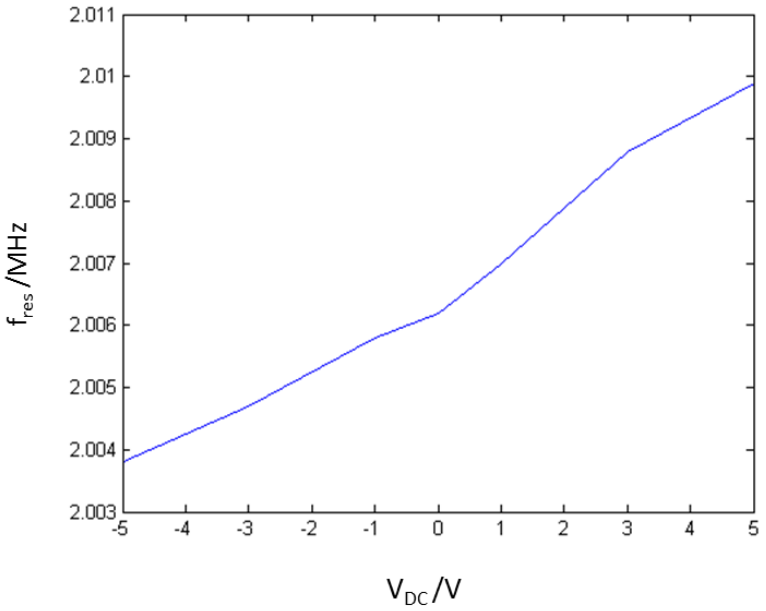

Fig. 4-10: f_{res} vs. V_{DC} (impedance analysis)

Hence, we obtain the DC bias dependency of the resonator is 0.03%/V. This result will also be compared to ring-down based measurements in the next section.

4.4 Ring-down measurement results

In this section, an overview of the results using ring-down measurement approach is described in two parts: resonance frequency measurement and quality factor measurement.

4.4.1 Resonance frequency

We apply an excitation (without DC bias) with 100mV amplitude and a frequency of 2.006MHZ (generated on the PCB) for the ring-down measurement.
All the feedback capacitors are selected, with a total capacitance of 1050fF. With a threshold voltage of 1.65V, we obtain the results shown in figure 4-11.

Fig. 4-11: Measurement results shown on the oscilloscope. (a) Control signals of switch 1,2,3 and 5. (b) Ring-down signal reads-out by the source follower. (c) Comparator output. (d) Zoom-in view of the upper half part.

Figure 4-11 shows an auto-zeroing measurement and a frequency counting measurement, with each measurement lasting about 1ms (chapter 2, section 2.3.3.3). The output signals of the two measurements (Fig. 4-11(3)) look similar because the offset is already stored on the auto-zeroing capacitor (C_{AZ}) due to the continuous excitation we apply. Figure 4-11(d) is the close-up view of the initial ring-down of the second measurement, where a clear square wave around 2MHz can be seen.

The resonance frequency can be calculated using equation 2-8 (chapter 2, section 2.2.3). We rewrite the equation here:

$$f_{res} = \frac{N}{M} \cdot f_0 \quad (4\text{-}5)$$

If we use the output signal (Fig. 4-11(c)) as the input of the FPGA development board, and count N=150 ring-down cycles, with f_0=50MHz (chapter 3, section 3.4), we obtain the value of M with the code in appendix B (Fig. 4-12(a)). Thus, with equation 4-3, we can calculate f_{res} (Fig. 4-12(b)).

Figure 4-12 displays the results of M and f_{res} by repeating the measurement 1000 times (iteration).

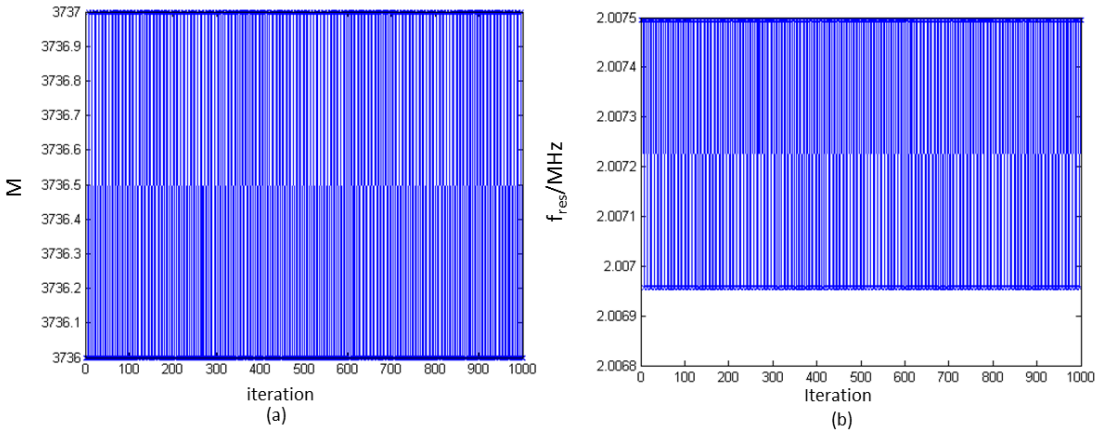

Fig. 4-12: (a) Number of reference clock cycles (b) Resonance frequency

Figure 4-12(a) shows that the number of reference clock cycles (*M*) is varying within one cycle (between 3736 and 3737), thus we can conclude that the above measurement is quantization-noise limited.
We average these 1000 results from figure 4-12(b); hence, we have:

$$f_{res} = 2.0073MHz \qquad (4\text{-}6)$$

Compared with equation 4-3 (f_{res} obtained by impedance measurement), the results are off by 0.05%, this is partially because with ring-down measurement, the resonator is actually biased with a DC voltage around 0.55V during the integration phase (section 4.3.1.3) , thus produces a bit bigger f_{res} value.

4.4.1.1 Resonance frequency versus number of ring-down cycles

In this sub-section, we give the measurement results of the resonance frequency under a situation that different number of ring-down cycles are applied, while the other conditions remain the same.
The detectable number of ring-down cycles (*N*) is limited by the SNR limitation (multiple transitions due to the noise level, see chapter 2, section 2.3.2). In this measurement, we take five different values of *N*, from 50 to 250. The results are shown in table 4-2 and figure 4-13.

Table 4-2: f_{res} vs. *N*

N	50	100	150	200	250
f_{res}(MHz)	2.0087	2.0077	2.0073	2.0073	2.0073

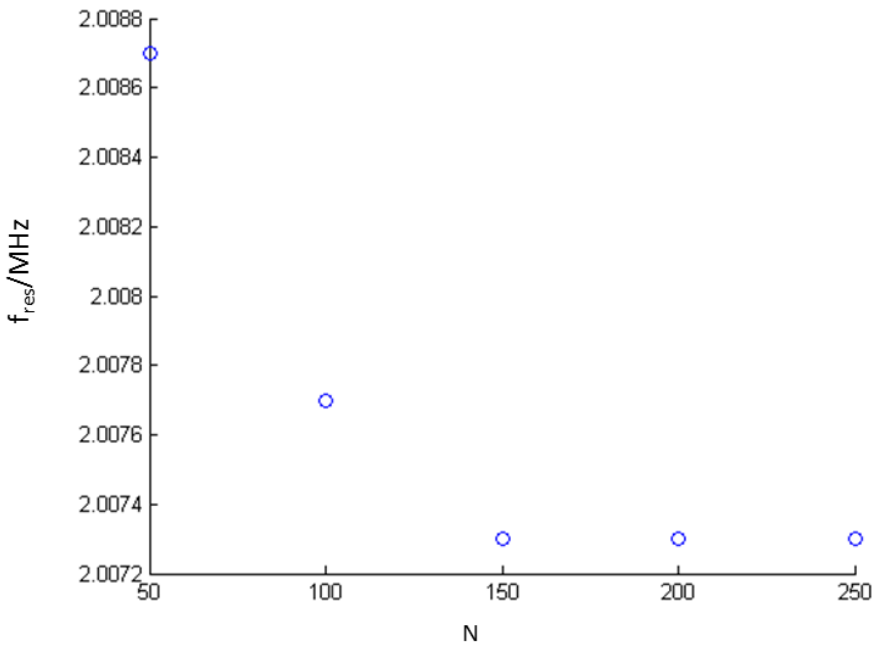

Fig. 4-13: f_{res} vs. N

The resonance frequency is slightly higher for smaller values of N, and remains stable when N reaches a certain value (150). A small N means a short measurement time in the frequency counting phase, which gives big relative quantization step with a fixed 50MHz reference clock, which explains what we see in figure 4-13 when N is small.

4.4.1.2 Resonance frequency versus DC biasing

Figure 2-5 demonstrates the way we operate the front-end circuit during the integration phase; to illustrate how we apply different DC biasing conditions to the resonator, we re-draw the circuit in figure 4-14.

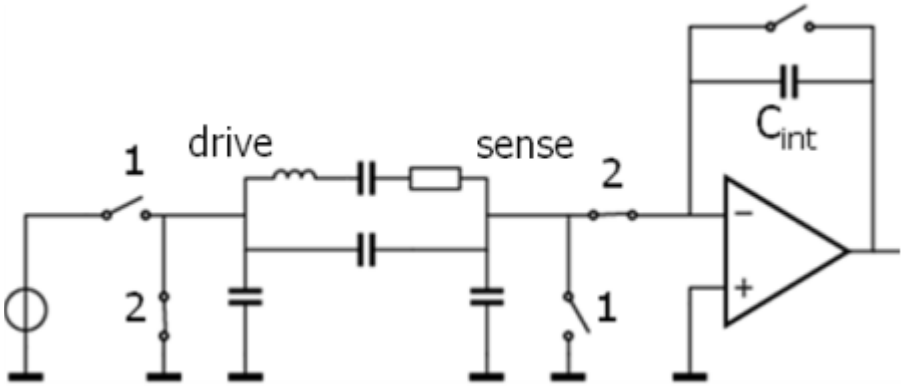

Fig. 4-14: Front-end circuit during the integration phase

The circuit operates in such a way that the ‘sense’ node (Fig. 4-14) of the resonator is connected to ground in the excitation phase, while the drive node is switched to ground in the integration phase, which makes the DC biasing across the resonator a fixed value (0V

during excitation phase, and around 0.55V during integration phase).
To be able to apply different bias levels, we modify the setup as shown in Figure 4-15.

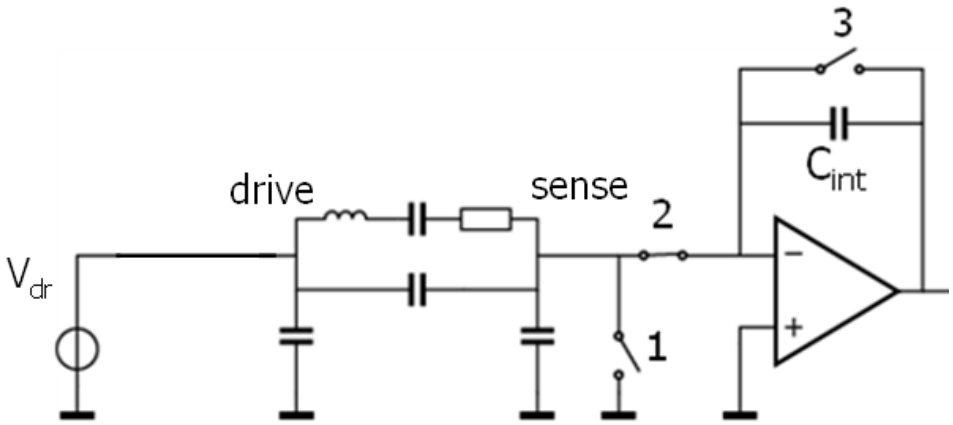

Fig. 4-15: Another way to apply excitation signal

We apply the excitation signal (V_{dr}) directly at 'drive' node of the resonator (without using the on-chip switches). This excitation signal is gated by the control signal of switch 1:

- When the control signal of switch 1 is 'high' during the excitation phase, V_{dr} is the driving signal
- When the control signal of switch 1 is 'low' during the integration phase, V_{dr} is 0V.

Hence, we can control the offset level of V_{dr} to apply different DC biasing (V_{DC}) to the resonator (section 4.2).
With the new measurement setup, we obtain the measurement results of the resonance frequency versus DC biasing shown in table 4-3 and figure 4-16.

Table 4-3: f_{res} vs. V_{DC}

V_{DC} (V)	-0.5	0	0.5	1	1.5	2
f_{res}(MHz)	2.0069	2.0073	2.0076	2.0079	2.0083	2.0087

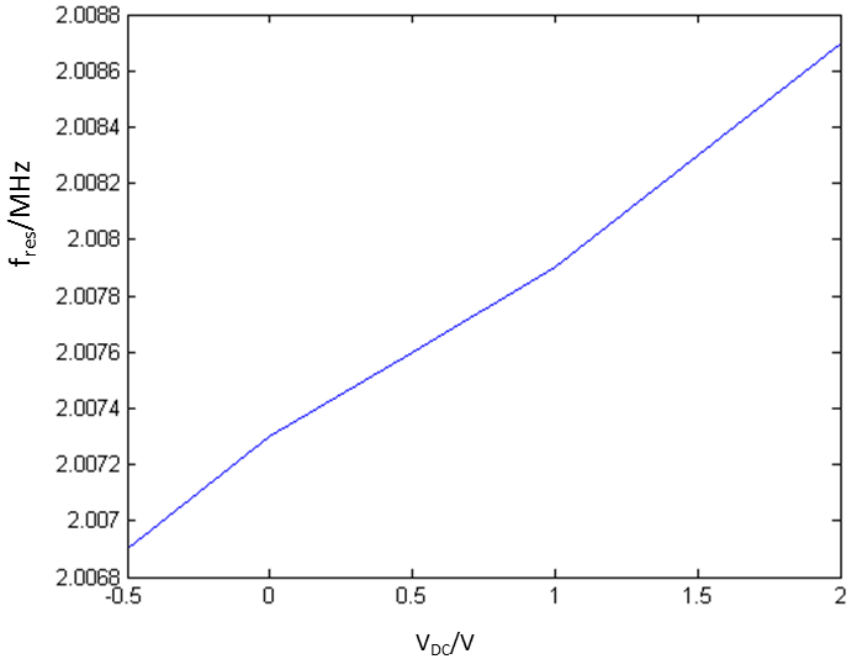

Fig. 4-16: f_{res} vs. V_{DC}

After simple calculations based on figure 4-16, we conclude that the DC biasing dependency of the resonator is around 0.035%/V. This result is nicely agree with what we obtained using impedance measurement (Fig. 4-10).

4.4.1.3 Exposure to water vapor

In the resonance frequency measurements, we also tried to breathe on the sensor gently during continuous monitoring to show a rough proof-of-concept of frequency shift due to humidity in breath. Even though uncoated, we can still see some frequency shift in the measurement results (Fig. 4-17).

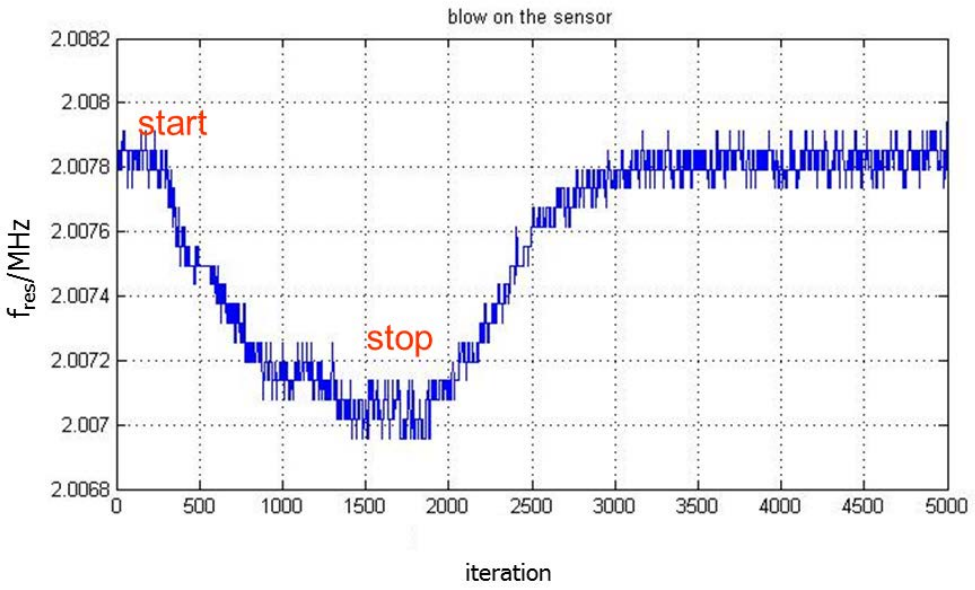

Fig. 4-17: Resonance frequency shift measured while breathing on the sensor

To have sufficient time to see the changes of f_{res}, we take 5000 repeated measurements, which is around 10s measurement time in total. We apply a 10-point moving-average filter to smooth the figure. We start blowing over the sensor in the beginning of the measurement and stop blowing at some point (Fig. 4-17).
As a result, we conclude that f_{res} decreases while blowing over the sensor and eventually comes back to the original value after the blowing has stopped. A similar behavior of the sensor response to humidity can be found in [1].

4.4.2 Quality factor

Two threshold voltages need to be applied to measure the quality factor (chapter 2, section 2.2.3). For each threshold voltage, total number of ring-down cycles has to be recorded.
Similar with the measurement of $f_{res,}$ we apply a driving signal with an amplitude of 100mV, a frequency of 2.006MHz; and a DC bias voltage of 0V. Again, for each threshold voltage, we repeat 1000 measurements.
In these 1000 results, few values appear that are far away from the average value; hence, we take the median value among the 1000 results to represent *Q*.
Although two threshold-levels are enough for quality factor measurement, we take three voltage levels to make more combinations. We use symbol '*a*' to represent the applied threshold-level (V_{thld}) relative to the output DC-level (1.65 V), and '*N*' for measured number of ring-down cycles. The measurement results are listed in table 4-4:

Table 4-4: Quality factor measurement results

Point	V_{thld}	*a* (V_{thld} -1.65 V)	*N*
*P*1(*a*1,*N*1)	1.75V	0.1V	259
*P*2(*a*2,*N*2)	1.85V	0.2V	114
*P*3(*a*3,*N*3)	1.95V	0.3V	28

Quality factor can be calculated by equation 2-13, we re-write it here:

$$Q = \frac{\pi \cdot \Delta N}{\ln(a_1/a_2)} \quad (4\text{-}7)$$

Hence, we have the calculated results of Q (Table 4-5).

Table 4-5: Results of quality factor

Points	P1,P2	P1,P3	P2,P3
Δ N	145	231	86
Q	657	661	666

The measured quality factor value varies due to the multiple transitions of the last ring-down cycles, which have a smaller SNR. The three results we obtained (Table 4-5) provide an average value to represent Q; hence, we have:

$$Q = 661 \quad (4\text{-}8)$$

This result nicely matches what we obtained by impedance measurement (Eq.4-4).

4.4.3 Energy consumption

To calculate the energy consumption, we measure the total DC current consumed by the chip through the pin 'vdd' (voltage supply for the integrator and the comparator, see Appendix D, Table D1). We measured the supply current in two cases:

- The cascode circuit is always powered on
- The cascode circuit is powered off after the excitation phase (chapter 3, section 3.1.2) to save energy

The total measurement time is defined by the frequency of the external clock (chapter 3, section 3.4). With a clock of 2.006MHz, we obtain a measurement time of 1.994ms. The comparator is always powered on in our measurements since we do not design the chip or PCB in the way that allows us to control the comparator supply easily (could be considered in further work).
The final results are listed in table 4-6.

Table 4-6: Energy consumption

Cascode circuit always powered on?	Supply voltage	Supply current	Time	Energy consumption
Yes	3.3V	41.6µA	1.994ms	273.7nJ
No	3.3V	36µA	1.994ms	236.9nJ

The reference currents ('I_{ref1}' and 'I_{ref2}', see Appendix D, Table D1) we apply are a bit less than what have been applied in the simulation; hence, the total DC current consumption is less than what we expected (chapter 3, Table 3-1).
Thus, we obtain the final energy consumption of 236.9nJ per measurement, less than what we derived in the simulation (272nJ per measurement, see section 3.3.5)
As mentioned before (chapter 3, section 3.3.5), by reducing the measurement time, we expect to achieve an energy consumption of around 120nJ per measurement.

4.5 Conclusions

In this chapter, we measure the resonance frequency and quality factor of the resonator using two methods: ring-down measurement and, for comparison, impedance measurement. We summarize the results in table 4-7:

Table 4-7: Summary of results

Method	f_{res}	Q
Ring-down measurement	2.0073MHz	661
Impedance measurement	2.0062MHz	667

Both resonance frequency and quality factor of these two methods are nicely in agreement.
The resonance frequency shift due to DC biasing (0.035%/V) is also in nicely agreement with what we obtained with impedance measurement (0.03%/V). The measurement of breath on the sensor shows the resonance frequency is responding to humidity in breath.

References

[1] D. M. Karabacak, "Enhanced sensitivity volatile detection with low power integrated," Lab on a Chip, vol. 10, pp. 1976-1982, Apr. 2010.

[2] D. M. Karabacak, "Modal sensitivity to DC biasing," Private Communication.

Chapter 5

Conclusions and Recommendations

5.1 Conclusions

Very high aspect (length/thickness) ratio doubly clamped beam resonators with integrated piezoelectric transducers have been provided by Holst Centre. These resonators are great candidates for application in wireless autonomous sensor systems, owning to their low power consumption, high integratability and high sensitivity. By applying appropriate coatings to these resonators, they can be used to sense concentration of volatile organic compounds like ethanol, benzene etc, by measuring shifts in resonance frequency f_{res} and quality factor Q. But they can only live up to the promise of being highly energy-efficient if energy-efficient readout circuits are available to read them out. This thesis describes the design and characterization of such a readout circuit.

Several approaches to read-out resonator sensors have been reported in literature. The three main methods are: oscillator-based readout, impedance analysis and ring-down measurement.

Oscillator-based readout is hard to apply to the resonators we studied, unless special techniques are applied to cancel the effects of their large parasitic capacitor C_p, which makes the phase shift of the resonator at f_{res} small and poorly defined (chapter 1, section 1.2.1.2). Furthermore, to measure oscillation frequency, power is need to ensure a well-defined phase shift of the oscillation circuitry. Also, quality factor measurement using this readout approach is not so straight forward.

Impedance analysis is applied mainly under laboratory conditions due to the costly and large equipment required. The required frequency sweep makes the measurement time consuming and energy hungry. Also, the curve-fitting needed to extract f_{res} and Q is relatively computationally intensive.

In this work, we apply the ring-down measurement technique. The basic principles of this technique have been reported in [1,2,3]. Earlier implementations of the technique were realized using discrete components. Moreover, the energy-efficiency potential of the technique was left unexplored. In this MSc project, we have developed an ultra-low-power integrated readout circuit based on ring-down measurement. This is, to our best knowledge, the first integrated implementation of the ring-down measurement technique.

Our readout circuit consists of four key parts: a driving circuit that excites the resonator at a frequency close (but not necessarily equal) to its resonance frequency, an integrator

that senses the ring-down current after the excitation is stopped, a comparator that detects the zero-crossings of the integrator's output voltage, and finally a counter that determines the frequency of these zero-crossings, which equals the resonance frequency. Moreover, we have shown how a modification of this architecture, using non-zero thresholds levels for the comparator, can be used to measure the resonator's quality factor.
Studies and analysis have been made at the architecture-level, to investigate the design choices (chapter 2). We have presented several key points:

- The proper resonance mode to work with.
- Front-end circuit operation to mitigate the effects of C_p
- Auto-zeroed comparator operation to enable proper zero-crossing detection in the presence of offset error.

We have analyzed the effects of quantization error, thermal noise and offset; and derived design requirements that should be met to achieve the desired detection limit of $\delta f_{res}/f_{res} < 10^{-4}$ based on this analysis. We concluded that a trans-conductance of at least 300µS is needed for the integrator, and a delay of at most 15ns for the comparator.
In the circuit design, we use a simple cascode amplifier and a two-stage comparator to achieve the required performance. We have applied low-leakage switches to improve the performance and switchable feedback capacitors to increase the design flexibility. The simulation results of the circuit-level design have been analyzed (see section 3.3) in terms of signal amplitude, noise, offset and energy consumption. With simulated SNR and offset match well with what we expected from the calculations.
After the layout design, a prototype chip has been fabricated in 0.35-µm CMOS technology. Together with a test PCB and a FPGA development board on which the digital part of the readout circuit has been implemented, a fully-functional ring-down based readout system has been realized.
We have measured the same resonator using two different methods: the proposed ring-down measurement using our prototype chip, and, for comparison, impedance analysis using a bench-top impedance analyzer. The measured resonance frequencies and quality factors chapter 4, Table 4-7), show good consistency. The measured resonance frequency shifts with changing DC biasing in both methods are also in good agreement. Moreover, measurements have been shown that demonstrate the transient response of the sensor to humidity.
With a total current consumption of 36µA in a measurement time of 1.994ms, we have a low energy consumption of 236.9nJ per measurement (which is expected to be reduced to 120nJ per measurement by applying a shorter measurement time, section 4.3.3).

5.2 Highlights

Compared with the existing work, the presented readout approach has several advantages：

- The circuit achieves low energy consumption, expected to be more energy-efficient than the oscillator-based approach.
- The circuit has the ability to measure quality factor (Q) easily.
- The circuit is insensitive to the parasitic capacitor (C_p).
- The circuit can be reconfigured relatively easily to operate with different devices and resonance modes.

5.3 Future Work

As a first approach, we use a relatively simple circuitry to implement this ultra-low-power integrated readout circuit. Though we have good results, various things can be addressed in future work to improve the performance:

- Do measurements in a gas chamber to check how the readout circuit responds to actual changing volatile concentrations.
- Optimize the energy consumption of the comparator.
  With our design, the comparator actually consumes more energy/supply than the main integrator (chapter 3, Table 3-1). An easy way is to power it on only from the auto-zeroing phase (at the end of the first measurement, see chapter 3, section 3.3.5)
- Design the comparator with hysteresis to avoid multiple transitions at the end of the ring-down signal due to small voltage fluctuations (noise). But there is a trade-off since the amplitude at the end of the ring-down is also small.
- Develop an optimized low-power excitation source that selectively excites the desired mode taking into account its exact frequency is unknown.
- Explore the possibilities of resistive feedback circuit.
  Any small leakage at the “sense” node (gate of the integrator) through the integrator capacitor (C_{int}) will cause a droop on the ring-down (chapter 3, section 3.1.4). With resistive feedback, the droop issue due to leakage can be solved (the induced offset can be cancelled out with auto-zeroing technique).
- Explore the possibilities of working at fundamental mode. For the Holst sensors,

the piezoelectric patch is better matched to the fundamental mode shape in comparison to other modes [5].

References

[1]M. Rodahl and B. Kasemo, “A simple setup to simultaneously measure the resonant frequency and the absolute dissipation factor of a quartz crystal microbalance”, Rev. Sci. Instrum, vol. 67, pp. 3238-3241, September. 1996.

[2]K. Zeng, “Time domain characterization of oscillating sensors: Application of frequency counting to resonance frequency determination”, Rev. Sci. Instrum, vol. 73, pp. 4375-4380, 2002.

[3]K. Zeng, “Threshold-crossing counting technique for damping factor determination of resonator sensors”, Rev. Sci. Instrum, vol. 75, pp. 5257-5261, Dec. 2004.

[4] Brian P. Otis, “A 300-µW 1.9-GHz CMOS Oscillator Utilizing Micro Micromachined Resonators”, IEEE Journal of Solid-state Circuit, vol. 38, NO. 7, July 2003.

[5] D. M. Karabacak, Private Communication.

Appendix A

Detection Limit Analysis Based on SNR

From the analysis of the thermal noise (chapter 2, section 2.3.2.2), we have obtained the following equation for the detection limit:

$$\frac{\delta f_{res}}{f_{res}} = \frac{V_{n,RMS}}{2 \cdot \pi \cdot N \cdot A_0 \cdot e^{-\pi}} \qquad (1)$$

We have also derived equation 2-7 for ring-down amplitude (chapter 2, section 2.2.1.2). Hence, we have the detection limit:

$$\frac{\delta f_{res}}{f_{res}} = \frac{V_{n,RMS}}{2 \cdot \pi \cdot N \cdot e^{-\pi} \cdot \frac{V_s}{2 \cdot \pi \cdot f_{res} \cdot C_{\text{int}} \cdot R_m} \cdot \frac{g_m}{\sqrt{g_m^2 + (2 \cdot \pi \cdot f_{res} \cdot C_p)^2}}} \qquad (2)$$

The output root-mean-square (RMS) noise can be calculated as:

$$V_{n,RMS} = \sqrt{\int_0^\infty S_Y(f) df} \qquad (3)$$

where $S_Y(f)$ is the integrator's output noise power spectral density (PSD). It holds that:

$$S_Y(f) = S_X(f) \cdot H(f)^2 \qquad (4)$$

where $S_X(f)$ is the input noise PSD, and $H(f)$ is integrator's transfer function.
Figure A1 depicts the circuit used for noise analysis.

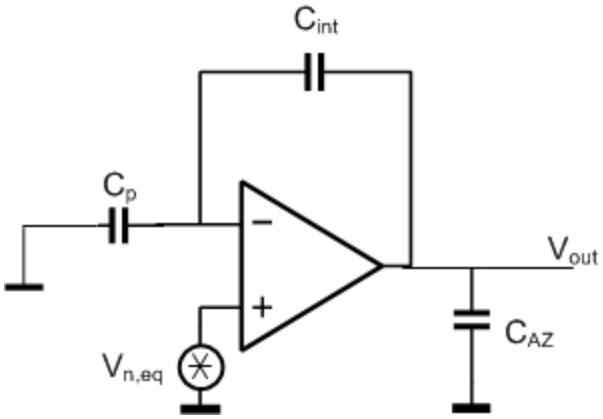

Fig. A1: Circuit used for noise analysis of the integrator.

$V_{n,eq}$ represents the equivalent input noise source, with a PSD of $(16/3)kT/g_m$ (chapter 2, section 2.3.2.3). With assumption we made in section 2.3.2.3 (infinite DC gain and input noise PSD), according to [A.1], we have the output RMS noise:

$$V_{n,RMS} = \sqrt{\frac{4 \cdot k \cdot T}{3 \cdot \beta \cdot C_0}} \qquad (5)$$

where β is the feedback factor, and C_0 is the load capacitance at the output. It holds that:

$$\beta = \frac{C_{\text{int}}}{C_{\text{int}} + C_p} \qquad (6)$$

$$C_0 = C_{AZ} + \frac{C_{\text{int}} C_p}{C_{\text{int}} + C_p} \qquad (7)$$

Hence, we derive the output RMS noise (assuming $C_p >> C_{\text{int}}$):

$$V_{n,RMS} = \sqrt{\frac{4 \cdot k \cdot T \cdot C_p}{3 \cdot C_{\text{int}} \cdot (C_{AZ} + C_{\text{int}})}} \qquad (8)$$

Combining equation (2) and (8) results in:

$$\frac{\delta f_{res}}{f_{res}} = \frac{\sqrt{\frac{4 \cdot k \cdot T \cdot C_p}{3 \cdot C_{\text{int}} \cdot (C_{AZ} + C_{\text{int}})}}}{2 \cdot \pi \cdot N \cdot e^{-\pi} \cdot \frac{V_{dr}}{2 \cdot \pi \cdot f_{res} \cdot C_{\text{int}} \cdot R_m} \cdot \frac{g_m}{\sqrt{g_m^2 + (2 \cdot \pi \cdot f_{res} \cdot C_p)^2}}} \qquad (9)$$

simplifying (9) gives:

$$\frac{\delta f_{res}}{f_{res}} = \frac{f_{res} \cdot R_m \cdot \sqrt{\frac{4 \cdot k \cdot T \cdot C_p \cdot C_{\text{int}}}{3 \cdot (C_{AZ} + C_{\text{int}})}} \cdot \sqrt{(\frac{2 \cdot \pi \cdot f_{res} \cdot C_p}{g_m})^2 + 1}}{N \cdot e^{-\pi} \cdot V_{dr}} \quad (10)$$

So far, we have the equation for the detection limit based on noise consideration. Together with equation 1-1 and 1-2 (chapter 1), we derive the equation in terms of the resonator parameters:

$$\frac{\delta f_{res}}{f_{res}} = \frac{R_m^{\ 2} \cdot \sqrt{\frac{4 \cdot k \cdot T \cdot C_p \cdot C_{\text{int}}}{3 \cdot (C_{AZ} + C_{\text{int}})}} \cdot \sqrt{(\frac{2 \cdot \pi \cdot f_{res} \cdot C_p}{g_m})^2 + 1}}{2 \cdot \pi \cdot L_m \cdot e^{-\pi} \cdot V_{dr}} \quad (11)$$

References

[A.1] R. Schreier, J. Silva, J. Steensgaard, G. C. Temes, “Design-oriented estimation of thermal noise in switched-capacitor circuits”, IEEE Transaction Circuits and System., vol. 52, no. 11, Nov. 2005.

Appendix B

Verilog Code for f_{res} Detection

```
module digital (VoutF, clkfast, clk,clk_DAQ,  reset, count, Vex, s1, s2, s3, s5, Cap150, Cap300, Cap600, SF_sel, A0, A1, s_casc);
input clk, clkfast, reset, VoutF;
output  count, count_steady, Vex, s1, s2, s3, s5, Cap150, Cap300, Cap600, SF_sel, A0, A1, s_casc, clk_DAQ;

reg[14:1] clkfast_reg;
reg[14:1] count;
reg[14:1] count_steady;
reg[9:1] VoutF_reg;
reg[12:1] clk_reg;
reg s1;
reg s2;
reg s3;
reg s5;
reg s_casc;
reg sh;
reg VoutF_sync;
wire clk_DAQ;
wire Cap150;
wire Cap300;
wire Cap600;
wire SF_sel;
wire A0;
wire A1;
wire Vex;

assign Vex = clk;
assign clk_DAQ = sh;
assign Cap150 = 1'b1;
assign Cap300 = 1'b0;
assign Cap600 = 1'b0;
```

```
assign SF_sel = 1'b1;
assign A0 = 1'b0;
assign A1 = ~A0;
assign test = clk;

always @(posedge clk)
begin
if (reset == 1'b0)
   begin
                clk_reg  <=12'b000000000000;
   end
else
   begin
                clk_reg  <= clk_reg+1'b1;
                if (clk_reg == 12'b111110100000)
                        begin
                                clk_reg  <=12'b000000000000;
                        end
   end
end

always @(posedge clk)
begin
if ((clk_reg >= 12'b000000000000 && clk_reg < 12'b000111110100) || (clk_reg >=
12'b011111010000 && clk_reg < 12'b100111000100))
        begin
                s1 <= 1'b1;
        end
else
        begin
                s1 <= 1'b0;
        end
end

always @(posedge clk)
begin
if ((clk_reg >= 12'b000000000000 && clk_reg < 12'b000111110110) || (clk_reg >=
12'b011111010000 && clk_reg < 12'b100111000110))
        begin
                s2 <= 1'b0;
        end
else
        begin
                s2 <= 1'b1;
        end
end
```

```
always @(posedge clk)
begin
if ((clk_reg >= 12'b000000000000 && clk_reg < 12'b000111111010) || (clk_reg >= 12'b011111010000 && clk_reg < 12'b100111001010))
	begin
		s3 <= 1'b1;
	end
else
	begin
		s3 <= 1'b0;
	end
end

always @(posedge clk)
begin
if ((clk_reg >= 12'b000000000000 && clk_reg < 12'b001000110000) || (clk_reg >= 12'b011111010000 && clk_reg < 12'b101000000000))
	begin
		s_casc <= 1'b1;
	end
else
	begin
		s_casc <= 1'b1;
	end
end

always @(posedge clk)
begin
if (clk_reg >= 12'b011100001000 && clk_reg < 12'b011111000110)
	begin
		s5 <= 1'b1;
	end
else
	begin
		s5 <= 1'b0;
	end
end

always @(posedge clk)
begin
	if (clk_reg >= 12'b100111001010)
		begin
			sh <= 1'b1;
		end
	else
```

```
                begin
                        sh <= 1'b0;
                end
end

always @(negedge clkfast)
begin
        VoutF_sync <= VoutF;
end

always @(posedge VoutF_sync)
begin
        if (sh == 1'b0)
                begin
                        VoutF_reg <= 9'b000000000;
                end
        else
                begin
                        if (VoutF_reg < 9'b111111111)
                                begin
                                        VoutF_reg <= VoutF_reg + 1'b1;
                                end
                end
end

always @(posedge clkfast)
begin
        if (VoutF_reg == 9'b000000000)
                begin
                        clkfast_reg <= 14'b00000000000000;
                end
        else
                begin
                        if (VoutF_reg > 9'b010010110)
                                begin
                                        count <= clkfast_reg;
                                end
                        else
                                begin
                                        clkfast_reg <= clkfast_reg + 1'b1;
                                end
                end
end

endmodule
```

Appendix C

Verilog Code for *Q* Detection

```
module digitalQ (VoutF, clkfast, clk,clk_DAQ,  reset, count, Vex, s1, s2, s3, s5, Cap150, Cap300, Cap600, SF_sel, A0, A1, s_casc);
input clk, clkfast, reset, VoutF;
output  count,  Vex, s1, s2, s3, s5, Cap150, Cap300, Cap600, SF_sel, A0, A1, s_casc, clk_DAQ;

reg[8:1] clkfast_reg;
reg[10:1] count;
reg[10:1] VoutF_reg;
reg[12:1] clk_reg;
reg[16:1] C;
reg s1;
reg s2;
reg s3;
reg s5;
reg s_casc;
reg sh;
reg sh_old;
reg VoutF_sync;
wire clk_DAQ;
wire Cap150;
wire Cap300;
wire Cap600;
wire SF_sel;
wire A0;
reg A1;
wire Vex;

assign Vex = clk;
assign clk_DAQ = sh;
assign Cap150 = 1'b1;
assign Cap300 = 1'b0;
```

```
assign Cap600 = 1'b1;
assign SF_sel = 1'b1;
assign A0 = 1'b0;

always @(posedge clk)
begin
if (reset == 1'b0)
   begin
                clk_reg  <=12'b000000000000;
   end
else
   begin
                clk_reg  <= clk_reg+1'b1;
                if (clk_reg == 12'b111110100000)
                        begin
                                clk_reg  <=12'b000000000000;
                        end
   end
end

always @(posedge clk)
begin
if ((clk_reg >= 12'b000000000000 && clk_reg < 12'b000111110100) || (clk_reg >=
12'b011111010000 && clk_reg < 12'b100111000100))
        begin
                s1 <= 1'b1;
        end
else
        begin
                s1 <= 1'b0;
        end
end

always @(posedge clk)
begin
if ((clk_reg >= 12'b000000000000 && clk_reg < 12'b000111110110) || (clk_reg >=
12'b011111010000 && clk_reg < 12'b100111000110))
        begin
                s2 <= 1'b0;
        end
else
        begin
                s2 <= 1'b1;
        end
end
```

```
always @(posedge clk)
begin
if ((clk_reg >= 12'b000000000000 && clk_reg < 12'b000111111010) || (clk_reg >= 12'b011111010000 && clk_reg < 12'b100111001010))
        begin
                s3 <= 1'b1;
        end
else
        begin
                s3 <= 1'b0;
        end
end

always @(posedge clk)
begin
if ((clk_reg >= 12'b000000000000 && clk_reg < 12'b001000110000) || (clk_reg >= 12'b011111010000 && clk_reg < 12'b101000000000))
        begin
                s_casc <= 1'b1;
        end
else
        begin
                s_casc <= 1'b0;
        end
end

always @(posedge clk)
begin
if (clk_reg >= 12'b011100001000 && clk_reg < 12'b011111000110)
        begin
                s5 <= 1'b1;
        end
else
        begin
                s5 <= 1'b0;
        end
end

always @(posedge clk)
begin
        if (clk_reg >= 12'b100111001010)
                begin
                        sh <= 1'b1;
                end
        else
                begin
```

```
                        sh <= 1'b0;
                end
end

always @(posedge clk)
begin
        if (clk_reg >= 12'b11111010000)
                begin
                        A1 <= 1'b0;
                end
        else
                begin
                        A1 <= 1'b1;
                end
end

always @(negedge clkfast)
begin
        VoutF_sync <= VoutF;
        if (VoutF_sync == 1'b0)
                begin
                        C <= 16'b0000000000000000;
                end
        else
                begin
                        C <= C + 1'b1;
                end
end

always @(posedge clkfast)
begin
        if (C == 16'b0000000000000010)
                begin
                        VoutF_reg <= VoutF_reg + 1'b1;
                end
        if (sh_old == 1'b1 && sh == 1'b0)
                begin
                        count <= VoutF_reg;
                end
        if (sh_old == 1'b0 && sh == 1'b1)
                begin
                        VoutF_reg <= 10'b0000000000;
                end
        sh_old <= sh;
end
endmodule
```

Appendix D

PCB design

We describe the PCB design in nine parts: the main chip, voltage supply, current supply, source follower supply, excitation signal generation, threshold-level generation, output DC-level generation, buffer stage, FPGA board connector.

D.1 Chip ‘Ring-down’

The 24-pin chip is shown in figure D1, 22 pins are used.

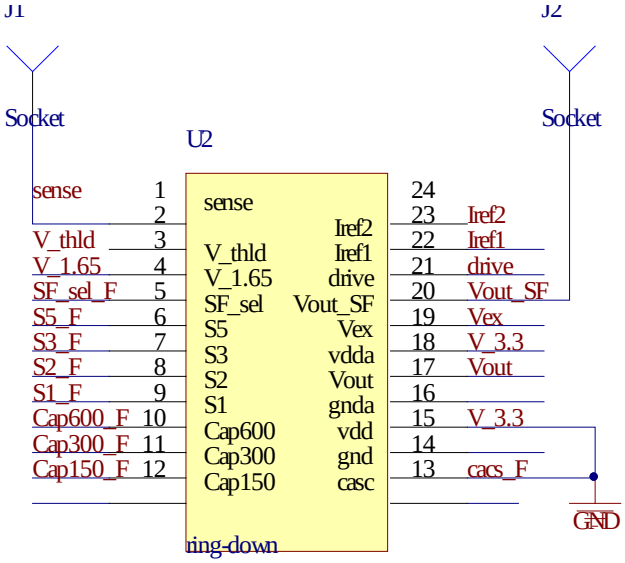

Fig. D1: Chip ‘ring-down’

The ‘sense’ and ‘drive’ pin of the chip are designed to connect both sides of the resonator. In this PCB design, we connect these two nodes to two sockets, which can be wired up to the resonator during the measurement. The ‘sense’ pin is the virtual ground of the integrator (Fig. 3-8), which is very sensitive to any DC leaking path. To avoid leakage currents to neighboring pins in the ceramic package, we make both sides of the sense line

unused. We connect pin 2 and pin 24, together with the package house, to a bias voltage generated on the PCB that is made approximately equal to the DC bias voltage ($V_{0.55}$) at the virual ground of the integrator.
Table D1 lists the description of the 22 pins:

Table D1: Pin description (the pin names in PCB schematic is different from the main text of this report)

Pin number	Name	Description
1	sense	Connect the resonator to the integrator
21	drive	Connect the resonator to the driving source
3	V_thld	Threshold-level (programmable)
4	V_1.65	Output DC-level
18	Vex	Driving source
17	Vout	The output signal of the comparator
20	Vout_SF	The output signal of the integrator (buffer)
15	vdd	3.3V supply for the main circuit
18	vdda	3.3V supply for the inverter bank
22	Iref1	DC current supply of the integrator
23	Iref2	DC current supply of the comparator
6,7,8,9	S1,2,3,5	Control signals for switch 1,2,3,4 and 5
5	SF_sel	Control signal to select the source follower
10,11,12	Cap150,300,600	Control signal to select the feedback capacitor
13	casc	Control signal to select the cascade supply

D.2 Voltage supply circuit

Voltage supply circuit generates three voltage levels: 3.3V, 5V and -5V. The chip is working under 3.3V supply, while 5V and -5V give supply voltages for other components on the PCB.
We use three voltage regulators to generate these voltage levels. Table D2 shows the components we choose:

Table D2: Components used in voltage supply part

Voltage level	Voltage regulator
3.3V	TPS76933
5V	TL750L
-5V	MC79L05ACPG

The circuit for voltage supply part is displayed in figure D2.

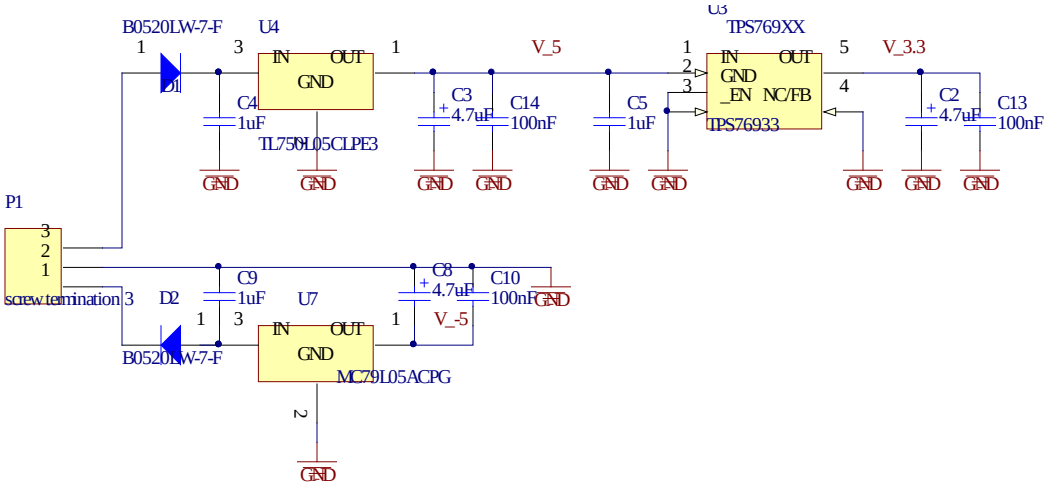

Fig. D2: Voltage supply circuit

The screw termination P1 connects with external positive, negative voltage supplies and ground. The two diodes are used here to make sure the current flow in the correct direction for PCB protection purpose. For each regulator, a 1µF input bypass capacitor, connected between IN and GND and located close to the regulator, is implemented to improve transient response and noise rejection. Also, two output bypass capacitors with the value of 4.7µF and 100nF are used between OUT and GND to decouple both low frequency and high frequency AC single from power supply.

D.3 Current supply circuit

Current supply circuit provides around 1µA DC current supplies for the current mirrors of the integrator and the comparator. The circuit is depicted in figure D3.

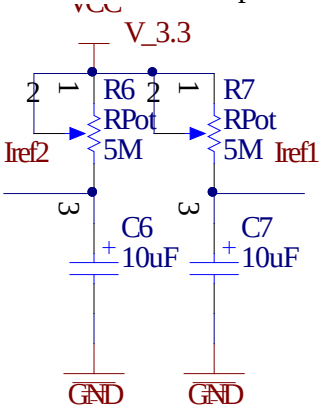

Fig. D3: Current supply circuit

To generate DC current, Ohm's law is applied. A 3.3V DC voltage supply is used across a 3.3MΩ resistance to produce the needed current. In order to slightly change the current supply during measurement, we choose a 5MΩ potentiometer for the resistor. Furthermore, a 10µF bypass capacitor is also implemented for decoupling.

D.4 Source follower supply

As described before, the source follower is used to read-out the ring-down signal. The power supply circuit of the source follower is given in this part (Fig.D4).

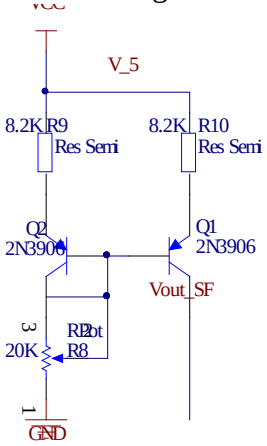

Fig. D4: Source follower supply circuit

We use a PNP current mirror to implement the circuit. 5V supply is applied to obtain enough output swing. Since the minimum needed current is around 120μA, we choose 8.2kΩresistor together with a 20kΩ potentiometer to give a flexible supply.
We choose the most commonly used component '2N3906' for both PNP transistors.

D.5 Excitation signal generation

We analyze this part in section 4.1. We choose 20MHz gain-bandwidth amplifier (OPA2604) for the 2MHz input signal.
The schematic of PCB design is illustrated in figure D5.

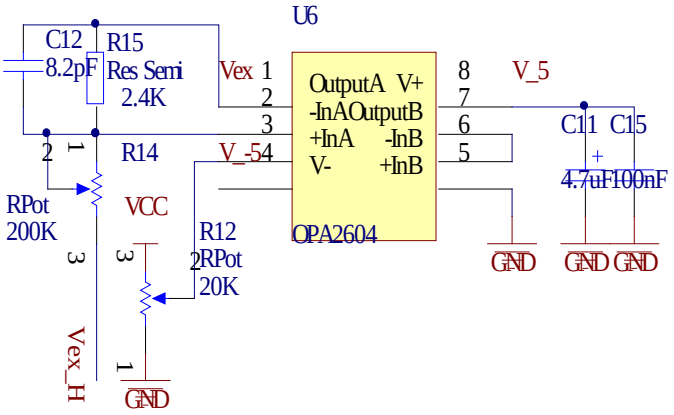

Fig. D5: Excitation signal generation circuit

The OP AMP is +5V and -5V dual supply, so the excitation signal is able to have 0V or negative DC level.

D.6 Threshold Voltage Generation

We analyze this part in section 4.1. The PCB schematic circuit is shown in figure D6.

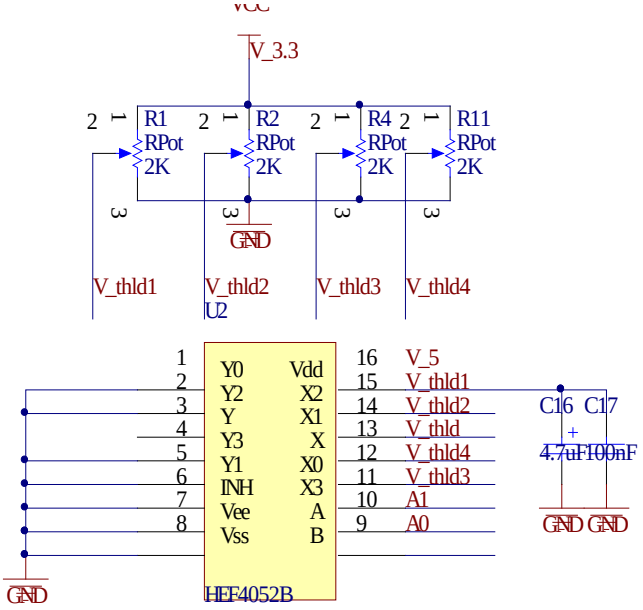

Fig. D6: Threshold voltage generation circuit

Our choice for the multiplexer is the most commonly used chip ‘HEF4205B’. ‘A0’ and ‘A1’ are control signals, which generated by FPGA development board.

D.7 Output DC-Level Generation

We use a simple resistor divider in this part (Fig. D7).

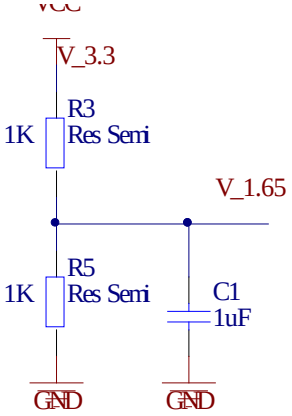

Fig. D7: Output DC-level generation circuit

Two resistors with the same value divide the 3.3V supply into half. A 1µF bypass capacitor is used here for decoupling.

D.8 Buffer Stage

A two-inverter buffer stage is used between the digital part and the analog part for output signal and excitation signal. We choose most commonly used chip '74HC14N' to provide buffers with Schmitt-trigger action and transform the slowly changing signals into sharply defined, jitter-free signals. The schematic is depicted in figure D8.

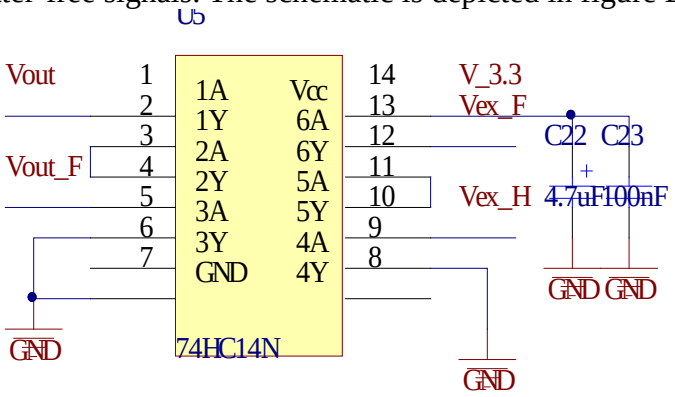

Fig. D8: Schematic of the buffer stage

In the above figure, 'Vout' is the output signal of the comparator, and the clean signal 'Vout_F' connects with FPGA connector, used as the input signal of frequency counting. 'Vex_F' is the excitation signal generated by FPGA, while 'Vex_H' used as input signal ($V_{dr(3.3V)}$) of the circuit of figure 4-5.

D.9 FPGA board connector

The FPGA development board provides two, 40-pin expansion headers. To make our life easy, we use the same 40-pin header on the PCB board (Fig. D9).

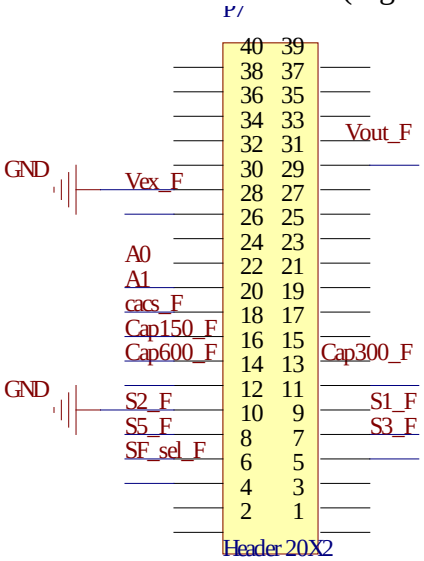

Fig. D9: Schematic of the FPGA board connector

All the control signals provided by FPGA board have 3.3V DC level, which can be directly applied to the 'ring-down' chip.

D.10 Whole System

Figure D10 demonstrates the compete schematic of the PCB design.

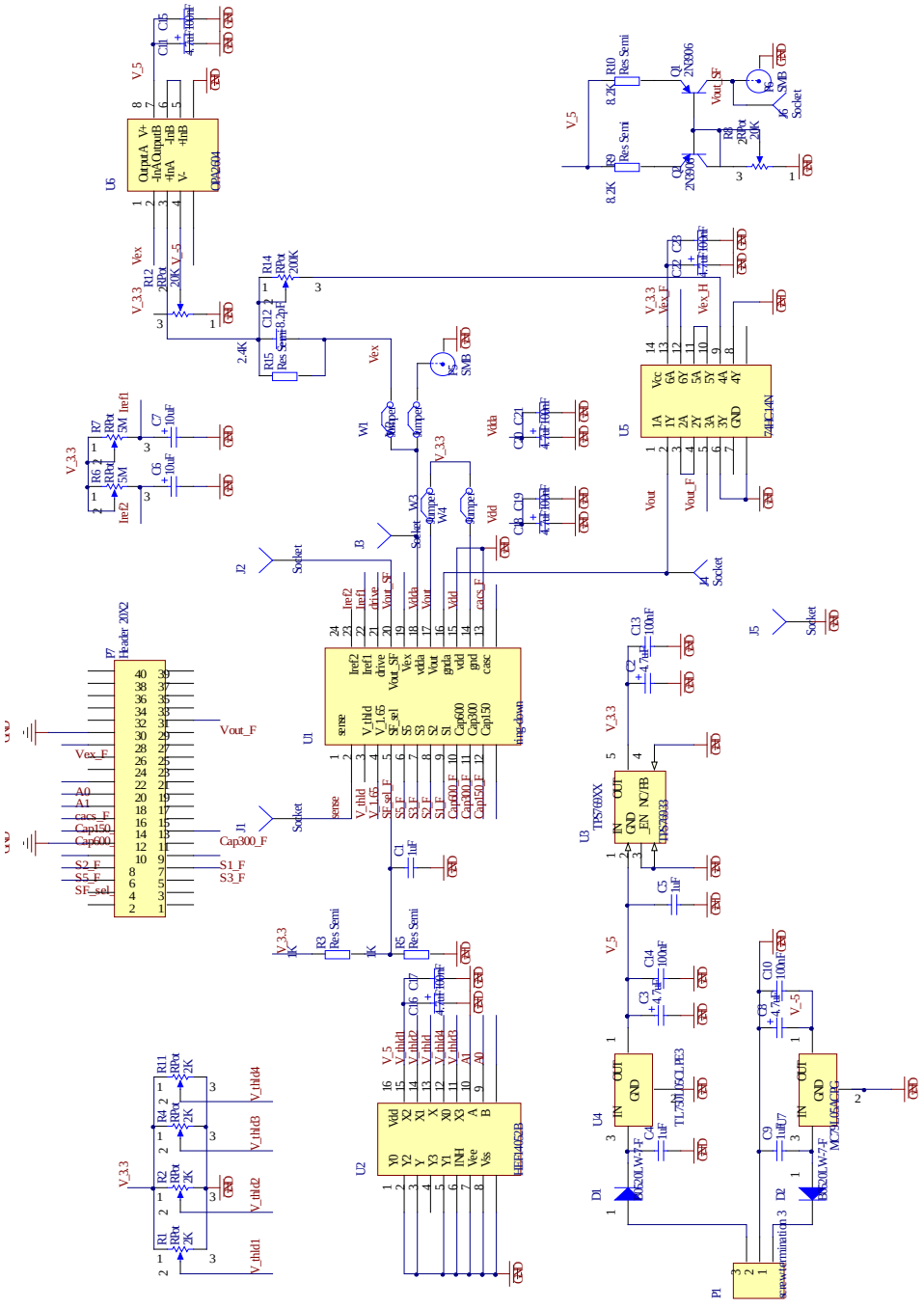

Fig. D10: PCB schematic

Figure D11 demonstrates the compete layout of the PCB design.

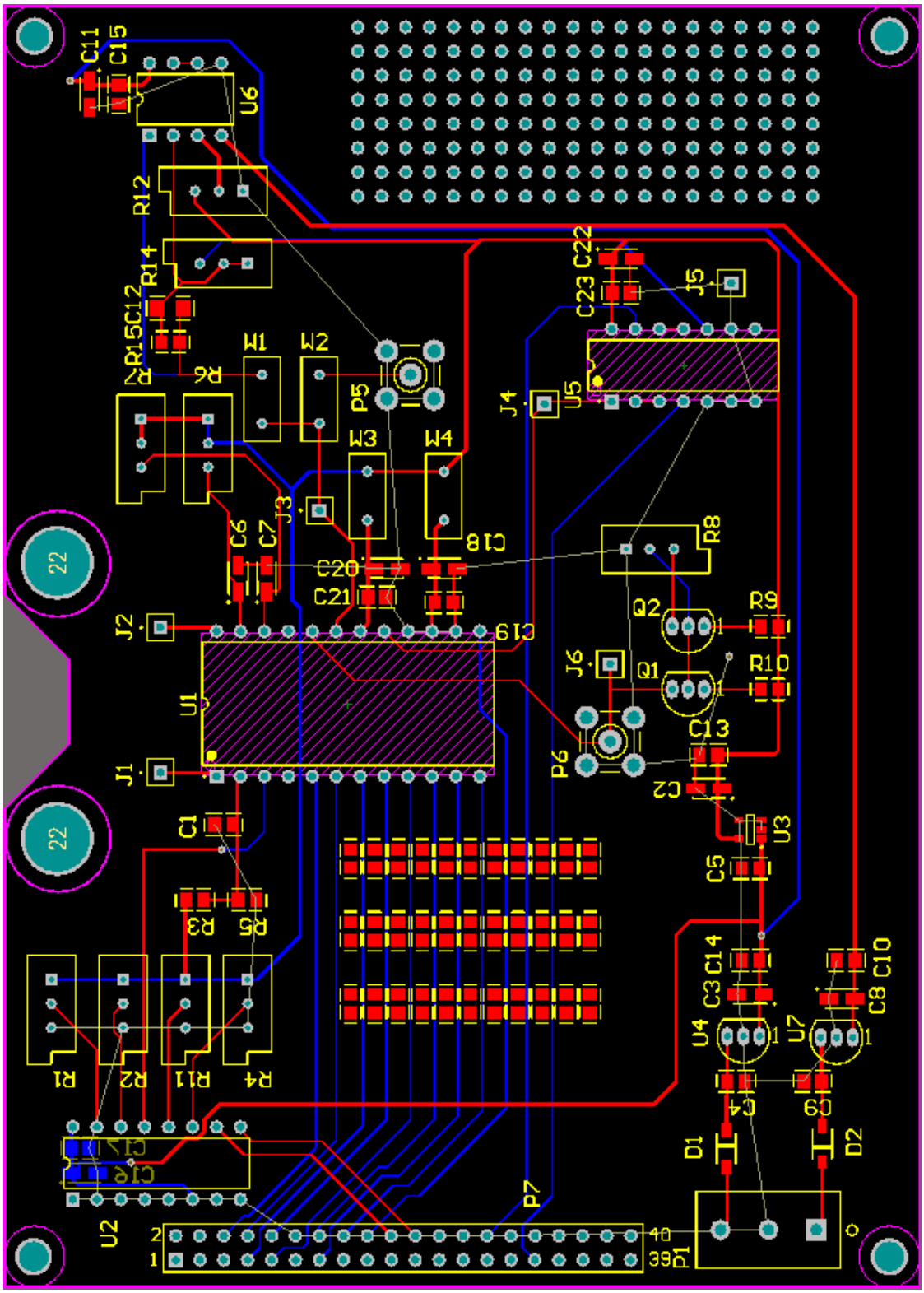

Fig. D11: PCB layout