12

Integrated MEMS: Opportunities & Challenges

P.J. French and P.M. Sarro
Delft University of Technology,
The Netherlands

1. Introduction

For almost 50 years, silicon sensors and actuators have been on the market. Early devices were simple stand-alone sensors and some had wide commercial success. There have been many examples of success stories for simple silicon sensors, such as the Hall plate and photo-diode. The development of micromachining techniques brought pressure sensors and accelerometers into the market and later the gyroscope. To achieve the mass market the devices had to be cheap and reliable. Integration can potentially reduce the cost of the system so long as the process yield is high enough and the devices can be packaged. The main approaches are; full integration (system-on-a-chip), hybrid (system-in-a-package) or in some cases separate sensors. The last can be the case when the environment is unsuitable for the electronics. The critical issues are reliability and packaging if these devices are to find the applications. This chapter examines the development of the technologies, some of the success stories and the opportunities for integrated Microsystems as well as the potential problems and applications where integration is not the best option.

The field of sensors can be traced back for thousands of years. From the moment that humans needed to augment their own sensors, the era of measurement and instrumentation was born. The Indus Valley civilisation (3000-1500 BC), which is now mainly in Pakistan, developed a standardisation of weight and measures, which led to further developments in instrumentation and sensors. The definition of units and knowing what we are measuring are essential components for sensors. Also if we are to calibrate, we need a reference on which everyone is agreed.

When we think of sensors, we think in terms of 6 signal domains, and in general converting the signal into the electrical domain. The electrical domain is also one of the 6 domains. The signal domain is not always direct, since some sensors use another domain to measure. A thermal flow sensor is such an example, and these devices are known as "tandem sensors". The signal domains are illustrated in Figure 1.

Over the centuries many discoveries led to the potential for sensor development. However, up to the 2nd half of the 20th century sensor technology did not use silicon. Also some effects in silicon were known, this had not led to silicon sensors. The piezoresistive effect was discovered by Kelvin in the 19th century and the effect of stress on crystals was widely studied in the 1930s, but the measurement of piezoresistive coefficients made by Smith in 1954, showed that silicon and germanium could be good options for stress/strain sensors (Smith, 1954). Many other examples can be found of effects which were discovered and a century later found to be applicable in silicon.

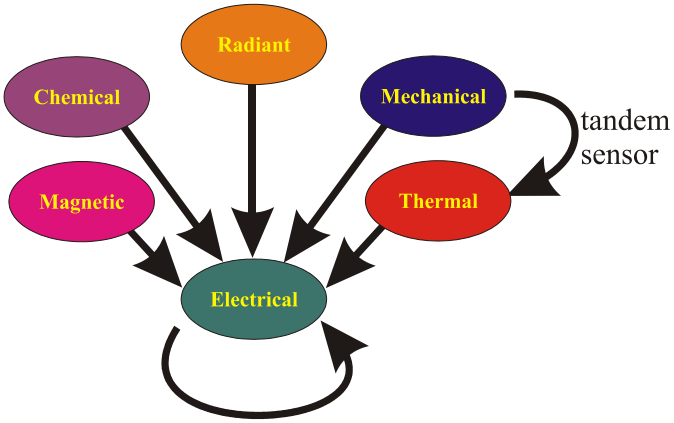

Fig. 1. The six signal domains

An important step towards The beginnings of integrated sensors go back to the first transistor, invented in 1947 by William Shockley, John Bardeen and Walter Brattain, while working at Bell Labs., which was fabricated in germanium. This quickly led to thoughts of integrating more devices into a single piece of semiconductor. In 1949 Werner Jacobi working at Siemens filed a patent for an integrated-circuit-like semiconductor amplifying device (Jacobi, 1949). In 1956 Geoffrey Dummer, in the UK, tried to make a full IC but this attempt was unsuccessful. In 1958 Jack Kilby, from Texas Instruments made the first working IC in germanium (Texas Instruments, 2008). This first device is illustrated in Figure 2. Six months later Robert Noyce, from Fairchild Semiconductor came up with hi own IC in silicon and manage to address a number of practical problems faced by Kilby. From these simple beginnings has come a major industry worth billions. John Bardeen, Walter H. Brattain and William B. Shockley won the Nobel Prize in 1956 and Jack Kilby in 2000.

Fig. 2. First working IC

The discovery of sensing effects in silicon and the development of electronic devices in silicon led to many new sensor developments. In the 1950s the idea of p-n junctions for photocells was first investigated (Chapin, 1954). Staying within the radiation domain groups

is Philips and Bell Labs. worked in parallel to develop the first CCD devices (Sangster, 1959 & Boyle, 1970).
At Philips, in the Netherlands, work had begun on a silicon pressure sensor and this early micromachined sensor is given in Figure 3 (Gieles, 1968 & 1969). The membrane was made using spark erosion and chemical etching, but the breakthrough was that the whole structure was in one material and therefore thermal mismatches were avoided.

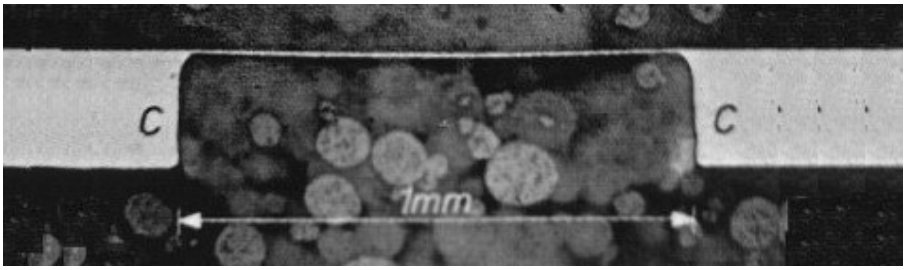

Fig. 3. Early pressure sensor in the early 1960's

Silicon had now been shown to be a material with many effects interesting for sensor development. The work of Gieles showed that the material could be machined. Work from Bean (Bean, 1978) showed the greater opportunities etching silicon with anisotropic etchants, and Petersen (Petersen, 1982) showed the great mechanical properties of silicon. The early days of IC and sensor development were quite separate, but time has shown that these two fields can benefit from each other leading to new devices with greater functionality.

2. Technology

Many of the technologies used in silicon sensors were developed for the IC industry, although the development of micromachining led to a new range of technologies and opportunities for new devices. IC technology is basically a planar technology, whereas micromachining often requires working in 3 dimensions which has presented new challenges, in particular when the two technologies were combined to make smart devices.

2.1 Planar IC technology

The basis of planar technology was developed in the 1940s with the development of a pn-junction, although the major breakthrough was in 1958 with the first IC. This development enabled more and more devices to be integrated into a single piece of material. IC processing can be seen as a series of steps including; patterning, oxidation, doping, etching and deposition. These have been developed over the decades to optimise for the IC requirements and to advance the devices themselves. The following sections will give a brief description of the main steps.

2.1.1 Lithography

Lithography is a basic step carried out a number of times during a process. Basically a resist layer is spun on to the wafer and, after curing, exposed to UV light through a mask. If we use positive resist, this will soften through exposure and negative resist will harden. This

can be done using a stepper (which projects the image onto each chip and steps over the wafer) or a contact aligner where the mask is a 1:1 image of the whole wafer. There are also techniques such as e-beam and laser direct write.

2.1.2 Oxidation and deposition

Silicon oxidises very easily. Simply left exposed at room temperature and oxide layer of 15-20Å will be formed. For thicker oxides the wafer is exposed to an oxygen atmosphere at temperatures between 700-1200^{o}C. For thick oxides, moisture is added (wet oxidation) to increase the growth rate.

A number of deposition steps are used in standard processing. The first of these is epitaxy. Epitaxy is the deposition, using chemical vapour deposition (CVD), of a thick silicon layer, usually single crystal, although polycrystalline material can also be deposited in an epi-reactor (Gennissen, 1997). The second group of depositions are low pressure CVD (LPCVD) and plasma enhanced CVD (PECVD). Some examples of LPCVD processes are given in Table 1. PECVD uses similar gasses, but the use of a plasma reduces the temperature at which the gasses break down, which is of particular interest with post-processing, where thermal budget is limited (Table 2). The temperatures for PECVD can be reduced through adjusting other process parameters. These are only examples and there are many other options.

Layer	Gasses	Temperature
Polysilicon	SiH_4	550^{o}C-700^{o}C
Silicon nitride	$SiH_2Cl_2 + NH_3$	750^{o}C-900^{o}C
	$SiH_4 + NH_3$	700^{o}C-800^{o}C
Silicon dioxide undoped	SiH_4+O_2	400^{o}C-500^{o}C
PSG (phosphorus doped)	$SiH_4+O_2+PH_3$	400^{o}C-500^{o}C
BSG (boron doped)	$SiH_4+O_2+BCl_3$	400^{o}C-500^{o}C
BPSG (phosphorus/boron doped)	$SiH_4+O_2+PH_3+BCl_3$	400^{o}C-500^{o}C
Silicon carbide	$SiH_4+ CH_4$	900^{o}C-1050^{o}C

Table 1. Examples of LPCVD processes.

Layer	Gasses	Temperature
a-Si	SiH_4	400^{o}C
Silicon nitride	$SiH_4 + NH_3 + N_2$	400^{o}C
Silicon dioxide undoped	$SiH_4+ N_2 + N_2O$	400^{o}C
Silicon dioxide, (TEOS)	$TEOS+O_2$	350^{o}C
Oxynitride	$SiH_4+ N_2 + N_2O + NH_3$	400^{o}C
BPSG (phosphorus/boron doped)	$SiH_4+ N_2 + N_2O + PH_3 + B_2H_6$	400^{o}C
	$SiH_4+ CH_4$	
Silicon carbide		400^{o}C

Table 2. Examples of PECVD processes.

The last of the deposition processes is the metallisation, which is usually done by sputtering or evaporation, which is widely used for metals.

2.1.3 Doping

An essential part of making devices is to be able to make p and n type regions. The main dopants are: As, P and Sb for n-type material and B for p-type material. The main techniques to dope silicon are diffusion and implantation. Diffusion is a process where the wafer is exposed to a gas containing the dopant atoms at high temperature. Implantation is a process in which the ions are accelerated towards the wafer at high speed to implant into the material.

2.1.4 Etching

Etching can be divided into two groups, wet and dry. Standard wet etching, in standard IC processing, is used for etching a wide range of materials. However, in recent years, dry etching is also widely used. Commonly used wet etchants are given in Table 3.

Etchant	Target		Target
49% HF	SiO_2	Si etch (85%, 160°C) 126 HNO_3; 60 H_20; 5NH_4F	Si
5:1 BHF	SiO_2		
		Aluminium etch	Al
Phosphoric acid	SiN	16H_3PO_4; HNO_3; 1Hac; 2H_20; (50°C)	

Table 3. Commonly used wet etchants.

3. Micromachining technologies

Micromachining technologies moved the planar technology for IC processing into the 3rd dimension. These technologies can be divided into two main groups, bulk micromachining and surface micromachining. In addition there is epi-micromachining which is a variation on the surface micromachining. The following sections give a brief outline of these technologies. A more detailed description can be found in the chapter on micromachining.

3.1 Bulk micromachining

Bulk micromachining can be divided into two main groups: wet and dry. There are also other techniques such as laser drilling and sand blasting. The first to be developed was wet etching. Most wet micromachining processes use anisotropic, such as KOH, TMAH, hydrazine or EDP. These etchants have an etch rate dependant upon the crystal orientation allowing well defined mechanical structures (Bean, 1978). The basic structures made with these etchants are given in Figure 4 with their properties in Table 4.

All of these processes are relatively low temperature and can therefore be used as post-processing after IC processing, although care should be taken to protect the frontside of the wafer during etching.

Bulk micromachining can also be achieved through electrochemical etching in HF. For this etchant there are two distinct structures. The first is micro/nano porous which is usually an isotropic process, or macro-porous which is an anisotropic process. The micro/nano pore structure can be easily removed due to its large surface area to leave free-standing structures (Gennissen, 1995). Porous silicon/silicon carbide can then be used as a sensor material such as humidity or ammonia sensors (O' Halloran, 1998, Connolly 2002).

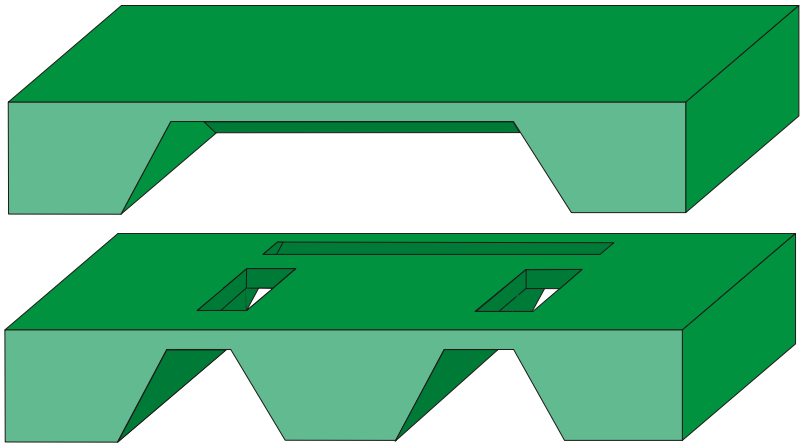

Fig. 4. Basic bulk micromachined structures using wet anisotropic etchants.

Etchant	Mask	Etch rate			Comments
		(100) μm/min (100/(111)	SiO_2 [Å/h]	SiN [Å/h]	
Hydrazine	SiO_2, SiN Metals	0.5-3 16:1	100	<<100	Toxic, potentially explosive
EDP	Au, Cr, Ag, Ta, SiO_2, SiN	0.3-1.5	120	60	Toxic
KOH	SiN, Au	0.5-2, up to 200:1	1700-3600	<10	Not cleanroom compatible
TMAH+ IPA	SiO_2, SiN	0.2-1, up to 35:1	<100	<10	Expensive

Table 4. Properties of main anisotropic etchants

The formation of macroporous silicon is usually done using n-type material and illumination from the backside to achieve deep holes with high aspect ratio. The idea was first proposed by (Lehmann 1996) and has been used to make large capacitors (Roozeboom, 2001) and micromachined structure (Ohji 1999). Both of these structures are illustrated in Figure 5.

The macro-porous process usually requires low n-doped material and illumination from the backside, which may not be compatible with the IC process. However, some macro-porous etching has been achieved in p-type material (Ohji, 2000), although the process is more difficult to control.

Deep reactive ion etching (DRIE), addressed some of the limitations of wet etching, although the process is more expensive. Two main processes are cryogenic (Craciun 2001) and Bosch processes (Laemer 1999). The cryogenic process works at about –100^{o}C and uses oxygen to passivation of the sidewall during etching to maintain vertical etching. The Bosch process uses a switching between isotropic etching, passivation and ion bombardment. This results in a rippled sidewall, although recent developments allow faster switching without losing etch-rate, thus significantly reducing the ripples. The etching can be performed from both front and back-side and can be combined with the electronics. In addition to DRIE being used for making 3-D mechanical structures, it has been applied to packaging (Roozeboom 2008).

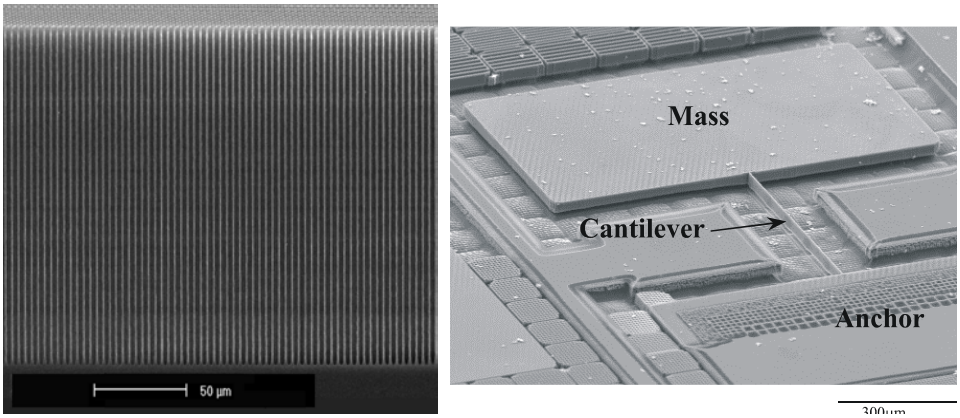

Fig. 5. (left) vertical holes using macro-porous techniques (reproduced with kind permission Fred Roozeboom Philips), and (right) free standing structure (Ohji).

3.2 Surface micromachining

Surface micromachining is quite different from bulk micromachining both in terms of processing steps and dimensions. Basically, this involves the deposition of thin films and selective removal to yield free standing structures. The basic process is given in Figure 6, although this can be augmented with additional sacrificial and mechanical layers.

There are many possible combinations of sacrificial and mechanical layers and a few examples are given in Table 5. It is important with deposited layers to have good stress control, preferably low tensile stress with little or no stress profile (Guckel, 1988, French 1996, 1997, Pakula, 2001). A further important issue when fabricating surface micromachined structures is the release while avoiding stiction. Techniques to achieve this include freeze-drying, super critical drying. Alternatively, vapour-etching has been applied, or dry etching of a sacrificial polymer layer.

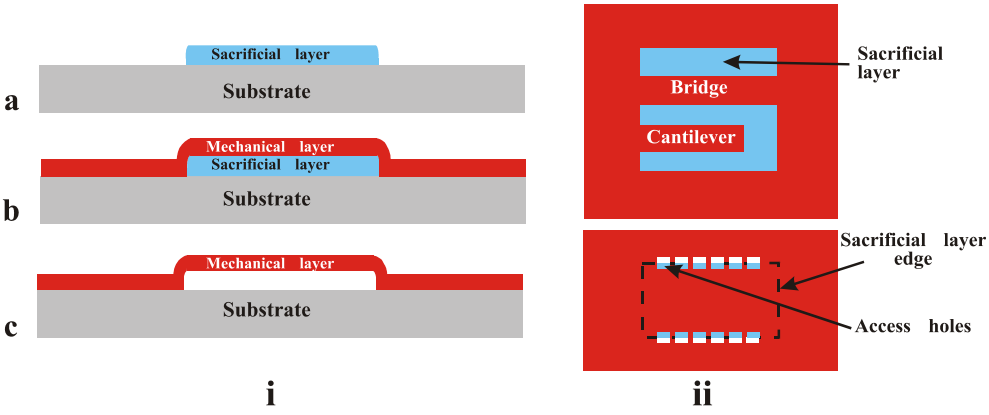

Fig. 6. Basic Surface micromachining process, (ia) deposition and patterning of sacrificial layer, (ib) deposition and patterning of mechanical layer and (ic) sacrificial etching, ii lateral view of typical structures.

Sacrificial layer	Mechanical layer	Sacrificial etchant
Silicon dioxide	Polysilicon, silicon nitride, silicon carbide	HF
Silicon dioxide	Aluminium	Pad etch, 73% HF
Polysilicon	Silicon nitride, silicon carbide	KOH
Polysilicon	Silicon dioxide	TMAH
Resist, polymers	Aluminium, silicon carbide	Acetone, oxygen plasma

Table 5. Examples of combinations of sacrificial and mechanical layers.

3.3 EPI micromachining

Epi-micromachining where the epitaxial layer is used as the mechanical layer. It can be seen as a variation on surface micromachining. There are a number of processes available which are described below.

3.3.1 SIMPLE

The SIMPLE process (Silicon Micromachining by Plasma Etching), forms micromachined structures using a single etch step (Li, 1995). This process makes use of a Cl_2/BCl_3 chemistry which etches low doped material anisotropically and n-type material above a threshold of about $8x10^{19}cm^{-2}$, isotropically. The basic process sequence is shown in Figure 7. The first additional step, to the bipolar process, is a heavily doped buried layer since the bipolar buried layer has a doping level which is too low to be under-etched. This is followed by the formation of the standard bipolar buried layer and epitaxial layer (Figure 7a) followed by an additional deep diffusion where the mechanical structure will be formed (Figure 7b). After this a full standard bipolar process is performed (Figure 7c). The final structure is given in Figure 7d. This shows clearly how the vertical etching continues in the trench during the lateral etching of the buried layer.

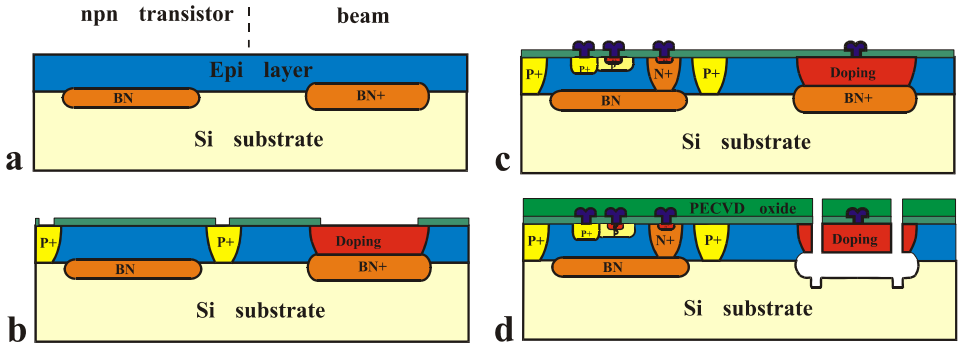

Fig. 7. Main steps for the SIMPLE process.

3.3.2 Silicon on Insulator (SOI)

Silicon-on-insulator wafers are used in standard IC processing, which give a number of opportunities for making mechanical structures. Plasma etching through the epi layer followed by wet etching of the oxide layer is one option. This basic process is given in Figure 8 (Diem, 1995).

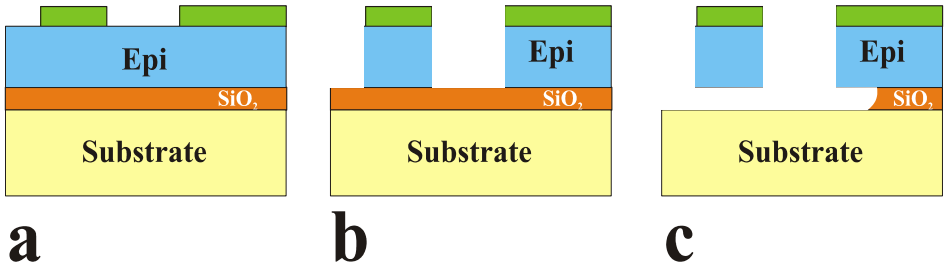

Fig. 8. SIMOX based micromachining

An alternative use of SOI was developed in Twente, The Netherlands, (de Boer, 1995). This process uses different modes of plasma etching to manufacture the free standing structure as shown in Figure 9. First the epi is etched anisotropically, a CHF_3 plasma etch is used to etch the underlying oxide and deposit a fluorocarbon (FC) on the sidewall which protects the sidewall during further etching and also has a low surface tension to reduce sticking. This is followed by a trench floor etch using $SF_6/O_2/CHF_3$. Finally an isotropic RIE etch removes the silicon from under the upper silicon resulting in the free standing structure which is also isolated.

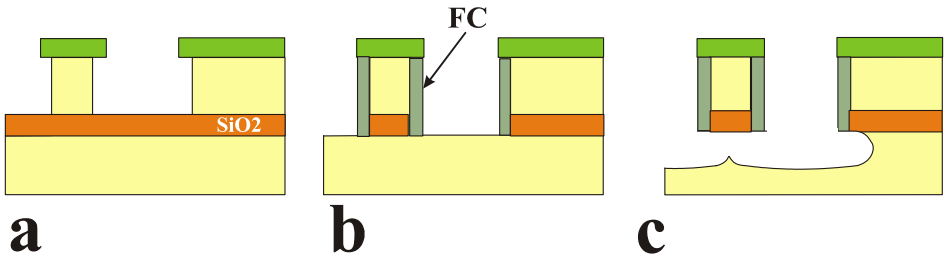

Fig. 9. Basic process steps for making free-standing SOI structures.

3.3.3 Merged Epitaxial lateral Overgrowth (MELO)

The MELO process (Merged Epitaxial lateral Overgrowth) is an extension of selective epitaxial growth SEG. Selective epitaxial growth uses HCl added to the dichlorosilane. The HCl etches the silicon. However, if there is a pattern of bare silicon and silicon dioxide, the silicon deposited on the oxide will have a rough grain like structure, with a large surface area, and will therefore be removed more quickly. Thus, although the growth rate will be lower than a normal deposition, a selective growth can be achieved. Once the silicon layer reaches the level of the oxide, both vertical and lateral growth will occur yielding lateral overgrowth. This basic process is illustrated in Figure 10 (Bartek, 1994).

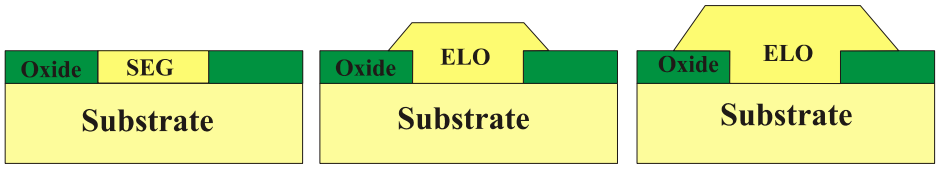

Fig. 10. Basic SEG process extended to ELO

If two of these windows are close enough together they will merge giving the MELO process. As a result we have buried silicon dioxide islands. This lends itself well to micromachining as shown in Figure 11 (Kabir 1993). This process has the advantage of producing single crystal structures, but the disadvantages that beams must be orientated in the <100> direction due to growth mechanisms of silicon (Gennissen, 1999) and since growth continues both laterally and vertically, the lateral dimensions are limited.

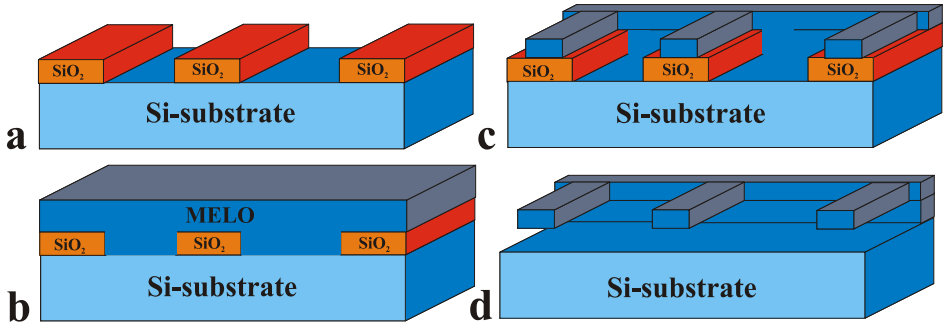

Fig. 11. Basic MELO process.

3.3.4 Sacrificial porous silicon

A process which using silicon as both mechanical and sacrificial layer is the sacrificial porous silicon technique (Lang, 1995, Gennissen, 1995, 1999, Bell, 1996). This process makes use of the fact that, without illumination, p-type material is made porous selectively. The high surface area of the porous materials results in rapid etching, after porous formation, in KOH. This makes the material highly suitable as a sacrificial material. The porous silicon formation rate is highly dependent upon the current density, HF concentration, illumination and the doping in the substrate (Gennissen, 1999). The process sequence is given in Figure 12. In this case the selective etching of p-type material over the n-type epi is used. First a plasma etch is used to etch through the epi-layer to reveal the substrate. The porous layer is then formed and finally removed in KOH at room temperature.

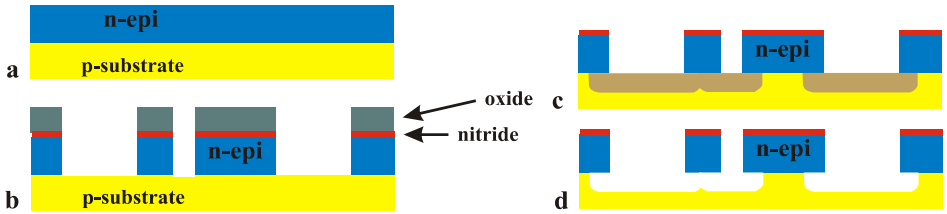

Fig. 12. Basic process steps for sacrificial porous silicon based micromachining

The porous silicon technique is extremely simple and can be applied as a post processing step and it is therefore fully compatible with the electronic circuitry. The only remaining problem is to protect the areas of electronics and metallisation from the HF etchant. One disadvantage of this technique is the added process complexity introduced by the requirement of a backside electrical contact during etching.

3.3.5 Epi-poly

Epi-poly is a polysilicon layers grown in the epitaxial reactor. Although this technique departs from using single crystal silicon as a mechanical material it has greater flexibility in terms of lateral dimensions. Alternatively, the mechanical layers can be formed at the same time as the single crystal epi required for the electronics (Gennissen 1997). The basic process is shown in Figure 13. After the formation of the sacrificial oxide, a polysilicon seed is deposited. A standard epi growth will then form epi-poly on the seed and single crystal where the substrate is bare. The epi growth rate on the polysilicon seed is about 70% of that on the single crystal silicon. Therefore the total thickness of the sacrificial layer and seed can be adjusted to ensure a planar surface after epi growth. A nitride layer is used to stop the polysilicon oxidising during subsequent process, thus minimising intrinsic stress. The mechanical layer is then patterned and released through sacrificial etching as shown in Figure 13d.

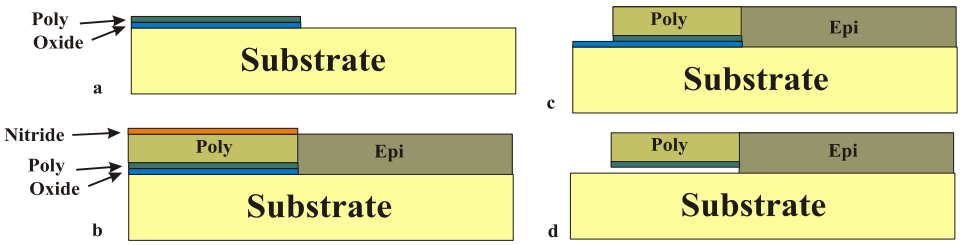

Fig. 13. Basic epi-poly process.

The epi-poly process requires minimal additional processing before epitaxial deposition and no detrimental effect on the electronics' characteristics has been found. The process is therefore fully compatible with the electronics processing.

3.4 Packaging

Packaging for standard ICs has been standardised, but for sensor, many additional challenges can arise and should be considered at an early stage. One of the issues, for example, is that many sensors have to be exposed to the environment. Another issue can be the wire bonding.

3.4.1 Wire bonding

Standard IC processing usually uses wire bonding to make electrical contact from the chip to the outside world. On each chip, metal bond pads are made, and wires (usually gold or aluminium) and made from the pad to the package.

In standard IC, this is all sealed in the package, but if the surface has to be exposed, these wires may not be desired. For example, sensors for catheters may not want bond wires on the front of the chip. In this case through wafer interconnect may be the best option. These options are shown, with the example of a catheter in Figure 14.

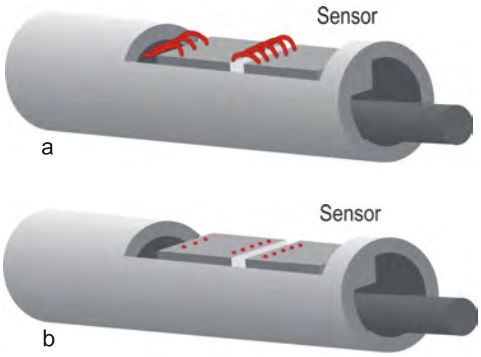

Fig. 14. (a) multi-chip approach using wire bonding, (b) multichip approach using through-wafer-interconnect and a printed circuit board substrate.

3.4.2 Flip-chip

As the field of Microsystems grew, there was more interest in combining different chips in a single package. Wire bonding from chip-to-chip is an option. An alternative is flip-chip. Flip-chip is a process where chips can be mounted. For this process a solder-bump is made on the wafer, after which two chips can be aligned and soldered together. An example of the solder process is given in Figure 15. Adapted from (Fujitsu 2003)

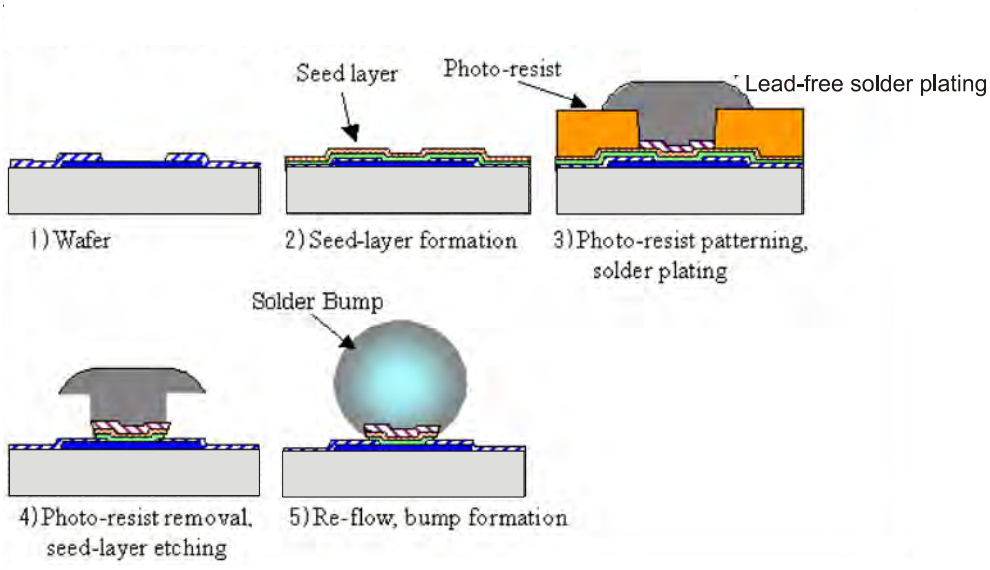

Fig. 15. Example of the Fujitsu solder-bump process.

3.4.3 Multi-chip package

There are a number of options for combining different chips in a single package through flip-chip, through wafer interconnect and simply wire bonding, some of these options , from NXP, The Netherlands, are given in Figure 16 (Roozeboom, 2008-2).

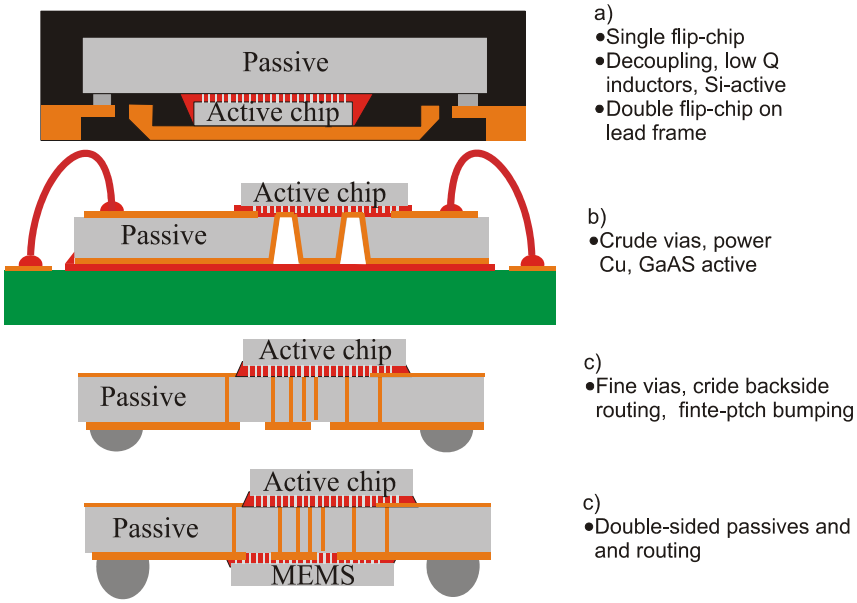

Fig. 16. Different approaches to systems-in-a-package, based on (Roozeboom, 2008-2).

4. Process integration

When deciding how to integrate it is important to choose how this is incorporated in the process. There are a number of options:

Pre-processing (Smith, 1996 – Gianchandani, 1997)

+ No access to process line necessary
+ No thermal limitations for additional processing
- Thermal considerations for additional layers
- Potential contamination problems

Integrated processing (van Drieenhuizen, 1994)

+ Flexibility
- Require access to the clean line
- Limitations on materials

Using existing layers (Fedder, 1996, Hierold, 1996)

+ Simple
- The layers may not optimised for the sensor application

Post-processing (Bustillo, 1994, Pakula 2004)

+ Flexibility in materials used
+ Fewer contamination problems
- Limited thermal budget

With these options there are a number of issues concerning the integration of the sensor structures with the electronics. In many cases the best option is to separate the sensor from electronics and then combining into a single package. The issues for integration are discussed below.

- COMPATIBILITY WITH THE CLEANROOM

Materials or processing steps for the sensor may not be compatible with the cleanroom and therefore cause contamination.

- COMPATIBILITY OF THE PROCESSING

Both ICs and mechanical structures can be very sensitive to any additional thermal process.

- YIELD

A major issue in industrial application is the yield. Standard IC processing has been developed to have a high yield. Any additional processing can potentially reduce yield, which will increase your overall cost.

- APPLICATION ISSUES

High temperatures operations may not benefit from integration. In some applications, the integrated option may be too expensive. In other applications the environment where the sensor has to work, may not be suitable for the electronics. However, if the above issues can be addressed there can be great benefits from integration.

Both surface and bulk micromachining present challenges in terms of integration. The following sections describe a number of integration options.

4.1 Bulk micromachining integration

As shown above there are a number of process technologies, which can be combined with electronics. Bulk micromachining is, in general, low temperature and does not yield any thermal limitations to the electronics. In some DRIE processes charging of the gate oxide can occur, but adjustment of the process can avoid this. With wet etching the main issue is masking/protecting the front side.

Using wet anisotropic etching we require a masking layer on the back of the wafer, which can be a PECVD layer and etching is performed through the wafer to produce, for example, membranes for pressure sensors, or mass/spring structures for accelerometers. One of the issues is how to define the thickness of the membrane. This can be done is several ways (Palik 1982): time stop, p+ etchstop (Gianchandani, 1991), electrochemical etchstop (Kloeck, 1989) and galvanic etchstop (Ashruf 1998 and Connolly 2003).

4.2 Surface micromachining integration

Surface micromachining presents more challenges. Most LPCVD processes use to high a temperature to be suitable as post-processing. However, PECVD processes and metal layers do have a much lower temperature, and can therefore, in principle, be added after IC processing. These options are discussed further below.

4.2.1 Pre-processing

Although described as pre-processing there are usually some processing steps also required after the standard processing. In the case of pre-processing the major consideration is to ensure that the mechanical properties are not detrimentally affected by the standard processing. Polysilicon has been used for pre-processing and this basic structure is given in Figure 17 (Smith 1996, Gianchandani 1997).

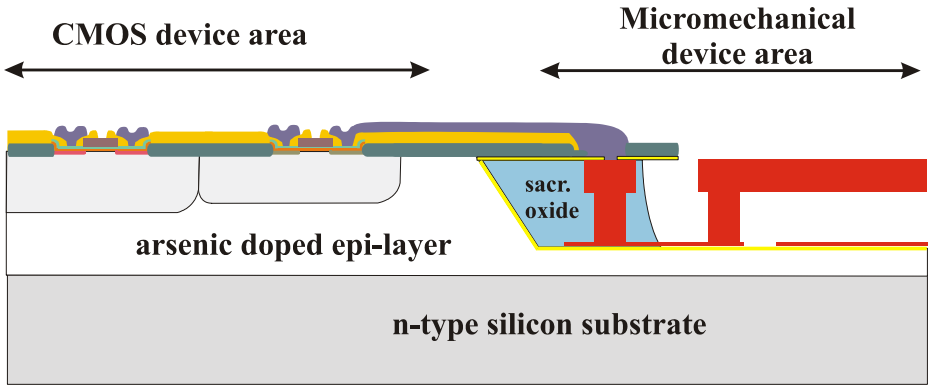

Fig. 17. Structure fabricated using pre-processing combined with CMOS.

4.2.2 Integrated processing

With the integrated process option the wafers are removed from the standard line and after the addition of micromachining steps return to the standard line. The position of the additional process steps is extremely important. In some cases the additional depositions are added after the main thermal processing but before the aluminium. Depending on the sensitivity of the electronics devices to thermal budget, a maximum thermal budget for the micromachining is determined. An example of an integrated process combining polysilicon-based surface micromachining with bipolar electronics is given in Figure 18 (van Drieenhuizen, 1994).

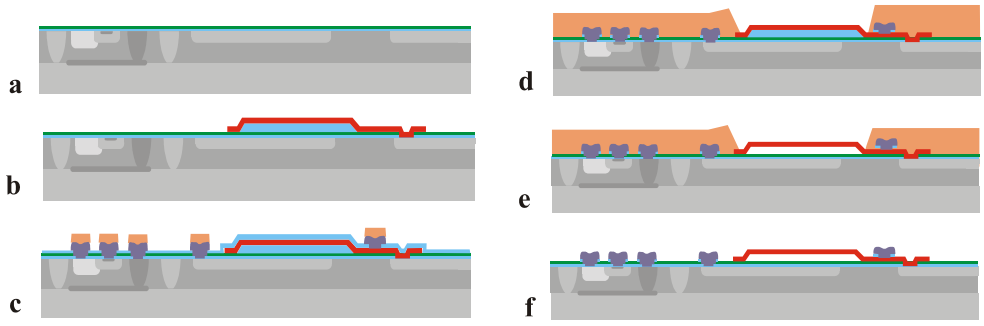

Fig. 18. Polysilicon based integrated surface micromachining process

A similar process has been developed by Fischer et. al. (Fischer, 1996) using an aluminium gate CMOS process. The basic process is shown in Figure 19. The interesting feature of this process is that the deposition of the micromechanical structures is performed before the gate oxidation.

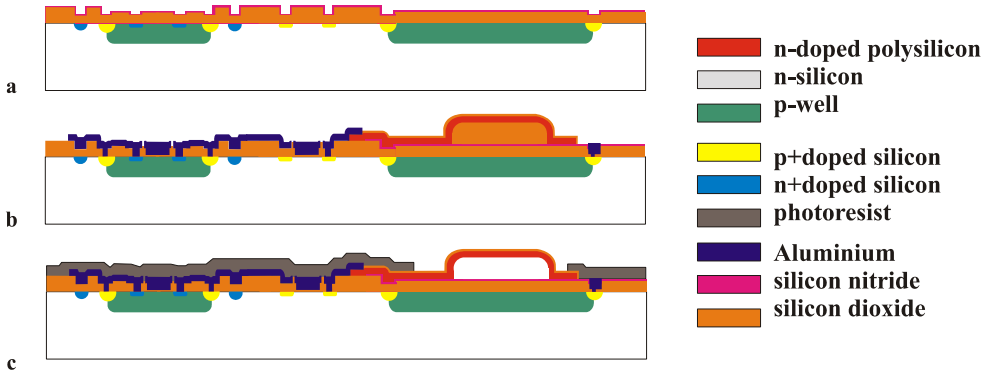

Fig. 19. Compatible surface micromachining process: a) After completion of the CMOS process (before gate oxidation) and capping silicon nitride; b) formation of the sacrificial and mechanical layers followed by gate oxidation and aluminium deposition; c) formation of the resist protection mask and sacrificial etching.

4.2.3 Post-processing

In the post processing option wafers go through the complete standard process. After standard processing either existing layers can be used or additional layers can be added. Both approaches can be found in the literature. Two examples can be seen in Figure 20. The first, Figure 20a uses the gate poly as the mechanical material (Hierold 1996) and the second, Figure 20b, (Fedder, 1996) a combination of oxide and metal used in standard processes.

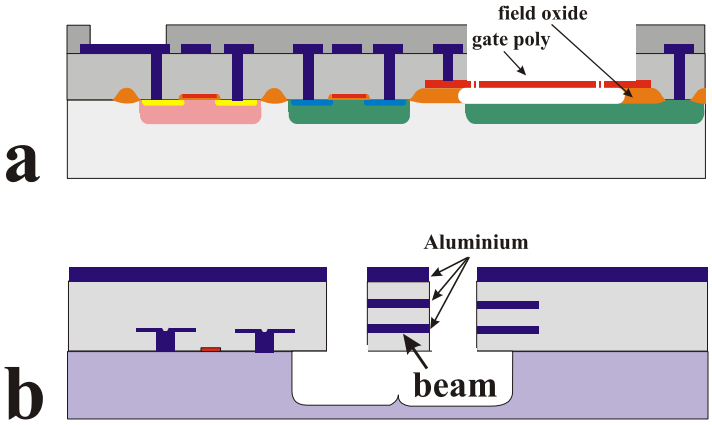

Fig. 20. Post processing micromachining with CMOS (a) using the gate poly and (b) using aluminium and oxide.

An alternative approach is to use one of the aluminium layers as a sacrificial layer, and protecting the remaining aluminium layers with oxide (Westberg, 1996). The resulting structure is shown in Figure 21. These approaches have the advantage of simplicity, but these layers are not optimised for their mechanical properties. The approach is through careful design.

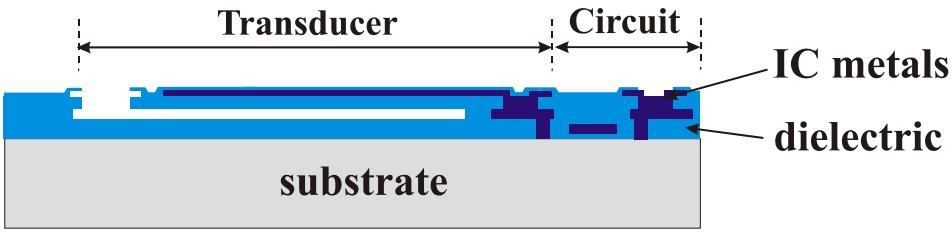

Fig. 21. Micromachining integrated into a CMOS process

One of the limitations of post-processing is the thermal budget. In particular, if aluminium is used for metallization, the maximum temperature that can be used is about 400°C. An alternative is to use another metal. Figure 22 shows an example where tungsten is used as the metal (Bustillo, 1994).

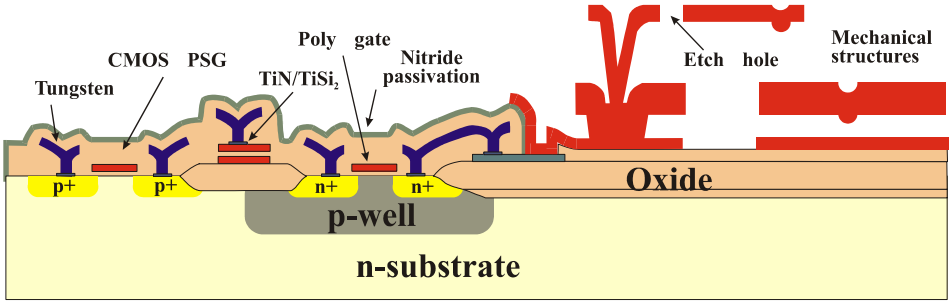

Fig. 22. Post processing micromachining using Tungsten metallisation for the electronics.

Alternatively, low temperature deposition materials, such as PECVD layers can be used. One PECVD layer with good mechanical properties is SiC (Pakula, 2004). With these low temperatures layers such as polyimides (Bagolini, 2002) can be used as sacrificial layer.

4.3 System-in-a-package

In the development of IC the packaging options were wire bonding in a package. This is still used today, but there are many other options. In many applications, the best option is to combine the sensors and the electronics in a single package, but not on a single chip. In this case the sensor can be optimised, without compromising the electronics. Furthermore, the larger production volume of the electronics chip can help to keep costs down. An example of this is given in Figure 23.

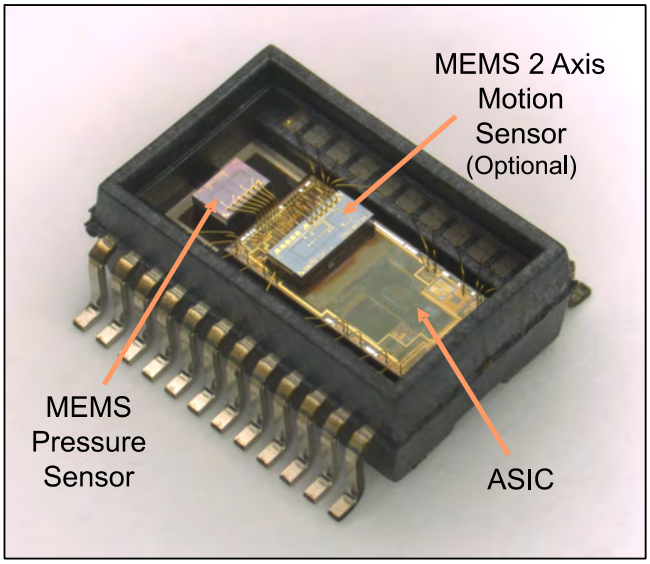

Fig. 23. Tyre Pressure Sensing System developed by LV Sensors integrated ASIC, pressure sensor and 2-axis acceleration sensor (reproduced with kind permission Janusz Bryzek).

The package can then be built into a complete system, as shown in Figure 24.

Fig. 24. Complete system fitted with the valve and a wireless communication system (reproduced with kind permission Janusz Bryzek).

4.4 Integrated sensor

One of the problems in developing a simple electronic compass based on the Hall effect was the offset. This was solved by the development of the "Spinning" Hall plate (Munter, 1990, Bellakom 1994). This technique can reduce the offset by a factor of 1000 to make it practical to be used as a compass. However, in order to make full use of this advantage, the devices should be integrated with a low-offset amplifier. Since the Hall plate only requires a thin diffused layer, this can be integrated with both bipolar and CMOS. This has since become a commercial product developed by Xensor Integration, in Delft. A photograph of this device is given in Figure 25.

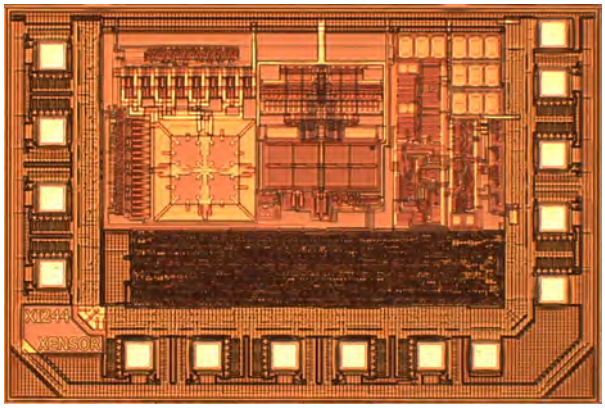

Fig. 25. Single Chip CMOS compatible Compass sensor based on hall technology. The chip incorporates a low-offset Hall sensor with ultra low-noise low offset amplifier, a sigma delta ADC and an SPI digital output. (Courtesy of Xensor Integration, The Netherlands).

Another sensor system which can benefit from integration is the temperature sensor. In this case the sensor can be a simple p-n junction or a transistor and the accuracy can be achieved through the read-out electronics. Furthermore, the electronics can be used to reduce the costs of calibration. A chip photograph of this device is given in Figure 26 (Bakker 1998, 2000, Pertijs 2005).

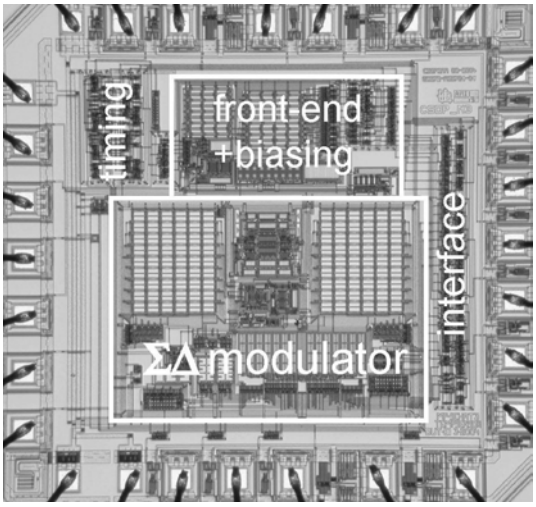

Fig. 26. Chip photograph and block diagram of a smart temperature sensor chip with bus interface.

A further example of sensor integrated is given in Figure 27. The basic sensor, was developed in the 1990s, and is shown on left. The thermopiles used for measuring temperature differences use polysilicon and aluminium. On the right is the integrated version, which contains all power management, read-out and A-D conversion. Although the chip is more expensive, the total system is much cheaper and more efficient.

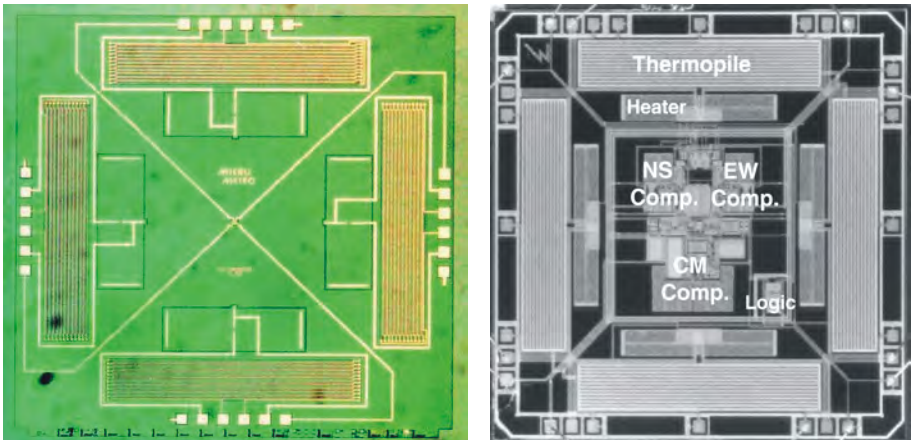

Fig. 27. Two wind-sensors (left) non integrated and (right) fully integrated (Makinwa, 2002).

The examples given above are where using standard processing. There have been many successes by integrating micromachining with electronics on a single chip. An important breakthrough for silicon sensors was with the introduction of integrated silicon accelerometers. Such an example is given in Figure 28. These devices could incorporate self-test and read-out electronics to make a complete system.

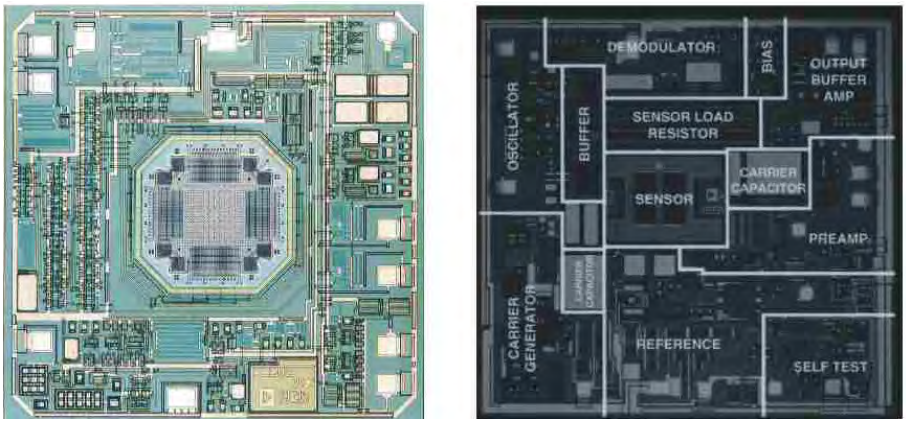

Fig. 28. Analog Devices integrated accelerometer, (left) a 2-D accelerometer, (right) a 1-D device with indication of the different circuitry (Copyright Analog Devices, Inc. All rights reserved).

A further example of a fully integrated device is the TI mirror array which, known at the digital light processor (DLP). This device makes use of the multiple aluminium layers to create the mechanical structure and also the mirrors. This is an excellent example of integrated devices. For this application the reflectivity of the aluminium is essential (Hornbeck, 1996). This device uses three layers of aluminium-based films for the mirror and its suspension system. The build up of the device is illustrated in Figure 29.

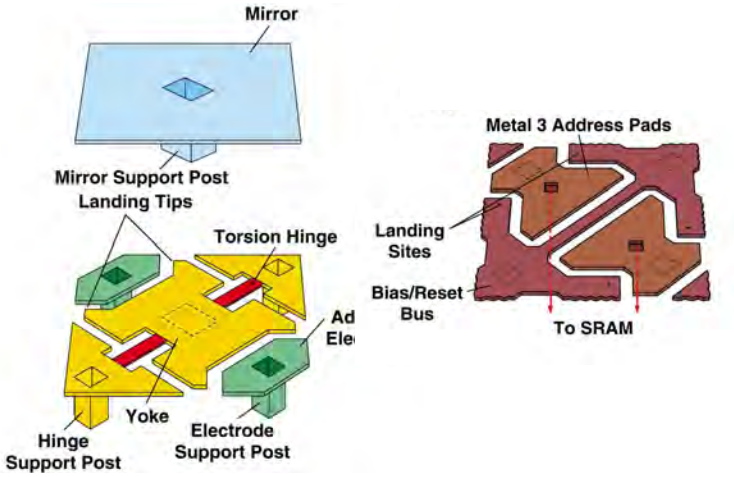

Fig. 29. Schematic of the TI digital display device (from http://www.dlp.com/).

5. Conclusions

There is no simple answer whether or not to integrate, for all applications. In many applications, the best option is system-in-a-package, in others it is better to move the electronics further away to protect it from the environment (in particular with high temperature applications). Another issue which may work against integration is potential increase in costs, through the more complex processing. In these cases the multi-chip approach is used. There are, however, examples where great benefits can be gained from integrating the sensor with the electronics, and a number of examples are given in this chapter. There is no simple answer to all applications and each case needs to be examined in its own right to decide the best path.

6. Acknowledgments

The author would like to thank the many colleagues who have provided pictures included in this chapter. Also the Technology Foundation STW, in The Netherlands, for their funding of work in Delft and their general support for Applied Research in The Netherlands. Last, but not least, colleagues in DIMES for their collaboration over the years.

7. References

Ashruf, CMA, French, PJ, Bressers, PMMC, Sarro, PM and Kelly, JJ, (1998), *A new contactless electrochemical etch-stop based on gold/silicon/TMAH galvanic cell*, Sensors & Actuators Vol A66 pp 284-291.

Bagolini, A, Pakula, L, Schotes, TLM, Pham, HTM, French, PJ and Sarro, PM, (2002) *Polyimide sacrificial layer and novel materials for post-processing surface micromachining*, J. Micromech. Microeng., Vol 12, pp 390-394.

Bakker, A and Huijsing, JH., (1998). *CMOS smart temperature sensor with uncalibrated 1oC accuracy*, Proceedings ProRISC, 26–27 November 1998, Mierlo, The Netherlands, pp. 19–22.

Bakker, A, (2000) *High-accuracy CMOS smart temperature sensors,* PhD thesis, TU Delft, The Netherlands, 2000, 132 p. ISBN: 90-901-3643-6.

Bartek, M. Gennissen, PTJ, Sarro, PM, French, PJ and Wolffenbuttel, RF, (1994) *An integrated silicon colour sensor using selective epitaxial growth* Sensors and Actuators, Vol A41-42, pp 123-128.

Bean, KE., (1978) *Anisotropic etching of silicon*, IEEE Trans Electron Devices, Vol ED-25, pp 1185-1193

T.E. Bell, TE, Gennissen, PTJ, de Munter, D and Kuhl, M (1996) *Porous silicon as a sacrificial material*, J. Micromech. Microeng., Vol 6, pp 361-369.

Bellekom, AA., and Munter, PJA, (1994) *Offset reduction in spnning-current Hall plates*, Sensors Mater., Vol 5, pp 253-263.

Boyle, WS. & Smith, GE. (1970) *Charge coupled semiconductor devices*, Bell Syst. Techn. J., Vol 49 pp 587- 593

Bustillo, JM, Fedder, GK, Nguyen CT-C and Howe, RT, (1994) *Process technology for the modular integration of CMOS and polysilicon microstructures*, Microsystem Technology, Vol 1, pp 30-41.

Chapin, DM., Fuller, CS. and Pearson, GL. (1954), *A new silicon p-n junction photocell for converting solar radiation into electrical power,* J. Appl. Phys. Vol 25, pp 676-677.

Connolly, EJ, O'Halloran, GM, Pham, HTM, Sarro, PM, French,PJ (2002). *Comparison of porous silicon, porous polysilicon and porous silicon carbide as materials for humidity sensing applications*, Sensors and Actuators Vol A 99 pp 25-30.

Connolly, EJ, Sakarya, S, French, PJ, Xia, XH and Kelly, JJ (2003) *A practical galvanic etch-stop in KOH using sodium hypochlorite*, Proceedings IEEE MEMS 2003, Kyoto, Japan, January 2003, pp 566-569.

Craciun, G, Blauw, M, van der Drift E and French, PJ, (2001) *Aspect ratio and crystallographic orientation dependence in deep dry silicon etching at cyrogenic temperatures,* Proceedings Transducers 01, Munich Germany, June 2001,

de Boer, M, Jansen, H and Elwenspoek, M, (1995), *Black silicon V: A study of the fabricating of moveable structures for micro electromechanical systems*, Proceedings Transducers 95, Stockholm, Sweden, pp 565-568.

Diem, B, Rey, P, Renard, S, Viollet Bosson, S, Bono, H, Michel, F, Delaye, MT and Delapierre, G, (1995) SOI 'SIMOX' from bulk to surface micromachining, a new age for silicon sensors and actuators, Sensors and Actuators, VolA46-47, pp 8-26

Fedder, GK, Santhanan, S, Read, ML, Eagle, SC, Guillou, DF, Lu, MS-C and Carley, LR, (1996) *Laminated high-aspect ratio microstructures in a conventional CMOS process*, Proceedings MEMS 96, San Diego, USA, Feb 1996, pp 13-18.

Fischer, M, Nägele, M, Eichner, D, Schöllhorn, C and Strobel, R (1996*) Integration of surface micromachined polysilicon mirrors and a standard CMOS process*, Sensors and Actuators, Vol A52, pp 140-144.

French, PJ, van Drieënhuizen, BP. Poenar, D, Goosen, JFL, Sarro, PM and Wolffenbuttel RF, (1996), *The development of a low-stress polysilicon process compatible with standard device processing*, IEEE JMEMS, Vol 5, (1996), pp 187-196.

French, PJ, Sarro, PM, Mallée, R, Fakkeldij, EJM and Wolffenbuttel, RF, (1997), *Optimisation of a low stress silicon nitride process for surface micromachining applications*, Sensors and Actuators, Vol A58, pp 149-157.

Fujitsu (2003), *Fujitsu Achieves Breakthrough in Ultrafine-Pitch Solder Bumping*, http://www.fujitsu.com/global/news/pr/archives/month/2003/20031215-02.html accessed August 2011

Hierold, C, Hilderbrandt, A, Näher, U, Scheiter, T, Mensching, B, Steger, M and Tielert, R, (1996) A pure CMOS surface micromachined integrated accelerometer, Proceedings MEMS 96, San Diego, USA 1996, pp 174-179.

Hornbeck, LJ, (1996) *Digital light processing and MEMS: An overview*, Proc. IEEE/LEOS 1996 Summer Topical Meetings, Aug. 7–8, 1996

Gennissen, PTJ, French, PJ, de Munter DPA, Bell, TE, Kaneko, H, Sarro, PM (1995), *Porous silicon micromachining techniques for acceleration fabrication* Proceeding ESSDERC 95, Den Haag, The Netherlands, 25-27 September 1995, pp 593-596.

Gennissen, PTJ, Bartek, M., Sarro, PM. and French, PJ. (1997) *Bipolar compatible epitaxial poly for smart sensor-stress minimisation and applications*, Sensors and Actuators, VolA62, pp 636-645.

Gennissen, PTJ, (1999) *Micromachining techniques using layers grown in an epitaxial reactor*, PhD Thesis, Delft University of Technology, 1999. Delft University Press. ISBN 90-407-1843-1.

Gianchandani, Y and Najafi, K, (1991) A *bulk dissolved wafer process for microelectromechanical systems*, IEDM Techn. Digest 1991, 757-760

Gianchandani, YB, Shinn, M and Najafi, K, (1997), *Impact of long high temperature anneals on residual stress in polysilicon*, Proceedings Transducers'97, Chicago, USA, June 1997, pp 623-624.

Gieles, ACM, (1968) Integrated miniature pressure sensor, *Dutch patent application, no 6817089*

Gieles, ACM, (1969) *Subminiature silicon pressure transducer*, Digest IEEE ISSCC, Philadelphia, 1969, pp. 108-109.

Guckel, H, Burns, DW, Visser, CCG, Tillmans, HAC, Deroo, D (1988), *Fine-grained polysilicon films with built-in tensile strain*, IEEE Trans. Electron. Dev. 35 pp 800–801.

Hierold, C, Hilderbrandt, A, Näher, U, Scheiter, T, Mensching, B, Steger, M and Tielert, R, (1996) *A pure CMOS surface micromachined integrated accelerometer*, Proceedings MEMS 96, San Diego, USA 1996, pp 174-179.

Jacobi, W. (1952), *Halbleiterverstärker*, DE patent 833366 priority filing on April 14, 1949, published on May 15, 1952.

Kabir, AE, Neudeck, GW and Hancock, JA (1993) *Merged epitaxial lateral overgrowth (MELO) of silicon and its applications in fabricating single crystal silicon surface micromachining structures*, Proceedings Techcon 93, Atlanta, GA, USA.

Kloeck, B, Collins, SD, de Rooij, NF and Smith, RL, (1989), *Study of Electrochemical Etch-Stop for High-Precision Thickness Control of Silicon Membranes*, IEEE Trans. Electron Dev., Vol 36, pp 663-669.

Laemer, F, Schilp, A, Funk, K, Offenberg, M, *Bosch deep silicon etching: improving uniformity and etch rate for advanced MEMS applications*, Proc. IEEE MEMS 1999 Conf., Orlando, FL, USA (1999).

Lang, W, Steiner, P, Sandmaier, (1995), H, *Porous silicon: a novel material for microsystems,* Sensors and Actuators Vol.A51 pp 31-36.

Lehman, V, (1996) *Porous silicon- a new material for MEMS*, Proc. IEEE MEMS Workshop '96, San Diego, USA pp.1-6.

Li, YX, French, PJ, Sarro, PM and Wolffenbuttel, RF, (1995) *Fabrication of a single crystalline capacitive lateral accelerometer using micromachining based on single step plasma etching*, Proceedings MEMS 95, Amsterdam Jan-Feb 1995, pp 398-403.

Makinwa, KAA and Huijsing, JH, (2002) *A smart CMOS wind sensor", Solid-State Circuits Conference*, Digest of Technical Papers. ISSCC. 2002 IEEE International Volume 2, Issue , Page(s):352 – 544

Munter, PJA, (1990), *A low-offset spinning-current Hall plate*, Sensors & Actuators, Vol A21-A23, pp 743-746.

O'Halloran, GM, Groeneweg, J, Sarro, PM and French, PJ, *Porous silicon membrane for humidity sensing applications*, Proceedings Eurosensors 98, Southampton, UK, 13-16 September 1998, pp 901-904.

Ohji, H, Trimp, PJ and French, PJ (1999) *Fabrication of free standing structures using a single step electrochemical etching in hydrofluoric acid*, Sensors and Actuators, . Vol A73 pp. 95-100

Ohji, H, French, PJ and Tsutsumi, K, (2000). *Fabrication of mechanical structures in p-type silicon using electrochemical etching*, Sensors and Actuators Vol A82 pp 254 – 258

Pakula, L, Pham HTM and French, PJ, (2001) *Novel material for low temperature post-processing micromachining*, Proceedings MME, Cork, Ireland, September 2001, pp 70-73

Pakula, LS, Yang, H, Pham, HTM, French, PJ and Sarro, PM, (2004) *Fabrication of a CMOS compatible pressure sensor for harsh environments*, J. Micromech. Microeng., Vol 14, pp 1478-1483.

Palik, ED, Faust, Jr., JW, Gray, HF and Greene, RF, (1982) *Study of the etch-stop mechanism in silicon*, J. Electrochem. Soc. 137 (1982) 2051-2059

Pertijs, MAP, (2005*). Precision Temperature Sensors in CMOS technology* promotor: prof. dr. ir. J.H. Huijsing, 330p. ISBN-10: 90-9020097-5; ISBN-13: 978-90-9020097-2

Petersen, KE., (1982) *Silicon as a mechanical material*, Poc. IEEE, VOL. 70, pp 420-457.

Roozeboom, F, Elfrink, R, Rijks, TGSM, Verhoeven, J, Kemmeren A, and van den Meerakker, J, (2001), Proc. 34th Int. Symp. on Microelectronics (IMAPS 2001), Baltimore, Oct. 9-11, 2001, pp. 477-483- Int. J. Microcircuits and Electronic Packaging, 24 (3) (2001) pp. 182-196

Roozeboom, F, Blauw, MA, Lamy, Y, van Grunsven, E, Dekkers, W, Verhoeven, JF, van den Heuvel, F, van der Drift, E, Kessels WMM and van de Sanden, MCM. (2008) *Deep Reactive Ion Etching of Through-Silicon Vias*, in 'Handbook of 3-D Integration: Technology and Applications of 3D Integrated Circuits', (P. Garrou, C. Bower and P. Ramm, eds.), Wiley-VCH Verlag, Weinheim, pp. 47-91.

Roozeboom, F, Klootwijk, J, Dekkers, W, Lamy, Y, van Grunsven, E and Kim, H, (2008-2) *System-in-package integration of passives using 3D through-silicon vias*, Solid State Technology, vol 51, No. 5

Sangster, LFJ & Teer, K. (1969) *Bucket-brigade electronics - new possibilities for delay, time-axis conversion and scanning*, IEEE J. Solid-State Circuits, SC-4 pp 131-136.

Smith, CS. (1954). *Piezoresistive effect in Germanium and Silicon*, Physical Review. Vol 94, (1954) pp 42-49

Smith, JH, Montague, S, Sniegowski, JJ, Murray, JR, Manginell, RP and McWhorter, PJ, (1996), *Characterisation of the embedded micromachined device approach to the monolithic integration of MEMS with CMOS*, Proceedings SPIE Micromachining and Microfabrication Process Technology II, Austin, Texas, USA, October 1996, vol 2879, pp 306-314.

Texas Instruments. (2008) . *The chip that jack built,* HTML accessed 10 August 2011

van Drieënhuizen, BP, Goosen, JFL, French, PJ, Li, XL, Poenar, D and Wolffenbuttel, RF, (1994), *Surface micromachined module compatible with BiFET electronic processing*, Proceedings Eurosensors 94, Toulouse, France, September 1994, p 108

Westberg, D, Paul, O, Andersson, GI and Baltes, H (1996) *Surface micromachining by sacrificial aluminium etching*, J. Micromech. Microeng., Vol 6, pp 376-384.