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A Quadrature Harmonic Rejection Voltage-Domain Mixer with 20 dBm OIP3 and 800 MHz IF Bandwidth

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***Abstract*— A wideband harmonic rejection voltage-domain mixer using resistive scaling is presented with excellent linearity and high IF bandwidth. Thin-oxide devices with constant gate-to-source voltages (V_{GS}) are utilized to maximize the switching linearity. A novel switching core topology providing low-impedance IF outputs is proposed to support wideband in-phase (I) and quadrature (Q) mixer outputs when loaded by ADCs. Eight LO clock phases, each with a 25 % duty cycle, are on-chip generated for quadrature down-conversion and harmonic rejection (HR). By cleverly activating and organizing the mixer branches, the RF mixer input impedance can be kept perfectly constant throughout all eight clock phases, enhancing the mixer's linearity. The TSMC 40 nm-CMOS realized mixer reaches 20.9 dBm OIP3 at an IF of 50 MHz with a conversion loss of 22.5 dB. It offers an 800 MHz 3-dB IF bandwidth at a differential capacitive loading of 0.15 pF, with a total power consumption of 40.7 mW drawn from a 1.1 V supply. The mixer targets linear wideband base station observation receiver applications.**

***Keywords*— passive mixer, voltage-mode, harmonic rejection, high linearity, observation receiver.**

I. Introduction

The fifth-generation cellular networks (5G) enforce stringent requirements on the spectral purity of wireless signals. As such, the transmit signal must have a minimum adjacent-channel-power-ratio (ACPR) of −45 dBc [1]. Therefore, 5G transmitters (TX) target nominal ACPR levels of −50 dBc. To achieve such a level with an energy-efficient power amplifier (PA), cellular base station transmitters employ a correction loop consisting of a directional coupler, filter, attenuator, down-converting observation receiver, and a digital pre-distorter (DPD) unit (Fig. 1a).

To allow accurate determination of the TX non-linearities at these large ACPR levels, the down-converting path in such a TX setup must offer at least 60 dBc spurious-free dynamic range (SFDR) to the ADCs, with 3× or 5× the bandwidth of the modulated TX signal (to include the IM3 and IM5 products). To achieve this, practical TX observation loops take a fraction of the TX output signal using a directional coupler. Filtering is applied before the mixer to avoid unintended down-conversion of the harmonic content in the TX signal to the baseband by the harmonics of the mixer LO. Next, high attenuation occurs before the mixer to relax the mixer linearity requirements. The mixer is usually implemented in the current-domain so as to limit the voltage swings on its intermediate modes. However, doing so requires linear-IF amplification after the mixer to drive the capacitive input of the ADC ($C_{in} \sim 0.15$ pF) with sufficient voltage swing (e.g., up to 0.2 V). These later requirements combined with 60 dBc

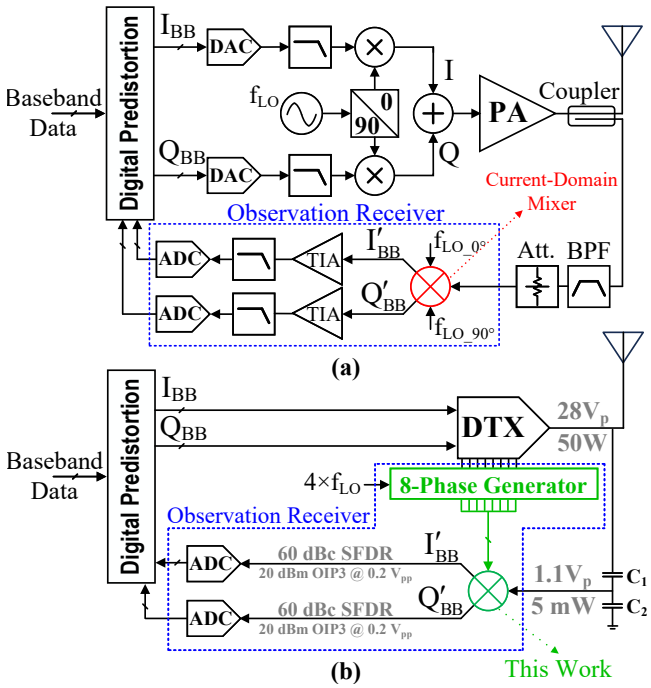

Fig. 1. Block diagram of a transmitter with an observation receiver containing the down-converting mixer and a digital pre-distorter (DPD) unit for an (a) analog intensive transmitter; (b) envisioned digital intensive transmitter.

SFDR translate to an OIP3 of the observation receiver of 7 dBv or 20 dBm when referred to a 50 Ω load. The linear-IF amplification (e.g., a trans-impedance-amplifier (TIA) following the mixer core) becomes more challenging and power-hungry with increasing modulation bandwidths. More specifically, in sub-6 GHz 5G systems, the transmitter modulation bandwidth can reach 400 MHz, which yields 200 MHz in-phase and quadrature-phase signal representations. However, since the observation receiver also needs to include the IM3 and IM5 products, its actual bandwidth must approach 1 GHz, making the linearity, bandwidth, and power consumption of the observation receiver more and more a concern.

In this work, by introducing a new passive voltage-domain mixer topology capable of providing very high OIP3 and large IF bandwidth and harmonic rejection (HR), we aim to drastically simplify the topology of an observation receiver and avoid the need for power-hungry wideband linear-IF amplification. Moreover, the need for a directional coupler, filter, and attenuator can also be omitted when adequately addressed in the down-converting mixer design. Additionally, when aiming for co-integrating the proposed mixer with a

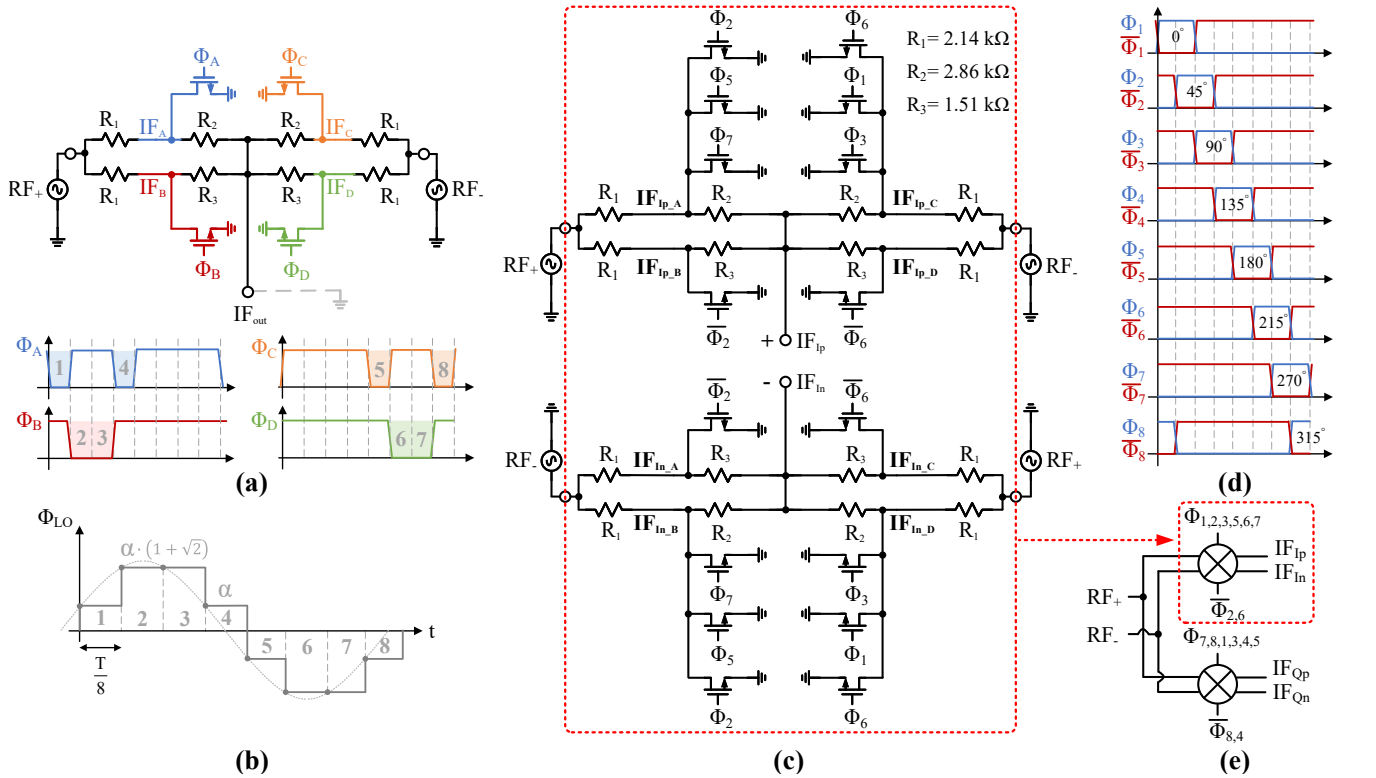

Fig. 2. (a) Simplified topology and related LO phases; (b) Effective harmonic-reject LO waveform; (c) Full proposed voltage-domain mixer topology (I-only); (d) 8-phases 25% duty cycle LO waveforms; (e) Extended I/Q mixer topology.

digital transmitter (DTX) [2], [3] the clock generation can be shared (Fig. 1b). This observation receiver configuration makes classical mixer performance parameters like IIP3 and conversion loss rather arbitrary since they entirely depend on the applied attenuation in the correction loop. Furthermore, since the correction loop aims to model the PA transfer function rather than monitor the TX signal itself, the noise contributions of the observation receiver are averaged out over time, relaxing the mixer noise figure requirement. Finally, since filtering in Fig. 1b is omitted, HR needs to be included in the mixer. Consequently, the attenuator stage can be as simple as a capacitive voltage divider as in Fig. 1b, where C2 $\gg$ C1.

HR in mixers is typically achieved by using multiple sub-mixers in parallel with phase-shifted LO clocks and scaled currents for their switching cores [4]. This approach allows the mimicking of an N-sampled sinewave LO [5]. These current-domain mixers mostly employ trans-impedance amplifiers (TIA) in their RF and/or IF path, which is one of the causes that their linearity is typically limited to <10 dBm in terms of IIP3 [6]–[8]. To date, HR voltage-domain mixers in sub-6 GHz bands have been demonstrated with an OIP3 up to 13 dBm [9]. Here, OIP3 is the fairer metric to compare, given the conversion loss. In these voltage-domain mixers, the limiting factor for the linearity is the variation of the on-resistance of the mixer switches; due to their dependence on the gate-to-source (V_{GS}) voltages, which fluctuate with the RF input signal [5], [9]. In addition, both current and voltage-domain-type mixers using TIAs are restricted by IF bandwidth limitations [6]–[8].

To overcome the above limitations, we propose a novel voltage-domain passive HR mixer topology for an observation receiver application in which the mixing switches' gate-to-source voltages (V_{GS}) always remain constant to achieve high OIP3. Furthermore, by proper scaling of its mixer branches while using eight LO phases with a 25 % duty cycle, the input impedance of the proposed mixer switching core can be kept constant throughout all LO phases, further boosting its linearity. Finally, the proposed mixer core provides low IF output impedance, allowing the direct wideband handling of capacitive loading by subsequent 'I' and 'Q' ADCs without any intermediate gain stage and, thus, lower power consumption.

II. Proposed Novel Voltage-Domain Mixer

A. The Voltage-Domain Mixer Concept

The principle of the proposed voltage-domain mixer core can be understood best by considering the simplified schematic of Fig. 2a, representing a single mixer branch with, for now, a virtual ground at the node IF_{out}. Only one of the resistor branches is active (contributing current to IF_{out}) at any of the eight LO phases (Fig. 2a). In this simplified topology, resistors R_1, R_2, and R_3 are sized such that currents flowing from IF_{out} to the virtual ground, resulting from an activated branch with resistors R_1 and R_2, is a factor $1+\sqrt{2}$ lower than that of an activated branch with resistors R_1 and R_3, thereby implementing the scaling for harmonic rejection of the LO waveform (see Fig. 2b). The proposed configuration benefits from all switches having a well-defined V_{GS} referenced to ground. Therefore, avoiding undesired R_{on} modulation due to the RF input or IF output signals, yielding strongly improved linearity.

The mixer in Fig. 2a avoids both RF and LO feed-through to the IF port, as it is effectively constituting a double-balanced

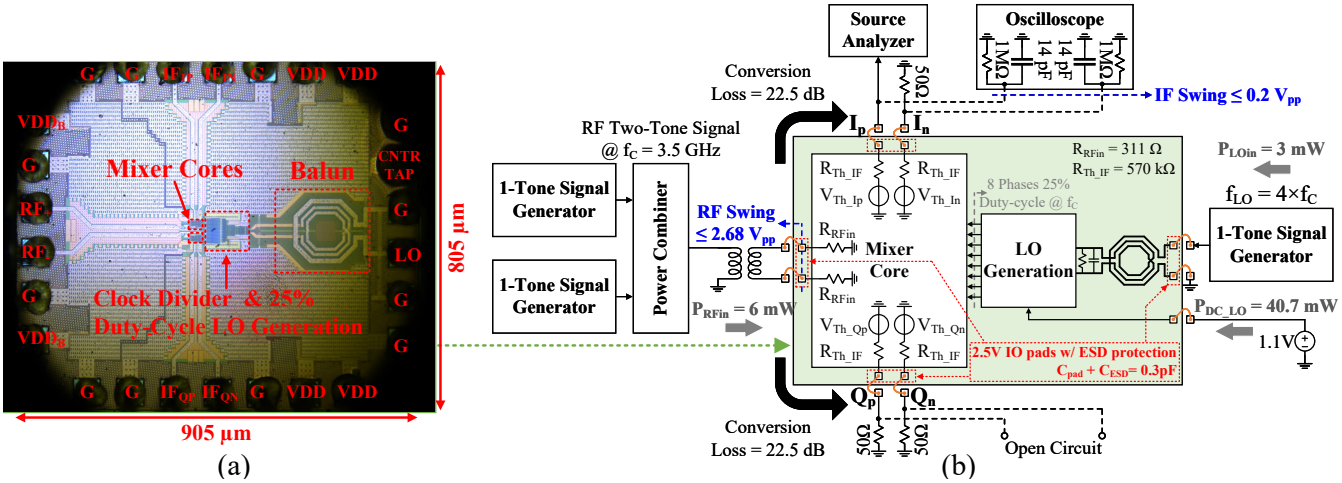

Fig. 3. (a) Fabricated chip micrograph of the voltage-mode mixer; (b) Measurement setup and port impedances.

mixer (the right-hand side of the schematic in Fig. 2a uses 180-degree rotated phases for both the RF and LO clock signals compared to the left-hand side). However, IF_{out} is a current summation node; therefore, any common-mode error appearing on the RF or LO ports will directly couple to the IF. To remedy that, the mixer topology is duplicated while flipping the polarity of the RF inputs to arrive at the final proposed mixer topology, shown in Fig. 2c. The resulting differential outputs IF_{Ip} and IF_{In} are now free of both differential as well as common-mode RF and LO input signals. Additionally, they provide a convenient differential signal to drive the subsequent ADC stages. Furthermore, since the use of different duty cycles to drive the switches (as in Fig. 2a) is problematic in practical circuit implementations, it is beneficial to maintain the same 25% duty cycle across all clocking phases, yielding better phase synchronization between the different clock-paths and, thus, better linearity and HR. This requires splitting each of the two switches controlled by Φ_A and Φ_B in the simplified topology of Fig. 2a, into three separate switches controlled by 25% duty cycle LO signals $\Phi_{1,3,6}$ and $\Phi_{2,5,7}$ respectively (see Fig. 2d).

To obtain useful representations of the IF output signals, the virtual ground in the simplified topology needs to be replaced. The most trivial way to do so is to introduce TIAs at these positions. However, practical TIAs will introduce linearity, bandwidth, and power-budget constraints. Since in our observation receiver the mixer conversion gain is not a concern, and all RF and LO signals are already canceled at the IF port, we can simply remove the virtual ground and use the network terminals IF_{Ip} and IF_{In} directly as the output nodes (Fig. 2c). With this change, the signals are now all in the voltage-domain. Doing so, resistors R_1, R_2, and R_3 need to be re-sized to include the IF port impedance in order to maintain the proper harmonic rejection ratios of Fig. 2b.

The extension to a differential quadrature down-conversion mixer is achieved by duplicating the mixer core topology once more and phase-shifting the LO by 90 degrees (Fig. 2e). The loading of the input nodes RF_+ and RF_- by the total I/Q mixer now remains perfectly constant throughout all phases of the LO cycle (thus vs. time), again contributing to the linearity of the proposed mixer.

B. Conversion Loss

The conversion loss of the mixer depends on the voltage division ratios; formed by R_2 and R_3 with R_1, from the four RF ports through the eight signal scaling paths towards the two differential IF ports in Fig. 2b. The different phases and effective duty cycles of the driving LO waveforms for each of the eight signal scaling paths contribute differently towards the fundamental component at the IF ports.

C. Output Impedance

In the observation receiver line-up shown in Fig. 1, the down-conversion mixer is followed by ADCs, which present a capacitive load to the down-conversion mixer outputs. Thus, the IF output impedance of the down-conversion mixer need to be low enough to allow a large IF bandwidth. The differential output impedance of either the I or Q outputs of the mixer provides a baseband impedance given by

$$R_{out} \approx \left(\tfrac{R_2}{2} \parallel R_3 \parallel (R_1 + R_3)\right) + \left(R_2 \parallel \tfrac{R_3}{2} \parallel (R_1 + R_2)\right). \quad (1)$$

Reducing the values of R_2 and R_3 (to reduce the IF output impedance) while keeping R_1 constant (to maintain the RF port loading) will result in a large conversion loss for the mixer as the voltage division ratios that these resistors form with R_1 will decrease, but in our observation receiver application we can simply reduce the attenuation before the mixer, proving a wealth of design freedom.

III. Mixer Implementation and Measurements

The mixer, including the eight phase LO generation (Fig. 2d), was implemented using thin-oxide transistors in TSMC 40 nm-CMOS technology. The mixer core occupies an area of 27 µm × 27 µm.

The on-chip clock generation uses a 14 GHz single-ended LO as an external frequency reference. An on-chip balun creates a differential 50 % duty-cycle LO. A phase-aligner and two consecutive divde-by-2 stages generate the eight-phase 50 % duty-cycle 3.5 GHz LO waveforms. AND/OR gates devised solely from symmetric NAND gates are then used to create the final eight-phase 25 % duty-cycle LO waveforms. Buffers and further phase-aligners are added throughout the clock tree

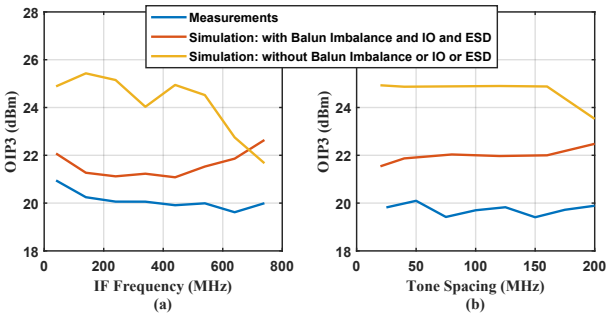

Fig. 4. Linearity at f_c = 3.5 GHz, (a) OIP3 vs. IF frequency with tone spacing = 20 MHz; (b) OIP3 vs. tone spacing with IF center frequency = 350 MHz.

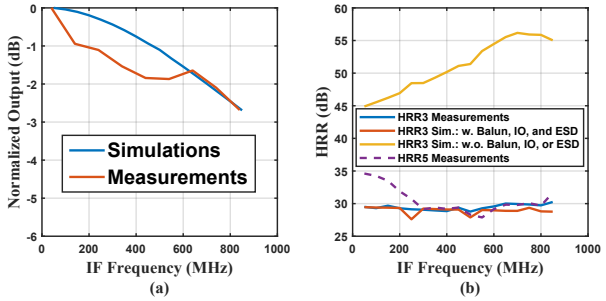

Fig. 5. (a) IF bandwidth; (b) Harmonic rejection ratio (HRR) at f_c = 3.5 GHz.

where needed. Including the LO generation circuitry, the total mixer area is 133 µm × 57 µm (Fig. 3a). All measurements are performed at a carrier frequency of 3.5 GHz targeting mMIMO base station applications.

The mixer's power consumption, including clock generation, is 40.7 mW from a 1.1 V supply. Conversion loss, linearity, and harmonic rejection measurements were performed using the setup shown in Fig. 3b. The output losses due to cable connections and board traces were de-embedded.

Since the final mixer application targets an on-chip IF ADC differential loading condition of 0.15 pF. The conversion loss was measured at a low IF frequency (1 MHz) using a Keysight oscilloscope (MSOS804A) with an input impedance of 1 MΩ || 14 pF yielding 22.5 dB, which matched well with simulations, indicating the fabricated resistor ratios were accurate. Thus, confirming the targeted IF bandwidth of 800 MHz for the original intended differential capacitive loading of 0.15 pF, since the bandwidth ($BW = 1/(2\pi \cdot 0.15\text{pF} \cdot R_{out})$) only depends on the same resistor ratios (1). Measured IF bandwidth is shown in Fig. 5a. The deviation from simulation is due to the inferior RF-input balun's response as well as IO and ESD. The targeted IF output voltage swing of 0.2 V_{pp} for a maximum RF-input swing of 2.68 V_{pp} was also confirmed.

Although the simulated linearity of the intrinsic mixer core in terms of OIP3 is very high (>24 dBm), IO-interconnect parasitics like bond wires and the non-linearity due to the ESD protection circuits degrade the linearity performance to some extent in our measurements. In spite of this, using a source analyzer (R&S FSUP50) with 50 Ω IF port loading, the measured OIP3 proved to be 20 dBm across the mixer's IF bandwidth (Fig. 4a); a comparable performance was also achieved versus RF tone-spacing (Fig. 4b).

The third harmonic rejection ratio (HRR3) was measured to be around 30 dB over the mixer's IF bandwidth (Fig. 5b). This somewhat reduced HRR3 was associated with an imbalance introduced by the on-chip balun connection. When including the balun imbalance and non-linearity caused by the ESD protection within our simulations, they align well with the measurements.

Table 1. Performance comparison with wideband highly linear mixers.

Design	[9]	[5]	[6]	**This Work**
Technology	32nm SOI	45nm SOI	28nm HPC	**40nm CMOS**
Mixing Domain	Voltage	Voltage	Current	**Voltage**
I/Q Paths	No	No	Yes	**Yes**
RF Frequency (GHz)	3.5	3	2	**3.5**
3 dB IF BW (MHz)	200	80	130	**800**
Conversion Gain (dB)	-7.5	-10	32.4	**-22.5**
HRR (dB)	40[a]	35[a]	0	**30**[b]
Harmonics Rejected	2	6	2	**2**
In-band OIP3 (dBm)	13	8	18.4	**20**
Supply Voltage (V)	1.1	1	1.8/1.2	**1.1**
Power (mW)	80	160	37.2	**40.7**

[a] measured with GSSG probes, [b] measured with bond wires.

IV. Conclusions

A novel highly linear wideband harmonic-reject voltage-domain mixer topology is proposed and implemented in CMOS 40 nm. By circumventing the non-linearity introduced by the variation of the mixer's switches' on-impedance and the need of power-hungry wideband linear-IF amplification, excellent linearity performance is achieved, making it an interesting candidate for the implementation of highly-linear, wideband, low-power base station observation receiver applications. The realized mixer (despite its ESD and interconnect parasitics) offers excellent performance in terms of OIP3 (20 dBm) and IF bandwidth (800 MHz) while offering HR and quadrature down-conversion functionality, placing it favorably among the state-of-the-art mixers, as can be concluded from Table 1.

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