Design and Analysis of PCB Embedded SiC Half-Bridge Packaging Cells With Low Thermal Resistance and Parasitic Inductance

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***Abstract*—Reducing parasitic parameters and thermal resistance is critical for advancing power electronic devices. This article designs and evaluates the three printed circuit board (PCB) embedded 1200 V SiC MOSFET half-bridge packaging cells, where the traditional wire bonding process is replaced by a redistribution layer (RDL) technique. A comprehensive evaluation of their electrical performance, thermal management, and mechanical performance is conducted. The three solutions that employ panel, active metal brazing (AMB), and lead—frame carriers, are developed through a streamlined process that includes die attach, molding, drilling, plating, and etching. This packaging approach readily reduces the parasitic inductance to below 5 nH. By utilizing a single-layer RDL with mutual inductance cancellation, the power loop inductance is reduced to as low as 2.4 nH (at 10 MHz), and the gate loop inductance to 1.57 nH (at 10 MHz). The junction-to-case thermal resistances of the three solutions are 1.88, 1.03, and 0.73 K/W, respectively. Compared with the other two packaging cells, the cell selecting AMB as a carrier reduces SiC MOSFET operational stress and deformation by approximately 34% and 75% . The lead—frame carrier offers superior thermal dissipation for potential TO package replacement in half-bridge topologies, while the panel solution is promising for dual-sided cooling applications. With low thermal resistance, minimal stress, and excellent backside electrical insulation, the packaging cell with an AMB carrier is ideally suited for integration with heatsinks in traction inverters.**

***Index Terms*—Half bridge, parasitic inductance, printed circuit board (PCB) embedded packaging cell, SiC MOSFET, thermal resistance.**

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I. Introduction

In response to global warming and to reduce dependence on fossil fuels in order to drive a low–carbon economic transformation, a worldwide surge in the development of new energy—such as new energy vehicles and clean power generation—has emerged [1], [2], [3]. In the processes of power generation, transmission, and consumption in new energy systems, power electronic devices (e.g., inverters and converters) play an indispensable role [4]. These devices achieve their functionality primarily through the turn–on and turn–off operations of power devices [5], [6]. In early medium–to–high voltage applications, switching was mainly implemented by Si–based metal-oxide-semiconductor field effect transistor (MOSFET) and insulated–gate bipolar transistor (IGBT) [5]. However, Si–based power devices suffer from drawbacks such as a narrow bandgap, low thermal conductivity, and high switching losses. With the development of silicon carbide (SiC) materials, SiC MOSFETs have gradually supplanted Si–IGBTs and Si–MOSFETs as the most promising power devices in the new energy field. Compared with Si materials, SiC offers significant advantages: an operating temperature approximately five times higher and a breakdown voltage roughly ten times greater. At the same voltage level, SiC devices exhibit lower switching losses and can operate at switching frequencies 5–10 times higher [7], [8]. Based on these merits, SiC devices are more suitable for power electronic applications such as new energy vehicle inverters, onboard chargers, converters, and so on [9].

In power electronics, power devices are often employed through module integration [10]. Currently, power modules are chiefly designed using half-bridge or neutral point clamped topologies to realize switching performance [11]. In high-current applications, such as traction inverters, a parallel configuration of multiple dies is typically employed [12]. During the design stage, merely integrating SiC MOSFETs into a power module does not fully exploit their superior performance [13].

The switching characteristics of SiC MOSFETs are influenced by various factors, notably parasitic inductance and capacitance [14]. Parasitic capacitance—introduced mainly during the fabrication processes of power devices and modules—is generally unavoidable [15]. During switching, excessive parasitic capacitance, particularly the Miller capacitance, can induce crosstalk that causes unintended conduction in the half-bridge, potentially resulting in a short-circuit [16]. Parasitic inductance arises primarily from aspects of module design and fabrication, such as power terminal, bonding wires and ceramic substrate layouts [17]. Excessive parasitic inductance may lead to significant voltage overshoots during switching, which can damage the device [18]. Moreover, high parasitic inductance slows the switching speed, thereby increasing switching losses and reducing overall system efficiency. The consequent rise in switching losses imposes continuous electrical and thermal stresses, ultimately shortening the lifetime of power modules [15], [17]. Hence, mitigating the parasitic parameters in power modules is critical to fully exploiting the potential of SiC MOSFETs.

So far, the internal electrical connection of mainstream industrial power modules (e.g., direct cooled molded) is primarily realized by two methods: wire bonding and copper clips [19], [20]. Compared with conventional aluminum wire bonding, Cu bond wires and Cu clips help reduce parasitic inductance and enhance power cycling lifetime [20]. However, whenever wire bonding is employed, it remains challenging to lower the internal parasitic parameters below 10 nH [21]. In contrast, the copper clip instead of wire bonding shows potential for achieving parasitic parameters slightly under 10 nH. In pursuit of further parasitic reduction, novel alternatives to wire bonding have been introduced in both academic research and the industrial field. For instance, Liang [22] adopted a double-sided direct bonded copper (DBC) solution that reduced the parasitic parameter to approximately 12.8 nH. Moreover, Virginia Tech and Huazhong University of Science and Technology proposed a printed circuit board (PCB)—on—DBC approach, lowering the module's parasitic inductance to 3.6 and 3.38 nH, respectively [23], [24]. Currently, these parasitic reduction methods are approaching the limits of traditional power modules, and their fabrication processes are relatively complex, making it difficult for commercial applications.

To simplify the fabrication process and further exploit the application potential of SiC MOSFETs, the development of novel power module packaging solutions is of paramount importance. As an alternative to wire bonding, PCB embedded packaging—also known as chip-in-polymer—is a pioneering 3D integrated packaging approach developed by Fraunhofer IZM and TU Berlin [25], [26], [27]. With advantages such as miniaturization, lightweight design, a simple manufacturing process, and low parasitic parameters, this scheme not only helps reduce costs but also further expands the application potential of both SiC MOSFETs and GaN HEMTs.

Currently, PCB embedded SiC MOSFET or GaN HEMT packaging cells predominantly utilize discrete devices, half-bridge or full-bridge topologies to evaluate their parasitic parameters, electrical performance, thermal performance, and mechanical performance [28], [29], [30], [31], [32], [33], [34], [35]. Due to current studies not addressing system terminal interface compatibility, differences in independently designed terminal extraction schemes often result in variations in parasitic inductance. However, PCB embedded packaging using a single-layer redistribution layer (RDL) can readily achieve both gate and power circuit inductances below 5 nH—with the parasitic parameters of discrete devices typically being significantly lower than those in half-bridge topologies. When the number of RDL is increased to 2–4, the gate and power loop inductances can be further reduced to approximately 1.6–1.8 nH and 1.45–2.4 nH, respectively [30], [33]. Additionally, since the current studies employ the same thermal dissipation pathway as the TO package, the junction-to-case thermal resistance ($R_{\mathrm{th}j\text{-}c}$) is about 0.5 K/W [29], [31], [32], [34], [35], [36]. However, with the backside serving as the drain of the SiC MOSFET, the applicable scenarios are consequently limited. Knoll et al. [30] have even designed a dual-sided air-cooled PCB embedded packaging scheme, reducing the $R_{\mathrm{th}j\text{-}c}$ to as low as 0.12 K/W. In summary, PCB embedded packaging not only ensures effective thermal management but also significantly minimizes parasitic parameters, making it a promising packaging platform for next-generation power module.

However, PCB embedded packaging also presents several challenges. Currently, there are two main thermal management strategies for PCB embedded packaging. One approach employs copper as the substrate for direct heat dissipation. However, since the copper heat sink also functions as the drain of the SiC MOSFET, this method is limited to lower-power applications that utilize air cooling. The other approach, similar to Infineon's solution [33], involves filling the space between the heat dissipation board and the drain substrate with an electrically insulating material. Nonetheless, compared to metal and ceramic materials, mainstream insulating materials—such as epoxy molding compound (EMC), BT prepreg, and glass fiber PP—exhibit lower thermal conductivity ($\leq$10 W/mK) [36], [37]. An excessively thick insulation layer severely impedes module heat dissipation, while a thinner layer raises challenges in insulation voltage withstand. Furthermore, the parasitic capacitance between the heat sink pad (typically earthed) and the drain pad may also cause common-mode noise to propagate to other parts of the system. Although some studies [38] have employed DBC as the carrier substrate, they lack empirical performance evaluation data. Their assessments of junction temperature and thermal resistance rely solely on thermal simulations. Therefore, the design approach of this article has been optimized and iterated upon the basis of prior research.

In order to broaden the application scenarios of PCB embedded packaging, this article proposes three embedded packaging solutions and provides a comprehensive comparison of their electrical, thermal, and mechanical performance.

The rest of this article is organized as follows. Sections II and III in this article design three distinct PCB embedded SiC MOSFET half-bridge packaging cells selecting panel, AMB, and lead-frame as carriers. Finite-element simulations are employed to evaluate the parasitic parameters, thermal performance, and mechanical properties. Section IV describes the process flow for each PCB embedded packaging cell, while Section V assesses

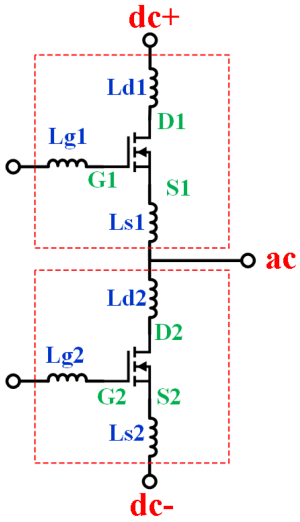

Fig. 1. Equivalent circuit model of the embedded half-bridge cell.

their static parameter characteristics and thermal resistances. Finally, Section VI concludes this article.

II. SiC MOSFET and Phase-Leg Power Module

Fig. 1 presents the equivalent circuit model of the PCB embedded half-bridge packaging cell, which includes the phase-leg of the half-bridge module as well as the parasitic inductances in its individual branches. The half-bridge module is primarily composed of high-side and low-side SiC MOSFET. During the packaging, the electrical connections introduce parasitic inductances into the internal branches of the power module. As shown in the figure, these parasitic inductances are mainly distributed across six branches. L_{g1}, L_{d1}, and L_{s1} represent the gate parasitic inductance, the parasitic inductance from dc+ to the drain, and the parasitic inductance from the source to ac of the high side, respectively. Similarly, L_{g2}, L_{d2}, and L_{s2} denote the corresponding inductances for the low side. Furthermore, the top surface primarily shows the location for terminal extraction, while the bottom is mainly utilized as the heatsink pad.

In this article, three PCB embedded packaging cells were developed and corresponding prototypes were fabricated to compare their electrothermalmechanical performance. These packaging cells are also suited for different application scenarios. Specifically, the designs utilize copper panel, AMB, and lead-frame as carriers for the respective packaging cells. Hence, the packaging structures are distinguished by these carrier types. SiC MOSFET (S1M040120B from SICHAIN Semiconductor) serves as the switching unit, which is embedded within each packaging cell, with its drain, source, and gate individually routed to the module surface, as shown in the phase-leg distribution of the three structures in Fig. 2.

III. PCB Embedded Package Cells Electrothermomechanical Evaluation

This section primarily evaluates the structural designs and electrothermomechanical performance of three PCB embedded

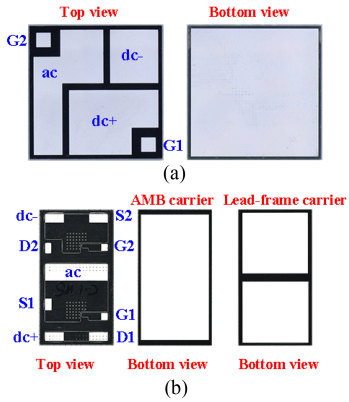

Fig. 2. Phase-leg distribution of the embedded packaging cell selecting. (a) Panel. (b) AMB and Lead-frame as carriers.

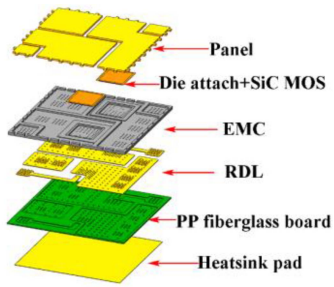

Fig. 3. 3D exploded view of embedded packaging cell for panel carrier.

packaging cells. The parasitic parameters of each branch were extracted using Q3D according to Fig. 1, and the effects of frequency on these parameters were analyzed. The accuracy of the thermal model simulations is validated by comparing the results of dual interface thermal resistance tests with simulations performed using COMSOL. This approach allows for precise quantification of the junction temperature, stress, and deformation across the three packaging cells.

A. Structural Design and Components of Embedded Packages

Fig. 3 shows the 3D exploded view of the PCB embedded packaging cell selecting panel as the carrier. The cell mainly comprises Panel, die attach, SiC MOSFET, EMC, RDL, polypropylene (PP) fiberglass board, and the heatsink pad. Fig. 3 illustrates the structure employing pressure-assisted silver sintering. Since the sintering equipment cannot cover the entire panel, the isolated portion carrying the SiC MOSFET serves as an independent carrier for pressure-assisted sintering. A cavity larger than the die size is provided at the die mounting area to ensure uniform RDL thickness.

Fig. 4 illustrates the 3D exploded diagrams of PCB embedded packaging cells employing AMB and lead-frame as carriers, respectively. These cells are mainly composed of the carriers (AMB or lead-frame), the die attach, the SiC MOSFET, EMC, RDL, and the ink layer. Both the AMB and lead-frame designs incorporate the cavity at the die placement area that is larger than the die itself, in order to enhance the uniformity of the RDL thickness.

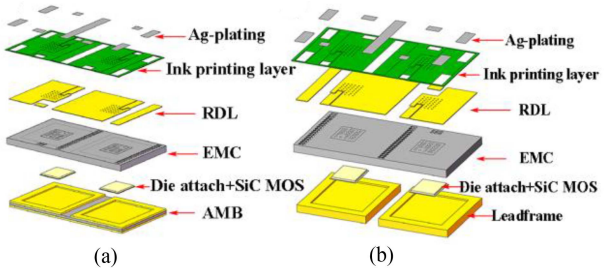

Fig. 4. 3D exploded view of embedded packaging cells for (a) AMB carrier and (b) lead-frame carrier.

B. Package Parasitic Inductances Extraction

Parasitic parameters in power modules are primarily composed of two components: intrinsic parasitic parameters of SiC MOSFET and those arising from packaging interconnections [39], with the former being negligible. The influence of parasitic parameters is crucial to the switching characteristics of power modules, directly affecting switching speed and switching losses. The frequency sweep range for parasitic parameter extraction spans from 0 Hz to 1 GHz, where linear steps are employed for 0 to 1 Hz and 100 MHz to 1 GHz, a logarithmic scale is adopted for the 1 Hz to 100 MHz range. The step sizes are set to 1 Hz for the 0 to 1 Hz and 100 MHz for the 100 MHz to 1 GHz, with 15 data points per decade collected between 1 Hz and 100 MHz.

Fig. 5 shows the extraction of parasitic parameters for the PCB embedded packaging cell with the panel carrier. The gate, source, and drain of the high side are denoted as G1, S1, and D1, respectively, while the gate, source, and drain of the low side are also represented as G2, S2, and D2. It is observed that the parasitic inductance decreases with increasing frequency, whereas the parasitic resistance increases, primarily due to the skin effect and proximity effect at high frequencies. At a specific frequency of 10 MHz, the power loop exhibits a parasitic inductance of 2.4 nH and a parasitic resistance of 5.4 mΩ. The parasitic inductances of the gate loops on the high and low sides are 3.8 and 2.5 nH, respectively, with corresponding parasitic resistances of approximately 12.5 and 8.3 mΩ. Due to the short conduction paths from dc+ to D1 and ac to D2, the parasitic inductances are as low as 71.6 and 53 pH, respectively, while the parasitic resistances are approximately 0.4 $\mu\Omega$, with the inductance remaining unaffected by frequency variations. The parasitic inductances from S1 to ac and S2 to dc− are relatively close, at approximately 0.24 nH and 0.27 nH, respectively, with corresponding parasitic resistances of about 0.9 and 1.0 mΩ.

Figs. 6 and 7 illustrate the extraction of parasitic parameters for PCB embedded packaging cells with AMB and lead-frame carriers, respectively. At a specific frequency of 10 MHz, the stray inductance of the two carriers is measured as 5.6 and 5.4 nH, while the parasitic resistance is 3.7 and 3.5 mΩ, respectively. Replacing the AMB substrate with the lead-frame reduces the high side gate inductance from 2.9 to 2.47 nH. Meanwhile, the low side parasitic inductance remains 1.57 nH. The inductance of dc+ to D1 for the AMB carrier is 194 pH, which is lower than the 232 pH observed for the lead-frame carrier. The parasitic parameters along the S2-ac, ac-D2, and S2-dc paths

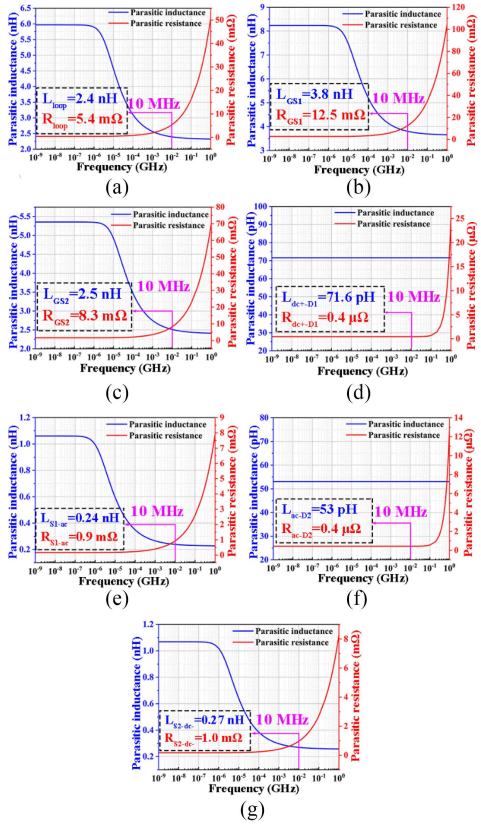

Fig. 5. Extraction of parasitic parameters for embedded packaging cells with panel carrier. (a) Power loop. (b) High-side gate loop. (c) Low-side gate loop. (d) DC+ to D1. (e) S1 to AC. (f) AC to D2. (g) S2 to DC−.

TABLE I
SUMMARY OF PARASITIC INDUCTANCE FOR PCB EMBEDDED PACKAGING CELLS

Type	Panel	AMB	Lead-frame
L_{loop}	2.4 nH	5.6 nH	5.4 nH
L_{GS1}	3.8 nH	2.9 nH	2.47 nH
L_{GS2}	2.5 nH	1.57 nH	1.57 nH
$L_{dc+\text{-}D1}$	71.6 pH	194 pH	232 pH
$L_{S1\text{-}ac}$	0.24 nH	388 pH	388 pH
$L_{ac\text{-}D2}$	53 pH	436 pH	0.43 nH
$L_{S2\text{-}DC\text{-}}$	0.27 nH	230 pH	230 pH

exhibit minimal differences between the two carriers, measuring approximately 388 pH, 0.43 nH, and 230 pH, respectively.

Table I summarizes the parasitic parameters of different paths for the three PCB embedded packaging cells. It can be observed that the loop parasitic inductance of PCB embedded packaging cells with panel carrier is the lowest. However, the gate loop exhibits relatively higher parasitic inductance due to the absence of the specifically designed Kelvin source for gate drive inductance cancellation. Additionally, other branches of the PCB embedded packaging cells with panel carrier consistently show lower parasitic inductance. Although reducing parasitic parameters through a single-layer conductor is challenging in power modules, a multilayer structure can leverage the mutual inductance effect to mitigate parasitic inductance [40]. The opposing

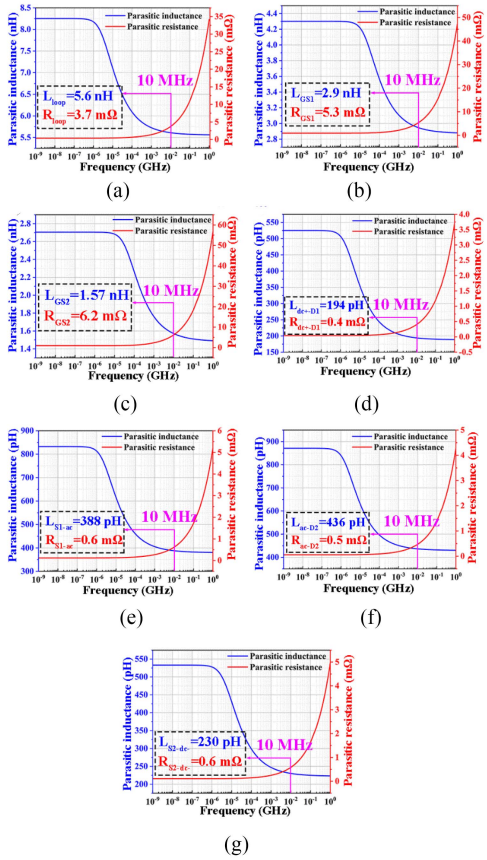

Fig. 6. Extraction of parasitic parameters for embedded packaging cells with AMB carrier. (a) Power loop. (b) High-side gate loop. (c) Low-side gate loop. (d) DC+ to D1. (e) S1 to AC. (f) AC to D2. (g) S2 to DC−.

current directions in two planar conductors induce a mutual inductance effect, particularly significant at high frequencies, as described in

$$L = \frac{\mu_0 l}{2\pi}\left(\ln\frac{2l}{t+a}+\frac{1}{2}\right) - \frac{\mu_0 l}{2\pi}\left[\ln\frac{2l}{d}+\frac{1}{2}-2\frac{d}{a}\tan^{-1}\frac{a}{d} -\frac{1}{2}\left(1-\frac{d^2}{a^2}\right)\ln\left(1+\frac{a^2}{d^2}\right)\right] \quad (1)$$

where the conductor length is l, width is a, thickness is t, conductor spacing is d, and μ_0 is the vacuum permeability.

As shown in Fig. 8, the embedded packaging cell with panel carrier employs mutual inductance cancellation to reduce the overall parasitic inductance in the power loop. In contrast, the mutual inductance cancellation effect of packaging cells utilizing AMB or lead frame carriers within power loop is extremely weak, aiming instead to explore the upper limit of parasitic inductance for the package platform. However, the gate drive loop in these cells adopts a mutual inductance cancellation to mitigate parasitic effects. Consequently, the packaging cell with panel exhibits lower parasitic parameters in the power loop, whereas the packaging cells with AMB and lead-frame achieve lower parasitic inductance in the gate loop. Currently, mainstream power modules for new energy traction inverters, such as Danfoss's Direct Cooled Molded and Infineon's Hybrid PACK Drive, exhibit

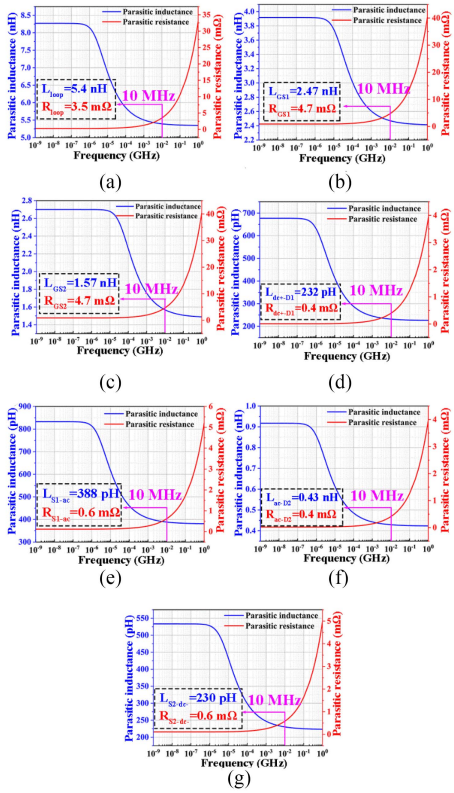

Fig. 7. Extraction of parasitic parameters for embedded packaging cells with lead-frame carrier. (a) Power loop. (b) High-side gate loop. (c) Low-side gate loop. (d) DC+ to D1. (e) S1 to AC. (f) AC to D2. (g) S2 to DC−.

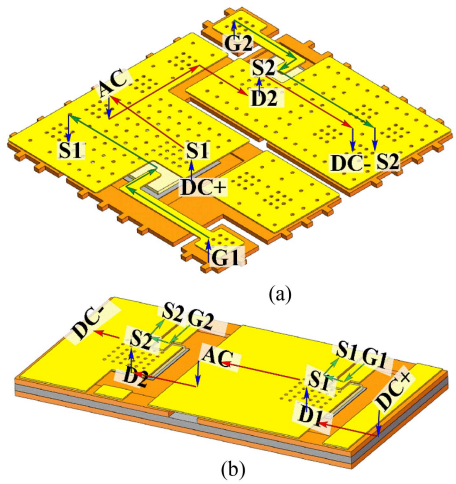

Fig. 8. Schematic diagram of the commutation loop of the PCB embedded packaging cells with (a) panel carrier and (b) AMB/lead-frame carrier.

a minimum stray inductance of approximately 5–10 nH [19], [41], while the parasitic inductance of PCB embedded packaging cell can be readily reduced to below 5 nH. Furthermore, previous studies have reported that the TO-247 package exhibits power loop and gate loop inductances of approximately 36.9 and 20.5 nH, respectively [28]. Therefore, PCB embedded packaging cells can enhance efficiency in both inverters and converters by virtue of their lower parasitic parameters.

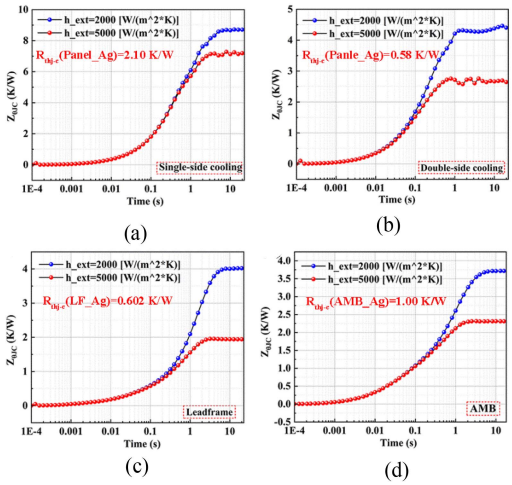

Fig. 9. Dual interface thermal impedance simulation. (a) Single-sided. (b) Dual-sided cooling for panel carrier. (c) Lead-frame carrier. (d) Active metal brazing.

TABLE II
THERMAL-MECHANICAL PARAMETERS OF DIFFERENT MATERIALS

Materials	ρ (g/cm^3)	K (W/m°C)	CTE (ppm/K)	E (GPa)	C (J/(kg·K))	υ
Cu	8.9	385	16.5	126	385	0.34
SiC	3.2	270	5.1	748	690	0.45
Ag	10.5	200	18.9	83	235	0.37
EMC	1.5	1.5	20	15	1200	0.38
PP	1	1.2	17	16	1000	0.3
Si_3N_4	3.1	20	2.3	250	700	0.23

C. Thermal Analysis

Reducing the thermal resistance of power modules not only enhances their reliability but also allows for a reduction in the number of SiC MOSFETs required at the same operating junction temperature [42], thereby lowering costs. Consequently, for high-power-density modules, it is critical to optimize the design to minimize both thermal resistance and junction temperature. This article proposes three solutions for PCB embedded packaging cells, aimed at investigating the impact of carriers on the thermal performance of the embedded packaging cells. Fig. 9 presents transient simulations of dual-interface thermal impedance curves for the three packaging solutions using COMSOL, with the specific heat consumption of SiC MOSFET set at 50 W. To facilitate the identification of the separation point on the thermal impedance curve for reading the junction-to-case thermal resistance, the convective heat transfer coefficients of the heat sink are set at 2000 W/(m^2·K) and 5000 W/(m^2·K), respectively. The die attach is assumed to employ silver sintering to enable a direct comparison of the effect of packaging cell designs on thermal resistance. Packaging material parameters are given in Table II. A comparison with the experimental thermal resistance in Section V only exhibits minor discrepancies between simulation and experiment, thus validating the simulation results as a reliable reference. The definition of the thermal impedance curve follows JESD51-14, as shown in

$$Z_{\theta JC}(\mathrm{t}) = \frac{T_J(\mathrm{t}) - T_a}{P_{\mathrm{loss}}} \tag{2}$$

where $Z_{\theta JC}$(t) is the transient thermal impedance, T_J(t) is the transient junction temperature of the SiC MOSFET at a specific power loss P_{loss}, and T_a is the ambient temperature.

According to the thermal impedance simulation results shown in Fig. 9(a), the PCB embedded packaging cell using panel carrier exhibits $R_{\mathrm{th}j\text{-}c}$ of approximately 2.10 K/W under single-sided cooling (with a heatsink pad serving as the cooling surface). Since the heat diffusion path is analogous to the current diffusion path, the thermal resistance under dual-sided cooling can be calculated as the equivalent of parallel resistances. When dual-sided cooling is employed, $R_{\mathrm{th}j\text{-}c}$ is significantly reduced to around 0.58 K/W, as shown in Fig. 9(b). The high thermal resistance in single-sided cooling primarily results from using fiberglass PP as the insulation layer, which has a low thermal conductivity of only 1.2 W/m°C. Nevertheless, this packaging design facilitates the application of dual-sided air cooling for lower power density applications. To further reduce thermal resistance, the PCB embedded packaging cell with lead-frame carrier is proposed, with thermal simulation results shown in Fig. 9(c). It is evident that adopting the lead-frame carrier can dramatically lower $R_{\mathrm{th}j\text{-}c}$ to 0.602 K/W. However, the cooling surface is connected to the drain of the SiC MOSFET. It can be either surface-mounted on or embedded in the PCB, making it a promising alternative to the TO package in half-bridge topology. However, because the traction inverter modules typically require pin-fin liquid cooling, electrical insulation in the substrate is necessary. Accordingly, an additional design employing an AMB carrier is introduced, which achieves an $R_{\mathrm{th}j\text{-}c}$ of about 1.00 K/W—intermediate between the panel and lead-frame carriers—as shown in Fig. 9(c).

The simulated thermal resistance results are in close agreement with the experimental values, thus validating their use for thermal performance evaluation. Based on the simulation settings described above, the maximum junction temperatures ($T_{j,\,\mathrm{max}}$) for the three embedded packaging cells were extracted (with the convection heat transfer coefficient set to 5000 W/(m^2·K)), as shown in Fig. 10. It can be observed that when using the panel carrier, $T_{j,\,\mathrm{max}}$ under single-sided cooling reaches as high as 398°C, whereas under dual-sided cooling it is only 167°C. When an AMB carrier is employed, the SiC MOSFET exhibits a significantly lower $T_{j,\,\mathrm{max}}$ of only 150°C. Moreover, with a lead-frame carrier, the SiC MOSFET achieves the lowest $T_{j,\,\mathrm{max}}$ among the three cells at merely 127°C.

In summary, using lead-frame carrier yields the lowest $R_{\mathrm{th}j\text{-}c}$ and $T_{j,\,\mathrm{max}}$, making it a viable substitute for TO package in half-bridge applications. With an AMB carrier, the PCB embedded packaging cell similarly demonstrates low $R_{\mathrm{th}j\text{-}c}$ and $T_{j,\,\mathrm{max}}$. Moreover, thanks to the electrical insulation on the backside of the AMB, this packaging cell can enable the interconnection with Pin-Fin, thereby providing a solution for traction inverters. In the case of a panel carrier, the dual-sided cooling effect is significantly superior to that of single-sided cooling, rendering it suitable for dual-sided air-cooled modules.

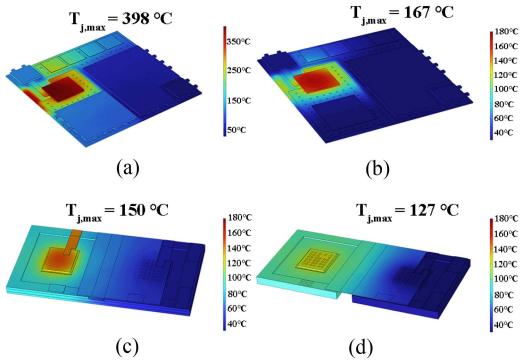

Fig. 10. Simulated $T_{j,\max}$ of SiC MOSFET for PCB embedded packaging cells. (a) Single-sided. (b) Dual-sided cooling for panel carrier. (c) Active metal brazing. (d) Lead-frame carrier.

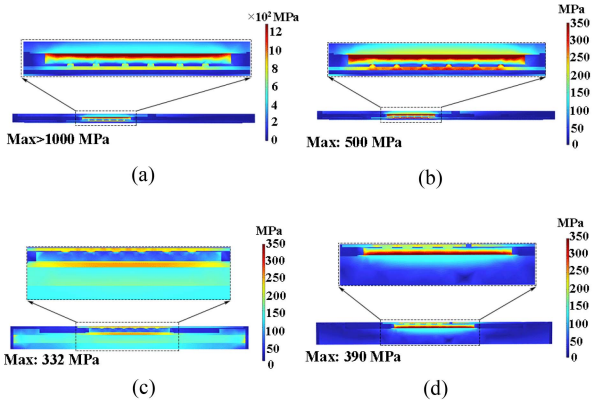

Fig. 11. Von Mises stress distribution during SiC MOSFET operating. (a) Single-sided. (b) Dual-sided cooling for panel carrier. (c) Active metal brazing. (d) Lead-frame carrier.

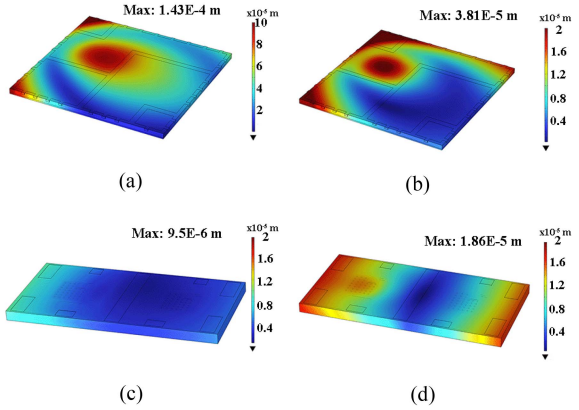

Fig. 12. Deformation during SiC MOSFET operating. (a) Single-sided. (b) Dual-sided cooling for panel carrier. (c) Active metal brazing. (d) Lead-frame carrier.

D. Thermo-Mechanical Analysis

In this article, a thermomechanically coupled model is employed to investigate the Von Mises stress distribution and deformation of the three embedded packaging cells during SiC MOSFET operation, as shown in Figs. 11 and 12 . The temperature physical field parameters are set identically to those used in the thermal analysis, while the constraints of the solid mechanics

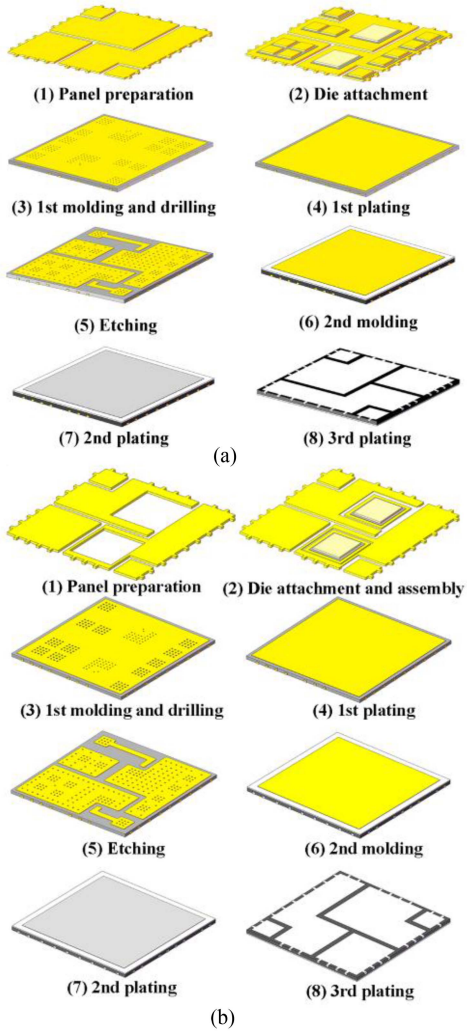

Fig. 13. Process flow of PCB embedded packaging cells with panel carrier. (a) Ag adhesive and solder paste. (b) Pressure-assisted sintered copper or silver.

physical field adopt a free-deformation approach. All the packaging materials utilized in the PCB embedded packaging cells are given in Table II. Due to mismatches in the coefficient of thermal expansion (CTE), dissimilar materials tend to develop stress concentrations at their interfaces, which can accelerate the failure of power modules under long-time fatigue loading.

Fig. 11 shows the Von Mises stress distributions for the three PCB embedded packaging cells. When the packaging cell with panel carrier is selected to utilize a heatsink pad for single-sided cooling, the stress is primarily concentrated at the die–panel interface, exceeding 1000 MPa, as shown in Fig. 11(a). Under dual-sided cooling, although the stress still concentrates mainly at the die–Panel interface (approximately 500 MPa), significant stress concentrations (around 360 MPa) also emerge at the junctions among the RDL, SiC MOSFET, and EMC, as depicted in Fig. 11(b). Therefore, employing dual-sided cooling can effectively reduce internal stress concentrations within the module. Similarly, when a lead-frame is used as the carrier, the stress is mainly concentrated at the die–lead-frame interface, with a maximum of approximately 390 MPa. In contrast, when an AMB

carrier is selected, a distinctly different phenomenon occurs: the most prominent stress concentration appears at the junction among the SiC MOSFET, RDL, and EMC, with the maximum about 332 MPa, and the peak stress at the SiC MOSFET–AMB interface is merely 250 MPa. It indicates that, unlike the other two packaging cells, the sandwich structure of the AMB can transfer the stress concentration away from the SiC MOSFET–carrier interface, thereby serving as a stress buffer. Compared with the dual-sided cooled panel and lead-frame packaging cells, the maximum stress can be reduced by approximately 34% .

Fig. 12 shows the deformation of the three PCB embedded packaging cells. When cooling is provided by a single-sided heatsink pad, the panel carrier cell experiences a maximum deformation of approximately 1.43×10^{-4} m, as shown in Fig. 12(a). In contrast, with dual-sided cooling, the maximum deformation decreases to 3.81×10^{-5} m, as illustrated in Fig. 12(b). The regions exhibiting the greatest deformation are located around the operating SiC MOSFET, indicating that dual-sided cooling contributes to reducing the deformation of the packaging cells. The packaging cell with a lead-frame carrier demonstrates a significantly lower deformation of only 1.86×10^{-5} m, with deformation primarily concentrated around the operating SiC MOSFET and along the module periphery. Among the three PCB embedded packaging cells, the solution employing an AMB carrier effectively minimizes module deformation, with the overall maximum deformation reaching only 9.5×10^{-6} m. As shown in Fig. 11(c), the AMB carrier packaging cell exhibits a more uniform stress distribution extending from the SiC MOS to the carrier. It indicates that the AMB absorbs a greater portion of the stress, and thus, the AMB carrier can be regarded as a buffering layer.

In summary, compared to panel and lead-frame carriers, employing AMB as the carrier can effectively mitigate the stress concentration and module deformation during the operation of SiC MOSFETs.

IV. Processing for PCB Embedded Packaging Cells

A. Processing Chart for PCB Embedded Packaging Cells

Fig. 13 depicts the process flowchart for the PCB embedded packaging cells with the panel carrier. The die employed in this article is 1200 V/80 A SiC MOSFET (S1M040120B from SICHAIN) with an $R_{ds(on)}$ of approximately 40 mΩ, and dimensions are approximately 4.134 mm $\times$ 3.74 mm $\times$ 0.2 mm. The top-side metallization utilizes a Ni/Pd/Au stack, while the back-side metallization comprises a Ti/Ni/Ag stack. The detailed packaging process is as follows.

First, a single-sided etching process is applied to the panel, which facilitates the separation of distinct functional zones and the formation of positioning grooves for the SiC MOSFETs and copper pads. Next, electrical connections are established via the die attach process. When pressure-assisted silver sintering and copper sintering are used, the dimensions of the sintering mold are insufficient to cover the entire panel. Therefore, the pressure-assisted approach requires dividing the panel into smaller units before conducting pressure-assisted sintering, as shown in the first step of Fig. 13. Nanosilver paste are dried at 120°C for 300 s.

TABLE III
Process Flow and Parameters Of Molding

Step	Temp. (°C)	Press (Kgf/cm^2)	Time (min)	Atmosphere
(1) EMC lamination	45	5	1	Vacuum
(2) Leveling	120	6	5	Vacuum
(3) Pre-drying	100	0	30	N_2
(4) Cu foil lamination	120	6	5	Vacuum
(5) Curing	180	0	120	N_2

Subsequently, the SiC MOSFETs are placed on the dried substrate with a force of 50 N. Finally, sintering is performed at 250°C with a pressure of 20 MPa for 20 min. Unfortunately, in this article, 3D stencil printing was not employed when designing the cavities on the AMB and lead-frame carriers, resulting in nonuniform printed layer thickness. This thickness variation led to localized stress concentration and cracking in the SiC MOSFET. Therefore, if cavities are introduced on the carriers to maintain uniform copper plating thickness, it is proposed to adopt 3D stencil printing or silver film sintering to ensure the flatness of the sintered layer.

Following the die attach, the molding process is required primarily to provide electrical insulation. The molding process is achieved by pressing EMC on the panel and laminating copper foil onto the EMC. The process comprises five main steps—EMC lamination, leveling, predrying, copper foil lamination, and curing—with key parameters given in Table III. To establish electrical connections, the surface after molding undergoes laser drilling to remove the EMC above the Source pad. CNC engraving is applied on the copper foil while laser drilling is used for creating EMC blind via. After fabricating the blind via, a strong oxidant is employed to eliminate residue, followed by polishing the via walls and the surfaces of the SiC MOSFETs.

After drilling and polishing, a chemical deposition of a 0.5 μm copper film is performed on the blind via walls to serve as a seed layer. Initially, following activator treatment, the EMC surface adsorbs a layer of active particles—typically palladium particles—which catalyze the reduction of copper ions to form initial copper nuclei. These nuclei then evolve into a catalytic layer that accelerates the reduction reaction, leading to continuous copper deposition that eventually covers the entire inner surface of the blind via. In addition to filling the blind vias, a copper layer is deposited on the opposite side to fill the gap formed after the assembly of the die attach unit, thereby establishing electrical connectivity.

Based on a predetermined circuit design, the copper foil is patterned through a series of steps—including photoresist coating, exposure, and etching—to implement the desired circuit logic. In addition, blind vias are etched on the RDL to enhance the interfacial bonding between the glass fiber reinforced PP and the RDL. After etching, the copper foil is treated with an acidic browning solution, which not only removes surface contaminants but also increases surface roughness. This treatment enhances the interfacial adhesion between the copper foil and the glass fiber-reinforced PP, effectively mitigating internal

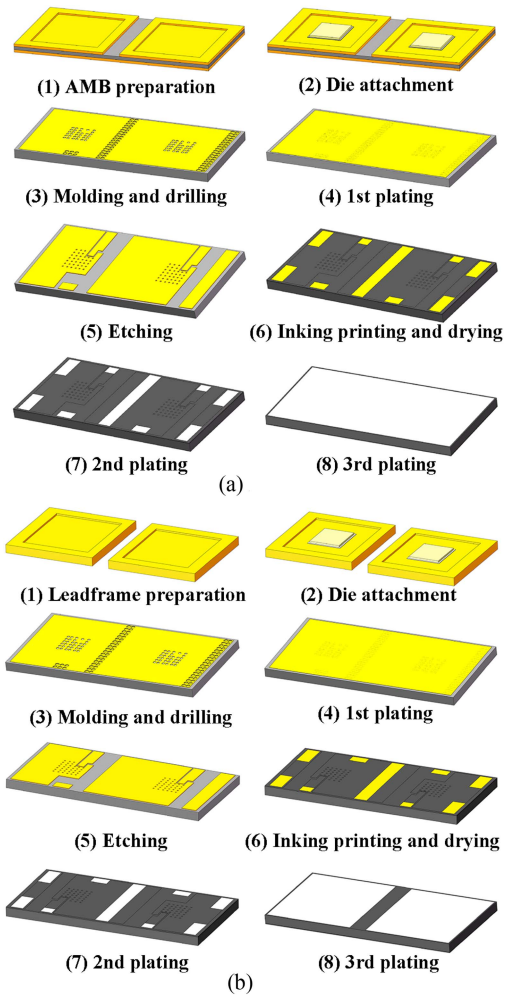

Fig. 14. Process flow of PCB embedded packaging cells with (a) AMB carrier and (b) lead-fame carrier.

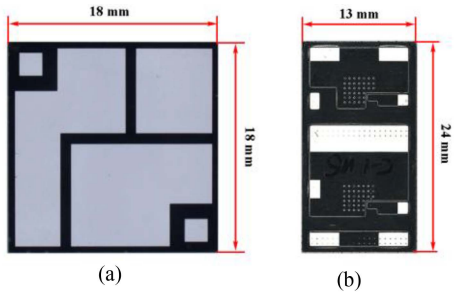

Fig. 15. Outline size of PCB embedded packaging cells selecting (a) panel and (b) AMB or lead-frame as carrier.

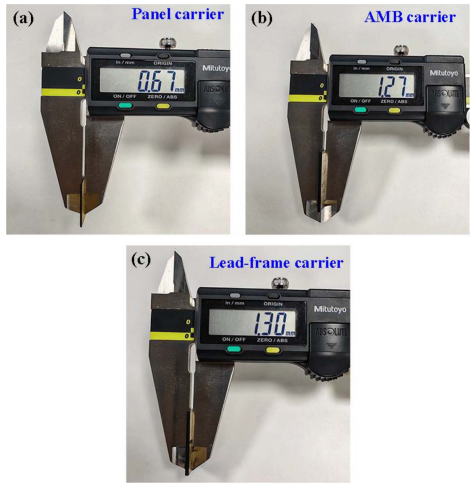

Fig. 16. Thickness of PCB embedded packaging cells: (a) panel carrier and (b) AMB carrier, and (c) lead-frame carrier.

stresses induced during deformation. Subsequently, the glass fiber-reinforced PP and the heatsink are laminated onto the surface of the patterned copper foil. Due to the minimal height difference between the copper foil and the EMC surface, both the glass fiber-reinforced PP and the heatsink can be simultaneously laminated in a single process. The lamination is conducted at 180°C under vacuum with a pressure of 6 Kgf/cm^2 for 7 min, followed by a curing process at 160°C in a nitrogen atmosphere for 120 min. Finally, silver plating is applied to the terminal pads and heatsink pads to prevent oxidation.

Similar to the process flow for PCB embedded packaging cell with panel carrier, the packaging processes for AMB and lead-frame carrier mainly consist of carrier preparation, die attach, molding and drilling, first plating, and etching, as shown in Fig. 14. However, there are also differences in the two major processes. First, the AMB carrier employs a sandwich structure composed of a symmetric 0.3 mm copper layer and a 0.4 mm Si_3N_4, whereas the lead-frame carrier is constructed solely as a copper frame. Second, after etching, an ink printing and drying process is predominantly used in place of glass fiber reinforced PP.

B. Appearance and Structure Analysis of PCB Embedded Packaging Cells

Figs. 15 and 16 illustrate the outline size and thicknesses of PCB embedded half-bridge packaging cells. The cell with a panel carrier exhibits a square structure, measuring approximately 18 mm × 18 mm. The packaging cell utilizing pressure-assisted sintering is approximately 0.67 mm. In contrast, the packaging cells with AMB or lead-frame carrier are rectangular, with dimensions of 13 mm in width and 24 mm in length. The thicknesses of the packaging cells with AMB and lead-frame carriers are approximately 1.27 mm and 1.30 mm, respectively. The ultra-thin solution of these packaging cells facilitates subsequent embedding into logic PCB.

To observe the internal structure of the module cell, sequential grinding was performed using water sandpapers with grits #80, #120, #240, #600, #800, #1200, and #1500. It was followed by mechanical polishing with a diamond spray polishing agent having a particle size of 0.5 μm. The polished cross section was then observed under an optical microscope to characterize the internal structure, as illustrated in Figs. 17 and 18.

Fig. 17 shows a cross section of PCB embedded packaging half-bridge cell with panel carrier. The measured thicknesses of the Heatsink Pad, the second molding layer, the RDL, and the 1st molding layer are approximately 30, 122, 70, and 86 μm,

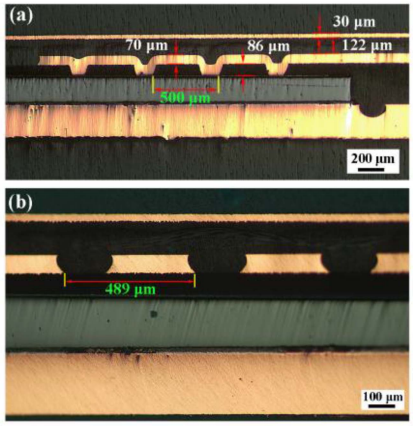

Fig. 17. Cross section of PCB embedded packaging cell with panel carrier: (a) cross-sectional view with RDL connected to SiC MOS and (b) cross-sectional view with RDL unconnected to SiC MOS.

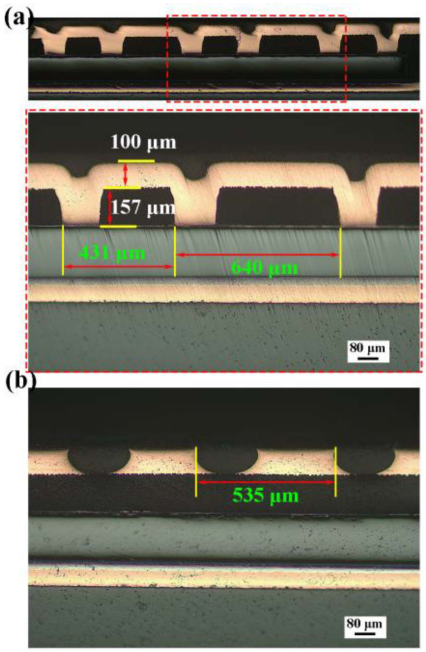

Fig. 18. Cross section of PCB embedded packaging cell with AMB carrier: (a) cross-sectional view with RDL connected to SiC MOS and (b) cross-sectional view with RDL unconnected to SiC MOS.

respectively. The top diameter, bottom diameter and thickness of vias for PCB embedded package with Panel carrier are 190, 132 and 86 μm. The diameter and thickness of PP filled vias are about 208 and 70 μm. The spacing between adjacent blind vias in the deposited copper is 500 μm, while the spacing between two neighboring blind vias filled with fiberglass-reinforced PP during second molding is approximately 489 μm. The blind vias used to fill fiberglass-reinforced PP help to improve bonding after molding.

Fig. 18 shows a cross section of PCB embedded packaging half-bridge cell with AMB carrier. It can be observed that the thicknesses of the RDL and the first molding layer are approximately 100 and 157 μm, respectively. The blind vias

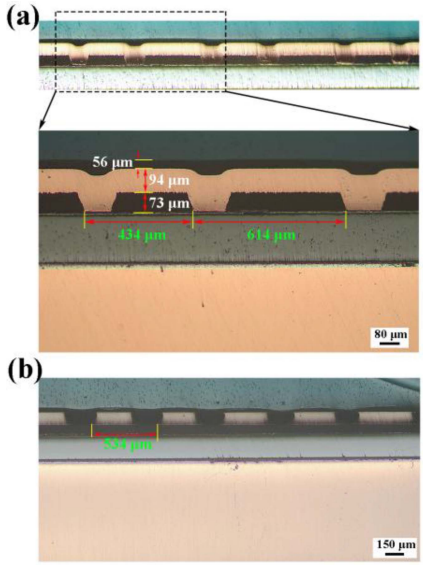

Fig. 19. Cross section of PCB embedded packaging cell with lead-frame carrier: (a) cross-sectional view with RDL connected to SiC MOS and (b) cross-sectional view with RDL unconnected to SiC MOS.

in the deposited copper are arranged in an alternating pattern of different pitches, with the smaller and larger spacings being approximately 431 and 640 μm, respectively, while the pitch for the ink-filled blind vias is about 535 μm. The top diameter, bottom diameter and thickness of deposited copper vias for PCB embedded package with AMB carrier are 199, 134 μm, and 157 μm. The diameter and thickness of PP filled vias are about 220 and 100 μm. Similarly, for the packaging cell with lead-frame carrier (see Fig. 19), the deposited copper blind vias also display an alternating arrangement, with small and large pitches of roughly 434 and 614 μm, respectively. The top diameter, bottom diameter and thickness of deposited copper vias for PCB embedded package with lead-frame carrier are 188, 143, and 73 μm. The diameter and thickness of PP filled vias are about 188 and 100 μm. The RDL layer and the overlying ink layer are approximately 94 and 56 μm thick, respectively, and the pitch of the ink-filled blind vias is around 534 μm. However, the first molding layer thickness is reduced to 73 μm, which accounts for the slightly lower parasitic inductance observed in the cell with lead-frame carrier compared to the AMB carrier.

In summary, the process flow for the three types of PCB embedded packaging cells is mainly divided into carrier preparation, die attach, first molding and drilling, first plating, etching, second molding or ink printing and drying, and final plating. The packaging cells selecting panel, AMB, and lead-frame as carriers measure approximately 18 mm $\times$ 18 mm $\times$ 0.67 mm, 13 mm $\times$ 24 mm $\times$ 1.27 mm, and 13 mm $\times$ 24 mm $\times$ 1.3 mm.

V. Package Performance Characterization

A. Thermal Resistance Characterization

To evaluate the thermal performance of the three PCB embedded packaging cells, a Mentor power tester was used to calibrate the K factor and measure the $R_{\mathrm{th}j\text{-}c}$, as illustrated in Fig. 20. For

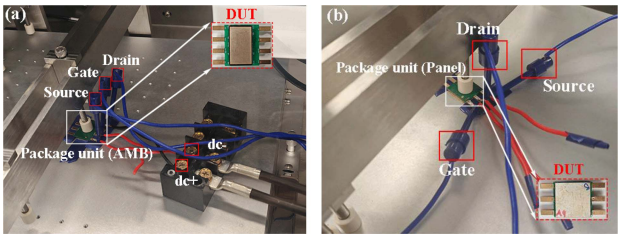

Fig. 20. (a) Thermal resistance test set up. (b) K-factor calibration set up.

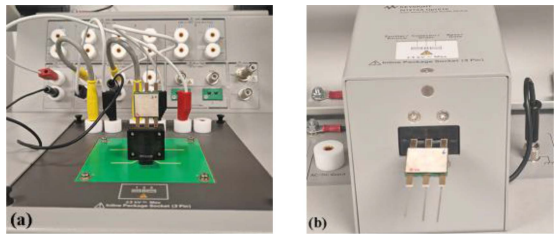

Fig. 22 Fixture for (a) static parameter measurement and (b) capacitance measurement.

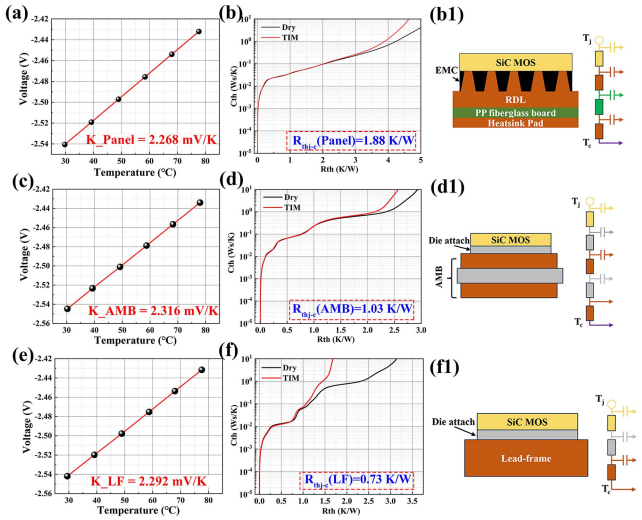

Fig. 21. (a), (c), (e) K-factor calibration, (b), (d), (f) Cumulative structure function curves, and (b1) (d1) (f1) thermal resistance network model of thermal resistance for PCB embedded packaging cells: (a), (b), (b1) panel carrier, (c), (d), (d1) AMB carrier, (e), (f), (f1) lead-frame carrier.

the K-factor calibration, the temperature was raised from 30 °C to 80 °C using a silicon oil heating method, with measurements taken at 10 °C intervals. A temperature fluctuation of less than 0.5 °C was maintained for 120 s as the stability criterion, and the body diode voltage was recorded at the specific temperature using a test current of 10 mA. The thermal grease used in this research is Xunyuan, with the thermal conductivity higher than 4.95 W/mK. Finally, the K factor was determined by linear fitting. To mitigate the effects of the SiC MOSFET wafer process and packaging on the K factor, each device under test was individually calibrated, as shown in Fig. 21. It is evident that slight differences exist in the K factors among packaging cells with various carriers.

The thermal resistance test was conducted using the body diode heating method, with a heating current of 9 A, a test current of 10 mA, and a gate voltage of –5 V. In order to ensure sufficient heating and cooling, the heating and cooling durations were set to 70 and 90 s, respectively. During the thermal resistance measurement, the water-cooled plate was operated with a flow rate of 20 L/min and a water temperature of 30 °C. Moreover, throughout both the K-factor calibration and the thermal resistance tests, the heatsink pad of the PCB embedded packaging cell with panel carrier, as well as the backsides of the AMB and lead-frame carriers, were in direct contact with the cooling plate, as depicted in Fig. 20.

Fig. 21 shows the cumulative structure function curves, K-factor calibration and thermal resistance network model of the PCB embedded half-bridge packaging cells, where silver sintering is selected as die attach process. There is little difference in the K-factors among the three packaging cells, as shown in Fig. 21(a)–(e). For the panel carrier, the $R_{\mathrm{th}j\text{-}c}$ is approximately 1.88 K/W. For the AMB carrier, the packaging cells display $R_{\mathrm{th}j\text{-}c}$ about 1.03 K/W. For the lead-frame carrier, the $R_{\mathrm{th}j\text{-}c}$ of the packaging cell is the lowest, approximately 0.73 K/W. Thus, among these three PCB embedded packaging cells, when silver sintering is uniformly adopted for die attach, the lead-frame carrier exhibits $R_{\mathrm{th}j\text{-}c}$ that is 61% and 29% lower than those for the panel and AMB carriers, respectively. According to the thermal resistance network model [see Fig. 21(b1), (d1), and (f1)], the relatively high thermal resistance of the embedded packaging with panel carrier is primarily attributed to the low thermal conductivity of the PP fiberglass board. In contrast, the thermal resistance of the embedded packaging with AMB carrier is lower than that with lead-frame carrier, mainly due to the ceramic materials.

In summary, the PCB embedded packaging cell with panel carrier exhibits the highest thermal resistance, whereas the lead-frame carrier demonstrates the lowest.

B. Static Characterization for the Three PCB Embedded Packing Cells

To evaluate the electrical performance of the three PCB embedded packaging cells, parasitic capacitance, and static parameter tests were conducted using the power device analyzer (B1505A). The static parameters measured included output characteristic curves, breakdown voltage, threshold voltage [V_{GS}(th)], gate leakage current (I_{GSS}), drain leakage current (I_{DSS}), and body diode forward voltage drop (V_{SD}). Fig. 22 shows the fixture employed for static parameter tests and parasitic capacitance tests.

Fig. 23 shows the output characteristics of the three PCB embedded packaging cells. The drain-source voltage (V_{DS}) is swept from 0 to 10 V, while the gate-source voltage (V_{GS}) is set from 7 to 15 V in 2 V increments. As shown in Fig. 23, with increasing V_{GS}, the differences between the output characteristic curves of the bare die and the packaged cells diminish. Notably, it reveals that there is no distinct boundary between the linear and saturation regions of SiC MOSFETs. There is no tendency for the drain current (I_D) to saturate as the V_{DS} increases. It can also be observed that for the same V_{GS} and V_{DS}, the I_D

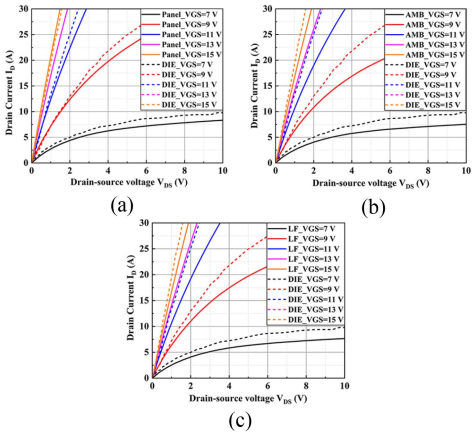

Fig. 23 Output characteristics of PCB embedded packaging cells selecting (a) panel, (b) AMB, and (c) lead-frame as carriers.

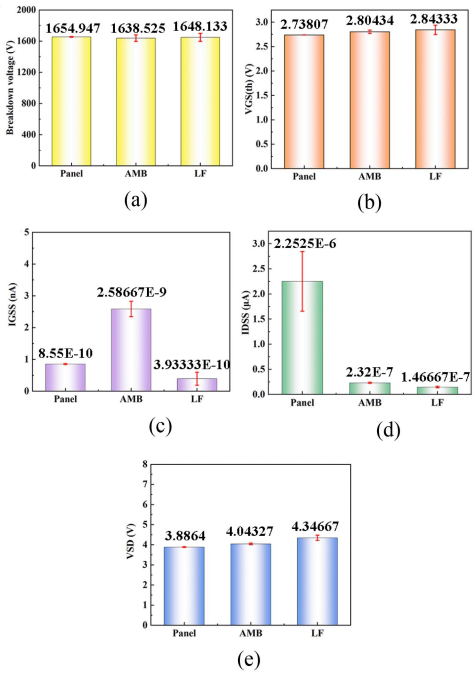

Fig. 24 Static parameter measurements of PCB embedded packaging cells. (a) Breakdown voltage. (b) V_{GS}(th), (c) I_{GSS}. (d) I_{DSS}. (e) V_{SD}.

of the packaging cells is lower than that of the bare die due to the presence of package parasitic resistance. In addition, based on the above simulation results, it suggests that the parasitic resistance of the packaging cell selecting panel as carrier are significantly lower than the other. In conclusion, its output characteristic curve after packaging is closer to that of bare die.

Fig. 24 shows the static parameter measurements of PCB embedded package cells. The breakdown voltage was tested under conditions specified in the datasheet: $V_{\mathrm{GS}} = 0$ V and $I_D = 100\ \mu$A, with a lower limit of 1200 V. As shown in Fig. 24(a), the breakdown voltages of the three PCB embedded packaging cells are approximately 1660 V, exhibiting good consistency and compliance with specifications. The test conditions for the threshold voltage are $V_{\mathrm{DS}} = 10$ V and $I_D = 10$ mA. Fig. 24(b) shows that the threshold voltages of the three packaging cells

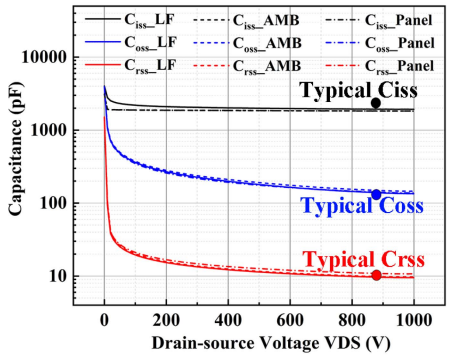

Fig. 25. C_{iss}, C_{oss}, and C_{rss} of PCB embedded packaging cells.

are around 2.8 V, also meeting the specifications. Fig. 24(c) and (d) illustrates the gate leakage current (I_{GSS}) and drain leakage current (I_{DSS}) of the three packaging cells, respectively. The I_{GSS} was tested with $V_{\mathrm{DS}} = 0$ V and $V_{\mathrm{GS}} = 15$ V, while the I_{DSS} was measured under $V_{\mathrm{DS}} = 1200$ V and $V_{\mathrm{GS}} = 0$ V. The maximum for I_{GSS} and I_{DSS} are 100 nA and 10 μA, respectively. It can be observed that, despite some differences among the three packaging cells, both I_{GSS} and I_{DSS} are significantly lower than the test specification. Fig. 24(e) displays the body diode forward voltage (V_{SD}) of the three packaging cells, tested under $V_{\mathrm{GS}} = -4$ V and $I_{\mathrm{SD}} = 20$ A. It can be observed that the V_{SD} of the three packaging cells is approximately 4 V, with the packaging cell selecting panel as the carrier exhibiting the lowest V_{SD}, primarily attributed to the lower parasitic parameters.

The dynamic characteristics of SiC MOSFETs are predominantly governed by the charging and discharging of parasitic capacitances, which primarily consist of the gate-source capacitance (C_{GS}), the drain-source capacitance (C_{DS}), and the gate-drain capacitance (C_{GD}) [43]. The latter, often referred to as the Miller capacitance, is mainly composed of a fixed gate oxide capacitance and a nonlinear depletion-layer capacitance. As the most critical and complex component, the Miller capacitance significantly affects crosstalk during switching. Parasitic capacitances are further categorized into the input capacitance (C_{iss}), output capacitance (C_{oss}), and reverse capacitance (C_{rss}) [44], which can be expressed as follows:

$$C_{\mathrm{iss}} = C_{\mathrm{GS}} + C_{\mathrm{GD}} \tag{3}$$

$$C_{\mathrm{oss}} = C_{\mathrm{DS}} + C_{\mathrm{GD}} \tag{4}$$

$$C_{\mathrm{rss}} = C_{\mathrm{GD}}. \tag{5}$$

The parasitic capacitance was measured under the following conditions: Freq: 100 kHz; $V_{\mathrm{ac}} = 25$ mV; $V_{\mathrm{GS}} = 0$ V; and $V_{\mathrm{DS}} = 1000$ V. The test results for the three PCB embedded packaging cells are shown in Fig. 25. The typical values for the bare die are approximately 2159 pF for C_{iss}, 127 pF for C_{oss}, and 10 pF for C_{rss}. As shown in Fig. 25, as V_{DS} increases from 0 to 1000 V, the parasitic capacitances tend to gradually stabilize. After packaging, C_{iss}, C_{oss}, and C_{rss} remain close to the typical values of bare die.

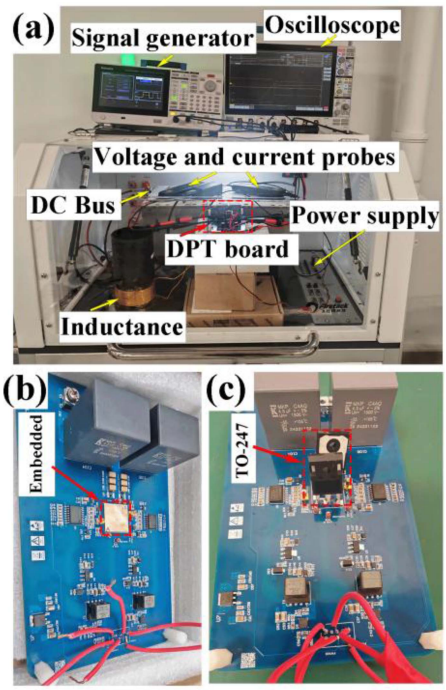

Fig. 26. (a) DPT experimental set up. (b) DPT board for embedded packaging cell. (c) DPT board for TO-247.

C. Double Pulse Tests

The double-pulse test (DPT) was conducted to evaluate the dynamic switching behavior of the packaged modules. The experimental setup is shown in Fig. 26(a). In this setup, the power supply and dc-bus voltage are integrated within the equipment. The DPT board, current and voltage probes, and the air-core inductor are enclosed within a glass chamber to ensure safe operation. The signal generator and oscilloscope are positioned on top of the equipment for convenient control and measurement. The DPT was performed at a voltage of 800 V, with an air-core inductance of approximately 100 μH. The V_{DS} was measured using a Tektronix THDP0200 differential probe (200 MHz, 1.5 kV). The drain current (I_D) was captured by a PEM Rogowski Current Waveform Transducer, while the V_{GS} was measured with a CYBERTEL OPB6050 isolated probe (500 MHz). Unfortunately, due to cavities in the die-attach regions of the AMB and lead-frame carriers, the printed silver paste became tilted during printing, leading to stress concentration and subsequent die damage during sintering. As a result, this sample could not be subjected to the DPT. Nevertheless, the advantages of the embedded packaging can still be evaluated by comparing the DPT results between the panel carrier and the TO-247 package. To ensure a fair comparison, the layout of the DPT test boards was kept identical, as shown in Fig. 26(b) and (c). In the DPT test, the high-side takes the charge of switching ON and OFF, while the body diode of low-side is used to reverse recovery. The turn-ON and turn-OFF gate resistances for the embedded packaging cell are both set to 5 Ω, while those for the TO-247 half bridge are set to 5 and 1 Ω, respectively. This configuration ensures that the *di/dt*(OFF) can be compared under the same voltage overshoot.

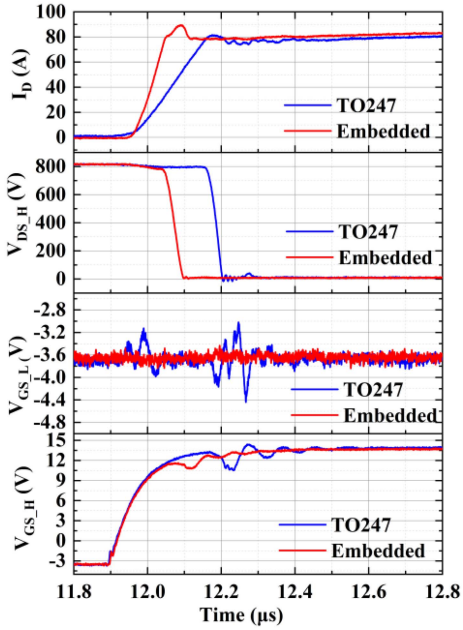

Fig. 27. Comparison of turn ON waveforms for embedded packaging cell and TO-247.

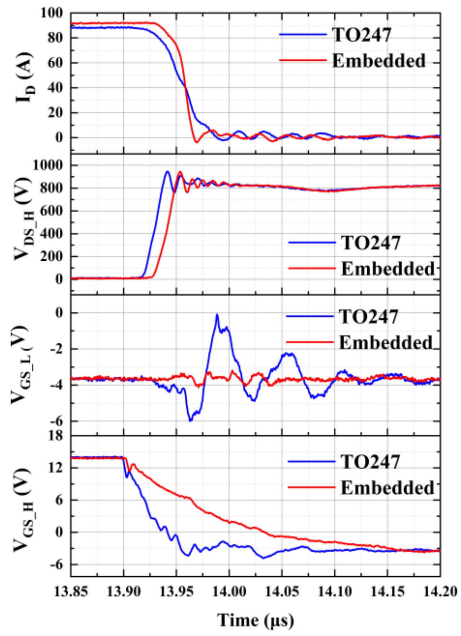

Fig. 28. Comparison of turn OFF waveforms for embedded packaging cell and TO-247.

Figs. 27 and 28 show the turn-ON and turn-OFF waveforms, respectively. Table IV compares the overshoot, switching speed, crosstalk, and switching losses between the TO-247 half bridge and the embedded packaging cell. As shown, under the same overshoot, the embedded packaging cell exhibits a turn-OFF *di/dt* of 10.82 A/ns, approximately 3.5 times that of the TO-247 half bridge. Consequently, the parasitic inductance of the embedded package is calculated to be 13.31 nH, while that of the TO-247 half-bridge is 47.25 nH. The measured values are slightly higher

TABLE IV
KEY PARAMETERS COMPARISON OF TO247 AND EMBEDDED PACKAGING CELL

Items	TO-247	Embedded packaging cell
Overshoot	946 V	944 V
di/dt (off)	3.09 A/ns	10.82 A/ns
di/dt (on)	0.411 A/ns	0.989 A/ns
Crosstalk (on)	−3.02 V	−3.43 V
Crosstalk (off)	−5.9 V	−4.1 V
E_{on}	6.89 mJ	3.52 mJ
E_{off}	1.46 mJ	1.17 mJ

due to unavoidable parasitic inductance introduced during PCB layout design. Based on previous research [45], the parasitic inductance of the TO-247 half-bridge power loop is approximately 36.9 nH, from which the intrinsic parasitic inductance of the embedded module can be roughly estimated as 2.96 nH—close to the simulation results. Furthermore, as shown in Figs. 27 and 28, the turn-ON and turn-OFF crosstalk of the embedded package are -3.43 and -4.1 V, respectively, which are significantly smaller than those of the TO-247 half-bridge. In addition, the turn-on and turn-off loss of the embedded package are 3.52 and 1.17 mJ, respectively, compared to 6.89 and 1.46 mJ for the TO-247 package. This corresponds to only 51% and 80% of the switching energy losses for TO-247 half-bridge. It clearly indicates that the embedded package achieves much lower switching losses. Moreover, the switching waveforms of the embedded package are noticeably smoother than those of the TO-247 half-bridge, primarily due to its significantly lower stray inductance. Based on the parameter comparison above, the embedded packaging cell can be applied at higher switching speeds; however, this also results in increased crosstalk. Therefore, when employing the embedded packaging cell, it is necessary to implement a Miller clamping in the gate driver and minimize the gate loop inductance. If the embedded packaging cell needs to be extended to higher-frequency applications, it is necessary to counteract common-mode interference such as selecting gate drivers with high CMTI, adding Y-capacitors, and designing appropriate filters.

In summary, the embedded packaging demonstrates superior switching performance compared to the conventional TO-247.

VI. CONCLUSION

In this article, three distinct PCB embedded 1200 V SiC MOSFET half-bridge packaging cells were designed and evaluated, employing an innovative RDL technique to replace conventional bonding wires. The packaging process for the three solutions is similar and relatively simple, involving key steps such as die attach, molding and drilling, plating, and etching. Notably, the single-layer RDL-even without the benefit of mutual inductance cancellation- can reduce the parasitic inductance in both the power and gate loops to under 5 nH. When mutual inductance cancellation is applied, the power loop inductance of the packaging cell with panel carrier can be reduced to 2.4 nH (at 10 MHz), while the gate loop inductance of the packaging cells with AMB and lead-frame carriers can be lowered to 1.57 nH (at 10 MHz). Thermal analysis shows that, under single-sided cooling, the packaging cell with panel carrier exhibits the highest $R_{\mathrm{th}j\text{-}c}$ at around 1.88 K/W, which can be further reduced to 0.58 K/W with dual-sided cooling. The solutions using the AMB and lead-frame carriers achieve $R_{\mathrm{th}j\text{-}c}$ values of 1.03 and 0.73 K/W, respectively, with the sandwich structure of the AMB cell reducing stress and deformation by up to 34% and 75% . All cells feature a compact design (panel: 18 × 18 × 0.67 mm; AMB/lead-frame: 13 mm × 24 mm × 1.27 mm/1.30 mm) and meet static and switching specifications. In summary, the packaging cell with lead-frame, despite utilizing the SiC MOSFET drain as the cooling surface, offers ultra-low parasitic inductance and excellent thermal performance for TO package replacement in specific applications. The packaging cell with AMB, with superior thermal dissipation, low stress, minimal deformation, and outstanding electrical insulation, is ideal for high-power applications such as traction inverters, while the solution with panel carrier holds promise for dual-sided cooling applications. However, several practical guidelines may be useful for readers during the design and development process.

1) From a design perspective, adopting two-layer or multilayer RDL structures can effectively reduce the module loop inductance.
2) From a manufacturing perspective, incorporating die-top system processes or applying thick copper plating (>15 μm) on the chip surface can help prevent chip damage during blind via fabrication.
3) If cavities are introduced on the carriers to maintain uniform copper-plating thickness, it is proposed to adopt 3D stencil printing or silver film sintering to ensure the flatness of the sintered layer.

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