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An Under Voltage Load Shedding Scheme Based on a Short Term Voltage Instability Detection Method

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Abstract: Faster detection of faults, can lead to better and more efficient control of power system against cascading failures triggered by the faults. This article presents a novel detection algorithm using statistical methods for the detection of events that lead to FIDVR. Furthermore we show that the algorithm is computationally efficient and quick enough to provide the control inputs to an UVLS scheme using in-feed PMU data. Thus, it is ensured that the minimal level of load to be shed is determined on-the-fly as the event develops.

Abbreviations

AC	Air Conditioner
CCT	Critical Clearing Time
CLM	Composite Load Model
FIDVR	Fault Induced Dynamic Voltage Recovery
PMU	Phasor Measurement Units
QCD	Quickest Change Detection
TCP/IP	Transmission Control Protocol/Internet Protocol
UVLS	Under Voltage Load Shedding

Nomenclature

f	Fraction of load shed.
Fd	Fault duration.
$P_i(t)$	Active power injected at a bus i at time t.
PL	Load active power.
P	Rated maximum active power of the load.
$Q_i(t)$	Reactive power injected at a bus i at time t.
QL	Load reactive power.
Q	Rated maximum reactive power of the load.
tf	Time of intial occurance of the fault.
$\theta_i(t)$	Phase angle of bus i at time t.
$V_i(t)$	Voltage of bus i at time t.
$W_{(b)}$	Sequence of statistics calculated for bus b.
$W_{(m,n)}$	Sequence of statistics calculated for line m and n.

1 Introduction

With the advent of PMU technologies, modern power system control rooms are getting equipped with systems capable of real-time health monitoring of the electricity grid. Such systems are capable of reporting the various stability aspects of power system such as rotor angle stability or long-term voltage stability. Yet, they require the insight of a control room operator to safeguard the system during a catastrophic cascading failure, like a blackout. With an operator in the loop, on-the-fly control of power system can be done at the order of several hundreds of seconds. A short-term voltage instability phenomenon, such as FIDVR, can also cause a cascading power failure and demands faster control action.

An FIDVR event occurs in the power systems with large penetration of AC loads, especially during the midsummer season, and is characterized by a prolonged voltage sag existing for a few seconds (most often less than 30 seconds). This voltage sag behavior is triggered by severe transmission line faults, like outage of a line or short circuit faults. Such faults cause the stalling of the induction motor loads and other electronic loads leading to increased reactive power consumption. The increased reactive power consumption is usually about 5-8 times the normal. The duration of the fault clearance is an important aspect in the mitigation of an FIDVR phenomenon, as it determines the post fault voltage. Many real-world power systems, such as [1, 2] have experienced the FIDVR event when the CCT i.e. the minimum time required to clear the fault, is greater than 6 cycles. Recent references have proposed methods for detection of FIDVR events, such as short term voltage instability indicator [3] and transient voltage severity index [4]. These detection methods can be used as an input to determine the mitigation strategy to control and prevent an FIDVR event.

Under voltage load shedding is the most effective and economic mitigation strategy for voltage instability events [5]. Heuristic optimization based UVLS schemes [6, 7] are best to minimize the amount of active power load shedding for a conventional and mid-term voltage stability problems. These methods are, however, time consuming and hence not suitable for short term voltage instability events. For an FIDVR event mitigation, a stage based UVLS scheme, using the simplest method [8] of monitoring the voltage and its rate-of-change and using it to determine a projected voltage recovery time, can be very effective. More recent references have used new methods, such as kinetic energy calculation based on inertia of induction motors, speed estimation of induction motors [10] and adaptive neuro-fussy inference system [11], to calculate the exact amount of load to be shed. The main advantages of the methods are the possibility of having on-line implementation, but the amount of load to be shed using the UVLS scheme is either estimated [9, 10] or calculated based on a black box method that is to be trained off-line [11].

In this paper we propose a centralized stage based UVLS scheme using a novel detection method. The proposed detection method uses voltage measurements from the buses in the transmission network to determine the exact duration and location of the fault. Since dynamics of an FIDVR event is determined by the duration and location of the fault, the fault detection plays a crucial role in determining the amount of load to be shed. The proposed detection method is based on the modification of the quickest change algorithm described in [13, 14]. In our approach, we use voltage measurements from PMUs to compute the sequence of statistics that is then being used as an input for a stage based UVLS scheme.

The rest of the article is divided into five main sections. Section 2 gives the basic description of QCD based on voltage measurements.

Section 3 explains the simulation results with separate subsections explaining the modeling of an FIVDR event, the implementation of the novel detection algorithm and the implementation of a stage based UVLS scheme. Section 4 shows the simulation results. Section 5 concludes the paper with a discussion and future scope of the work.

2 QCD based on Voltage Measurements

The QCD algorithm [13] was originally developed for detection of transmission line outages and it works based on the voltage angle difference between the measurement sets from PMU installed in the system. For the present paper, we modified it so as to make it based on difference between the voltage magnitudes and further used it for the proposed stage based under voltage load shedding. The rest of the section introduces the QCD formulation as described in [13] with modification made under the assumptions from [14] for the proposed voltage based detection method.

We consider a power system of N nodes denoted by a set $\chi = \{1, \ldots, N\}$, each of which correspond to a bus, and assume that there are L edges. Let (m, n) denote the transmission line between buses m and n. Let $V_i(t)_i(t)$ and $\theta_i(t)_i(t)$ denote the voltage magnitude and phase angle respectively, at bus i. Also, let $P_i(t)_i(t)$ and $Q_i(t)_i(t)$ denote the net active and reactive power respectively, injected at bus i. In order to represent the quasi-steady-state behavior of the power system, the real and reactive power balance components at each bus i can be written as:

$$P_i(t) = p_i(\theta_1(t), \ldots, \theta_N(t), V_1(t), \ldots, V_N(t)) \quad (1)$$

$$Q_i(t) = q_i(\theta_1(t), \ldots, \theta_N(t), V_1(t), \ldots, V_N(t)) \quad (2)$$

where $p_i(\cdot)$ and $q_i(\cdot)$ are functions used to represent the dependence on the network parameters. A linearized small signal power flow model is, however, considered and is used to perform the statistical test for change detection.

Considering the discretized version of the active and reactive power equations, we have

$$P_i[k] = p_i(\theta_1[k], \ldots, \theta_N[k], V_1[k], \ldots, V_N[k]) \quad (3)$$

$$Q_i[k] = q_i(\theta_1[k], \ldots, \theta_N[k], V_1[k], \ldots, V_N[k]) \quad (4)$$

where the time instant $t = k\Delta t$, $k = 1, 2, \ldots$ and $\Delta t > 0$. Defining $\Delta P_i[k] = P_i[k] - P_i[k-1]$, and $\Delta Q_i[k] = Q_i[k] - Q_i[k-1]$, and assuming that, for each bus i, $p_i(\cdot)$ and $q_i(\cdot)$ are continuously differentiable with respect to each θ_i and V_i at $\theta_i[k]$ and $V_i[k]$, $\Delta P_i[k]$ and $\Delta Q_i[k]$ can be expressed using first order Taylor series expansion of (3) and (4) as

$$\Delta P_i[k] \approx \sum_{j=1}^{N} a_{ij}[2k]\Delta\theta_j[k] + \sum_{j=1}^{N} b_{ij}[2k]\Delta V_j[k] \quad (5)$$

$$\Delta Q_i[k] \approx \sum_{j=1}^{N} c_{ij}[2k]\Delta\theta_j[k] + \sum_{j=1}^{N} d_{ij}[2k]\Delta V_j[k] \quad (6)$$

where a_{ij} and b_{ij} are, respectively, the derivatives with respect to θ_j and V_j of p_i, and c_{ij} and d_{ij} are, respectively, the derivatives with respect to θ_j and V_j of q_i.

Based on the decoupling assumptions in the analysis of transmission systems, we have $a_{ij}[k] \gg b_{ij}[k]$, and $d_{ij}[k] \gg c_{ij}[k]$, and using the dc assumptions, $a_{ij}[k]$ becomes only the function of network alone, that is $a_{ij}[k] = a_{ij}$ and $d_{ij}[k] = d_{ij}$, and the analysis is presented for $\Delta P_i[k]$, $\Delta Q_i[k]$, giving

$$\Delta P_i[k] \approx \sum_{j\in\chi, j\neq 1} a_{ij}\Delta\theta_j[k] \quad (7)$$

$$\Delta Q_i[k] \approx \sum_{j\in\chi, j\neq 1} d_{ij}\Delta V_j[k] \quad (8)$$

In matrix form, the above expression can be written as

$$\Delta P[k] \approx H_0\Delta\theta[k] \quad (9)$$

where $\Delta P[k] \in \mathbb{R}^{N-1}$ and $\Delta\theta[k] \in \mathbb{R}^{N-1}$, the entries of which are $\Delta P_i[k]$ and $\Delta\theta_i[k]$ for $i \in \chi$, $i \neq 1$.

$$\Delta Q[k] \approx L_0\Delta V[k] \quad (10)$$

where $\Delta Q[k] \in \mathbb{R}^{N-1}$ and $\Delta V[k] \in \mathbb{R}^{N-1}$, the entries of which are $\Delta P_i[k]$ and $\Delta\theta_i[k]$ for $i \in \chi$, $i \neq 1$.

The original QCD algorithm described in [13] calculates a sequence of statistics $W_{(m,n)}$ from phase angle measurements. The present paper considers the sequence of statistics based on voltage magnitude measurements. For this we consulted the decoupled DC approximations described in [14], from where it can be noted that H_0 and L_0 matrices are identical and equal to the network susceptance matrix. Hence, following the same procedure as in [13] and using (10) the sequence of statistics is determined as

$$W_{(m,n)}[k+1] = \left(W_{(m,n)}[k] + log\frac{f^{\sigma}_{(m,n)}(\Delta V[k+1])}{f_0(\Delta V[k+1])}\right)^{+} \quad (11)$$

where $W_{(m,n)}[0] = 0$ and the plus sign defined as $(x)^{+} = x$ if $x \geq 0$, otherwise $(x)^{+} = 0$.

We calculate the sequence of statistics W_b associated with particular bus in the system using (12) as

$$W_b = \sum_{(m,n)\in\beta} W_{(m,n)} \quad (12)$$

where β denotes the set of all lines (m, n) connected to particular bus b.

This value of $W_{(b)}$ is used to determine the input to the stage based UVLS scheme. Assessing the slope of the W_b value, the time corresponding to first occurrence of a three phase fault is determined. Next, the fault duration is computed assessing the slope of the W_b value corresponding to the fault clearance. The fault location is determined as the bus having highest slope of the W_b value. Thus, the detection algorithms determines the time of the initial occurrence of the fault tf, together with the fault duration and the fault location. This information is used as an input for the stage based UVLS scheme.

3 UVLS Scheme Implementation

Fig. 1 shows the interface diagram of the experimental setup made for the present study. RTDS/RSCAD software is used for real time

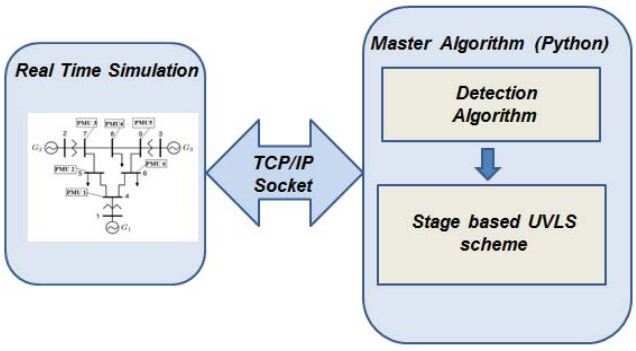


Fig. 1: Diagram of the experimental setup

simulation of the test system. This simulation provides measurement data in real-time emulating the in-feed of measurements to a control room. A TCP/IP socket connection is established via the GTNET

card of the RTDS hardware and this socket connection binds test system with a Python based master algorithm thus facilitating closed loop control. The detection algorithm is implemented in the master algorithm and it provides input to the UVLS scheme. The UVLS scheme is executed by the python based master algorithm in the following steps.

- Obtain the voltage measurement for the sampling instant $t = k\Delta t$ from the RTDS through the socket channel.
- Determine the location and duration of the fault using the detection algorithm.
- Compute the fraction of load to be shed based on the input from the detection algorithm.
- Share the information on the fraction of the load to be shed with the RTDS through the socket channel at specific time intervals.

The UVLS scheme is implemented as stage-based UVLS scheme [12] . Listing 1 shows the control logic used for the stage based UVLS scheme. The variable tf denotes the time corresponding to the initial occurrence of the fault and its value is provided by the detection algorithm.

```
if t > tf + 0.5 and V < 0.95:
  PL = 0.2*f*P
  QL = 0.2*f*Q
if t > tf + 0.6 and V < 0.95:
  PL = 0.4*f*P
  QL = 0.4*f*Q
if t > tf + 0.7  and V < 0.95:
  PL = 0.6*f*P
  QL = 0.6*f*Q
if t > tf + 0.8 and V < 0.95:
  PL = 0.8*f*P
  QL = 0.8*f*Q
```

Listing 1: Pseudocode of the control logic for UVLS scheme

The variables PL, QL, P, Q are as defined in the nomenclature section. The variable f denotes the increment in the shed load. The value of f determines the percentage of load shed at each time interval i.e. by selecting a value of 0.5 for the variable f, $f \cdot 0.2 \cdot 100 = 10\%$ of the load is shed in each time interval.

4 Simulation Results

The IEEE 9-bus system is used as the test system in this paper. The Fig. 2 shows the PMU locations in the test system and this system is simulated in RTDS as the representation of the actual power system. The simulation results section is further divided into three subsections, the first subsection explains the short term voltage instability event modeling, the second section explains the results of implementation of QCD as the detection algorithm and the third section explains the implementation of the stage based UVLS scheme.

4.1 Modeling of FIDVR event

Here we explain how an FIDVR event is added in the IEEE 9-bus system. Load at Bus 5 is replaced with the CLM as shown in Fig. 3. The FIDVR event is primarily caused by the composite load model in response to the three-phase fault that is not cleared in less than 3 cycles. The CLM model is created in resemblance to the model from [15] and the parameters of different components are mostly obtained from [16]. Some parameters are modified for the sake of better illustration of the FIDVR behavior. Fig. 4 shows an FIDVR event in the IEEE 9-bus system simulated using RTDS software for 5 seconds. The FIDVR event is triggered by a short circuit fault happening at Bus 5 at 0.2 seconds and lasting until 0.3 seconds. It can be noticed from Fig. 4 that the post fault voltage at Bus 5 has severe deviation.

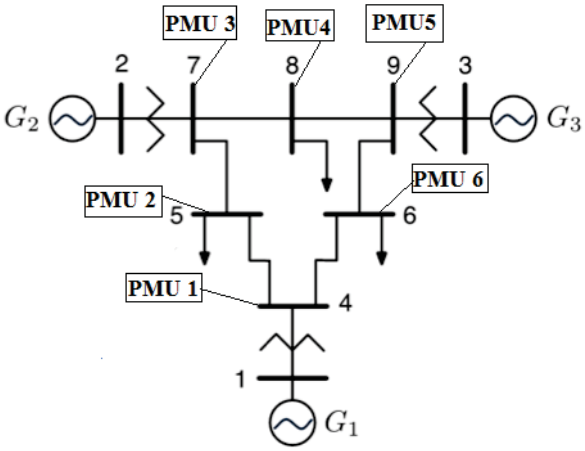


Fig. 2: IEEE 9-bus system with PMUs

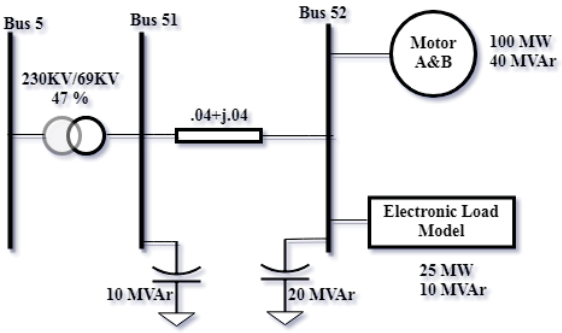


Fig. 3: Composite load model as specified in

4.2 Detection Algorithm Implementation

This section explains how novel detection algorithm presented in Section II is used for the detection of a three-phase short circuit faults along with the duration of the fault. Fig. 5 shows the sequence of statistics values calculated using the detection algorithm implemented in Python based master algorithm. The sequence of statistical values calculated corresponds to same short circuit fault as specified by Fig. 4.

The detection algorithm uses the voltages magnitude values as input at an in-feed data sample rate of 60 samples per second. First the sequence of statistics $W_{(m,n)}$ for each line (m, n) is calculated for a period of one second. The time taken by the Python based master algorithm for this calculation is 0.0624 seconds. In the case of the three-phase short circuit event as shown in Fig. 5, the slope of $W_{(m,n)}$ of the lines connected to that bus will be the highest at the moment of the fault and at the moment of the fault clearance. Since the fault is at Bus 5, the W_5 value, calculated as the sum of $W_{(4,5)}$ and $W_{(5,7)}$, has the highest value, as seen in Fig. 5b. Since this value is higher than W_b values of other buses, we can conclude that the dynamics of the post fault voltage of Bus 5 has severe deviation. This way the detection algorithm is able to detect the exact fault location with the initial time of occurrence of the fault and its duration in a time much less than 70 milliseconds.

Fig. 6 corresponds to a three-phase short circuit event occurring at Bus 5 at 0.2 seconds when the fault is cleared after different time durations. Fig. 6a shows the voltage values of Bus 5 corresponding

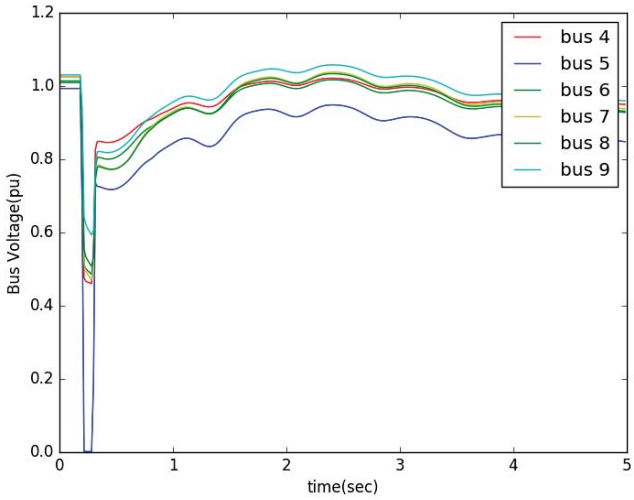


Fig. 4: Measured voltage values under a three-phase short circuit fault.

to different fault durations in range of 100 to 300ms, thus representing faults cleared in 5 cycles to 15 cycles of operation. It was noticed from the experimental results that the voltage shows no recovery for fault durations greater than 250 ms. Fig. 6b shows the sequence of statistics corresponding to Bus 5 i.e. W_b computed for the entire time-window by the detection algorithm. The detection algorithm detected these faults with the corresponding fault location and duration, utilizing the same principle as explained previously.

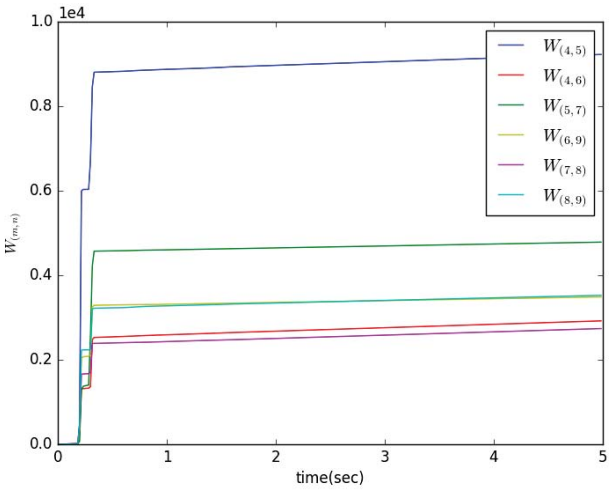
4.3 Stage based UVLS Scheme Implementation

Fig. 7 shows the stage based UVLS scheme implemented for three phase short circuit faults with different fault durations occurring at 0.1 seconds. For fault cases shown in fig. 7, by selecting the sampling instant as 0.5 seconds, with a data sampling rate of 60 samples the detection algorithm is able to detect the fault duration Fd and location in 0.0467 seconds. The fraction of the load to be shed i.e. the value of f is determined from a previously calculated look up table, as shown in Table 1. This value corresponds to the respective Fd value as computed by the detection algorithm. The f value is fed as an input to stage based UVLS scheme implemented in RTDS. The first stage of the UVLS is executed at 0.6 seconds and later stages are implemented in time intervals of .1 seconds till the voltage is recovered to a stable limit. For this paper this value was chosen as .95 pu and this value varies for different power system operator. The changes during the recovery by UVLS scheme are predominant in later stages as shown in the zoomed in portion in Fig. 7.

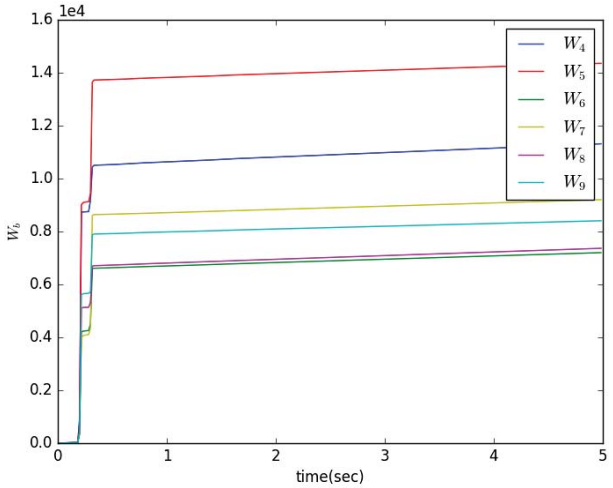
Thus, by detection of location, duration and starting time of a three phase short circuit fault, the stage based UVLS is implemented for the test system during the FIDVR caused by the same fault.

Table 1: Relation between fault duration and the fraction of load shed.

Fault duration $Fd[sec]$	Fraction of load shed $f[-]$
0.1	0.20
0.2	0.23



(a) $W_{(m,n)}$ values calculated.



(b) W_b values calculated.

Fig. 5: Sequence of statistics values calculated for three-phase short circuit fault.

5 Conclusion and Future Work

This paper presents a novel detection algorithm for the events triggering an FIDVR event. The detection algorithm further determines the event duration based on a metric calculation. This metric is further used to provide control inputs to a stage based UVLS scheme. Due to the short execution time, it is possible to have an on-line implementation of the proposed detection based UVLS scheme.

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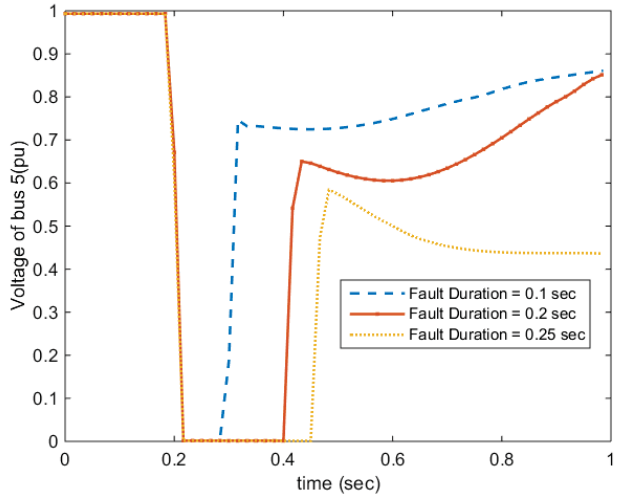
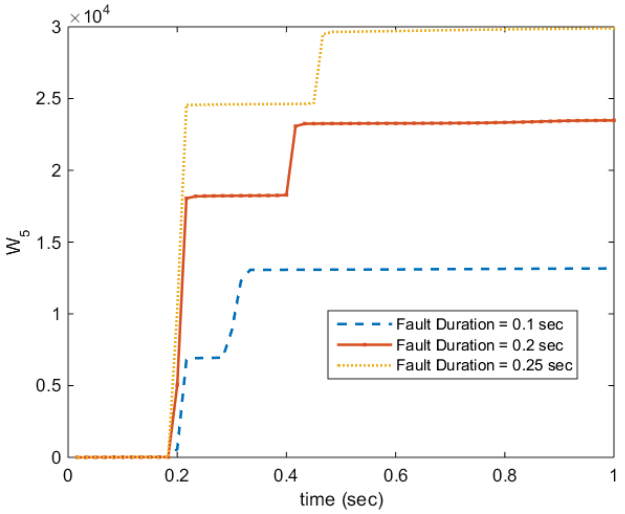


(a) Measured Voltage values of Bus 5.



(b) W_5 values calculated.

Fig. 6: Three-phase short circuit in Bus 5.

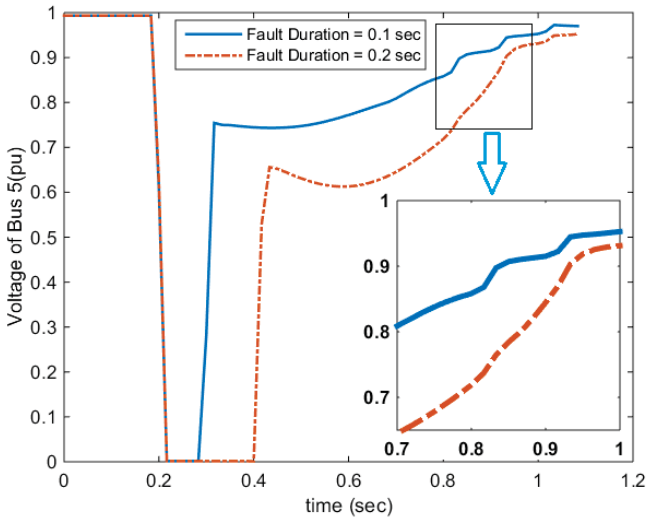


Fig. 7: Stage based UVLS implemented for different fault duration

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