Power Amplifier PAE and Ruggedness Optimization by Second-Harmonic Control

Marco Spirito, *Student Member, IEEE,* Leo C. N. de Vreede, *Member, IEEE,* Lis K. Nanver, *Member, IEEE,* Stephan Weber, and Joachim N. Burghartz, *Fellow, IEEE*

***Abstract*—Second-harmonic control is applied to optimize power-added efficiency (PAE) and ruggedness of silicon power amplifiers (PAs). A differential push-pull topology is chosen because it facilitates independent fundamental load and second-harmonic control. Various amplifiers using high-Q passives for fundamental and harmonic matching have been implemented. Experiments demonstrated an increase in PAE and ruggedness simultaneously even under high mismatch conditions. The amplifiers are operating in class-AB and are intended for use in the digital communication system (DCS) band.**

***Index Terms*—Differential output stages, power-added efficiency (PAE), ruggedness, second-harmonic termination.**

I. Introduction

ONE OF THE most difficult requirements to fulfill for power amplifiers (PAs) in mobile communication systems is the capability to handle high mismatch conditions while preserving a high power-added efficiency (PAE). This requirement on ruggedness generally leads to a compromise in the collector design of the bipolar devices. Compared with Si–SiGe, III-V technologies have the advantage of an inherently better tradeoff in device breakdown versus speed. This allows significant headroom during the design and development of the III-V-based PA modules. However, to achieve low-cost PAs, Si–SiGe technologies are quite often preferred. To enable this, two major problems have to be solved. First, the robustness of silicon-implemented designs under severe mismatch conditions must be improved without compromising the speed and gain of the device. Second, the high losses related to Si integrated passives must be lowered. Both points can be addressed by implementing low-loss matching networks in a high-resistivity silicon (HRS) technology. With these matching networks, proper harmonic terminations at the source and load of the active device can be provided. In this paper, we extend the conclusions of [1] and [2] to the differential push-pull amplifier architecture, which, in principle, can facilitate second-harmonic termination independent of the fundamental loading conditions. First, single-ended and differential class-AB PAs with second-harmonic termination are reviewed. Then, different topologies of passive structures providing high-quality second-harmonic shorts (2ndHS) and balun/matching operation are described and compared for their performances. Finally, we present various differential push-pull class-AB amplifiers for the digital communication system (DCS) band that utilize the passives developed for the harmonic matching. Using these amplifier configurations, an experimental verification of the theory will be given. The power levels of the designed PAs range from 20 to 26 dBm.

Manuscript received December 6, 2002; revised April 18, 2003. This work was supported by Secure Mobile Solutions, Infineon Technologies, Munich, Germany.

M. Spirito, L. C. N. de Vreede, L. K. Nanver, and J. N. Burghartz are with he Laboratory of Electronic Components, Technology and Materials, DIMES, Delft University of Technology, 2600 GB Delft, The Netherlands (e-mail: m.spirito@its.tudelft.nl).

S. Weber was with the Silicon Power Amplifier Group, Infineon Technology, D-81609 Munich, Germany. He is now with Cadence Design Systems GmbH, 85622 Feldkirchen, Germany.

Digital Object Identifier 10.1109/JSSC.2003.815918

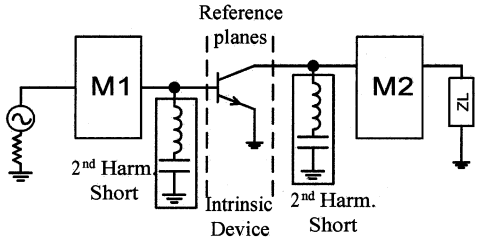


Fig. 1. Single-ended amplifier with second-harmonic shorts at the input and output of the active device.

II. Amplifier Operation

A. Single-Ended PAs

In [2], it was shown that varying the second-harmonic termination at the source and load of a single-ended amplifier can set the active device to operate in class-AB or the so-called inverse class-AB, where class-AB refers to the classical class-AB operation (voltage waveform sinusoidal, current waveform half-sinusoidal) with a maximum peak voltage of $2V_{\rm CE}$ and an output power of $(1/4)V_{\rm CE}\cdot {\rm I}_{\max {\rm class}-{\rm AB}}$ [1]. The inverse class-AB operation refers to an opposite behavior of the class-AB waveforms (voltage waveform half-sinusoidal, current waveform sinusoidal) with a higher maximum peak voltage of $\pi\cdot V_{\rm CE}$ and an output power given by $(\pi/8)V_{\rm CE}\cdot {\rm I}_{\max\ {\rm inverse\ class}-{\rm AB}}$ [1].

Both classes show a comparably high PAE (maximum collector efficiency of $\pi/4$). Although inverse class-AB was shown to be more robust with respect to load mismatch in terms of second-harmonic terminations, the preferred operation for our analysis is class-AB, since we want to improve the ruggedness by lowering the output voltage swing. We can achieve this device operation, in the single-ended configuration, by using 2ndHS at the input and output of the intrinsic device (Fig. 1) [2].

Note from this figure that the 2ndHS can be implemented using series resonators at the input and output of the ampli-

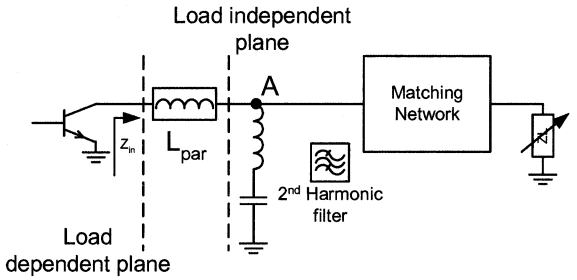


Fig. 2. Degradation of the 2ndHS for varying load conditions by the parasitic (bondwire) inductance.

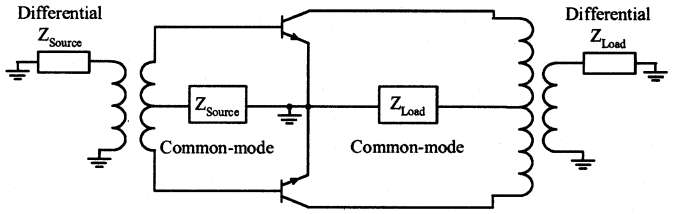


Fig. 3. Differential push-pull schematic used in the simulations with ideal transformers at the input and output.

fier. In a hybrid implementation (Fig. 2), bondwire and interconnect parasitics will be a part of the required inductance of the resonating harmonic short. Since the varying load is connected through the matching network to node A (Fig. 2), the short at the device reference plane becomes load dependent. Consequently, the short condition, for a given frequency, at the device-under-test (DUT) reference plane can only be achieved for a single $Z_{\rm load}$ value. This yields the conclusion that 2ndHS for single-ended configurations have to be integrated on chip, in order to minimize the effect of $L_{\rm par}$. Since integration of an effective short on a Si substrate will be limited by the quality factor Q of the inductor, most likely only a partial suppression of the voltage swing at the collector, due to the 2ndHS, will occur. This will complicate the enforcement of the required class-AB mode. Even more due to its limited Q, the series resonator will also affect the signal transfer at the fundamental, and consequently, it will also influence the PAE of the amplifier through its losses (as will be discussed in Section V-B). The above considerations have led to the conclusion that on-chip series-resonator shorts should only be applied at the input of the PA, since here the reduced power levels will yield a lower degradation of the PAE.

B. Differential PAs

Considering the push-pull stage shown in Fig. 3, we can repeat the analysis presented in [1] and [2] for single-ended devices. The simulation is performed using Agilent's Advance Design System (ADS); the active part is included through the mextram 503 model of the B6HFC bipolar transistor technology. Using an ideal transformer in our simulation we can decouple common-mode from differential signals [3]. The fundamental impedance at the input is set to a conjugate match to maximize the power transfer to the input of the active device and, consequently, enhance the gain. At the output, the desired impedance is found using a load-pull analysis for maximum $\rm P_{out}$ [4]. The second-harmonic impedance is controlled through the center tap

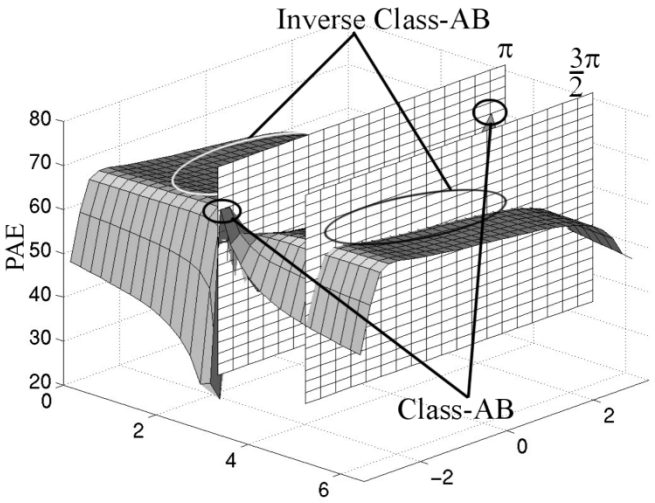


Fig. 4. Simulated PAE versus $\angle\Gamma_{\rm 2nd}$ source and load with $|\Gamma_{\rm 2nd}| = 1$, cross-section plane at π and $3/2\pi$.

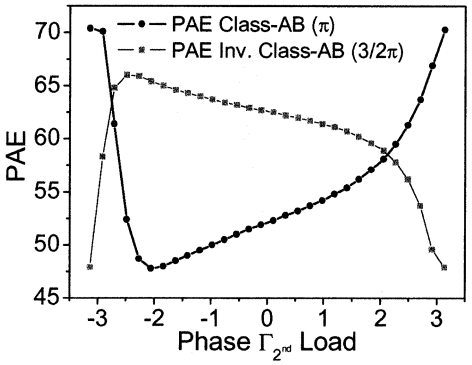


Fig. 5. Cross section of Fig. 3, for $\angle\Gamma_{\rm 2nd\ source} = \pi$ and $\angle\Gamma_{\rm 2nd\ source} = 3/2\pi$.

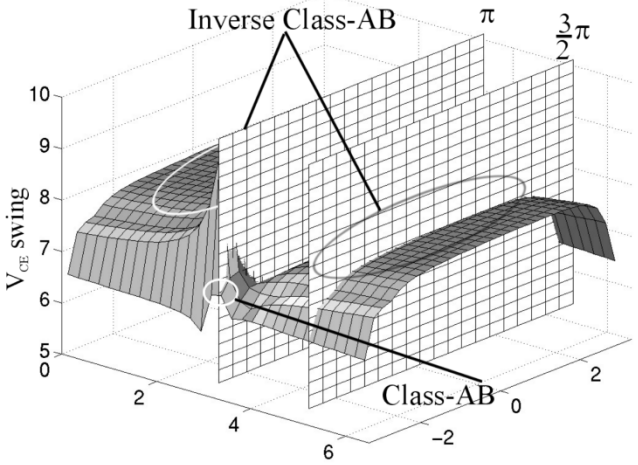


Fig. 6. Simulated $V_{\rm CE}$ voltage swing versus $\angle\Gamma_{\rm 2nd}$ source and load with $|\Gamma_{\rm 2nd}| = 1$, cross-section plane at π and $3/2\pi$.

of the transformer; the amplitude of the reflection coefficient will be kept constant to 1 and the phase swept over a 2π range.

The results of this analysis are similar to the single-ended case and are given in Figs. 4–7. The x and y axes of the three-dimensional plots represent the second-harmonic phase in radians

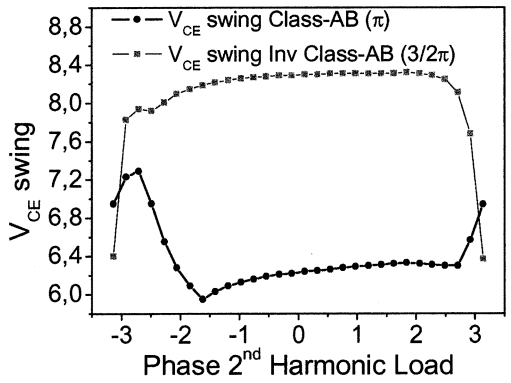


Fig. 7. Cross section of Fig. 5, for $\angle\Gamma_{\text{2nd source}} = \pi$ and $\angle\Gamma_{\text{2nd source}} = 3/2\pi$.

of, respectively, the load ($-\pi < \varphi < \pi$) and source phase ($0 < \varphi < 2\pi$). In Figs. 4 and 6, we can clearly identify the class-AB and inverse class-AB operating regions. The most important difference with the single-ended case is the even more constant PAE region for the inverse class-AB operation versus the second-harmonic terminations. From Figs. 5 and 7, it can be seen that class-AB (in and out 2ndHS) provides the highest PAE combined with the lowest V_{CE} swing.

III. Implementation of Second-Harmonic Shorts

Differentially driven amplifiers will generate even in-phase (common-mode) harmonics and odd anti-phase (differential-mode) harmonics. The orthogonality between fundamental and second-order components allows a decoupling in the matching networks [3]. This makes it possible, in principle, to circumvent the limitations of the single-ended topology with respect to the dependency of the 2ndHS on varying load conditions. Since most applications require an overall single-ended operation, baluns will be needed. It is, therefore, a logical step to implement the second-harmonic termination within the balun in order to obtain the lowest overall losses. One of the most suitable balun structures is the center-tapped transformer. Note that in this structure the common-mode signals will not couple to the secondary windings and, consequently, they only experience the impedance connected to the center tap. Under a differential excitation, the signal will couple to the secondary winding and (assuming a perfect balance) no signal will appear at the center tap. This ensures independence of the second-harmonic termination for a varying load condition (as provided by the antenna). In a real transformer, the coils are not perfectly coupled ($k < 1$), the value of the inductance is finite, and there will be losses related to the finite conductivity of the windings and the nonperfect isolation of the substrate.

This leads to an inductive behavior for the common-mode impedance (see L_{S} in Fig. 8). One can cancel this inductive behavior for the 2ndHS by creating a series resonance at the second-harmonic frequency using a capacitor at the center tap (C_{tap}) [see (1)], with L_S being the secondary winding inductance [see (2)].

$$C_{\text{tap}} = \frac{2}{\omega^2 \cdot L_S} \tag{1}$$

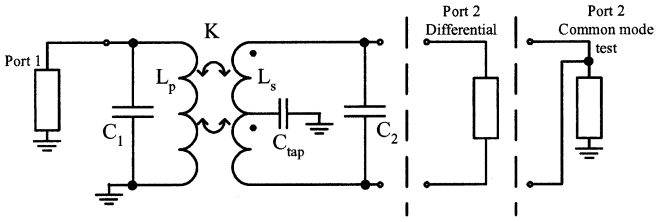


Fig. 8. Center-tapped transformer with nonideal coupling using port 2: as differential configuration for calculation of transfer parameters, and as common-mode test for calculation of common-mode impedances.

$$L_S = \frac{M^2}{k^2 \cdot L_P}. \tag{2}$$

Note that the nonideal coupling will also degrade the differential operation. To compensate for this, one can enforce a parallel resonance for both primary and secondary windings using shunt capacitors (C_1 and C_2 in Fig. 8). Doing so, the energy transfer is optimized for a given transformer structure and a chosen frequency. The metal and substrate losses will strongly affect the performance of the resonating transformer [5], but nevertheless, different transformer design optima are found for specific primary and secondary impedance levels.

IV. Implementation of the Push-Pull Amplifiers

Various topologies of the PA were designed and realized. Output power levels range from 20 to 26 dBm. An overview of the different circuit implementations is given in Table I. The technologies used for the circuit implementations are Infineon's modified B6HFC (three metals, $f_T = 25$ GHz, $\text{BV}_{\text{ceo}} = 5.2$ V) and the DIMES-04 process technology (two metals, $f_T = 25$ GHz, $\text{BV}_{\text{ceo}} = 4$ V). Infineon's transistor technology gives, in principle, the best performance for the active part of the high-power amplifier circuit, while the DIMES process allows the use of a high-ohmic substrate ($> 1000\ \Omega$·cm) and a thick top metal (3 μm) option, facilitating the integration of high-quality and low-loss passive structures such as coils and transformers.

V. Circuit Blocks

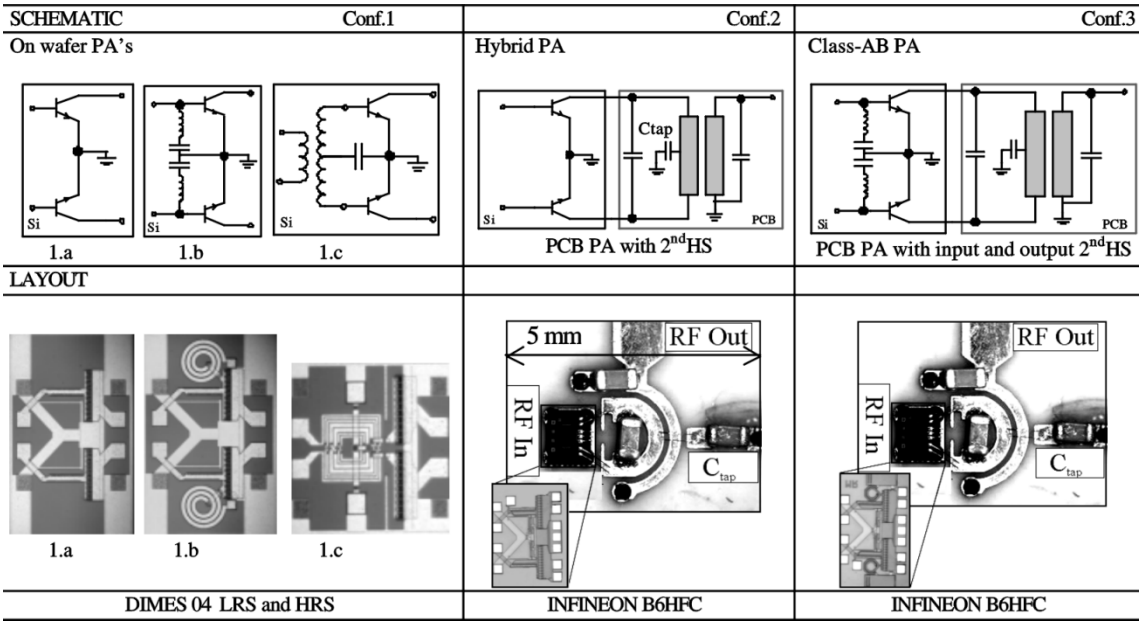
A. Active Core

The PA implemented in Infineon B6HFC technology is composed of twelve parallel transistors cells in each branch of the push-pull stage. Each cell has an active emitter area of 32 μm^2. The electrical configuration of the cells is two emitters, three bases, and two collector fingers. The output stage in the DIMES-04 technology consists of ten devices per branch, each with an emitter area of 32 μm^2 and the same finger configuration as the Infineon case. In both designs, ballasting resistors were omitted.

B. Series Resonators

A series resonator with one side grounded provides a harmonic short at its resonance frequency. The advantage of such a structure is its intrinsic simplicity and the small area occupancy, facilitating direct connection between base and emitter of the PA, minimizing the influence of parasitic inductance, as

TABLE I
CIRCUIT CONFIGURATIONS USED IN THE VARIOUS EXPERIMENTS (LRS: LOW RESISTIVITY SILICON, HRS: HIGH RESISTIVITY SILICON)



discussed in Section II-A. The spiral coil is the limiting factor of the resonator's Q since metal–insulator–metal (MIM) capacitors can achieve very high quality factors (over 50 in the technologies mentioned). A relatively low inductor Q results in a noneffective short for the second harmonic when the input impedance is relatively low, in our case, $Z_{\rm in}$ at $2 \cdot f_0 < 10\,\Omega$.

From Fig. 9, we can conclude that the achieved equivalent impedance for the 2ndHS at $2f_0$ is 10 and 5 Ω for the DIMES technologies with thin metal (1.4 μm) and is as low as 2.5 and 2.8 Ω for Infineon's B6HFC and DIMES HRS thick-metal technology, respectively. The latter two will be used in our experiments.

To achieve a good harmonic short (low ohmic value), the parasitic resistance of the inductor has to be low, yielding low inductance values. For this reason, the spiral inductors used in the circuits all have values below 1 nH.

The implemented resonators were realized using spiral inductors with two metal layers connected in parallel to reduce the series resistance [6]. The MIM capacitor in Infineon technology was realized using three metal layers to reduce the area occupancy. From Fig. 9, we can see that the influence of the series resistance of the metal line can degrade the performance of the short more than the substrate losses. Fig. 10 presents the S_{21} normalized to a 5-Ω port impedance, which is by approximation the input impedance level of the transistor. As can be seen from this figure, the frequency of the short can be accurately controlled by the capacitance value, while its reactance at f_0 is of limited influence for the applied port impedance.

Calculating the Q factor of the series resonator as

$$Q = \frac{f_r}{2} \frac{\partial \,\mathrm{phase}\,(Z)}{\partial f} \tag{3}$$

we obtain for the implemented structure a peak Q of 7 at the resonant frequency of $2f_0 = 3.6$ GHz.

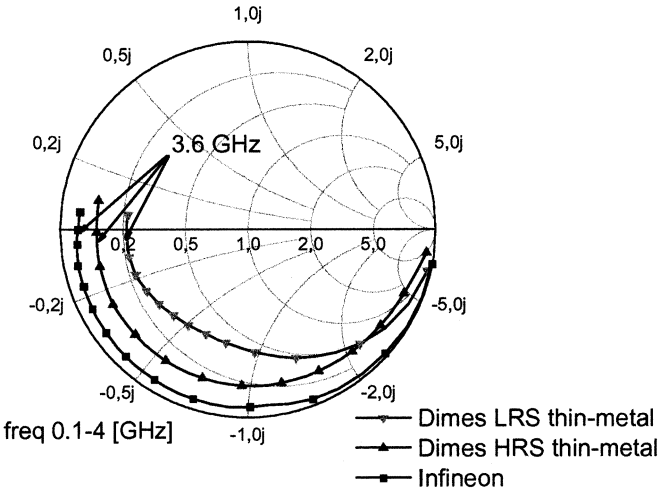


Fig. 9. One port measured data for the 2ndHS series resonator using DIMES and Infineon technology (marker at 3.6 GHz).

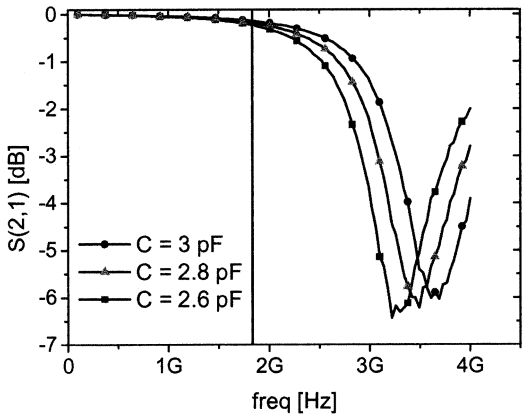


Fig. 10. Two port measured data of 2ndHS normalized to 5 Ω, Infineon technology (marker at $f_0 = 1.8$ GHz).

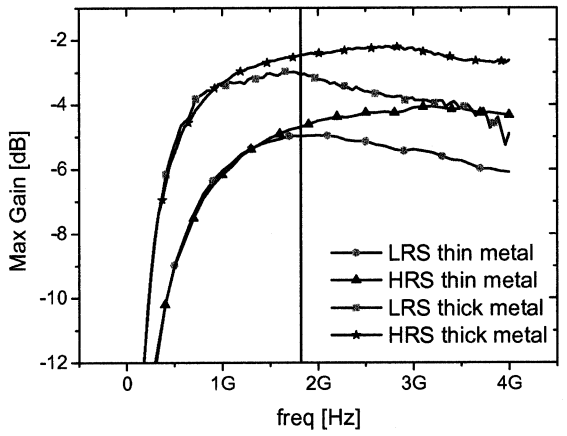


Fig. 11. Maximum available gain of DIMES-04 input transformer (differential-to-differential configuration) for various technology implementations (marker at $f_0 = 1.8$ GHz).

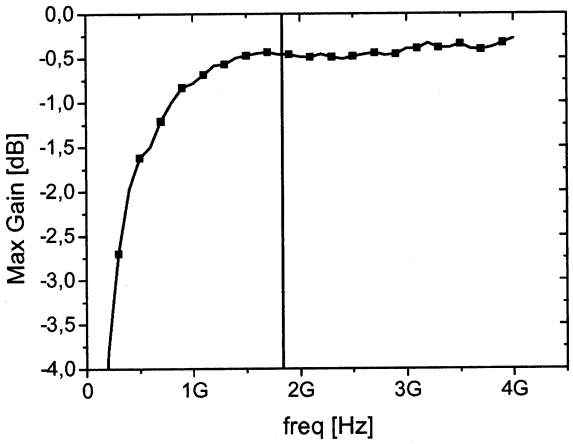


Fig. 13. Maximum available gain of coupled-line balun in single-ended-to-differential configuration (marker at $f_0 = 1.8$ GHz).

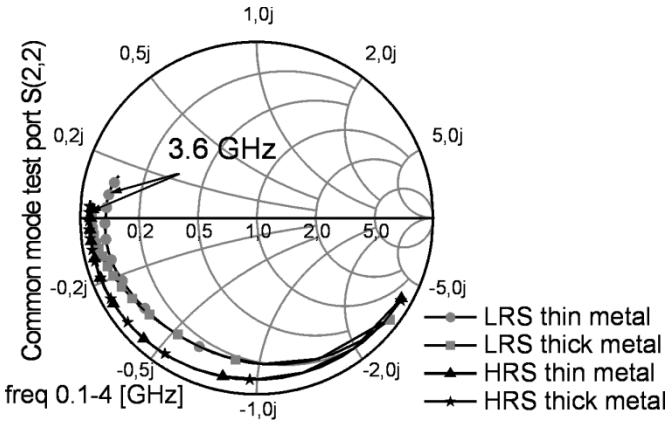


Fig. 12. One-port common-mode test measurement of DIMES-04 input transformer for various technology implementations.

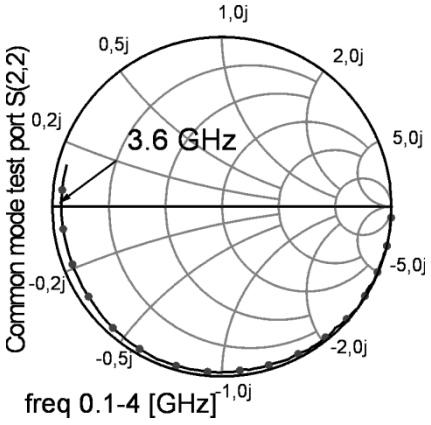


Fig. 14. One-port common-mode test measurement of PCB balun.

C. Center-Tapped Input Transformer

A spiral transformer was implemented at the input of the DIMES-04 PA (configuration 1.c in Table I). The structure is a variation of a concentric spiral transformer: The primary winding is on the outside, as well as on the inside of the secondary winding [7]. This allows a lower mutual capacitance, compared with an interwinded configuration [5] of the transformer at the price of a lower mutual coupling (k factor $= 0.64$). The power transfer of the structure at the design frequency is optimized by shunt resonating the secondary winding with the input capacitance of the transistor itself. The center tap at the secondary port is connected to a series capacitor to achieve a 2ndHS at the input of the transistor stage. The capacitance value is obtained using two capacitors in parallel for reason of symmetry (see conf. 1.c in Table I). The same structure was implemented in both high (HRS) and low resistivity silicon (LRS). The HRS implementation has 1-dB improved insertion loss at the frequency of interest ($f_0 = 1.8$ GHz; see Fig. 11). To characterize the common-mode impedance, a four-port S-parameter measurement was performed; the acquired data was then excited with a common-mode port test stimulus, as shown in Fig. 8. The results for the different technology implementations are shown in Fig. 12.

D. PCB Balun

When considering low-voltage high-power PAs, the high current levels at the output of the device require very high-Q matching networks to minimize losses. On-chip transformers, which present very low metal losses, require an undesirably large Si area. To overcome this problem, we have implemented a very compact coupled-line center-tapped printed circuit board (PCB) balun, which is a modification of the work presented in [8]. The modification of the balun lies in a center-tap connection that facilitates an independent control of the second-harmonic termination.

The symmetry of the structure becomes a fundamental issue when introducing the center tap, to avoid differential-to-common-mode conversion. Thus, the geometry was optimized using a 2.5D EM simulator, namely, Agilent's Momentum.

As the coupled lines are by far smaller than the typical $(1/4)\lambda$ length required for a high coupling, capacitors are used to resonate the lines in order to shift the optimal power transfer to the frequency band of interest. Fig. 13 presents the maximum available gain of the structure in a balanced–unbalanced configuration. The width and length difference between the inner and outer lines also provides some impedance transformation. Fig. 14 shows the value of the 2ndHS measured using the

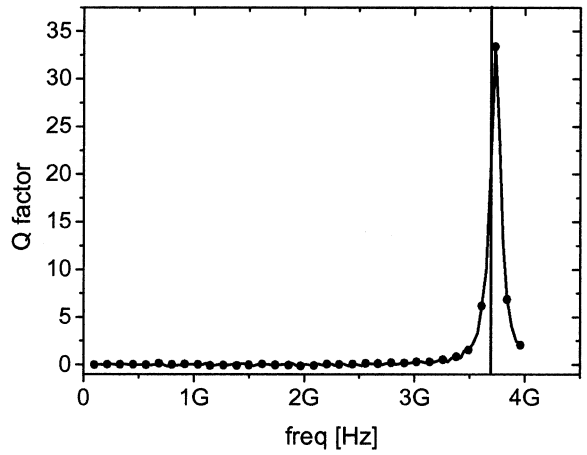


Fig. 15. Quality factor of 2ndHS of PCB balun (marker at $2f_0 = 3.6$ GHz).

common-mode test setup (see Fig. 8). Fig. 15 shows the Q factor, calculated using (3) of the 2ndHS.

VI. Measurement Setup

Two different setups were used for the measurements: one for the small-signal S-parameter characterization which has been used for the various passive test structures, and one for the large-signal load-pull characterization.

A. S-Parameter Measurements

The setup for measuring the mixed-mode S-matrix of the three-port and four-port passive networks is based on an HP 8753E vector network analyzer (VNA) combined with the N4000 four-port test set from ATN. The wafer probes used are of the Cascade APC-40 ground-signal-signal-ground (GSSG)-type with a pitch of 200 μm [9].

This measurement system enables a fully corrected four-port [10] S-parameter measurement, which has been used to determine the common-mode and differential impedances of the implemented structures. A custom calibration procedure facilitated a high-accuracy calibration up to the probe tips, which is independent of probe pitch and probe tip electrical configuration (e.g., GSSG, GSGSG).

B. Large-Signal Measurements

The custom load-pull setup for the differential amplifiers is presented in Fig. 16. The load and source tuning was performed by the Maury ATS MT982E system. Two Macom 180° hybrids were used at the input and output (when required) in order to create the differential signals.

The measured mode rejection of these hybrids is better than 30 dB for the band of interest (1–3 GHz) [11]. For this reason, we will neglect the generation of common-mode signals by the hybrids. Following the hybrids, the differential signals are fed to the circuit using dual-line Cascade ACP-40 GSSG probes.

To enable standard de-embedding procedures for the hybrids and the dual-line probes, a mixed-mode S-parameter representation [12] is used for the network shown in Fig. 17. This, together

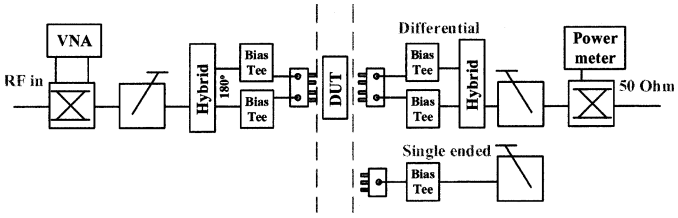


Fig. 16. Load-pull measurement setup used for the large-signal differential PA characterization.

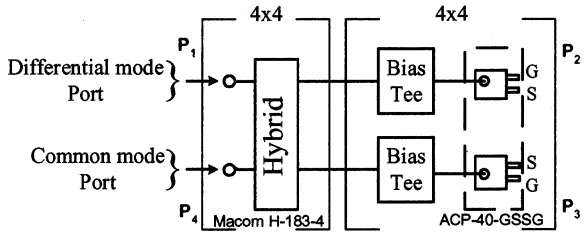


Fig. 17. Hybrid, bias-tees, and wafer probes as a 4×4 network. P_1 represents the port to connect the RF source in order to generate a differential signal between ports P_2 and P_3. Port P_4 is terminated to 50 Ω.

with the assumption on the hybrids, allows us to reduce the matrix of the network to a 2×2 one:

$$\begin{bmatrix} b_1 \\ b_d \end{bmatrix} = \begin{bmatrix} s_{11} & \frac{1}{\sqrt{2}}(s_{12} - s_{13}) \\ \frac{1}{\sqrt{2}}(s_{21} - s_{31}) & \frac{1}{2}(s_{33} - s_{32} + s_{22} - s_{23}) \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_d \end{bmatrix}. \tag{4}$$

The resulting matrix is a representation of the network (Fig. 17) driven single-ended at port P_1 with the differential output between port P_2 and P_3 and port P_4 terminated to 50 Ω. This matrix enables the use of the standard two-port de-embedding procedure [11].

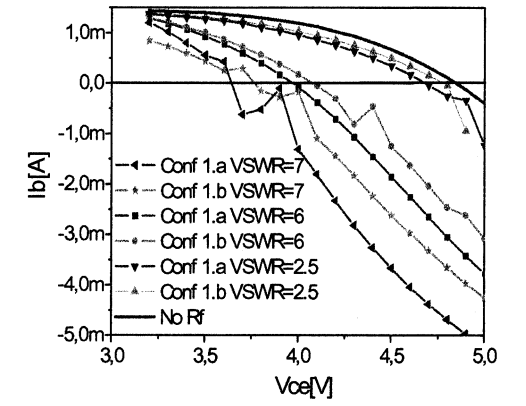
By using a VNA at the input of our system and properly de-embedding up to the DUT reference plane, we can monitor the differential reflection coefficient ($\Gamma_{\mathrm{in-diff}}$) during the measurements. This facilitates an easy and direct determination of the input matching conditions.

VII. PA Measurements

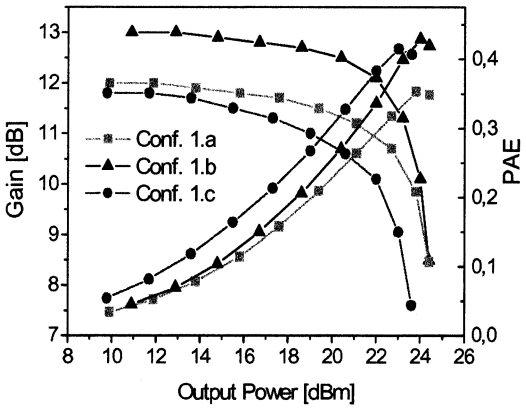
The presented measurement setup [13] was used for both PAE and ruggedness measurements with a focus on verifying the influence of the second-harmonic terminations at the input and output of the PA.

A. Second-Harmonic Short at the Input

As shown in Figs. 6 and 7, providing a 2ndHS at the input of the PA should lower the voltage swing at the output and, thus, yield an improved ruggedness. We can relate the ruggedness of a device to the amount of avalanche current generated by the bipolar device under mismatch conditions. For this purpose, we monitor I_{b} versus V_{CE} in configurations 1.a and 1.b [see Fig. 18(a)] under various voltage standing wave ratio (VSWR) conditions of the load, while keeping the power at the input constant at 11.9 dBm at $f = 1.8$ GHz. Note that the curve labeled *no RF* in Fig. 18(a) represents our reference case when no power is applied to the input. The trace is the same for both configurations, as the dc performances of both PAs are the same. For all

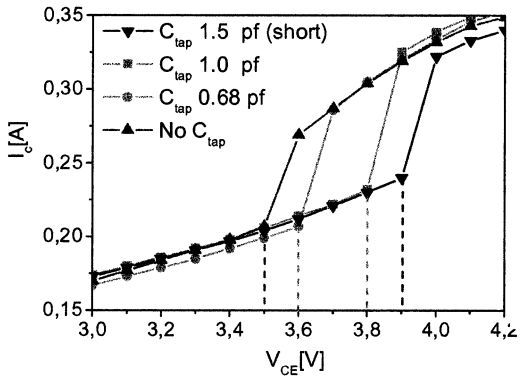


(a)

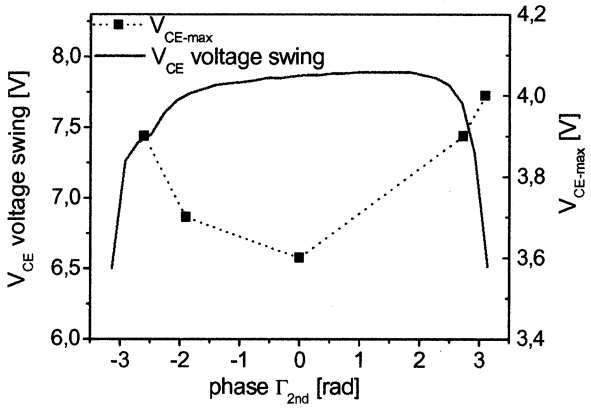


(b)

Fig. 18. Comparison between different configurations 1. (a) Breakdown mechanism for different loads VSWR monitored through $I_{\rm b}$. (b) Optimum RF performance found in load-pull measurements.



(a)



(b)

Fig. 19. Configuration 2 measurements. (a) Breakdown mechanism for different $C_{\rm tap}$ values, monitored via $I_{\rm c}$. (b) Comparison of $V_{\rm CE-max}$ measured value and simulated $V_{\rm CE}$ voltage swing.

the traces in Fig. 18(a), configuration 1.b experiences a negative $I_{\rm b}$ region for higher values of $V_{\rm CE}$ compared with configuration 1.a. This shows that, as expected from the simulation results, the 2ndHS at the input puts the device in lower stress operation. Fig. 18(b) shows also that the RF performance of the device in configuration 1.b is better than that of configuration 1.a.

B. Second-Harmonic Control at the Output

The effect of the second-harmonic output termination on the ruggedness can be demonstrated best when applying a nonshorted condition for the second harmonic at the input (see inverse class-AB in Fig. 6). In our experiment, we apply a constant $P_{\rm in}$ ($=13.9$ dBm at $f=1.8$ GHz) and increase $V_{\rm CE}$ while monitoring $I_{\rm c}$.

The experiment is repeated using different values for $C_{\rm tap}$. This results in an effective control of $\angle\Gamma_{\rm 2nd\_out}$, as becomes apparent from the following equations:

$$Z_{\rm even} = j\omega L + \frac{1}{j\omega C_{\rm tap}} \tag{5}$$

$$\Gamma_{\rm 2nd-harmonic} = \frac{Z_{\rm even} - Z_0}{Z_{\rm even} + Z_0} \tag{6}$$

where L is the parasitic inductance of the balun obtained using the common-mode port test. The ruggedness versus $\angle\Gamma_{\rm 2nd\_out}$ is now given by the $V_{\rm CE}$ voltage where the sudden increase in $I_{\rm c}$ indicates a soft device breakdown, denoted as $V_{\rm CE-max}$ [see Fig. 19(a)]. The higher $V_{\rm CE-max}$, the better the ruggedness of the PA. Fig. 19(a) shows that the increase in $V_{\rm CE-max}$ between a shorted ($\angle\Gamma_{\rm 2nd}=\pi$) and an open condition ($\angle\Gamma_{\rm 2nd}=\pi$) for the second harmonic at the output is 0.4 V.

In Fig. 19(b), we have superimposed the value of the measured $V_{\rm CE-max}$ on the simulated results of the $V_{\rm CE}$ voltage swing, both versus $\angle\Gamma_{\rm 2nd\_out}$. We can observe that the highest $V_{\rm CE-max}$ occurs in conjunction with the minimum in the $V_{\rm CE}$ voltage swing (simulated data) at $\angle\Gamma_{\rm 2nd\_out}=\pm\pi$. This is in agreement with the explanation from the theory and supports that highest $V_{\rm CE-max}$ conditions can indeed be related to the minimum stress condition of the bipolar output stage.

C. Second-Harmonic Control at the Output and 2ndHS at the Input

Considering the hybrid solution in configuration 3 (on-chip 2ndHS at the input of the PA), we can control the phase of the $\angle\Gamma_{\rm 2nd\_out}$ via the $C_{\rm tap}$ as discussed in the previous section. This next experiment is done to prove that a simultaneous 2ndHS condition at the input and output is required for high efficiency of the PA.

Fig. 20 shows the agreement between the behaviors of the PAE versus $\angle\Gamma_{\rm 2nd\_out}$ as extracted from the measurements and provided by simulations. Note that in the simulation and measurements presented in Fig. 20, the values for the resonating capacitors (C_1 and C_2, Fig. 8) were not optimized for maximum power transfer, resulting in a somewhat lower PAE.

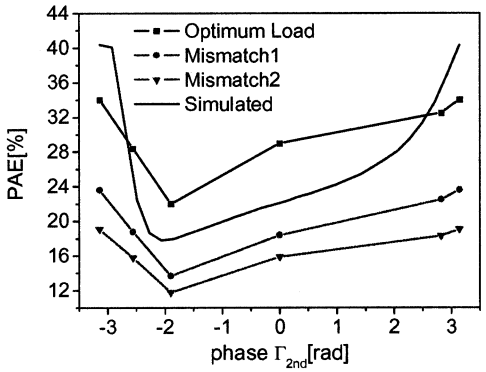


Fig. 20. Measured and simulated PAE of configuration 3 as function of $\angle\Gamma_{2nd\_out}$.

TABLE II
MEASURED PERFORMANCES OF THE DIFFERENT PA CONFIGURATIONS

Circuit Configuration	PAE[%]	$Pout_{1dB}$	Gain
Conf.(1.a) DIMES-04 HRS 3μm	36	22.7	12
Conf.(1.b) DIMES-04 HRS 3μm	43	23	13
Conf.(1.c) DIMES-04 HRS 3μm	41	20.6	11.7
Conf (2) B6HFC (No c_{tap})	42.5	25.2	11.2
Conf. (3) B6HFC*	47	25.6	11.8

* Different sample than one used in Fig. 20.

As supported by Fig. 20, even under high mismatched conditions, the pure class-AB operation (2ndHS at input and output) yields the highest PAE.

VIII. CONCLUSION

In this paper, we have presented differential amplifiers optimized for PAE and ruggedness using 2ndHS. Various second-harmonic terminations have been designed and implemented in Si-based substrates and PCB. Dedicated center-tapped transformer/baluns have been developed, providing high-quality 2ndHS independent of the fundamental loading. The experimental data supports the presented theory. An overview of the PA performance for the different configurations and technology options is given in Table II.

ACKNOWLEDGMENT

The authors would like to thank all the DIMES and Infineon staff for their great support in fabricating and assembling the various integrated circuits, in particular, H. Schellevis, S. Milosavljevic, R. Klerks, and W. van der Vlist, and also G. Doing for his helpful suggestions and support.

REFERENCES

[1] F. van Rijs, R. Dekker, H. A. Visser, H. G. A. Huizing, D. Hartskeerl, P. H. C. Magnee, and R. Dondero, "Influence of output impedance on power added efficiency of Si-bipolar power transistors," in *IEEE MTT-S Dig. Tech. Papers*, Boston, MA, 2000, pp. 1945–48.

[2] H. F. F. Jos, "Future developments and technology options in cellular phone power amplifiers: From power amplifier to integrated RF front-end module," in *Proc. BCTM*, Minneapolis, MN, 2000, pp. 118–125.

[3] M. P. van der Heijden, H. C. de Graaff, and L. C. N. de Vreede, "A novel frequency-independent third-order intermodulation distortion cancellation technique for BJT amplifiers," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1175–1183, Sept. 2002.

[4] S. Cripps, *RF Power Amplifier for Wireless Communications*. Boston, MA: Artech House, 1999.

[5] J. R. Long, "Monolithic transformers for silicon RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1368–1382, Sept. 2000.

[6] J. N. Burghartz, M. Soyuer, and K. A. Jenkins, "Microwave inductors and capacitors in standard multilevel interconnect silicon technology," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 100–104, Jan. 1996.

[7] W. Simbürger, H.-Di. Wohlmuth, P. Weger, and A. Heinz, "A monolithic transformer coupled 5-W silicon power amplifier with 59% PAE at 0.9 GHz," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1881–1892, Dec. 1999.

[8] K.-C. Tsai and P. Grey, "A 1.9-GHz 1-W CMOS class-E power amplifier for wireless communications," *IEEE J. Solid-State Circuits*, vol. 34, pp. 962–970, July 1999.

[9] Cascade Microtech, Inc., Beaverton, OR. [Online]. Available: http://www.cmicro.com/index.cfm/fuseaction/pg.view/pID/126

[10] M. Schindler, P. Phillips, M. Fennelly, V. Adamiam, and P. Enquist, "Characteristics and accuracy of a fully corrected four-port vector network analyzer," in *50th Automatic RF Techniques Group (ARFTG) Conf. Dig.*, Portland, OR, Dec. 1997, pp. 127–130.

[11] M. Spirito, M. P. van der Heijden, M. De Kok, and L. C. N. de Vreede, "A calibration procedure for on-wafer differential load-pull measurements," in *61th Automatic RF Techniques Group (ARFTG) Conf. Dig.*, Philadelphia, PA, June 2003, pp. 1–4.

[12] D. E. Bockelman and W. R. Eisenstadt, "Combined differential and common-mode scattering parameters: Theory and simulation," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 1530–1539, July 1995.

[13] R. Mahmoudi, M. Spirito, P. Valk, and J. L. Tauritz, "A novel load and source tuning system for balanced and unbalanced WCDMA power amplifiers," in *54th Automatic RF Techniques Group (ARFTG) Conf. Dig.*, Atlanta, GA, Dec. 1999, pp. 1–9.

Marco Spirito (S'01) received the M.Sc. degree in electrical engineering from the University of Naples Federico II, Naples, Italy, in 2000. He is currently working toward the Ph.D. degree in electrical engineering at Delft University of Technology, Delft, The Netherlands.

He joined the Laboratory of Electronic Components, Technology, and Materials, Department of Information Technology and Systems, Delft University of Technology, in 2000. Since then, he has worked on the design of high-performance rugged power amplifiers. His research interests include large signal characterization techniques such as passive and active load pull.

Leo C. N. de Vreede (M'01) was born in Delft, The Netherlands, in 1965. He received the B.S. degree in electrical engineering from The Hague Polytechnic, The Hague, The Netherlands, in 1988 and the Ph.D. degree from Delft University of Technology in 1996.

In 1988, he joined the Laboratory of Telecommunication and Remote Sensing Technology, Department of Electrical Engineering, Delft University of Technology. From 1988 to 1990, he was involved in the characterization and physical modeling of CMC capacitors. From 1990 to 1996, he worked on modeling and design aspects of HF silicon ICs for wide-band communication systems. In 1996, he was appointed as Assistant Professor with the Delft University of Technology, working on the nonlinear distortion behavior of bipolar transistors at the device physics, compact model, and circuit level, at the Delft Institute of Microelectronics and Submicron Technology (DIMES). In the winter of 1998–1999, he was a guest of the High-Speed Device Group, University of San Diego, San Diego, CA. In 1999, he became an Associate Professor, responsible for the Microwave Components Group of the Delft University of Technology. His current research interest is technology optimization and circuit design for improved RF performance and linearity.

Lis K. Nanver (S'80–M'83) received the M.Sc. degree in physics from the University of Aarhus, Aarhus, Denmark, in 1979 and the Dr. Ing. degree from the Ecole Nationale Superieure des Télécommunications, Paris, France, in 1982, where she worked on the simulation of CCD structures. She received the Ph.D. degree from the Delft University of Technology, Delft, The Netherlands, in 1987, where she developed a medium-frequency BIFET process.

In 1988, she joined the DIMES IC Process Research Sector as a Bipolar Process Research Manager. She became an Associate Professor in 1994 and a Professor in 2001 with the Faculty of Electrical Engineering, Mathematics and Computer Science, Delft University of Technology, detached at DIMES Technology Center. Within the Laboratory of Electrical Components, Technology, and Materials, she manages the research on advanced Si-based devices that is mainly directed toward optimization and development of high-frequency Si BJT/SiGe HBT devices and the integration of passives. This research involves technologies such as AP/LPCVD epitaxy, dopant activation by excimer laser annealing, and substrate transfer techniques. She has served on the committees of ESSDERC and BCTM.

Stephan Weber was born in 1966 in Berlin, Germany. He studied electrical engineering from 1985 to 1990 at the Technical University Berlin. In 1990, he moved to the Hahn-Meitner Institute for Nuclear Physics, where he received the Ph.D. degree on modeling of field-effect transistors.

He moved to Siemens (now Infineon Technologies) in July 1995, where he started with the design of DECT receivers. He was responsible for the development and concept engineering of Silizium RF power amplifiers and was also involved with special CAD topics such as on-chip coils, transistor modeling, technology optimization. He is currently working with the Cadence Design Systems GmbH, Feldkirchen, Germany. He holds many patents on circuits and system topologies for DECT, receicers, amplifiers, and bias and control circuits.

Joachim N. Burghartz (M'90–SM'92–F'02) received the M.S. degree from the Rheinisch–Westfälische Technische Hochschule (RWTH), Aachen, Germany, in 1982 and the Ph.D. degree from the University of Stuttgart, Stuttgart, Germany, in 1987, both in electrical engineering.

From 1982 to 1987, he was with the University of Stuttgart, where he developed sensors with integrated signal conversion with a special focus on magnetic-field sensors. He joined the IBM T. J. Watson Research Center, Yorktown Heights, NY, in 1987, where he first worked on selective epitaxial growth of silicon and related applications. From 1989 to 1992, he worked on high-speed Si and SiGe bipolar integration processes and was with the IBM team that pioneered IBM's SiGe technology. From 1992 to 1994, he was partly responsible for the development of a 0.18-μm CMOS technology at IBM's Advanced Silicon Technology Center, East Fishkill, NY. In 1994, he returned to the IBM T. J. Watson Research Center, where he made an original contribution to the integration of RF spiral inductors and other passive components on silicon substrates, and also worked on RF circuit design. In 1998, he became a full Professor at the Technical University Delft, Delft, The Netherlands, where he set up a research program in high-frequency silicon technology. Since 2001, he has been the Scientific Director of the research institute DIMES. He has published more than 150 papers in reviewed journals and at technical conferences, and he holds 13 U.S. patents.

Dr. Burghartz is an IEEE Distinguished Lecturer. He has served on several IEEE conference committees, including IEDM, BCTM, and ESSDERC. Currently, he is an Associate Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES.