A Compact Temperature-Stable RC Frequency Reference

By

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Abstract

This paper presents a 0.01mm^2 10MHz FLL-based RC frequency reference that does not require the use of resistors with complementary temperature coefficients (TCs), thus facilitating its implementation in a wide range of standard CMOS processes. Fabricated in a 0.18µm CMOS process, it achieves a frequency inaccuracy of ±0.28% from −45°C to 125°C after a 1-point trim, which is currently the best reported performance for a compact (<0.02mm^2) frequency reference.

Acknowledgment

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Xiaomeng

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Contents

Chapter 1 Introduction

This thesis describes the design and realization of a compact temperature-stable CMOS frequency reference. Chapter 1 presents the motivation, a review of the state of the art, the objectives and the design challenges of this work. At the end, the structure of this dissertation is described.

1.1 Background and Motivation

Low-power integrated circuits are in high demand in applications such as wireless sensor networks (WSNs). These consist of many specialized sensors with a wireless communications infrastructure to monitor and gather data on physical conditions, such as temperature, pressure, humidity, vital body functions, and pollution levels. The sensor nodes of some applications are hard to reach, and it is impossible or impractical to change their batteries. Other applications, such as implantable sensors, must operate for as long as possible without battery replacement. To prolong battery life while preserving cost, the main targets of WSN design are small area, low power consumption, and long-term stability.

In a WSN, the wireless interface is usually a radio. Good frequency accuracy is then necessary to select the portion of the RF spectrum used for inter-node communication. The design of frequency references with good accuracy, low power and low area is a challenging and popular topic. In the 1920s, the crystal oscillator was the most commonly used frequency reference, and its stability was determined by the mechanical resonance of a quartz crystal. These have excellent frequency accuracy, in the order of a few parts per million (ppm) and good noise performance. However, their large size and silicon integration problem limit their use in area-constrained applications. With the development of CMOS technology, on-chip transistors have become smaller and cheaper, making them suitable for large-scale applications. As a result, much effort has been spent on developing CMOS oscillators. Although such oscillators are more vulnerable to process–voltage–temperature (PVT) variations, many frequency compensation and calibration techniques have been developed to solve this problem. Today, frequency accuracies of several hundred ppm can be achieved after calibration, while chip area has been reduced dramatically.

This work aims to design a temperature-stable CMOS oscillator that is also power- and area-efficient. Its topology is chosen based on a review of the prior art. To compensate for PVT variation, the temperature compensation and frequency trimming of the oscillator are the two design challenges of this work.

1.2 State-of-the-art

In the following sections, the advantages and disadvantages of some silicon-based oscillator topologies are reviewed. A suitable oscillator topology is then chosen and the research challenges are discussed.

1.2.1 MEMS based oscillator

The Microelectromechanical systems (MEMS) oscillator [1] is a good replacement for the expensive and bulky crystal oscillator. MEMS resonators can also generate kHz-MHz frequencies with good noise performance. However, MEMS resonators are usually implemented in dedicated processes and must be combined with electronics implemented on a CMOS die. The result is a two-die solution, which is more expensive and bulky than an all-CMOS oscillator.

1.2.2 LC oscillator

LC oscillators, whose oscillating frequencies are mainly determined by a tuned resonant LC circuit, are widely used in radio frequency (RF) circuits because of their high frequency operation and good phase noise properties. For example, an LC oscillator usually serves as a voltage-controlled oscillator (VCO) in a phase-locked loop (PLL) [2, 3]. However, a large inductor is required to generate frequencies in the kHz-MHz range, which would take a large chip area. Besides, a large inductor also leads to a low-quality factor. As a result, the phase noise performance becomes worse.

1.2.3 Ring oscillator

The ring oscillator is famous for its small size, wide tuning range and low power consumption. They are widely used in circuits for ultra-wideband impulse radio (IR-UWB), phase-locked loops (PLLs), and high-speed clock data recovery (CDR). As shown in Figure 1.1, a ring oscillator consists of an odd number of inverters connected in a ring. The propagation delay of signals through the complete chain determines the oscillation period. Unfortunately, this parameter is vulnerable to PVT variations, resulting in an inaccurate output frequency.

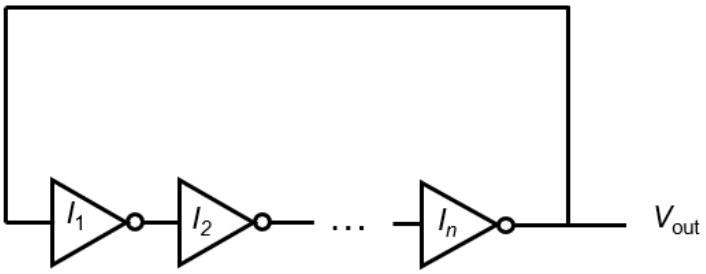

Figure 1.1 Diagram of a conventional ring oscillator

In [4], a compact and low TC ring oscillator with a novel zero temperature coefficient (ZTC) algorithm is proposed as shown in Figure 1.2. The ZTC theory can be explained as follows: The drain current I_{DS} of a transistor in the saturation region may be expressed as in equation 1.1. One can observe that the current varies proportionally with the mobility (μ) and Vgs-Vth. As the temperature increases, both μ and Vth increase, leading to an increasing μ and a decreasing Vgs-Vth. Hence, there is a specific operation point where μ and Vgs-Vth mutually

compensate each other, and I_{DS} is insensitive to the temperature. This point is known as the ZTC point. The same theory can also be applied when it comes to a ring oscillator.

$$I_{DS} = \frac{\mu C_{ox}}{2} \times \frac{W}{L} \times (V_{GS} - V_{th})^2 , \quad 1.1$$

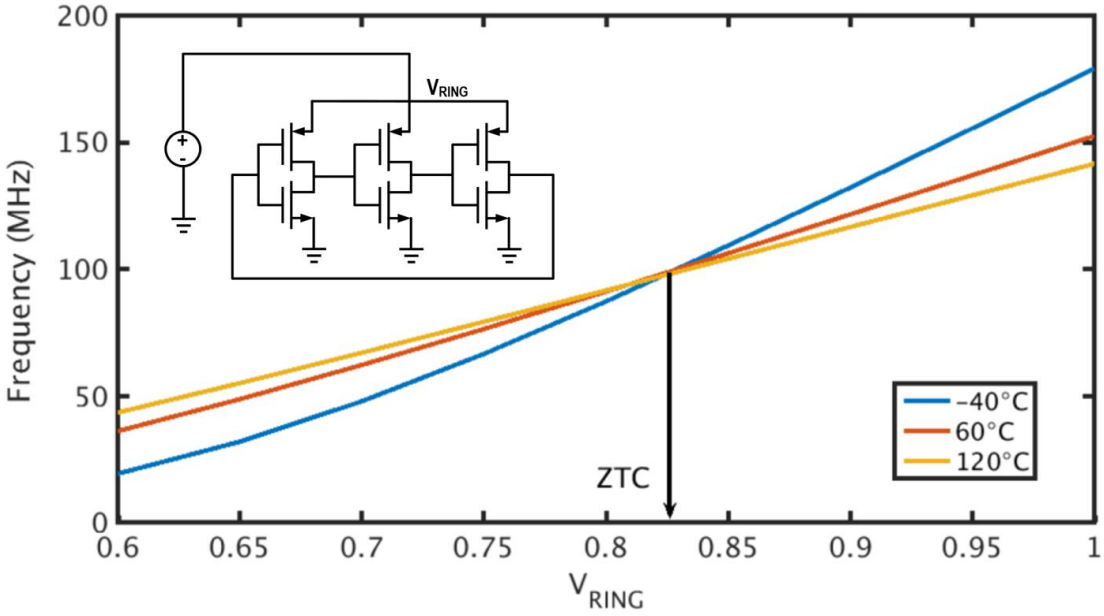

Figure 1.2 Mobility/Threshold-voltage mutual compensation effects [4]

The theory of the ZTC point seems to be an intuitive and helpful way for a ring oscillator to compensate for the temperature variation. However, it is challenging to ensure that the oscillator operates exactly at the ZTC point as this suffers from PVT variation. In [4], the measured frequency error after 2-step calibration is around 0.5% for nominal output frequencies of several MHz.

1.2.4 RC-based oscillator

Compared to LC oscillators and ring oscillators, RC-based oscillators offer a smaller and more power-efficient alternative for generating frequencies in the kHz-MHz range. Theoretically, the period of an RC-based oscillator only depends on the values of on-chip resistors and capacitors. However, these suffer from PVT variation, which limits the achievable frequency accuracy and stability. This section will investigate high precision methodologies, e.g., temperature compensation and high-resolution frequency trimming.

1.2.4.1 RC Relaxation oscillator

The basic structure of a conventional RC relaxation oscillator with two comparators is given in Figure 1.3. The circuit comprises a logic circuit, two comparators with pre-set threshold voltages (V_H and V_L), and a set-reset (SR) latch. The working principle can be described as follows: Assume initially Q=1 and switch SW1 is closed. The voltage Vc across the capacitor C rises and triggers the comparator CMP1 when Vc reaches V_H. Then the SR latch changes to Q=0 and switch SW2 closes. As a result, the capacitor enters the discharging phase. When Vc drops to V_L, comparator CMP2 is triggered, and Q is set to high. As a result, the capacitor

charges and discharges periodically between the voltage intervals of two comparators (V_L, V_H). Equation 1.2 expresses this oscillator's period T_{osc}, and equation 1.3 gives its duty cycle D_{osc}.

$$T_{osc} = \mathrm{RC} \times \ln\left(\frac{V_{DD} - V_L}{V_{DD} - V_H} \times \frac{V_H}{V_L}\right), \quad 1.2$$

$$D_{osc} = \ln\left(\frac{V_{DD} - V_L}{V_{DD} - V_H}\right) \Big/ \ln\left(\frac{V_{DD} - V_L}{V_{DD} - V_H} \times \frac{V_H}{V_L}\right), \quad 1.3$$

Where R is the timing resistance, C is the timing capacitance, V_H and V_L are the higher and lower threshold voltages of the comparators, and V_{DD} is the supply voltage. By generating using a resistive voltage divider to generate both V_H and V_L from V_{DD}, the output frequency will be independent of the supply voltage. The main drawback of this oscillator topology is the non-linear frequency inaccuracy caused by the various non-idealities (temperature-dependent delay time, offset and hysteresis) of the comparators and the logic circuits. Reducing comparator delay requires a fast, power-hungry comparator, which does not match with the requirement for low power consumption.

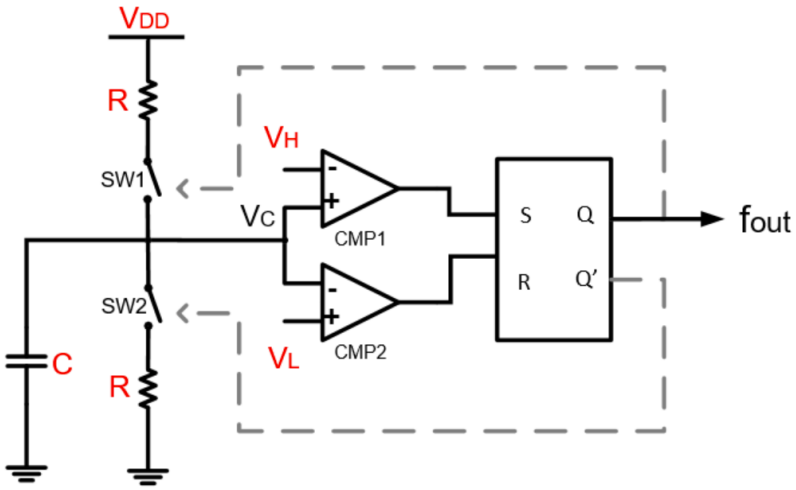

Figure 1.3 A conventional RC relaxation oscillator with two comparators [5]

In [6], the concept of Voltage Averaging Feedback (VAF) to get an accurate oscillating frequency is proposed as shown in Figure 1.4. It uses an analog feedback loop to automatically adjust the reference voltage of the comparators to correct for their delay time.

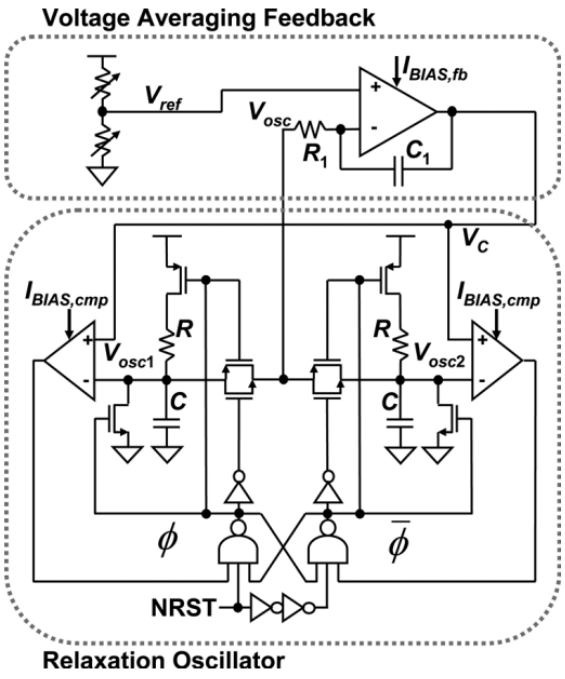

Figure 1.4 Voltage averaging feedback oscillator [6]

In [7], an RC oscillator with a comparator offset cancellation technique is proposed as shown in Figure 1.5. By building dual RC paths, the roles of the comparator's inputs are reversed periodically, allowing offset and low frequency noise cancellation.

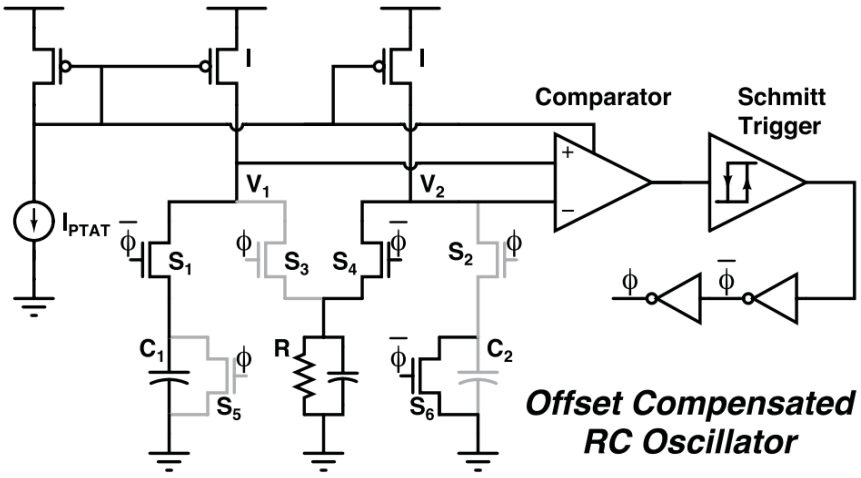

Figure 1.5 An offset compensated RC oscillator [7]

These designs reduce the impact of comparator non-idealities to some extent, achieving frequency inaccuracies in the order of several thousand ppm over a wide temperature range. However, some issues still exist. Firstly, [7] requires a replica of the RC networks, which is a waste of area and power. Second, the RC value of the active-RC LPF in VAF configuration must be large to extract the waveform's DC component accurately, which is not area-efficient.

1.2.4.2 RC-based Oscillator with FLL readout

An alternative RC-based oscillator topology is the Frequency-locked loop (FLL) [8-12]. A simplified block diagram is presented in Figure 1.6. Driven by the output frequency f_{out}, a Frequency-to-Voltage Converter (FVC) outputs a frequency-dependent voltage V_{fb}. This voltage is compared with a reference voltage V_{ref}, the voltage difference will be integrated and then used to drive a Voltage-Controlled Oscillator (VCO). The output frequency accuracy relies on the precise time-to-voltage/current conversion, as well as the mechanism applied to generate a voltage/current proportional to the resistor and capacitor.

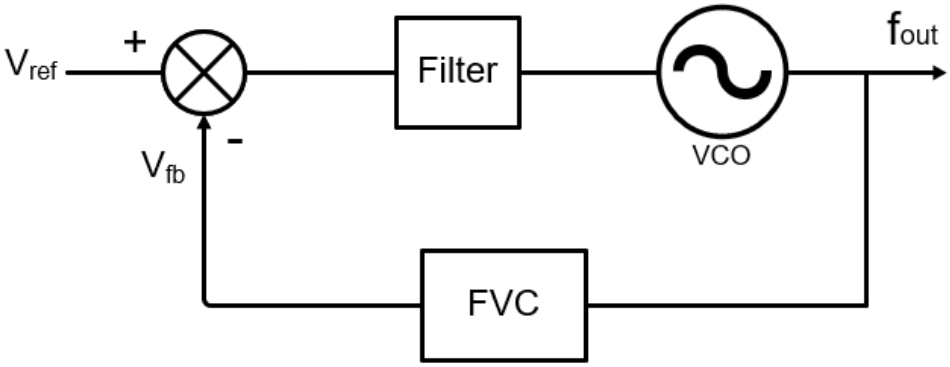

Figure 1.6 A simplified block diagram of FLL

In contrast to the traditional RC relaxation oscillator topology, the use of an FLL removes the comparator from the loop, thereby removing the trade-off between the area/power and comparator non-idealities. The power-consuming comparator is replaced by an integrator. It is possible to make the power consumption very small, since the integrator provides tracking of the VCO output frequency's temperature changes. Practically, the temperature changes are slow, and hence the integrator can have limited bandwidth and low power.

Although the problem of temperature dependency of the comparator is solved with FLL, the PVT effect on resistors and capacitors will still degrade the frequency accuracy. Although on-chip capacitors are relatively stable, resistors have a large temperature coefficients (TCs > 100ppm/°C). In addition, resistors and capacitors both suffer from spread (about ±15%) due to process variations. This variation is static after fabrication. To address these issues, many designs have proposed temperature compensation and absolute frequency trimming techniques.

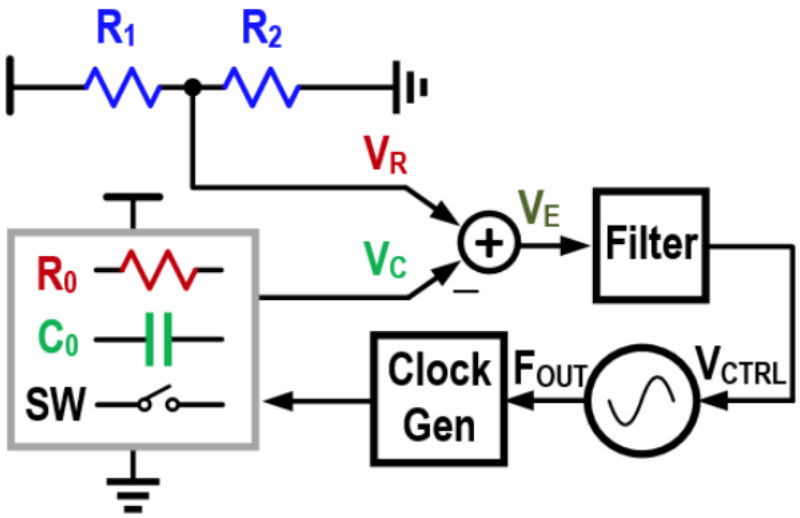

Figure 1.7 System diagram of a conventional RC oscillator with FLL

Figure 1.7 shows a system diagram of an FLL-based RC frequency reference with a conventional temperature compensation method. Resistors R_1 and R_2 are of the same type. Therefore, voltage V_R is temperature-independent. The most straightforward and traditional temperature compensation way is to build a temperature-independent V_C using a zero-TC R_0 by combining two resistors with complementary TCs. The drawback of this temperature compensation technique is the non-ideality (i.e., parasitic capacitors and on-resistance) introduced by trimming switches in the frequency-sensitive RC network.

In [13], a dual-RC frequency reference based on an FLL topology is proposed as shown in Figure 1.8(a). It locks the frequency of a DCO to the combined phase-shift of two Wien Bridge filters. To achieve a net zero temperature dependence, one Wien Bridge utilizes silicided p-poly resistors to generate a positive-temperature phase shift, whereas the other Wien Bridge employs non-silicided n-poly resistors to generate a negative-temperature phase shift. After proper 2-point calibration, only a frequency inaccuracy of ±200ppm from -45°C to 85°C is left. However, using two Wien Bridge filters, digitizing their phase-shifts and then digitally combining them consumes a lot of power (110pJ/cycle) and area (1.59mm^2).

In [14], another FLL-based RC frequency reference is presented as shown in Figure 1.8(b). It uses only one Wien Bridge (WB) filter and its temperature dependency is corrected using data from a Wheatstone-bridge (WhB) temperature sensor. Both WB and WhB exhibit similar non-linearity of temperature dependencies, resulting in good accuracy after a 2-point trim. In contrast to [13], although the frequency inaccuracy is increased to ±400ppm from -45°C to 85°C, the power (25pJ/cycle) and area (0.3mm^2) performances are highly improved. It is also possible for this design to achieve better accuracy, but it requires more complicated data processing (high-order polynomials). In [11], a similar architecture to [14] is proposed as shown in Figure 1.8(c), but it combines the WB and WhB into one architecture with fewer components. It also achieves a ±400ppm inaccuracy from -45°C to 85°C after 1-point room-temperature trim and has 2x improvement on power (9.9pJ/cycle) and area (0.14mm^2) consumption compared to [14].

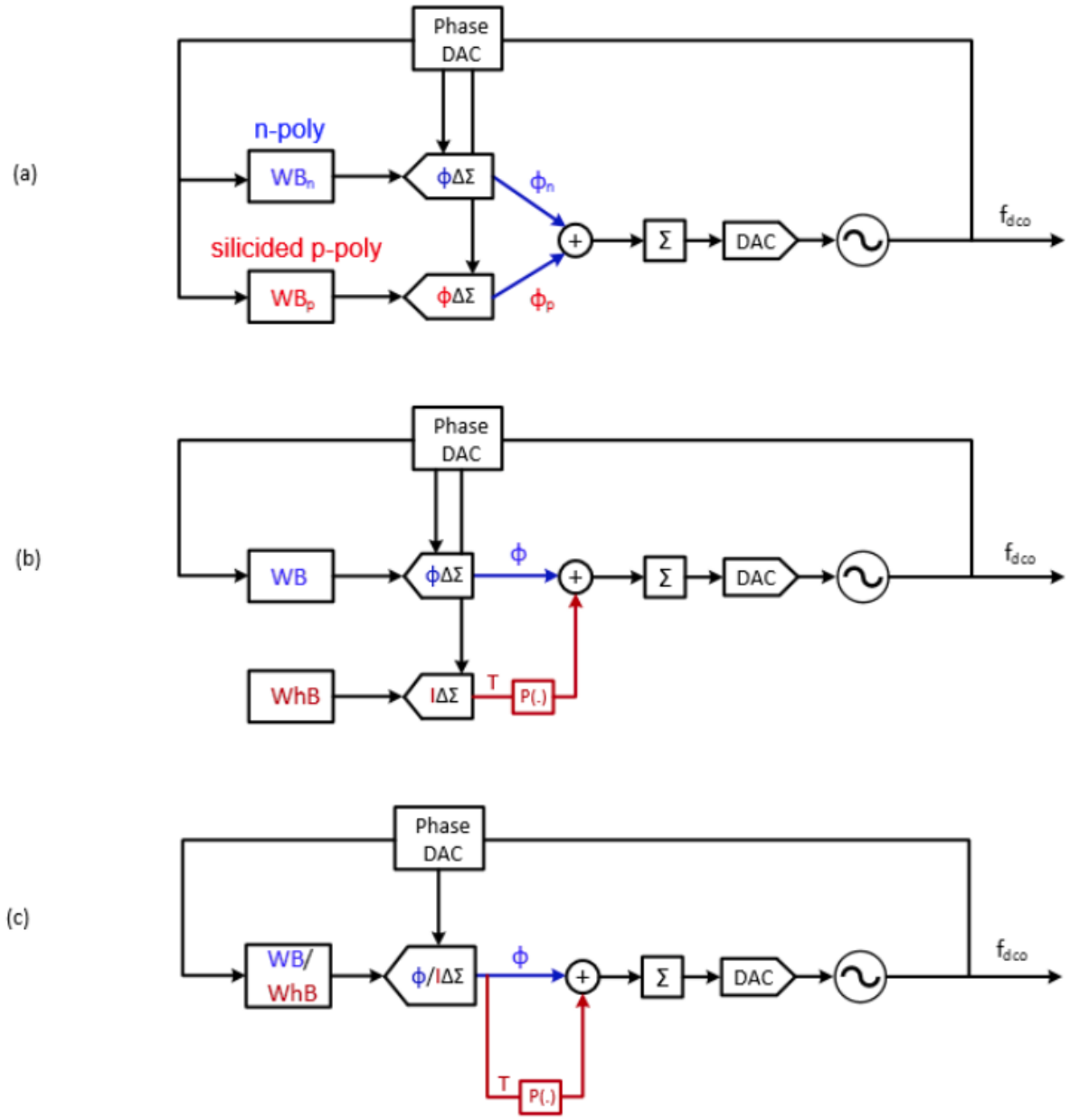

Figure 1.8 Block diagram of frequency references (a) with 2 LPF [13], (b) with 1 LPF and 1 temperature sensor [14], (c) with combined LPF and temperature sensor [11]

In [15], an FLL that locks the period of a voltage-controlled ring oscillator (VCRO) to an RC time-constant is proposed. Resistor TC cancellation is achieved by constructing the reference resistor as a parallel combination of two switched-resistors R_1 and R_2, with complementary TCs, which are digitally controlled by pulse-density modulated sequences. After trimming at two temperatures, it achieves a frequency inaccuracy of ±530ppm from -40°C to 85°C.

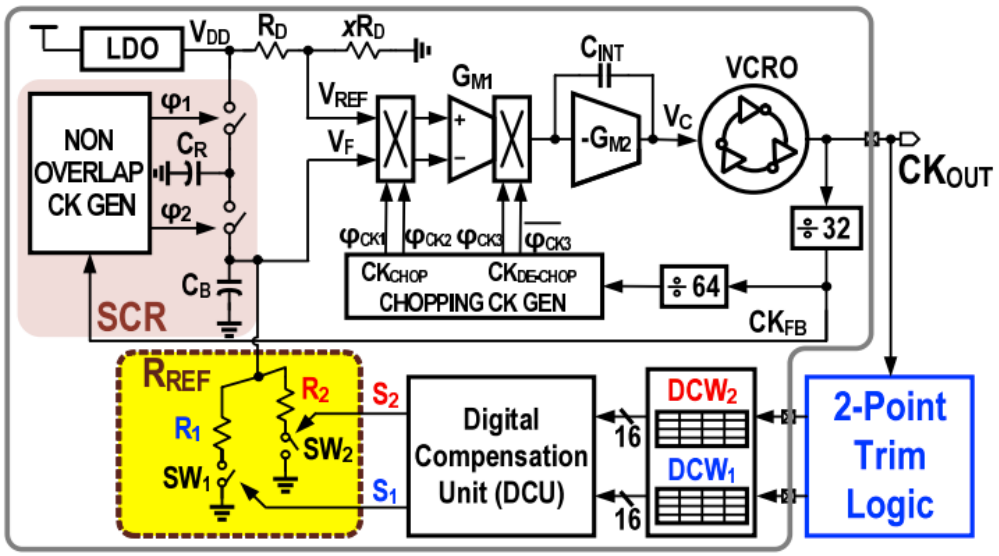

Figure 1.9 Complete architecture of the published frequency reference with pulse-density modulated resistors [15]

Although the above solutions can achieve a decent frequency accuracy over temperature, the circuits are complex, which takes a large chip area. Also, most of them require complementary-TC resistors, which are not always available in some processes.

1.2.4.3 Design conclusion and research gap

In the scope of 10MHz oscillators, the RC oscillator with FLL outperforms other types of oscillators due to its small size and robustness to PVT variations. However, one can notice from the review of prior art that the existing designs with decent accuracy in the order of 100ppm over the industrial temperature range from -40°C to 85°C need complex trimming networks, resulting in a large chip area. For designs with small sizes, they usually apply very coarse or even no trimming networks, which causes a large frequency inaccuracy. Moreover, most of those designs use resistors with complementary TCs, limiting application in some processes.

1.3 Design Objectives

The aim of this project is to design a 10MHz CMOS frequency reference circuit targeted for WSN applications. To expand the applicability, this frequency reference should function well over a wide temperature range (-45°C to 125°C) and achieve a low temperature coefficient (<35.3ppm/°C). The circuit will be fabricated under a TSMC 0.18µm process. Its targeted chip area is 100µm×100µm and the current consumption is limited under 30µA. Moreover, to make the calibration easy for industrial applications, the trimming point is limited to one to save the calibration cost.

Additional specifications are as follows. The supply voltage range is from 1.5V to 1.8V. The period jitter should be less than 30ps_rms. Power-down mode is also required. Table 1.1 Frequency reference design specification

summarizes the design targets of this project.

Specification	Target
Principle of Operation	The best should be chosen
Process	TSMC 0.18µm
Frequency	10MHz
Area	0.02mm^2
Temperature Range	-45°C to 125 °C
Temperature Coefficient	35.3ppm/°C
Trimming Points	1
Inaccuracy After Trimming	±0.3%
Supply Range	1.5V-1.8V
Period Jitter	30ps(RMS)
Current Consumption	30µ

Table 1.1 Frequency reference design specification

1.4 Thesis Organization

The rest of the thesis is organized as follows.

Chapter 2: Architecture Design. The system-level modelling and the proposed oscillator architecture are analyzed in this chapter. The loop model is built to help derive the specification of each block.

Chapter 3: Circuit Design. This chapter focuses on the implementation of the proposed RC oscillator. The detailed design of the front-end, including temperature compensation and absolute frequency trimming schematics, and the FLL readout circuit (integrator, VCO and phase generator) will be presented.

Chapter 4: Measurement Results. This chapter focuses on the chip measurement results. In this chapter, the design layout, the measurement setup, and the measurement results will be analyzed.

Chapter 5: Conclusion. In this chapter, the main findings of this project will be summarized, and a conclusion of this thesis will be drawn. Finally, some recommendations for further research are also given.

Chapter 2 Architecture Design

According to the literature review of the prior art, an RC-based oscillator with FLL is chosen for this application due to the compact structure, the high long-term stability and the easy calibration. In this chapter, the system level design and small-signal analysis are presented.

2.1 System Overview

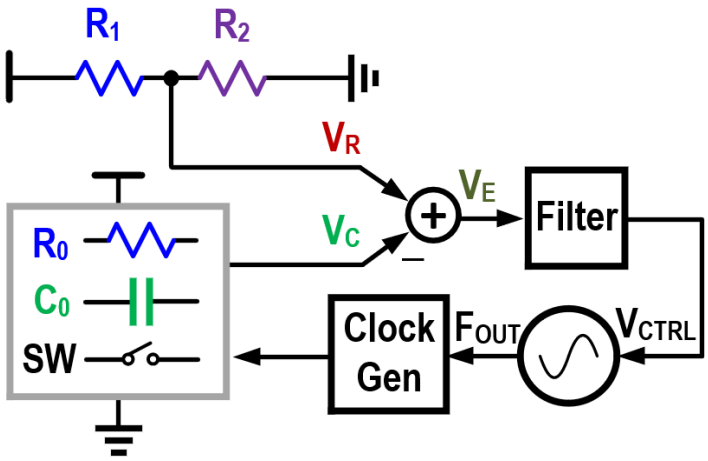

Figure 2.1 Block diagram of the proposed RC-based frequency reference

The block diagram of the proposed RC-based frequency reference based on the frequency-locked-loop is shown in Figure 2.1. The output clock of a voltage-controlled oscillator (VCO) drives an RC frequency-to-voltage converter (FVC) to generate a frequency-dependent voltage V_C. This voltage is compared to a reference voltage V_R and the voltage difference V_E is integrated and then sent to control the VCO. The voltage difference V_E will approach zero with the help of a large loop gain. Theoretically, the output frequency will then only be determined by the RC network and the resistive divider.

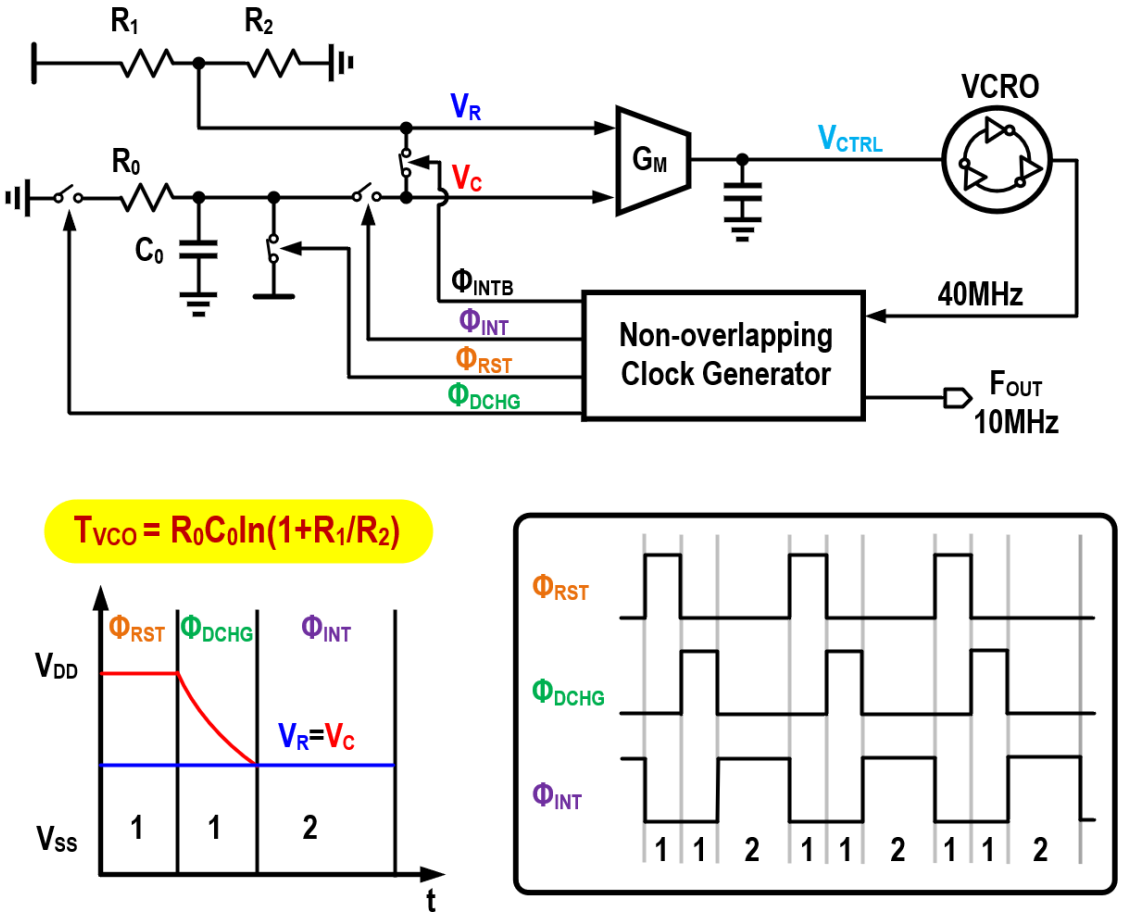

Figure 2.2 (a)Proposed RC-based frequency reference (top); (b)Timing diagram (bottom)

The realization of the design is shown in Figure 2.2(a). The RC frequency-to-voltage converter comprises a resistor, a capacitor and two switches. The timing diagram in Figure 2.2(b) shows the control clocks of three phases, along with the voltages, V_R and V_C. The first phase is the reset phase (ϕ_{RST}), where the capacitor charges up to V_{DD}. The next phase is the discharging phase (ϕ_{DCHG}), in which the charge accumulated on C_0 discharges through R_0. Finally, the voltage V_C sampled at the end of ϕ_{DCHG} is forwarded to the loop filter during the integration phase (ϕ_{INT}), which outputs the control voltage of the VCO. An extra switch is added across two integrator inputs, providing a short path when the integrator is not supposed to work. For energy efficiency and circuit simplicity, the integrating time is set to be 2x longer than the reset and discharging time. To relax the area constraint and facilitate the generation of the 3-phase control signals, the center frequency of the VCO is set to be 40MHz, which is 4x higher than the desired 10MHz output frequency. The expressions of V_R and V_C are presented in equation 2.1 and 2.2. At steady-state, V_C is expected to be equal to V_R in the third integration phase as expressed in equation 2.3. As a result, the expression of the output period of VCO is derived in equation 2.4. The output period of the proposed oscillator is four times smaller than that of the VCO as expressed in equation 2.5.

$$V_R = \frac{R_2}{R_1 + R_2} \times V_{DD} \qquad 2.1$$

$$V_{\mathrm{C}} = V_{DD} \times e^{-\frac{T_{OSC}}{4R_0C_0}} \quad 2.2$$

$$V_{\mathrm{R}} = V_{\mathrm{C}} \quad 2.3$$

$$T_{VCO} = R_0C_0 \times \ln\left(1 + \frac{R_1}{R_2}\right) \quad 2.4$$

$$T_{OSC} = T_{VCO}/4 \quad 2.5$$

Until now, the basic structure of the proposed RC frequency reference has been presented. Some accuracy-harming ingredients, like PVT variations and offset, are now the design focus. Methods to reduce these effects are discussed as follows:

(A) Temperature compensation

Unlike conventional ring oscillators and RC oscillators, the oscillation period of FLL-based design is only determined by the value of passive elements as shown in equation 2.4 instead of the PVT-sensitive delay of other logic circuits. However, although the TC of a capacitor is small, on-chip resistors have a nonnegligible TC (> 100ppm/°C), resulting in a temperature dependence of the output frequency. In this design, V_R is trimmed to follow V_C over temperature as shown in Figure 2.3(b). As a result, V_R and V_C show the same temperature sensitivity so that the TC of the output frequency is minimized. The main advantage of this approach is fewer parasitics introduced in the frequency-dependent RC path. Moreover, this method only requires resistors with the same polarity TC, which extends the application to many processes.

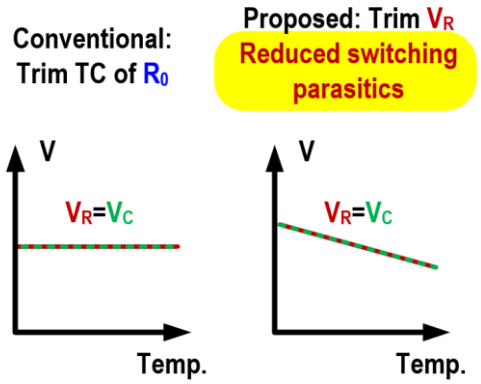

Figure 2.3 (a) Conventional and (b) proposed temperature compensation methods

(B) Absolute frequency trimming

Except for the temperature dependence, resistors and capacitors also have around ±15% process spread, causing nominal frequency errors. Limited by the high trimming resolution and small area, the trimming is implemented on the capacitor. In the end, the absolute frequency will always be adjusted to 10MHz at room temperature.

(C) Offset cancellation

Another factor that influences the accuracy is the offset of the integrator. This cannot be distinguished from the FLL's error signal and so its drift with time and temperature will degrade frequency accuracy. This can be addressed by using so-called dynamic offset cancellation techniques.

Auto-zeroing and chopping are the most commonly used dynamic offset cancellation techniques [16]. Auto-zeroing is a discrete-time sampling technique and it samples the offset and then subtracts the offset from the input signal. A 1-10µV offset can be achieved with auto-zeroing. However, the kT/C noise of the sampling circuit and noise folding cause issues. In contrast, chopping is a continuous-time modulation technique and it modulates the offset to a high frequency and then filters it. Although chopping can achieve a 50nV-10 µV offset and does not cause noise folding, it gives a chopping ripple at the output of the integrator due to the up-modulated offset. This voltage ripple spoils the jitter performance of the VCO. Traditionally, a higher chopping frequency and a larger integration capacitor can suppress the ripple. However, the former leads to a larger residual offset and thus worse inaccuracy over PVT, while the latter results in a trade-off between capacitor area and jitter performance.

In this design, choppers are utilized to remove the low-frequency noise and a sample-and-hold (S&H) circuit is implemented to remove the ripple [17]. As shown in Figure 2.4, in each S&H phase, the triangular ripple will be sampled at the same position, e.g., the zero-crossings. The sampled value will be held until the next sampling point. In the end, the output voltage will be near a constant and the period jitter performance can be highly improved.

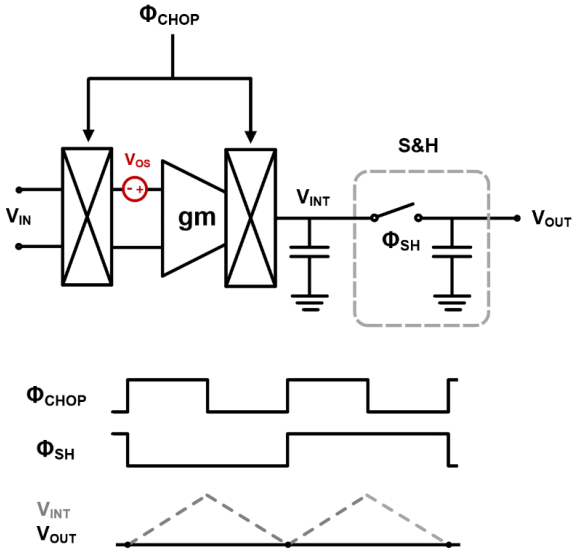

Figure 2.4 Chopped integrator with S&H notch filter and the corresponding timing diagram

Compared to the two-phase filter used in [17], the use of a single-phase filter results in less ripple due to the absence of mismatched charge injection errors, at the expense of 2x more delay. However, the resulting delay is still quite small compared to that of the integrator, and so has a negligible effect on loop stability.

Figure 2.5 shows the complete schematic of the proposed frequency reference design. The design details of each sub-block will be discussed in the next chapter.

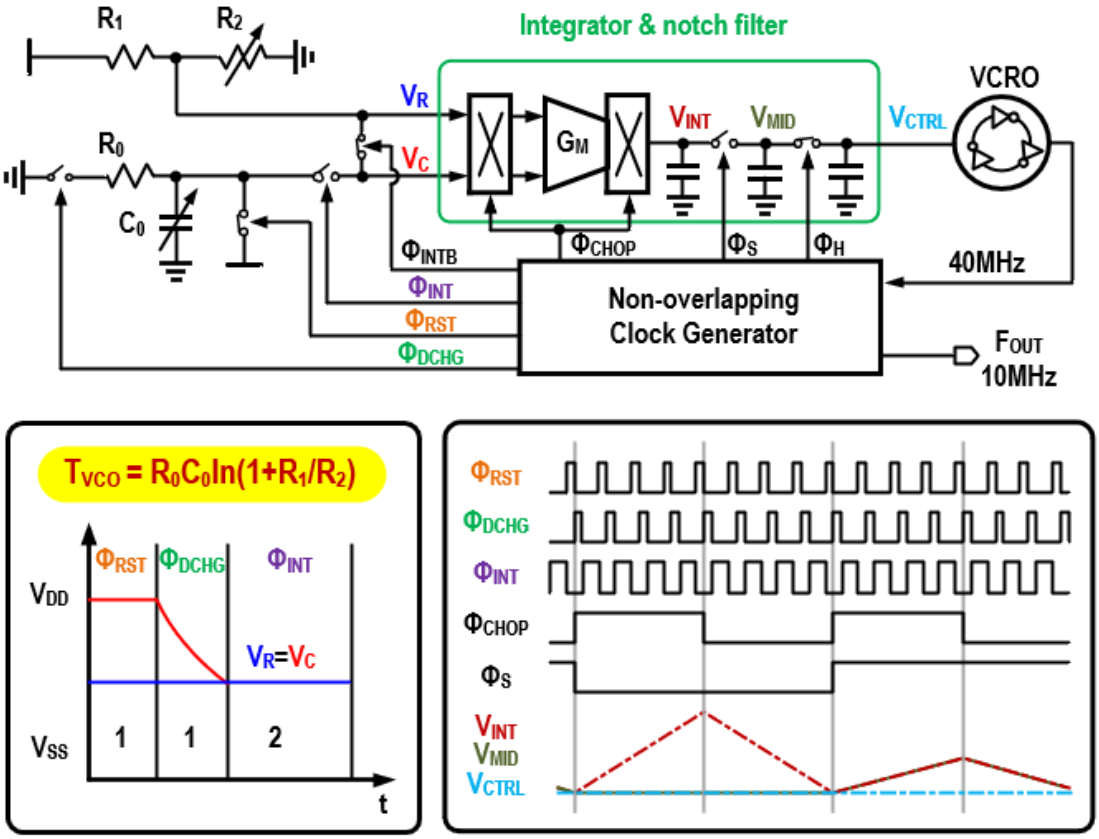

Figure 2.5 Complete schematic

2.2 Loop modelling

A linear model of the proposed oscillator is presented in Figure 2.6.

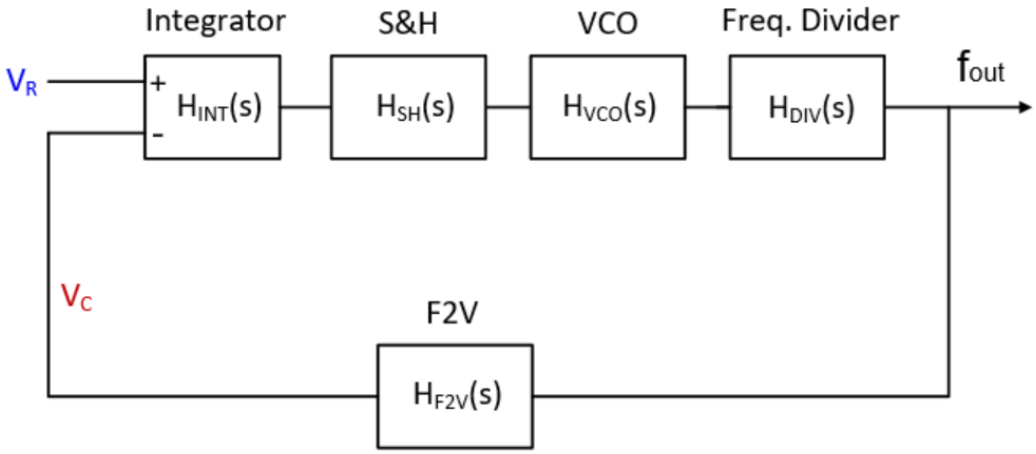

Figure 2.6 Loop model of the proposed design

The integrator provides a high dc gain K_{INT} and a dominate pole τ_{INT}

$$H_{INT}(s) = \frac{K_{INT}}{1 + s\tau_{INT}} \quad 2.6$$

The S&H introduces a delay and its transfer function is shown below. Where T_s is the sample period.

$$H_{SH}(s) = \frac{1 - e^{-sT_s}}{s} \quad 2.7$$

The frequency response of a voltage-controlled oscillator is usually modelled as a linear relationship with its control voltage. VCO's transfer function is shown below with a voltage-to-frequency gain, K_{VCO}.

$$H_{VCO}(s) = K_{VCO} \quad 2.8$$

The frequency divider divides the output frequency of VCO by 4 and its transfer function is

$$H_{DIV}(s) = 1/4 \quad 2.9$$

Considering the frequency model of the frequency-to-voltage (F2V) converter, its input frequency is the feedback frequency of the frequency divider and the output is a voltage signal, V_C. The frequency is transferred into a voltage through a switched-capacitor resistor (SCR) network. The charges accumulated in the capacitor will be discharged within a quarter of a period of time. The SCR's step response for an input step of f_{FB} can be calculated as

$$V_C(f_{FB}) = V_{DD} \times e^{-\frac{1}{4R_0C_0f_{FB}}} \quad 2.10$$

The F2V's transfer function can be derived as

$$H_{F2V}(s) = \frac{K_{F2V}}{1 + s\tau_{F2V}} \tag{2.11}$$

Where

$$K_{F2V} = \frac{dV_c}{df_{FB}} = \frac{V_c}{4R_0C_0f_{FB}^2} \tag{2.12}$$

In the steady state, V_C=V_R

$$K_{F2V} = \frac{V_R}{4R_0C_0f_{FB}^2} \tag{2.13}$$

The open loop gain $H_{OL}(s)$ is

$$H_{OL}(s) = \frac{K_{INT}}{(1 + s\tau_{INT})} \frac{K_{F2V}}{(1 + s\tau_{F2V})} \frac{K_{VCO}}{N_{DIV}} \frac{(1 - e^{-sT_s})}{s} \tag{2.14}$$

The unity-gain frequency is located at

$$\omega_u = \frac{K_{INT}K_{F2V}K_{VCO}}{N_{DIV}} \tag{2.15}$$

To make the loop stable, the unity-gain frequency should locate between the dominant pole ($1/\tau_{INT}$) and the first non-dominant pole ($1/\tau_{F2V}$). Besides, ω_u should be much smaller than $1/\tau_{F2V}$ to ensure enough phase margins.

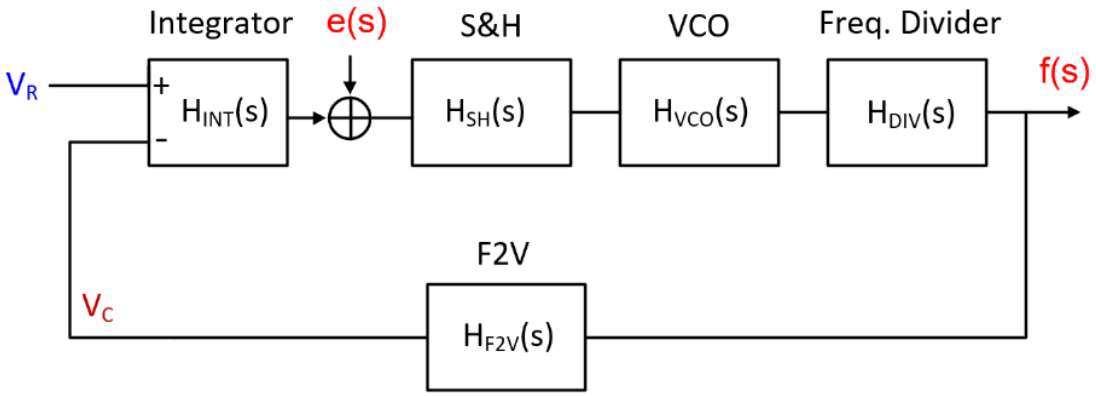

Figure 2.7 Noise transfer function model

Figure 2.7 presents a noise transfer function (NTF) model of the error signal e(s), like offset or noise. Equation 2.16 shows the derived NTF. The high gain of the integrator and F2V converter can suppress the noise. However, the gain of the F2V is unchangeable since the parameters in equation 2.13 are fixed. Therefore, a high dc gain design of the integrator helps to suppress the error.

$$NTF = \frac{f(s)}{e(s)} = \frac{H_{SH}(s)H_{VCO}(s)H_{DIV}(s)}{1 + H_{INT}(s)H_{SH}(s)H_{VCO}(s)H_{DIV}(s)H_{F2V}(s)} \tag{2.16}$$

Chapter 3 Circuit Design

3.1 RC Front-end Design

3.1.1 On-chip resistors and capacitors

In a TSMC 0.18µm technology, silicided/unsilicided P-/N- poly/diffusion resistors are provided. The temperature coefficient (TC) and voltage coefficient (VC) of resistors are listed in Table 3.1. When selecting the resistor type, the first consideration is the sheet resistance (R_{sh}). Since the chip area is supposed to be kept small (0.02mm^2), only four resistor types are appropriate: the n-poly without silicide, the p-poly without silicide, the HRI p-poly without silicide, and the N-well. However, the HRI p-poly without silicide resistor has a large corner spread [18] and the N-well resistor depends more on the power supply because of the variations in the thickness of the depletion region between the n-well and the p-substrate. The p-poly resistor behaves better in terms of temperature- and voltage-dependence than the n-poly one. Hence, the p-poly type resistor will be used in this design, while the n-poly resistor is also used but only for the temperature compensation.

Resistor Type	Sheet Resistance (ohm/sq)	TC (ppm/°C)	VC(ppm/V)
n-diffusion	61.6	1470	80
p-diffusion	140.6	1383	183
n-poly	295.3	-1506	-70
p-poly	321.8	-238	-50
silicided n-diffusion	6.82	3350	49.7
silicided p-diffusion	7.76	3440	6.62
silicided n-poly	7.89	2920	370
silicided p-poly	7.9	2880	220
n-well under diffusion	440	3680	3570
n-well under STI	927	2970	6880
HRI high-resistance-poly	1037	-867	-87

Table 3.1 Resistors in a TSMC 0.18µm process

Three types of capacitors are available in a TSMC 0.18µm technology: Metal-Insulator-Metal (MIM), Metal-Oxide-Metal (MOM), and Metal-Oxide-Semiconductor (MOS). MOS capacitors have the largest temperature and voltage dependency among them. MOM capacitors require at least three stacked metal layers together with the poly shield. In contrast, MIM capacitors only require the fifth and sixth metal layers and have a larger density. Therefore, for the benefit of a small area, the MIM capacitor is chosen in this design. Its first- and second-order temperature and voltage coefficients are TC_1=-29.4ppm/°C, TC_2=0, VC_1=-128ppm/V, and VC_2=-57ppm/V^2.

3.1.2 Value determination of resistors and capacitors

Figure 3.1 shows the RC front-end schematic with resistor and capacitor values. The RC front-end requires two well-defined signals: A frequency-dependent signal V_C and a reference signal V_R. Considering the power efficiency and the common mode voltage of the integrator, the reference signal is set to ½*V_{DD} with the ratio R_1/R_2 =1. Given a 40% area budget for the front-end, the RC time constant is R_0C_0=3.6e-8 to target a 10MHz output frequency. Since MIM capacitors can be placed on top of transistors, but resistors cannot according to drc rules, it is better to keep the resistor small and have a relatively large capacitor to save chip area. In this design, R_0 is set to 36kΩ and C_0 is set to 1pF. Considering the trade-off between average power and area, R_1=R_2 are set to 100kΩ. The size of each CMOS switch is determined by optimizing the frequency error introduced by the on-resistance variation. SW2 is located in the RC path, so its on-resistance also contributes to the RC time-constant. To minimize the due to its spread, the on-resistance of SW2 is 0.5kΩ, which is relatively small compared to the 36kΩ R_0.

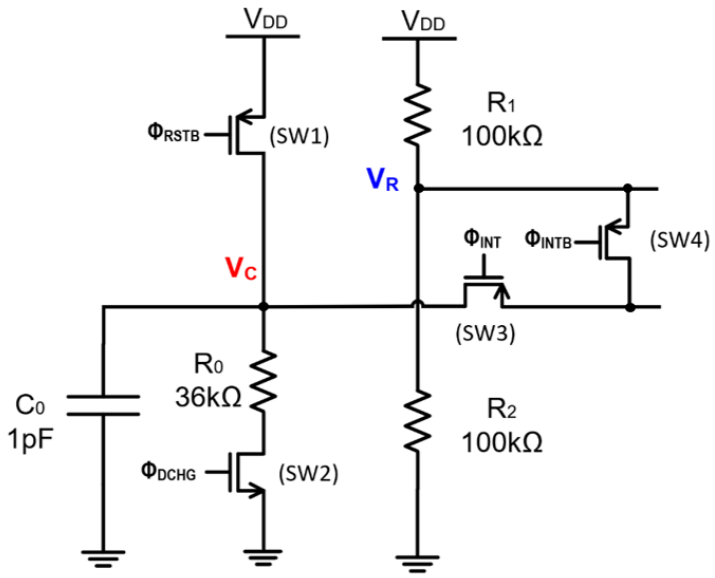

Figure 3.1 Front-end schematic

3.1.3 Output Frequency Trimming

In the nominal case, the output frequency is 10MHz. However, on-chip resistors and capacitors have around ±15% process spread, leading to ±30% frequency inaccuracy at the worst case. Hence, an elegant and easy trimming circuit is necessary.

3.1.3.1 Specification and Design Choice

The design accuracy specification is to achieve less than ±0.3% frequency error in every corner. Among all error sources, the error caused by the temperature sensitivity dominates and the value is around ±0.25% from -45°C to 125°C. Therefore, only a 0.1% error budget is left for the trimming error. Besides, the trimming range should cover the worst case, that is, ±30% frequency inaccuracy due to resistors and capacitors process spread. In conclusion, the

specification for the trimming circuit is to cover a ±30% trimming range with 0.1% trimming resolution.

Trimming R_0 or C_0 can adjust the output frequency to the target over corners. However, the trade-off between trimming resolution and chip area becomes a practical limitation. For example, trimming a 36kΩ p-poly resistor with 0.1% trimming resolution in this design needs a 36Ω ΔR for each trimming step. However, the sheet resistance of a p-poly resistor is 321.8Ω/sq. Even when using the minimum resistor width (1µm) and setting the distance between two switches to 1µm, the minimum trimming step ΔR is still far from our target. It is obvious that trimming R_0 to meet the trimming specification is not possible. Similarly, direct trimming of a 1pF capacitor with 0.1% resolution (1fF) is also not easy to achieve. In this work, a segmented coarse-fine trimming circuit for the capacitor is used to relaxes the trimming resolution restriction. Moreover, the minimum value of a MIM capacitor is around 40fF, however, the straight binary shceme requires a 10fF capacitor, which is difficult to achieve. In this work, a sharing decoding sheme is used and will be shown in the following secntion.

3.1.3.2 Design

The trimming circuit is presented in Figure 3.2. A 50fF capacitor C_S is connected in series with a 6-bit binary fine-trimming C_F, which is much larger than C_S. Trimming C_F to a larger value makes the equivalent value of C_S in series with C_F closer to C_S. The series connection of C_S and C_F is then connected in parallel with a 6-bit binary coarse-trimming C_C. Figure 3.3 shows the connection diagram of a 6-bit binary trimming circuit. C_C(C_F) increases from 720fF(130fF) to 1350fF(760fF) with 10fF trimming steps.

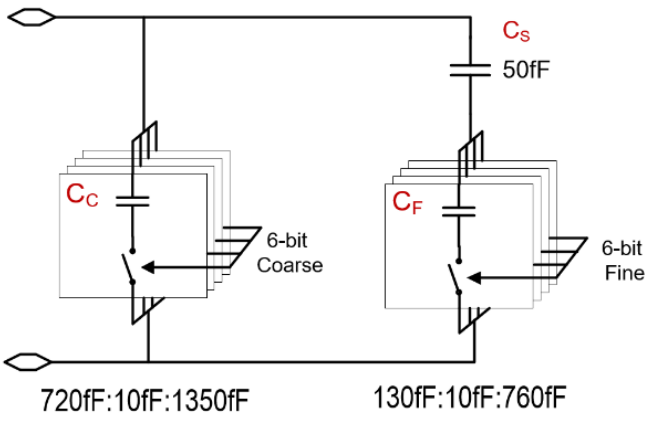

Figure 3.2 Nominal frequency trimming on C_0

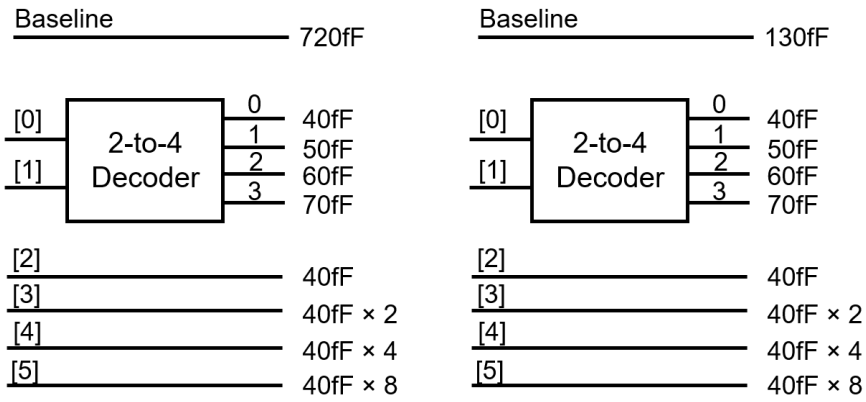

Figure 3.3 Connecting diagram of the coarse trimming capacitor C_C (left) and the fine trimming capacitor C_F (right)

Cadence simulation results are shown below to verify that this trimming network can meet the requirement of a ±30% trimming range with a worst-case trimming resolution of 0.1%. Figure 3.4 gives the corresponding frequency with each coarse trimming code. The trimming range covers from 7MHz to 13MHz, verifying that the coarse trimming can cover the ±30% trimming range.

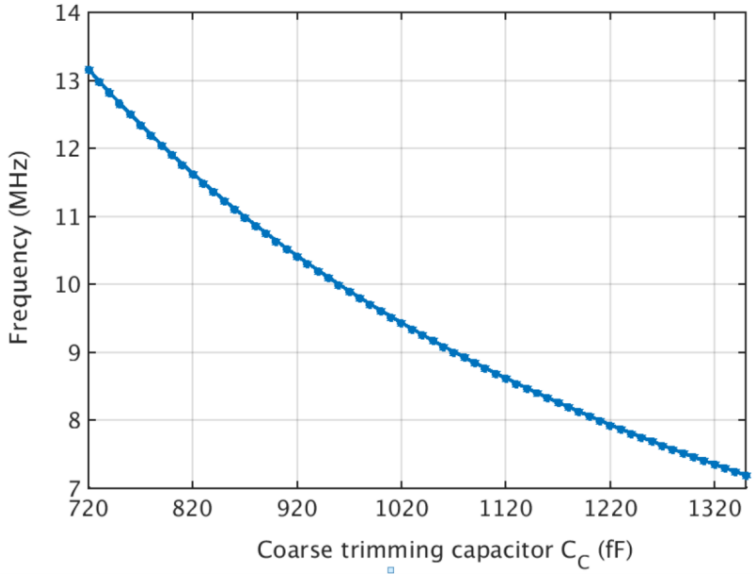

Figure 3.4 Coarse trimming range

Figure 3.5 shows the frequency resolution with each fine trimming code in TT, SS, and FF corners. The worst-case trimming resolution is 0.1%, or equivalently 1fF, with a practically realizable 10fF DAC LSB.

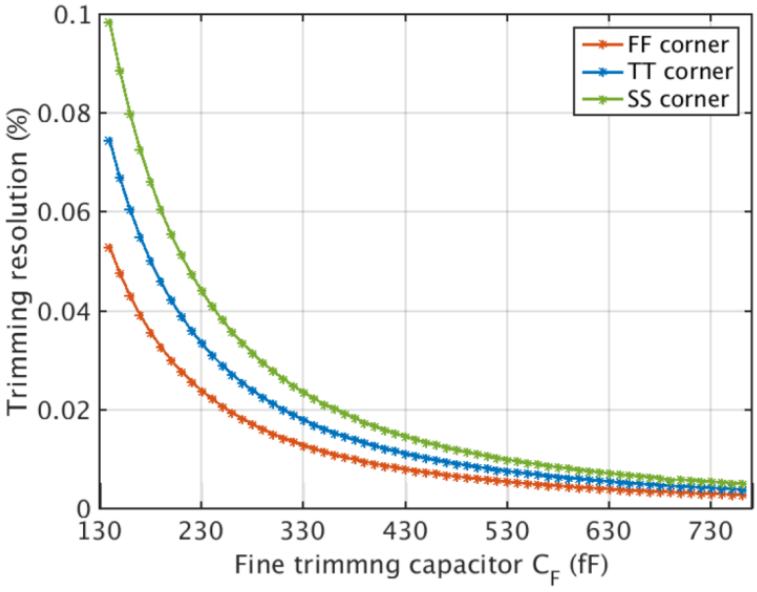

Figure 3.5 Frequency error for each trimming step

The trimming circuit should cover the entire frequency range without leaving a dead zone when switching between different trimming codes. Figure 3.6 shows the fine trimming range with three different but neighboring coarse trimming codes at the worst case (C_C=720fF, 730fF and 740fF). There is always a frequency overlap between two neighboring fine-trimming ranges.

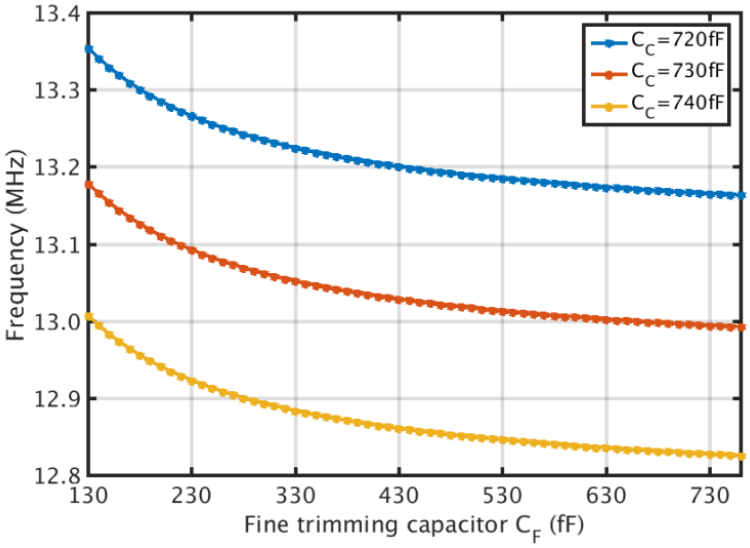

Figure 3.6 Fine trimming range overlap at worst case

3.1.4 Temperature Compensation

3.1.4.1 Specification and Design Choice

As discussed in Section 2.1, instead of building a zero-TC resistor using resistors with complementary TCs, the proposed temperature compensation is implemented via the voltage divider using resisitors with same TC polarity. The temperature compensation specification of this work is to achieve a <35.3ppm/°C TC from −45°C to 125°C after 1-point trimming.

3.1.4.2 Theoretical Temperature-dependent Model

The temperature dependence models of each resistor, capacitor and output frequency are expressed in equation 3.1-3.5. For simplicity, only their first-order TCs are taken into the consideration.

$$R_0(\Delta T) = R_{00} \cdot (1 + TCR \cdot \Delta T) \quad 3.1$$

$$R_1(\Delta T) = R_{10} \cdot (1 + TCR_1 \cdot \Delta T) \quad 3.2$$

$$R_2(\Delta T) = R_{20} \cdot (1 + TCR_2 \cdot \Delta T) \quad 3.3$$

$$C_0(\Delta T) = C_{00} \cdot (1 + TCC \cdot \Delta T) \quad 3.4$$

$$T_{osc}(\Delta T) = 4 \cdot R_0(\Delta T) \cdot C_0(\Delta T) \cdot \ln\left(1 + \frac{R_1(\Delta T)}{R_2(\Delta T)}\right) \quad 3.5$$

R_{00}, R_{10}, R_{20} and C_{00} are the nominal values of R_0, R_1, R_2 and C_0; TCR_0, TCR_1, TCR_2 and TCC are the TCs of R_0, R_1, R_2 and C_0; ΔT is the temperature change. Taking the first derivative of $T_{osc}(\Delta T)$ ($T_{osc}'(\Delta T)$) and approximating it with Taylor's theorem, when ΔT approaches zero, $T_{osc}'(\Delta T)$ can be simplified in equation 3.6. To minimize the first-order TC, $T_{osc}'(\Delta T)$ is set to zero, resulting in an optimized TCR_2 expressed in equation 3.7.

$$T_{osc}'(\Delta T) = 4R_0C_0 \cdot \left[(TCR_0 + TCC_0) \cdot \ln\left(1 + \frac{R_{10}}{R_{20}}\right) + (TCR_1 - TCR_2) \cdot \frac{R_{10}}{R_{10} + R_{20}}\right] \quad 3.6$$

$$TCR_2 = (TCR_0 + TCC_0) \cdot \left(1 + \frac{R_{20}}{R_{10}}\right) \cdot ln\left(1 + \frac{R_{10}}{R_{20}}\right) + TCR_1 \quad 3.7$$

R_0 and R_1 are p-poly resistors, C_0 is a MIM capacitor, and the optimized TCR_2 can be calculated according to equation 3.7 as -600ppm/°C. Such a resistor can be created by combining a 72.6kΩ p-poly resistor (R_{2a} with TC=-234ppm/°C) with a 27.4kΩ n-poly resistor (R2b with TC=-1500ppm/°C) in the nominal case. As a result, a zero 1st-order TC is obtained for the oscillation frequency by using resistors that have the same TC polarity, making the method applicable to all processes. Taking the higher-order TC into consideration, especially the second-order TC, the temperature dependency of the output frequencyis shown in Figure 3.7, resulting in an approximately 24ppm/°C residual TC.

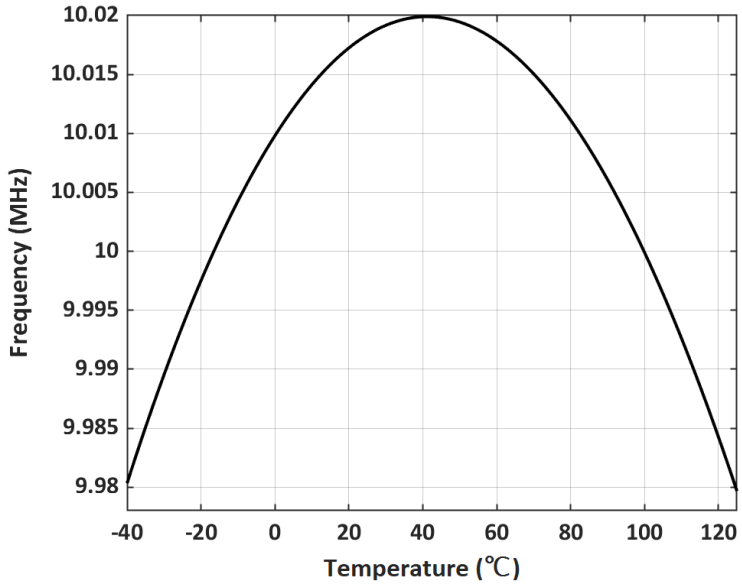

Figure 3.7 Theoretical temperature dependency model

Until now, all passive elements in the front-end are determined as summarized in Table 3.2.

Component	Type	Nominal value	TC_1	TC_2
R_0	p-poly resistor	36kΩ	-2.38e-4	8.85e-7
R_1		100kΩ		
R_{2a}		72.6kΩ		
R_{2b}	n-poly resistor	27.4kΩ	-1.506e-3	2.679e-6
C_0	MIM capacitor	1pF	-2.94e-5	0

Table 3.2 Value of the passive components

3.1.4.3 Implementation

To achieve a near zero first-order TC in every corner and save area, a 4-bit TC trimming network is implemented in R_2, where the p-poly resistor R_{2a} is connected with the n-poly resistor R_{2b} by a series of switches as shown in Figure 3.8. By closing one switch at one time, the ratio between R_{2a} and R_{2b} changes but the length of the resistive path that the current flows through is the same. In this way, the value of R_2 is roughly the same, which relaxes the requirement for the trimming range since the frequency error caused by the variation of R_2 can be trimmed.

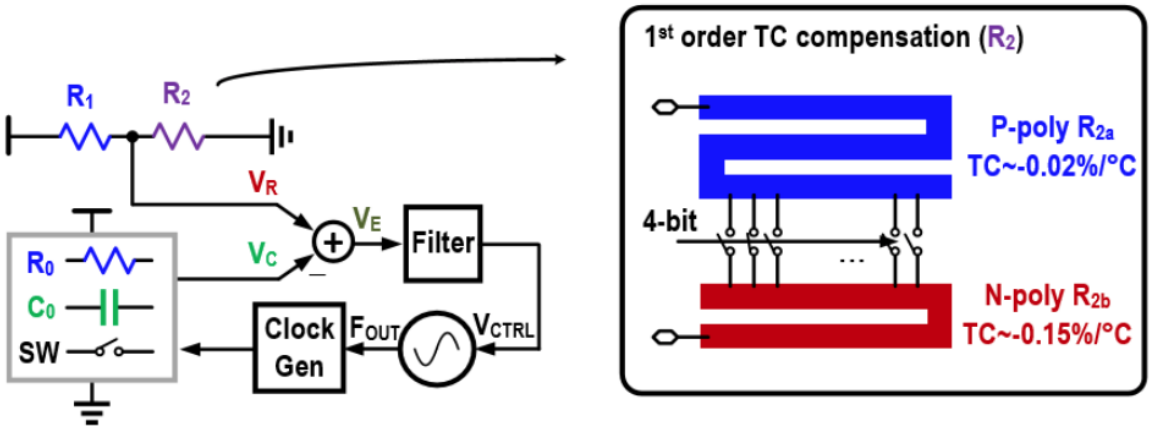

Figure 3.8 R_2 connection diagram with a 4-bit temperature trimming network

On-chip resistors have a ±15%~±20% spread in different corners. The 4-bit TC trimming achieves a 5ppm/°C trimming step and the TC can always be minimized under 35.3ppm/°C in the worst case (R_{2a} has a +15% spread and R_{2b} has a -15% spread). Figure 3.9 shows the layout of R_2, which takes 9% of the overall chip area. When decreasing/increasing the TC trim code by 1 step, R_2 will have a 0.09% value variation due to a 90Ω resistance difference between the p-poly (=809.5Ω) and n-poly (=721.7Ω) unit trimming resistors. This will lead to a 0.06% frequency variation, but the frequency trimming network can correct it. Trimming switches are realized by NMOS transistors. To reduce the error introduced by on-resistance of the switch, these NMOS switches are designed to have a small on-resistance of 190Ω.

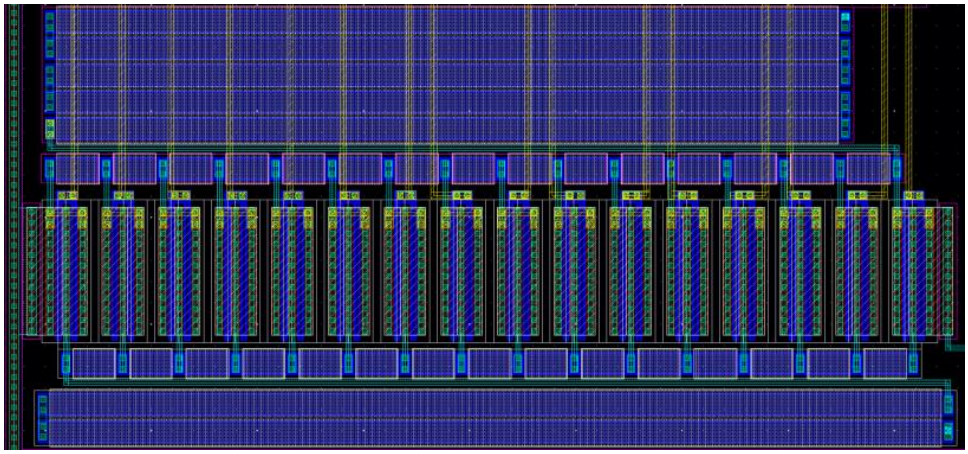

Figure 3.9 Layout of the 4-bit trimmable R_2

3.2 FLL Readout Design

3.2.1 Voltage-Controlled Oscillator

3.2.1.1 Specification

The voltage-controlled oscillator (VCO) is the main core of the loop. The output clock is a rail-to-rail square wave. The center frequency of VCO is 40MHz. The input signal of the VCO is from the integrator stage. Hence, the input signal range of the VCO must be within the output range of the integrator.

3.2.1.2 Design

Figure 3.10 shows the structure of the proposed VCO. It is implemented using a 3-stage current-starved ring oscillator. The oscillating period is determined by the delay of each inverter stage. To relax the restriction of the integrator's output swing, a 4-bit unary current DAC is applied for the corner trimming. Figure 3.11 gives the VCO's output frequency variation for different control signals due to temperature and process changes. The input signal range of VCO is from 680mV to 900mV.

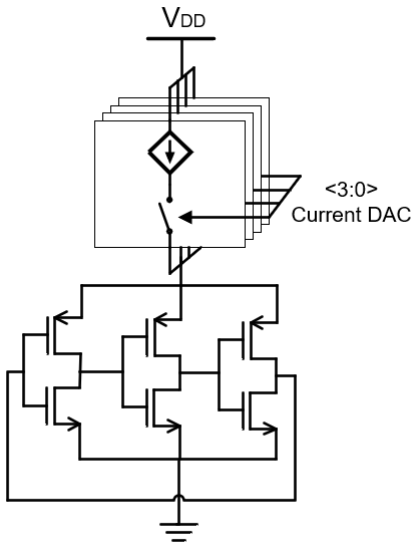

Figure 3.10 VCO schematic

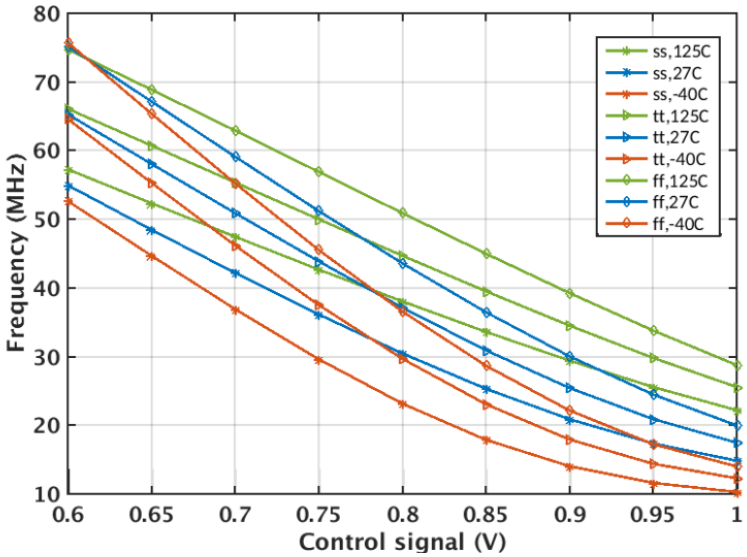

Figure 3.11 VCO input range

Figure 3.12 shows the detailed design of the bias current source. M1 is the input transistor, providing a voltage-to-current gain gm. M2 is a cascode transistor, providing a shielding property. The output-node voltage V_{cco} is not always a constant, if Vcco changes by ΔV, the resulting voltage change at the source of the cascode is much less. In other words, the cascode transistor "isolates" the input transistor from the variations in the output voltage. This

cascode transistor M2 is a PMOS with a medium threshold (MVT) whose threshold voltage is smaller than that of the nominal PMOS. In this way, M2 can be biased with the same voltage as the input transistor without an extra biasing circuit. The dimension of M2 is kept small to reduce the voltage coupling between the input and the output signal.

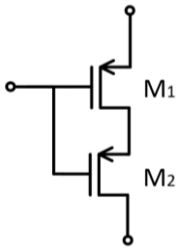

Figure 3.12 Bias current source structure

3.2.1.3 Level shifter

The output of the 3-stage current-starved ring oscillator swings from ground to V_{cco}. The function of the level shifter is to modulate one voltage level to another, providing compatibility across integrated circuits with varying voltage needs.

In this work, a level shifter is applied as shown in Figure 3.13. Transistors Mp3 and Mp4 speed up the low-to-high transition of the output clock. The power consumption of the level shifter is 1.34µA. Figure 3.14 gives the noise performance at the level shifter's input and the output node. Simulation results show that the added jitter due to this level shifter is only 1ps.

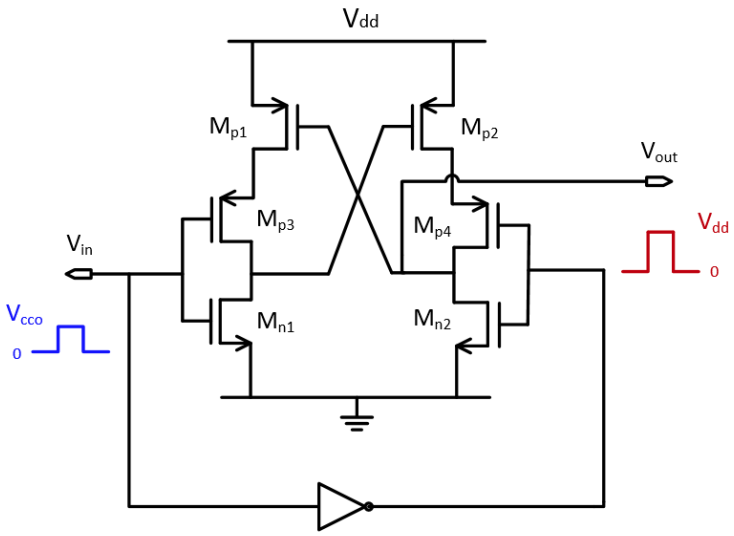

Figure 3.13 Convention mitigated level shifter

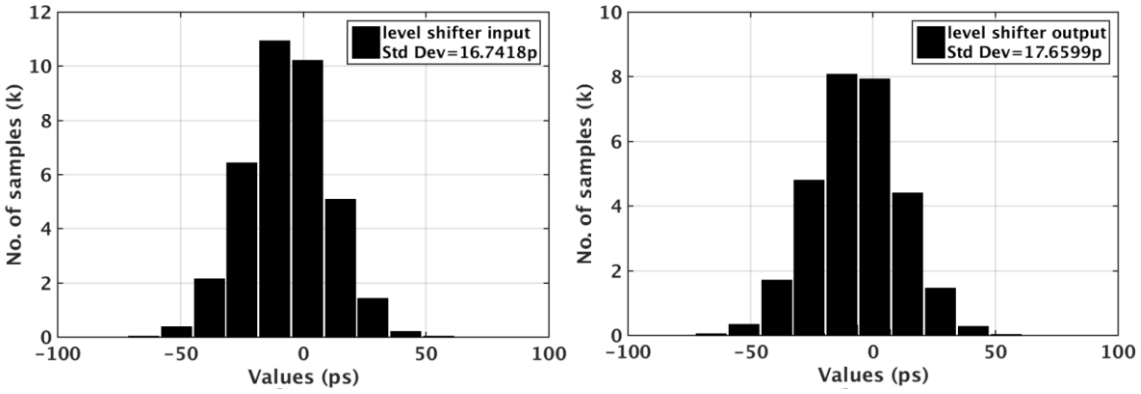

Figure 3.14 Period jitter at level shifter's input (left) and output (right)

3.2.2 GmC Integrator

3.2.2.1 Specification

There are some design specifications for the integrator: First, the integrator's output swing should cover the VCO's input swing (680mV to 900mV). Second, its noise and power contribution should be optimized for the benefit of good energy efficiency.

3.2.2.2 Design

Although the folded opamp has a wider output swing, the requirement of the output swing in this deisgn is not strict. The folded opamp has more branches between the power supply and the ground, which leads to increased power consumption. In this design, a compact and power-saving telescopic opamp is utilized as shown in Figure 3.15. Similar to the connection of the bias current of VCO, the PMOS and NMOS cascode transistors are all medium threshold (MVT) devices. The PMOSMVT cascode is biased with the same voltage as the PMOS current source and the NMOSMVT cascode is biased with the same voltage as the input pair, that is, the reference voltage V_R=1/2*V_{DD} from the front-end.

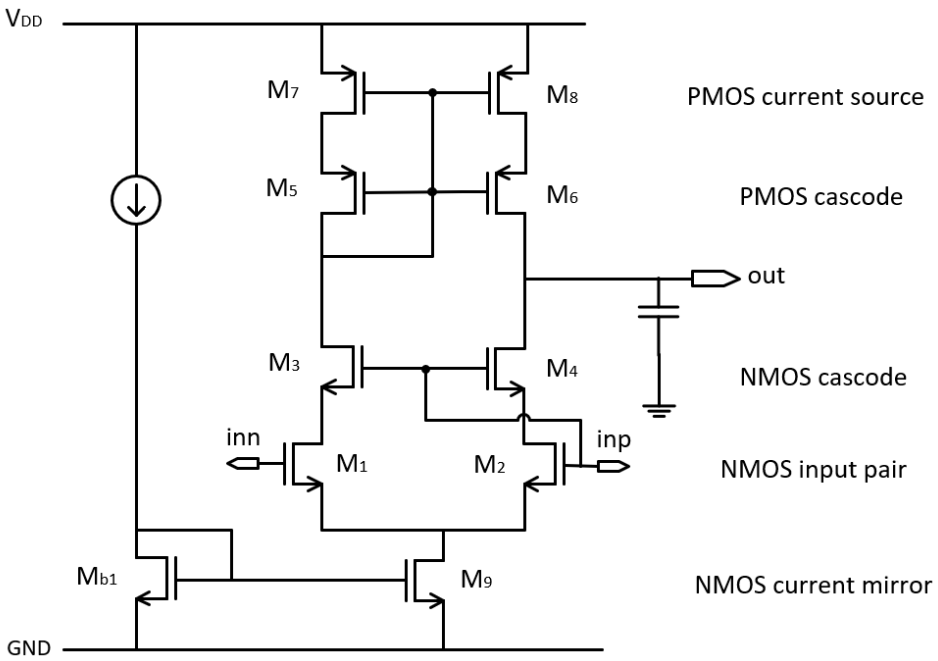

Figure 3.15 GmC integrator schematic

The DC gain (Av) of the opamp is determined by the transconductance (gm) and the output impedance (Rout) as expressed in equation 3.8

$$A_v = GmR_{out} \approx gm_1[(gm_3 r_{03} r_{01})||(gm_5 r_{05} r_{07})] \quad 3.8$$

There are two main thermal noise contributors: the RC front-end and the FLL readout circuit. Resistors in the front-end contribute to the thermal noise and the total noise power spectrum density (PSD) is

$$\overline{V_{n,FE}^2} = 4kT \times (R_1||R_2) + 4kT \times R \quad 3.9$$

Most of the thermal noise from the readout comes from the gm stage and the input referred PSD of the differential gm stage is

$$\overline{V_{n,gm}^2} = 2 \times 4kT\gamma/gm \quad 3.10$$

The noise from the reaout circuit should be equal or lower than that from the front-end (2.23nV/$\sqrt{\text{Hz}}$ from calculation). The weak inversion operation region has been selected for the transistors due to a large gm/I_D ratio of around 20. Considering an even noise consumption split between the front-end and the gm stage, the gm is set to be 5µS to achieve good power efficiency. The integration capacitor (C_{int}) is 7pF.

Figure 3.16 shows the ac simulation result of the gm stage. The integrator provides an 80dB dc-gain and a 90° phase margin. The dominant pole is at 40Hz and the gain-bandwidth frequency is 300Hz. A second pole is at 40MHz, located at the gate of M7, approximately given by $gm_7/2\pi C_p$, where C_p is the total parasitic capacitors from the gate of M7 to the ground. This pole is usually at a higher frequency compared to the main pole.

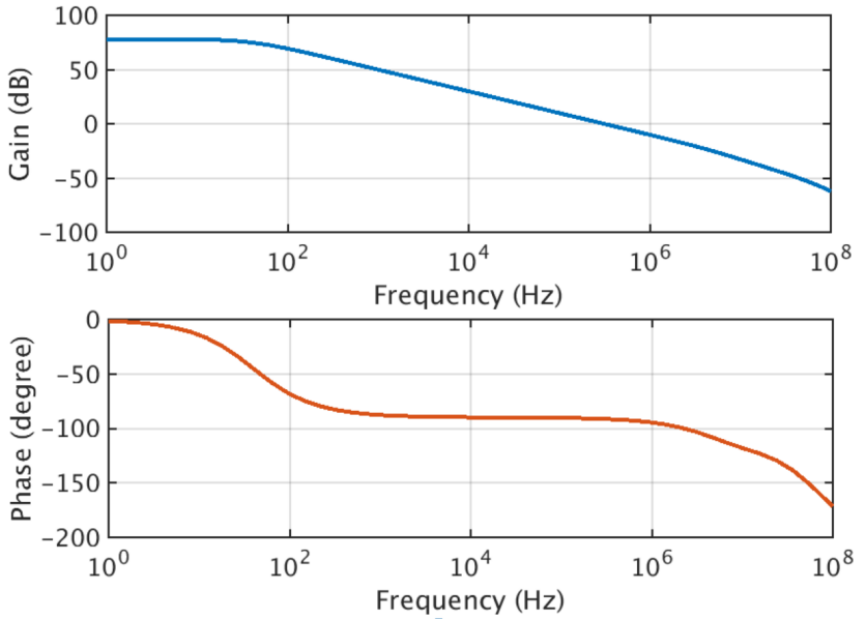

Figure 3.16 AC simulation of the GmC integrator

The noise simulation of the gm stage is shown in Figure 3.17. The flicker noise dominates at low frequency, while the thermal noise dominates at high frequency. The corner frequency is at 4kHz, where the flicker noise equals the thermal noise.

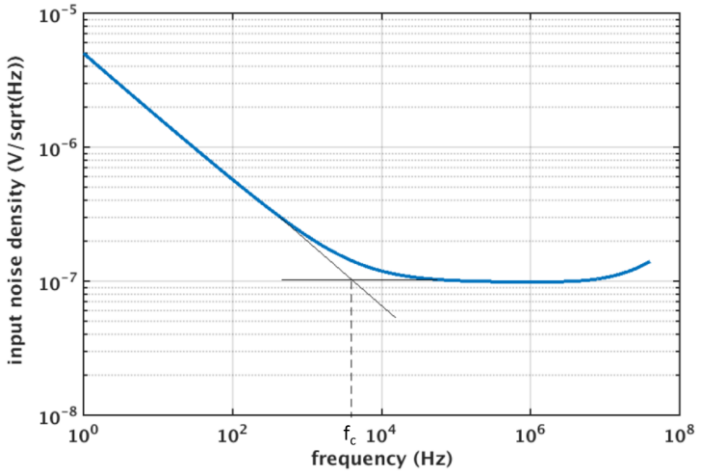

Figure 3.17 Noise floor of the gm stage

The minimum output voltage is limited by the three NMOS overdrive voltages and the maximum output voltage is limited by the two PMOS overdrive voltages. Connecting the OTA in a unity-gain feedback style as shown in Figure 3.18, and giving a rail-to-rail sinusoidal signal at the input, the output in the linear amplification range is from 0.5V to 1V, as shown in Figure 3.19.

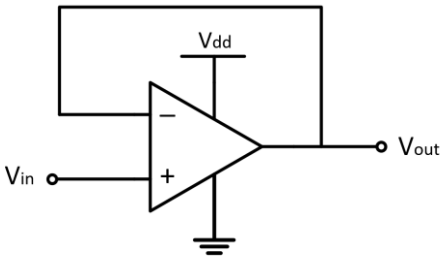

Figure 3.18 Unity-gain amplifier

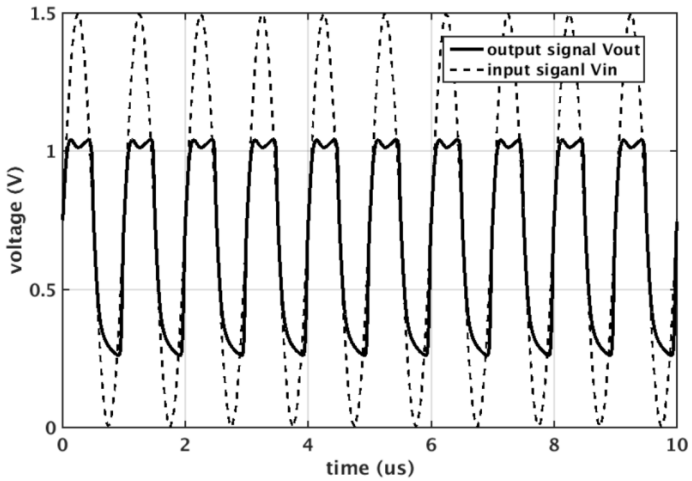

Figure 3.19 Output swing of the gm stage

3.2.2.3 Chopper and notch filter

As discussed in Section 2.1, the chopper is utilized to remove the error due to the low-frequency noise, e.g., the offset and the 1/f flicker noise of the gm stage. The chopper is a polarity reversing switch with the connection shown in Figure 3.20. Figure 3.21 shows the chopping principle in the frequency domain. The low-frequency input signal is modulated to high frequency by the input chopper and then demodulated back to low frequency, while the low-frequency error is only modulated once by the output chopper to high frequency and then filtered out by a low-pass filter whose cut-off frequency is lower than the chopping frequency.

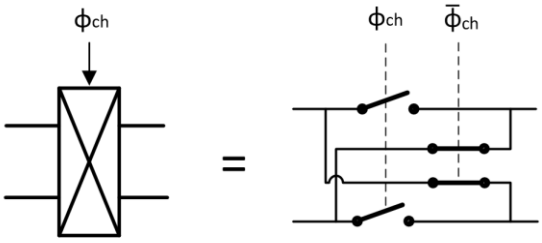

Figure 3.20 Chopper schematic

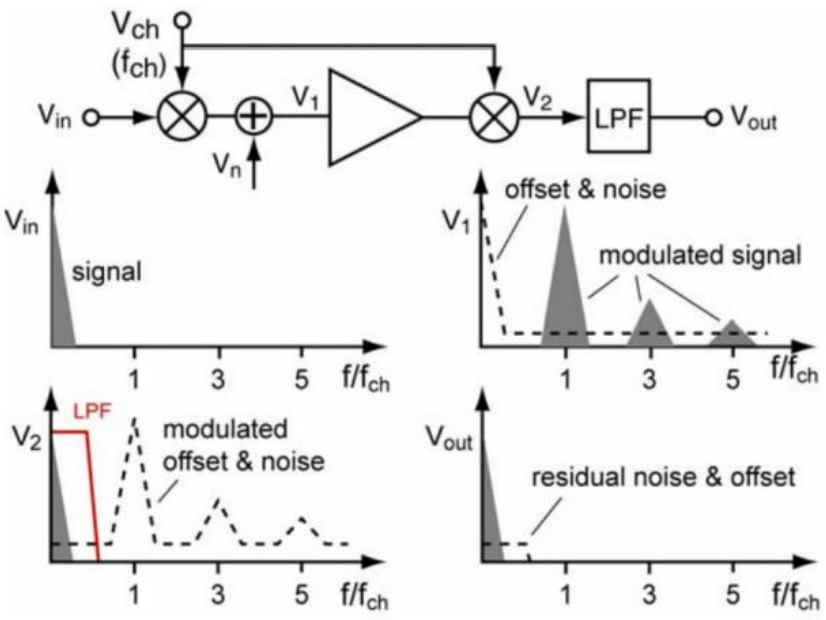

Figure 3.21 Chopping principle in the frequency domain [16]

Assuming a 10mV input-referred offset of the gm stage, simulation results show the frequency error without and with chopper is 4% and 0.04%. However, by switching the polarity of the switches, the current goes into and out of the integration capacitor period, resulting in a 14mV peak-to-peak ripple. As discussed in Section 2.1, a single-phase notch filter is implemented in this design. Figure 3.22 shows the design of the filter, it consists of two capacitors C_{MID} (=1.8pF) and C_{HOLD} (=2.7pF) and two switches driven by the sample (Φ_S) and hold (Φ_H) signals. Since the VCO input range is 0.68V to 0.9V, the switches are realized by the combination of NMOS and PMOS transistors.

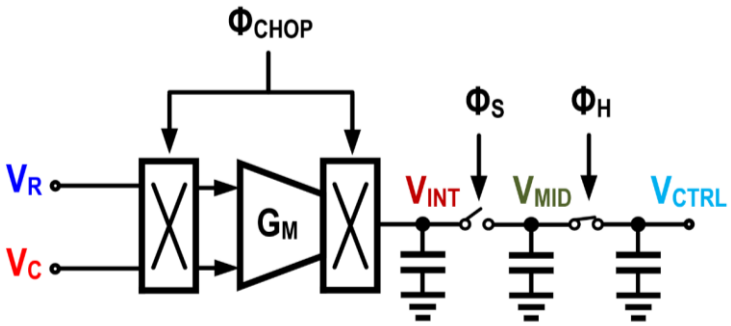

Figure 3.22 Notch filter schematic

3.2.3 Phase generator

Figure 3.23 shows the overall design of the phase generator. As discussed in Section 2.1, the 40MHz output clock of the VCO is divided by 4 by a chain of 2 DFFs. The chopping frequency is 1.25MHz. The sample-and-hold frequency is half of the chopping frequency.

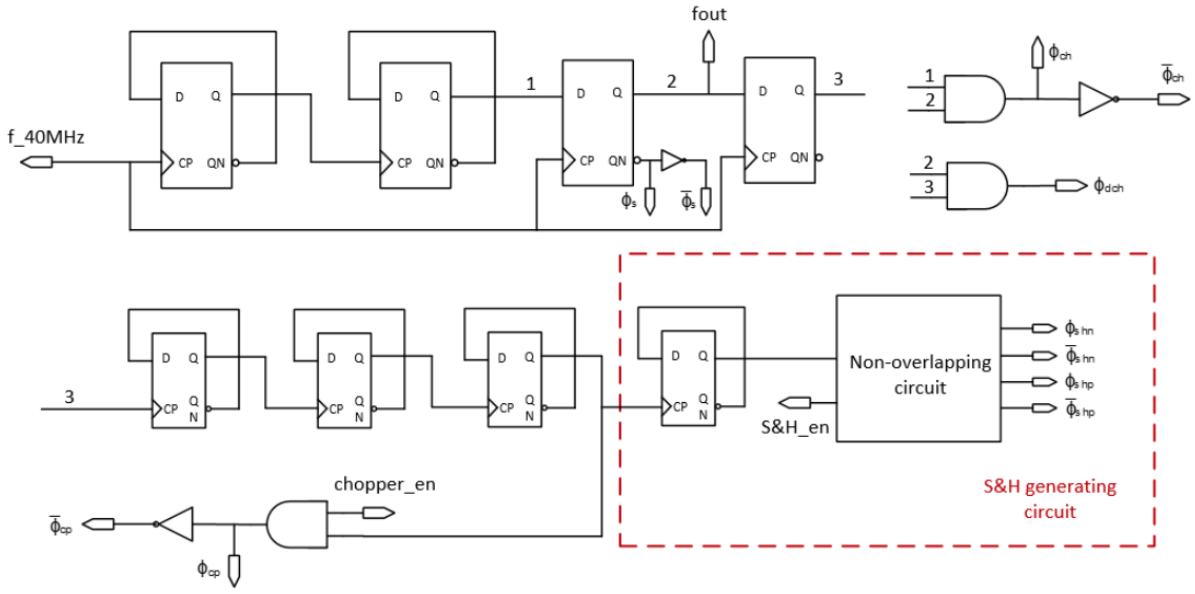

Figure 3.23 Phase generator circuit diagram

The phase generator block is powered individually by a digital supply. It consumes an 8.8µA current in the nominal case. The time domain simulations of the phase generator are shown in Figure 3.24.

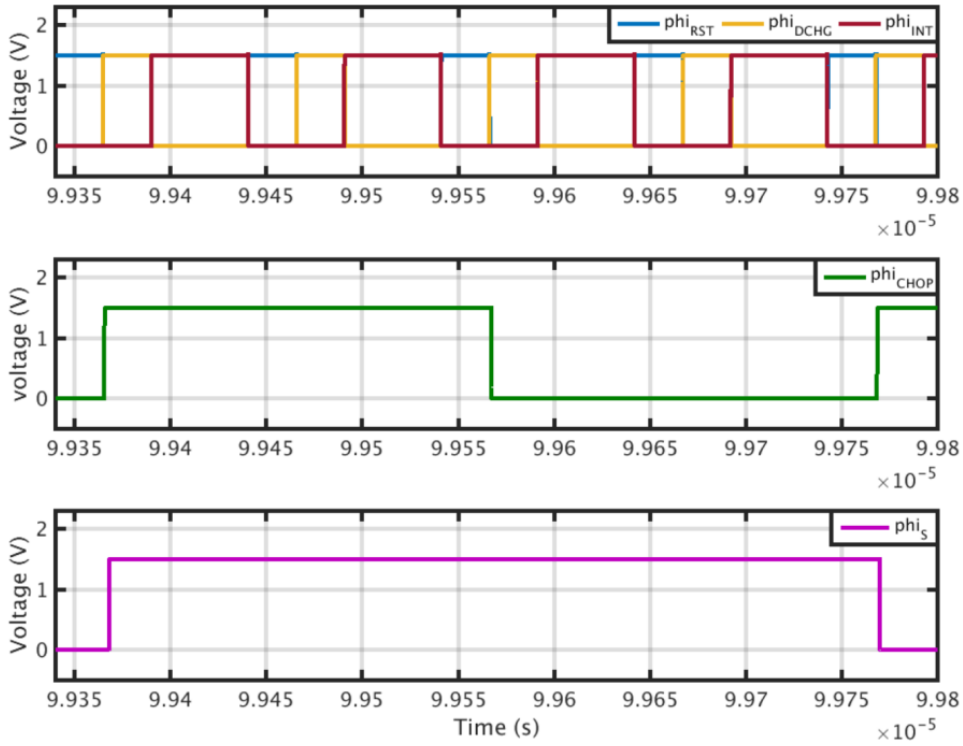

Figure 3.24 The timing diagram of the generated phase signals

Chapter 4 Measurements

The frequency reference prototype was fabricated in a TSMC 0.18µm CMOS process, and the microphotographs are shown in Figure 4.1. Seven chips (112 samples) were packaged in 16-pin dual-in-line (DIL) ceramic packages. Figure 4.2 shows a picture of a ceramic-packaged chip. One oscillator has a chip area of 100µmx100µm and draws 56.7µA (27.5µA analog and 29.2µA digital) from a 1.5V supply. About 2/3 of the digital power is used to drive the output buffer.

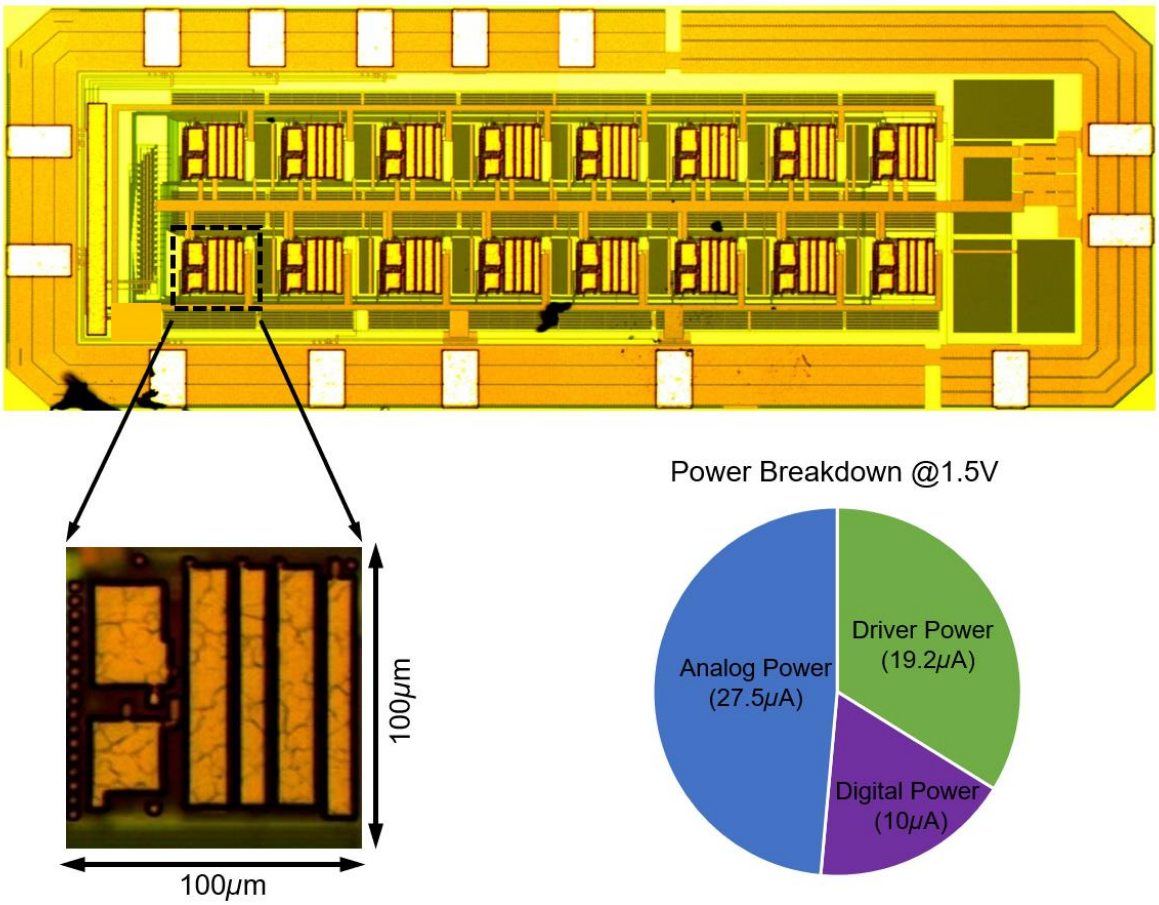

Figure 4.1 Chip micrograph and its power breakdown

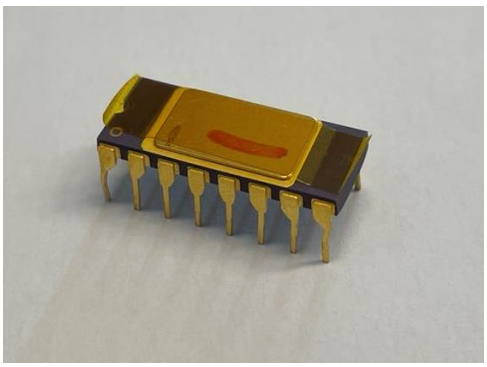

Figure 4.2 Picture of a ceramic-packaged chip

4.1 Measurement setup

Temperature characterization of the chips was performed in a Votsch VT 7004 oven. The temperature reference was a Pt-100 temperature sensor, whose resistance was measured using a Keithley 2002 precision multimeter. By placing the chips and the Pt-100 sensor inside a metal box, thermal equilibrium can be achieved, which eliminates the effect of the oven's temperature error. The diagram of the measurement setup is shown in Figure 4.3. A frequency counter Agilent 53152A was used to measure the output frequency at each temperature point.

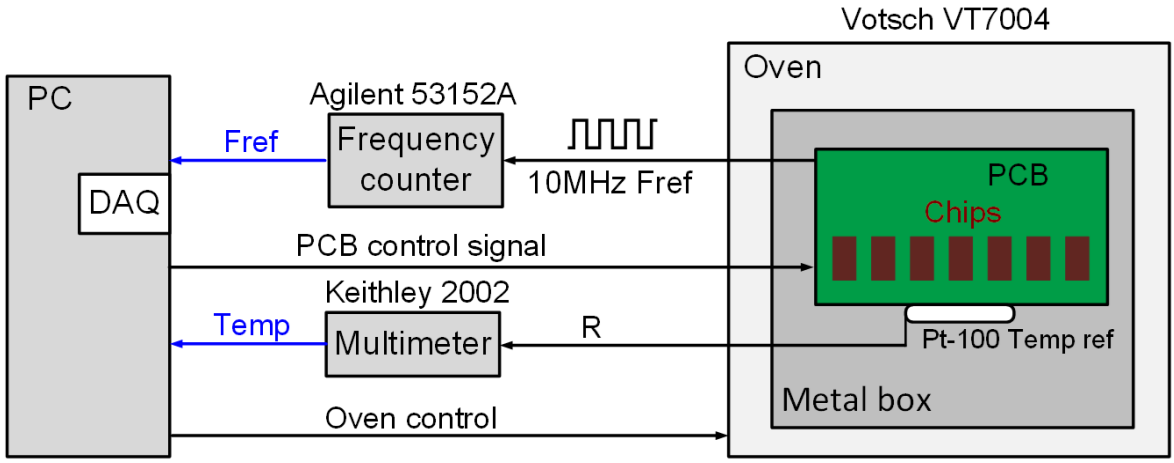

Figure 4.3 Measurement setup

4.2 Measurement results

Based on the agreement with Cadence simulations in the TT corner, it is easy to distinguish that all chips were manufactured in the TT corner. The same TC trim codes were applied to all samples, since the intra-batch TC spread turned out to be quite small (±8ppm/°C). The absolute frequency f_0 has a spread of ±1.9% and was individually trimmed at room temperature (RT, ~25°C). To rule out the effect of moisture, a dehumidifier was used during characterization.

As shown in Figure 4.4, the frequency reference achieves an inaccuracy of ±0.28% over the automotive temperature range from −45°C to 125°C, resulting in a residual TC of 31.5ppm/°C (box method). However, significant hysteresis (1500ppm worst-case) is observed as the samples are cycled from hot to cold, mainly due to the instability of the polysilicon resistors. Each sample was cycled twice, resulting in a cycle-to-cycle variation of less than ±200ppm as shown in Figure 4.5, which is much smaller than the observed hysteresis.

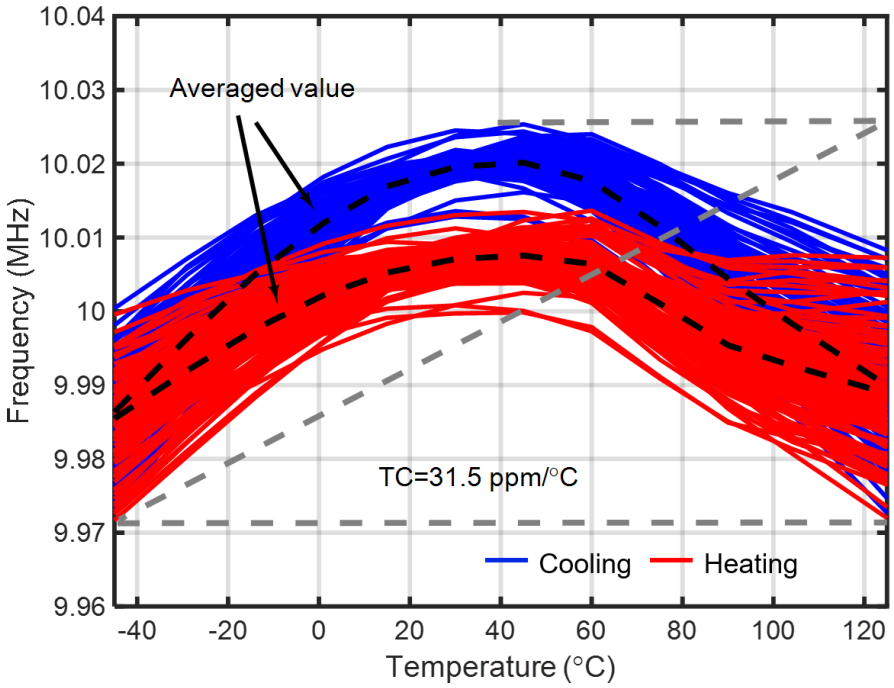

Figure 4.4 Temperature sensitivity and hysteresis of the frequency reference (112 samples)

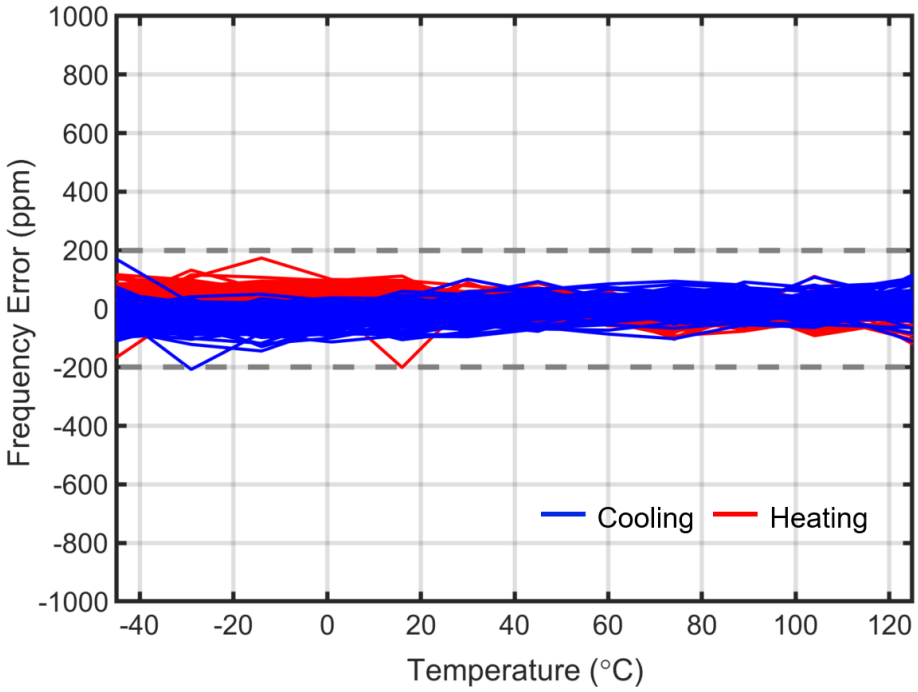

Figure 4.5 Measurement repeatability error

Since polysilicon resistors are also known for large drifts [19], accelerated aging experiments were conducted by baking the measured samples at 150°C for one week. After that, the chips were characterized using the same TC and f_0 trim codes as those before aging. As shown in Figure 4.6, after aging, the frequency reference achieves an inaccuracy of ±0.35% over the

automotive temperature range from −45°C to 125°C, resulting in a residual TC of 41.5ppm/°C (box method). Less than ±250ppm cycle-to-cycle frequency error is observed as shown in Figure 4.7.

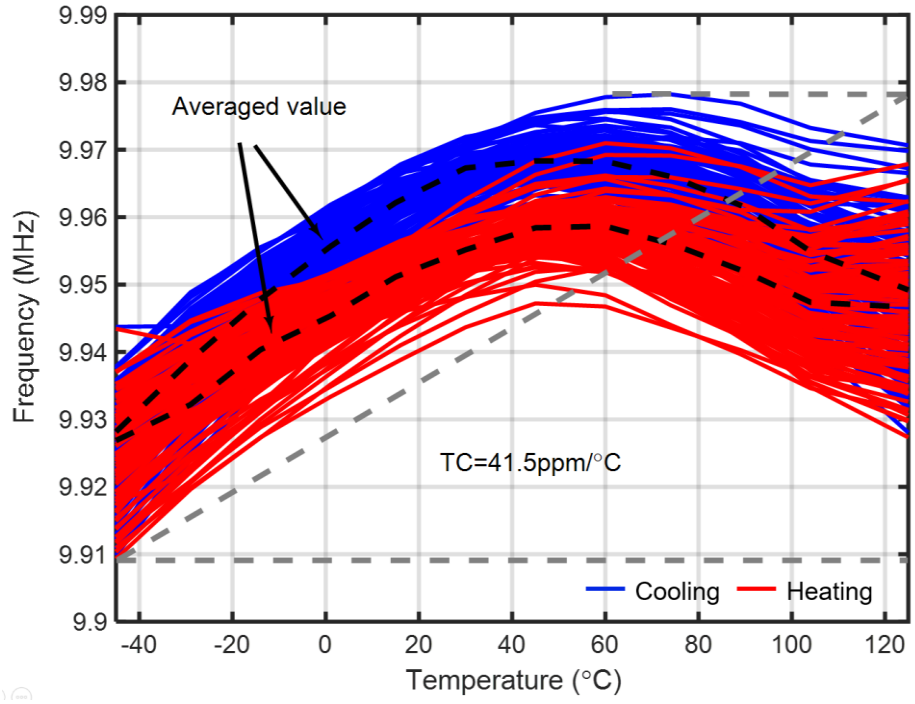

Figure 4.6 Temperature sensitivity and hysteresis of the frequency reference (112 samples) after aging

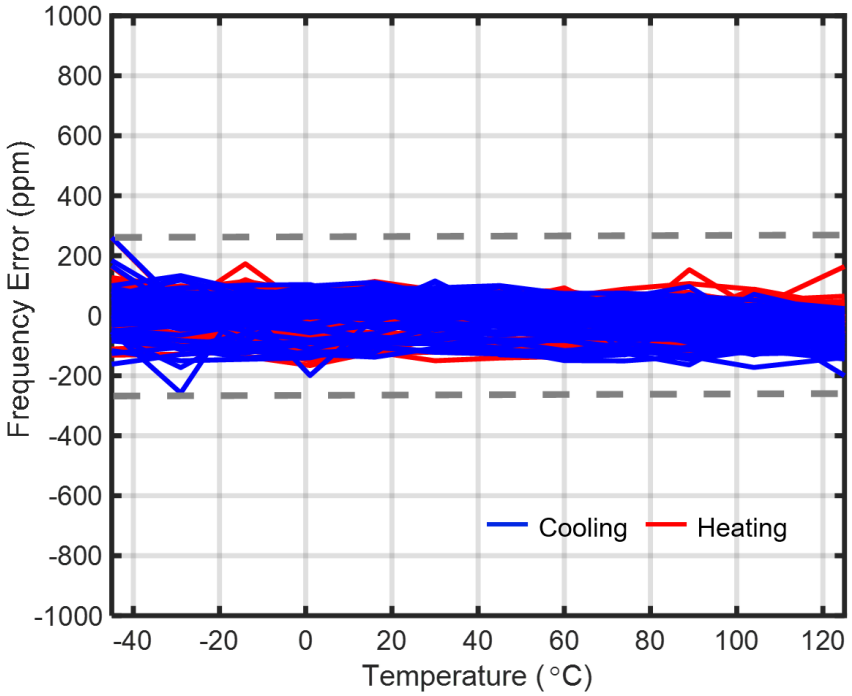

Figure 4.7 Measurement repeatability error after aging

To compare the chips' performance before and after aging, Figure 4.8 shows the averaged frequency of 112 samples before and after aging in the same plot. Both the nominal frequency

(0.5%) and TC (10ppm/°C) suffer from drift. However, the former can be trimmed at room temperature with the help of an external reference [20], while the latter is 3x smaller than the original residual TC, and results in much less (0.17%) additional frequency error over a lifetime.

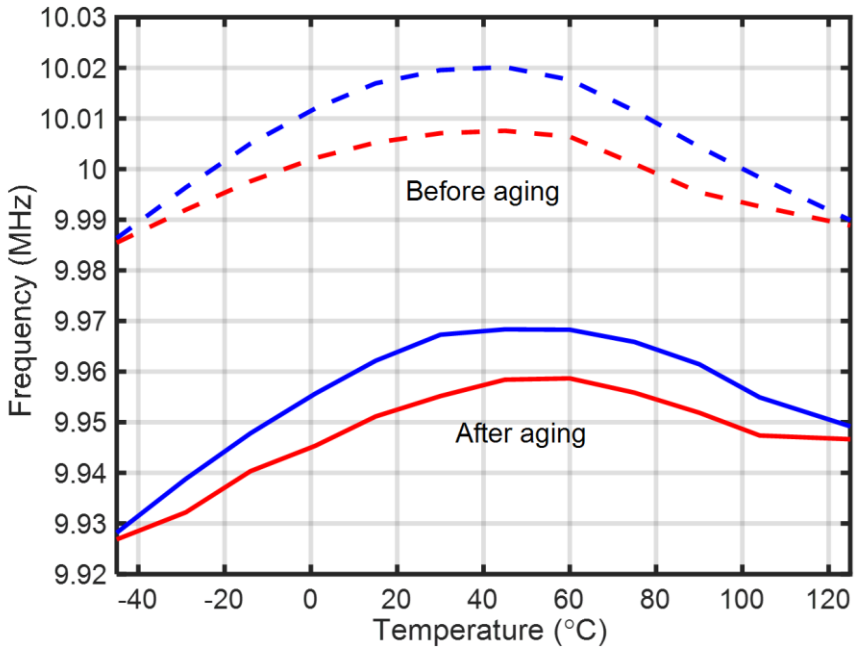

Figure 4.8 Averaged frequency of 112 samples before and after aging

The measured supply sensitivity is 9000ppm/V from 1.5V to 1.8V as shown in Figure 4.9.

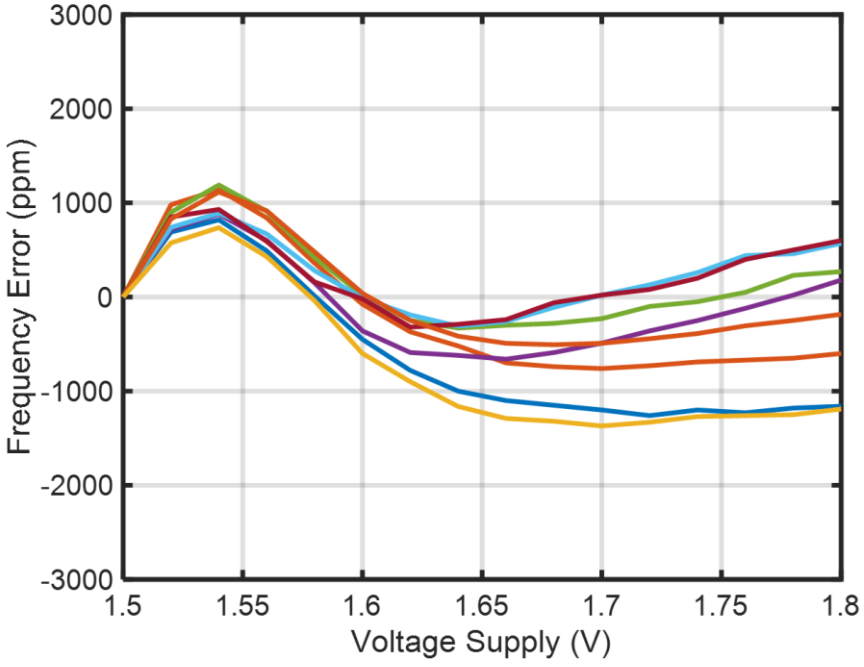

Figure 4.9 Frequency error versus supply voltage of 8 samples

Figure 4.10 shows the start-up behavior of the frequency reference. After setting V_{CTRL} to ground, the output frequency settles within 30µs. Enabling chopping and notch filtering

results in a step-wise settling transient, but does not change the settling time. The frequency reference achieves an output period jitter of 41.4ps$_{rms}$ (Figure 4.11, top) and an Allan deviation of 2.3ppm for a 0.6s-stride (Figure 4.11, bottom).

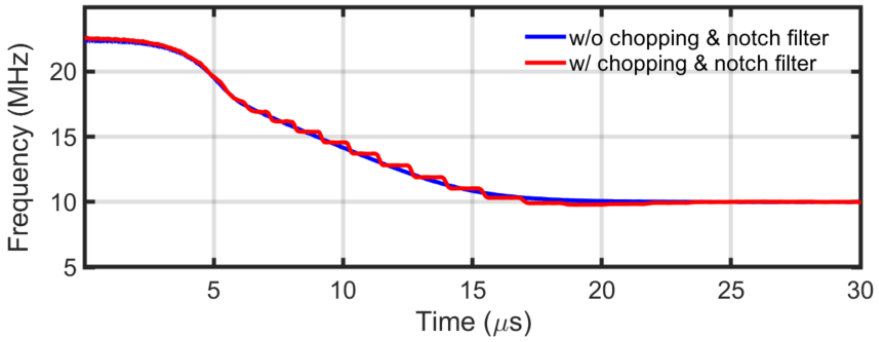

Figure 4.10 Transient response after V_{CTRL} reset

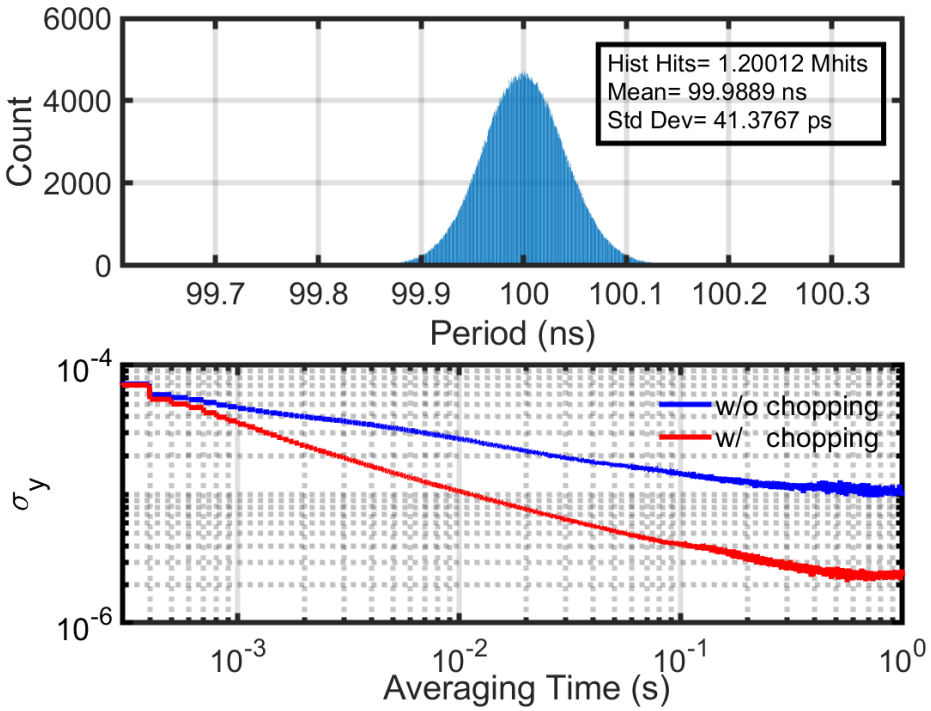

Figure 4.11 Measured period jitter (top) and Allan deviation (bottom)

To characterize the effect of packaging stress, seven plastic-packaged chips (112 samples) were also measured. Figure 4.12 shows a picture of a plastic-packaged chip. As shown in Figure 4.13, the plastic-packaged frequency reference achieves an inaccuracy of ±0.3% over the automotive temperature range from −45°C to 125°C, resulting in a residual TC of 35.3ppm/°C (box method). A less than 1200ppm hysteresis can still be observed. The plastic-packaged chips were also baked at 150°C for one week. As shown in Figure 4.14, after aging, the frequency inaccuracy is increased to ±0.36% over the temperature range −45°C to 125°C, resulting in a residual TC of 42.3ppm/°C (box method).

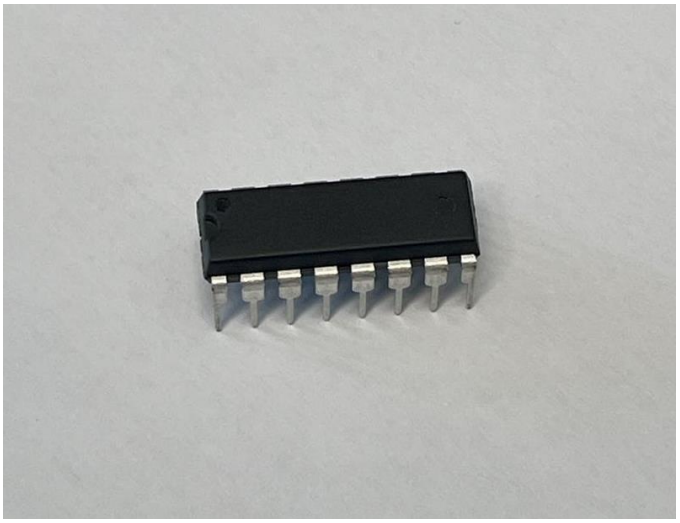

Figure 4.12 Picture of a plastic-packaged chip

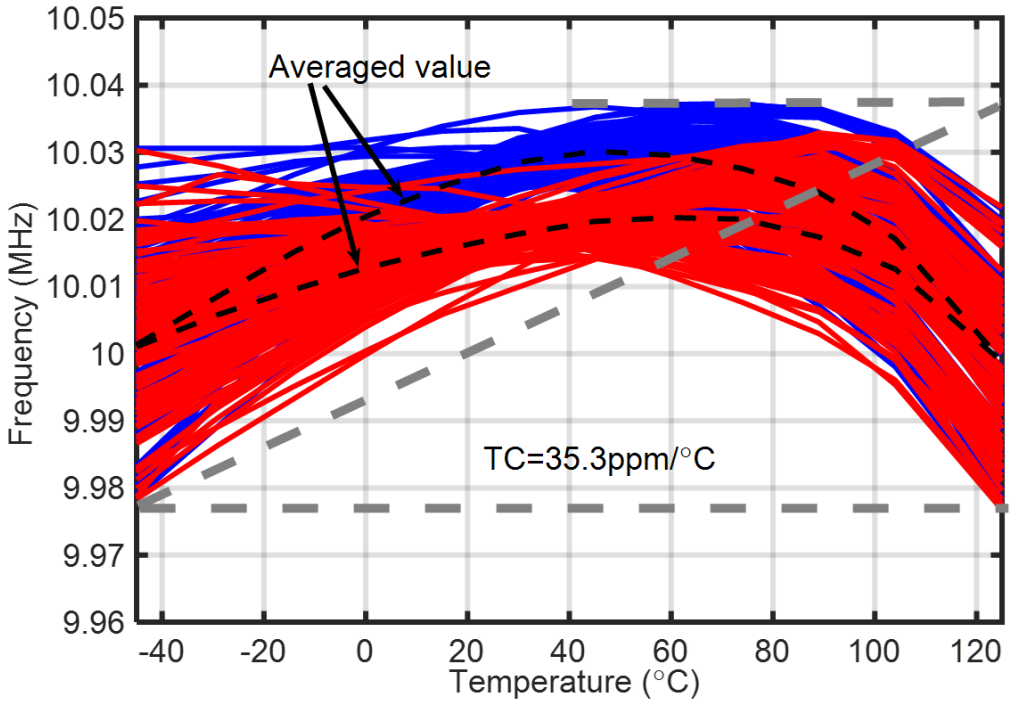

Figure 4.13 Temperature sensitivity and hysteresis of the frequency reference (112 samples with plastic packages)

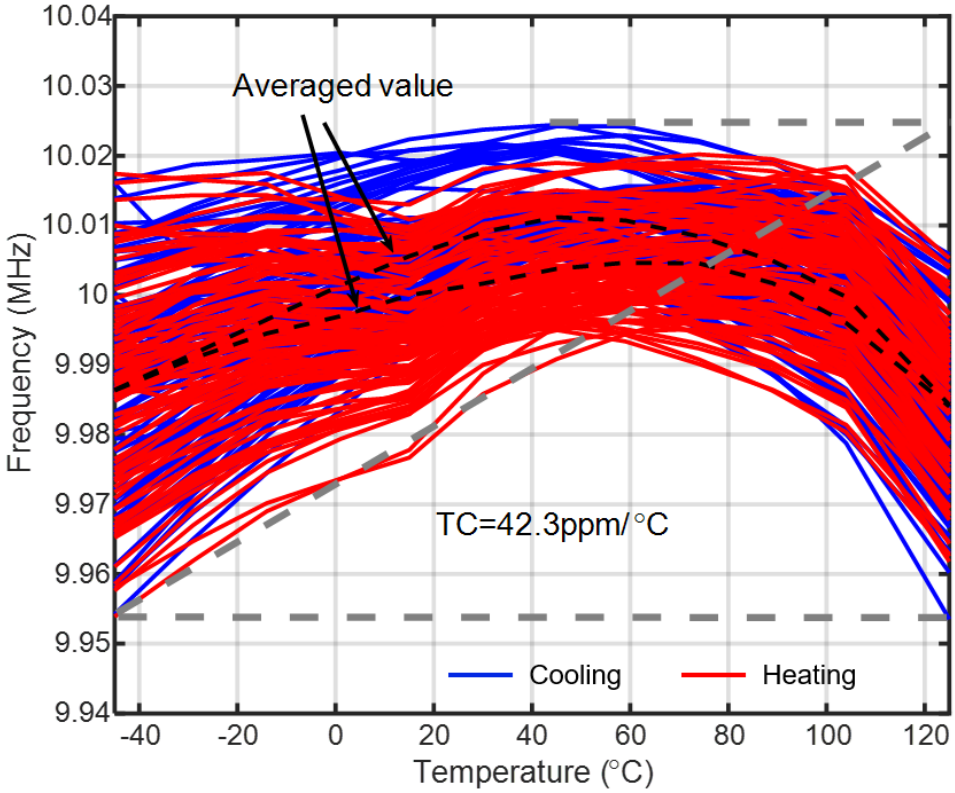

Figure 4.14 Temperature sensitivity and hysteresis of the frequency reference (112 samples with plastic packages) after aging

To compare the plastic-packaged chips' performance before and after aging, Figure 4.15 shows the averaged frequency of 112 samples before and after aging in the same plot. Both the nominal frequency (0.2%) and its TC (7ppm/°C) suffer from drift.

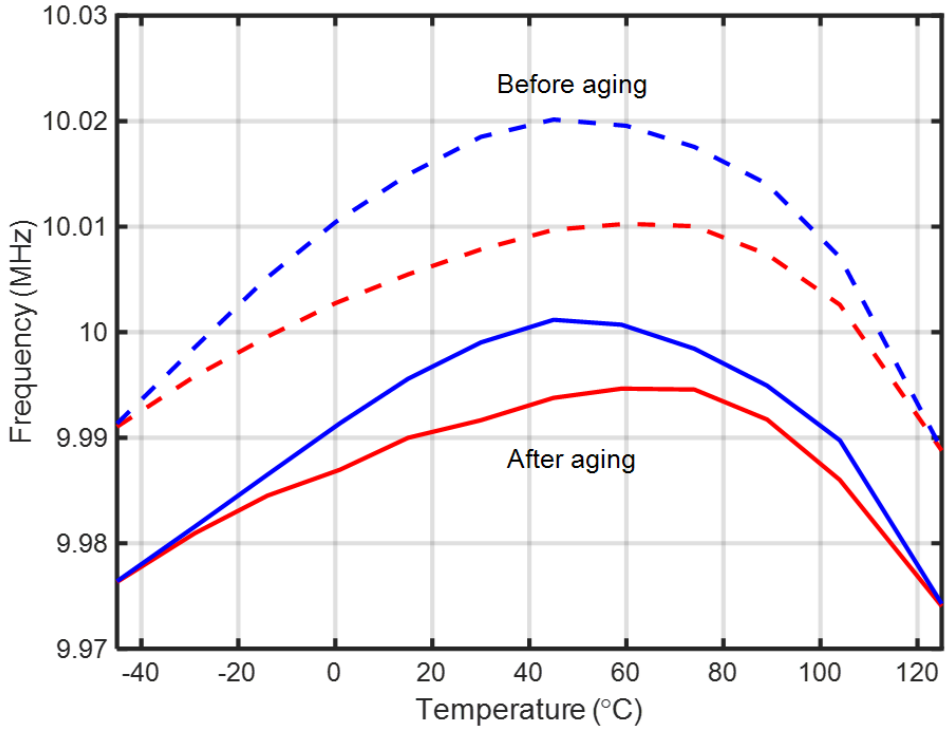

Figure 4.15 Averaged frequency of 112 samples with plastic packages before and after aging

4.3 Measurement summary

In Table 4.1, the performance of the proposed RC frequency reference with both ceramic and plastic packages is compared with that of other compact RC frequency references. To make a more straightforward comparison, the TC vs. chip area is shown in Figure 4.16. Despite the use of a mature 0.18µm technology, it achieves the best on-chip trimmed inaccuracy among compact (<0.02mm^2) CMOS frequency references, making it a competitive timing solution for low-cost IoT applications.

Reference	This work		JSSC 2022 [1]	JSSC 2022 [2]	JSSC 2022 [3]	TCAS-I 2016 [4]	JSSC 2020 [5]
Technology	0.18µm		0.18µm	65nm	65nm	0.18µm	0.18µm
Area [mm^2]	0.01		0.3	0.06	0.18	0.012	0.015
Frequency [Hz]	10M		16M	28M	32M	12.77M	10.5M
Power [µW]	85 [a]		220	142	34	56.2	219.8
Energy [pJ/cycle]	8.5 [a]		13.8	5	1.1	4.4	21
Supply range [V]	1.5~1.8		1.6~2	0.85-1.05	1.1~2.3	0.6~1.1	1.4~2.2
Supply sensitivity [ppm/V]	9000		1200	2900	80 [d]	10000	44000
Jitter [ppm]	414		638	196	713	983	104
Allan deviation [ppm]	2.3		0.32	2	2.5	-	2.8
Temp. range [°C]	-45~125		−45~85	−40~85	−40~85	−30~120	-45~125
Packaging	Ceramic	Plastic	Ceramic	-	Plastic	-	-
Max. Freq. error [ppm]	±2800	±3000	±90	±200	±400	±9000 [b]	-
Temp. coefficient [ppm/°C]	31.5 [c]	35.3 [c]	1.3 [c]	2.56 [c]	8.4	31	137
Trimming points	1+batch (1st order)		2+batch (3rd order)	2+batch (5th order)	2	1	0
Number of samples	112	112	20	16	6	4	15

Table 4.1 Comparison table

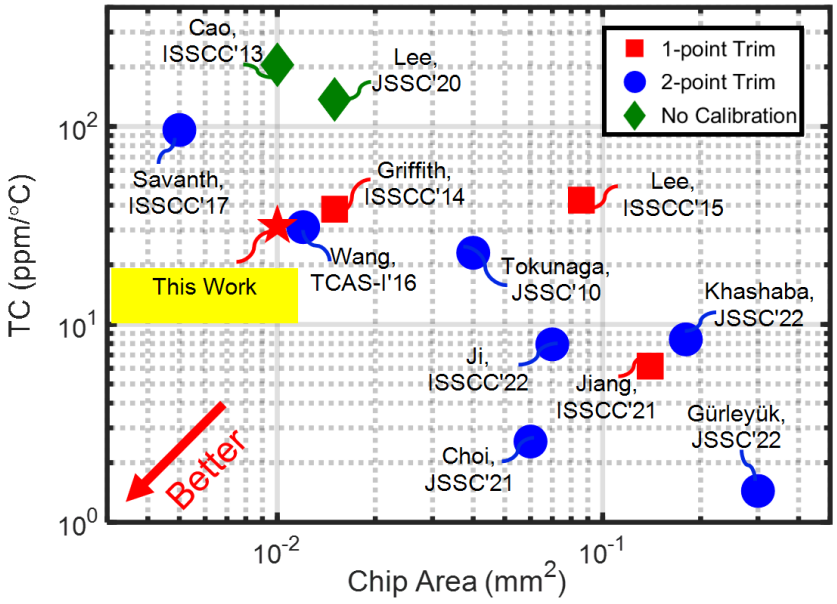

Figure 4.16 Chip area and residual TC among state-of-the-art RC frequency references

Chapter 5 Conclusion and Future work

5.1 Conclusion

This work describes a compact RC frequency reference targeted for WSN applications. Fabricated in a standard 0.18µm technology, the 0.01mm^2 10MHz reference achieves a ±0.28% inaccuracy from −45°C to 125°C after 1-point trim, which represents the state-of-the-art for designs with a similar area. Moreover, the proposed temperature compensation scheme does not require resistors with complementary TCs, which significantly extends its application scope. Besides, this work reports two newly discovered frequency inaccuracy sources from the measurement results: the hysteresis error (0.15%) and the aging error (0.5%).

5.2 Future work

The proposed RC frequency reference uses p-poly resistors due to the high density and the proper TC. However, as discussed in Section 4.2, the frequency drifts by 0.5% after aging mainly because of the instability of the polysilicon resistor. This is a big issue for RC frequency references using polysilicon resistors, especially for those designs whose target inaccuracy is far less than 0.5%.

In the same 180nm technology, for example, replacing the polysilicon resistors with more stable resistors (e.g., diffusion or silicide resistors [18, 21]) might improve the frequency accuracy at the expense of chip area. According to the theoretical analysis in Section 3.1.4.2, the best TC of R_2 can be calculated in equation 3.7. After the polysilicon resistors, the p-diffusion resistors are chosen due to their large sheet resistance and good stability. If R_0 and R_1 are p-diffusion resistors, the TC of R_2 should be 3300ppm/°C to achieve a zero first-order TC for the output frequency. This R_2 can be achieved by combing p-diffusion resistors with silicided p-diffusion resistors or n-well under diffusion resistors.

(A) p-diffusion resistor + silicided p-diffusion resistor

In this example, we use p-diffusion and silicided p-diffusion resistors to construct R_2. To get a zero first-order TC, R_2 is built with a combination of an 81.9kΩ silicided p-diffusion resistor with an 18.1kΩ p-diffusion resistor in TT corner at room temperature. The unit trimming resistors are designed to be 800Ω to cover the process spread. According to the simulation as shown in Figure 5.1 and Figure 5.2, the residual TC is 120ppm/°C from −45°C to 125°C and the power supply sensitivity is 1000ppm/V from 1.5V to 1.8V.

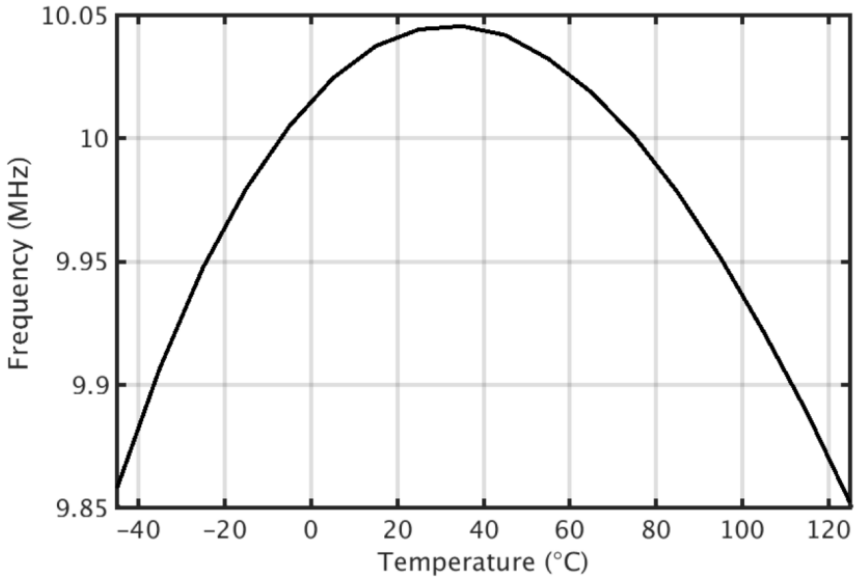

Figure 5.1 Post-simulation results of the temperature sensitivity of the design with p-diffusion and silicided p-diffusion resistors

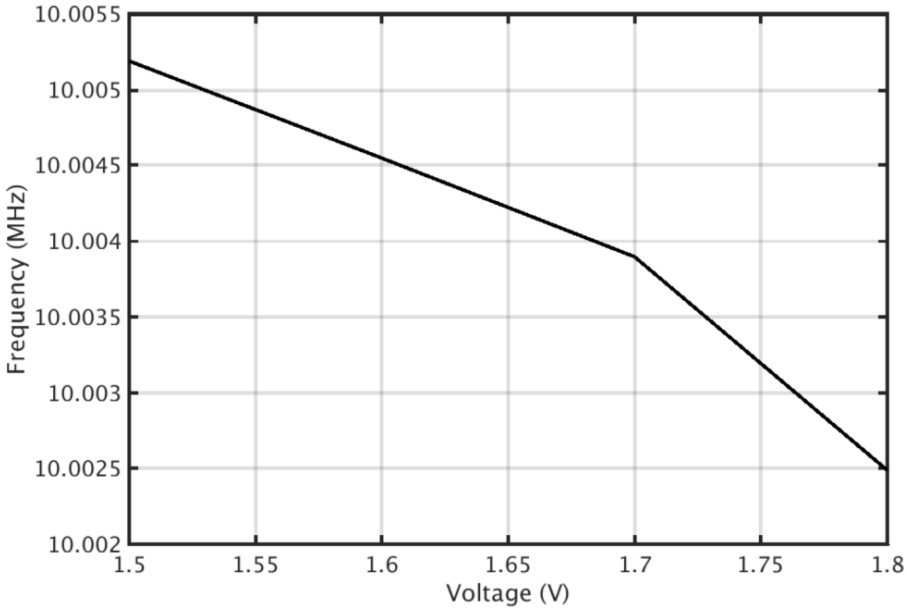

Figure 5.2 Post-simulation results of the voltage sensitivity of the design with p-diffusion and silicided p-diffusion resistors

Figure 5.3 shows the layout of the newly proposed R_2 with p-diffusion and silicided p-diffusion resistors. In this design, vias at the corner of serpentine resistors are removed to reduce the inaccuracy due to the instability of vias, and the missing corners are filled with effective resistance layers. Besides, according to drc rules, silicided p-diffusion resistors are customized with a minimum width of 220nm to save chip area. To ensure the accuracy of the customized resistors, their values are checked with simulations.

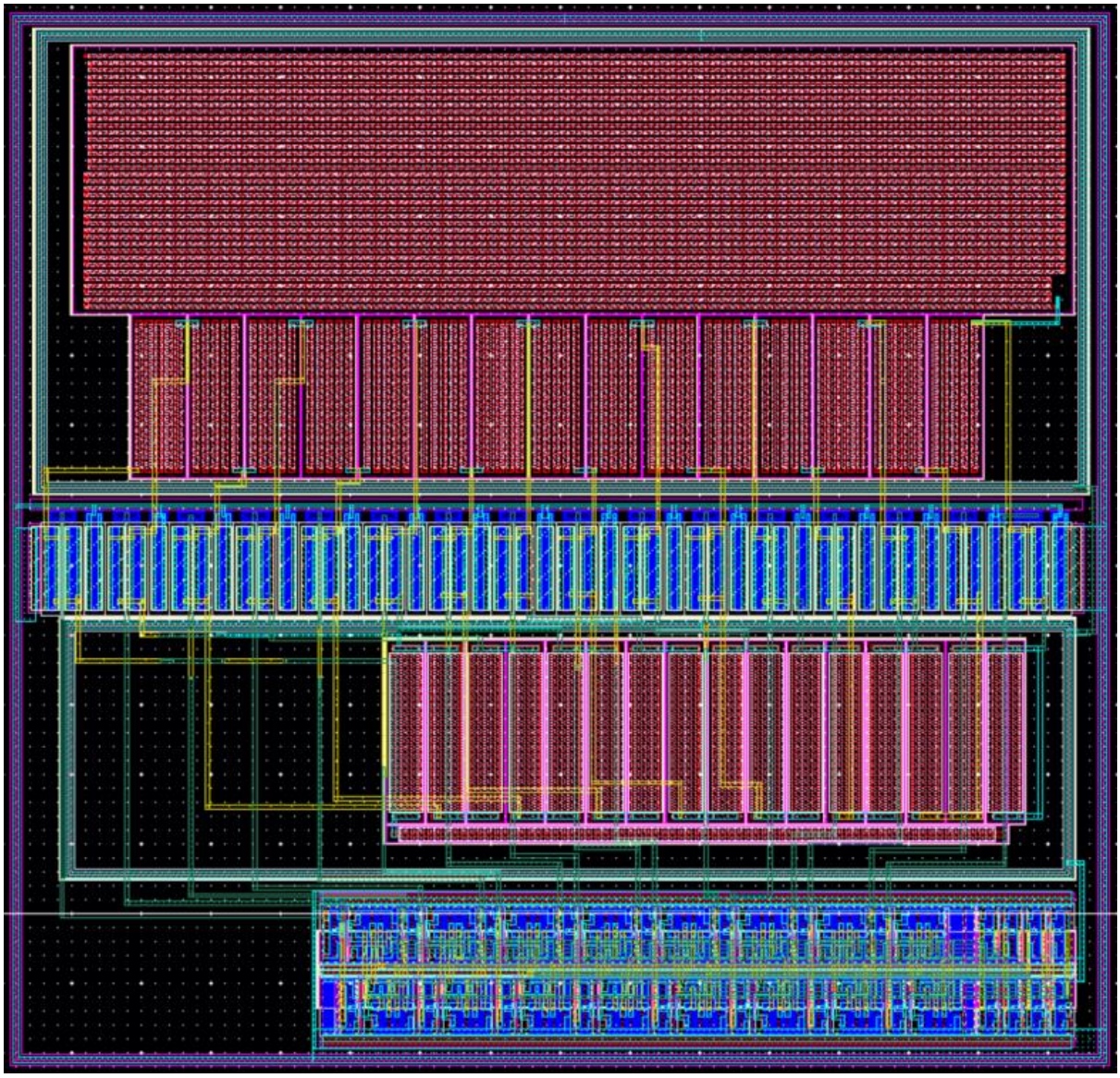

Figure 5.3 New R_2 layout with p-diffusion and silicided p-diffusion resistors

(B) p-diffusion resistor + n-well under diffusion resistor

Similarly, a 75.6kΩ n-well resistor and a 24.4kΩ p-diffusion resistor can be combined to get a 3300ppm/°C R_2. The unit trimming resistors are designed to be 800Ω. According to the simulation in Figure 5.4 and Figure 5.5, the residual TC is 90ppm/°C from −45°C to 125°C and the voltage sensitivity is 2300ppm/V from 1.5V to 1.8V.

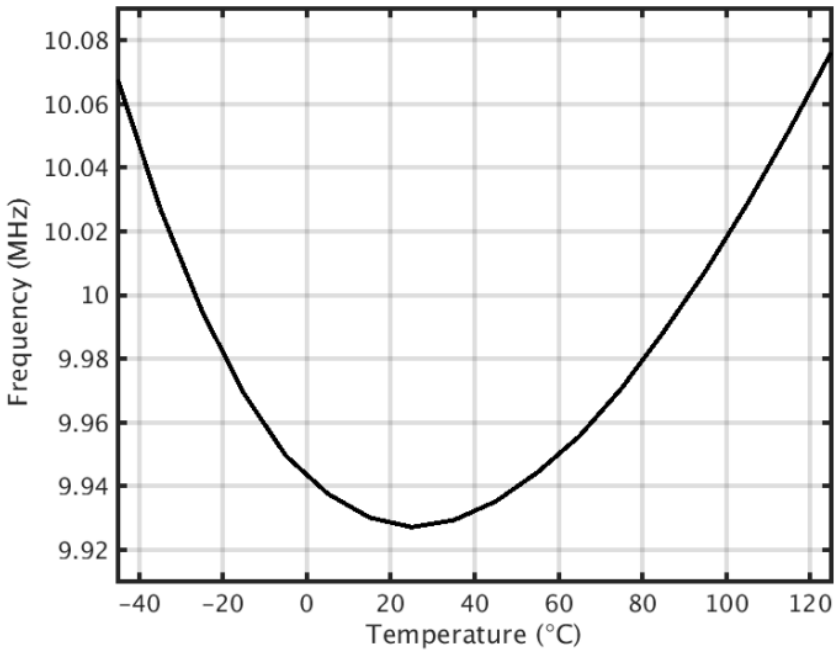

Figure 5.4 Post-simulation results of the temperature sensitivity of the design with p-diffusion and n-well resistors

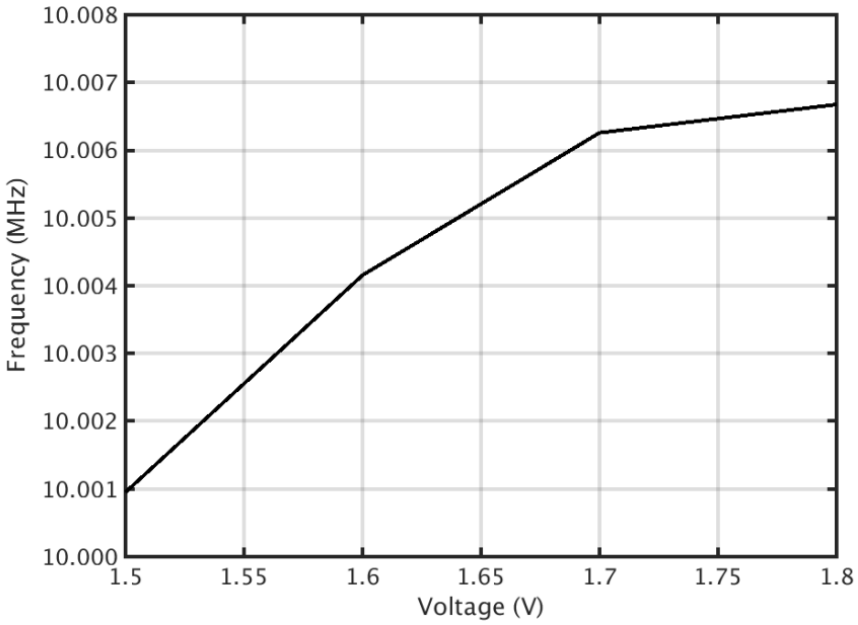

Figure 5.5 Post-simulation results of the voltage sensitivity of the design with p-diffusion and n-well resistors

Figure 5.6 shows the layout of the new proposed R_2 with p-diffusion and n-well under diffusion resistors. Similarly, vias are removed from the serpentine resistors and replaced with effective resistance layers. This layout also improves the circuit's sensitivity to stress, especially for that coming from n-well resistors.

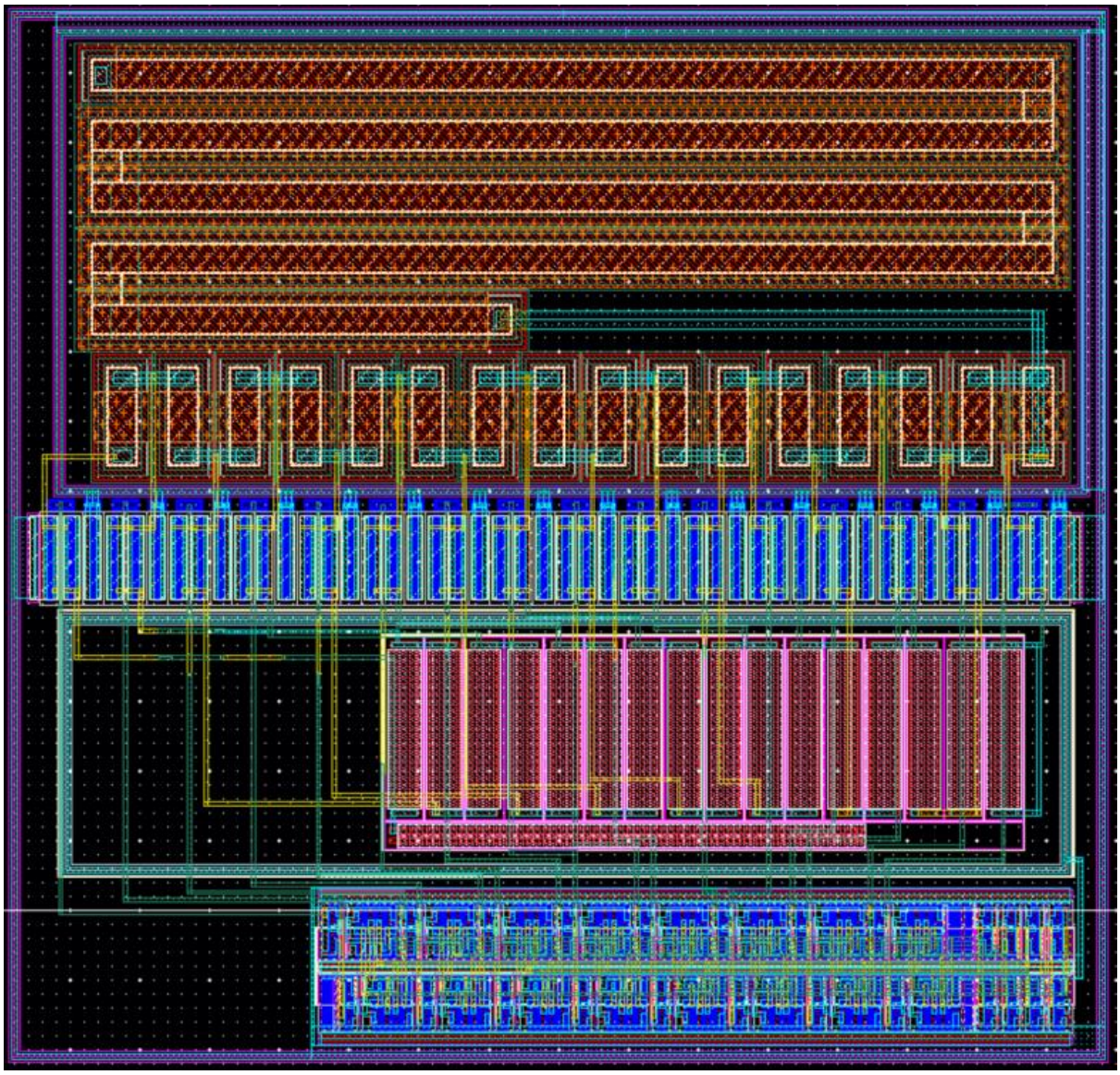

Figure 5.6 New R2 layout with p-diffusion and n-well under diffusion resistors

From the top level of the design, both designs occupy 140µmx104µm chip area. Other performances are expected to be the same as the previous design except for the TC and the supply sensitivity. Table 5.1 summarizes some properties of the three different designs based on the simulation results. Although the second and third designs sacrifice more chip area and result in a larger residual TC due to their high-order TC, they are still worth investigating to determine if the aging inaccuracy can be improved.

The chip, which contains 8 oscillators using p-diffusion and silicided p-diffusion resistors and 8 oscillators using p-diffusion and n-well resistors, was sent to be taped out in September 2022. They will be measured in the future.

	Deisgn 1	Design 2	Design 3
TC Compensation Resistor Type	**p-poly** + n-poly	**p-diffusion** + silicided p-diffusion	**p-diffusion** + n-well under diffusion
Area (mm2)	0.01	0.0145	0.0145
Supply Sensitivity (%/V)	0.21	0.1	0.23
Temp. coefficient (ppm/°C)	29	120	90

Table 5.1 Performance summary of the 3 different designs

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