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# A Chip Integrity Monitor for Evaluating Long-term Encapsulation Performance Within Active Flexible Implants

Omer Can Akgun\*, Kambiz Nanbakhsh\*, Vasiliki Giagka\*<sup>†</sup> and Wouter A. Serdijn\*

\*Section Bioelectronics, Delft University of Technology, the Netherlands

Email: {o.c.akgun, k.nanbakhsh, v.giagka, w.a.serdijn}@tudelft.nl

<sup>†</sup>Technologies for Bioelectronics Group, Fraunhofer Institute for Reliability and Microintegration IZM, Berlin, Germany

**Abstract**—One key obstacle in employing silicon integrated circuits in flexible implants is ensuring a long-term operation of the chip within the wet corrosive environment of the body. For this reason, throughout the years, various biocompatible insulating materials have been proposed, yet, evaluating their long-term encapsulation performance on representative silicon samples still remains to be the main challenge. For this aim, in this work, a sensitive platform is introduced that can track the integrity of the chip against water and ion ingress. This platform is developed to be used for long-term monitoring of chip integrity and study of encapsulation layers in wet environments. The platform comprises a sensing array and a measurement engine and operates by tracking the changes in the inter-layer dielectric resistance within the chip. The proposed system uses a novel charge/discharge-based time-mode resistance sensor that can be implemented using simple yet highly robust circuitry. The sensor array is implemented together with the measurement engine in a standard  $0.18\ \mu\text{m}$  6-metal CMOS process. For chip validation, dry and wet measurements in saline are presented in this paper.

**Index Terms**—Chip integrity, flexible implants, encapsulation, charge-discharge, time-mode operation, monitoring, reliability.

## I. INTRODUCTION

For years, active medical implants have relied on titanium cases for protecting the inside components against the fluidic environment of the body. Despite their long-term reliability, these implants end up having large volumes, are heavy, and unlike biological tissue, are stiff and rigid. For this reason, a great deal of research has been dedicated to replacing the bulky titanium cases with flexible polymers and thin-film coating layers [1], [2]. Recently, these efforts have been further endorsed by the new field of bioelectronic medicine, in which small, flexible, and lightweight implants are needed for targeting the delicate nerve structures within the body [3]. In previous work, we have shown an active electrode array for epidural spinal cord stimulation in which silicone rubber was used for the packaging of the miniature integrated circuits (ICs) [4]. In [5], a millimeter scale wireless peripheral nerve stimulator has been reported where parylene, as a thin biocompatible polymer, has been used for the final packaging of the chip and the piezoelectric crystal. Such approaches add minimal overhead to the volume and weight of the device, and have a number of additional physical and mechanical advantages. Nevertheless, the coating performance of these biocompatible layers still has to be evaluated on representative material surfaces and in wet environments to justify their use for pre-clinical or clinical applications.

In wet ionic environments, failure of electronics can occur due to water molecule and ion ingress through the protective layers (due to imperfections, defects, pinholes, etc), first causing parameter changes in the passive (capacitance/resistance) and active (MOS transistor) components, and later causing shorts and/or hard opens [1], [6], [7]. For polymer encapsulated single-chip implants, the ingress of water and ions could initiate from

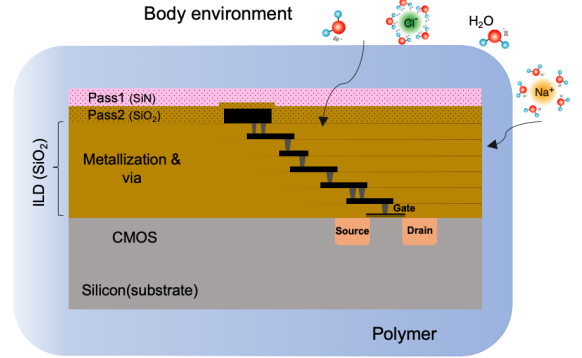


Figure 1. Illustration of the two pathways for water and ion ingress in the silicon die (dimensions not to scale).

the top passivation and/or the edges of the chip (Fig. 1). Given the micro/sub-micrometer scale of components inside the chip, even tiny amounts of water or ions could lead to performance loss or total device failure [1], [7]. For this reason, a sensitive on-chip platform is needed to evaluate the long-term encapsulation performance of the coating materials in wet ionic environments. In [8] the advantages of an in situ sensing system was highlighted and a circuit was proposed to detect water infiltration from the edges of the silicon die.

In this work we present the implementation of an in situ sensing array that can detect leakage pathways through the top and edges of the chip and track the propagation of the leakage in realtime. The employed sensing method is based on tracking the resistance change in the inter-layer dielectrics (ILD) between successive metal layers in the chip. The platform can track the resistance change throughout the  $234 \times 23$  sensor array and at different depths of the chip. Time-mode operation [9] is used, where a pulse-width carries the measurement information, and time measurements are used to detect the changes in the ILD with a tuneable measurement range and measurement accuracy.

The organization of this paper is as follows: the top-level overview of the proposed time-mode resistance measurement system and measurement concept is introduced in Sec.II. The design of the sensor pixel is presented in Sec.III. Chip implementation and measurement results are given in Sec.IV, and finally, conclusions are drawn in Sec.V.

## II. RESISTANCE MEASUREMENT SYSTEM

### A. System Level Implementation

The proposed whole-chip measurement system is implemented as a sensor pixel array as shown in Fig. 2. The array consists of 234 rows and 23 columns. To measure each pixel's value, a fully-digital measurement engine that can automatically check all the cells for integrity and degradation within the  $\text{SiO}_2$  ILD is implemented. *Row enable* enables a row of pixels for sensing,

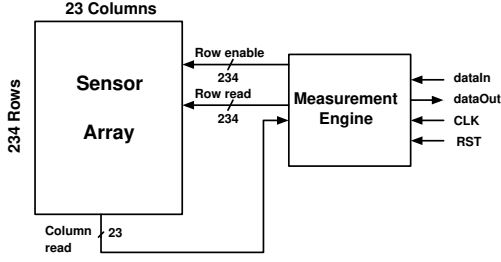


Figure 2. Implemented sensor array with on-chip measurement engine showing top-level signals.

and *Row read* enables the output of the chosen row's pixels. Then all columns are read by the measurement engine (*Column read*) and further processed.

A serial-in, serial-out architecture is used to minimize the number of bonding pads (6 in total) to ease the handling of the device during testing in wet environments. The clock (*CLK*) and reset (*RST*) signals together with the data-input port (*dataIn*) are used for controlling the measurement engine externally, and the output is sent off-chip through *dataOut*. As it will be shown in Sec.IV-A, it is possible to change both the accuracy and maximum resistance measurement capability of the system by changing the clock frequency, hence adapting the system for different measurement conditions.

### B. Measurement principle

The proposed measurement method employed in each pixel is based on charging a node, leaving that node floating to discharge and measuring the discharge time. A simple model of the method is shown in Fig. 3(a). In the figure, **n1** is the node that is charged and then left floating when the switch opens,  $R_{ox}$  is the resistance of the ILD oxide, representing the irregularities in the oxide structure that is intended to be monitored,  $C_{ox}$  is the oxide capacitance between the floating node and the ground plane, and  $R_{shunt}$  represents all the other shunt resistance elements connected to **n1**. As the model in Fig. 3(a) shows, a familiar parallel RC circuit is created once the switch opens. The charge on the capacitor will discharge through the resistors as shown in Fig. 3(b). The voltage at **n1** is  $V_{DD}$  just before the switch opens, and after the switch opens, at time  $t$ , it is given by

$$V_{n1}(t) = V_{DD} \cdot e^{-t/R_{eq}C_{eq}} \quad (1)$$

where  $R_{eq} = R_{ox} \parallel R_{shunt}$  and  $C_{eq}$  is the combination of all the capacitances to ground at node **n1**. By measuring the time it takes for node **n1** to be discharged to a specific value, in our case  $V_{DD}/2$ , the RC time constant between **n1** and ground may be measured with a very high accuracy. For a target discharge threshold of  $V_{DD}/2$ , the discharge time and the RC time constant at **n1** are given by

$$T_{discharge} = \ln(2) \cdot R_{eq}C_{eq} \quad (2)$$

$$R_{eq}C_{eq} = \frac{T_{discharge}}{\ln(2)} \quad (3)$$

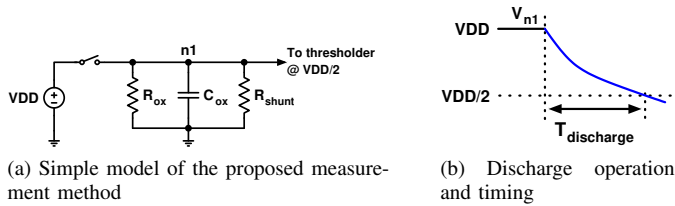


Figure 3. Proposed ultra-high resistance measurement method.

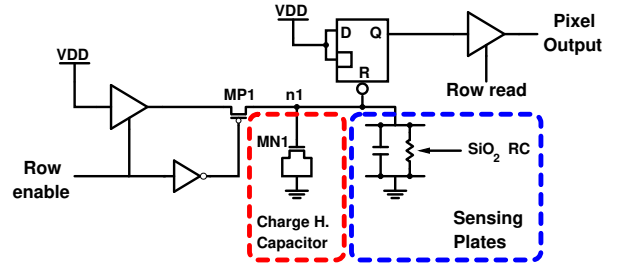


Figure 4. Schematic of the unit measurement pixel. The charge holding capacitor and the sensing plates for measuring oxide degradation are marked.

### III. SENSOR PIXEL CIRCUIT DESIGN

The concept presented in the previous section has been designed and implemented in a  $0.18 \mu m$  standard CMOS process with 6 metal layers. The novel resistance sensor used in each pixel is presented in Fig. 4. The implemented pixel uses logic gates from the standard cell library, and consists of 3-state buffers, an inverter, a D-latch with active-low reset, a MOSCAP (MN1), which is used for charge holding and reducing the effect of parasitic capacitances and capacitance variation at **n1** due to process mismatch, a high-threshold PMOS transistor (MP1) to reduce the current leakage path through the 3-state buffer, and sensing plates to sense the change in the oxide over the pixel.

*Sensor element:* two successive metal layers are used as the sensing plates to monitor the changes in the properties of the oxide over the pixel (Fig. 5). The top plate of the sensing structure is connected to node **n1** and the bottom plate is connected to ground. In the presented implementation, there are three different versions of the sensor pixel shown previously in Fig. 4, with different metal layer pairs, namely M6-M5, M5-M4, and M4-M3. Taking into account the probability of failure over a cell area being uniform, we calculated that, to be able to capture the change in the oxide with maximum probability, the upper plate area should be half of the area of the bottom plate, and to realize such a structure with regularity, we opted for the design in Fig. 5. In the layout of the sensor array, cells with different sensor capacitors are placed alternately, e.g., an M6-M5 cell is followed by an M5-M4 cell, which is followed by an M4-M3 cell, both in the x and y directions. In the extracted layout, it was seen that the capacitance at **n1** varies between 23.5 and 24.5 fF (17.5 fF from the MOSCAP), depending on the used metal layers. Furthermore, different metal combinations give us the ability to track the changes at different depths of the ILD.

*Operation:* the operation of the pixel is shown in Fig. 6 and is as follows: when a sensor pixel is to be measured, the *Row enable* signal for the chosen pixel row is raised for a clock cycle. During this cycle, the input 3-state buffer and the high-threshold PMOS transistor MP1 are turned on, charging node **n1** to  $V_{DD}$ . The node charge is stored on the MOSCAP, the  $SiO_2$  capacitance of the sensing plates, and the parasitic capacitances at **n1**. An NMOS MOSCAP is used as the main charge holding element to reduce the effects of pixel-to-pixel variation due to process mismatch by increasing the node capacitance. As soon as node **n1** is charged, the output of the latch is automatically set to

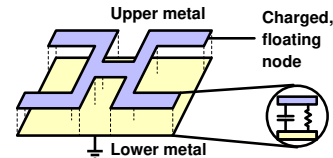


Figure 5. Capacitor structure for sensing the changes in the  $SiO_2$  between the metal plates.

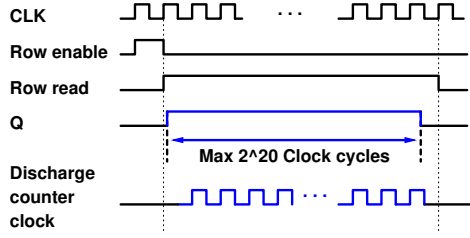


Figure 6. Timing of the measurement pixel operation.

VDD, as both the D input and enable signals of the latch are connected to VDD. In the next clock cycle two things happen: i) *Row enable* is lowered, stopping the charging process, turning off both MP1 and the input 3-state buffer, and leaving node *n1* floating, and ii) *Row read* is raised to read the pixel output at the column output.

During operation, the measurement engine in Fig. 2 selects both the row and the column to be measured. Therefore, as soon as the pixel output is enabled and raised (the Q output of the latch is already at VDD), the 20-bit counter in the measurement engine starts counting with *CLK*. The count stops when either node *n1* is discharged below the reset threshold ( $VDD/2$ ) of the latch, effectively resetting the latch (Q goes low), or a count of  $2^{20} - 1$  is reached. Thus, time-mode time constant measurement is realized.

**Measurement process:** the self-reset process of the latch in Fig. 4 for realizing oxide change measurement is as follows. When node *n1* is left floating, the possible discharge paths are through the oxide resistance of the ILD and the added shunt resistance connected to this node, which consists of the following elements: the current leakage path through MP1 and output of the 3-state buffer, the gate leakage through the latch, and the gate leakage of MN1. It is assumed that in the presence of water or ions in the ILD layer, the dominant discharge path for *n1* will be through the ILD oxide. Therefore, we use the variation in the discharge time of node *n1* to track the changes in the resistance and capacitance of the  $SiO_2$  layer between any two metal layers that act as our sensing plates (Fig. 5). Finally, we convert the time it takes *n1* to discharge to  $VDD/2$  to a time count and calculate the measured resistance using this time count.

In the absence of water molecules and ions in the ILD  $SiO_2$  layer between two successive metals, the resistance of the ILD will be very high (in the order of  $10^{15}$  ohms). At this point, the dominating resistance at node *n1* will be mainly from the gate leakage of MN1. However, as the chip integrity is breached and water molecules and ions penetrate the ILD layers, there will be multiple changes but mainly: i) the conductance of the ILD  $SiO_2$  that has been breached will increase (i.e., the resistance will reduce), and ii) due to the presence of water molecules and ions, the dielectric constant of the  $SiO_2$  will increase, hence increasing the capacitance of the layer. In such a case, if we monitor a lower discharge time count, we can conclude that the reduction in the resistance is higher than the increase in the capacitance. Moreover, we expect the discharge time of *n1* to be reduced in proportion to the reduced resistance (representing the amount of ions and molecules in the oxide).

#### IV. CHIP IMPLEMENTATION AND MEASUREMENT RESULTS

A prototype system containing the sensor array and the measurement engine core is implemented in a  $0.18\mu m$  standard CMOS process. Fig. 7(a) shows the implemented chip together with the polydimethylsiloxane (PDMS) covering the pads and wire bonds. For proof of concept, in this paper, all the dry and wet measurements are done with bare dies where the top passivation is the only insulating layer. For this aim, PDMS is only applied over the pads and wire bonds leaving the sensor array fully exposed. Chip area including the bonding pads is  $1.1\text{ mm} \times$

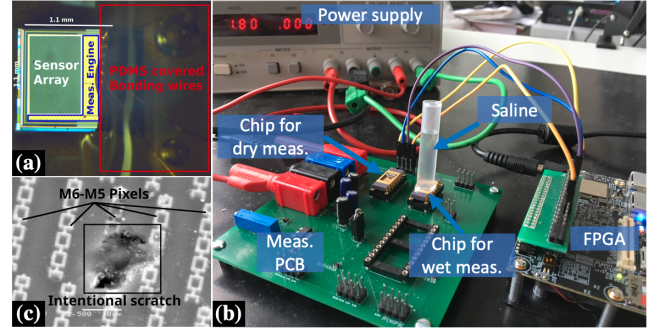


Figure 7. (a) Chip photo showing the sensor array, measurement engine, and polydimethylsiloxane (PDMS) covered bonding wires. (b) Measurement set-up showing the custom designed PCB used for both dry and wet measurements. (c) SEM image illustrating the intentional scratched passivation surface of the chip. Pixels with M6-M5 sensor plates are marked.

$1.1\text{ mm}$ . The sensor array consists of 5382 sensor pixels, with varying metal sensor plate structures, as explained previously. The size of each pixel is  $3.92\mu m$  by  $29.68\mu m$ , hence giving the same resolutions in the y and x directions, respectively.

The test setup consists of a custom-designed PCB, a power supply and an FPGA board to control the on-chip measurement engine and to save and process the data from the chip (Fig. 7(b)). The custom PCB accommodates three packaged chips at the same time for parallel measurements. In the photo, a setup for both dry and wet measurements is shown.

##### A. Dry measurements

To verify the correct operation of the system and determine the measurement capabilities, the first measurements are done in dry conditions. For each chip, dry measurement results are also used as a reference for comparing to wet measurements. The external clock frequency for the measurement engine is adjustable from 75 MHz down to 125 kHz. The clock frequency will allow for measurement of the discharge time with differing accuracy and maximum resistance limits. For example, for a clock frequency of 50 MHz, the minimum discharge time-step that can be measured is 20 ns. Using Eq. (3), and an average value of 24 fF for  $C_{eq}$ , it can be calculated that the minimum measurable resistance change is  $1.2\text{ M}\Omega$ . Any changes greater than  $1.2\text{ M}\Omega$  will be captured by the system as a reduction in the discharge counter, with a maximum measurable value of  $1.26\text{ T}\Omega$ . To increase the

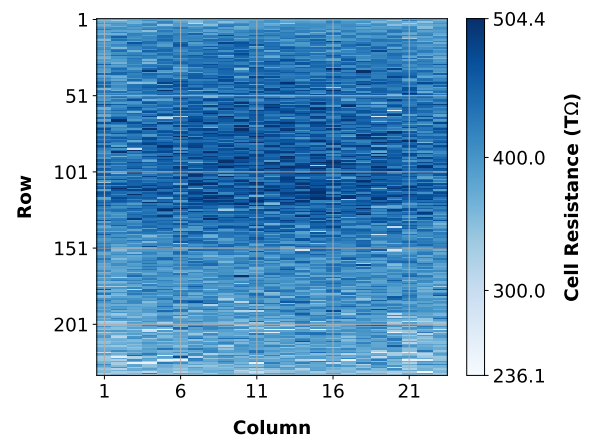


Figure 8. Dry measurement results for the whole sensor array. Calculated resistance varies between  $0.236\text{ P}\Omega$  and  $0.504\text{ P}\Omega$  due to intra-die process variation.



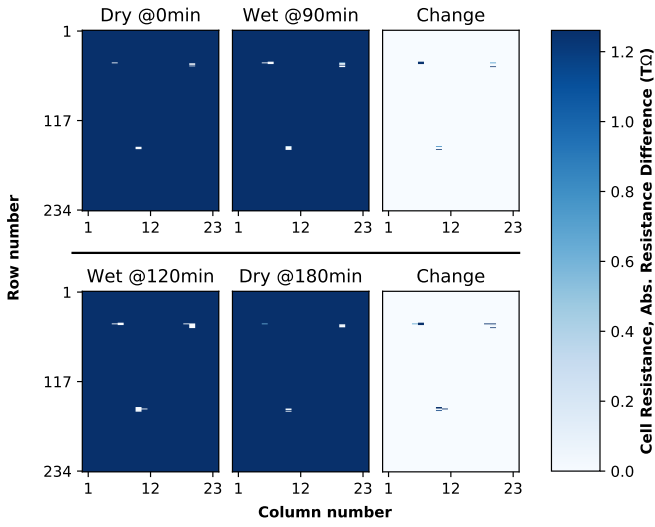


Figure 9. Dry, wet, and re-dried measurement results for a chip with scratched passivation showing how water/ion ingress through the scratched area can change the resistance in neighboring pixels.

measurement range, the external clock can be reduced to a lower frequency, e.g., 125 kHz, where the maximum measurable resistance becomes 0.504 peta-ohm [ $0.504 \cdot 10^{15} \Omega$ ]. During our measurements we found out that a 125 kHz clock is sufficient to set the upper range of the measurement, as resistance values higher than 0.504 peta-ohm in the ILD oxide are not measurable due to the shunt current leakage paths ( $R_{shunt}$ ) in each pixel. The shunt current leakage path in each pixel is dominated by the gate-leakage of the MOSCAP transistor, and our measurements are in agreement with our expected gate-leakage calculations and the results that have been previously published [10]. To measure all the pixels with a 125 kHz clock, approximately 12.5 hours is needed. Results of such a measurement are presented in Fig. 8, showing the measurement capabilities of the implemented platform.

### B. Wet measurements

Wet measurements were performed to verify the capabilities of the implemented platform in tracking water/ion ingress through the ILD stacks. Our earlier wet experiments after two weeks of continuous soaking in saline showed no changes in the array when compared to dry measurements. This suggests the good insulating properties of the chip passivation provided by the foundry. Therefore, in this paper, to test the functionality of the proposed circuit in a controlled environment, three scratches were intentionally introduced on the chip passivation surface using an ultrasonic cutter. This would allow faster propagation of water/ions in the chip ILD layer. A SEM image of one such scratch is shown in Fig. 7(c).

After scratching the surface of the chip, measurements under different conditions were made. First, a dry measurement of the chip was done. Fig. 9 shows the results of this measurement where the scratched areas on the chip are seen as lighter colour pixels compared to the rest of the array. The lighter colours indicate a faster discharge time and could be due to an introduced damage in the top metal when scratching the passivation surface. In these measurements a clock of 50 MHz was chosen to increase the accuracy of the measurement as explained previously. Second, we tested the chip in a phosphate-buffered saline (PBS) solution with a pH of 7.4. The solution was kept on the sensor array using a tube (Fig. 7(b)). Results of the measurement after soaking the chip in the solution for 90 minutes, and the difference between the dry and wet measurements are shown in the middle and

right panes of the top row of Fig. 9, respectively. The third group of measurements were taken to verify both the effects of continuous exposure to liquids and change in the properties of the oxide due to water/ion penetration: i) at 120 minutes after soaking the chip (bottom left figure), and ii) after drying the chip surface and letting it stay dry for 60 minutes (180 minutes after the beginning of the measurements, bottom middle figure). Again, the difference between the wet and dried measurements is presented at the bottom right figure. The results in Fig. 9 show the monitoring capabilities of the chip in detecting changes in the ILD resistance as water/ions propagate in the chip structure over time, both through the damaged and undamaged neighboring cells. All the measurements were done while the chip was supplied by a 1.8 V voltage source and the average current consumption during the measurements was 4.78 mA, which also includes the consumption of the ESD protection circuitry.

### V. CONCLUSIONS

A fully integrated, standard-CMOS, chip integrity monitor has been presented. The implemented chip utilizes novel charge/discharge-based, time-mode pixels that monitor the changes in the sensing element's oxide through ultra-high resistance measurements. The sensor array is implemented together with a digital measurement engine that continuously monitors the sensor readings. The system can measure resistance values up to 0.5 peta-ohm, with controllable measurement steps that can be as low as 1.2 M $\Omega$ .

### ACKNOWLEDGMENT

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