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9.9 A 0.6nm Resolution 19.8mW Eddy-Current Displacement Sensor Interface with 126MHz Excitation

Vikram Chaturvedi[1], Mohammad Reza Nabavi[2], Johan Vogel[1], Kofi A. A. Makinwa[1], Stoyan Nihtianov[1]

[1]Delft University of Technology, Delft, The Netherlands
[2]Catena Microelectronics, Delft, The Netherlands

Displacement sensing with sub-nanometer resolution is required in advanced metrology and high-tech industry, e.g., to measure the lens position in wafer scanners. Linear encoders and interferometers are often used for this purpose, but they are bulky and costly. Capacitive sensors [1], though compact, are sensitive to environment and require electrical access to the target. Eddy-current sensors (ECSs) do not have these disadvantages, but their resolution and stability are limited by the skin-effect [2-5]. For sub-nm measurements, this can be alleviated by using excitation frequencies >100MHz. This calls for stable flat sensing coils (to minimize parasitics) in close proximity to the ECS interface, whose power dissipation must then be low enough to avoid self-heating and displacement errors due to thermal expansion [2,6].

Mechanical assembly tolerances pose another challenge for ECSs. Although sub-nm resolution must be achieved over a typical range of only a few micrometers, the stand-off distance X_{so} to the target is often hundreds of micrometers. This results in sensor offset, which exacerbates the dynamic range (DR) and linearity requirements on the ECS interface. Hence, this sensor offset, proportional to X_{so}, must be cancelled before its amplification. Another challenge is the excitation oscillator's noise and drift. Although this can be suppressed by ratiometric techniques, its efficacy is limited by any non-linearity, e.g., due to G_m stages, in the signal chain [2,4].

In this work, we present an ECS interface with 0.6nm resolution, 2kHz BW and a 126MHz excitation frequency (f_{exc}). It is based on an oscillator that excites both a shielded reference coil, as well as a sensor coil whose inductance is modulated by the displacement of a nearby copper target. To obtain power-efficient and linear (>70dB) demodulation of coil voltages, capacitors are used as linear voltage-to-current converters, obviating the need for G_m stages [2,4]. Furthermore, the anti-phase relationship between the sensor and reference coil voltages is exploited to cancel sensor offset. The interface consumes 11mA from a 1.8V supply, including 2.2mA consumed by two output buffers.

The architecture of the 2-channel ECS interface is shown in Fig. 9.9.1. Its front-end consists of a cross-coupled oscillator, which excites a reference coil L_{ref} and a sensor coil $L_{sen} = L_{ref} \pm \Delta L(x)$. The amplitude of the oscillator outputs V_{sen} and V_{ref} is then directly proportional to L_{sen} and L_{ref}, respectively. To mitigate sensor offset ($\propto L_{ref}, X_{so}$), these are converted to currents by capacitors C_{in}=C_{drr}=500fF, demodulated by mixer M_{ix1} and summed at the virtual ground of a transimpedance amplifier (TIA) $G_{m,sen}$. This causes the effective input current of M_{ix1} to be proportional to $\pm\Delta L(x)$, rather than $L_{ref} \pm \Delta L(x)$. Smaller currents through down-conversion mixers also reduce their noise contribution. Mixers are sized to add parasitic capacitance of only 50fF, which degrades noise of TIA by 10%. To enable a ratiometric computation of displacement [2], V_{ref} is demodulated by a reference channel, consisting of C_{ref} (=β.C_{in}), M_{ix0} and TIA $G_{m,ref}$. The scale factor β corresponds to the desired measurement range X_{max}, i.e., β= X_{max}/X_{so}=1/10. The mixer's synchronous clock f_{mix} (=f_{exc}) is generated by a continuous-time current comparator whose virtual ground is driven by the oscillator output via capacitor C_{comp} (=200fF). At f_{exc}=126 MHz, the comparator's ~0.4ns delay causes ~5% signal attenuation. Due to their high-frequency operation, the charge injection of mixers M_{ix1} and M_{ix0} would cause significant residual offset. This is mitigated by a nested-chopping scheme operating at f_{mix}/4096. The output of the two TIAs is buffered and then digitized by off-chip ADCs.

Figure 9.9.2 depicts the sensor's signal path in more detail. Anti-phase currents I_{sen} and I_{ref}, are summed at TIA's virtual ground, to cancel sensor offset and generate the current I_{mix}. This current is then converted by R_f (=50kΩ) into an output voltage $V_{o,sen}$. Although the use of a differential signal path reduces charge-injection errors, its unbalanced inputs lead to large common-mode (CM) signals at 2*f_{mix}. These are suppressed by common-mode feedback (CMFB) circuitry and capacitor C_s. To ensure a clean virtual ground, TIA's OTA is designed for >110dB DC gain and >1GHz GBW ($\approx$ 8*f_{mix}) with a 1pF capacitive load. The OTA consists of a 2-stage Miller-compensated amplifier. To achieve sufficient gain at such high frequencies, auxiliary (gain-boosting) amplifiers of both PMOS and NMOS cascodes are also realized as 2-stage amplifiers. Together with the 1st stage, these are chopped to mitigate their offset and low-frequency noise. Chopping clock f_{chop} is synchronized to f_{mix} to obviate down-conversion of spectrum around higher harmonics of f_{mix}. As shown in Fig. 9.9.7, the ECS interface occupies 1.18mm^2 in TSMC 0.18μm CMOS technology.

Figure 9.9.3 depicts the structure of the PCB-based sensor that was used to characterize the ECS interface. It consists of two flat coils implemented in the top and bottom layer of a custom 4-layer PCB. Each coil consists of four, 35μm thick, turns with a 200μm pitch and an 8mm outer diameter. The coils are shielded from each other by two ground planes. Their distance to the moving and reference targets is established by a number of 10μm stainless-steel spacers (placed 3mm away from the coils so as not to affect their sensitivity). With a copper target and X_{so} = 105μm, the total inductance of L_{ref} is ~100nH (including PCB trace parasitic inductance of ~20nH).

Figure 9.9.4 shows the measured transfer characteristic of the ECS interface and the PCB-based sensor, where $D_{out} = V_{o,sen}/V_{o,ref} \approx \Delta L(x)/(\beta.L_{ref})$. The zero-crossing around the nominal X_{so}=105μm shows that sensor offset is indeed compensated by the ECS interface. The deviation of zero-crossing from X_{so}=105μm is due to small mismatch (~3nH) between L_{sen} and L_{ref}. The limited voltage output range of TIA manifests itself as the desensitization of D_{out} at larger displacements. Measured FFTs of two output voltages and D_{out} are shown in Fig. 9.9.5, with ΔX =10μm. The suppression of oscillator's low-frequency amplitude noise due to ratiometric readout is clearly noticeable. In a 2kHz BW, the calculated SNR is 86.6dB, which corresponds to a resolution of 14.1b over X_{max} (=10μm), i.e., a resolution of 0.6nm. With β = 0.1, this translates into an overall system resolution of 17.4b (β=X_{max}/X_{so}) for a linear sensor. Using an LNA (SR560) and a low-noise spectrum analyzer (HP4395A), the reference channel's output noise floor was found to be 136nV/√Hz. This would translate into a 92.9dB SNR if all of oscillator's amplitude-noise is suppressed by the ratiometric readout. In practice, it is slightly less because the demodulator's finite input impedance allows some of this noise to escape from the LC tank. This residual low-frequency noise can also be observed in Fig. 9.9.5.

Figure 9.9.6 summarizes the performance of the ECS interface and compares it to the state of the art. By increasing f_{exc} and cancelling sensor offset, it achieves sub-nanometer displacement-resolution. Despite its higher f_{exc}, larger signal bandwidth and implementation in a deep sub-micron CMOS process, it dissipates similar power. Furthermore, it achieves an inductance resolution of 0.58 pH which outperforms that of precision LCR meters [7].

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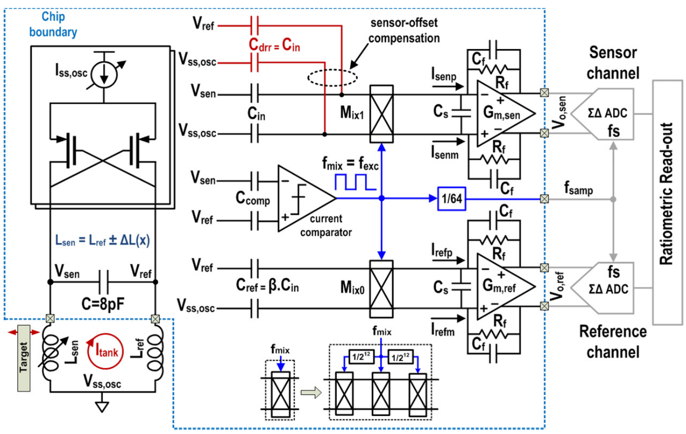

Figure 9.9.1: Architecture of the eddy-current-sensor interface.

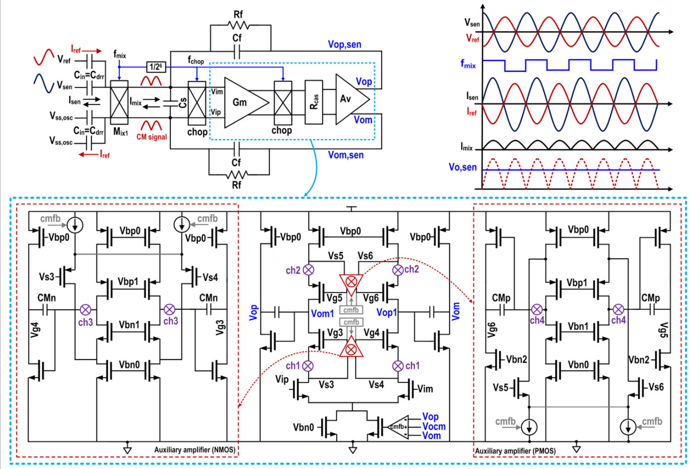

Figure 9.9.2: Sensor channel with standoff offset cancellation.

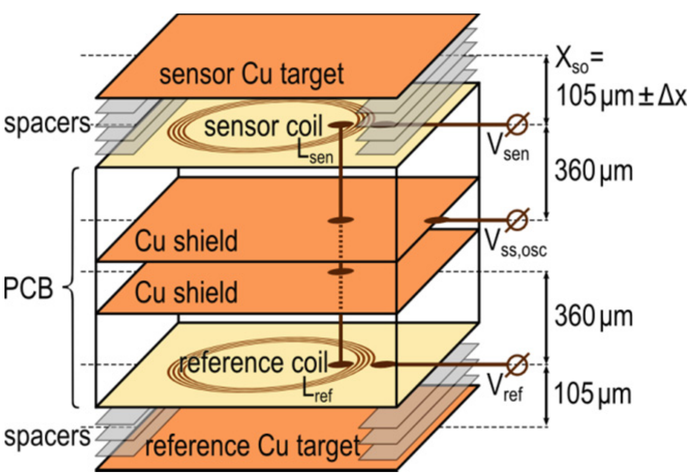

Figure 9.9.3: Stacked flat-coils in 4-layer PCB used as the sensor.

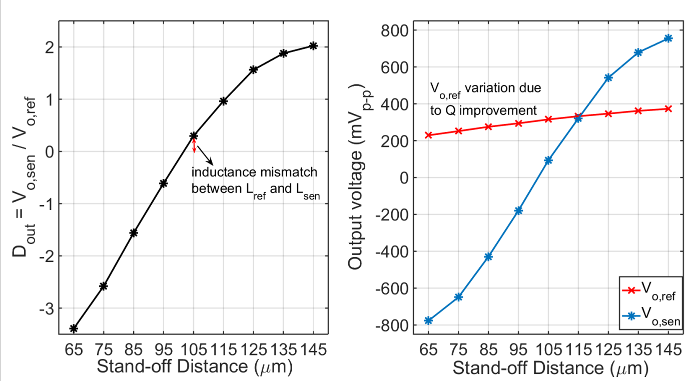

Figure 9.9.4: Measured transfer characteristics of the ECS interface.

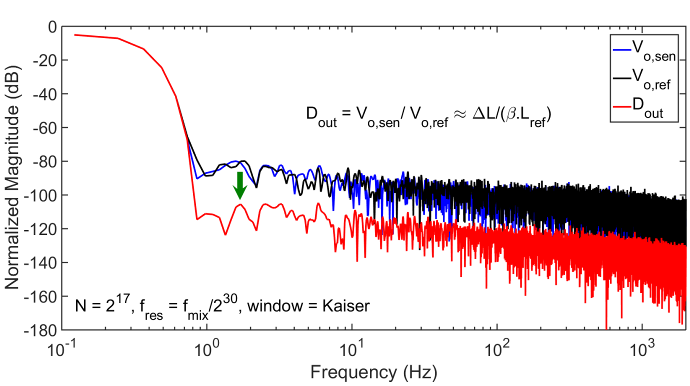

Figure 9.9.5: Measured FFT of output voltages and D_{out}. X_{so} = 115µm.

	This work	[2]	[3]	[4]	[5]	[6]
Stand-off Distance	**105 µm**	3 mm	Sub-mm to tens of mm	3 mm	Sub-mm to tens of mm	3 mm
Sensor Excitation Frequency (Hz)	**126M**	20M	1M	15M	1M	312.5k
Displacement resolution (nm) (Inductance resolution (pH))	**0.6 (0.58)**	65 (1.5)	-	135 (3.8)	-	2930(-)
Bandwidth (Hz)	**2k**	1k	1k	1k	1k	10k
Resolution (bit)	**14.1 (ENOB)***	15.5 (ENOB)	20	15	~ 14	10
Power consumption excl. ADC# (mW)	**19.8**	18	375	18	2500	7.3
Technology	**0.18 µm CMOS**	0.35 µm BICMOS	-	0.35 µm BICMOS	-	0.6 µm CMOS

An on-chip ADC will only reduce power consumption as output buffers (2.2 mA current consumption) will not be required then. The power consumption of an output ADC against that of ECS interfaces is negligible.

* Calculated over the useful displacement range X_{max} = 10 µm. For a linear sensor, this corresponds to 17.4 bits of system resolution, with β = 0.1.

Figure 9.9.6: Performance comparison with state-of-the-art works.

9

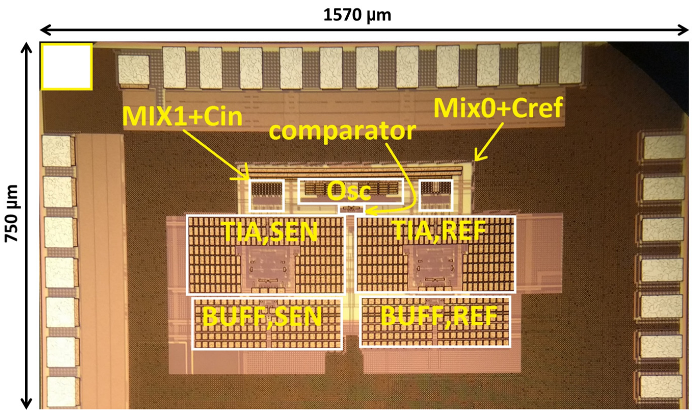

Figure 9.9.7: Die micrograph of the ECS interface.

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