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***Abstract*—This paper proposes a novel sensorless phase-shift modulation-based voltage balancing technique for a 5-level Packed U-Cell (PUC5) inverter. Two phase-shifted triangular carriers are used to modulate the reference signal and generate the appropriate gate pulses. The switching pulse generation is specifically designed to charge and discharge the capacitor at the speed of switching frequency, resulting in a fast voltage balancing of the auxiliary capacitor. Compared with the reported level-shifted modulation method, the proposed technique simplifies comparators and logic gates while keeping the benefit of fast sensorless voltage balancing and, consequently, the capacitor size reduction. In other words, it modifies the reference signal to achieve the fast voltage balancing of the auxiliary capacitor in PUC5. Simulation results are shown to investigate the effectiveness of the proposed technique.**

***Index Terms*—multilevel inverter, 5-level packed U-cell (PUC5), sensorless voltage balancing.**

I. Introduction

Multilevel Inverters (MLI) are widely used in industries for higher power applications due to low harmonic pollution and high efficiency [1]. Therefore, they are widely utilized in energy conversion systems to enhance inverter efficiency and to realize the electrification of industrial processes and low-pollution, low-carbon-emission clean energy transition [2–8]. Among MLI topologies, Cascaded H-bridge (CHB), Neutral Point Clamped (NPC), and PUC5 are popular choices. Furthermore, the intricacy of control and modulation techniques for classic MLIs is significantly heightened with an increased number of voltage levels [9–11].

PUC5 inverter has many merits, including low complexity, modularity & scalability, two redundant switching states to increase flexibility, and inherently regulate the auxiliary capacitor's voltage at half of the DC voltage. The classic PUC5 inverter is introduced in [12–14]. It regulates the capacitor voltage level at half of the DC voltage using the sensorless voltage balancing technique. However, this control method necessitates four level-shifted (LS) triangular carriers. Besides, a switching states table is needed to generate switching signals. Additionally, one of the most important drawbacks of the PUC5 inverter with sensorless voltage balancing is that the output voltage ripple can not be ignored, which requires a matching large auxiliary capacitor to improve the output voltage quality. Due to the slow charging/discharging frequency and bulky auxiliary capacitor, the charging/discharging period

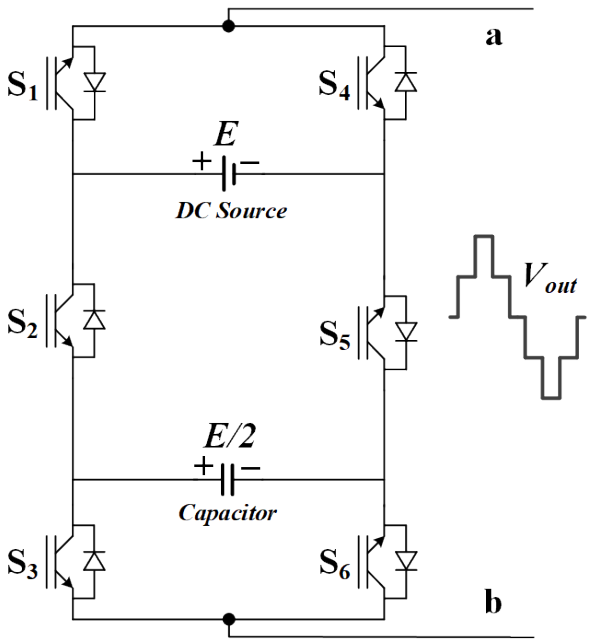

Fig. 1. PUC5 Inverter topology

is also significant. In [15], an LS-based modulation method aims to solve those issues. The proposed method uses two level-shifted triangular carrier waves and logic gates. The number of triangular carriers is halved, and the switching states table is eliminated, resulting in a remarkable reduction in the complexity of the proposed modulation method. However, additional logic gates are introduced to generate appropriate pulses and perform the voltage balancing of the auxiliary capacitor. Although the phase-shift switching technique is well known for its harmonic mitigation performance, it has not been regularly implemented on multilevel inverters due to the complexity at a higher number of levels and difficulty in voltage balancing of the auxiliary capacitors in the configuration [16], [17]. To further improve the performance of the PUC5 inverter, a phase-shift modulation method has been designed and implemented in [18] yet suffers the capacitor's slow voltage balancing and high voltage ripple.

In this paper, a phase-shift (PS) modulation technique is designed for the PUC5 inverter featuring fast sensorless voltage balancing of the auxiliary capacitor, which decreases

the size and, consequently, cost of that capacitor, increasing power density and reliability. Section II describes the PUC5 inverter. Section III briefly discusses the general PS modulation method used in [18]. In Section IV, the proposed phase-shift modulation method is presented. Finally, simulation results are shown and discussed in section V.

II. PUC5 Inverter

The PUC5 Inverter topology is illustrated in Fig. 1, which consists of one pair of low frequency ($S1\&S4$) and two pairs of high frequency ($S2\&S5$ and $S3\&S6$) switches, one auxiliary capacitor and one isolated DC source [19]. In the PUC5 inverter, the capacitor voltage is controlled at half the DC source voltage amplitude using the redundant switching states listed in Table I [12]. Consequently, the need for voltage and current sensors for voltage balancing purposes in the PUC5 inverter can be eliminated.

Given three pairs of switches, there are eight switching states to generate five output voltage levels in the PUC5 Inverter. The switching states, output voltage V_{out}, and capacitor status are shown in Table I. The values 1 and 0 correspond to the ON and OFF states of the switch S_X, respectively, while S_X and S_{X+3} are complementary. There are two redundant states in each positive/negative half cycle that use different switching paths while generating the same voltage levels of $+E/2$ or $-E/2$ at the output. They can be used to increase the flexibility in choosing the proper current path to charge or discharge the capacitor. The effect of each state on the capacitor voltage is also stated in that table. In the traditional sensorless voltage balancing method [12], the capacitor charges during the positive half cycle and discharges during the negative half cycle of the output voltage waveform, which means the speed of charging/discharging is fixed at the reference voltage or line frequency, like 50 Hz. Thus, a large capacitor is required to diminish the voltage ripples in a steady state, which inevitably causes a longer start-up charging time.

TABLE I
SWITCHING STATES OF PUC5 INVERTER

Switching State	S_1	S_2	S_3	V_{out}	Capacitor Charge/Discharge
V_1	1	0	0	$+E$	\
V_2	1	0	1	$+E/2$	Charge
V_3	1	1	0	$+E/2$	Discharge
V_4	1	1	1	0	\
V_5	0	0	0	0	\
V_6	0	0	1	$-E/2$	Discharge
V_7	0	1	0	$-E/2$	Charge
V_8	0	1	1	$-E$	\

III. Phase-shift Modulation of PUC5 Inverter

In PS modulation, the carrier waves have the same frequency and peak-to-peak amplitude. But as its name suggests, a fixed phase shift angle ϕ_{cr} exists between any two adjacent carrier waves, given by:

$$\phi_{cr} = \frac{360^\circ}{(m-1)} \tag{1}$$

Where m is the number of output voltage levels. Moreover, for an m-level converter, $m-1$ carrier waves are required for PS modulation. Therefore, In PUC5, with 5 voltage levels at the output, a 90° angle exists between any two adjacent carrier waves. The required carrier waves are shown in Fig. 2.

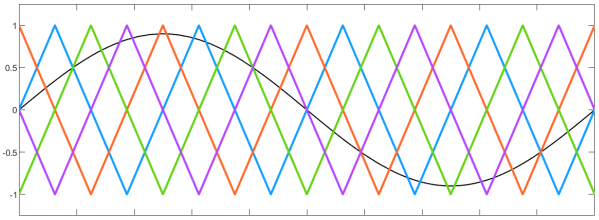

Fig. 2. Required carrier and reference waves for PUC5 Inverter with basic PS modulation ($f_{ref} = 50Hz, f_{sw} = 200Hz$)

Each carrier wave (C_1, C_2, C_3, C_4) is compared with the reference wave during every discrete time period. When the reference is greater than C_x, it outputs 1, otherwise 0. As described in [17], the result of those comparisons will be added at each interval, generating a discrete number between 0 and 4 corresponding to the output voltage levels of $-E$ to $+E$, respectively. The flowchart of the generalized phase-shift modulation is shown in Fig. 3.

IV. Proposed Phase-shift Modulation Method

A. Switching Pattern of Proposed Phase-Shift Modulation Method

The proposed PS modulation method is depicted in Fig. 4, which comprises only two phase-shifted triangular carrier waves, $Cr1$ and $Cr2$, without complex logic gates or a switching table. Therefore, the proposed method doesn't require complex calculations or logic gates, making it easily implementable on affordable microcontrollers.

PUC5 Converter balances the capacitor voltage at the frequency of the reference voltage V_{ref}. The goal of this new scheme is to increase the balancing frequency from the fundamental frequency f_{ref} (50 or 60 Hz) to the switching frequency f_{sw} (in kilohertz). Given Table I, the switching pattern of PUC5 Converter can be generalized as follows:

$S1$ is always on when the reference voltage is positive while off when the reference voltage is negative. $S4$ is complementary with $S1$. The pair of switches $S1$ and $S4$ only answer to the change of polarity of the reference voltage. Therefore, it uses low-frequency switches. For the other two pairs of switches, they are responsible for reference voltage tracking

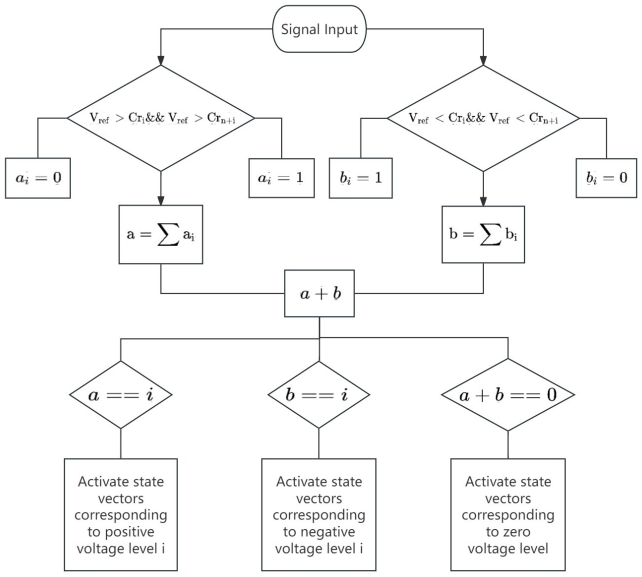

Fig. 3. Flowchart of generalized phase shift modulation for multilevel converters

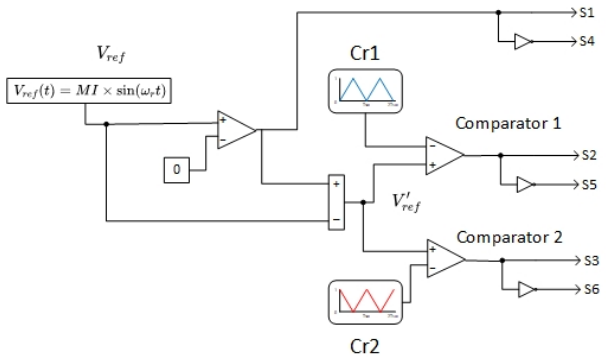

Fig. 4. Proposed phase-shift modulation for PUC5 Converter

and capacitor voltage balancing. They need high-frequency switches. Charging and discharging happen in switching states V_2/V_3 and V_6/V_7, which only involve the transition of S_2 and S_3 with complimentary switching of S_5 and S_6. Thus, S_2 and S_3 are designed to have 180°phase shift to ensure regular transition.

The proposed switching method utilizes a zero-crossing comparator (Z_C) to detect the positive half cycle of the reference voltage (V_{ref}) and control (S_1, S_4) at the fundamental frequency. The expressions for Z_C and (S_1, S_4) are as follows:

$$Z_C = \begin{cases} 1, & V_{\text{ref}} \geq 0 \\ 0, & V_{\text{ref}} < 0 \end{cases} \tag{2}$$

$$S_1 = \overline{S_4} = Z_C \tag{3}$$

Decoupling the switching actions of S_1 from S_2 and S_3, the reference signal V_{ref} should be modified in a way to generate appropriate pulses for S_2 and S_3. Therefore, one can assume that V'_{ref} is a modification of V_{ref} with the switching matrix shown in Table II. To generate those 4 states for S_2 and S_3 by standard PS modulation, 2 carrier waves are required (Cr1 and Cr2), which are shifted 180°.

TABLE II
DESIRED SWITCHING MODULATION METHOD

S_2	S_3	Modulation Method
0	0	$V'_{ref} < Cr1$ & $V'_{ref} < Cr2$
0	1	$V'_{ref} < Cr1$ & $V'_{ref} \geq Cr2$
1	0	$V'_{ref} \geq Cr1$ & $V'_{ref} < Cr2$
1	1	$V'_{ref} \geq Cr1$ & $V'_{ref} \geq Cr2$

According to Fig. 1, the relationship among output voltage V_{out}, DC link voltage V_1 and auxiliary capacitor voltage V_c can be written as below:

$$V_{out} = V_1 - V_c \tag{4}$$

Here, one can decouple the mathematical model of the PUC5 converter into two switching parts [20]. It works when the switching frequency is high enough compared to the fundamental frequency [21] [22]. Therefore, the reference signals for generating required pulses of those decoupled parts can be written based on Eq. (4). V_{ref} represents the reference signal for output voltage, Z_c is assigned for the switching behavior of (S_1,S_4), so:

$$V_{ref} = Z_c - V'_{ref} \tag{5}$$

Thus, the modified reference signal V'_{ref} can be calculated as the following:

$$V'_{ref} = Z_C - V_{ref} \tag{6}$$

Eq (6) is essential to generate the V'_{ref}, which will be modulated by $Cr1$ and $Cr2$ to generate the pulses for S_2 and S_3. The switching pattern, defined alternative function outputs, and output voltage waveform of the proposed modulation method are illustrated in Fig. 5.

B. Sensorless Voltage Balancing of the Auxiliary Capacitor

In the proposed modulation method, the auxiliary capacitor undergoes charging and discharging in each switching period based on the load current direction and the switching operation. The voltage balancing process of the PUC5 converter capacitor in each PWM period is depicted in Fig. 6.

To better illustrate the balancing process, a zoomed-in figure is depicted in Fig. 7. In this cycle, the reference voltage is kept positive, and S_1 is on. When S_2 is on while S_3 is off, during t_2 and t_4, the capacitor discharges. When S_2 is off while S_4 is on, during S_1 and S_4, the capacitor charges. Because the switching frequency f_{sw} is very high, the charging/discharging time is very short, and the change of capacitor current i_c can

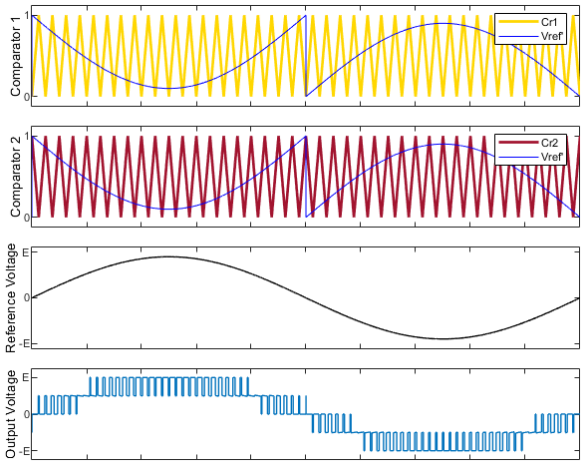

Fig. 5. Switching pattern of the proposed modulation method, alternative reference voltage and output voltage of PUC5 Converter ($f_{ref} = 50Hz, f_{sw} = 2000Hz$)

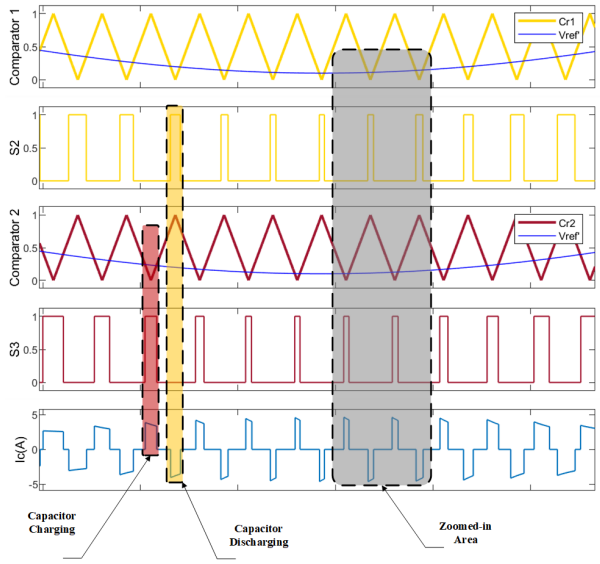

Fig. 6. Balancing the Q_{charge} and $Q_{discharge}$ processes of the PUC5 converter capacitor in each PWM period ($f_{ref} = 50Hz, f_{sw} = 2000Hz$)

be taken as a constant. The electrical charge of the capacitor q is derived as:

$$q = \int i_c dt = i_c(t_1 + t_3 - t_2 - t_4) \quad (7)$$

$$= i_c(t_{sw3on} - t_{sw2on}) \quad (8)$$

Where t_{sw2on} and t_{sw3on} are the on time of switches S_2 and S_3 respectively. In steady state, as long as t_{sw2on} and t_{sw3on} are equal, the PUC5 converter capacitor voltage is always balanced at the voltage level of $E/2$. Since the negative reference voltage half cycle is mirroring with the positive cycle, the voltage balancing works as well.

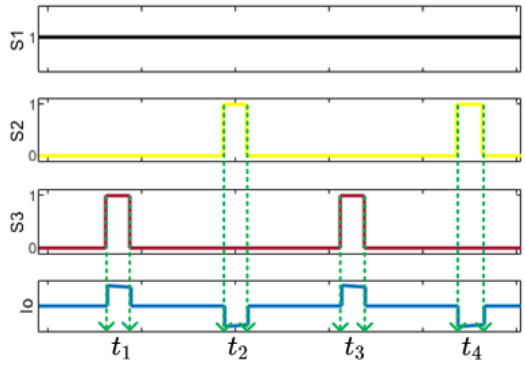

Fig. 7. Zoomed-in capacitor pattern of one switching cycle from Fig. 6

V. Simulation Results

MATLAB/Simulink is used to simulate a standalone system feeding RL load to verify the proposed modulation method and integrated fast sensorless voltage balancing technique. Parameters of the simulation are listed in Table III. The basic PS modulation method and the proposed one have been implemented separately in the simulation for a fair comparison.

Steady-state Simulation results are shown in Fig 8. A smooth 5-level voltage waveform is generated at the output of the PUC5 inverter due to the accurate voltage balance of the auxiliary capacitor. Consequently, a low harmonic current is also drawn by the load.

TABLE III
Simulation Parameters

DC source voltage	$200V$
RL load	$40\Omega, 10mH$
Switching frequency	$2kHz$
Capacitor	$100\mu F$ / $2000\mu F$
Modulation index	0.9

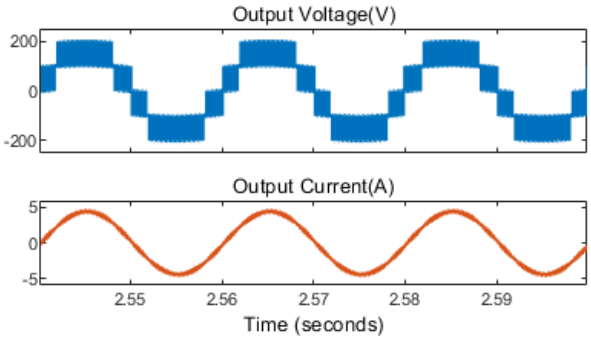

Fig. 8. Output voltage and current of the proposed modulation method

To show the efficient functionality of the proposed switching technique in precise tracking of the reference voltage, a step change has been applied in the amplitude of the DC source. therefore, E has been changed from 200V to 300V and results

are shown in Fig 9. It is clear that the capacitor voltage has been properly balanced at half of the DC voltage.

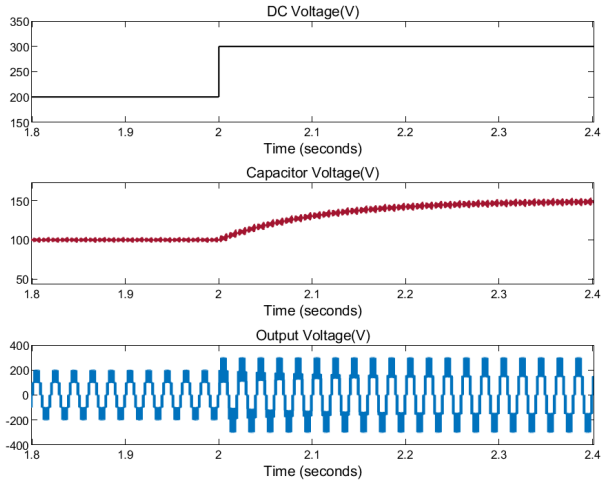

Fig. 9. Transient behavior of sensorless voltage balancing in proposed modulation method

In the next test, the auxiliary capacitor's voltage ripple and the start-up charging time were measured, and this is shown in Fig. 10. It is clear that the capacitor voltage reaches the reference level in almost 0.3s with a peak-to-peak ripple of 7V.

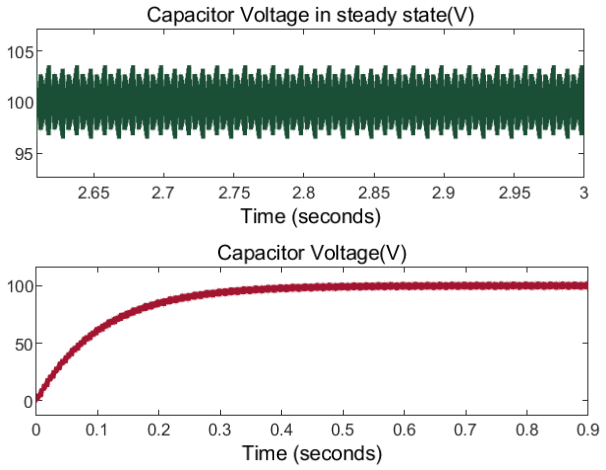

Fig. 10. Capacitor voltage in the steady state of the proposed phase-shift modulation method with C=100μF

Eventually, to have a fair comparison with the basic PS modulation technique, a 2000μF capacitor replaced the 100μF as the auxiliary capacitor to have the same voltage ripple of almost 7V. Results are depicted in Fig. 11, showing the same amount of voltage ripple but a long start-up charging time of almost 1.2s. Moreover, the frequency of the charge/discharge transition is obvious from those figures. Obviously, the proposed technique charges/discharges the capacitor at the switching frequency, resulting in a significant reduction in the capacitor size. As shown here, the capacitor size has been reduced by 95% from 2000μF to 100μF after implementing the proposed switching technique.

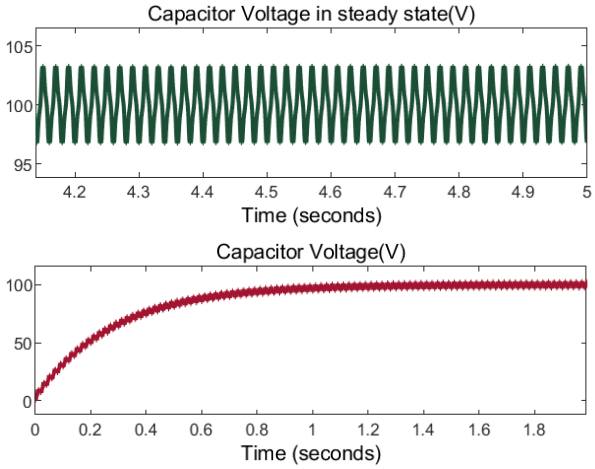

Fig. 11. Capacitor voltage of the basic phase-shift modulation method C=2000μF

VI. Conclusion

In this paper, a fast sensorless PS-modulation-based voltage balancing for the PUC5 inverter has been designed and implemented. Compared to other reported methods, the proposed technique not only reduced the complexity of the voltage balancing algorithm but also increased the speed of charge/discharge transition of the capacitor, which led to low voltage ripple and size reduction significantly. Various simulation results have been illustrated and discussed, proving the efficiency and accuracy of the proposed technique in balancing the voltage and tracking the reference value. Moreover, a comparison to basic PS modulation showed an achievement of 95% capacitor size reduction with the proposed technique while having the same performance and voltage ripple at the auxiliary capacitor.

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