Novel Digital Controller for Boost PFC

Master of Science Thesis

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Abstract

LED lighting, as the fourth-generation lighting technology, is developing rapidly over the past years due to its high energy efficiency, longer life span and sustainability compared to incandescent light bulbs and CFLs. Today's stand-alone LED drivers for professional lighting systems contain two cascaded power converters: an input and an output power stage. The output power stage drives the LED load with constant average current to achieve a uniform light output without visible light flicker and stroboscopic effects. The input power stage is a boost converter which acts as a power factor corrector (PFC), providing to the mains a power factor (PF) of at least 0.9 and a constant average supply voltage to the output power stage.

In high-end LED drivers, both the boost PFC converter as well as the converter in the output power stage are digitally controlled by a PI controller. The PFC controller currently being used has a low bandwidth as to not interfere with the power factor correction function. Because of this low bandwidth, disturbance from mains and load will be transferred to the boost PFC output capacitor, which, on its turn, can lead to undesired visible light effects if these disturbances are too large.

The thesis aims at improving the dynamic response of the boost PFC converter without sacrificing PF/THD performance. Three solutions:

1. Digital notch/comb filter
2. Input voltage feedforward
3. Variable gain

are proposed and investigated in detail. Simulation result for each solution shows improved dynamic response to both mains and load disturbances. Four criteria are applied to evaluate the 3 proposed methods. Finally system with notch filter is implemented to verify the performance of the proposed design. The experimental result shows improved dynamic response to both mains and load disturbances, as well as improved THD performance.

Acknowledgement

First and foremost, I would like to express my deepest gratitude to my supervisors Dr. Jeroen van Helvoort and Jurgen Willaert within Philips, and Dr. Jelena Popovic from TU Delft, who guided me without reservation throughout the past one year. Except for the countless academic guidance, the more important thing that Jeroen and Jurgen teach me is how to think and behave as an engineer, from which I will benefit for the rest of my life. I am still not good enough, but thanks for making me better. This thesis wouldn't have been done without their guidance.

My great thanks also go to Chrstiaan van Dijk, for saving me from helplessness during implementation and also, for all the support during the past one year. Thanks for showing me how a good engineer should be, for sure you are the role model to me for my future career. I would also like to thank Erik de Wilde and all other people who helped me with this thesis. Furthermore, I would like to give my sincere thanks to Dik Pardijs for hiring me as a trainee here, and all other colleagues in the electronics group for spending such a pleasant year with me.

Cheers to the most amazing two years ever! Thanks Junting, Si and Di for all the fun that we had, the sorrow we shared and the company we gave to each other during all the hard times. Thank you Qi and Jiawei for the overseas support. You make me believe that friendship lasts forever.

This thesis is dedicated to my parents, who have given me more than that I could ask for. I will always love you, respect you and take care of you, as what you did for me all over these years.

Hey girl. I am so proud of you.

Contents

Chapter 1 Introduction

1.1 Problem definition

Today's stand-alone LED drivers for professional lighting systems contain two cascaded power converters: an input and an output power stage. The output power stage drives the LED load with constant average current to achieve a uniform light output without visible light flicker and stroboscopic effects. The input power stage is a boost converter which acts as a Power Factor Corrector (PFC), providing to the mains a Power Factor (PF) of at least 0.9 and a constant average supply voltage to the output power stage. The block diagram for the stand-alone LED driver is shown in figure 1-1.

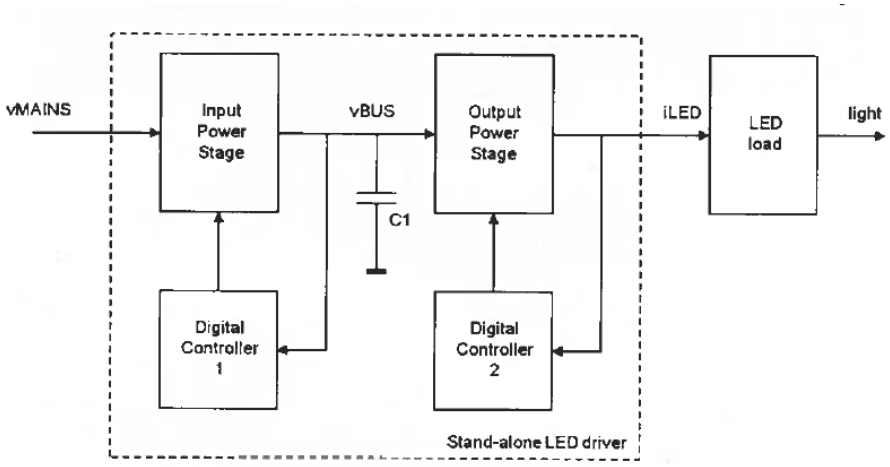


Figure 1-1 Block diagram of stand-alone high-end LED driver

In high-end LED drivers, both the boost PFC converter as well as the converter in the output power stage are digitally controlled by a PI controller. The PFC controller currently being used has a low bandwidth (10-20Hz) as to not interfere with the power factor correction function. Because of this low bandwidth, disturbances from mains and load are transferred to the boost PFC output capacitor, which, on its turn, can lead to undesired visible light effects if these disturbances are too large.

To summarize, the problem existing now is the compromise between good PF and fast dynamic response. The reason for this contradiction will be further explained in detail in section 2.1.5.

1.2 Objective

Based on the problem which is defined in last section, the dynamic response of the system needs to be improved without sacrificing PF to provide a more stable light output under disturbances. The objective of this research aims at designing a novel digital controller for the boost PFC which:

1. Reduces voltage disturbances on the output capacitor to the minimum
2. Achieves an excellent power factor

The target improvement factor in sensitivity to disturbances should be at least 10(20dB).

1.3 Approach

To achieve the objective, the operation mode and control methods of the boost converter are first investigated. For detailed analysis of the control loop, each part of the system is modelled and the transfer functions are derived. Based on the transfer function of each part of the system, three control methods are proposed to improve the dynamic response of the boost PFC without harming PF:

1. Digital notch/comb filter
2. Feedforward
3. Variable gain

The detailed designs and simulations of the three proposed solutions will be discussed in chapter 5. According to the simulations, all three methods show improved system dynamic response to both mains and load disturbances and good power factor.

1.4 Organization

The remaining part of the report is organized as follow. In chapter 2, the related background knowledge for this assignment will be reviewed. In chapter 3, each part of the control loop will be modelled and the corresponding transfer functions will be derived. In chapter 4, the system and design requirements will be specified and the system behaviors with conventional controller will be shown in simulation. In chapter 5, three novel controllers to improve the system dynamic response will be designed, simulated and compared with conventional controller. In chapter 6, the three proposed controllers in chapter 5 will be evaluated with four criteria. After evaluation, the use of a notch filter scores highest and will go for implementation. In chapter 7, notch filter will be implemented with a 32-bit microcontroller. The experimental results show a significantly improved dynamic response to both mains and load disturbances. In chapter 9, the main conclusions will be drawn and further research works will be recommended.

Chapter 2 Literature Review

2.1 Power Electronics

2.1.1 Power Factor and THD

Power factor (PF) of an AC electrical power system is defined as the ratio of the real power flowing to the load to the apparent power in the circuit. Real power (unit in W) is the capacity of the circuit for performing work in a particular time. Apparent power (unit in VA) is the product of the current and voltage of the circuit, which is the sum of real power and reactive power (unit in var). The relationship of real power, reactive power and apparent power is shown in Figure 2-1.

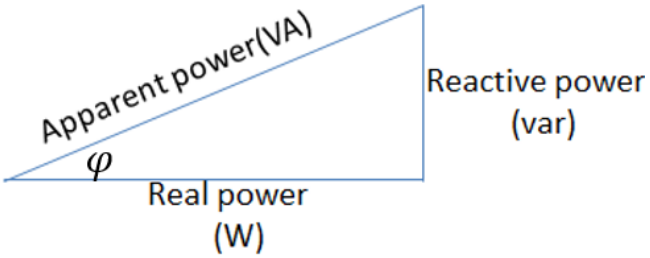


Figure 2-1 power triangle

In real circuits, real power is used by resistive components while inductive and capacitive components contribute to reactive power. In linear circuits with sinusoidal voltages and currents, the equation for power factor can be simply written as,

$$\boldsymbol{PF = cos\,\varphi} \qquad \text{Equation 2-1}$$

Where, φ is the phase angle between current and voltage.

But in real power system, line current drawn from the utility by the power electronic equipment is not always a pure sinusoidal waveform, sometimes it deviates significantly from a sinusoidal waveform (as shown in Figure 2-2). Then the definition of total harmonic distortion (THD) which is the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency is introduced.

$$\boldsymbol{THD = \frac{\sqrt{I_2{}^2 + \cdots + I_n{}^2}}{I_1}} \qquad \text{Equation 2-2}$$

Where I_1 is the fundamental frequency component, $I_2, \ldots, I_n$ are the harmonic components. Thus, the total power factor for the non-linear loads can be written as,

$$\boldsymbol{PF = \frac{\cos\varphi}{\sqrt{1+THD^2}} = \frac{DPF}{\sqrt{1+THD^2}}} \qquad \text{Equation 2-3}$$

Where φ is the phase angle between current and voltage, DPF is the displacement power factor which is the same as the power factor in linear circuits with sinusoidal voltages and currents.

From the above definitions and equations, it can be concluded that power factor measures how efficiently the power drawn from the source is being converted into real work. It is always an important aspect to consider in an AC circuit. Good power factor can benefit both the supplier and the customer.

First of all, a good power factor means that the reactive power drawn by the load is very low and a high percentage of the supplied power can be turned into real power, which represents a good efficiency from the supplier to the customer. The power loss due to the transmission line can be written as,

$$\boldsymbol{P_L = I^2 R_L} \qquad \text{Equation 2-4}$$

So if power factor is poor, which means that more current need to be drawn from the grid to meet the demand of the load compared to that with good power factor. This results in a high value of current on the transmission line which means more transmission losses, thus more electricity generated by the supplier. The wasted electricity will cause additional costs for the electricity supplier and consequently these costs are passed on to the customer.

Secondly, the poorer the power factor is, the larger amount of current flows through the transmission line and the larger the voltage drop on the transmission line will be. As a result, the voltage on the custom side will significantly drops with a poor power factor. This voltage drop makes the electrical equipment work below the nominal condition thus limit the performance of the electrical equipment.

Furthermore, the reactive power drawn by the loads will flow back to the grid eventually, which may create harmonics to the grid thus contaminating the power grid.

Therefore, a good power factor is of great importance not only for the electricity supplier but also the customer.

In view of the development of power electronic equipment connected to the utility system, various national and international agencies have been considering limits on harmonic current injection to maintain good power quality as have stated in previous sections that the value of THD influences the performance of PF. As a consequence, various standards and guidelines have been established that specify limits on the magnitudes of harmonic currents and harmonic voltage distortion at various harmonic frequencies [1].

One of the most widely used standards is the *IEEE guide for harmonic control and reactive compensation of static power converters,* which contains recommended practices and requirements for harmonic control in electric power systems, specifies requirements on the user as well as on the utility. Table 2-1 lists the limits on the harmonic currents that user of power electronic equipment and other non-linear loads is allowed to inject into the utility system. Table 2-2 shows the quality of the voltage that the power producer is required to furnish a user, which is based on the voltage level.

I_{SC}/I_1	Odd Harmonic Order h (%)					Total Harmonic Distortion (%)
	$h < 11$	$11 \le h < 17$	$17 \le h < 23$	$23 \le h < 35$	$35 \le h$	
<20	4.0	2.0	1.5	0.6	0.3	5.0
20–50	7.0	3.5	2.5	1.0	0.5	8.0
50–100	10.0	4.5	4.0	1.5	0.7	12.0
100–1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

Table 2-1 Harmonic current limits for nonlinear load connected to a public utility at the point of common coupling(PCC) with other loads at voltages of 2.4-69kV [1]

Where Isc is the maximum short-circuit current at PCC. I_1 is the maximum fundamental-frequency load current at PCC. Even harmonics are limited to 25% of the odd harmonic limits above.

	2.3–69 kV	69–138 kV	> 138 KV
Maximum for individual harmonic	3.0	1.5	1.0
Total harmonic distortion	5.0	2.5	1.5

Table 2-2 Harmonic voltage limits (Vh/V1)% for power producers [1]

2.1.2 PFC

In the front-end stage of conventional converters, which typically consists of a rectifier bridge followed by a capacitor filter, an unregulated DC bus from the AC mains is found. The filter capacitor must be large enough to have a relatively low ripple on the DC level. This means that the instantaneous line voltage is below the voltage on the capacitor for most of the time. So the rectifiers conduct only for a small period of each half mains cycle[1]. This may result in distortion of the AC line current. The traditional input stage with capacitive filter has a low PF (0.5-0.7) and a high THD (>100%) as shown in Figure 2-2.

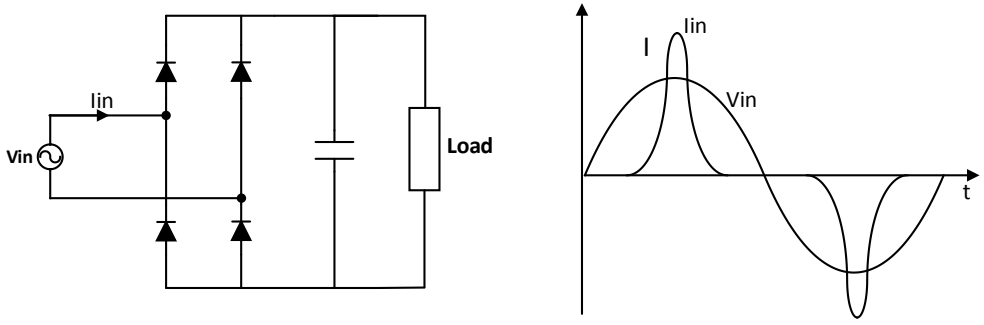


Figure 2-2 Current & voltage waveforms for bridge rectifier

Because of the large harmonic components as indicated by Figure 2-2, typical diode rectifiers used for interfacing power electronic equipment with the utility system may exceed the limits on individual current

harmonics and THD specified in Table 2-1, which can have significant effect to the mains, the output filter capacitor and the EMI filter[1]. As a result a PFC is needed for a better THD and PF performance at the interface.

There are two kinds of PFC in general, which are Passive PFC and Active PFC, respectively. The realization of these two kinds of PFCs are explained below.

1. Passive PFC

In a passive PFC, inductors and capacitors are used in combination with the diode bridge rectifier to improve the waveform of the current drawn from the grid. One example of the passive PFC circuit and the corresponding waveforms are shown in Figure 2-3.

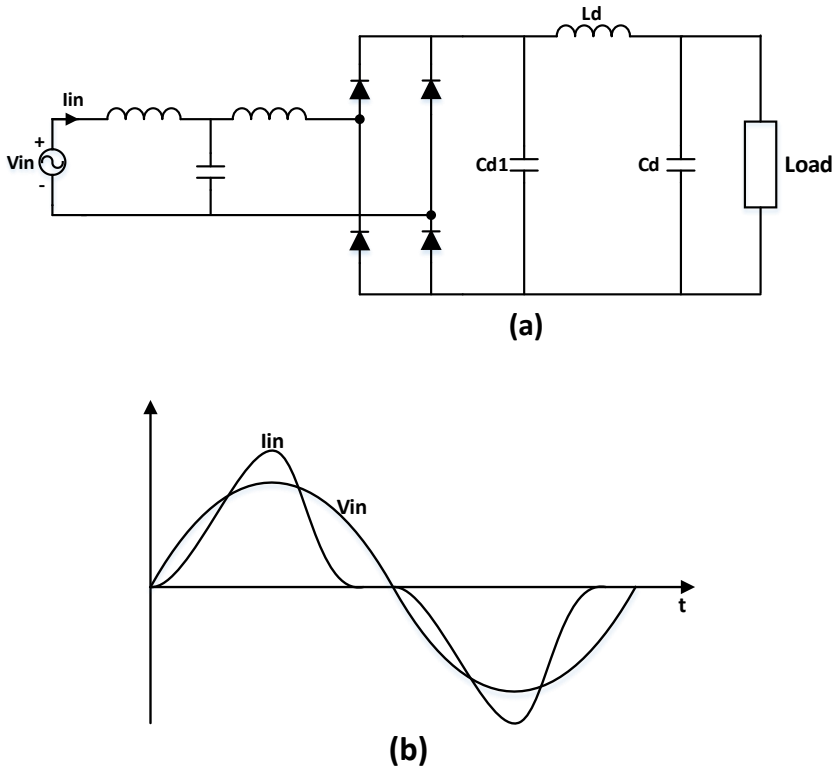


Figure 2-3 Passive filters (a) Passive PFC schematic (b) current waveforms in respect to mains voltage

A capacitor C_{d1} which is smaller relative to C_d is directly connected across the rectifier bridge. The ripple in v_{d1} is larger but results in an improved waveform of i_s. The ripple in v_{d1} is filtered out by the low-pass filter which is formed by L_d and C_d. By applying passive PFC, the power factor is improved from very poor to somewhat acceptable. But still, the overall energy efficiency remains almost the same because there are additional losses in the inductor [1]. However, the obvious disadvantages of such a circuit are cost, size, losses and the significant dependence of the average dc voltage v_d on the power drawn by the load. To further improve PF and to solve the above mentioned disadvantages, active PFC is introduced.

2. Active PFC

By using switching techniques, an active power factor corrector located between the rectifier bridge and the filter capacitor is applied to regulate the current shape and allow a sinusoidal current drawn from the mains, in phase with the line voltage. PF can then become very close to 1. Also, the cost, power losses and size of the current shaping circuit is rather small by using active PFC circuits compared to that of passive PFC circuits.

Theoretically, any switching topology can be used to achieve a high PF, but, in practical, boost topology has become the most popular one because of the following reasons:

1. The circuit requires the fewest external parts.(low-cost solution)
2. The boost inductor located between the bridge and the switch causes the input di/dt to be low, thus minimizing the noise generated at the input and, therefore, the requirements on the input EMI filter.
3. The switch is source-grounded, therefore easy to drive.

The basic schematic using a boost converter as PFC and the corresponding waveforms are shown in Figure 2-4.

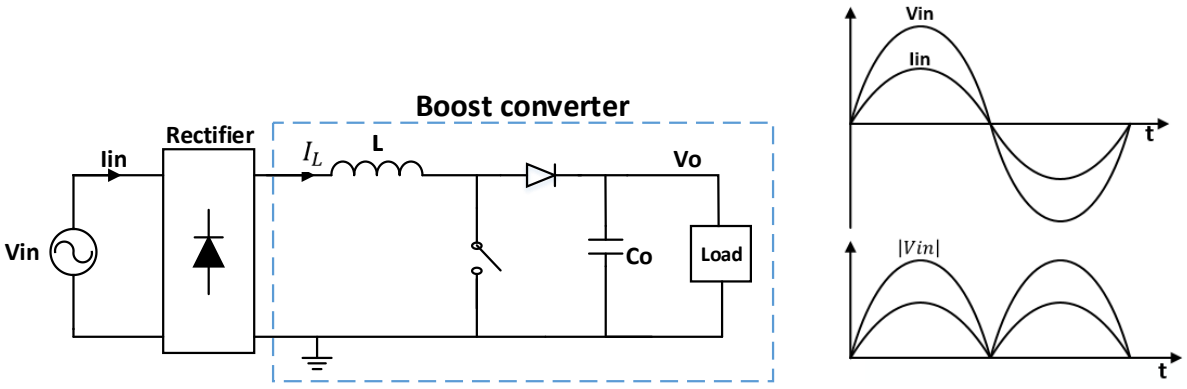


Figure 2-4 Active PFC with boost converter and the corresponding voltage & current waveforms

The operation details of boost converter will be introduced in further sections.

2.1.3 Boost PFC

Figure 2-5 shows the schematic of a boost converter.

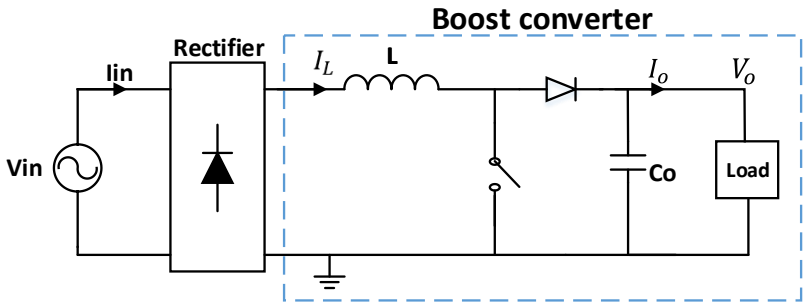


Figure 2-5 Boost topology schematic

A boost converter can operate in 3 modes: continuous conduction mode (CCM), discontinuous conduction mode (DCM) and boundary conduction mode (BCM), which depends on the current flowing through the energy storage inductor of the boost converter. Each of these three modes refers to different control methods and circuit behavior when the boost converter is used as a PFC.

The above 3 operating modes are compared for the application of power factor correction as shown in Table 2-3.

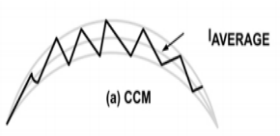
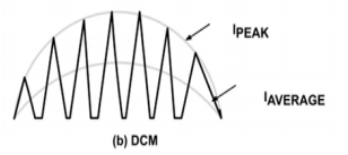
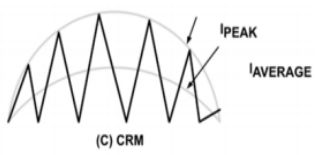
	CCM	DCM	BCM
Waveform (over half main cycle)			
Switching frequency	Fixed/variable	fixed	variable
MOSFET stress	Average(hard switching, high turn-on, turn-off losses)	High(peak current stress causes conduction losses; low turn-on losses(ZVS possible), large turn-off losses)	High(peak current stress causes conduction losses; low turn-on losses(ZVS possible), large turn-off losses)
Diode	Fast diode with low reverse recovery current	Turn off naturally, reverse recovery in diode can be eliminated	Turn off naturally, reverse recovery in diode can be eliminated
EMI	Small di_{in}/dt	Large di_{in}/dt	Large di_{in}/dt
Inductor size	Large(can be 10 times larger than that of BCM)	small	medium
Inductor loss	Low losses(due to low current ripple)	High losses(due to large current ripple)	High losses(due to large current ripple)
Control method	Fixed frequency: duty cycle control Variable frequency: tolerance-band control(current control)	Constant on-time control	Constant on-time control/ peak current control
Control complexity	Complex	Simple	Simple
PF/THD	best	good	better
Application	Any power level	Never use intentionally but unavoidable at light loads	<200W(due to high peak current EMI issues)

Table 2-3 Comparison of CCM, BCM, DCM

DCM is never used intentionally but sometimes it is unavoidable to enter DCM at light loads. CCM operation can achieve low input current distortion and have the best PF and THD performance. However the significant reverse recovery losses on the boost diode and the high switching losses will limit the efficiency. Operating in BCM can eliminate the reverse recovery and switching losses of boost diode thus provide higher efficiency. Also the smaller inductor size for BCM can lower the cost and the size of the PFC. Since for most residential LED lighting applications power is no more than 200 watts, BCM is the best operating mode for higher efficiency, small inductor size and simple control method.

2.1.4 Basic Operation of BCM Boost Converter

Based on the boost converter in Figure 2-5, the waveforms for a boost converter operating in BCM are shown in figure 2-6.

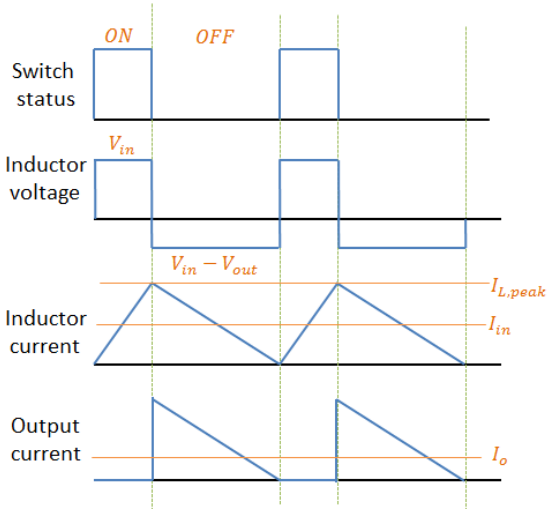


Figure 2-6 waveforms for BCM

The basic equations can be written as,

$$\boldsymbol{D = \frac{t_{on}}{T} = \frac{V_{out}-V_{in}}{V_{out}}} \qquad \text{Equation 2-5}$$

$$\boldsymbol{I_{L,peak} = \frac{V_{in}}{L} \cdot t_{on} = \frac{V_{out}-V_{in}}{L} \cdot t_{off} \quad \frac{V_{out}-V_{in}}{V_{out}}} \qquad \text{Equation 2-6}$$

$$\boldsymbol{I_{in} = \frac{1}{2} I_{L,peak}} \qquad \text{Equation 2-7}$$

$$\boldsymbol{I_o = (1 - D) I_{in}} \qquad \text{Equation 2-8}$$

Where D is the duty cycle, $\boldsymbol{I_{L,peak}}$ is the peak inductor current, $\boldsymbol{I_{in}}$ is the input current, $\boldsymbol{I_o}$is the output current, $\boldsymbol{t_{on}}$is the on time of the switch, $\boldsymbol{T}$ is the switching period, $\boldsymbol{V_{out}}$ is the output voltage, $\boldsymbol{V_{in}}$ is the input voltage, L is the boost inductor value.

As indicated in the name BCM, new switching period is initiated when the inductor current returns to zero, which is at the boundary of continuous conduction and discontinuous conduction operations. BCM creates better switching condition for the MOSFET and diode. The diode reverse recovery can be eliminated and a fast-recovery diode is not needed. Also, MOSFET can be turned on with zero voltage, which reduces the switching losses. When the power transistor of the boost converter is turned on for a fixed time, the peak inductor current is proportional to the input voltage. Since the current waveform is triangular, the average value in each switching period is proportional to the input voltage. In a sinusoidal input voltage, the input current of the converter follows the input voltage waveform with very high accuracy and draws a sinusoidal input current from the source. This behavior makes the boost converter in BCM operation a good choice for power factor correction. The operation waveforms during one mains cycle are shown in figure 2-7.

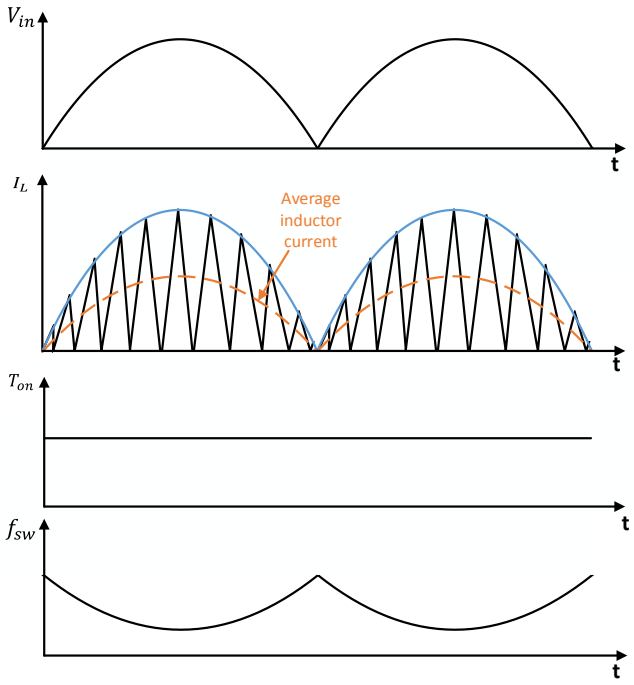


Figure 2-7 Operation waveforms of BCM PFC

Switching frequency of the MOSFET can be calculated as equation 2-9.

$$\boldsymbol{f = \frac{1}{T} = \frac{1}{t_{on}+t_{off}} = \frac{{V_{in,pk}}^2}{4LP_{avr}V_o}\left(1 - \frac{V_{in,pk}}{V_o}\sin \omega t\right)} \qquad \text{Equation 2-9}$$

Then the maximum and minimum switching frequencies are shown in Equation 2-10 and 2-11.

$$\boldsymbol{f_{min} = \frac{{V_{in,pk}}^2}{4LP_{avr}V_o}\left(1 - \frac{V_{in,pk}}{V_o}\right)} \qquad \text{Equation 2-10}$$

$$\boldsymbol{f_{max} = \frac{{V_{in,pk}}^2}{4LP_{avr}V_o}} \qquad \text{Equation 2-11}$$

It can be seen from the waveforms and the equations, the switching frequency of the MOSFET changes within half mains cycle. The lowest frequency occurs at the peak of sinusoidal line voltage. Also when the load decreases, the peak inductor current diminishes with reduced MOSFET on time and, therefore, the switching frequency increases. This can cause severe switching losses at light-load condition and too-high switching frequency operation may occur at startup. Therefore, switching is often limited to a predefined max value. Also, to avoid audible noise, the minimum switching frequency must be above audible frequency (35kHz) which means that an appropriate inductance value must be chosen.

The above waveforms and analyses in this section are based on neglecting the oscillation of the boost inductor and the parasite capacitance of the MOSFET after the current through the diode goes to zero. If oscillation is taken into account, then sometimes zero voltage switching cannot be guaranteed, the situation of hard switching may occur. Figure 2-8 shows the equivalent circuit.

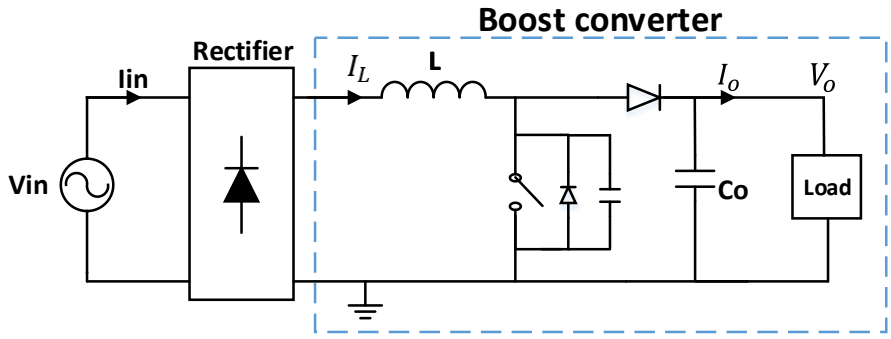


Figure 2-8 Equivalent circuit with parasite capacitance

Then the switching waveforms are shown in Figure 2-9 [2].

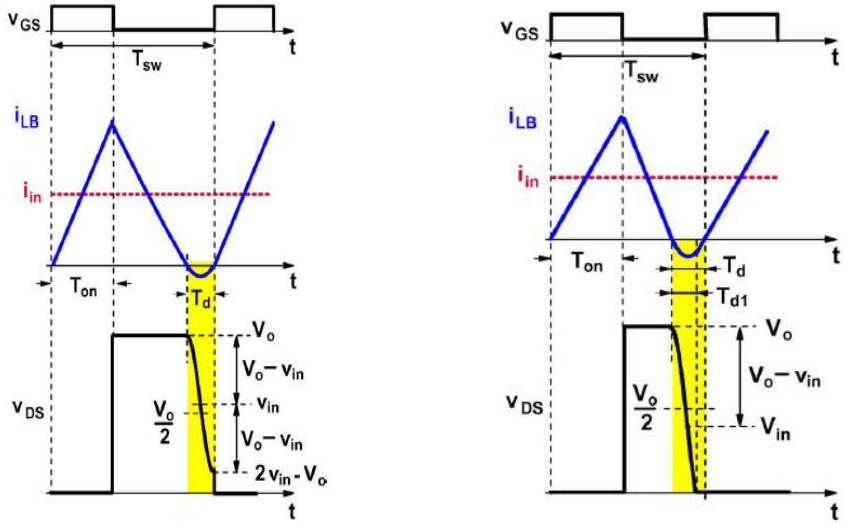


Figure 2-9 a) Vin>Vo/2, valley switching **b) Vin<Vo/2, ZVS**

As can be seen from the waveforms, when input voltage is larger than half of the output voltage, valley switching will take place (hard switching which results in turn-on losses of the switch); otherwise, zero-

voltage switching can be achieved. In this case, the switch is closed after the intrinsic body diode of the MOSFET switch has started to conduct, turn-on is now only with 0.7V on drain-source.

2.1.5 Control of Boundary Conduction Mode Boost PFC

Normally there are two control loops in a PFC: a wide-bandwidth cycle by cycle current control loop and a low-bandwidth voltage feedback control loop.

For the inner high bandwidth current control loop, constant on-time control and peak current control are the most widely used methods, which are also defined as current-mode control and voltage-mode control respectively. In voltage mode, the error signal directly controls the on-time of the transistor. While in current mode, the error voltage sets the inductor peak current. The schematic of the two control methods are shown in figure 2-10 and figure 2-11.

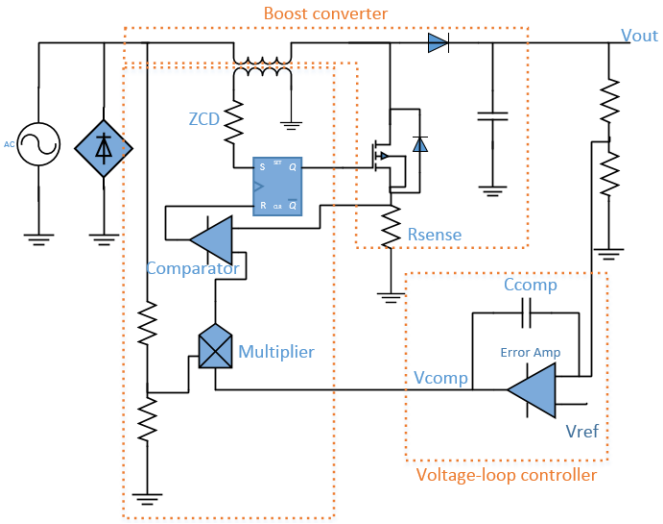


Figure 2-10 Current-mode control for boost PFC

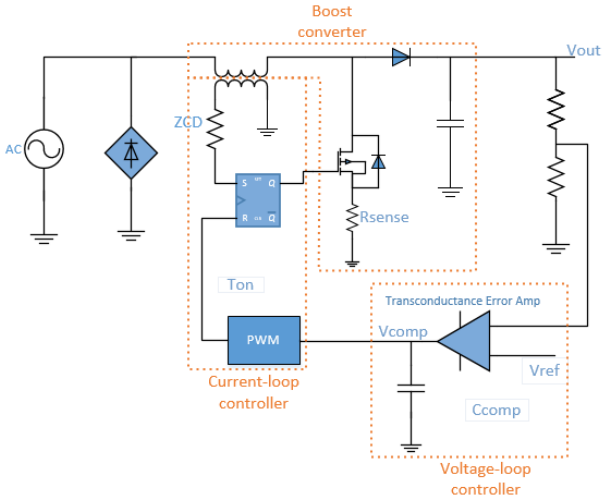


Figure 2-11 Voltage-mode control for boost PFC

1. High bandwidth current control loop

For both the constant on time controlled and peak current controlled BCM controllers, the boost switch is turned on when the boost inductor current reaches zero. This is measured with a zero-current-detect resistor connected to the auxiliary winding, which feeds that signal into the control IC. The main difference between the two control methods is how the controller decides when to turn off the power MOSFET.

In peak current control, the error signal Vcomp is fed into the multiplier and multiplied by a percentage of the rectified mains voltage. The result is a rectified sinusoid whose peak amplitude depends on the mains peak voltage and the value of the error signal. This multiplied value is the reference signal for the current comparator, which sets the transistor peak current cycle by cycle. At steady state, the error signal is a constant so the inductor current can follow the shape of the rectified voltage.

In constant on time control, the error signal is directly compared with a PWM signal to control the on time of the transistor. At steady state, the error signal is a constant value so constant on time can be achieved, which means that the current can follow the shape of the rectified voltage.

As can be seen from the control schematic, for current mode operation the input voltage, transistor current and output voltage need to be sensed to provide the reference current for switching. So it requires accurate sensing for control loop accuracy and relatively high voltage levels. This voltage level can result in significant power loss. However, output voltage regulation is independent of current with voltage mode, which makes relatively crude current sensing is acceptable since it is only necessary for output overload protection, the relatively crude current sensing can save considerable circuit complexity and reduce circuit power loss.

Also, if seen from digital implementation, constant on time control is much easier because of the relatively simpler control procedure.

Therefore, constant on-time control is used for later design and implementation.

2. Low bandwidth voltage control loop

As mentioned before, there is another feedback control loop which controls the output voltage of the boost PFC. This control loop has a very low bandwidth, normally between 10Hz to 20 Hz. To explain this low bandwidth, energy storage has to be introduced.

For a given constant load, the load current I and the instantaneous load power P_{load} are also constant. However, the instantaneous input power of a single-phase ideal rectifier P_{ac} is not constant. The above expressions can be written as equation 2-12 and 2-13.

$$\boldsymbol{P_{load}(t) = VI} \qquad \text{Equation 2-12}$$

$$\boldsymbol{P_{ac}(t) = v_g(t) i_g(t)} \qquad \text{Equation 2-13}$$

Where $v_g(t)$ and $i_g(t)$ are the instant input voltage and current from the mains side. If the above equations are combined, then P_{ac} can be written as,

$$\boldsymbol{P_{ac}(t) = \frac{V_M^2}{Re}\sin^2(\omega t) = \frac{V_M^2}{2Re}(1 - \cos(2\omega t))} \qquad \text{Equation 2-14}$$

As can be seen from equation 2-14, the input power varies in time. So some element within the rectifier must supply or consume the difference between the instantaneous ac input power and output dc power. Therefore, it is necessary to add to the system a low-frequency energy storage element such as a capacitor. The difference between the instantaneous input and load power flows through this capacitor. The waveforms of the two powers and the voltage across the capacitor are shown in figure 2-12.

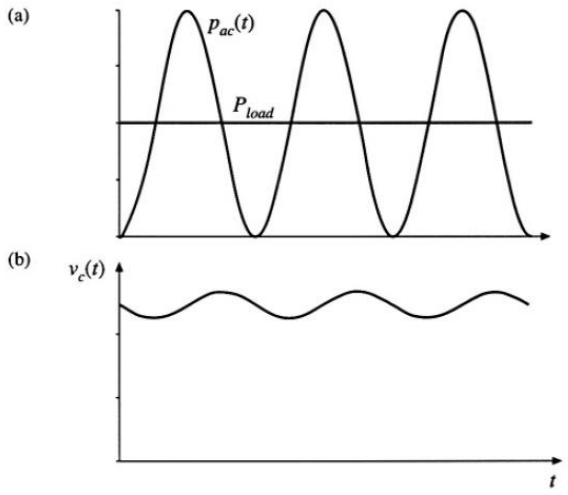


Figure 2-12 (a) Instantaneous ac input power $\mathbf{P_{ac}(t)}$ and constant dc load (b) Energy storage capacitor voltage $\mathbf{v_c(t)}$

The bandwidth of the energy storage capacitor voltage controller can lead to significant ac line current harmonics. When this control loop has high bandwidth and high gain, then it varies the input resistor quickly and tries to remove the voltage ripple on the output capacitor, which will result in a distortion the ac line current waveform. In the extreme limit of perfect regulation of the energy storage capacitor voltage, which is when the capacitor stored energy is constant and the instantaneous input ac line power and load power are equal. The controller prevents the energy storage capacitor from performing its low-frequency energy storage function. The ac line current can then be written as equation 2-15.

$$\boldsymbol{i_{ac}(t) = \frac{p_{ac}(t)}{v_{ac}(t)} = \frac{p_{load}(t)}{v_{ac}(t)} = \frac{P_{load}}{V_M \sin(\omega t)}} \qquad \text{Equation 2-15}$$

This waveform is sketched in figure 2-13.

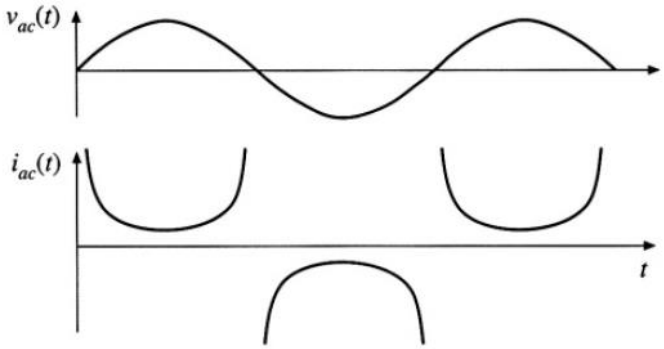


Figure 2-13 waveforms with pure dc output (vc(t) = Vc)

In this case, ac line current tends to infinity at the zero crossings of the ac line voltage waveform, such that the instantaneous input power is constant. It can be shown that the THD of this current waveform is infinite, and its distortion factor and power factor are zero. So the bandwidth of this controller should be limited. This loop must have sufficient small gain at frequency $2\omega_{line}$ so that it will not attempt to remove the capacitor voltage ripple that occurs at the second harmonic of the ac line frequency.

For the consideration of a unity power factor, if seen from the mains side, the PFC including the connected load should be with a resistive property which refers to a bandwidth as low as possible. However, for the consideration of a good bus regulation, the PFC including the connected load should behave as a constant voltage load, which requires a bandwidth as high as possible. In other words, a low bandwidth can generate a nearly fixed on-time over half mains cycle and thus low input current THD and good PF can be achieved. But on the other hand, because of this low bandwidth, the PFC stage react to changes in output load or input voltages slowly. Consequently, there is a risk of overshoots during startup, load steps and line steps. Therefore, there is always a compromise between a good PF/THD and fast dynamic response.

For system controlled with a PI controller, the relationship between the bandwidth and THD performance is shown in table 2-4(ideal model).

Bandwidth (Hz)	Suppression at $2f_{line}$ (dB)	THD (%)
10	-20	4.8
20	-14.3	9.5
50	-6.3	23.1
80	-2.4	34.4

Table 2-4 THD as a function of bandwidth

2.2 Control

2.2.1 Control theory

This assignment focuses on the voltage control loop of PFC. A few definitions related to control theory need to be introduced to analyze the system behavior in frequency domain. The basic block diagram of close loop system is shown in Figure 2-14.

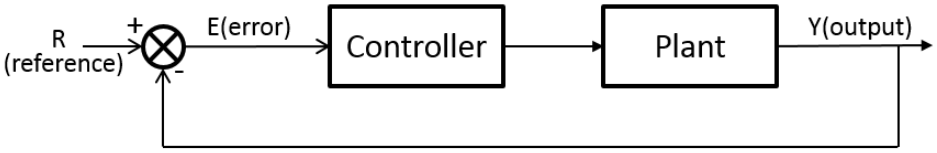


Figure 2-14 Block diagram of close loop system

Open loop of the system is defined as controller multiply by plant as shown in equation 2-16.

$$\boldsymbol{OL = C \cdot P} \qquad \text{Equation 2-16}$$

The open-loop bode plot gives information about the system: system gain, bandwidth, phase margin and gain margin, which gives clues about the system performance.

Open-loop gain is a proportional value that shows the relationship between the magnitude of the input to the magnitude of the output signal under steady state. A high DC gain indicates small steady state error. The bandwidth of a closed loop system can be defined in many ways, in this report, the bandwidth is defined as the frequency at which open-loop gain equals 0dB. A high bandwidth indicates a good system dynamic response to disturbances. Phase margin (PM) and gain margin (GM) are two key concepts to measure the stability of the closed-loop system. Phase margin is the distance between the phase at bandwidth frequency and -180 degrees. It indicates relative stability, the tendency to oscillate during its damped response to a disturbance such as a step function[3]. Gain margin is defined as the system gain when the phase becomes -180 degrees. It indicates absolute stability and the degree to which the system will oscillate without limit giving any disturbances. According to design guideline, at least 30 degrees PM and 10dB GM should be provided to ensure the performance of the system. Also, during design, the open-loop bode amplitude plot should cross0dB line with a slope of -20dB/dec. An example of system open-loop bode plot and the corresponding system evaluation parameters are shown in figure 2-15.

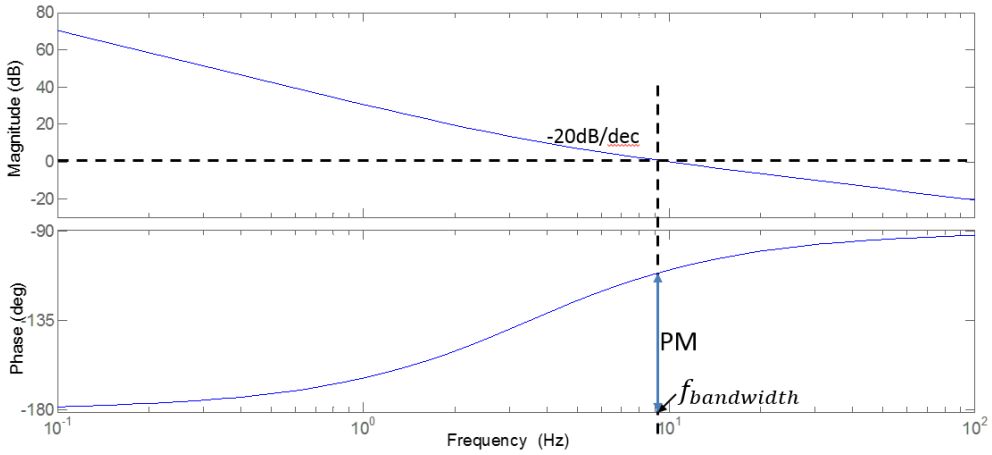


Figure 2-15 Open loop amplitude and phase Bode plot

To further see the system's ability to suppress an error, sensitivity is then introduced, which can be defined as error divided by reference which is shown in equation 2-17.

$$\boldsymbol{S = \frac{E}{R} = \frac{1}{1+CP}} \qquad \text{Equation 2-17}$$

Sensitivity tells how the error can be attenuated by the controller. The nearer sensitivity is to 1, the less attenuation to the error. As can be observed in Figure 2-16, system can suppress error to a very small value for low frequency disturbance. However, if the disturbance frequency is higher than the bandwidth, the system cannot react to the error at all. Also, there is an overshoot at bandwidth frequency. Higher bandwidth will result in larger overshoot.

2.2.2 Digital implementation

For many years, PFCs are mostly controlled by analog controllers. PFCs with analog controllers can already be well controlled and achieve good power. However, for the consideration of the system monitoring capabilities, digital controllers have better performance compared to analog ones. During the past several years, digital control continued to improve in cost and usability, which makes digital control more appealing to replace analog control in the near future. The benefits digital control over analog control can be simplified as,

1. The number of components of digital systems is reduced compared with analog controlled systems.
2. Digital components are less susceptible to aging and environmental variations.
3. Digital processing is less sensitive to noise, which can eliminate the distortion of the signal during transmission which is the case for analog controller.
4. Controller function can be changed only by reprograming; there is no need to change the hardware.
5. Digital control is able to realize more complex control processes.

However, there are still some issues associated with digital control. One major issue is the delay introduced by digital control compared to analog way which will be clearly shown later.

Analog controllers work in continuous-time domain, while digital controllers are implemented in discrete-time domain. In real life, most of the signals are analog signals. To implement digital control, certain conversions need to be done between analog and digital signals. Analog to digital conversions are done by sampling with certain frequency. Digital to analog conversions are commonly done by ZOH (zero-order hold). To further explain the conversion between analog and digital signals, the conversion block diagram and the corresponding waveforms are shown in Figure 2-16. The transfer function for ZOH is shown in Equation 2-18 and a 2/T time delay can be observed.

$$G_{ZOH}(s) = \frac{2/T}{s+2/T} \qquad \text{Equation 2-18}$$

Where T is the sample period.

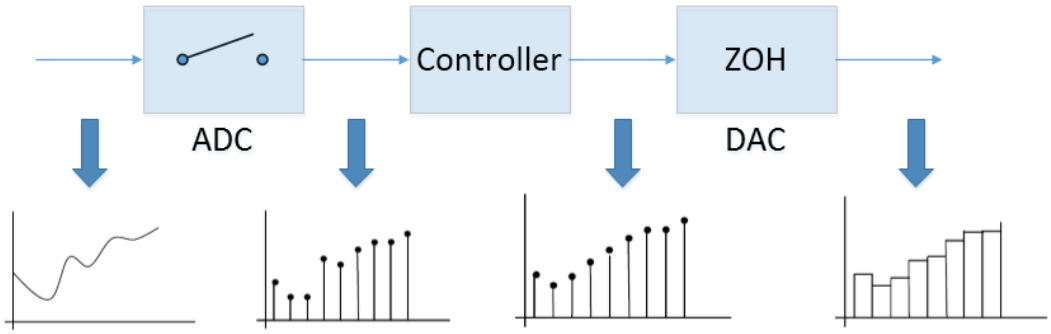


Figure 2-16 Conversion between analog and digital signal

For ADC process, according to Nyquist–Shannon sampling theorem, the condition for the signal to be accurately reconstructed from the samples is that it must have no frequency component greater than half the sample rate[4]. If not, aliasing will happen and the consequence of aliasing on a digital control system can be substantial. As a result, the highest frequency that can be accurately represented by discrete samples is the Nyquist rate which is half the sample rate.

The basic block diagram for the implementation of digital control is shown in Figure 2-17.

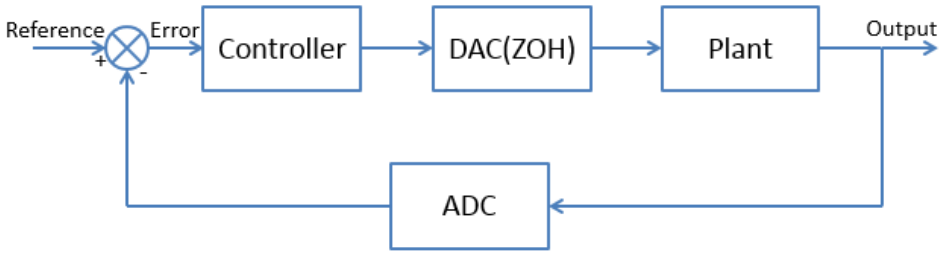


Figure 2-17 Block diagram of digitally controlled system

As mentioned above, there is time delay introduced by digital implementation. This time delay can be from every single part of the digitally controlled system: the sensor, communication, ZOH and also the

computing time of the controller. Normally, ZOH introduces a time delay of half sample period. All the other parts of the system introduce a time delay of one sample period. So in total there is 1.5 sample delay. This time delay results in certain phase lag of the system. The relation between phase lag and frequency is shown in Figure 2-18.

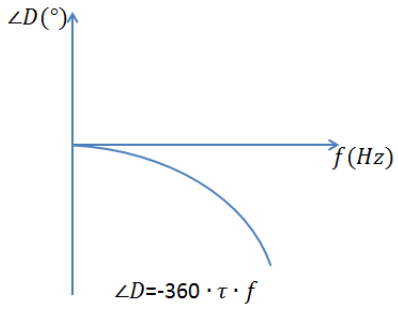


Figure 2-18 Relation between phase lag and frequency (log scale)

Where $\angle D$ is the phase lag, τ is the delay time (normally around 1.5 sample period).

To further show the influence of digital implementation to a system, the open loop Bode plot of a system with the transfer function of $G(s) = s$ for both analog control system and digital control system are shown in Figure 2-19.

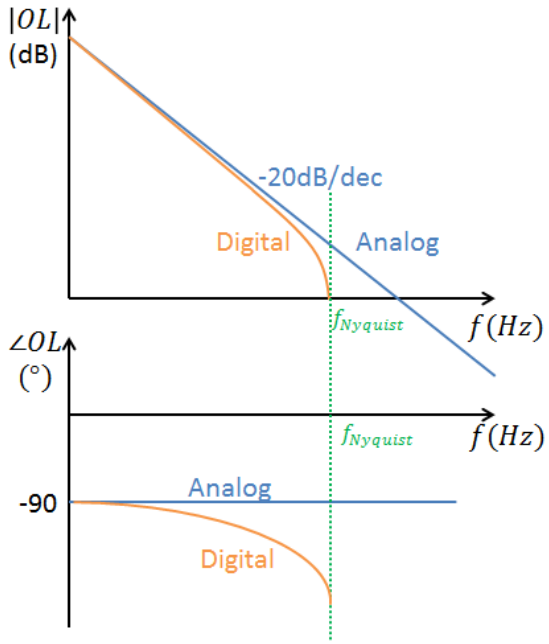


Figure 2-19 Open loop Bode plot for a system with transfer function $\boldsymbol{G(s) = s}$

Chapter 3 Modelling

To analyze the system from control point of view, each part of the system will be modeled in this chapter. The control block diagram for the system is shown in Figure 3-1.

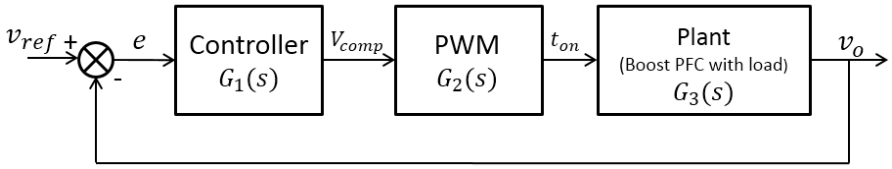


Figure 3-1 System Control Diagram

System open loop transfer function $G(s) = G_1(s)G_2(s)G_3(s)$

3.1 Large-Signal Average Model for Constant On-time Controlled Boost PFC

To inspect system behavior, a simplified averaged large-signal model which averages the circuit over one switching cycle can be used to address most questions[5]. From simulation point of view, averaging makes it much faster than the real switching circuit.

It is assumed that all the components in the boost converter are ideal during the derivation of the large-signal model. The schematic of a boost converter is shown in Figure 24. According to the waveforms drawn in Figure 3-2, the following equations can be achieved.

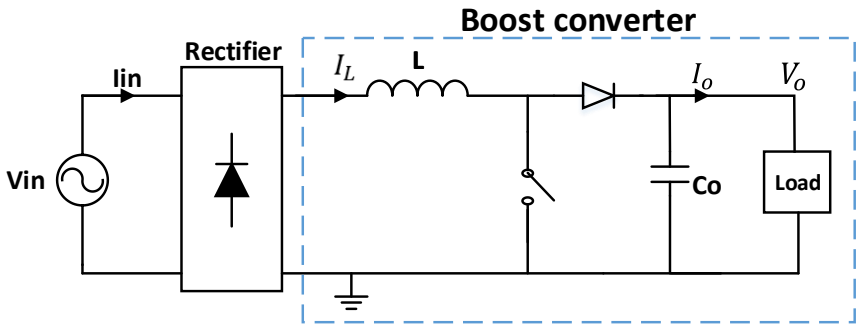


Figure 3-2 Boost topology with controller

The inductor peak current can be written as,

$$\boldsymbol{I_{L,peak} = \frac{V_{g,rms}}{L} \cdot T_{on}} \qquad \text{Equation 3-1}$$

$$\boldsymbol{I_{L,av} = \frac{1}{2} I_{L,peak} = \frac{V_{g,rms}}{2L} \cdot T_{on}} \qquad \text{Equation 3-2}$$

$$\boldsymbol{I_o = (1 - D) I_{L,av} = \frac{V_{g,rms}}{V} \cdot I_{L,av}} \qquad \text{Equation 3-3}$$

Where $I_{L,peak}$ is the peak current of the inductor, $I_{L,av}$ is the average current of the inductor, I_o is the output current, D is the duty cycle, $V_{g,rms}$ is the rectified mains voltage, L is the inductance of the boost converter.

Based on these equations a Simulink large-signal (average) model of a BCM boost converter is shown in Figure 3-3.

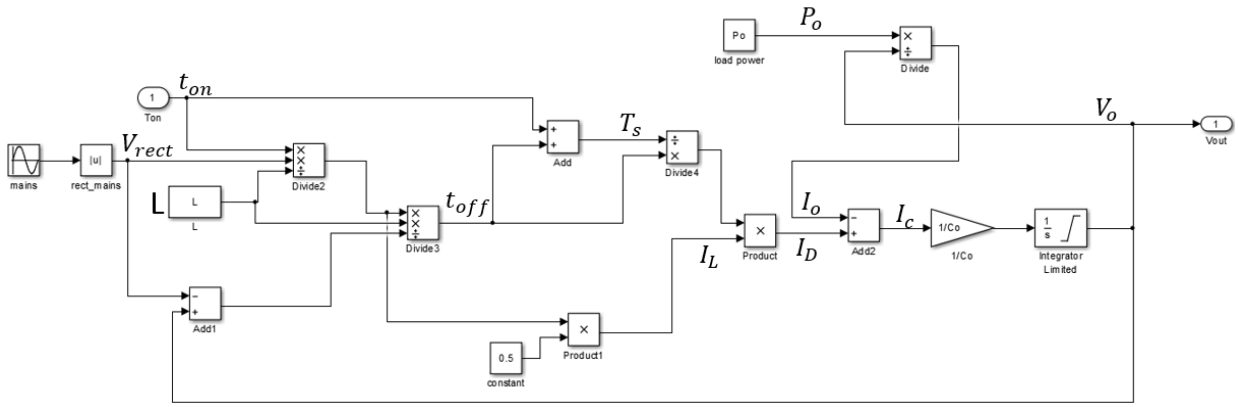


Figure 3-3 large-signal model of boost converter

Simulation can be done much faster with this averaged model to investigate system behavior, but for more precise investigation, a real switching model will be needed.

3.2 Small-Signal Model for PWM

There are many analogue ways to realize the function of PWM. One basic schematic of PWM for constant on-time controlled PFC and its control method is shown in Figure 3-4 & 3-5. In this way a constant on time can be achieved.

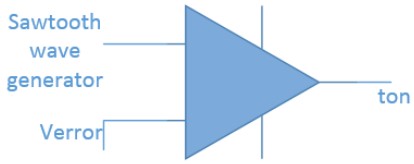


Figure 3-4 Block diagram of PWM for constant on-time control PFC

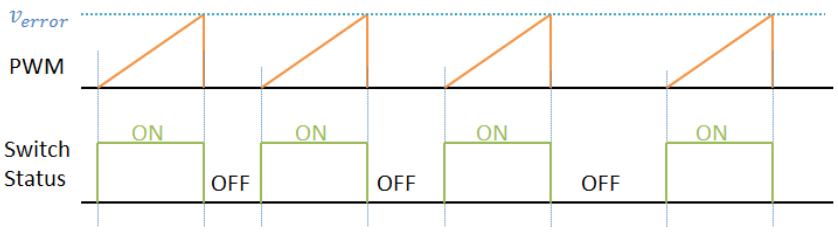


Figure 3-5 PWM

It can be seen from figure 3-5 that the relation between t_{on} and v_{error} is linear. So the transfer function from v_{error} to t_{on} can be simply written as,

$$\boldsymbol{G_2(s) = \frac{\tilde{t}_{on}}{\tilde{v}_{error}} = k} \qquad \text{Equation 3-4}$$

In digital implementation, PWM generator is integrated in the microcontroller so no analogue components are needed.

3.3 Small-Signal Model for Constant On-time Controlled Boost PFC

3.3.1 Loss-free resistor model

Assuming a loss-less system with a unity PF, the PFC including the connected load can be considered as a resistor, so the rectifier input current $i_{ac}(t)$ should be proportional to the applied input voltage $v_{ac}(t)$,

$$\boldsymbol{i_{ac}(t) = \frac{v_{ac}(t)}{R_e}} \qquad \text{Equation 3-5}$$

Where Re is the effective resistance. An equivalent circuit is therefore an effective resistance Re, as shown in figure 3-6. Re simply models how the PFC loads the ac power system. Output regulation is accomplished by variation of the effective resistance Re. The variation of the PFC power can be controlled with Re since the average power can be written as,

$$\boldsymbol{P_{av} = \frac{V_{ac,rms}^2}{Re(vcontrol)}} \qquad \text{Equation 3-6}$$

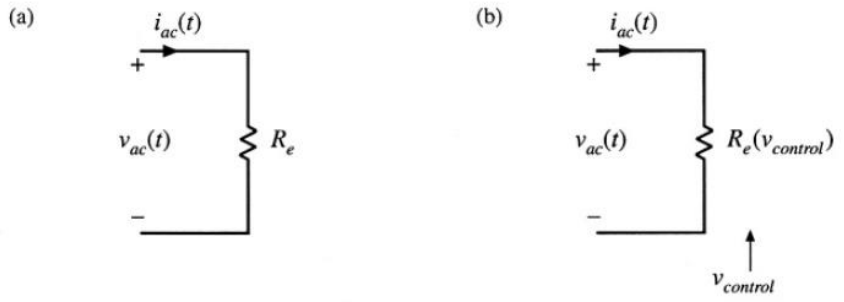


Figure 3-6(a) Equivalent circuit for the ac port of a system with unity power factor (b) the controllable Re

The changing Re results in a time-varying system with generation of harmonics. To avoid generation of significant amounts of harmonics and degradation of the power factor, variations in Re and in the control input must be slow with respect to the ac line frequency.

This model is lossless and contains negligible internal energy storage, the instantaneous power flowing into Re must appear at the rectifier output port. So a two-part model for the unity-power factor single-phase PFC is as shown in figure 3-7.

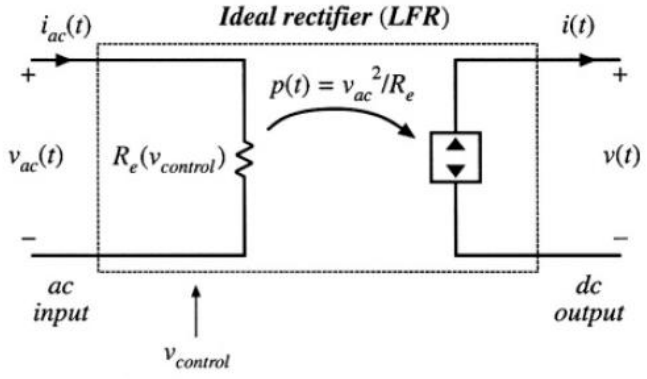


Figure 3-7 Two-part model for the ideal unity-power factor single-phase PFC [6]

This model is called a loss-free resistor (LFR). Then the single-phase ac to dc power supply regulation system LFR model is shown in figure 3-8.

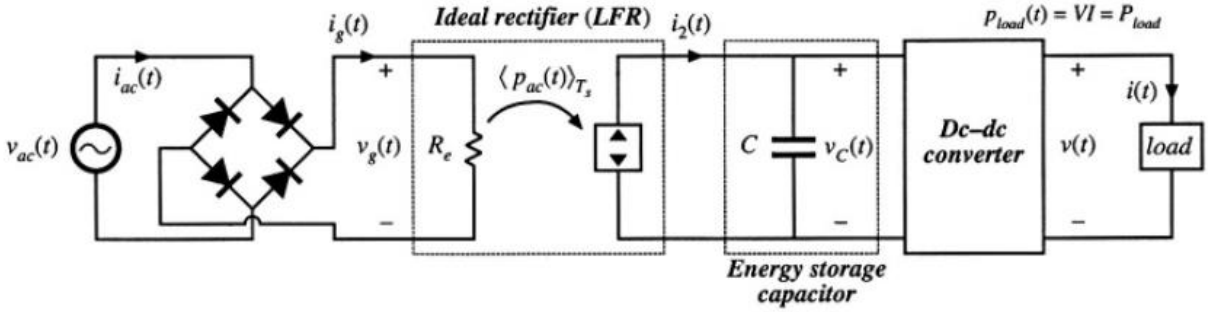


Figure 3-8 LFR model of single-phase ac to dc power supply regulation system [6]

This model is further used in the next section to explain and model the boost converter with a low bandwidth voltage control loop.

3.3.2 Small-signal modelling by averaging over half mains cycle

The voltage-loop controller is realized by varying effective resistance Re to balance the average ac input and dc load powers. Perturbation and linearization of the LFR model can lead to a small-signal equivalent circuit, thus transfer function from the output to the controlled parameter (on time for this case) can then be achieved.

As already explained before, the bandwidth of the voltage feedback control loop must be sufficiently small and cannot try to remove the ripple on the capacitor at double line frequency. Therefore, for the purpose of designing the low-bandwidth voltage control loop, it is necessary to remove all the high frequency behaviors. If it is assumed that the current-loop controller operates ideally at low frequencies, then the low-frequency behaviors of the system can be represented by Figure 3-9(a), where the converter high frequency switching ripple is removed by averaging over one switching period. However, components with frequency lower than the switching frequency but higher than the bandwidth of the control loop, which include the

double line frequency components and dc components of output voltage still exist. It is rather difficult to use this model to design the feedback voltage control loop because it is non-linear and time-varying.

The rectified mains voltage can be written as,

$$\boldsymbol{v_g(t) = \sqrt{2} v_{g,rms} |\sin \omega t|} \qquad \text{Equation 3-7}$$

Where $= 2\pi f_{line}$, f_{line} is the mains frequency.

Average the rectified mains voltage over one switching cycle leads to,

$$\boldsymbol{< v_g(t) >_{T_s} = v_g(t)} \qquad \text{Equation 3-8}$$

Then from the model in Figure 3-12(a), the instantaneous output power over one switching cycle is,

$$\boldsymbol{< p(t) >_{T_s} = \frac{< v_g(t) >_{T_s}{}^2}{R_e(v_{control}(t))} = \frac{v_{g,rms}{}^2}{R_e(v_{control}(t))} (1 - cos\, 2\omega t)} \qquad \text{Equation 3-9}$$

As can be seen from Equation 3-9, the output power consists of two terms, one is a constant term $\frac{v_{g,rms}{}^2}{R_e}$ and another varies at double line frequency. Then the model in Figure 3-9(a) can be separated. The separated model is shown in Figure 3-9(b).

The varying double-line frequency component leads to time-varying system equations. Also, variations in Re lead to an output voltage containing components not only at the frequencies present in $v_{control}(t)$, but also at the even harmonics of the ac line frequency. It is desired to model only the low-frequency components excited by slow variations in $v_{control}(t)$, the load and the ac line voltage. In other words, by assuming the bandwidth of the feedback voltage control loop is far less than double-line frequency in today's PFCs, it is fine to just model the low-frequency behavior of the system for the controller design(low frequency here represents frequency lower than double-line frequency but higher than the bandwidth of the voltage control loop). Then the even harmonics of the ac line frequency can be further removed by averaging over one-half of the ac line cycle.

$$\boldsymbol{T_{2L} = \frac{1}{2} \frac{2\pi}{\omega} = \frac{\pi}{\omega}} \qquad \text{Equation 3-10}$$

Therefore, the system is first averaged over one switching period T_s to remove the switching harmonics, and then averaged again over one-half of the ac line period T_{2L} to remove the even harmonics of the ac line frequency. By averaging the model in Figure 3-9(b) over half main cycle period, the model in Figure 3-9(c) can be achieved. The equivalent in Figure 3-9(c) is time-invariant, but still non-linear. Now perturbation and linearization can be done to develop a linear small-signal model. Assume that the averaged output voltage $< v(t) >_{T_{2L}}$, converter averaged output current $< i_2(t) >_{T_{2L}}$, rms line voltage $v_{g,rms}$ and control voltage $v_{control}(t)$ can be represented as constant values (start with capital letters) plus small slow variations:

$$< \boldsymbol{v_o(t)} >_{T_{2L}} = \boldsymbol{V_o} + \tilde{\boldsymbol{v}}_o(\boldsymbol{t}) \quad \text{Equation 3-11}$$

$$< \boldsymbol{i_2(t)} >_{T_{2L}} = \boldsymbol{I_2} + \tilde{\boldsymbol{i}}_2(\boldsymbol{t}) \quad \text{Equation 3-12}$$

$$\boldsymbol{v_{g,rms}} = \boldsymbol{V_{g,rms}} + \tilde{\boldsymbol{v}}_{g,rms}(\boldsymbol{t}) \quad \text{Equation 3-13}$$

$$\boldsymbol{v_{control}(t)} = \boldsymbol{V_{control}} + \tilde{\boldsymbol{v}}_{control}(\boldsymbol{t}) \quad \text{Equation 3-14}$$

$$\boldsymbol{V_o} \gg \tilde{\boldsymbol{v}}_o(\boldsymbol{t}) \quad \text{Equation 3-15}$$

$$\boldsymbol{I_2} \gg \tilde{\boldsymbol{i}}_2(\boldsymbol{t}) \quad \text{Equation 3-16}$$

$$\boldsymbol{V_{g,rms}} \gg \tilde{\boldsymbol{v}}_{g,rms}(\boldsymbol{t}) \quad \text{Equation 3-17}$$

$$\boldsymbol{V_{control}} \gg \tilde{\boldsymbol{v}}_{control}(\boldsymbol{t}) \quad \text{Equation 3-18}$$

In the averaged model of Figure 3-12(c), $< i_2(t) >_{T_{2L}}$ can be written as equation 3-19.

$$< i_2(t) >_{T_{2L}} = \frac{< p(t) >_{T_{2L}}}{< v(t) >_{T_{2L}}} = \frac{{v_{g,rms}}^2(t)}{R_e\left(v_{control}(t)\right) < v_o(t) >_{T_{2L}}}$$

$$= \boldsymbol{f}\left(\boldsymbol{v_{g,rms}(t)}, < \boldsymbol{v_o(t)} >_{T_{2L}}, \boldsymbol{v_{control}(t)}\right) \quad \text{Equation 3-19}$$

Expansion of Equation 3-23 and elimination of higher-order nonlinear components leads to equation 3-20.

$$\boldsymbol{R_e(V_{control})V_o\tilde{i}_2(t) = 2V_{g,rms}\tilde{v}_{g,rms}(t) - I_2VR_e(\tilde{v}_{control}(t)) - I_2R_e(V_{control})\tilde{v}_{control}(t) + {V_{g,rms}}^2 - I_2R_e(V_{control})V}$$
Equation 3-20

After averaging over half mains cycle, the input power and the output power are equal, which is shown in equation 3-21.

$$\frac{{\boldsymbol{V_{g,rms}}}^2}{\boldsymbol{R_e(V_{control})}} = \boldsymbol{I_2V_o} \quad \text{Equation 3-21}$$

Combination of equation 3-20 & 3-21 leads to equation 3-22.

$$\tilde{\boldsymbol{i}}_2(\boldsymbol{t}) = \boldsymbol{g_2}\tilde{\boldsymbol{v}}_{g,rms}(\boldsymbol{t}) + \boldsymbol{j_2}\tilde{\boldsymbol{v}}_{control}(\boldsymbol{t}) - \frac{\tilde{v}_o(t)}{r_2} \quad \text{Equation 3-22}$$

Where,

$$\boldsymbol{g_2} = \left.\frac{df(v_{g,rms},V_o,V_{control})}{dv_{g,rms}}\right|_{v_{g,rms}=V_{g,rms}} = \frac{2}{R_e(V_{control})}\frac{V_{g,rms}}{V_o} \quad \text{Equation 3-23}$$

$$\left(-\frac{1}{r_2}\right) = \left.\frac{df(V_{g,rms},<v_o>_{T_{2L}},V_{control})}{d<v_o>_{T_{2L}}}\right|_{<v_o>_{T_{2L}}=V_o} = -\frac{I_2}{V_o} \quad \text{Equation 3-24}$$

$$j_2 = \left.\frac{df(V_{g,rms},V_o,v_{control})}{dv_{control}}\right|_{v_{control}=V_{control}} = -\left.\frac{V_{g,rms}^2}{V_o R_e^2}\frac{dR_e(v_{control})}{dv_{control}}\right|_{v_{control}=V_{control}}$$ Equation 3-25

A small-signal model based on equation 3-22 is shown in Figure 3-9(d).

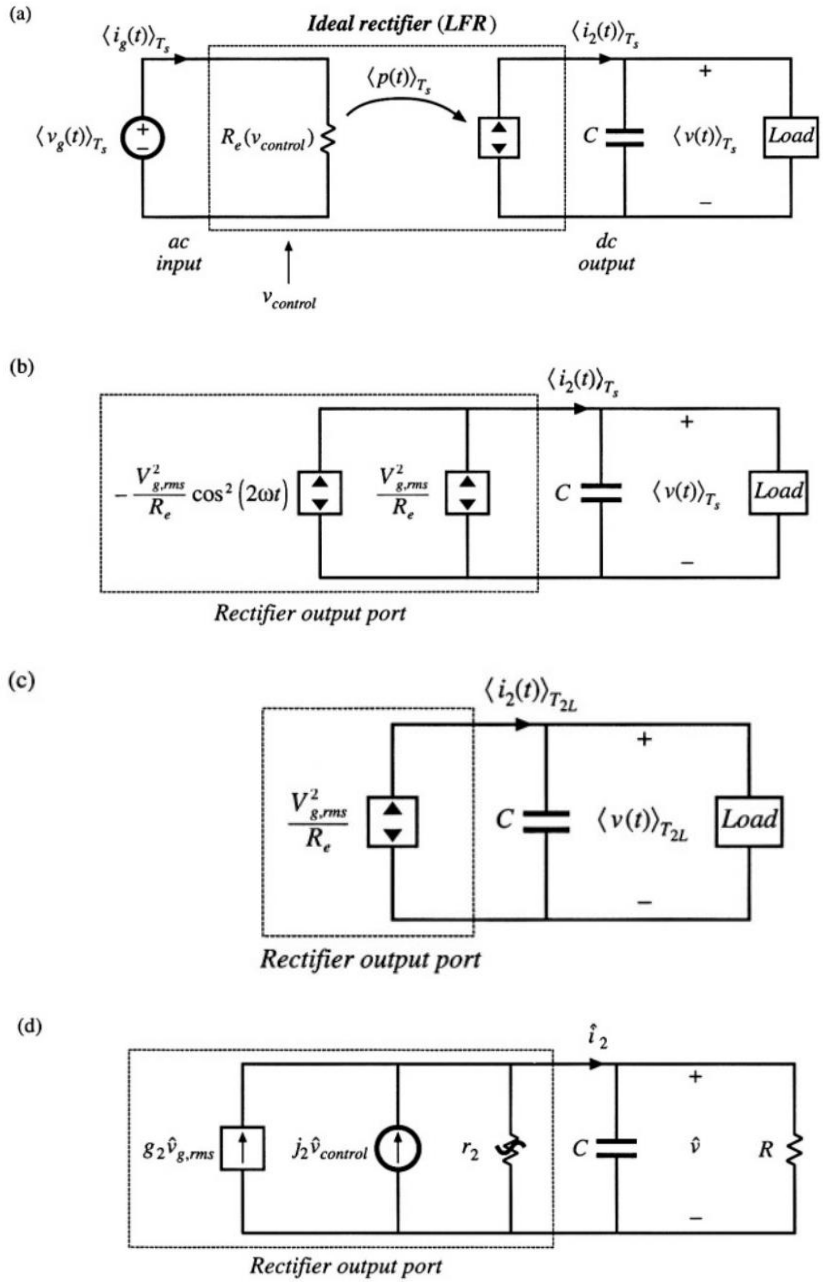


Figure 3-9 (a) large-signal LFR model, averaged over one switching cycle T_s (b) separation of power source into its constant and time-varying components (c) removal of double-line frequency components by averaging over one-half of the ac line period T_{2L} (d) small-signal model obtained by perturbation and linearization of 3-9(c) [6]

For a boost constant on-time controlled converter operating under BCM, equation 3-26 to 3-28 can be written.

$$v_{control} = t_{on} \quad \text{Equation 3-26}$$

$$R_e(V_{control}) = \frac{{V_{g,rms}}^2}{P_{av}} \quad \text{Equation 3-27}$$

$$\frac{dR_e(v_{control})}{dv_{control}} = -\frac{R_e(V_{control})}{T_{on}} \quad \text{Equation 3-28}$$

Then the control-to-output transfer function can be written as equation 3-29.

$$\frac{\tilde{v}_o(s)}{\tilde{t}_{on}(s)} = j_2 R \| r_2 \frac{1}{1+sCR\|r_2} \quad \text{Equation 3-29}$$

Where C is the output capacitor, R is the equivalent load resistance, r_2 is the effective resistance of the ac power source, P_{av} is the averaged ac input power. For different kinds of loads, the equivalent load resistances R are different.

For resistive load, the average ac input power and the dc output power are the same, which means $R = r_2$, according to Figure 3-9(d). For constant power load, the load behaves as a negative resistor since voltage is inversely proportional to current. Then the equivalent load resistance $R = -r_2$. For constant current load, R can be considered infinite. The corresponding curves of different loads are shown in Figure 3-10.

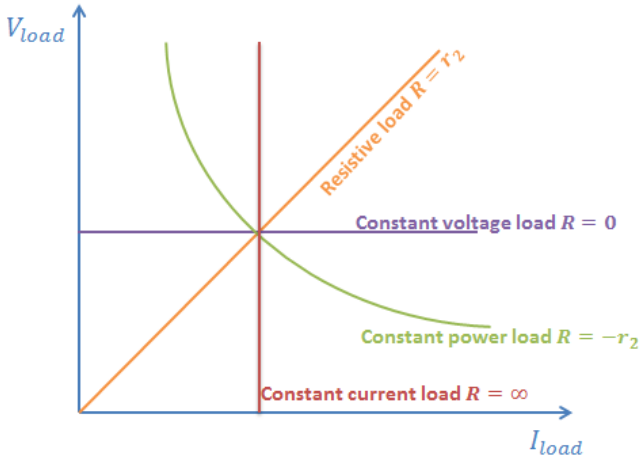


Figure 3-10 I-V curves of different loads

Then the transfer function from on time to output can be written as,

$$\frac{\tilde{v}_o(s)}{\tilde{t}_{on}(s)} = \begin{cases} \frac{P_{av}}{V_o T_{on}} \cdot \frac{1}{2} \cdot \frac{\frac{R}{2}}{1+\frac{RC_o}{2}s} & (\boldsymbol{resistive\ load}) \\ \frac{P_{av}}{V_o T_{on}} \cdot \frac{1}{C_o s} & (\boldsymbol{constant\ power\ load}) \\ \frac{P_{av}}{V_o T_{on}} \frac{r_2}{1+C_o r_2 s} & (\boldsymbol{constant\ current\ load}) \end{cases}$$

Equation 3-30

Where $\frac{P_{av}}{VT_{on}} = \frac{1}{2L}\frac{{V_{g,rms}}^2}{V}$, $T_{on} = \frac{2P_{av}L}{{V_{g,rms}}^2}$, L, is the inductance of boost converter, C_o is the output capacitance.

3.3.3 Small-signal verification for system with higher bandwidth

The small-signal model that is derived in last section is under the assumption of a system with a bandwidth much lower than double line frequency. For system with a conventional controller which has a bandwidth of 10Hz- 20Hz, this model will definitely fit. However, for systems with a much higher bandwidth that are going to be discussed in details in later sections, this small-signal model is no longer guaranteed to be valid. To further check the applicability, the 'transfer function estimation' function in Simulink can be used.

First of all an on-time controlled boost converter is built up in Simulink. Then define the system input as the on time of the switch, output as the output voltage of the boost converter. By using 'tfe' function in Simulink, small variations with different frequencies are applied to the on time of the switch and the corresponding variations of the output voltage can be achieved. By relating the variations of the input and output for every tested frequency, the transfer function of the boost converter can be estimated.

To make sure the double line frequency component in the output voltage does not affect the accuracy of the transfer function estimation, especially for input variations that has a higher frequency than double line frequency, the identification period t should satisfy equation.

$$\boldsymbol{t = k_1 \frac{1}{f_1} = k_2 \frac{1}{2f_{mains}}}$$

Equation 3-31

Where f_1 is the frequency of the applied variation in the on time of the switch, f_{mains} is the frequency of the mains, $k_1$and k_2 should both be integers.

Consider a system with 230V RMS sinusoidal input, 200W output, 200µH inductor, 220µF output capacitor, the plant (boost converter) amplitude bode plots with both Simulink estimation and previously derivation are shown in Figure 3-11.

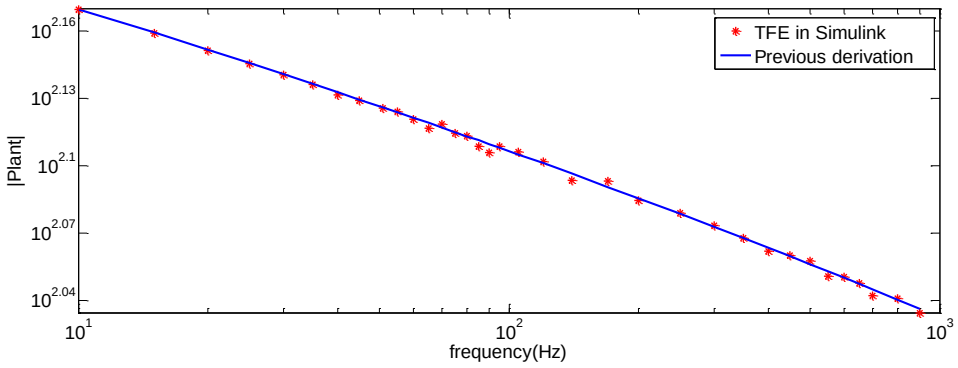


Figure 3-11 the plant (boost converter) amplitude bode plots with both Simulink estimation and previously derivation (for bandwidth much lower than double line frequency)

As can be seen from Figure 3-11, the small-signal model that is derived in the previous section is not only valid for a system with a bandwidth far lower than double line frequency, but also valid for a wider range of frequency.

3.4 Summary

In this chapter, the large signal model of the BCM boost PFC is built up for faster simulation. Small-signal model and the corresponding transfer function for each part of the voltage control loop is derived.

The control block diagram for the system is shown in Figure 3-12.

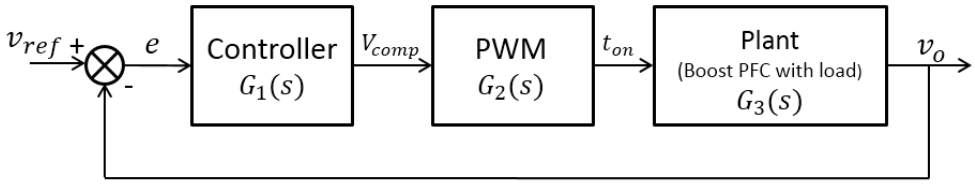


Figure 3-12 System Control Diagram

System open loop transfer function $G(s) = G_1(s)G_2(s)G_3(s)$

Generally, the system is controlled with a PI controller, the transfer function is written in equation 3-32.

$$\boldsymbol{G_c(s) = k \cdot \frac{s+a}{s}} \qquad \text{Equation 3-32}$$

The transfer function for PWM and the plant that are derived in this chapter can be written as equation 3-33 and 3-34.

$$\boldsymbol{G_2(s) = \frac{\tilde{t}_{on}}{\tilde{v}_{comp}} = k} \qquad \text{Equation 3-33}$$

$$\boldsymbol{G_3(s)} = \frac{\tilde{v}_o(s)}{\tilde{t}_{on}(s)} = \begin{cases} \dfrac{\boldsymbol{P_{av}}}{\boldsymbol{V_o T_{on}}} \cdot \dfrac{\mathbf{1}}{\mathbf{2}} \cdot \dfrac{\frac{\boldsymbol{R}}{\mathbf{2}}}{\mathbf{1}+\frac{\boldsymbol{RC_o}}{\mathbf{2}}\boldsymbol{s}} & (\boldsymbol{resistive\ load}) \\ \dfrac{\boldsymbol{P_{av}}}{\boldsymbol{V_o T_{on}}} \cdot \dfrac{\mathbf{1}}{\boldsymbol{C_o s}} & (\boldsymbol{constant\ power\ load}) \\ \dfrac{\boldsymbol{P_{av}}}{\boldsymbol{V_o T_{on}}} \dfrac{\boldsymbol{r_2}}{\mathbf{1}+\boldsymbol{C_o r_2 s}} & (\boldsymbol{constant\ current\ load}) \end{cases} \qquad \text{Equation 3-34}$$

Where $\frac{P_{av}}{V_o T_{on}} = \frac{1}{2L}\frac{{V_{g,rms}}^2}{V}$,$T_{on} = \frac{2P_{av}L}{{V_{g,rms}}^2}$ L is the inductance of boost converter, C_o is the output capacitance.

Chapter 4 System specification and Conventional Controller Design

4.1 System Specification

All the design in this report is based on a lossless 36W constant on-time controlled BCM boost PFC. The inductor value is 2.7mH, the output capacitor is $10\mu F$. Mains Voltage is a sinusoidal AC voltage with a RMS value of 230V, the output voltage of the boost PFC is 410V. The load type of the boost PFC can be considered as constant power load since the PFC is connected to an output stage which is a converter driving LED load. Sampling frequency of the output voltage is chosen to be 1kHz to match the sample frequency of the existing product.

With the nominal output power $P_o = 36W$ and output voltage $V_o = 410V$, output current can be written as equation 4-1.

$$\boldsymbol{I_o = \frac{P_o}{V_0} = 87.8mA} \qquad \text{Equation 4-1}$$

Inductor current can be divided into two integrals: one is rising current when MOSFET is on and the other is output diode current when MOSFET is off, as shown in Figure 4-1.

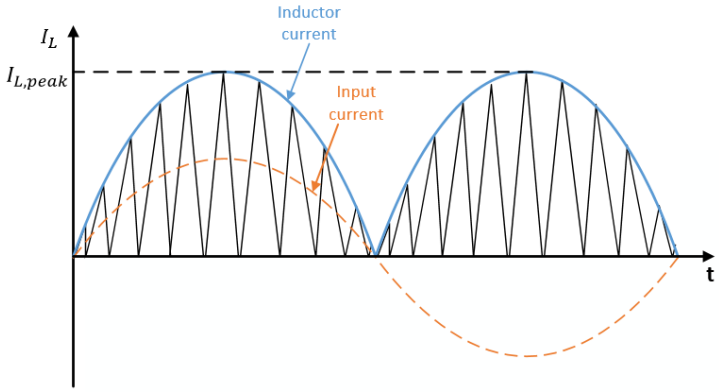


Figure 4-1 Inductor and input current

Because switching frequency ($\geq 35kHz$) is much higher than line frequency (50Hz), input current can be assumed to be constant during a switching period. With 230V RMS line voltage, the maximum inductor current then can be calculated as,

$$\boldsymbol{I_{L,peak} = \frac{2\sqrt{2}P_o}{V_{line,rms}} = 443mA} \qquad \text{Equation 4-2}$$

The maximum peak input current is,

$$\boldsymbol{I_{in,peak} = \frac{1}{2}I_{L,peak} = 221.5mA} \qquad \text{Equation 4-3}$$

The RMS value of the input current is,

$$\boldsymbol{I_{in,rms} = \frac{I_{in,peak}}{\sqrt{2}} = 157mA} \qquad \text{Equation 4-4}$$

Table 4-1 shows the specifications for the system.

Boost Inductor L	2.7mH
Output Capacitor C_o	$10\mu F$
Line Frequency f_{line}	50Hz
Line RMS Voltage $V_{line,rms}$	230V
Output Power P_o	36W
Output Voltage V_o	410V
Output Current I_o	87.8mA
Inductor Peak Current $I_{L,peak}$	443mA
Input Peak Current $I_{in,peak}$	221.5mA
Input RMS Current $I_{in,rms}$	157mA
V_o Sampling Frequency	1kHz
Load type	Constant power load

Table 4-1 System Specifications

4.2 Design Specification

According to design guidelines, after design system should meet the following requirements:

1. System open loop should give at least 20dB suppression at double line frequency (100Hz) to ensure THD performance of the system.
2. At least 30 degrees phase margin
3. At least 6dB gain margin

All designs in this report are according to this design specification.

4.3 Conventional Feedback Loop Controller Design and Simulation

4.3.1 Conventional feedback loop controller design

Since the transfer function of PWM is just a pure gain as derived in section 3.3, in further design, PWM can be considered a part of the controller gain. Then the system control block diagram can be drawn with a controller and a plant as shown in Figure 4-2.

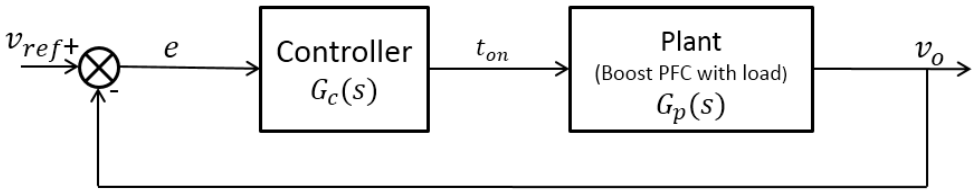


Figure 4-2 Control block diagram

As derived in chapter 3, for constant power load, the transfer function of the plant is,

$$\boldsymbol{G_p(s) = \frac{1}{2L} \cdot \frac{{V_{line,rms}}^2}{V_o} \cdot \frac{1}{sC}} \quad \text{Equation 4-5}$$

With $V_{line,rms} = 230V, L = 2.7mH, V_o = 410V, C = 10\mu F$,

$$\boldsymbol{G_p(s) = \frac{2.389\times10^9}{s}} \quad \text{Equation 4-6}$$

The transfer function of a PI controller can be written as,

$$\boldsymbol{G_c(s) = k \cdot \frac{s+a}{s}} \quad \text{Equation 4-7}$$

Then the system open loop is,

$$\boldsymbol{G_{ol}(s) = G_c(s) \cdot G_p(s) = k \cdot \frac{s+a}{s} \cdot \frac{2.389\times10^9}{s}} \quad \text{Equation 4-8}$$

As stated before, according to design guidelines, to ensure THD performance, system should have at least 20dB suppression at 100Hz. If 20dB suppression at 100Hz is chosen, the system bandwidth is then 10Hz (open-loop gain is with -20dB/dec slop from 10Hz to 100Hz). Take $s = j\omega = j \cdot 10 \cdot 2\pi$, the system open-loop transfer function can then be written as equation 4-9.

$$\boldsymbol{G_{ol}(s) = G_c(s) \cdot G_p(s) = \frac{j\cdot2\pi\cdot10+a}{j\cdot2\pi\cdot10} \cdot \frac{2.389\times10^9}{j\cdot2\pi\cdot10} = 1} \quad \text{Equation 4-9}$$

If the zero is put too close to the origin, the system will have a very long rise time. According to the rule of thumb, breakpoint should be set at 1/3 of bandwidth, which determines the zero position as shown in equation 4-10.

$$\boldsymbol{a = \frac{1}{3} \cdot 10 \cdot 2\pi \approx 7\pi} \quad \text{Equation 4-10}$$

Then k can be calculated as,

$$\boldsymbol{k = 2.48 \times 10^{-8}} \quad \text{Equation 4-11}$$

After design, the controller transfer function is shown in Equation 4-12.

$$G_c(s) = 2.48 \times 10^{-8} \cdot \frac{(s+7\pi)}{s} \qquad \text{Equation 4-12}$$

The system open-loop transfer function is,

$$G_{ol}(s) = G_c(s) \cdot G_p(s) = 2.48 \times 10^{-8} \cdot \frac{(s+7\pi)}{s} \cdot \frac{2.389 \times 10^9}{s} \qquad \text{Equation 4-13}$$

The open-loop block diagram and bode plot of system with 1kHz sampling frequency and 10Hz bandwidth as designed above are shown in figure 4-3 and 4-4. ZOH block in figure 4-3 represents for the sampling of the system, after sampling the discrete signal is then automatically converted to continuous signal to fit in the s-domain transfer function in Simulink.

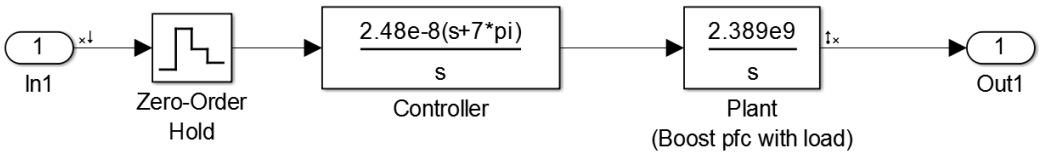


Figure 4-3 System Open-loop control block diagram with conventional controller

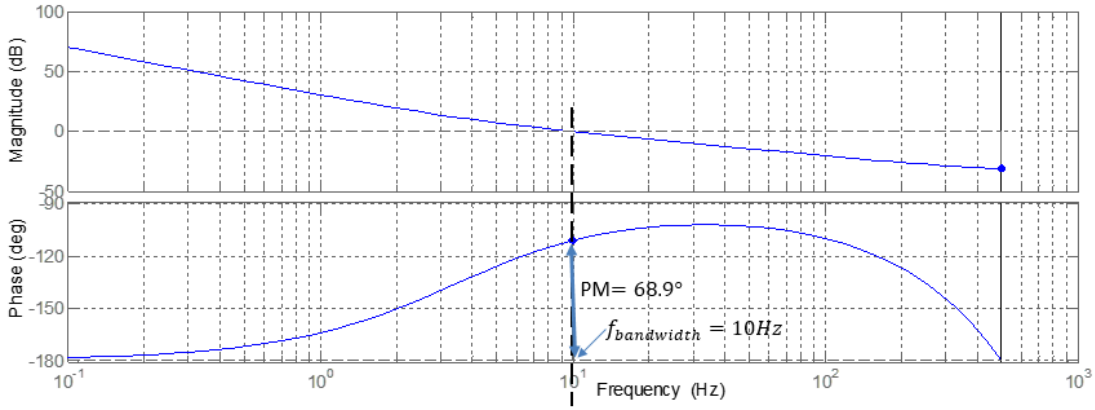


Figure 4-4 System Open-loop bode plot with conventional controller

From the bode plot, a 68.9 degrees phase margin and 10Hz bandwidth can be seen. At 100Hz, system open-loop gain is -20dB.

All the designs in later chapters are compared with this 10Hz bandwidth system which is controlled with a PI controller. This controller is referred as system with conventional controller in later chapters.

4.3.2 Simulation

Based on the large-signal (average) model that is built up in section 3.1, Simulink setup for the system is shown in Figure 4-5.

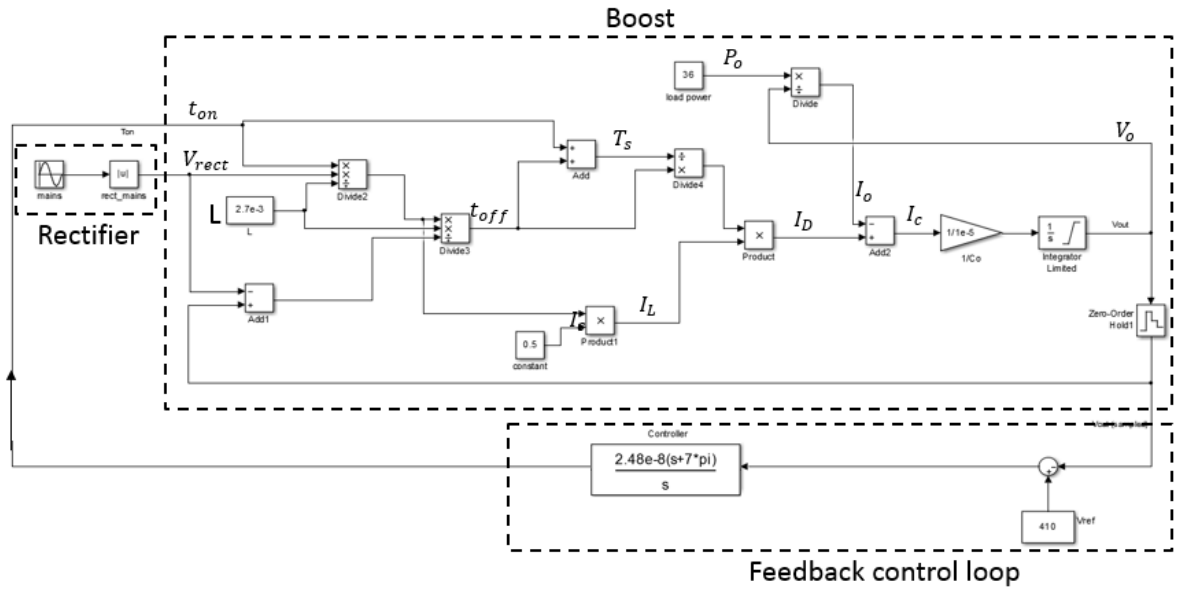


Figure 4-5 Simulink model for system with conventional controller

Under steady state operation, THD of the system is 4.75%.

To observe the dynamic response of this system, certain kinds of disturbances need to be applied to the system. Two main disturbance sources can be considered as disturbances from mains and load. For disturbance from mains side, the amplitude change can represent most of the cases. A $\pm 10\%$ variation in amplitude can be expected. In Netherlands the mains RMS voltage is 230V, with $\pm 10\%$ variation the mains voltage varies from 207V to 253V. For disturbance from the load side, a load change from full load to 10% load can be considered, which is from 36W to 3.6W. In the simulation the disturbances are modeled as step to represent the worst case.

The output voltage waveforms after applying mains amplitude change 207V-253V-207V and load change 36W-3.6W-36W at time t=0.2s and t=0.4s are shown in figure 4-6 and 4-7.

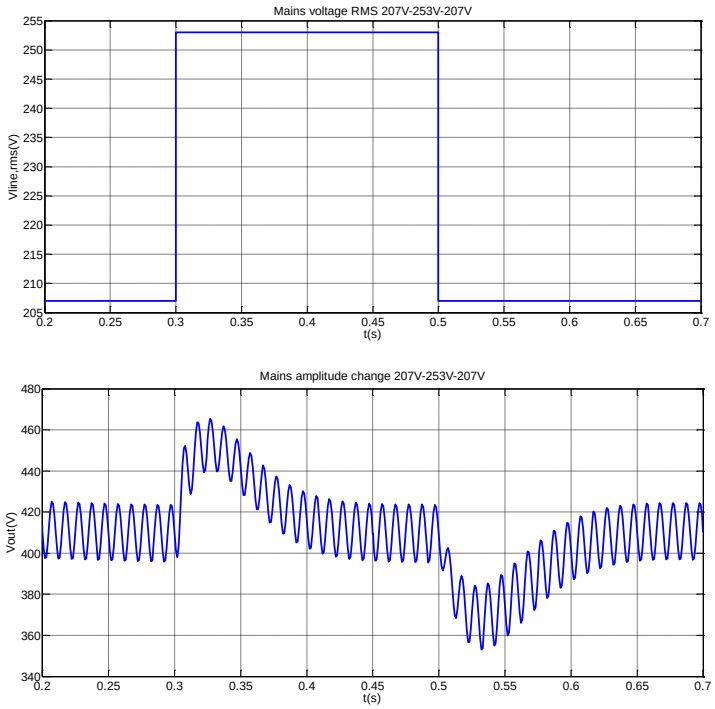


Figure 4-6 Output voltage response to mains amplitude change 207V-253V-207V

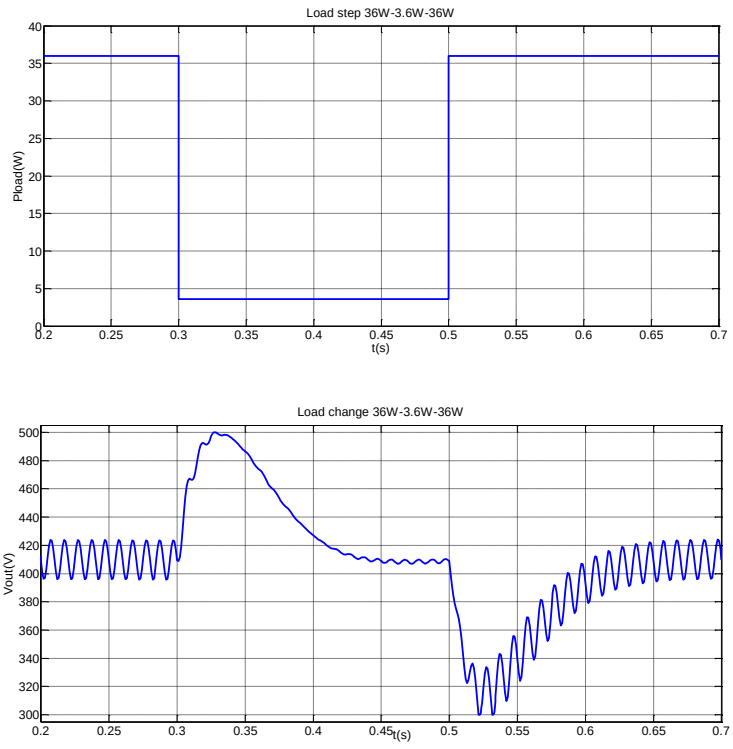


Figure 4-7 Output voltage response to load change 36W-3.6W-36W

4.4 Summary

In this chapter, the system is defined and a feedback controller is designed which achieves 10Hz bandwidth. Based on the defined system and controller, a simulation model is built up in Simulink. The simulation results for dynamic response to mains and load disturbances and the steady state THD performance are all presented for further comparisons with the novel controllers.

Chapter 5 Novel Controllers Design

Several solutions have been proposed to improve the dynamic response of a boost PFC. These solutions are based on 3 basic ideas [7]:

1. Ripple cancellation (The removal of the 2nd harmonic from signal that is fed into the controller)
2. Load current and/or input voltage feed-forward
3. Regulation band (variable gain)

Three solutions based on the three ideas above will be discussed in details in this chapter.

5.1 Ripple Cancellation

The output voltage of the boost PFC contains a double-line frequency ripple, which can be written as,

$$\Delta V \approx \left|\frac{I_o}{C_o \omega_{line}} \sin 2\omega_{line} t\right| = \left|\frac{P_o}{V_o C_o \omega_{line}} \sin 2\omega_{line} t\right| \qquad \text{Equation 5-1}$$

Based on the system specified in chapter 4, the peak to peak voltage ripple is,

$$\Delta V_{p-p} = \left|\frac{36}{410 \cdot 10 \cdot 10^{-6} \cdot 2\pi \cdot 50}\right| = 28V \qquad \text{Equation 5-2}$$

The output voltage waveform under steady state operation is shown in Figure 5-1.

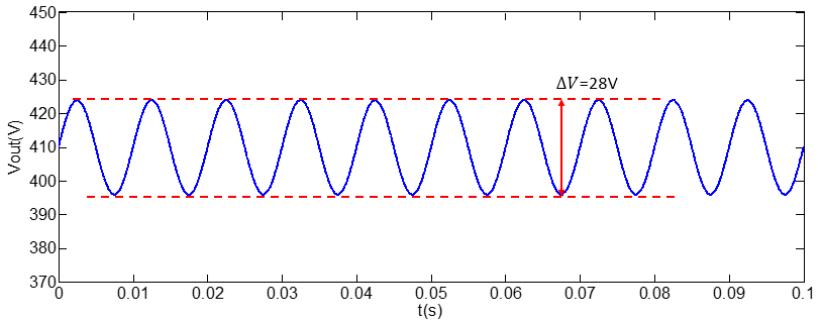


Figure 5-1 Output voltage waveform

As explained before, if the controller tries to remove the ripple on the output voltage, the input current will be distorted and thus result in a bad THD. The idea of ripple cancellation is to eliminate the 2nd harmonic component from the controller input, so the controller can be fed with a ripple free signal, then the bandwidth of the system can be increased. Based on ripple cancellation, 2 possible solutions are proposed: the use of a digital notch/comb filter [8], [9] and output voltage ripple compensation [10]. The use of a digital notch/comb filter can suppress the double-line frequency component, while the solution of output voltage ripple compensation is to extract the voltage ripple from the output voltage by doing calculation based on the circuit operating principle. However, for ripple compensation, the extraction of the output voltage ripple is realized by calculation using the measured values from the circuit. The calculation is only valid under the assumption of a pure sinusoidal mains input voltage. As a result, in practical implementation

the accuracy of the ripple extraction is a big issue which can lead to a bad THD performance. Therefore, ripple compensation will not be discussed in detail in this report, while the use of a digital filter will be discussed in detail in this section.

The control block diagram after applying a digital filter is shown in Figure 5-2.

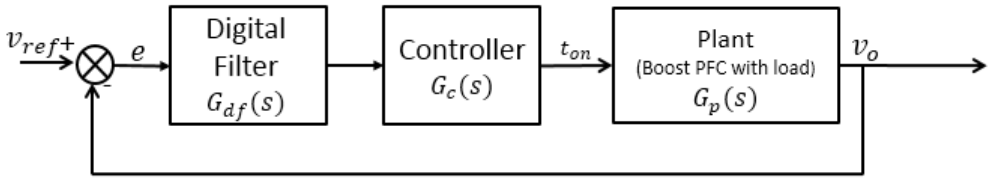


Figure 5-2 Control block diagram with a digital filter

Compared to an analogue filter, the implementation of a digital filter can be implemented without any additional hardware. Analogue filters are sensitive to component tolerances, requiring expensive components that are susceptible to thermal drift. However, digital filters will only be susceptible to the clock and timing drift. The filter coefficients need to be adapted to the actual operating line frequency for maximum performance, which is very difficult to implement in analogue way.

In the next two sections, notch filter and comb filter will be discussed in more detail as digital filter for double mains frequency on output filter capacitor.

5.1.1 Notch Filter

1. Design

An ideal notch filter can provide infinite attenuation at center frequency and unity gain at all other frequencies. Therefore, an ideal notch filter frequency response can be expressed as:

$$|\boldsymbol{G_{nf}(s)}| = \begin{cases} \boldsymbol{0} & \boldsymbol{center\ frequency} \\ \boldsymbol{1} & \boldsymbol{other\ frequencies} \end{cases} \qquad \text{Equation 5-3}$$

However, during implementation a filter can never behave as an ideal one. It will not be able to give infinite attenuation, also amplitude and phase change will take place at non-center frequencies. The transfer function of a notch filter is shown in Equation 5-4.

$$\boldsymbol{G_{nf}(s)} = \frac{\boldsymbol{s^2+2\xi_1\omega_o s+{\omega_o}^2}}{\boldsymbol{s^2+2\xi_2\omega_o s+{\omega_o}^2}} \qquad \text{Equation 5-4}$$

Where ξ_1/ξ_2 determines the attenuation of center frequency (damping) and the phase shift brought by the filter, ξ_2 determines the width of the attenuation curve, ω_o is the center frequency.

As mentioned before, to ensure good PF, system open loop should give at least 20dB suppression at 100Hz. More suppression will lead to better PF. However too large suppression is hard to achieve in real implementation. In this case, consider a notch filter with 30dB suppression at 100Hz,

$$\mathbf{20log}(\xi_1/\xi_2) = -\mathbf{30} \qquad \text{Equation 5-5}$$

Take ξ_2 equals 100, then according to equation 5-5, ξ_1 equals 3.16.

The transfer function of the above designed notch filter is shown in equation 5-6.

$$\boldsymbol{G_{nf}(s) = \frac{s^2+3.16s+(200\pi)^2}{s^2+100s+(200\pi)^2}} \qquad \text{Equation 5-6}$$

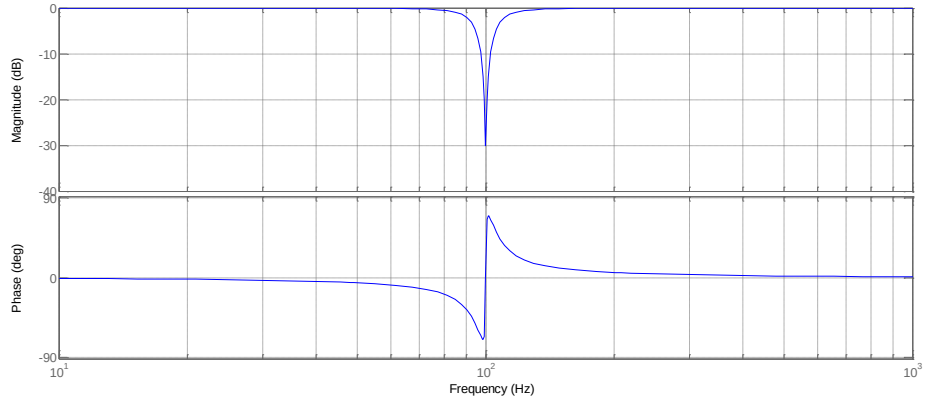


Figure 5-3 Bode plot of the notch filter

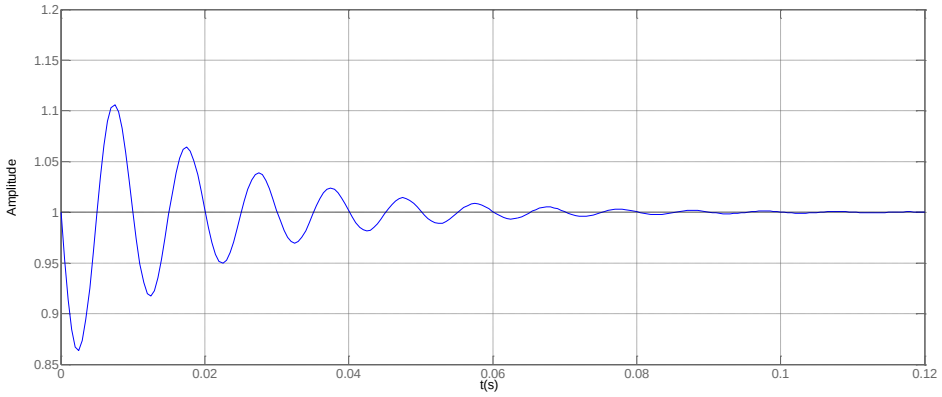


Figure 5-4 Step response of the notch filter

As can be seen from figure 5-3 and 5-4, the notch filter gives -30dB attenuation and 70 degrees phase shift at the notch frequency, the settling time of the filter is 0.06s.

As derived before, the plant transfer function is,

$$\boldsymbol{G_p(s) = \frac{2.389\times10^9}{s}} \qquad \text{Equation 5-7}$$

For a system with 90Hz bandwidth, the design procedure is the same as that is shown in section 4.3. After design, the PI controller is shown in equation 5-8.

$$G_c(s) = 2.67 \times 10^{-7} \cdot \frac{s+10\pi}{s} \qquad \text{Equation 5-8}$$

The system open-loop block diagram is shown in figure 5-5. The open-loop bode plot of the system is shown in figure 5-6.

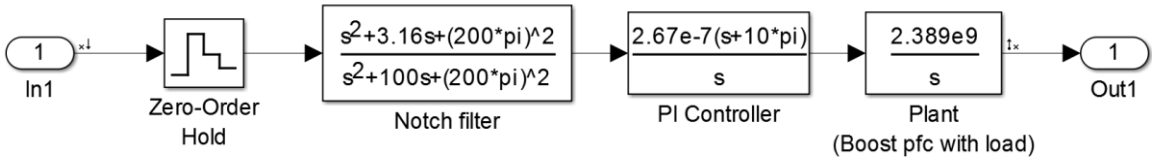


Figure 5-5 90Hz system open loop block diagram

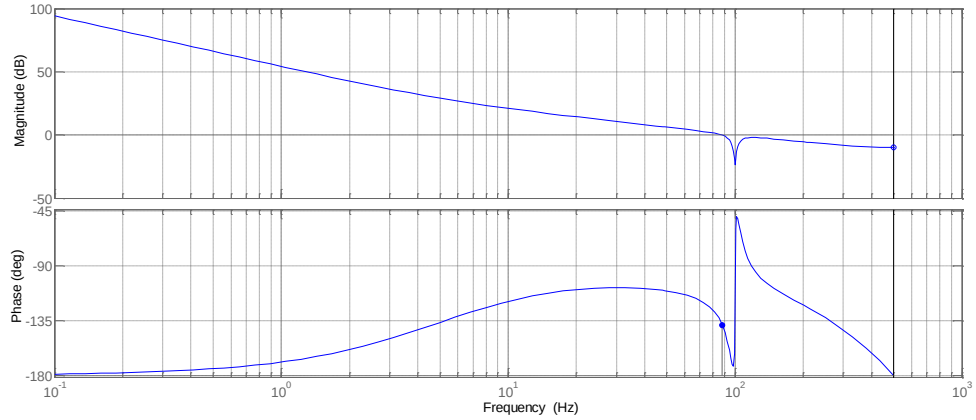


Figure 5-6 System open loop bode plot

As can be seen from the bode plot, system has a bandwidth of 90Hz and a phase margin of 42 degrees. At 100Hz, system gives 24dB suppression.

Because the input voltage RMS value has impact on the transfer function, to ensure the system transient behavior when there is mains RMS change, the system stability at the maximum and minimum mains voltage needs to be taken into account. As defined before, $\pm 10\%$ of amplitude variation can be expected from the mains. In this case, for a 230V mains input, the minimum value is 207V and the maximum value is 253V. Then the plant transfer function under minimum and maximum mains input can be written as Equation 5-12 and 5-13.

$$\boldsymbol{G_{p\_min}(s) = \frac{1.935\times10^9}{s}} \qquad \text{Equation 5-9}$$

$$\boldsymbol{G_{p\_max}(s) = \frac{2.823\times10^9}{s}} \qquad \text{Equation 5-10}$$

After doing the linear analysis and drawing the bode plots of systems with the minimum and maximum mains input, with the minimum input the system gives 54.8 degrees phase margin (79Hz BW), with the maximum input the system gives 32 degrees phase margin (94Hz BW). So under both minimum and maximum mains input, the system is always stable.

Further increase in the controller gain k will lead to higher bandwidth. However, with 70 degrees phase shift brought by the notch filter at 100Hz, it is hard to guarantee a good phase margin when the bandwidth is increased above 100Hz. Moreover, further increase in bandwidth will lead to less suppression at 100Hz, which will further cause bad THD performance. The Nyquist plots and bode plots for system with 130Hz bandwidth and 200Hz bandwidth is shown in figure 5-7 and 5-8.

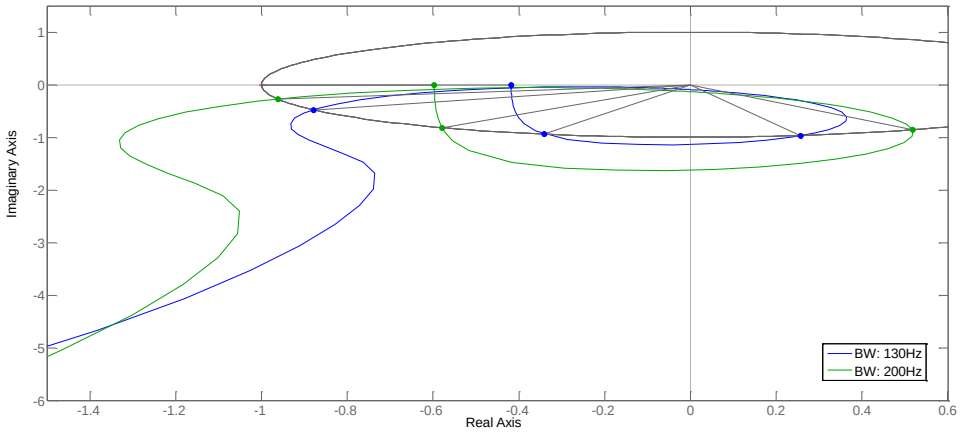


Figure 5-7 Nyquist Plots for system with 130Hz bandwidth and 200Hz bandwidth

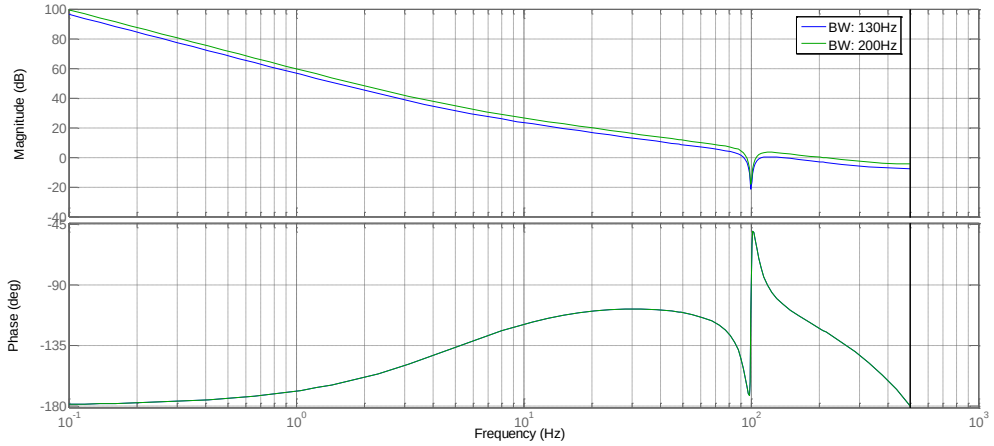


Figure 5-8 System open-loop bode plots for system with 130Hz BW and 200Hz BW

The 0dB crossing points around 100Hz are the most critical ones since they have the minimum phase margin as shown in figure 5-7. For system with 130Hz bandwidth, at 96.1Hz the system open loop equals 0, the

phase margin is 28.5 degrees (<30 degrees). For system with 200Hz bandwidth, at 97.7Hz the system open loop equals 0, phase margin is 16.5 degrees (<30 degrees). Further increase in bandwidth will result in even less phase margin at the 0dB crossing point around 100Hz. Moreover, the increase in bandwidth will result in less suppression at 100Hz, which will on its turn lead to bad THD performance. According to figure 5-8, the system open-loop gain at 100Hz for system with 130Hz bandwidth and 200Hz bandwidth are -21.4 and -18.7 respectively.

Therefore, for systems with bandwidth higher than 100Hz, to ensure enough phase margin, the phase shift brought by the notch filter at 100Hz should be less than 60 degrees (guarantee 30 degrees phase margin). The bode plot of a notch filter with 60 degrees phase shift is shown in figure 5-9.

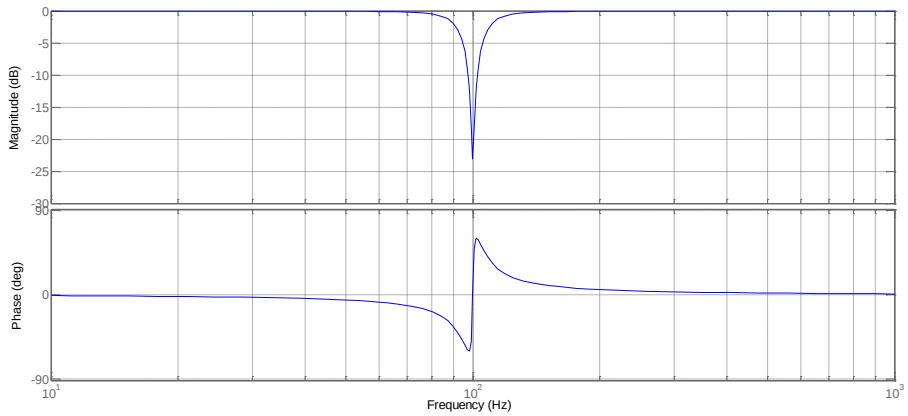


Figure 5-9 Notch filter with 60 degrees phase shift

As can be seen from figure 5-9, the notch filter gives 23dB suppression at 100Hz. When the bandwidth of the system is increased beyond 100Hz, the suppression at 100Hz will be lower than 20dB. According to design guideline, system should give at least 20dB suppression at 100Hz otherwise it will result in a bad THD performance.

To summarize, for system with notch filter, the bandwidth is limited to 100Hz. Further increase in bandwidth will result in bad phase margin and bad THD performance.

2. Simulation

To system behaviors with notch filter and conventional controller, Simulink model is built up and used for simulation. The Simulink model for system with a notch filter is shown in Figure 5-10.

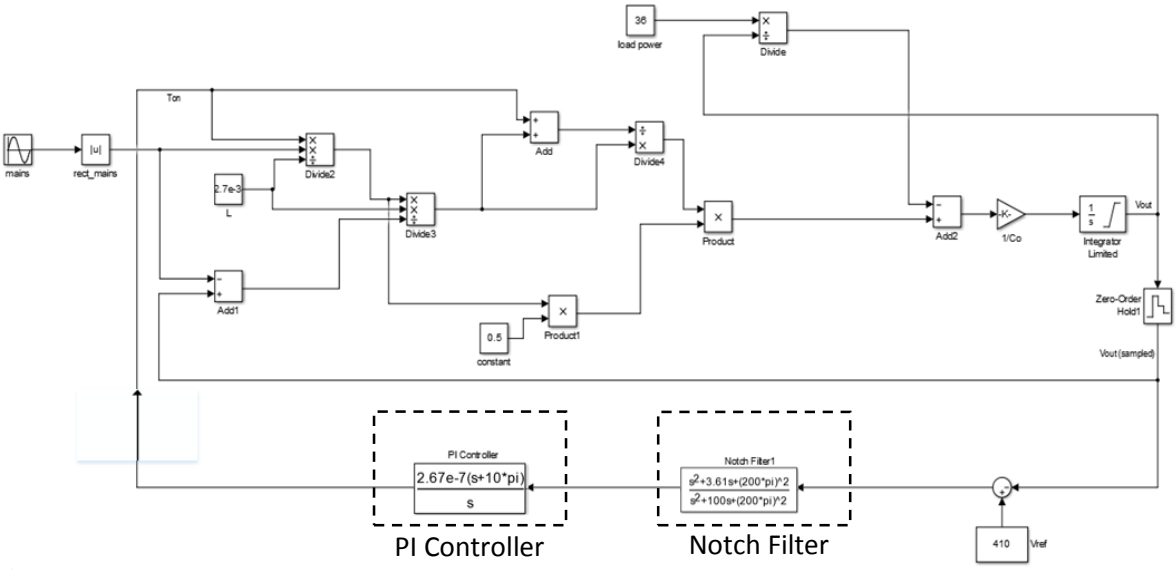


Figure 5-10 Simulink setup for system with a notch filter

Under steady state, THD is 2.3%.

The output voltage behaviors of both systems after applying mains and load disturbances are shown in figure 5-11 and 5-12. To make the waveform clearer to see, the output voltage is drawn in terms of moving average value.

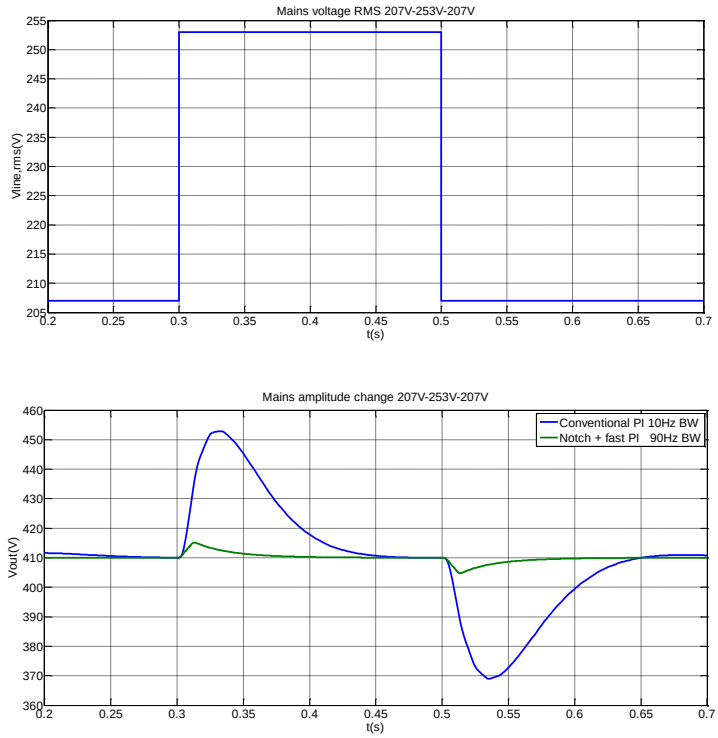


Figure 5-11 Output voltage response to mains amplitude change 207V-253V-207V at t=0.3s and t=0.5s

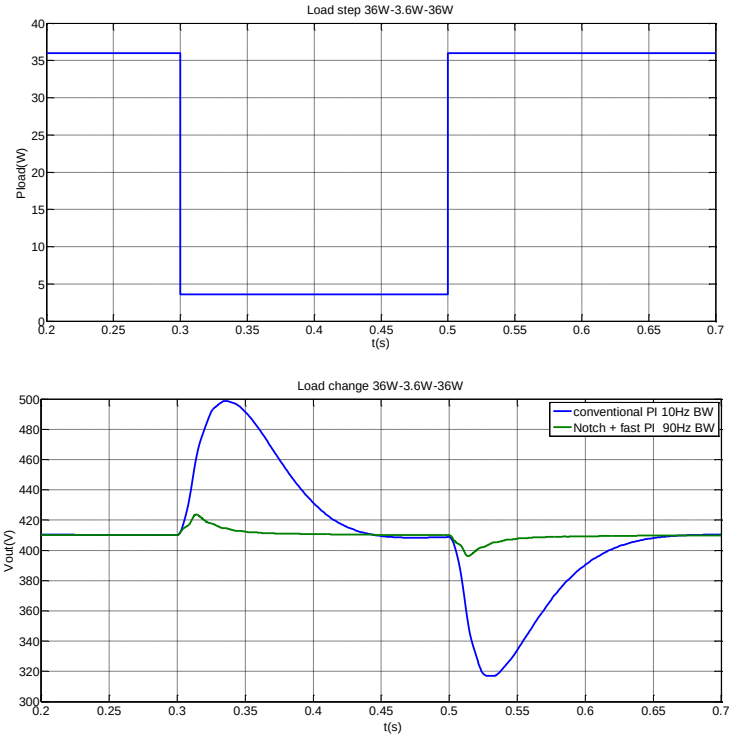


Figure 5-12 Output voltage response to load change 36W-3.6W-36W at t=0.3s and t=0.5s

As can be seen from Figure 5-11 and 5-12, systems with notch filter shows a better dynamic response to mains and load disturbances compared to that of system with conventional controller.

5.1.2 Comb Filter

Another kind of digital filter which can provide even a better THD performance compared to a notch filter is a comb filter. Comb filter can be considered as a notch filter with multiple notches. An ideal comb filter gives infinite attenuation at all the multiples of the center frequency and has no effect on all other frequencies, which can be shown in Equation 5-15.

$$\left|\boldsymbol{G_{cf}(s)}\right| = \begin{cases} \boldsymbol{0} & \boldsymbol{multiples\ of\ center\ frequency} \\ \boldsymbol{1} & \boldsymbol{other\ frequencies} \end{cases} \qquad \text{Equation 5-11}$$

The order of a comb filter is relatively high because it needs to provide attenuation at multiple frequencies, as a result it cannot be applied in analog ways. The discrete transfer function of the comb filter can be written as,

$$\boldsymbol{G_{cf}(z)} = \frac{\boldsymbol{1-z^{-M}}}{\boldsymbol{1-z^{-1}}} \cdot \frac{\boldsymbol{1-(r\cdot z)^{-1}}}{\boldsymbol{1-(r\cdot z)^{-M}}} \qquad \text{Equation 5-12}$$

Where the zero frequencies are $f_{zk} = \frac{f_{vs}}{M} \cdot k = f_c \cdot k$, f_{vs} is the voltage sampling frequency, f_c is the center frequency (double line frequency), k=1, 2, … , M. Parameter r determines the width of the attenuation curve. The effects of r can be shown in figure 5-13.

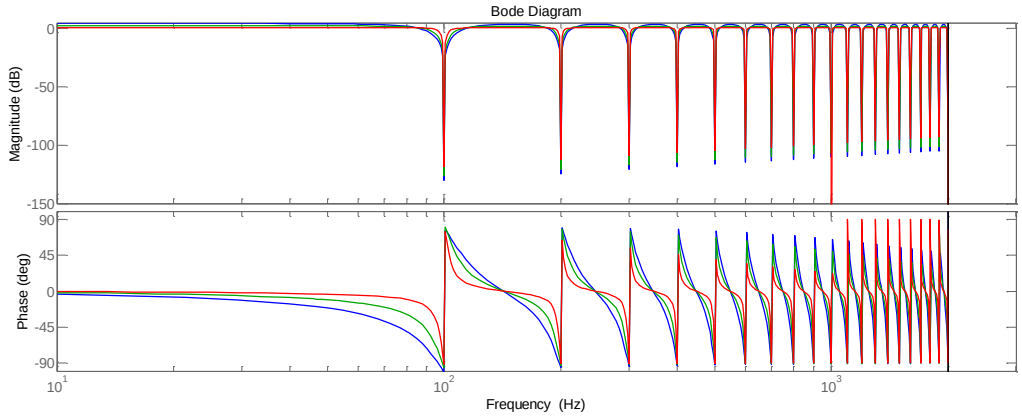


Figure 5-13 Bode plots of comb filters with different r (M=40, , f_{vs}= 4kHz, Red: r=0.995, Green: r=0.985, blue: r=0.97)

Same as the design of a notch filter, when the bandwidth of the system increases to over 100Hz, the phase lag brought by the filter should be at least 30 degrees less than 90 degrees to provide enough phase margin when the amplitude of open loop crosses the 0 dB line. However, this will result in less attenuation of the filter. So in order to guarantee a comparable THD performance compared to that of conventional controller, when the bandwidth of the system increases over 100Hz, it is hard to maintain enough phase margin at the same time.

In conclusion, a comb filter can provide even better THD performance than a notch filter. When the bandwidth of the system is under 100Hz, both the notch and comb filter can provide better THD compared to a conventional controller. However, for implementation, a comb filter needs more memory storage places than a notch filter because of its high order. So it is more cost effective to use a notch filter than a comb filter. So system with a comb filter will not be investigated in details.

5.1.3 Conclusion

Two kinds of digital filters are introduced in this section: notch filter and comb filter. Both of these two filters can increase the system bandwidth to maximum 100Hz, they can provide better THD than system with conventional controller. Further increase in bandwidth will result in bad THD performance and bad phase margin. However, because of larger memory storage place required by a comb filter, a notch filter is a more cost effective way in implementation.

Simulation result shows a significantly improved dynamic response of the system to both mains amplitude change and load change compared to the system with conventional PI controller. THD performance is also improved with the use of a notch filter.

System with notch filter is very sensitive to mains frequency change. As a result, to guarantee the performance of the notch filter, the synchronization of the mains frequency and notch frequency will be needed.

5.2 Feedforward Controller

5.2.1 Controller design

Feedforward is a term describing an element or pathway within a control system which passes a controlling signal from a source in its external environment, often a command signal from an external operator, to a load elsewhere in its external environment. A control system which has only feed-forward behavior responds to its control signal in a pre-defined way without responding to how the load reacts [11]. For the feedforward loop of constant on-time controlled pfc, the controller output is not determined by error, instead it is based on the knowledge about the system mathematic model, each part of which is based on the measurement of the system. After applying feedforward, the bandwidth of the original feedback loop is still designed to be low, fast dynamic response is realized by feedforward loop [12]. Feedforward on time is calculated and updated by the measured input voltage and load power. The control diagram after introducing the feedforward loop is shown in Figure 5-14.

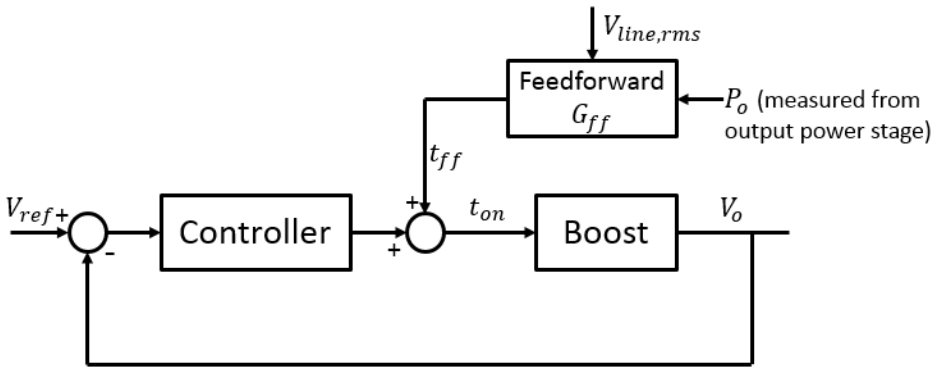


Figure 5-14 Control diagram with feedforward

According to boost operating equations, on time of the switch can be written as,

$$\boldsymbol{t_{on} = t_{ff} = \frac{2LP_o}{V_{line,rms}^2}} \qquad \text{Equation 5-13}$$

Where $V_{line,rms}$ is the RMS value of input voltage, $P_o$is the load power and L is the boost inductor value.

As mentioned in previous chapters, the LED driver contains two power stages. Boost PFC is the input stage while the output stage is another converter driving LED load. Load power in the feedforward loop is better to be measured from the output power stage. If the load power is measured from the input stage, it creates an additional feedback loop which may cause instability issues. Besides, the voltage and current of the output power stage are always measured under normal operating condition with only feedback controller, additional sensing won't be needed for the implementation of feedforward.

5.2.2 Simulation

The system after applying feedforward loop can be built up in Simulink as shown in Figure 5-15.

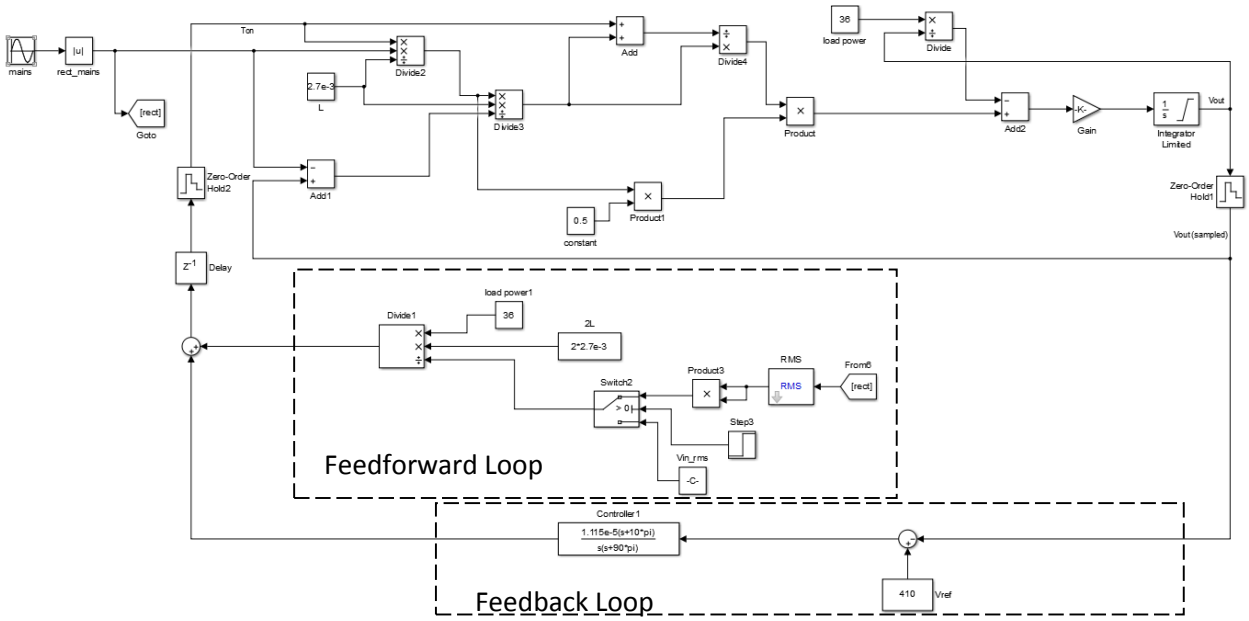


Figure 5-15 Simulink setup with feedforward

Under steady state, THD performance of system applying feedforward control is the same as system with conventional controller.

The function of the feedback and feedforward loop can be considered separately. During transients, because of the instantaneous change of the measured values in the feedforward loop, the system can get back to steady state very fast. However, because there is no setpoint for feedforward, the steady state after transients can be different from the initial state. Feedback loop provides a setpoint for the output voltage, which guarantees the output voltage can always return to the set value after transients. Figure 5-16 shows the transient behavior of systems with pure feedforward controller, pure feedback controller and the combination of feedforward and feedback controller. A mains voltage amplitude change 207V- 253V-207V is applied at t=0.3s and t=0.5s. To make the figure clear to see, the output voltage is drawn in terms of moving average.

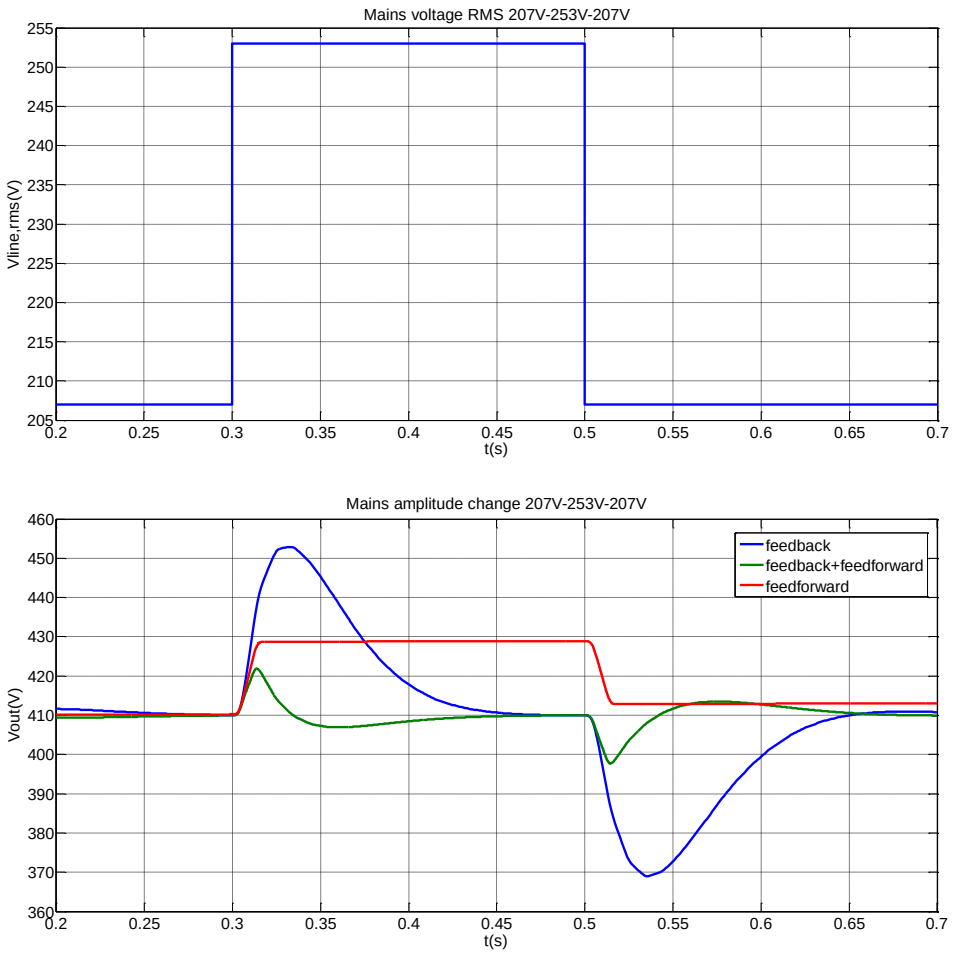


Figure 5-16 Transient responses to mains disturbance for systems with feedback, feedforward and feedback + feedforward controllers. (Vout is the moving average of the output voltage)

At time 0.3s when the amplitude of the input voltage changes, more current flows into the capacitor (see Figure 5-17) which causes an increase in the output voltage. With pure feedforward, the controller reacts right after the increase in the output voltage takes place. Because there is no setpoint for pure feedforward, a new state is recognized as the steady state by the controller. Consequently, the controller keeps drawing the proper amount of current into the capacitor to keep the system at the new state. After further applying the feedback loop to the system, the combined efforts of the two controllers can make the output voltage get back to the setpoint faster than a single feedback controller. The result shows the fact that the feedforward controller has to work in cooperation with feedback controller to provide the system a good transient response to mains disturbance.

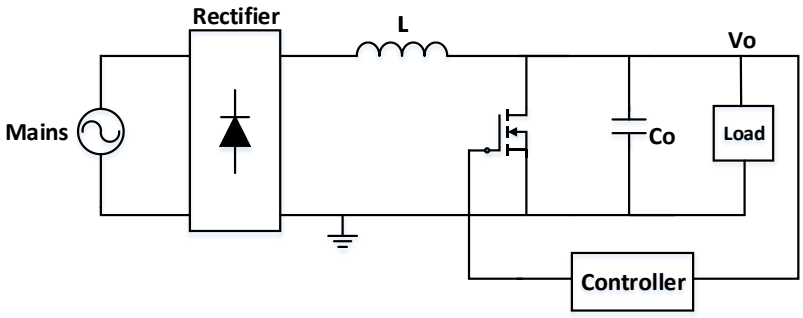


Figure 5-17 Boost topology

Then a disturbance from load change is introduced. Load power change 36W-3.6W-36W is applied at t=0.3s and t=0.5s. The corresponding waveforms for the load step, systems with feedforward + feedback controllers and conventional feedback controller are shown in Figure 5-18.

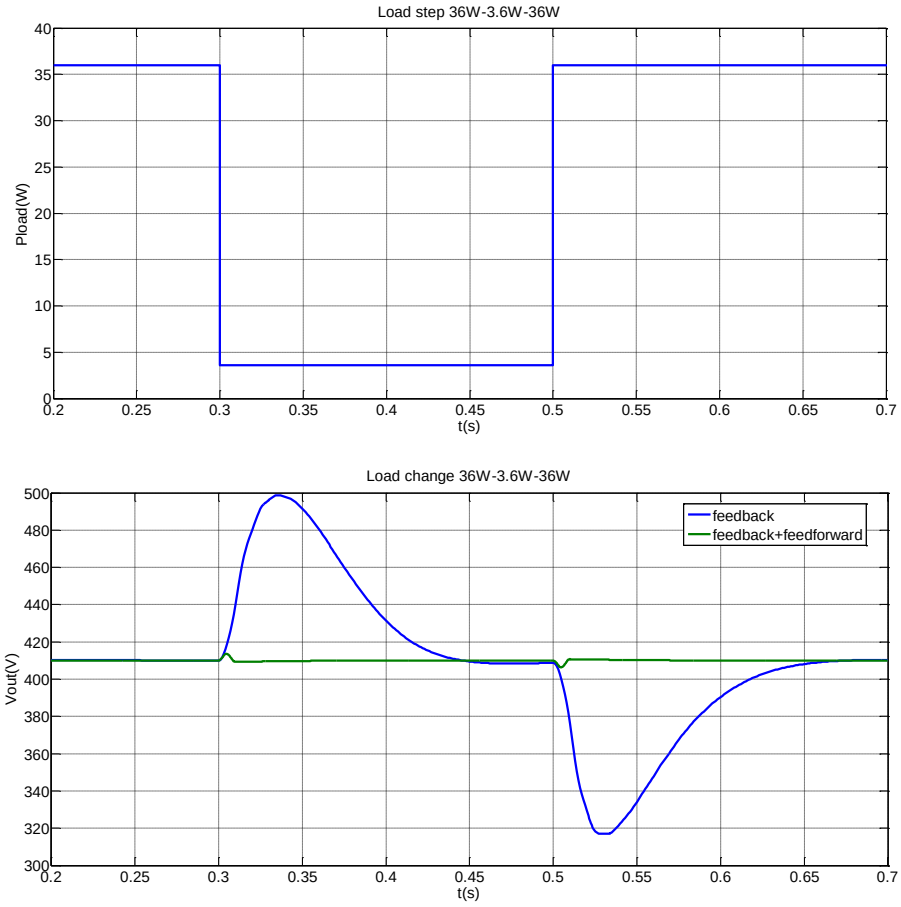


Figure 5-18 Transient responses to load change 36W-3.6W-36Wfor systems with feedback and feedback + feedforward controllers (Vout is the moving average of the output voltage)

As can be seen from the simulation result, after adding a feedforward loop to the system, dynamic response to both mains and load disturbances can be improved significantly compared to the conventional controller with feedback loop only. THD performance after applying feedforward is the same as system with conventional controller.

5.2.3 Conclusion

According to the simulation result, system with feedforward controller shows improved dynamic response to both mains and load disturbances. However, due to the RMS measurement of the mains voltage (the measured RMS value of boost input voltage can only be completely refreshed after half mains cycle), the actual dynamic response to mains disturbances with feedforward loop cannot be better than a system with 100Hz bandwidth.

Since steady state behavior is not changed by the feedforward loop, so the THD performance of system applying feedforward control is the same as system with conventional controller.

5.3 Variable-gain Controller

The basic idea of a variable gain controller is to change the controller parameters according to the amplitude of the error signal that is fed to the controller. When the amplitude of the error signal is lower than a predefined threshold value, the controller operates under the slow mode with the same bandwidth as the conventional controller. Once the error is larger than the threshold value (e.g. due to sudden disturbances in mains voltage or load power), the controller is switched to fast mode with higher bandwidth to achieve a fast dynamic response. The steady state operation is not changed compared to that of the conventional controller, which has a very low bandwidth of 10-20Hz to guarantee a good PF. However, during transients, fast dynamic response is of more importance than THD, a fast controller takes place to get the output voltage back to reference value.

The determination of the threshold value relates to the steady state operation of the boost converter. As already explained in the beginning of this chapter, under steady state the output voltage of the converter is not a constant DC value but a signal with a double-line frequency ripple. The Threshold value is then set to be the maximum voltage ripple of the output voltage, which is the voltage ripple value under nominal load [13]. To ensure the threshold is larger than the voltage ripple under steady state, the threshold value is chosen to be 0.1V larger than the maximum voltage ripple.

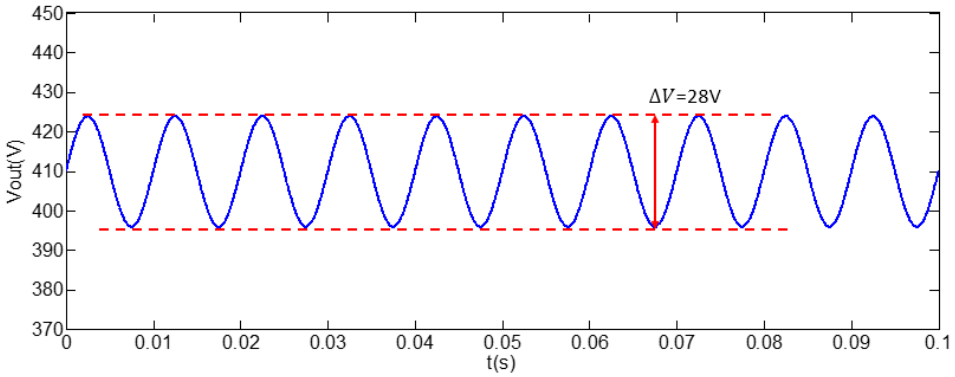


Figure 5-19 PFC output voltage

$$TH = \frac{\Delta V}{2} + 0.1 = \frac{\frac{P_O}{V_O C_O \omega_{line}}}{2} + 0.1 = 14.1\text{V}$$

5.3.1 Controller design

The equation for a PI controller is shown in Equation 5-14.

$$\boldsymbol{u(t) = k_p(t)e(t) + k_i(t)\int_0^t e(t)dt} \qquad \text{Equation 5-14}$$

Where e is the error signal which is fed into the controller, u is the output signal of the controller.

However, if the variable gain controller is built up in this way, there will be a big step in the output of the controller during the switching transients between the two controllers, which can be detrimental to the system. To avoid the step from the controller output, the controller algorithm needs to be written in the way as shown in equation 5-15.

$$\boldsymbol{u(t) = k_p(t)e(t) + \int_0^t k_i(t)e(t)dt} \qquad \text{Equation 5-15}$$

The difference in the integration function between equation 5-14 and 5-15 can be shown by figure 5-20. During the switching transients from the slow controller to the fast controller, the output of the integrator are shown in figure 5-20.

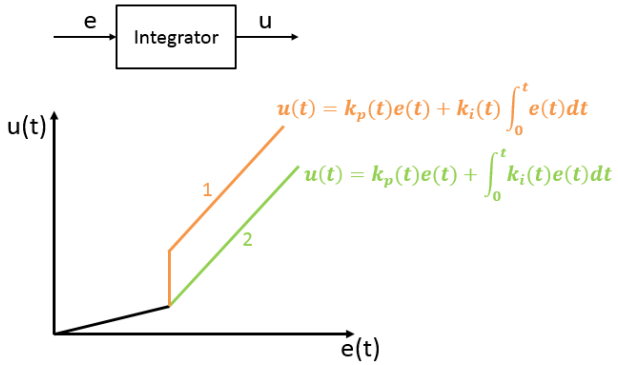


Figure 5-20 two ways of building up the integrator

One way to realize the controller in equation 5-15 is to use state space. The state space representation is shown in equation 5-16.

$$\begin{cases} \dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathrm{e} \\ \mathbf{u} = \mathbf{C}\mathbf{x} + \mathbf{D}\mathrm{e} \end{cases} \quad \text{Equation 5-16}$$

Where e is the input vector, which is the error signal that is fed into the controller, u is the output vector of the controller, x is the state vector. The block diagram of the state-space equation is shown in Figure 5-21.

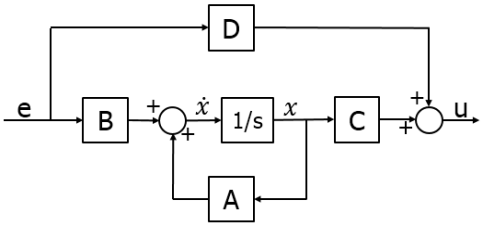


Figure 5-21 Block diagram of the state-space equation

For PI controller, matrix A is always a zero matrix and matrix C is unity matrix. The switching between the two controllers is realized by changing matrix A and B. Then the state space expression can be drawn as figure 5-22.

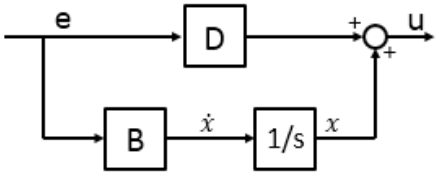


Figure 5-22 state-space equation for PI controller

The design procedures are the same as before. The transfer function of a slow controller with 10Hz bandwidth and 69 degrees phase margin can be written as,

$$\boldsymbol{G_{c\_slow}(s) = 2.48 \times 10^{-8} \cdot \frac{s+7\pi}{s}} \quad \text{Equation 5-17}$$

Then in state space equation,

$$\boldsymbol{B_{slow} = 2.48 \times 10^{-8} \times 7\pi, D_{slow} = 2.48 \times 10^{-8}} \quad \text{Equation 5-18}$$

The transfer function of a fast controller can be written as,

$$\boldsymbol{G_{c\_fast}(s) = 6 \times 10^{-7} \cdot \frac{s+7\pi}{s}} \quad \text{Equation 5-19}$$

System with the fast controller has a bandwidth of 250Hz and a phase margin of 43 degrees. In state space equation,

$$\boldsymbol{B_{fast} = 6 \times 10^{-7} \times 7\pi, D_{fast} = 6 \times 10^{-7}} \qquad \text{Equation 5-20}$$

To further guarantee the system performance during switching transients of the two controllers, a hysteresis band can be introduced. The hysteresis function can be realized by the setting of an outer regulation band, the operation of the hysteresis band is shown in Figure 5-23.

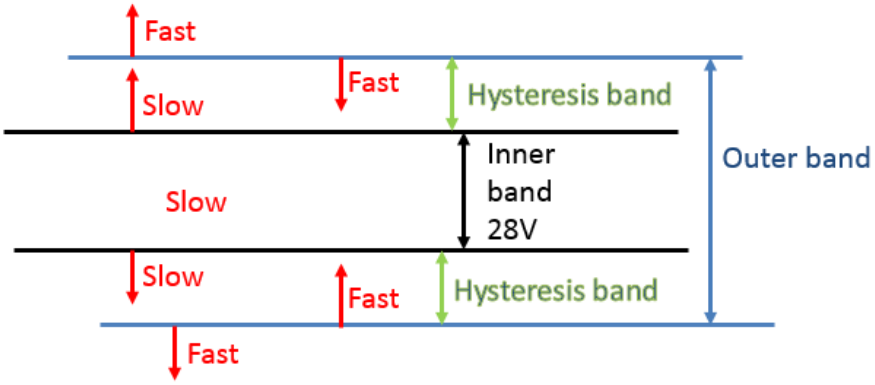


Figure 5-23 Hysteresis band

The working principle of the hysteresis band can be explained as follows: If the output voltage enters the hysteresis band from the inner band, the system is controlled with the slow controller. Once the output voltage exceeds the outer band, the fast controller takes place until the output voltage is within the inner band again.

Wider hysteresis band results in less oscillation during the switching transients between the two controllers, however, it will increase the time needed to bring the voltage back to the reference value. The relationship between width of the hysteresis band and the system behavior will be shown later during simulation.

5.3.2 Simulation

The simulation setup in Simulink is shown in Figure 5-24.

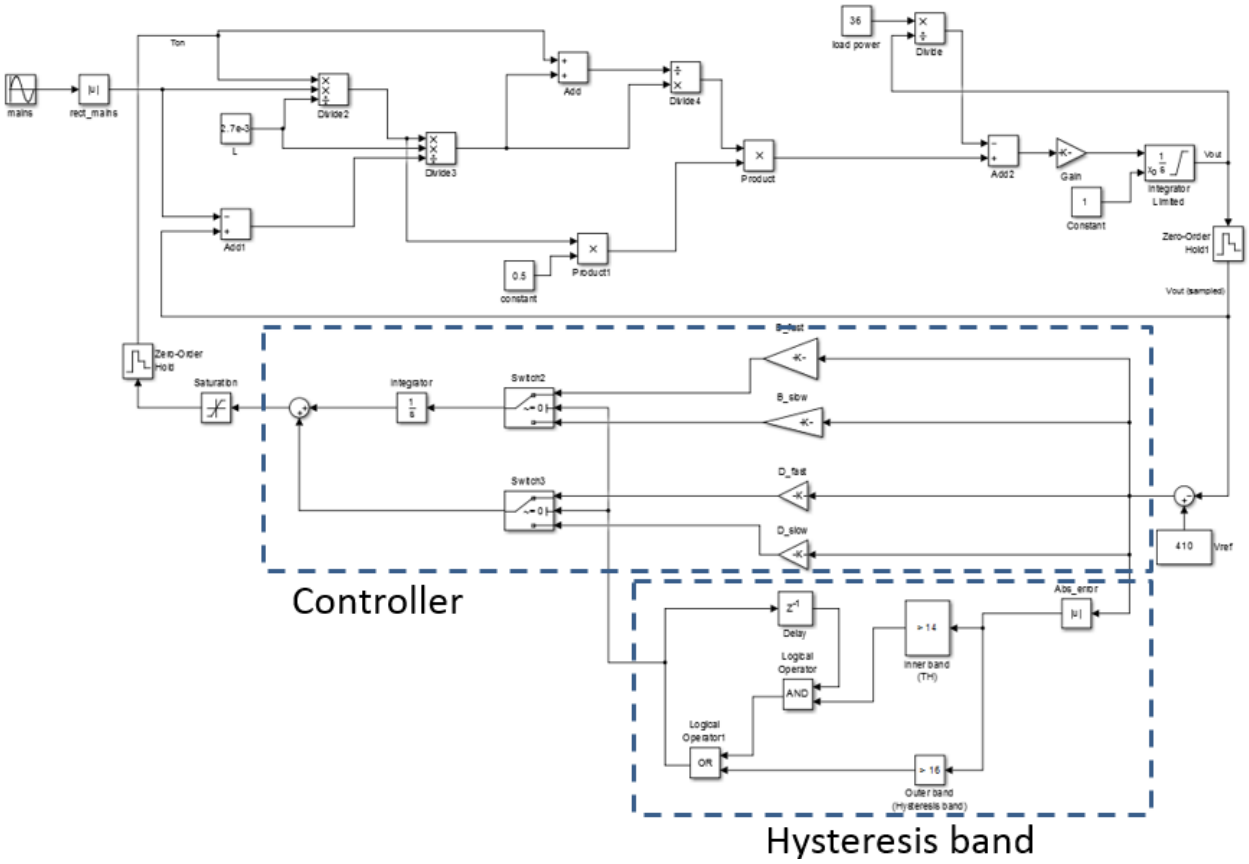
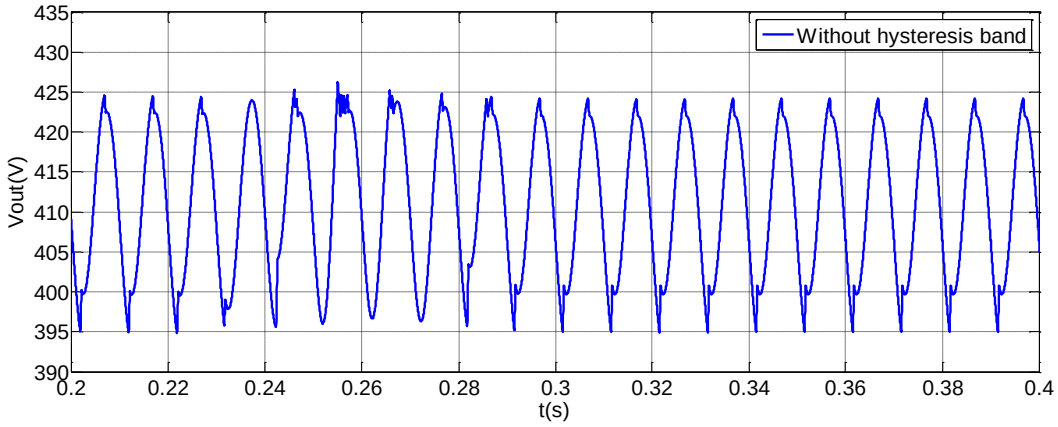


Figure 5-24 Simulink setup for variable-gain controller

The hysteresis bands are set to be 0V, 2V and 6V respectively. For each hysteresis band, a mains disturbance from 207V to 253V is applied. The output voltage behaviors are shown in Figure 5-25.



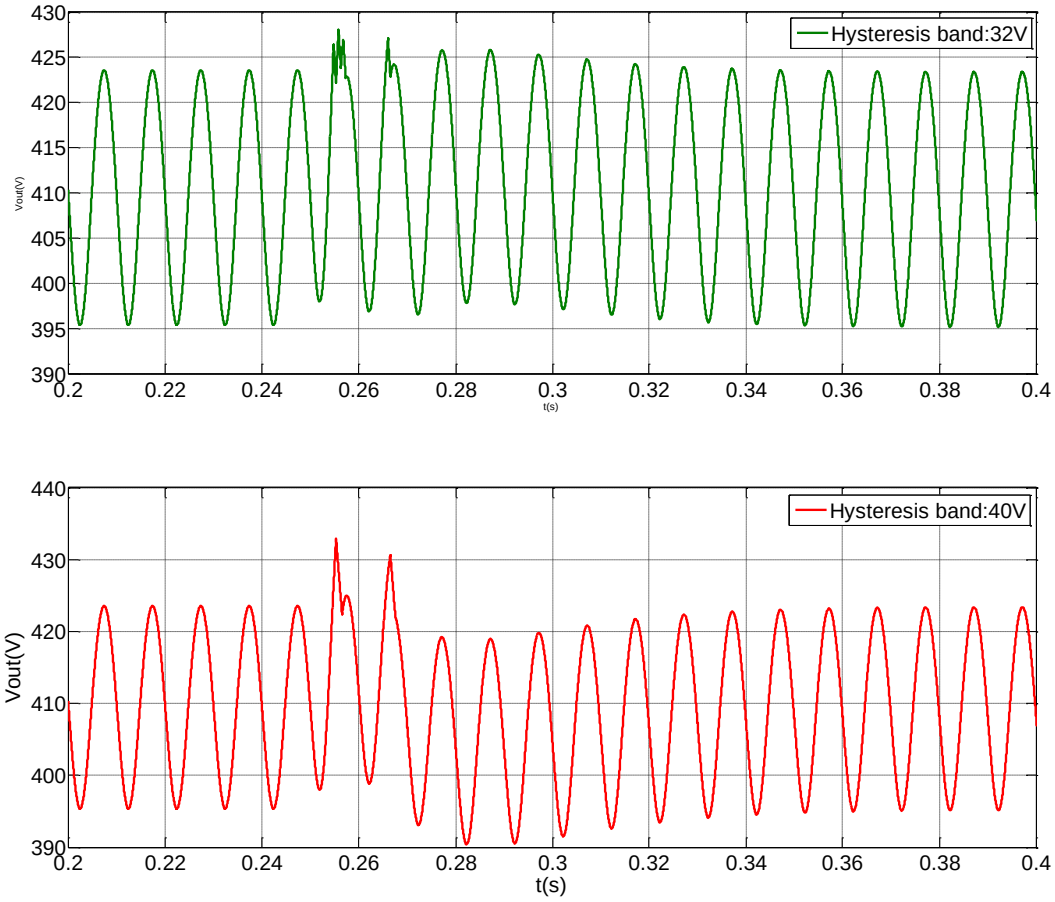


Figure 5-25 System behaviors with different hysteresis bands

To ensure both less oscillations during the switching between the two controllers and fast regulation of the output voltage, 2V hysteresis band is chosen for later simulation.

Under steady state, THD is the same as system with conventional controller, since the use of variable gain does not change the steady state operation of the system.

A mains amplitude change 207V-253V-207V is applied to the system at t=0.3s and t=0.5s. The mains voltage step, output voltage behavior of system using variable-gain controller and conventional controller are shown in figure 5-26. To show the comparison more clear, the output voltage is drawn in terms of moving average.

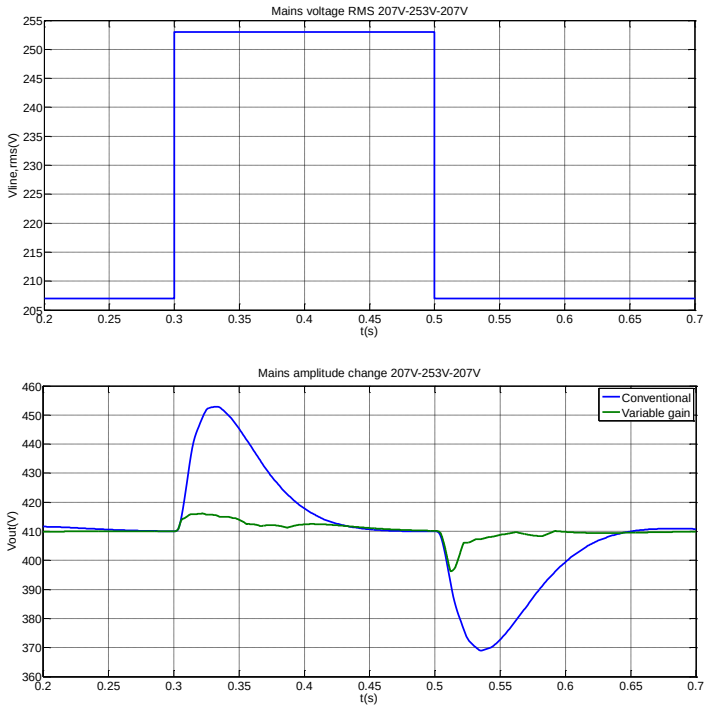


Figure 5-26 Mains amplitude change 207V-253V-207V (Vout : moving average)

Load change 36W-3.6W-36W is applied to the system at t=0.3s and t=0.5s. Load power step, output voltage behavior of system using variable-gain controller and conventional controller is shown in figure 5-27.

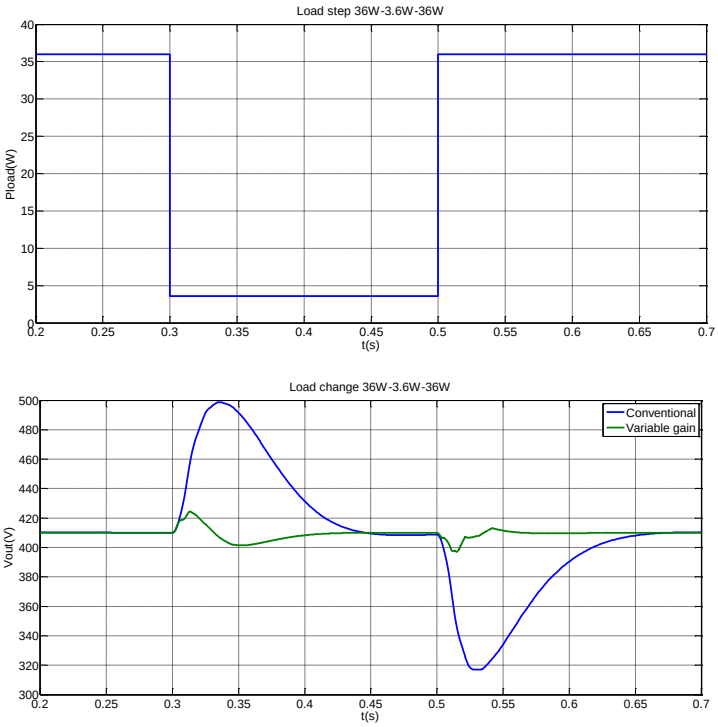


Figure 5-27 Load change 36W-3.6W-36W (Vout is the moving average of the output voltage)

As can be seen from the simulation result, the dynamic response of system with variable-gain controller is improved compared to system with conventional controller.

5.3.3 Conclusion

According to the simulation result, after applying variable gain controller, system shows improved dynamic response to both load and mains disturbances. THD performance is the same as that of conventional controller, since the steady-state operation is not chanced by the variable-gain controller.

However, stability analysis during switching transients between the two controllers needs more effort to be carried out. Also, when the system is operating under light load, the voltage ripple is much smaller than the threshold voltage since the threshold is set according to the maximum voltage ripple. This will make the system blind to errors which are smaller than the threshold voltage.

5.4 Summary

In this chapter, three novel digital controllers,

1. Digital notch/ comb filter
2. Feedforward
3. Variable gain

are designed and analyzed. Based on these designs, simulation are done and the corresponding simulation results are shown. Each solution shows an improved dynamic response to both mains and load disturbances.

Each solution has advantages and drawbacks compared to each other, the comparison and evaluation will be discussed in next chapter.

Chapter 6 Evaluation

Based on the analysis and simulation results of notch filter, feedforward and variable-gain controller, evaluation can be made according to four criterion: dynamic response which includes mains disturbance dynamic response and load disturbance dynamic response, requirement for MCU, implementation difficulty and THD performance.

The purpose of the research is to improve the dynamic response of the boost PFC without sacrificing THD. So dynamic response and THD performance are the two key factors to consider during evaluation. In principle, dynamic response and THD performance should have the same weighing factor during evaluation. However, according to the simulation results in chapter 5, all three methods show the same or even better THD performance compared to conventional controller, which means that all three methods can improve the dynamic response of the boost PFC without further distorting input current. Dynamic response can then become the key evaluation criterion. Load change and mains voltage amplitude change are two main disturbance sources, dynamic response is further evaluated with mains disturbance and load disturbance, each of which has a weighing factor of 30%. The weighing factor of THD performance is set to be 20%. Besides dynamic response and THD performance, there are two more criteria that are considered: requirement for microcontroller and implementation complexity. Requirement for microcontroller indicates how the control algorithm of each controller will affect the selection of MCU. Implementation complexity indicates the realistic issues that are not considered in simulation but are present during real implementation. Both requirement for MCU and implementation complexity have 10% weighing factor. The evaluation criterion and the corresponding weighing factors are shown in table 6-1.

Criterion		Weigh Factor (%)
Dynamic Response	Load Disturbance	30
	Mains Disturbance	30
THD		20
Requirement for MCU		10
Implementation Complexity		10

Table 6-1 Evaluation criterion

The overall score of a conventional controller is considered to be 0 as a reference. The score has a maximum value of 10 and a minimum value of -10. The evaluation, comparison and the overall score will be presented in this chapter.

6.1 Dynamic Response

The controllers are scored according to the maximum change of output voltage after the disturbance takes place, this change implies how well the controller can act to give the output a constant voltage. A score of 0 means that the dynamic response is the same as the conventional controller, a score of 10 means the system can achieve unchangeable output voltage after the disturbance. The moving average of the output voltage waveforms in response to mains amplitude change and load change for all the three controllers are

shown in figure 6-1 and figure 6-2. The use of moving average is to make the figure clear to see (otherwise with 100Hz ripple the figure will look quite messy).

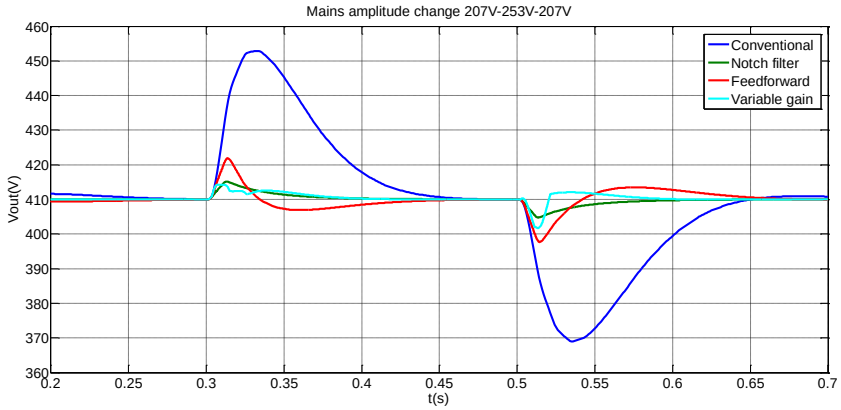


Figure 6-1 Output voltage response to mains amplitude change 207V-253V-207V at t=0.3s and t=0.5s

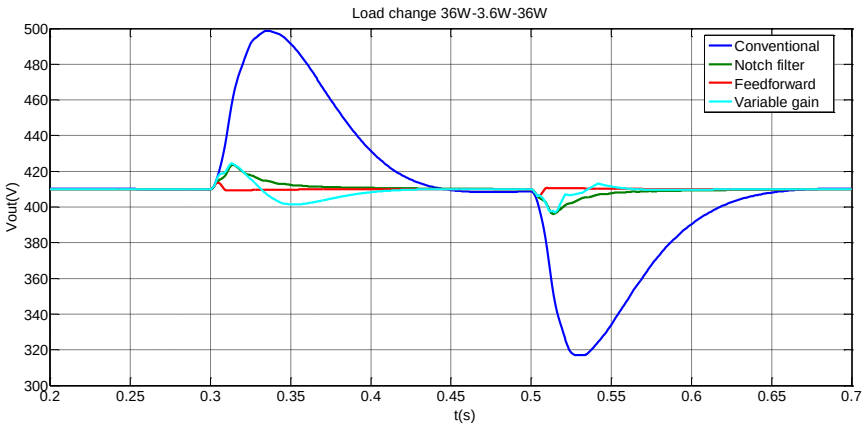


Figure 6-2 Output voltage response to load change 36W-3.6W-36W at t=0.3s and t=0.5s

The scores are then given in table 6-2.

$$score = 10 - \frac{10 \cdot V_{change}}{V_{change,conventional}}$$

Method	Load disturbance (weighing factor: 30%)		Mains disturbance (weighing factor: 30%)		Overall score
	Maximum voltage change(V)	Score	Maximum voltage change(V)	Score	
Conventional	90	0	43	0	0
Notch Filter	14	8.44	5	8.84	17.28
Feedforward	5	9.22	13	6.97	16.19
Variable-gain	15	8.33	8	8.14	16.47

Table 6-2 Scores based on the evaluation criterion: dynamic response

6.2 THD performance

System with notch filter has better THD performance compared to system with conventional controller. The performance depends on the resolution of the microcontroller, higher resolution enables more suppression at the double-line frequency, which will result in better THD. System applying feedforward loop has the same THD performance as the conventional controller since it doesn't change the steady state operation. System with variable-gain controller shows the same THD compared with system conventional controller. Then the scores based on the evaluation criterion THD performance are shown in table 6-3. This evaluation criterion has a weighing factor of 20%.

Method	Conventional	Notch Filter	Feedforward	Variable-gain
Score (weighing factor:20%)	0	>0	0	0

Table 6-3 Scores based on the evaluation criterion: THD performance

6.3 Requirement for MCU

This MCU requirement criteria implies the need for computing ability of the microcontroller for all of the previously discussed controllers. The requirement is given a weighing factor of 10%.

For the implementation of a variable-gain controller, the requirement for the microcontroller doesn't differ a lot from that of the conventional controller. It requires two additional 'if' sentences to determine the control mode of the system and needs to store some states such as previous controller's state. No additional calculation is needed.

For the implementation of an additional feedforward loop, the equation for the feedforward on time is shown in equation 6-1.

$$t_{ff} = \frac{2LP_o}{V_{g,rms}^2} \qquad \text{Equation 6-1}$$

As can be seen from equation 6-1, the calculation of the on time requires the measurement of mains RMS value, which means that the controller has to do calculations for both root, mean and square. These additional calculations result in higher requirement for the microcontroller. The implementation of feedforward loop can be achieved by an 8-bit microcontroller.

For the implementation of a notch filter, one of the realization structures of a digital notch filter is shown in figure 6-3.

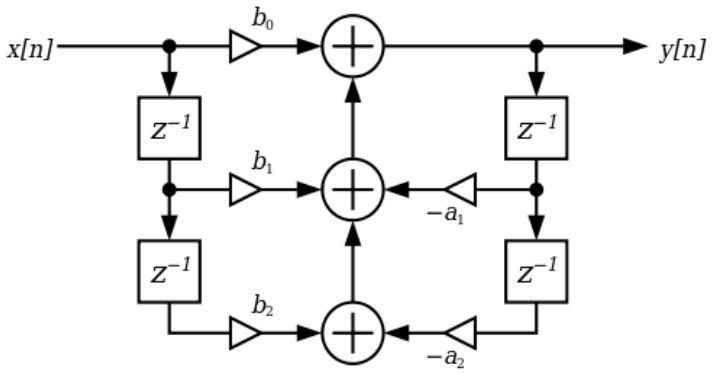


Figure 6-3 Realization structure of a digital notch filter

As can be seen from figure 6-3, the implementation needs 5 multiplications and 3 additions. Moreover, to maintain the desired suppression at the mains frequency, the states need to be able to represent values much larger than the input value times the coefficient size, which makes the states between input and output a 32-bit number. It then becomes not so time efficient to implement the notch filter on an 8-bit microcontroller since operations with such large numbers will need more time (can still be implemented in a 8-bit MCU, but need some tricks to speed the calculation up while programming). So a microcontroller with higher resolution may then be needed. Details in implementation of the notch filter will be explained later in chapter 7.

Based on the analysis above, the score for each of the controller is shown in table 6-4.

Method	Conventional	Notch Filter	Feedforward	Variable-gain
Score (weighing factor:10%)	0	-5	-3	-1

Table 6-4 Scores based on the evaluation criterion: requirement for MCU

6.4 Implementation Complexity

Implementation complexity implies the realistic issues that are not considered in simulation but are present during real implementation. The weighing factor of this evaluation criterion is 10%.

Since the hardware doesn't have a floating point math unit in later implementation, also the software implementations of floating point functions are quite slow, all the controllers are designed to operate in fixed point, which requires quantizing the filter. The controllers need to operate with sufficient precision so that roundoff errors or overflow issues will not occur. For feedforward and variable gain this is not a big issue. However, for notch filter implementation, because the pole states need to have a wide range to maintain the internal resonance behavior which is needed for the notch to work properly, the selection of coefficient precision then becomes a tricky issue. The coefficient precision needs to be sufficient to achieve filters with desired properties without roundoff or overflow, however, higher precision will increase the variable size and further results in slowing computing speed, which will eventually bring delay to the system.

Also, during the previous design and simulation, realistic issues such as distorted mains are not taken into account. If such kind of realistic issues are taken into the account, the equations and the waveforms that are shown in early chapters will deviates from what happens in real implementation. These realistic issues will affect the operation of system applying feedforward the most. The on time of the PFC is directly provided by the feedforward loop and the relatively big impact brought by the unrealistic issues makes the equation deviates from what is derived in equation 6-1. This deviation of on time will result in a bad performance of the system.

For the implementation of variable-gain controller, stability analysis during the switching transient between the two controllers is hard to carry out. Furthermore, the aging issues of the output capacitor need to be taken into account.

Based on the analysis above, the implementation for variable-gain controller can face the most implementation problems due to the lack of stability analysis. The implementation issues brought by the notch filter can be somehow overcome by increasing the resolution of the microcontroller, so it gives the least difficulty during implementation compared to the other two controllers. Then the scores according to the criterion implementation difficulty are shown in table 6-5.

Method	Conventional	Notch Filter	Feedforward	Variable-gain
Score (weighing factor:10%)	0	-3	-4	-5

Table 6-5 Scores based on the evaluation criterion: implementation difficulty

6.5 Overall score

For criteria dynamic response and THD performance, scores are based on simulation and can be quantified accurately. However, criteria requirement for MCU and implementation difficulty cannot be accurately quantified, so scores of these two criteria may change with different considerations and situations.

	Conventional	**Notch Filter**	**Feedforward**	**Variable-gain**
Load Disturbance (30%)	0	8.44	9.22	8.33
Mains Disturbance (30%)	0	8.84	6.97	8.14
THD (20%)	0	>0	0	0
Requirement for MCU (10%)	0	-5	-3	-1
Implementation difficulty (10%)	0	-3	-4	-5
Overall	0	>4.41	4.15	4.34

Table 6-6 comparison table for system with conventional controller, notch filter, feedforward and variable gain controller

Based on the analysis in previous sections and the overall score shown in table 6-6, notch filter scores the highest. The implementation of a system with a notch filter will be shown in Chapter 7.

6.6 Summary

In this chapter, four evaluation criteria are applied to evaluate the overall performance of the three possible solutions proposed in last chapter. After comparison, system with a notch filter scores the highest. So system with a notch filter will go for implementation.

Chapter 7 Implementation

7.1 Introduction to the experiment setup

In this chapter, a system with a notch filter + PI controller is implemented and compared with system controlled by conventional PI controller. A 32-bit fixed point microcontroller is used to achieve the control of the boost PFC. The output voltage of the PFC is sampled at 1kHz.

In chapter 4, the load of the input power stage is considered to be constant power load because the pfc is connected to another converter driving LED load. However, most of the electronic loads which are able to apply a load step do not have a constant power mode. Because of this, resistive load is then used for further experiment to verify the notch filter.

System specification for experiment is shown in table 7-1.

Boost Inductor	2.7mH
Output Capacitor	$10\mu F$
Line Frequency f_{line}	50Hz
Line RMS Voltage $V_{line,rms}$	230V
Output Power P_o	36W
Output Voltage V_o	410V
Output Current I_o	878mA
Inductor Peak Current $I_{L,peak}$	443mA
Input Peak Current $I_{in,peak}$	221.5A
Input RMS Current $I_{in,rms}$	157mA
V_o Sample Frequency	1kHz
Load type	Resistive load (4700Ohms)

Table 7-1 System Specifications

As derived in chapter 3, plant transfer function for system with resistive load is shown in equation 7-1.

$$\boldsymbol{G_{p\_resistive}(s) = \frac{1}{2L}\frac{V_{line,rms}^{\ 2}}{V_o}\cdot\frac{\frac{R}{2}}{1+\frac{RC_o}{2}s}} \qquad \text{Equation 7-1}$$

With the above system specifications, the plant transfer function then becomes,

$$\boldsymbol{G_{p\_resistive}(s) = \frac{5.615\times10^7}{0.0235s+1}} \qquad \text{Equation 7-2}$$

As already derived in previous chapters, the plant transfer function with constant power load is shown in equation 7-3.

$$G_{p\_constantp}(s) = \frac{2.389\times10^9}{s}$$ Equation 7-3

The plant bode plot of both system with resistive load and constant power load is shown in figure 7-1.

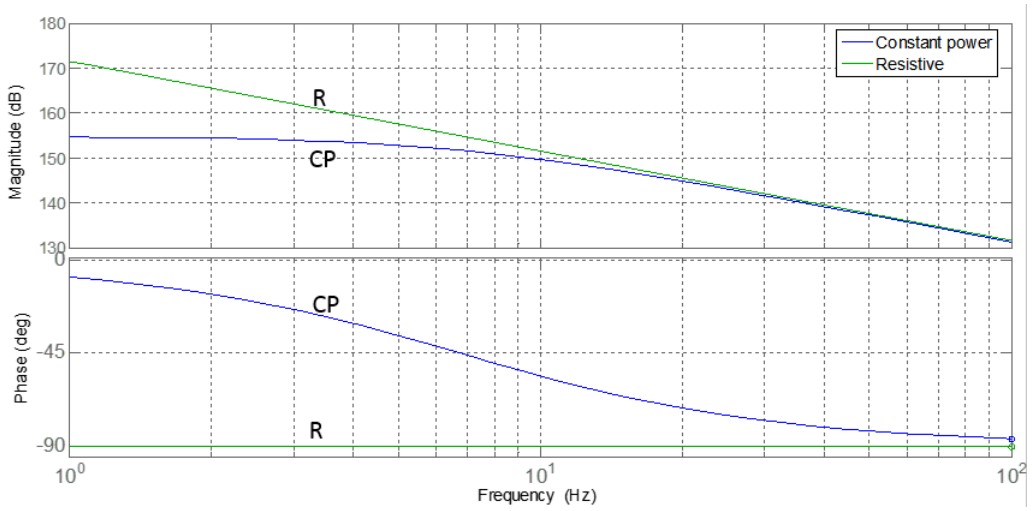


Figure 7-1 Plant bode plot with resistive load and constant power load

As can be seen from figure 7-1, the gain and phase of system with resistive load and constant power load has a big difference at low frequencies. However, above 10Hz the difference then becomes very small. So system open-loop bode plot with resistive load is almost the same as that of system with constant power load at frequencies higher than 10Hz. Therefore, experiment with resistive load is already able to indicate the system behavior with constant power load.

The experiment setup is shown in figure 7-2.

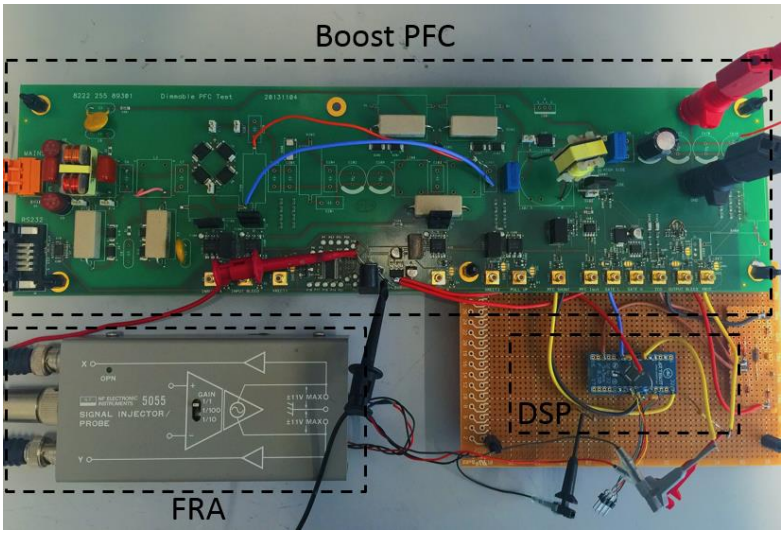


Figure 7-2 Experiment setup

The controller function is realized by the 32-bit DSP. FRA (frequency response analyzer) is used to do the frequency domain analysis of the system, which can further indicate the system stability. The operation of the FRA will be explained in later section.

7.2 Notch Filter Implementation

Two types of realization structures are typically used for digital filtering [14], direct form I and direct form II, as shown in figure 7-3 and 7-4. In the case of the notch filter, direct form I is used since the numerator states are the same resolution as the input, which can reduce the numerator (b_1, b_2) multiplies.

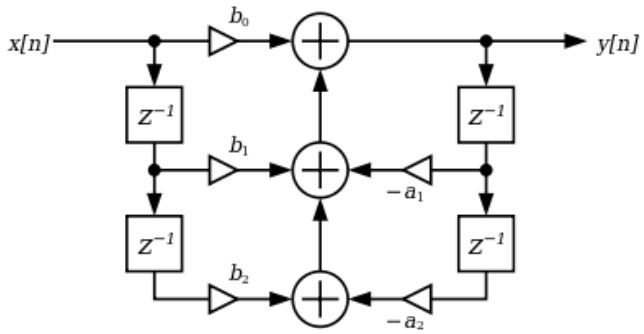


Figure 7-3 Direct form I realization (diagram from Wikipedia 2013)

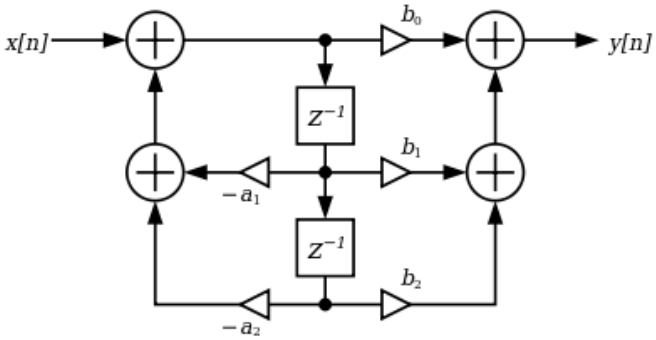


Figure 7-4 Direct form II realization (diagram from Wikipedia 2013)

Since the software implementations of floating point functions are too slow, the filter is then designed to operate in fixed point, which requires quantizing the filter. The filter needs to operate with sufficient precision so that roundoff errors don't either contribute too much noise of cause the filter to stop operating by overflow. Tests with the notch found that the notch would operate normally at high power levels, but abruptly stop operating at low input error levels. At low input signal amplitudes roundoff would stop the oscillation of the pole states required for the filter to operate. At high signal amplitudes the variables would overflow causing erratic behavior and destroying the filter behavior. These two limitations, roundoff of small inputs, and overflow of large inputs drive the selection of the variable sizes and precision used in the filter. Analysis of the notch behavior found that to give the input 15 times suppression (-23dB), the pole states need to have a range about 60dB (1000×input) to maintain the internal resonance behavior needed

for the notch[15]. Based on the analysis in [15], all the quantization sizes of the notch are shown in figure 7-5.

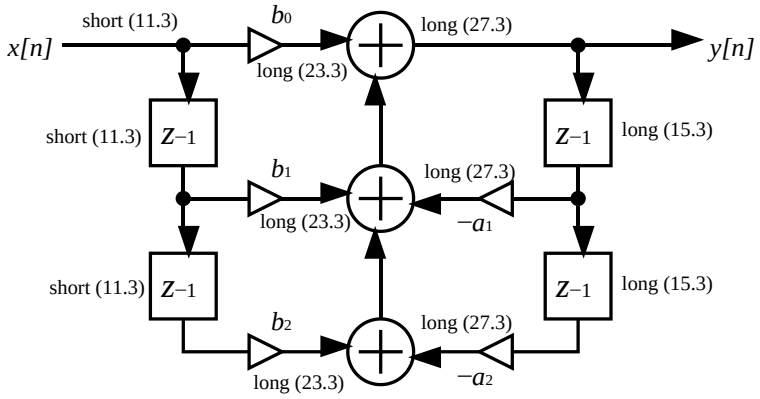


Figure 7-5 Notch quantization sizes

All numbers in figure 7-5 are signed. Short(11.3) means a number stored in a short with a value up to -1023, with 3 bits of precision.

Larger suppression at the notch frequency results in larger accumulator size and more precision bits, which will on its turn result in slower computing speed. To guarantee the performance, for implementation the target suppressing factor for the input is chosen to be 1/15 (-23dB). Which means the notch gives -23dB suppression at the notch frequency. The discrete transfer function of the notch filter is shown in equation 7-4.

$$\boldsymbol{G_{nf}(s) = \frac{z^2 - 1.596z + 0.9744}{z^2 - 1.292z + 0.6703}} \qquad \text{Equation 7-4}$$

The bode plot and step response of the notch filter is shown in figure.

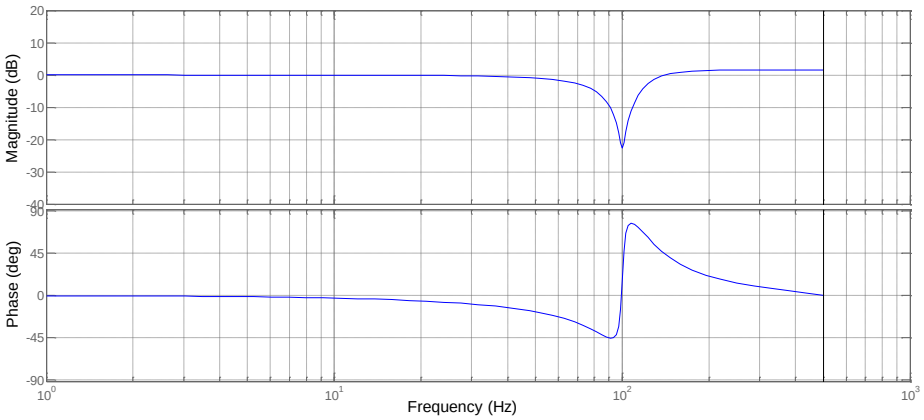


Figure 7-6 Bode plot of the notch filter

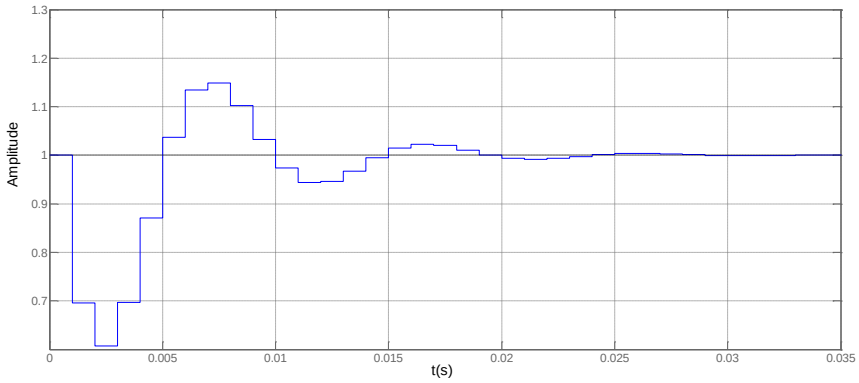


Figure 7-7 Step response of the notch filter

7.3 Experimental Result

After integrating the notch filter to the existing product which is only controlled with a PI controller, experiment is done to see the system performance under both mains and load disturbances with and without the notch filter.

7.3.1 FRA measurement

The open-loop bode plot of both systems are measured with a frequency response analyzer (FRA). The operation of the FRA can be explained by figure 7-8.

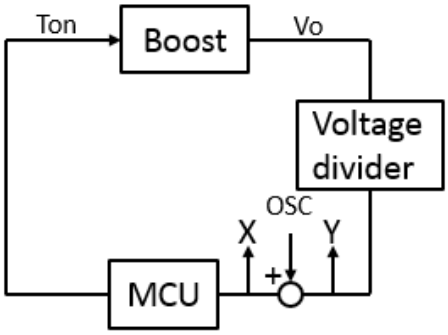


Figure 7-8 FRA operation

The loop is opened after the voltage divider, an oscillating signal is injected to the loop. Then X/Y can be measured, which is the system open loop. Because of the injected signal, the system changes from an inverting system to a non-inverting system. This change has no influence on the open-loop gain, however, open-loop phase will have a 180 degrees phase shift. As a result, the phase measured by the FRA can be considered as the phase margin of the system.

The open-loop bode plot of both systems (conventional PI controller, notch filter + PI controller) are then measured. The plots are shown in figure 7-9 and 7-10. Blue line represents phase and red line represents gain.

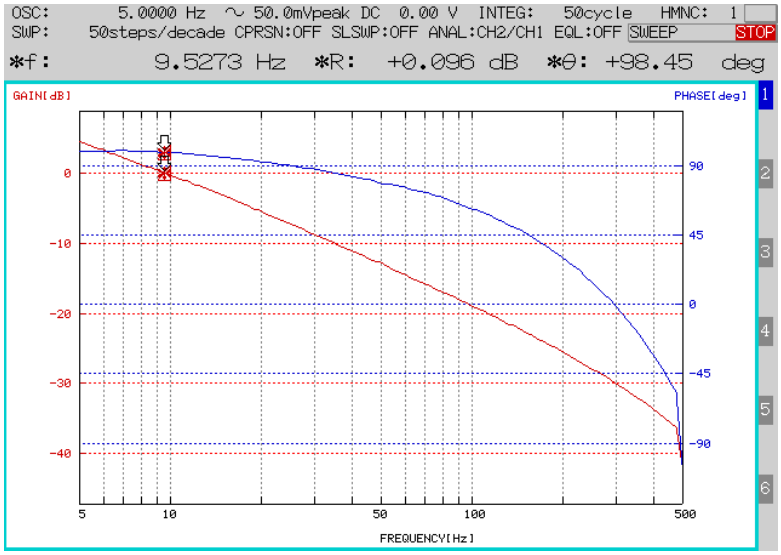


Figure 7-9 FRA measured open-loop bode plot for system with conventional controller

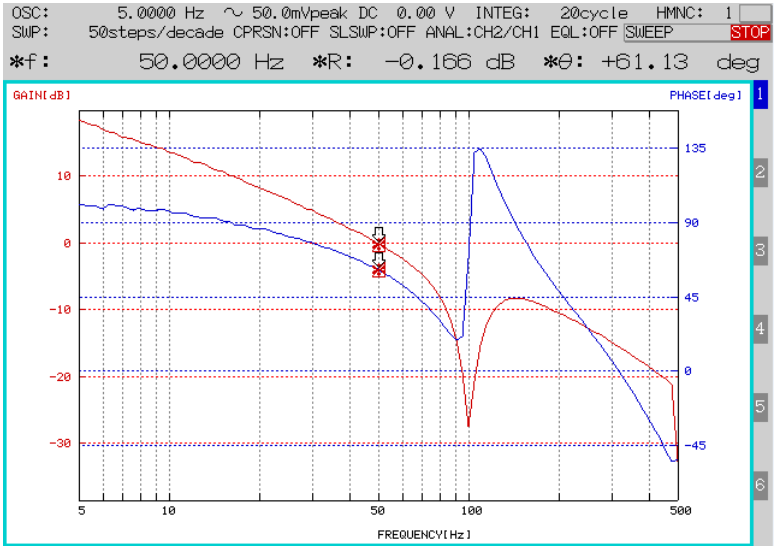


Figure 7-10 FRA measured open-loop bode plot for system with NF+PI

As can be seen from figure 7-9 and 7-10, system with conventional PI controller has a bandwidth of 9.5Hz and phase margin of more than 90 degrees. System with notch filter and a PI controller has 50Hz bandwidth and 61 degrees phase margin. The Simulink simulated system open-loop bode plot for both systems are shown in figure 7-11 and 7-12.

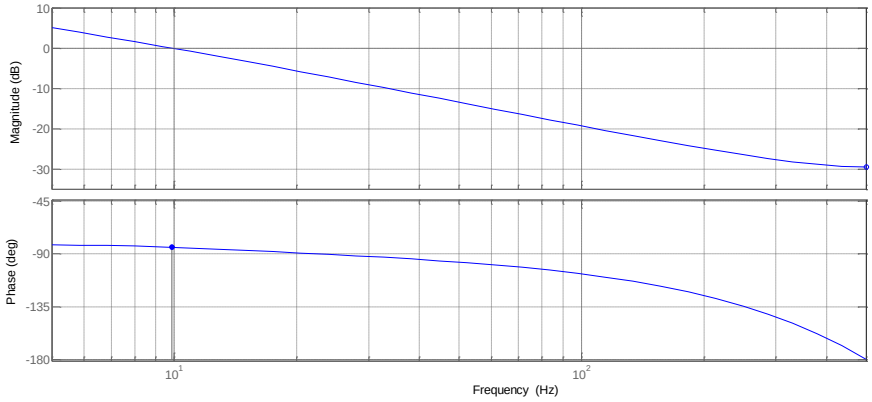


Figure 7-11 Simulink simulated open-loop bode plot for system with conventional controller

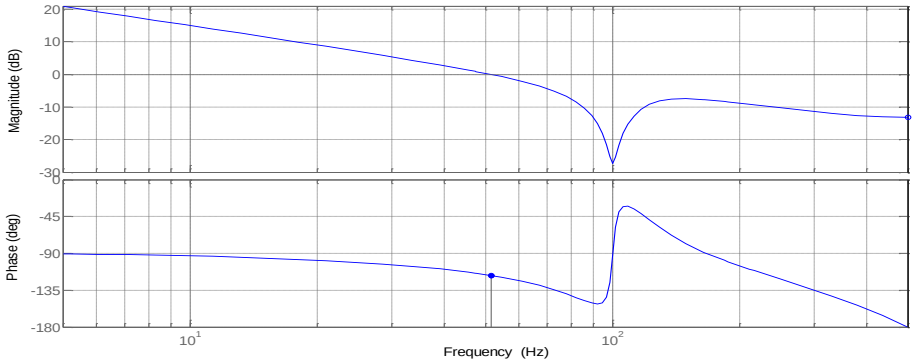


Figure 7-12 Simulink simulated open-loop bode plot for system with NF+PI

The comparisons between the FRA measured and Simulink simulated open-loop bode plots are shown in table 7-2 and 7-3.

Frequency (Hz)		10 (BW)	50	100	200
FRA	Gain (dB)	-0.2	-12.9	-19.1	-25.6
	Phase (deg)	-81	-100	-119	-150
Simulink	Gain (dB)	0	-13.4	-19.5	-25.1
	Phase (deg)	-84	-97	-107	-126

Table 7-2 Comparison between simulation and measurement for system with conventional controller

Frequency (Hz)		20	50 (BW)	100	200
FRA	Gain (dB)	8.3	-0.2	-27.1	-10.4
	Phase (deg)	-94	-119	---	-132
Simulink	Gain (dB)	9.1	0.3	-27.2	-9.6
	Phase (deg)	-98.5	-117	---	-105

Table 7-3 Comparison between simulation and measurement for system with NF+PI

As can be seen from table 7-2 and 7-3, the measurements show slightly difference (measurement error) in gain, but more phase lag. This indicates that there are more delay in the system.

7.3.2 THD performance

With nominal mains input (230V) and load power (36W), output voltage of both systems are controlled to 406V. Because of the tolerance of voltage divider, it shows 4V difference compared to the desired output voltage 410V. The output voltage and input current waveforms are shown in figure 7-13.

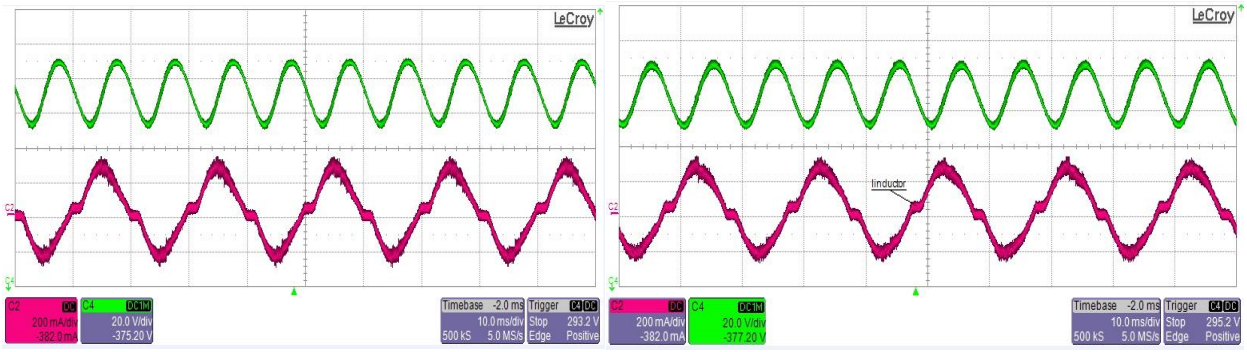


Figure 7-13 Input current and output voltage with 230V mains input, 36W load power. Left: conventional PI controller, 10Hz BW Right: Notch filter + PI, 50Hz BW

According to measurement, under steady state (230V input, 36W output power), THD of system with conventional controller is 16.41%, while for system with notch filter, THD is 14.14%. As explained before, system with notch filter shows a better THD performance because it gives more suppression at 100Hz. THD performance of system as a function of input voltage and output power is shown in figure 7-10 and 7-11.

It can be observed from figure 7-14 and 7-15 that at higher mains voltage or lighter load, THD becomes worse. This can be easily explained by the transfer function of the plant shown in equation 7-1. At higher mains voltage and lighter load, the plant has a larger gain, which will result in an increasing system bandwidth. This increase in bandwidth will eventually result in worse THD performance of the system.

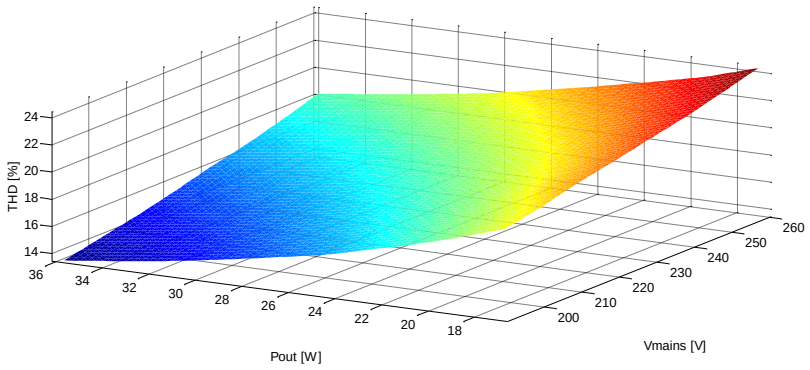


Figure 7-14 THD as a function of output power and mains voltage (conventional controller, 10Hz BW)

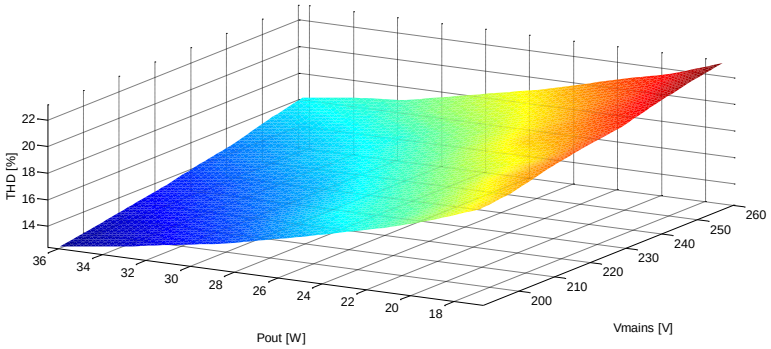


Figure 7-15 THD as a function of mains voltage and load power (with notch filter, 50Hz BW)

7.3.3 Mains step

A mains step 207V-230V-207V is applied to both systems. After applying this mains step, the output voltage overshoot for system with conventional PI controller is already getting close to the OVP value of the output voltage (460V), so larger mains steps cannot be applied. The responses for both systems are shown in figure 7-16 and figure 7-17.

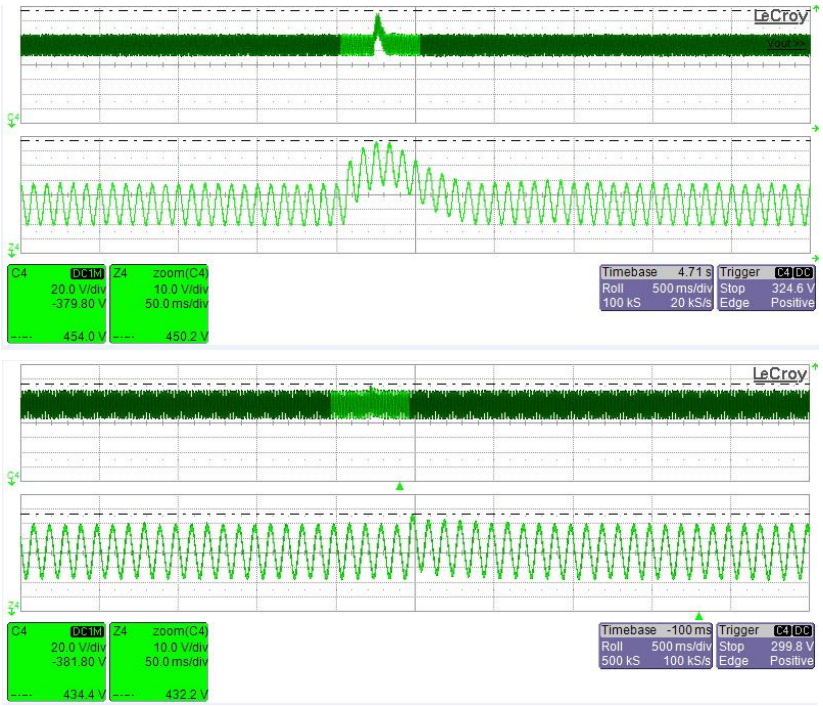


Figure 7-16 Output voltage behavior for mains step from 207V-230V (upper: conventional PI, 10Hz BW bottom: notch filter+ fast PI, 50Hz BW)

After applying mains step from 207V to 230V, system with conventional PI controller shows 450.2V peak voltage. However, system with notch filter + fast PI controller has only 432.2V peak voltage.

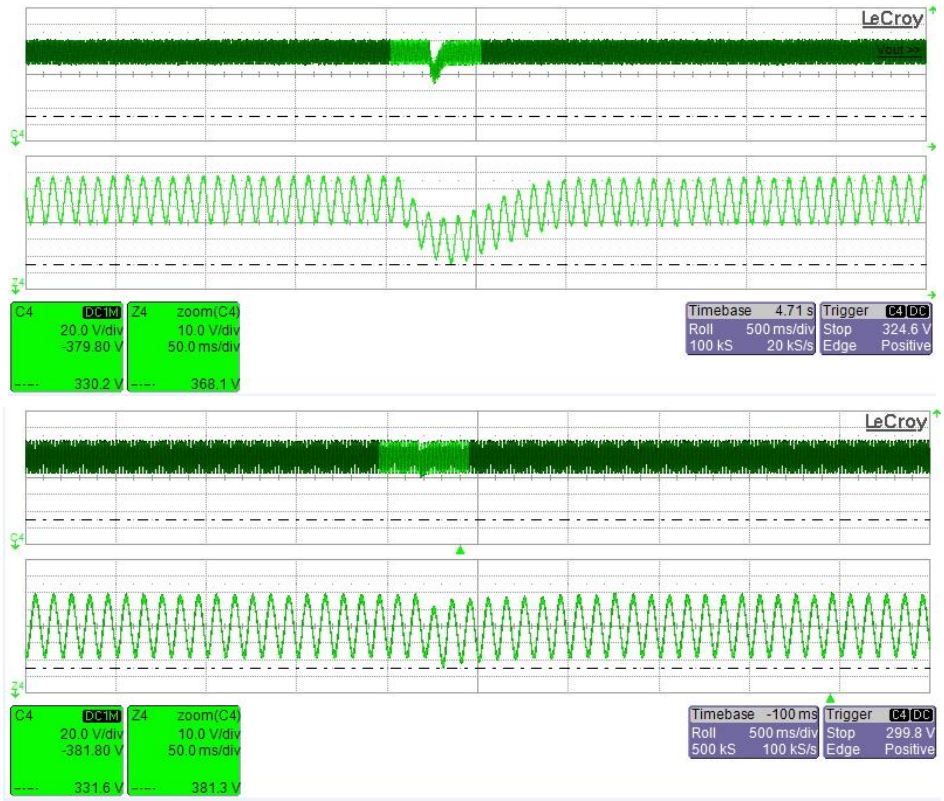


Figure 7-17 Output voltage behavior for mains step from 230V-207V (upper: conventional PI, 10Hz BW bottom: notch filter+ fast PI, 50Hz BW)

After applying mains step from 230V to 207V, system with conventional PI controller shows voltage dip to 368.1V. However, system with notch filter + fast PI controller dips to only 381.3V.

According to the measurement, system with NF+ fast PI provides a more stable bus voltage compared to system with conventional PI controller.

7.3.4 Load step

A load step 36W-24W-36W is applied to both system. For the same reason, larger steps will trigger the OVP of the system. The system performances after applying the load step are shown in figure 7-18 and 7-19.

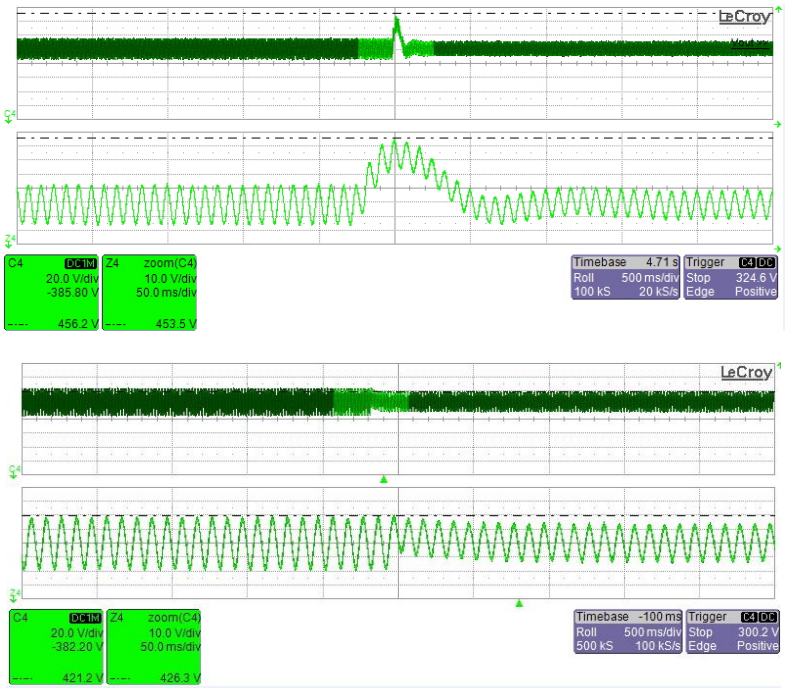


Figure 7-18 Output voltage behavior for load step from 36W-24W (upper: conventional PI, 10Hz BW bottom: notch filter+ fast PI, 50Hz BW)

After applying load step from 36W to 24W, system with conventional PI controller shows 453.5V peak voltage. However, system with notch filter + fast PI controller has only 426.3V peak voltage.

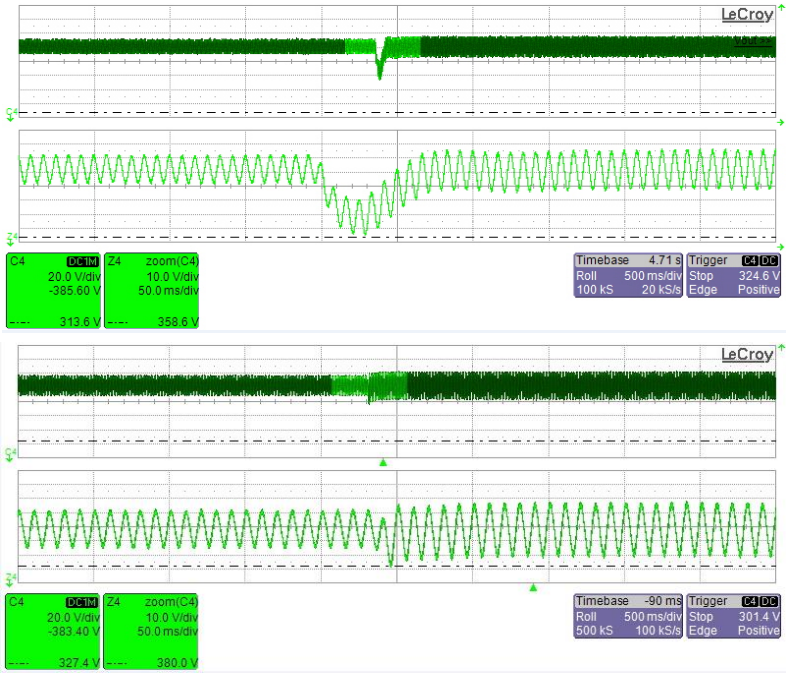


Figure 7-19 Output voltage behavior for load step from 24W-36W (upper: conventional PI, 10Hz BW bottom: notch filter+ fast PI, 50Hz BW)

After applying mains step from 24W to 36W, system with conventional PI controller shows voltage dip to 358.6V. However, system with notch filter + fast PI controller dips to only 380.0V.

According to the measurement, system with NF+ fast PI provides a more stable bus voltage compared to system with conventional PI controller.

7.4 Summary

In this chapter, two systems are considered: system with conventional PI controller, system with notch filter + PI controller. The open loops of the two considered system are measured by FRA. The former one has around 15Hz bandwidth and almost 90 degrees phase margin and the latter one has 50Hz bandwidth and 61 degrees phase margin.

THD performances of the two systems are measured by the power analyzer. System performances after applying both load and mains steps are measured on the oscilloscope. The measured data for both systems are shown in table 7-4.

	BW /Hz	PM /Deg	THD/% ($V_{mains,rms} = 230V$ $P_o = 36W$)	Mains step		Load step	
				207V-230V V_o peak(V)	230V-207V V_o valley(V)	36W-24W V_o peak(V)	24W-36W V_o valley(V)
Conventional PI	9.5	≈ 90	16.41	450.2	368.1	453.5	358.6
NF + PI	50.0	61	14.14	432.2	381.3	426.3	380.0

Table 7-4 system performances conventional PI vs NF+PI

As can be seen from table 7-2, after applying the notch filter, the bandwidth of the system can be further increased without distorting the input current. Because of the increase in bandwidth, the system shows better dynamic performance to both mains and load disturbances. Also, since there is more suppression brought by the notch filter at 100Hz, the THD performance is improved compared to that of conventional PI controller.

Chapter 8 Conclusions and Recommendations

8.1 Conclusions

The input power stage (boost PFC) of today's stand-alone LED drivers for professional lighting systems has a very low bandwidth (10-20Hz) as to not interfere with the power factor correction function. Because of this low bandwidth, disturbances from the mains and load side are transferred to the boost PFC output capacitor, which, on its turn, can lead to undesired visible light effects if these disturbances are too large.

The research work aims at increasing the bandwidth of the boost PFC, so that the input stage can have better suppression to disturbance, thus minimizing the undesired visible light effects under disturbances. To investigate the low-bandwidth control loop, each part of the input stage is modelled and the transfer functions are derived. Based on the derived control loop models and transfer functions, three possible solutions to increase the PFC dynamic response are proposed:

1. Digital notch/comb filter
2. Feedforward
3. Variable gain

The proposed three controllers are designed and investigated in detail. Simulation results of all three solutions show an improved dynamic response compared to system with conventional controller only.

Four criteria: Dynamic response, THD, requirement for MCU, implementation complexity are then applied to evaluate the 3 proposed solutions. The use of a digital notch filter scores the highest after comparison.

Based on the evaluation, a notch filter is implemented with a 32-bit fixed point microcontroller. A system controlled by notch filter + PI controller is used for the experiment. It has 50Hz bandwidth and 61 degrees phase margin measured by FRA. THD performances are measured, load and mains steps are applied for both system with conventional PI controller (14Hz bandwidth) and system with notch filter + PI controller (50Hz bandwidth). Experimental result shows that system with notch filter + PI controller not only has a better THD performance, but also provides much more stable output voltage in response to both load and mains disturbances.

With this improved dynamic response, the PFC is able to provide a more stable bus voltage when disturbances occur, which will on its turn result in good light quality.

8.2 Recommendations

During the process of designing a novel digital controller for the boost PFC to improve its dynamic response, some open issues need to be addressed for further research.

8.2.1 Stability analysis for switching controller

During the design of variable-gain controller, stability analysis during switching transients between the two controllers has not been done. The result would me more convincing with precise stability analysis. The analysis requires deeper knowledge in control theory and could be an interesting topic for further work.

8.2.2 Plant Gain Scheduling

As derived in chapter 3, the transfer function of the boost converter will change with different mains voltage, load power, inductor and output capacitor value. During operation, the change in each of the above mentioned four parameters (e.g. dimming, mains voltage change, aging of the output capacitor) will change the plant gain, thus change the bandwidth and margins of the closed loop system. To further guarantee the system performance, the system open-loop gain is better to be kept constant. To achieve this, the controller coefficients can be designed automatically adjusted depending on the operating point.

8.2.3 Further increase in bandwidth

The bandwidth of systems using notch/comb filter and feedforward are both somehow limited to 100Hz. For variable gain controller, system can be blind for disturbances under light load. For better dynamic response of the system, further research can be done to increase the system bandwidth to beyond 100Hz.

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