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Toward a Full-Flexible and Fast-Prototyping TOF-PET Block Detector Based on TDC-on-FPGA

Esteban Venialgo¹, Nicola Lusardi, Fabio Garzetti, Angelo Geraci, Stefan E. Brunner, Dennis R. Schaart², and Edoardo Charbon³

Abstract—Typically, a time-of-flight (TOF) positron emission tomography (PET) block detector is built using application-specific integrated circuits (ASICs), since they integrate a high number of channels at a reasonable power consumption and into a small area. However, ASICs' flexibility is limited and prototyping times are long because a semiconductor fabrication process is required in every design iteration. Alternatively, fast terminal (FT) silicon photomultipliers (SiPMs) require a simplified analog front-end in order to achieve TOF accuracy. In addition, field-programmable gate arrays (FPGAs) can allocate time-to-digital converters as well as complex digital readout logics. In this paper, we propose building TOF-PET block detectors based on FPGAs, FT-SiPMs, and minimal amount of off-the-shelf components. In this way, TOF-PET accuracy is achieved with a full-flexible and fast prototyping solution. We evaluated the coincidence resolving time, performance degradations due to channel multiplexing, energy resolution, and scintillator pixel encoding performance of SiPM arrays utilizing the proposed approach. Experimental results show minimal timing degradations, when multiplexing FTs. Moreover, simulation results show a low reduction in the singles count rate of multiplexed channels at typical brain-PET radioactive doses.

Index Terms—Coincidence resolving time (CRT), field-programmable gate array (FPGA), positron emission tomography (PET), silicon photomultiplier (SiPM), time-of-flight (TOF), time-to-digital converter (TDC).

I. INTRODUCTION

SINCE the introduction of the positron emission tomography (PET) block detector in the 1980s, it was possible to

build PET scanners in a modular approach [1]. One advantage of breaking out the detection area into many independent block detectors was the drastic increase in the count rate capability of the PET scanner [2], [3].

With the advent of time-of-flight (TOF) PET and PET/MRI imaging modalities, new technologies were introduced, e.g., silicon photomultipliers (SiPMs), in order to fulfill the new requirements, such as high timing resolution and magnetic field insensitivity. In addition to SiPMs, application-specific integrated circuit (ASIC) development appeared as a solution that integrates even more independent channels per PET block detector up to a single channel per scintillator pixel [4], [5]. This solution avoids utilizing scintillator pixel encoding circuits, which are usually difficult to calibrate on the edge of the block detector, and additionally allows to further increase the singles count rate. However, the main disadvantages of the ASIC approach are the lack of flexibility and long development and testing cycles.

More recently, digital SiPMs appeared as an alternative photodetector utilized in combination with scintillators for gamma photon detection in PET [6]–[8]. These types of sensor represent a further step into system integration and ASIC development, since they integrate single-photon avalanche diode (SPAD) cells along with a comprehensive readout circuit into the same die. In addition, the analog readout is entirely removed by exploiting the intrinsic digital nature of SPADs when detecting light. Once the sensor is developed, it allows a direct system integration; however, its main drawbacks are the even longer development and testing cycles due to their high complexity.

In order to obtain accurate timing information from an analog SiPM, which features a relatively large output capacitance, specialized shaping circuits are required in order to keep a fast signal rise time. However, since the introduction of the fast terminal (FT) by SensL, a fast signal can be obtained without any specialized circuits [9]. Because the FT is integrated into the SiPM, the analog readout circuit can be simplified by removing the timing shaping circuits entirely and reducing it to few off-the-shelf components.

In PET instrumentation, time-to-digital converters (TDCs) replaced free-running fast sampling analog-to-digital converters (ADCs) for timestamping gamma-photon events [10]. Field-programmable gate arrays (FPGAs) can allocate TDCs as well as digital readout and interfacing logic in order to

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E. Venialgo is with the Applied Quantum Architectures Department, Delft University of Technology, 2628CD Delft, The Netherlands (e-mail: e.venialgo@tudelft.nl; e.charbon@tudelft.nl).

N. Lusardi, F. Garzetti, and A. Geraci are with DEIB, Politecnico di Milano, 20133 Milan, Italy.

S. E. Brunner and D. R. Schaart are with the Radiation Science and Technology Department, Delft University of Technology, 2628CD Delft, The Netherlands.

E. Charbon is with the Advanced Quantum Architecture Laboratory, EPFL, CH-2002 Lausanne, Switzerland.

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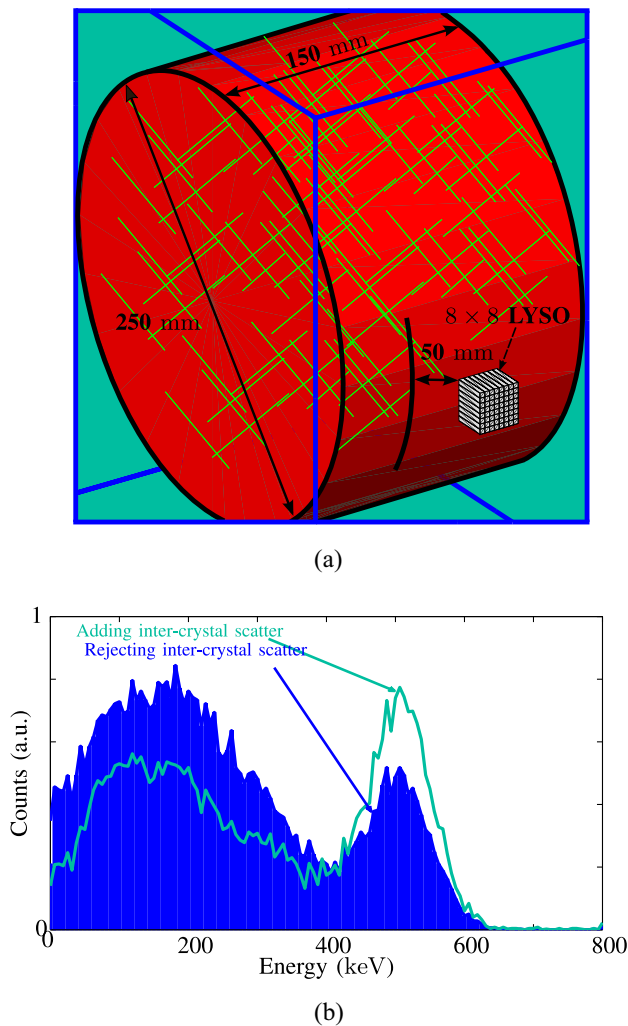


Fig. 1. GATE/Geant4 single count rate simulation. (a) Simulation setup description. (b) Obtained simulated energy spectrum (the energy resolution was set to 20% at 511 keV).

build a PET block detector. As an added benefit, FPGAs can be reprogrammed at any point in time of the development cycle in order to add or fix PET detector functionalities [11], [12].

In this paper, we performed a series of experiments in order to demonstrate that fully flexible and fast-prototyping TOF-PET block detectors can be built directly from off-the-shelf components without ASIC development. The prototype circuits are based on TDC-on-FPGA, off-the-shelf components, and FT J-series SiPMs from SensL [13]–[15].

II. SINGLE COUNT RATE AND CHANNEL MULTIPLEXING

When designing a PET scanner, the noise equivalent count rate (NECR) and the sensitivity are among the most important parameters under consideration [2], [3]. The NECR is reduced mainly by three factors: 1) detector dead time; 2) unrejected scatter events; and 3) random coincidences.

The amount of unrejected random coincidences depends on the single count rate and the coincidence-window width. If the system-level coincidence resolving time (CRT) is smaller than

the field-of-view (FOV) diameter in terms of time distance, which is 833 ps for a 250 mm diameter, the coincidence-window width is limited by the FOV diameter. Additionally, the coincidence-window width is extended beyond the FOV in terms of time by a factor that depends on the scanner CRT, in order not to suppress valid events due to the timing measurement uncertainty.

The unrejected scattered events depend on energy resolution. Finally, the NECR sensitivity can be reduced significantly, depending on the injected radioactivity, which moreover depends on the specific PET application.

Incrementing the number of channels by subdividing the detector area into blocks drastically improves the NECR [2], [3]. However, implementing several channels within the same PET block detector might not increase the NECR significantly, because it also depends on the injected radioactive dose and scanner geometry.

We performed a GATE/Geant4 simulation in order to study the impact of the channel multiplexing on the single count rate of a PET block detector [16]. We considered a brain-PET block detector case, which is described in Fig. 1(a), because this application requires high NECR and sensitivity [17], [18].

For the simulation, a cylindrical phantom, which is 250 mm in diameter and 150 mm in length, was filled with ^{18}F and water. The phantom radioactivity was varied from 0.1 to 1000 MBq. A PET block detector composed of 8×8 LYSO pixels of 3 mm pitch and 20 mm depth was simulated. In order to simulate a scanner inner bore diameter of 350 mm, the inner face of the PET block detector was placed 50 mm away from the external side of the cylindrical phantom. The obtained energy spectrum is depicted in Fig. 1(b). In all the simulations, an energy resolution of 20% at 511 keV was assumed based previous works [17].

For calculating the single count rate, all of the detected events were considered singles, as an example of extreme conditions for the instrumentation, without filtering events by an energy window.

In PET instrumentation, after detecting a gamma event an energy discrimination is applied in order to immediately discard Compton scattered gamma photons. For instance, if we select a low threshold of the energy-window around 300 keV, gamma events that generate multiple hits from Compton scattering within the scintillators and the energy of any individual hits lower than 300 keV are rejected. As a consequence, about 14% of the events with intercrystal scatter were rejected [see Fig. 1(b)]. Therefore, in order to accept events with multiple hits, the PET detector module must be capable of detecting individual hits and combine them as a single gamma event.

As mentioned, the detector was composed of 64 LYSO pixels and we analyzed the single count rate for several scintillator pixel multiplexing cases [see Fig. 2(a)–(d)]. In the following analysis, 64 channels refer to one independent measurement channel per LYSO pixel. Conversely, one channel means that the 64 LYSO pixels share a single measurement channel. We considered that the detector is composed of TDCs for gamma-photon timestamping and energy estimation [10]. Additionally, we assumed that the dominant dead time of the system is

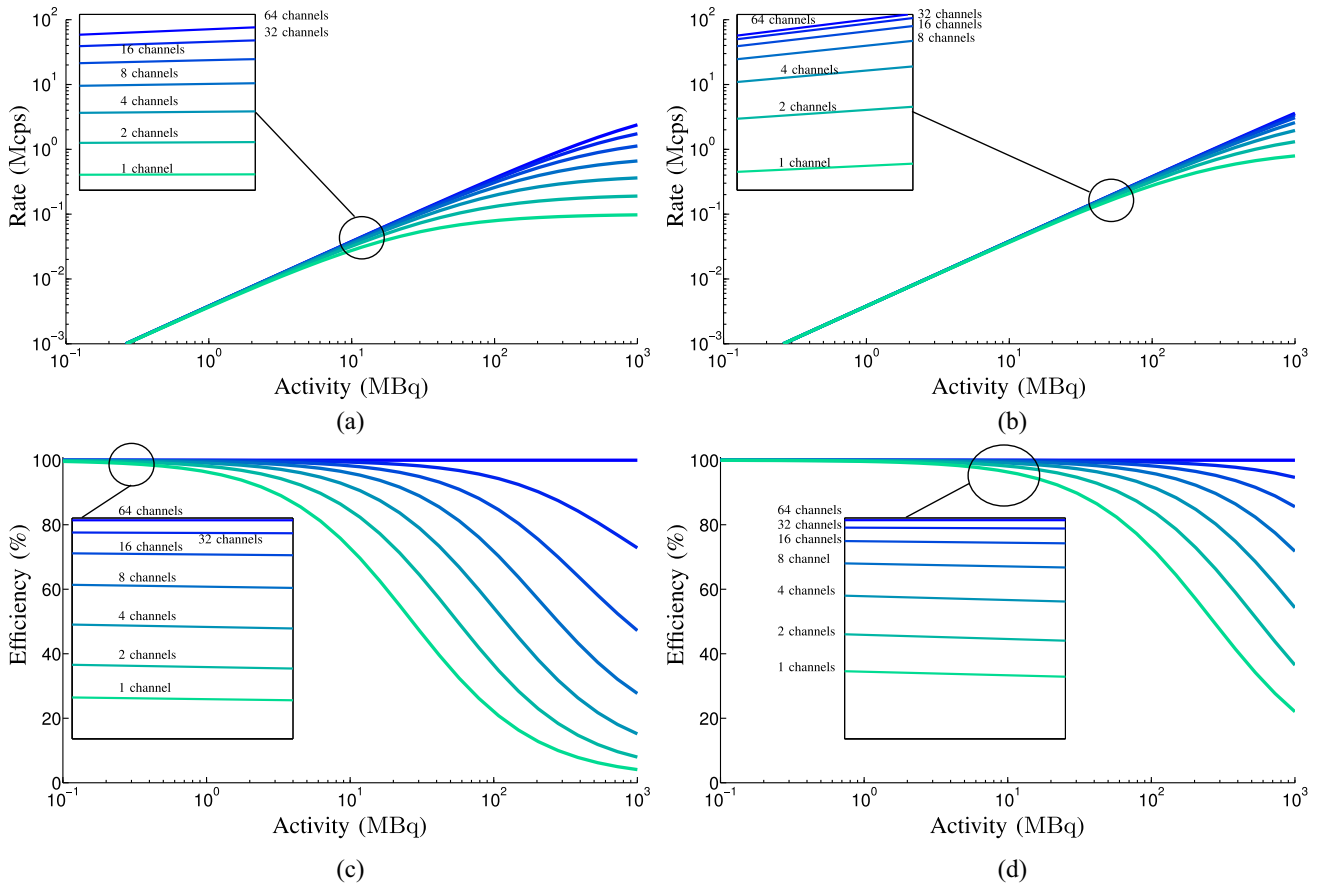


Fig. 2. Single count rate comparison for several channel multiplexing configurations and channel dead times. (a) Absolute single count rate with a channel dead time of 10 μ s. (b) Absolute single count rate with a channel dead time of 1 μ s. (c) Normalized singles count rate relative to the 64 channel case, with a channel dead time of 10 μ s. (d) Normalized singles count rate relative to the 64 channel case, with a channel dead time of 1 μ s.

the time-of-conversion of the TDCs, which can be modeled as nonparalyzable. Furthermore, we chose 1 μ s dead time as a reasonable time-of-conversion that can be achieved by a TDC on FPGA and 10 μ s as a worse-case comparison point [10].

Fig. 2(a) and (b) shows the absolute count rate of single events when sweeping the phantom activity for the 10 and 1 μ s channel dead time cases, respectively. In addition, we calculated the relative singles count rate normalized with respect to the optimum case, which is 64 channels. Fig. 2(c) and (d) depicts the relative singles count rate for the 10 and 1 μ s channel dead time cases, respectively.

In previously reported injected doses utilized in brain-PET imaging, which were around 400 MBq, we observed a relative count rate loss of about 55% and 12% for the 10 and 1 μ s channel dead time cases, respectively, in the case of eight channels [see Fig. 2(c) and (d)] [17]. Therefore, we concluded that a reasonable number of channels per PET block detector is 8, if the channel dead time is 1 μ s, since the decrease in efficiency of the single count rate is low with respect to having 64 independent channels. An additional argument to favor eight channels is that a row-wise readout circuitry can be implemented when choosing an 8 \times 8 SiPM array, in order to achieve eight independent measurement channels, as it is shown in the following sections.

III. TIMING RESOLUTION AND CHANNEL MULTIPLEXING

Previously, we demonstrated that state-of-the-art CRT can be achieved by PET detectors composed of TDC-on-FPGA and SiPMs equipped with FTs [10]. The case of having one timing channel per LYSO pixel requires many TDCs integrated on the FPGA. Additionally, an extensive analog front-end, which consumes a significant amount of power, is needed. To achieve a fully flexible ASIC-less design channel multiplexing is necessary, in order to reduce power consumption and FPGA implementation complexity. We studied the timing impact of sharing the same measurement channel among several SiPM FTs. In all of the experiments presented in this paper, which were performed at room temperature, the bias voltage of the SiPMs was 30 V. The utilized J-series SiPMs are characterized by a minimum and maximum breakdown voltage of 24.2 and 24.7 V at 21 $^{\circ}$ C, respectively [19].

A. Reference Detector Characterization

First, we calibrated our reference detector that was composed of a SensL single SiPM evaluation board of a J-series 3 mm SiPM. We performed a coincidence measurement with two identical detectors in order to estimate the single detector

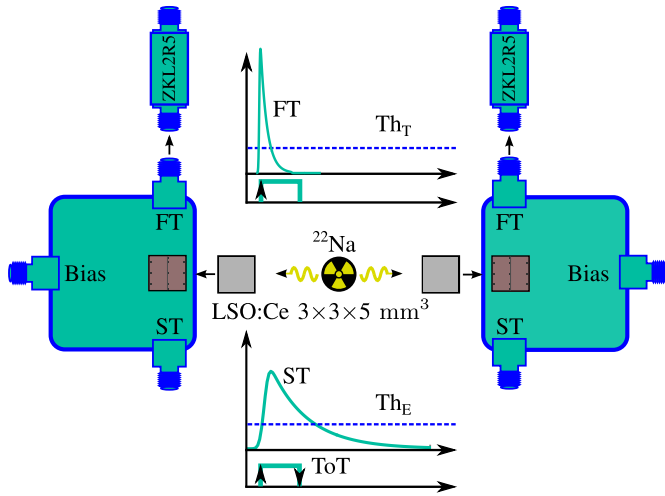


Fig. 3. Block diagram of the reference detector measurement setup.

resolution (SDR) (see Fig. 3). $3 \times 3 \times 5 \text{ mm}^3$ LSO:Ce scintillators from Agile were glued on top of the SiPMs.

In comparison to our previous work [10], we utilized a newer version of the TDC on FPGA board that comprises an Artix7 system-on-module (SOM), digital-to-analog converters (DACs) for automatic threshold scanning, low-jitter comparators (ADCMP607), and a high-speed USB 3.0 interface. This board, known as Panther, can allocate up to 16 TDC channels [see Fig. 4(a) and (b)] [13]. The TDCs are implemented based on a tapped-delayed line architecture achieving an LSB of 4.7 ps and a single-shot resolution of $12 \text{ ps } \sigma$ [14]. A full scale-range of $2.4 \mu\text{s}$ is obtained utilizing the nutt technique (see Table I) [15]. The total FPGA occupation per channel is 1200 SLICES, 54 kbit BRAM, and 1 DSP48E1. The 16 TDCs have a common stop signal connected to an internally generated clock, and the start signals are externally interfaced through a low-jitter comparator [see Fig. 4(a)].

We estimated the energy of the gamma event using the time-over-threshold (ToT) technique. For this reason, we connected two TDC channels per SiPM standard terminal (ST) in order to timestamp the falling and rising edges of the energy signal (see Fig. 3). The gamma-photon timemark estimation was performed by a single TDC connected to the FT after amplifying its signal with a metal-shielded case wideband amplifier of 30 dB gain and 2.5 GHz bandwidth (Minicircuits ZKL2R5).

As observed in Fig. 5(c), we obtained a CRT of $122 \pm 8.9 \text{ ps}$ FWHM and the uncalibrated ToT spectra of both detectors are shown in Fig. 5(a) and (b). In the latter measurements, we utilized one of these detectors as a reference with an SDR of 86.3 ps FWHM. The SDR is derived from the measured CRT of 122 ps by considering the two detectors with identical SDR.

B. Fast Terminal Multiplexing

Second, we built SiPM array test circuits in order to evaluate the impact of sharing FTs on the same TDC channel. The circuit was divided into three test structures: 1) single SiPM; 2) row of SiPMs with Schottky diodes; and 3) SiPM row without Schottky diodes (see Fig. 6).

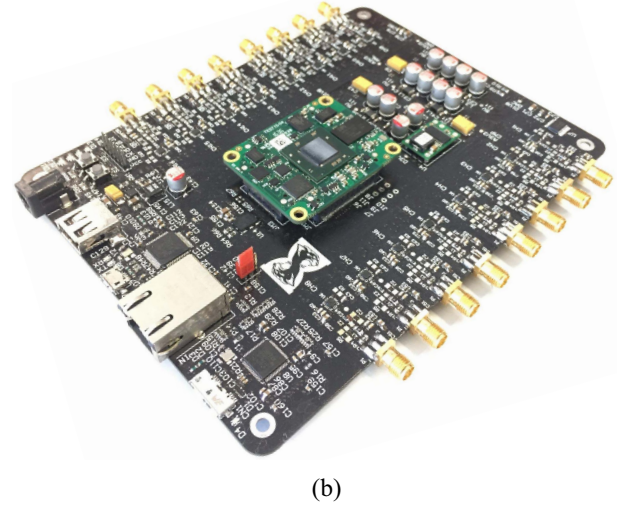
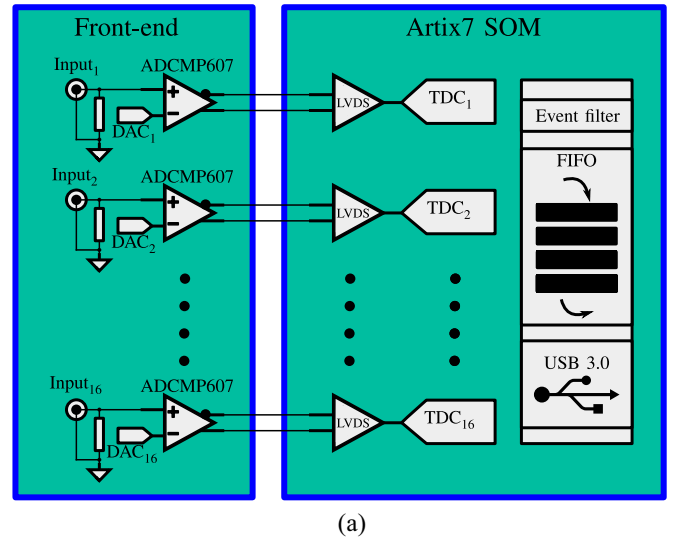


Fig. 4. Panther board. (a) Simplified system block diagram. (b) Panther board photograph.

TABLE I
PANTHER BOARD PERFORMANCE SUMMARY TABLE

Feature	Value
Number of channels	16
Logic per channel	1200 Slices, 54kbit BRAM, 1 DSP48E1s
Channel latency	110 ns
Maximum channel rate	20 MHz
System-on-module	Artix7 Trenz
Single shot resolution	12 ps (σ)
full scale range	2.4 μs

In the first test structure, the single SiPM's FT was connected to a surface-mount wideband amplifier (BGA2818) (see Fig. 7). And, its ST was connected to a transimpedance amplifier (TIA) based on the OPA656 (see Fig. 8). The single SiPM is the number 13 on the 4×4 SiPM array (see Fig. 6). The hysteresis value ADCMP607 that connected the BGA2818 was kept as low as possible by removing its programming resistor, in order to achieve an accurate leading edge threshold.

In the second test structure, the FTs were connected in parallel through Schottky diodes in order to partially decouple their output capacitance (see Fig. 9) [20], [21]. In addition, an

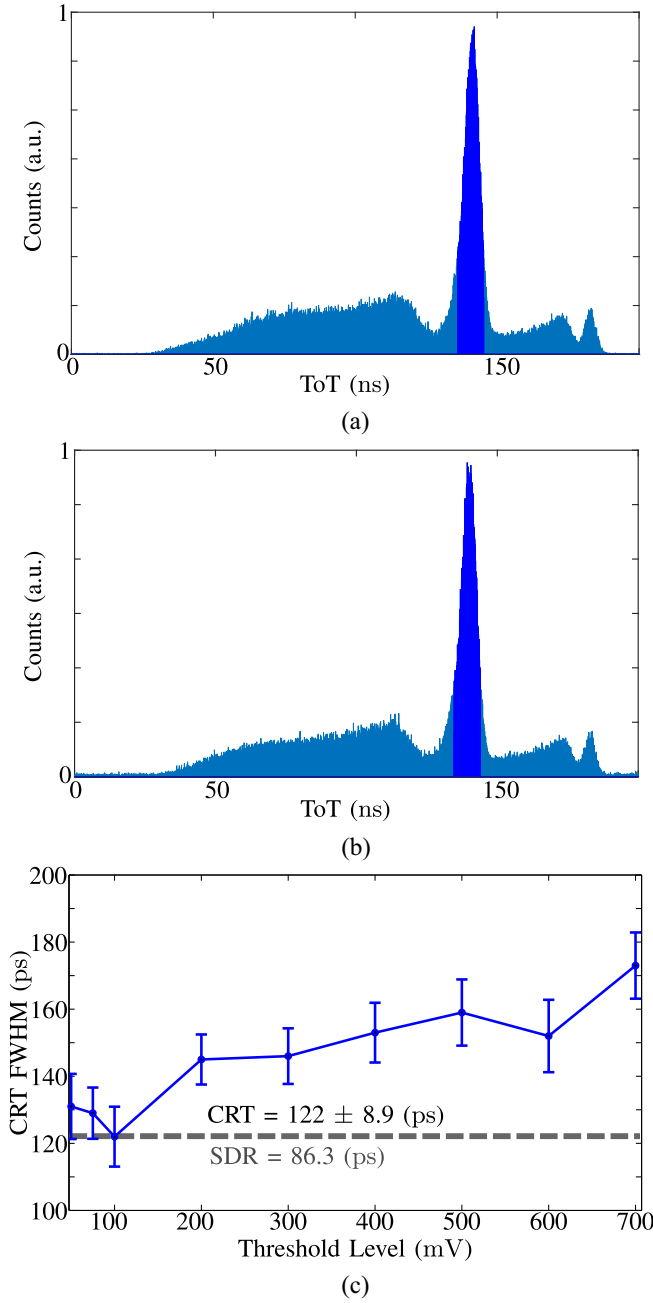


Fig. 5. Reference detector timing calibration. (a) ToT spectrum of the first detector. (b) ToT spectrum of the second detector. (c) CRT threshold scan.

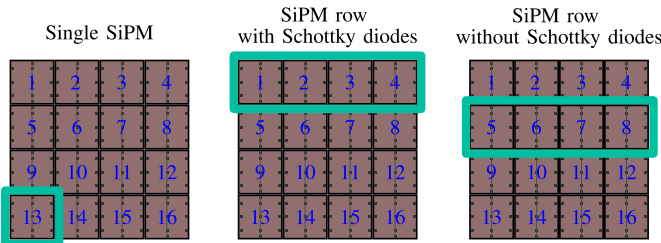


Fig. 6. Location of the SiPM array test circuits.

external bias voltage can be applied to the Schottky diodes that guarantees a faster signal transmission from the FTs to a second BGA2818 wideband amplifier [20], [21]. The STs were

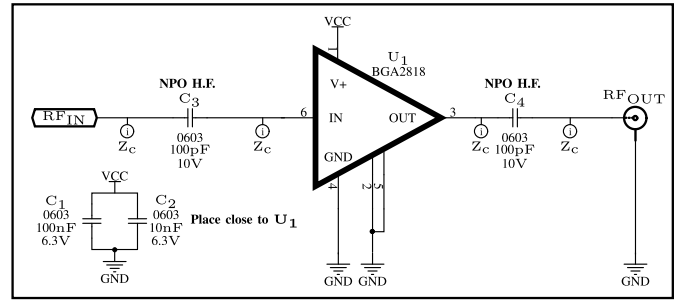


Fig. 7. RF amplifier schematic.

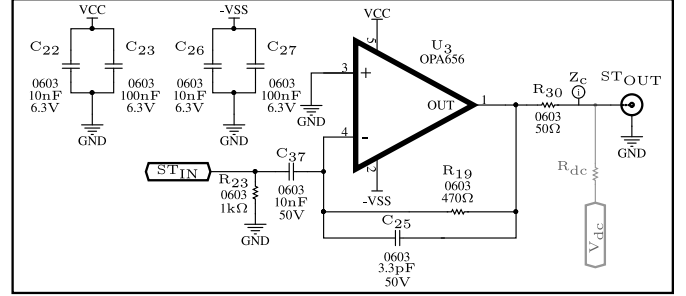


Fig. 8. TIA schematic.

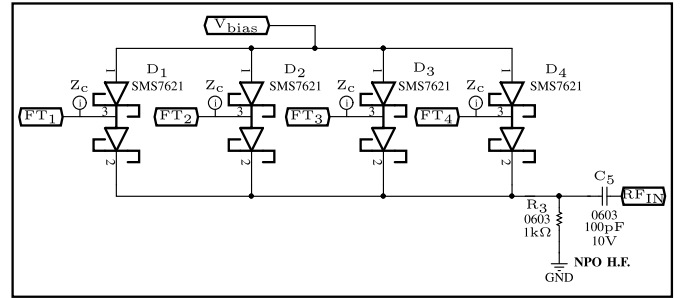


Fig. 9. Schottky circuit schematic.

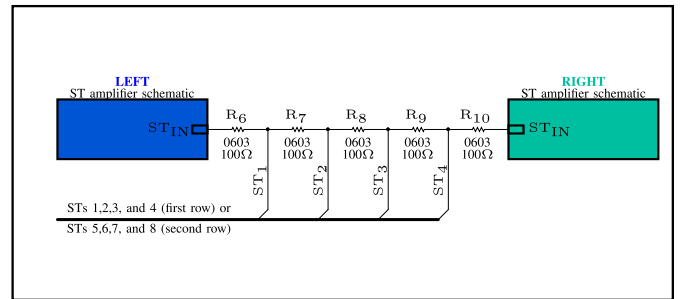


Fig. 10. Scintillator pixel encoding circuit schematic.

connected into a resistor divider chain, which is amplified by two additional TIAs, for scintillator pixel identification and energy estimation (see Figs. 8 and 10). The TIAs are called left and right amplifiers (see Fig. 10). This circuit connected the SiPMs 1–4 (see Figs. 6 and 10).

The third test structure is similar to the second but the FTs were connected directly to a third wideband amplifier without any Schottky diodes. Also, two additional TIAs

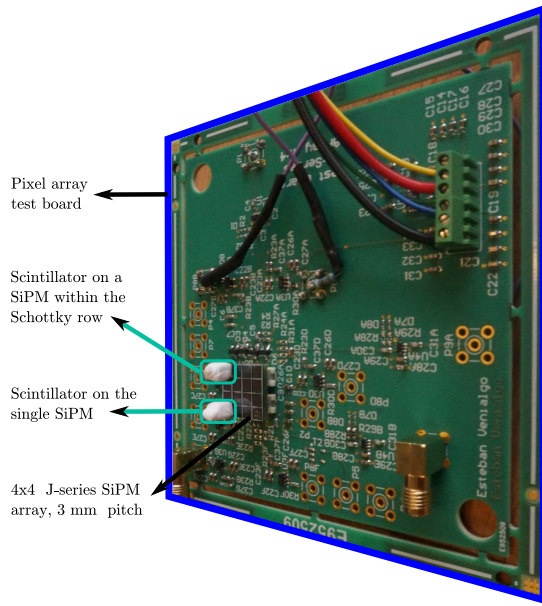


Fig. 11. Photograph of the custom SiPM array testing board.

were connected in a second scintillator pixel encoding circuit (see Figs. 8 and 10). This circuit connected the SiPMs 5–8 (see Figs. 6 and 10).

In the actual hardware, the TDCs, comparators, and DAC references were located into the Panther board [see Fig. 4(a)]. A custom SiPM array testing board, which allocated the rest of the circuits, was built with off-the-shelf surface-mount wideband amplifiers (BGA2818), Schottky diodes (SMS7621), and TIAs based on the OPA656 (see Fig. 11). We chose small footprint SMD components in order to verify their performance and confirm that a compact PET readout circuit can be designed in this way.

First, we verified the performance of the single SiPM circuit in terms of timing, which is based on the BGA2818 instead of the bulky Minicircuits ZKL2R5. We attached a $3 \times 3 \times 5 \text{ mm}^3$ scintillator of LYSO Gen3 from Saint-Gobain to the SiPM 13 (see Figs. 6 and 11) and measured the CRT against the reference detector (see Figs. 11 and 12) [22]. In this measurement, only the single SiPM test circuit and reference detector signals were connected to the Panther board. The CRT threshold scan is depicted in Fig. 13 and no significant change was observed between the reference detector characterization and this measurement. We concluded that no timing degradation was detected between the timing channel based on the Minicircuits ZKL2R5 and that based on the BGA2818.

Second, we studied the timing resolution of the SiPM row that shares a single timing channel through Schottky diodes. This measurement was also performed against the reference detector. We connected the circuits of the corresponding SiPM row and the reference detector to the Panther board [see Figs. 4(b) and 6]. We attached the scintillator of $3 \times 3 \times 5 \text{ mm}^3$ scintillator of LYSO Gen3 to the SiPM 1 (see Figs. 6 and 11), aligned the reference detector, and disconnected the single SiPM test circuit (see Fig. 11). Consequently, in this SiPM row one out of four SiPMs has a scintillator;

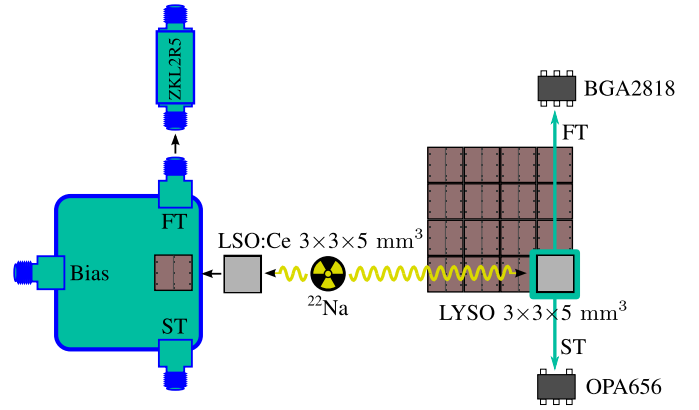
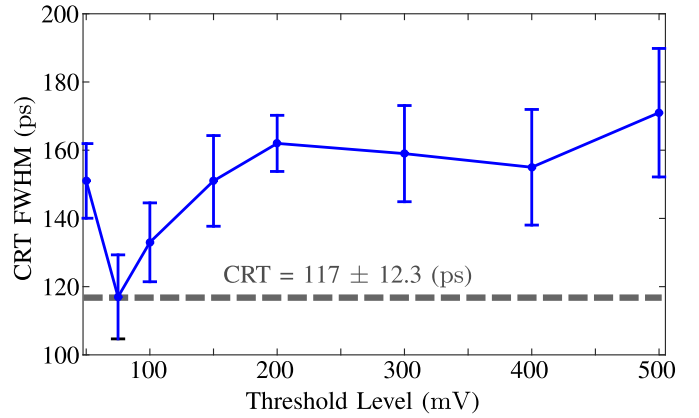


Fig. 12. Measurement block diagram of the single SiPM setup.

Fig. 13. CRT threshold scan of the single SiPM within the 4×4 array.

however, the four SiPMs of the row were biased and had the FTs connected. If nonuniformities, such as breakdown voltage variation, become significant, they can be compensated for by implementing an individual overvoltage-adjustment circuit based on ultralow power DACs such as DAC088S085.

The minimum measured CRT was $128 \pm 7.8 \text{ ps}$ [see Fig. 14(a)] but at a lower threshold, which increases the sensitivity to threshold variations. The amplitude of the FT signal is slower in comparison to the single SiPM circuit because it is loaded with extra capacitance, which is partially decoupled by the Schottky diodes, added by the row FTs. After subtracting the SDR of the reference detector in quadrature and assuming two identical detectors, we extrapolated a CRT* of 138 ps FWHM. In addition, we performed a Schottky bias scan at a fixed comparator threshold, which was 10 mV. The best of CRT performance was achieved when each Schottky diode was biased at 1.5 V, showing a current of $337 \mu\text{A}$ per diode [see Fig. 14(b)].

Last, we reglued the $3 \times 3 \times 5 \text{ mm}^3$ scintillator of LYSO Gen3 from the SiPM row with Schottky diodes to the SiPM row without Schottky diodes (SiPM 5). And, we reconnected the Panther board to that SiPM row. The result of the CRT threshold scan of this case is shown in Fig. 15. The measured CRT was $135 \pm 10.3 \text{ ps}$ and the extrapolated CRT* assuming identical detectors was 147 ps FWHM.

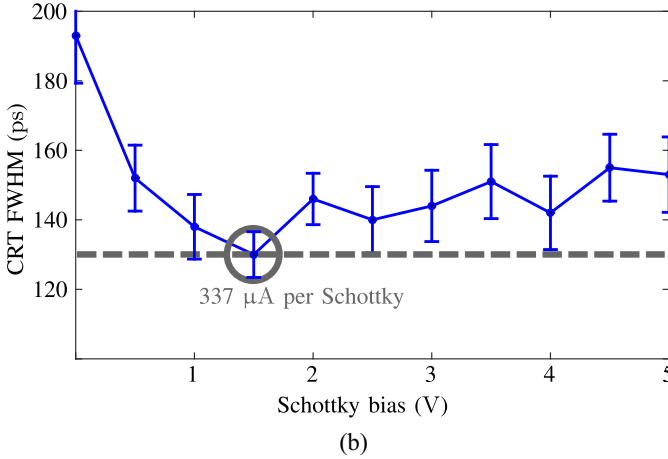
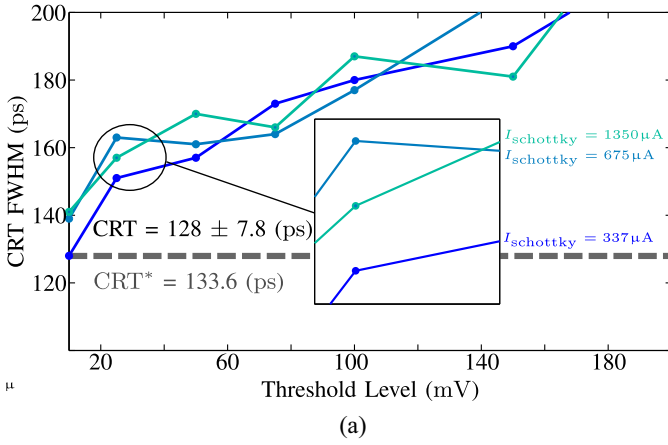


Fig. 14. CRT threshold scan of the SiPM within the Schottky row. (a) CRT threshold scan. (b) Schottky diode bias scan at a fixed comparator threshold.

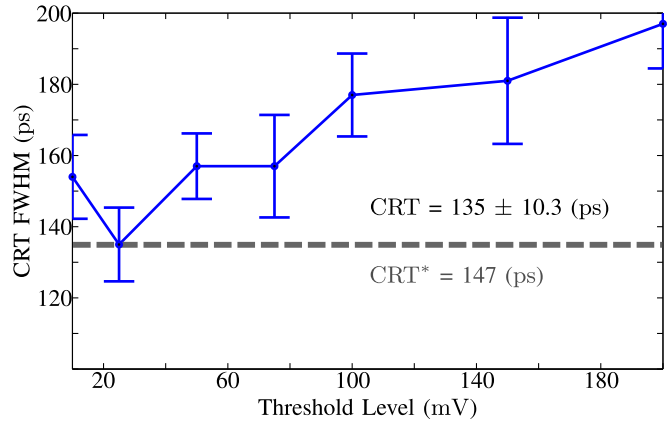


Fig. 15. CRT threshold scan of the SiPM row without the Schottky diodes.

C. Timing Signal Waveforms

For comparing the output signals of the timing circuits, a source of ^{137}Cs was placed close to the detectors in order to obtain a maximum deposited energy of 662 keV, which is close to 511 keV. We reglued the $3 \times 3 \times 5 \text{ mm}^3$ scintillator of LYSO Gen3 onto the SiPMs 1, 5, and 13. An oscilloscope with 2.5 GS/s and 500 MHz bandwidth was connected to the BGA2818 outputs. Since several amplitudes were measured

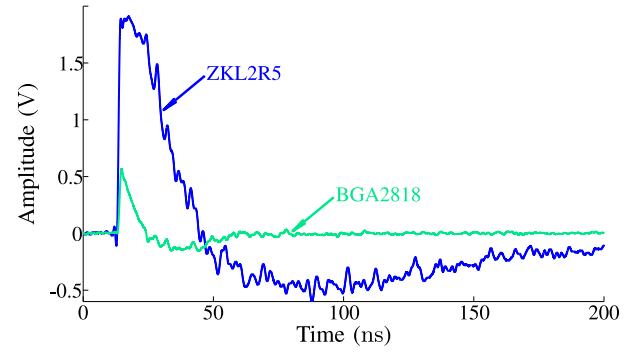


Fig. 16. FT captured waveforms of single SiPMs amplified with BGA2818 and Minicircuits ZKL2R5.

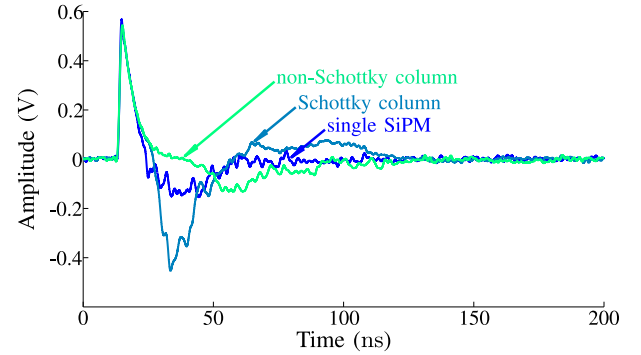


Fig. 17. FTs captures of the SiPM 13, the Schottky row SiPM 1, and the non-Schottky row SiPM 5 amplified with BGA2818.

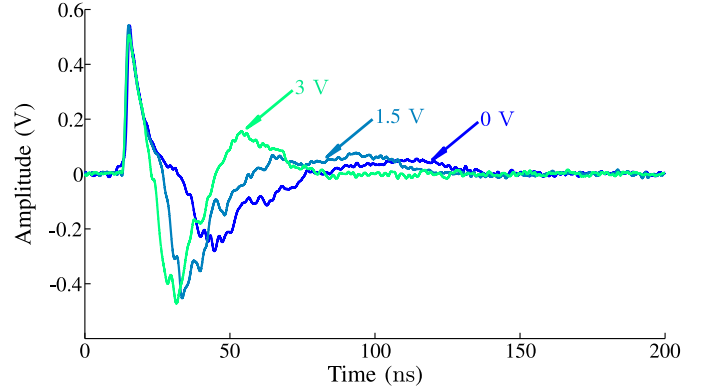


Fig. 18. FTs captures of the Schottky row SiPM 1 amplified with BGA2818 at several Schottky bias voltages.

from the detector, the oscilloscope's trigger was set to the maximum measured amplitude.

Fig. 16 shows the captured waveforms of the array's single SiPM amplified by the BGA2818 circuit and the reference detector amplified by the Minicircuits ZKL2R5. Although the gain of both amplifiers is the same, a lower amplitude is observed from the BGA2818 because of its lower saturated output power. Additionally, the saturated pulse is differentiated by the RC circuit created by the 50Ω load and C_4 (see Fig. 7). However, accurate timing relies on the amplification of the beginning of the timing pulse, which is produced by the early photoelectrons, before reaching the saturated output power of the wideband amplifier [23].

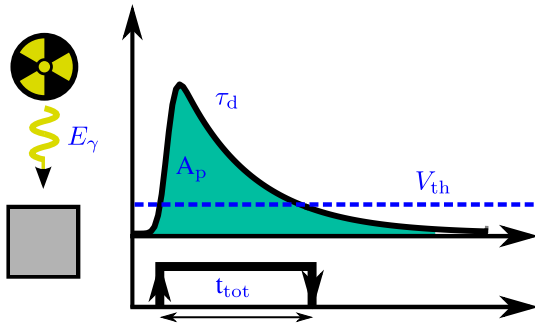


Fig. 19. Energy calibration scheme.

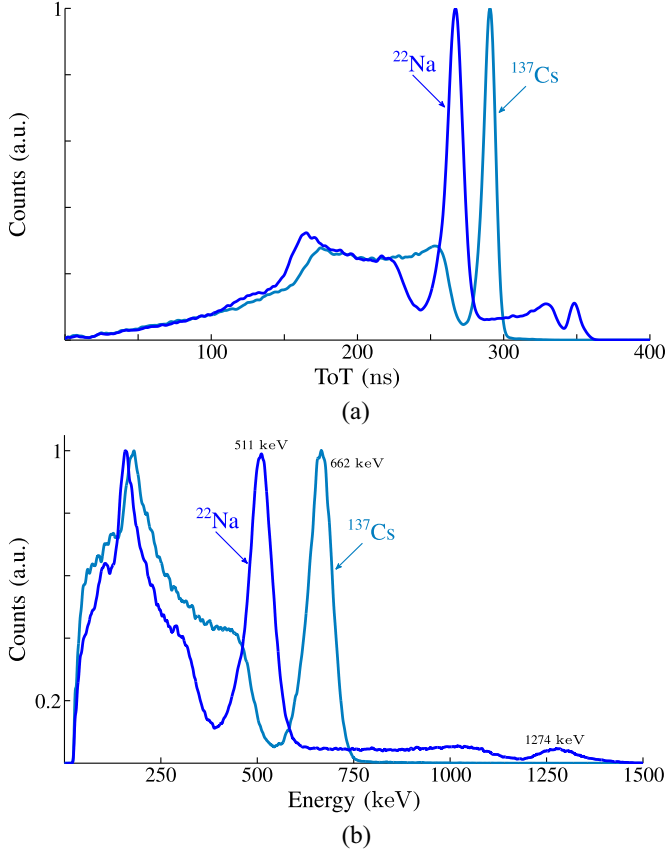
Fig. 20. Energy calibration procedure. (a) ToT energy spectra of ^{22}Na and ^{137}Cs sources. (b) Calibrated energy spectra of ^{22}Na and ^{137}Cs sources.

Fig. 17 compares the captured waveforms of the three testing circuits of the SiPM array (SiPM row with Schottky diodes, SiPM row without Schottky diodes, and single SiPM). In addition, Fig. 18 compares the captured waveforms of the BGA2818 output that is connected to the Schottky row at several Schottky bias voltages. The difference of peak amplitudes was not observed between the SiPM rows with and without Schottky diodes. The tail length variations observed in Fig. 18 are related to the different speeds in which C_5 (in Fig. 9) is discharged that depends on the Schottky biasing.

D. LYSO Pixel Encoding

Since the TIAs' output pulse polarity is negative, a dc voltage was added for connecting the TIAs to the Panther

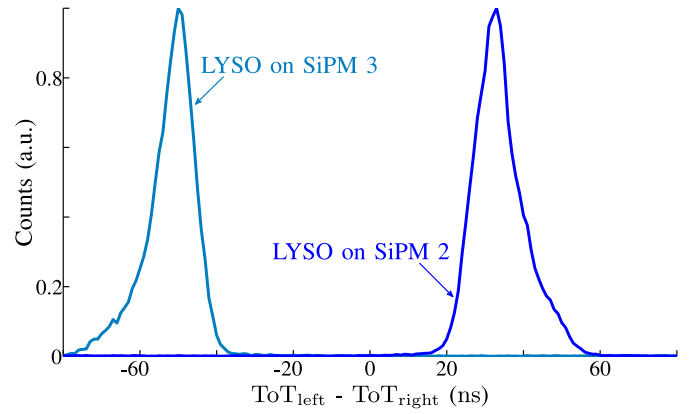
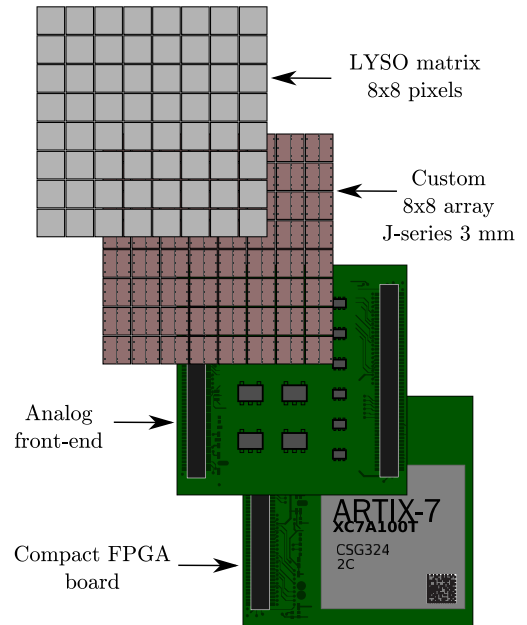
Fig. 21. Time difference histogram between ToT_{left} and $\text{ToT}_{\text{right}}$, when the LYSO scintillator was glued on the SiPMs 2 and 3.

Fig. 22. Full PET block detector description diagram.

board (see Fig. 10), which required a positive input voltage. In order to test the scintillator pixel encoding circuit, the $3 \times 3 \times 5 \text{ mm}^3$ LYSO Gen3 scintillator was glued on the SiPMs 1–4 (see Fig. 6). Then, we captured the corresponding output waveforms of the left and right TIAs for each case, with an oscilloscope of 2 GS/s and 200 MHz bandwidth.

Fig. 23 shows the captured waveforms and the ToT calculations that correspond to the left and right TIAs' signals. In these experiments, we also utilized the ^{137}Cs source and triggered the oscilloscope with the maximum amplitude of the FT. In a full PET module implementation, the dc voltage can be replaced by connecting ST_{IN} to the SiPM cathode, and biasing the anode to negative voltage. The dc voltage causes extra power consumption and R_{dc} produces a slight impedance mismatch.

Additionally, we glued the $3 \times 3 \times 5 \text{ mm}^3$ LYSO Gen3 scintillator on the SiPM 2, place the ^{22}Na source close to the scintillator, and measured the time difference between ToT_{left}

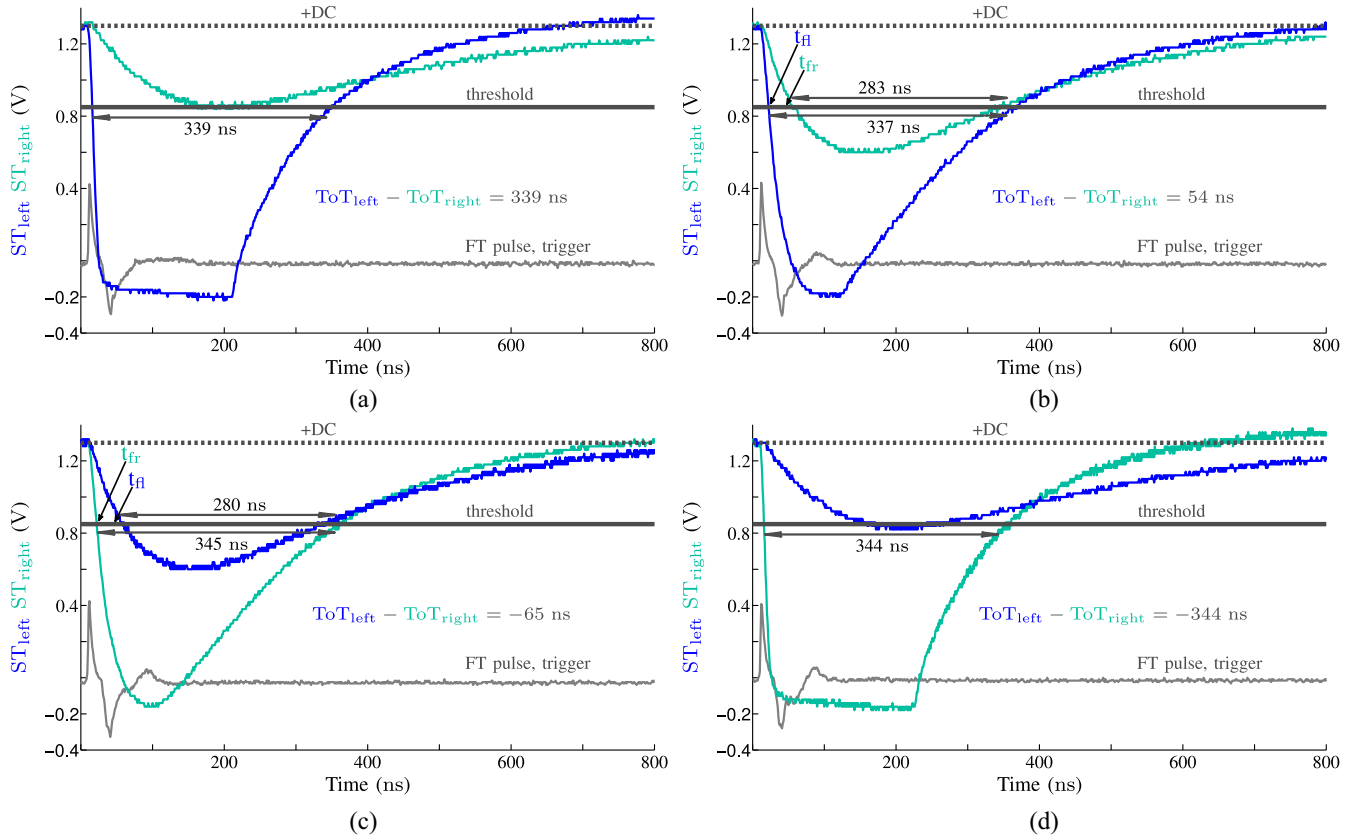


Fig. 23. Oscilloscope captures of the scintillator pixel encoding circuit. Left and right TIA outputs. (a) Scintillator glued on the SiPM 1 of the Schottky's row. (b) Scintillator glued on the SiPM 2 of the Schottky's row. (c) Scintillator glued on the SiPM 3 of the Schottky's row. (d) Scintillator glued on the SiPM 4 of the Schottky's row.

and ToT_{right} with the Panther board. The measured events were filtered by an energy window that captured the entire 511 keV photopeak. We also performed the same experiment on the SiPM 3 in order to verify the LYSO pixel identification. Fig. 21 shows the histograms that corresponds to the two previously explained experiments. Also, the falling edges of the right and left TIA pulses can be used for SiPM 3 and SiPM 2's LYSO pixel identification, since in this architecture the individual fall and rising timestamps are available [see t_{fr} and t_{fr} in Fig. 23(b) and (c)].

IV. ENERGY RESOLUTION

In our previous work, we calculated the energy resolution of a PET detector composed of TDC-on-FPGA and J-series SiPMs [10]. We repeated a similar procedure but on the SiPM 1 (see Figs. 3 and 6). During the measurement the threshold level of the ADCMP607 was 800 mV, which did not allow to observe ^{241}Am pulses (see Fig. 23). Therefore, the third calibration point was the 1274 keV photopeak of the ^{22}Na source.

We calibrated the ToT values into gamma energy following two equations:

$$A_p = V_{th} \tau_d \exp\left(\frac{t_{tot}}{\tau_d}\right) \quad (1)$$

$$E_\gamma = -A_{pmax} \log\left(1 - \frac{A_p}{A_{pmax}}\right). \quad (2)$$

Equation (1) expresses the nonlinearity between area of the pulse and the measured ToT, assuming a single exponential SiPM output pulse. Equation (2) represents the SiPM cell saturation effect. In (1), A_p is the area of ST pulse, V_{th} is the threshold voltage of the comparator, τ_d is the single exponential decay constant, and t_{tot} is the measured ToT. In (2), E_γ is the absorbed gamma energy, and A_{pmax} is the maximum pulse area (see Fig. 19). There are three unknown values, which are V_{th} , τ_d , and A_{pmax} ; therefore, we estimated them by measuring the spectra of three different photopeaks [see Fig. 20(a) and (b)]. Later, we used the calibrated constant to convert the t_{tot} values to its corresponding E_γ by following (1) and (2). The calibrated spectra are shown in Fig. 20(b) where an energy resolution of 14% is achieved. The ToT energy spectra of Fig. 20(a) have more dynamic range than Fig. 5(a) and (b) because the measurement was performed at a lower threshold.

V. OUTLOOK

We propose to use TDC-on-FPGA in combination with a simple analog front-end based on off-the-shelf components in order to build a PET block detector (see Fig. 22). The target application of this PET block detector is brain molecular imaging.

The detector is composed of an array of 8×8 SiPMs of 3 mm pitch and equipped with FTs. The board that allocates the SiPMs on the top layer is customized in order

TABLE II
DETAILED POWER CONSUMPTION AND AREA OCCUPATION DESCRIPTION

	Total devices	Power per device	Area per device	Total power	Total area
BGA2818	8	65 mW	0.87 %	520 mW	7 %
OPA656	16	280 mW	1.01 %	4400 mW	16 %
LT6230-10	16	11 mW	1.56 %	176 mW	25 %
TLV320	16	1 < mW	0.52 %	16 < mW	8.36 %
ADCMP607	8	37.5 mW	1.56 %	300 mW	25 %
total analog power ^a				1.012 W	
Artix7	1	2.5-4 W	40 %	2.5-4 W	40 %

^aPower calculated with LT6230-10 instead of OPA656

TABLE III
ASICs FOR TOF-PET COMPARISON TABLE

	Channels	Trigger	Hit Rate (per channel)	TDCs	Energy Estimation	Max. Throughput	Total Power
STiC3 ^a	64	adjustable	40 kcps	50 ps LSB	ToT	160 Mbps	1.6 W
FlexTOT ^b	16	adjustable	>1000 kcps	non-integrated	ToT	-	0.16 W
TOFPET2 ^c	64	adjustable	600 kcps ^d	31 ps LSB	ToT	3200 Mbps	0.524 W ^e
Outlook design	8 ^f	adjustable	> 1000 kcps	12 ps ^g	ToT	3200 Mbps ^h	1 W+ (2.5-4 W) ⁱ

^aValues according to [5], [26].

^bValues according to [27].

^cValues according to [28].

^dSimultaneous maximum rate in every channel is limited by the data throughput.

^eThis parameter depends on certain settings.

^fIt includes a scintillator pixel encoding circuit in order to allocate 64 SiPMs.

^gThe TDC's single-shot resolution is specified as (σ).

^hThis parameter is limited by the FT600. It can be extended by using the GTP transceivers of the FPGA [24].

ⁱThe FPGA power consumption can be reduced further by optimizing the SOM circuitry (see table II).

to host the small footprint Schottky diodes (SMS7621), in addition to small board-to-board connectors. The analog front-end allocates the fast comparators (ADCMP607), the wide-band amplifiers (BGA2818), and the TIAs circuits based on the LT6230-10. The last board contains a small footprint FPGA (Artix7-100T-CSG324) and all the required circuitry to operate it.

The block detector has independent row circuitries, in order to realize eight independent measurement channels. Each SiPM row also has an independent scintillator pixel encoding circuit that also improves the scintillator identification in order to avoid edge packing effects. The experimental results were measured with four SiPM FTs connected in parallel. However, in the proposed PET block detector, there are eight FTs per column. If the amplitude of the FTs is further reduced, this effect could be mitigated by choosing a wideband amplifier with a larger gain. The total number of required high-accuracy TDCs is 8 (for timing estimation) and the total number low resolution TDCs is 16 for ToT calculations.

The timing experiments were performed utilizing small scintillation crystals in order to verify that state-of-the-art CRT can be achieved with off-shelf-components [23]. However, in the complete PET detector module thicker scintillation crystals are required for detecting the 511 keV gamma photons with high efficiency. Subsequently, timing deterioration is expected with ticker scintillators due to degrading factors, such as light transport variations [9].

A power consumption estimation is shown in Table II. In addition, Table II describes the required area of the components' footprints relative to the detector size. Although we utilized the OPA656 as an TIA, we propose to use the LT6230-10 as a lower power consumption alternative. The Artix SOM

expends 2.5 W when is idle and around 4 W when the 16 TDC channels are operating at full capacity (see Table II). In addition, we included the comparator TLV320 for the scintillator pixel encoding and energy estimation ToT circuits because it has a lower power consumption than the ADCMP607 (see Table II). We kept the ADCMP607 for the timing channels because of its low jitter and programmable hysteresis feature.

The power consumption of a typical PET ASIC is about 25 mW per channel, which leads to a total power consumption of 1.6 W on the 64 channels [5]. In our design, we observe a power consumption, which is around 1 W for the analog front-end in addition to 2.5–4 W for the FPGA and all its required circuitry (see Table II). However, we also include an FPGA per block detector for data post-processing and communication [24]. Power consumption becomes critical in PET scanner implementations with reduced space for a cooling system, such as PET/MRI inserts [25]. Table III compares the proposed detector with respect to state-of-the-art ASICs for TOF-PET.

VI. CONCLUSION

We demonstrated that fully flexible and fast prototyping TOF-PET block detectors can be build from off-the-shelf components, TDC-on-FPGA, and FT-SiPMs. We achieved a sub-120 ps CRT at a single SiPM level. A minimum degradation was observed when multiplexing the FTs with Schottky diodes. We obtained an energy resolution of 14%, which is compatible for the targeted PET applications. In addition, we verified the LYSO pixel identification of an SiPM row composed of four elements.

The Schottky diode decoupling circuit avoids the signal amplitude reduction when connecting FTs in parallel. However, we did not observe a significant CRT degradation in

the multiplexing circuit without Schottky diodes, which is 135 ± 10.3 ps FWHM with respect to the 128 ± 7.8 ps FWHM achieved without Schottky diodes.

We also concluded that the proposed block detector does not lose a significantly large amount of gamma events when the SiPM array shares the same measurement channel row-wise. This requires a measurement channel with a dead time of 1 μ s, which it is already achieved by the Panther board.

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