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An Analog Front-End With Reconfigurable Biasing for Broadband Noise Optimization of Biosensing

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***Abstract*—In the design of ultra-low-noise biosensing analog front-ends, input stage noise optimization remains a critical challenge. This paper presents a reconfigurable capacitive transimpedance amplifier designed for broadband biosensing applications with optimized noise performance. The proposed architecture employs a digitally controlled biasing scheme that adaptively configures the geometry and bias current of the input stage according to the sensor capacitance and target bandwidth. Post-layout simulations in a 40 nm CMOS process demonstrate a consistent transimpedance gain of $154.5\,\mathrm{dB\Omega}$ across all configurations, with bandwidth scalable from $3\,\mathrm{MHz}$ to $82.3\,\mathrm{MHz}$. Input-referred noise is minimized over a sensor capacitance range of $0.4\,\mathrm{pF}$ to $6\,\mathrm{pF}$. For a sensor capacitance of $4\,\mathrm{pF}$, the simulation result shows $29.7\,\mathrm{pA}$ and $7.3\,\mathrm{nA}$ input-referred RMS noise at $500\,\mathrm{kHz}$ and $80\,\mathrm{MHz}$ bandwidth, respectively. The proposed front-end achieves improved noise efficiency with increasing bandwidth, making it suitable for measurements of ion channels, nanopores, and other biosensing applications.**

***Index Terms*—analog front-end, C-TIA, noise optimization, adaptive biasing, biosensing**

I. Introduction

The growing demand for ultra-low-noise and broadband analog front-ends (AFEs) in biosensing applications is driven by emerging fields such as nanopore sensing [1]–[3] and single ion-channel recordings [4], [5]. In these applications, the current generated by the sensor has a bandwidth up to the MHz range, and is converted and amplified into a voltage by transimpedance amplifiers (TIAs). Among typical TIA architectures, resistive TIAs (R-TIAs) offer structural simplicity but are limited by feedback parasitic and constrained bandwidth. In contrast, capacitive TIAs (C-TIAs) are preferred in broadband applications due to their superior signal-to-noise ratio (SNR) performance [6], [7].

One basic AFE with a C-TIA structure is based on an integrator with a feedback capacitor, a cascaded differentiator to restore a flat gain frequency response, and a DC servo-loop to avoid integrator saturation, as shown in Fig. 1. Minimizing the broadband noise of this structure has two fundamental requirements. Firstly, the integrator input stage must exhibit superior noise performance, as it typically dominates the overall noise contribution. Secondly, the DC servo loop should be designed to introduce minimal additional noise. Prior research has demonstrated that employing a continuous-time (CT) approach for the DC servo loop enables high bandwidth while avoiding extra noise at higher frequencies [8]–[10]. In contrast, optimizing the noise performance of the input stage remains a persistent challenge. A widely accepted noise optimization method, known as the capacitive matching rule

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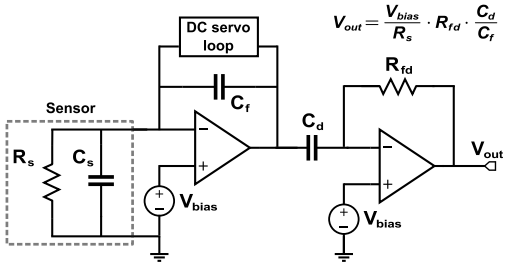

Fig. 1. Conventional integrator-differentiator structure

[11], [12], indicates that a TIA with a MOS-based transistor front end achieves its minimum noise when the input transistor is sized so that its intrinsic capacitance is close to the sensor capacitance. However, the existing capacitive matching rule primarily focuses on optimizing the thermal noise of the transistor while neglecting flicker noise, which significantly impacts noise performance at both low and medium frequencies. Minimizing flicker noise typically requires a lower bias current for a given transistor area, or a larger area for a given bias current, which in turn reduces its intrinsic capacitance, thereby shifting the optimal design point away from that predicted by the capacitive matching rule [13]. As both thermal and flicker noise are frequency-dependent but exhibit distinct frequency dependencies, the design trade-off between them introduces bandwidth range as a critical consideration. For broadband noise optimization, the TIA biasing conditions should be adjusted in accordance with the target operating bandwidth to achieve the best possible noise performance. In this work, we present an AFE featuring a reconfigurable biasing C-TIA to optimize the broadband noise performance of biosensor current readout systems. Depending on the sensor capacitance and the target bandwidth, the C-TIA is adaptively biased through adjustments in device geometry and driving current to achieve optimized noise performance. This article is organized as follows. Section II shows the noise analysis of a typical C-TIA and introduces the proposed circuit architecture. Section III discusses the circuit implementation. Section IV presents the post-layout simulation results and Section V summarizes this article.

II. Working Principle and System Architecture

A. C-TIA Noise Analysis

Fig. 2(a) illustrates the distribution of dominant noise sources of the C-TIA. Over the frequency range of interest, the noise contributions from the differentiator stage, the sensor resistance, and the DC servo loop are assumed to be non-dominant. The input-referred noise power spectral density

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(PSD) of the C-TIA is characterized by two noise components from the input stage of the integrator opamp: S_{v_f}, representing the input-referred flicker noise, and S_{i_d}, denoting the channel thermal noise. For a biased MOS transistor, the terms B and D define the corresponding transfer parameters. Their symbolic expressions are given by:

$$S_{v_f} = \frac{K_F}{C_{OX}^2 WLf}\left(1+\frac{V_{ov}}{V_{KF}}\right)^2, \tag{1}$$

$$S_{i_d} = 4kT\gamma g_m, \tag{2}$$

$$B = -\frac{1}{g_m}, \quad D = -\frac{sC_{iss}}{g_m} \tag{3}$$

where k is Boltzmann's constant, T is the absolute temperature, K_F [$\mathrm{C}^2/\mathrm{m}^2$] is the flicker noise coefficient, and C_{OX} [F/m^2] is the oxide capacitance per unit area. W and L denote the channel width and length, respectively. The increase in flicker noise under strong inversion is modeled using the gate overdrive voltage V_{ov} and parameter V_{KF} as an inversion coefficient dependency of K_F. The input transistor's transconductance is denoted by g_m, and C_{iss} is the intrinsic capacitance [14]. Given a sensor capacitance C_s and feedback capacitance C_f, the total input-referred current noise PSD $S_i(f)$ can be written as:

$$\begin{aligned} S_i(f) &= \left|Bj2\pi f(C_s+C_f)+D\right|^2 S_{i_d} \\ &\quad + (2\pi f)^2(C_s+C_f)^2 S_{v_f} \\ &= \underbrace{\frac{(C_s+C_f+C_{iss})^2}{C_{iss}f_T}\cdot 8\pi kT\gamma f^2}_{\text{Thermal noise}} \\ &\quad + \underbrace{\frac{1}{C_{iss}}\left(1+\frac{V_{ov}}{V_{KF}}\right)^2 \cdot \frac{8\pi^2 K_F(C_s+C_f)^2}{3C_{OX}} f}_{\text{Flicker noise}} \end{aligned} \tag{4}$$

where f_T is the unity gain cut-off frequency of the input transistor denoted as $g_m/2\pi C_{iss}$, and C_{iss} is approximated by $C_{iss} = \frac{2}{3}WLC_{OX}$. By neglecting the flicker noise term in (4), the optimal noise design indicates that the intrinsic capacitance should be equal to the sum of the source capacitance and the feedback capacitance, while the transistor operates at its maximum f_T, as predicted by the capacitive matching rule [11], [12]. However, below the corner frequency f_c, where thermal noise is equal to flicker noise, the latter becomes the dominant contributor to the overall noise performance, as illustrated in the PSD diagram of a typical C-TIA in Fig. 2(b). In these conditions, to minimize flicker noise, the input transistor can either be enlarged in size or biased with reduced current, thus operating in the weak-inversion region. Based on the above analysis, a reconfigurable system with two design strategies is proposed to optimize the broadband noise performance of C-TIAs. For high-frequency operation ($f \gg f_c$), the input transistor should be biased to achieve the highest possible f_T and match its intrinsic capacitance C_{iss} to the sum of the feedback capacitance and the source capacitance to suppress thermal noise. On the other hand, for low-frequency operation ($f \ll f_c$), the bias current of the input transistor should be reduced, or its area should be increased to suppress flicker noise.

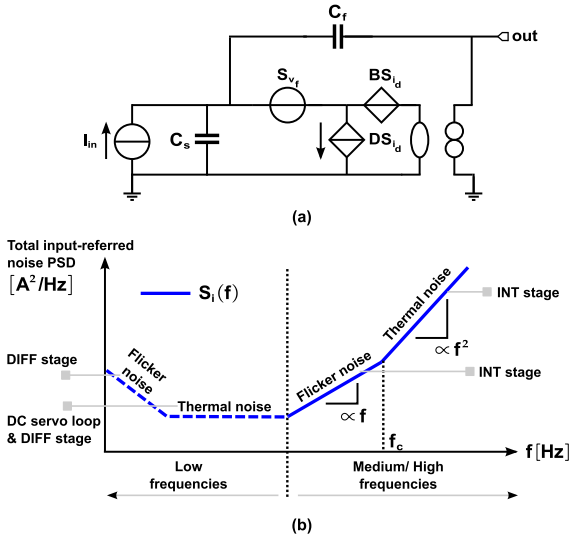

Fig. 2. (a) Dominant noise sources of C-TIA driven from a capacitive source. (b) The input-referred noise PSD of the C-TIA, with I_{in} defined as the input current, includes noise contributions originating from the integrator (INT) stage and the differentiator (DIFF) stage.

B. Reconfigurable C-TIA architecture

The proposed reconfigurable C-TIA is illustrated in Fig. 3. It consists of 2^N integrator channels. Among these channels, one channel is designated for low-frequency operation, while the remaining 2^N-1 channels are configured for high-frequency operation. Each channel includes a low-noise opamp, a feedback capacitor, and a DC servo loop to prevent output saturation. The operational state is determined by N digital inputs, denoted as A_0 through A_{N-1}, which allows the C-TIA to be reconfigured for 2^N-1 different sensor capacitance. By default, all digital inputs are set to zero, placing the system in low-frequency operation, during which the high-frequency channels are disabled by grounding their respective V_{bias} signals. In the low-frequency configuration, the opamp is designed with reduced bias current, resulting in lower bandwidth and power consumption, which effectively suppresses flicker noise without enlarging geometry. To increase bandwidth while maintaining optimal noise performance, the system switches to high-frequency operation. In this mode, the capacitive matching rule is applied by proportionally scaling both the bias current and the geometry of the input transistor to match the sensor capacitance. This enables optimal noise performance across varying sensor conditions and bandwidths.

Targeting applications in ion-channel readout circuits [4], [5], the system is designed with $N = 4$, optimizing noise for a maximum capacitance of $C_{max} = 6\,\mathrm{pF}$ and a unit capacitance of $C_{unit} = 0.4\,\mathrm{pF}$, which corresponds to the intrinsic capacitance of the basic input stage. For example, under high-frequency operation with a sensor capacitance of $C_s = 3.6\,\mathrm{pF}$, the ninth channel is enabled, and the digital control inputs are configured as $A_3 = 1$, $A_2 = 0$, $A_1 = 0$, and $A_0 = 1$.

The connection between the C-TIA and the sensor is modeled using ideal switches. Since each channel has an independent input, only one can be connected to the sensor at any time, with the connection logic governed by the digital

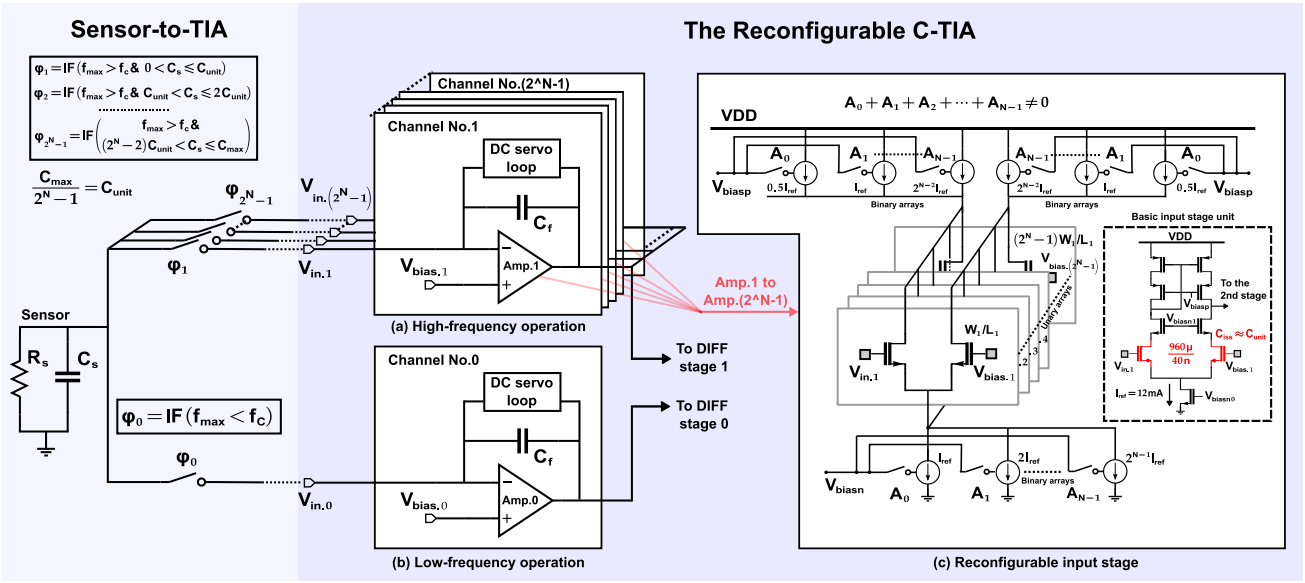

Fig. 3. The proposed reconfigurable C-TIA architecture and the connection principle between the sensor and the TIA. (a) High-frequency operation and (b) Low-frequency operation are two working states of the proposed C-TIA. In high-frequency operation, the transistor-level design of the opamp is shown in (c), where the geometry and bias current of the input stage are configured based on digital inputs A_0 to A_{N-1}.

inputs. In practical PCB implementation, manual switches are used in place of MOS switches to prevent additional noise.

III. Circuit Implementation and Design

A. Reconfigurable input stage for noise optimization

The implementation of the reconfigurable input stage is depicted in Fig. 3(c). In high-frequency operation mode, the amplifier array design utilizes linear scaling by varying the width of the input transistor while maintaining a constant channel length. This approach enables the intrinsic capacitance to scale proportionally with power dissipation while preserving both gain and signal swing. The linear scaling strategy differs for the biasing network and the input transistors. For biasing, binary current source arrays are employed, controlled by digital inputs A_0 through A_{N-1}. In contrast, the input transistor array is implemented as a unary structure to avoid excess noise from gate switches, with the cost of increased area. The basic input stage unit adopts a telescopic cascode structure, where the input transistor is designed with the minimum channel length of the technology ($L = 40\,\mathrm{nm}$) to achieve the highest possible f_T. I/O transistors are used as biasing devices to ensure sufficient saturation margin within the cascode configuration. Due to the small-signal variation in transconductance g_m and output resistance r_0 caused by linear scaling across different configurations, a shared Class-AB output stage is employed as the second stage. This arrangement ensures adequate gain and bandwidth are maintained for all operational configurations.

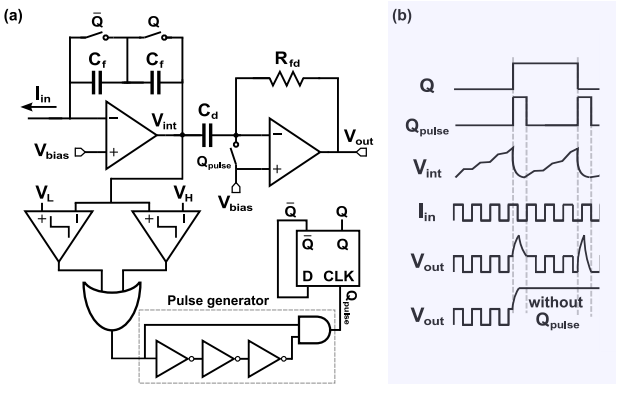

Fig. 4. (a) DC servo loop and (b) its timing diagram.

B. DC servo loop

A self-timed switched-capacitor reset network [10] is implemented as the DC servo loop, as illustrated in Fig. 4(a). Two complementary control signals, Q and $\bar{Q}$, alternately configure the integrator stage between two identical feedback capacitors C_f. During the operation of the DC servo loop, one capacitor-switch pair is active while the other is in the reset state. When the integrator output exceeds a predefined threshold range $[V_L, V_H]$, the control signals Q and $\bar{Q}$ are toggled to initiate a reset of the integrator output. The proposed CT reset approach, which operates without an external reset clock, allows the integrator bandwidth to remain independent of the sampling rate. The dominant noise contribution from the DC servo loop arises from the thermal noise of the reset switches, which is negligible when using transistors with small geometries.

Fig. 4(b) shows the timing diagram of the DC servo loop. The reset transition inherently induces significant output saturation due to the large transient current amplified by R_{fd}. To mitigate this issue, a pulse signal Q_{pulse} is synchronized with Q to short the inputs of the differentiator opamp at the reset instant. This allows most of the transient current to be shunted through the biasing voltage V_{bias}, thereby minimizing the recovery time from saturation.

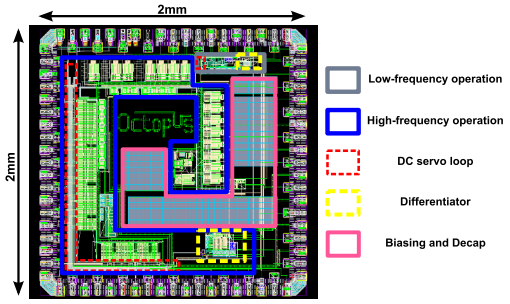

Fig. 5. Layout of the proposed C-TIA.

IV. Post-Layout Simulation Results

The C-TIA is designed with TSMC 40nm CMOS process, occupying a total area of $2\,\mathrm{mm} \times 2\,\mathrm{mm}$. At both $1.1\,\mathrm{V}$ and $2.5\,\mathrm{V}$ supply, the circuit consumes $38\,\mathrm{mW}$ power in low-frequency operation and $252\,\mathrm{mW}$ to $672\,\mathrm{mW}$ power in high-frequency operation, depending on the operation state. The layout is shown in Fig. 5. The differentiator output is connected to a $12.5\times$ buffer with $R_{fd} = 40\,\mathrm{k\Omega}$ during high-frequency operation, and to a unity-gain buffer with $R_{fd} = 500\,\mathrm{k\Omega}$ during low-frequency operation. This configuration results in an ideal transimpedance gain of $50\,\mathrm{M\Omega}$ for both modes, with $C_f = 200\,\mathrm{fF}$ and $C_d = 20\,\mathrm{pF}$. The simulated frequency responses of three operating states are shown in Fig. 6. The proposed C-TIA achieves a transimpedance gain of $153.9\,\mathrm{dB\Omega}$ ($49.5\,\mathrm{M\Omega}$) under both operating conditions. In low-frequency operation, the -3 dB bandwidth is $3\,\mathrm{MHz}$, while in high-frequency operation, the -3 dB bandwidth extends to $82.3\,\mathrm{MHz}$ across configurations ranging from $A_3A_2A_1A_0 = 0001$ to $A_3A_2A_1A_0 = 1111$. The corresponding input-referred noise PSD for each configuration is shown in Fig. 7. The appropriate operating mode can be selected based on the crossover frequency between the two noise PSD curves. For instance, in the case of a $6\,\mathrm{pF}$ sensor, the high-frequency operation should be selected when the measurement bandwidth exceeds f_1 significantly. Fig. 8 presents the simulated input-referred RMS noise at bandwidths of $80\,\mathrm{MHz}$ (Y1) and $500\,\mathrm{kHz}$ (Y2), plotted against the equivalent unary inputs across all configurations. At a bandwidth of $500\,\mathrm{kHz}$, the low-frequency operating mode ($A_3A_2A_1A_0 = 0001$) demonstrates the best noise performance among all configurations, yielding RMS noise currents of $21.1\,\mathrm{pA}$ and $29.7\,\mathrm{pA}$ for sensor capacitances of $2\,\mathrm{pF}$ and $4\,\mathrm{pF}$, respectively. Under high-frequency operation with a bandwidth of $80\,\mathrm{MHz}$, optimal noise performance occurs near the capacitive matching point.

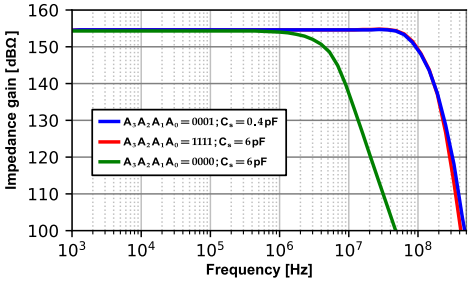

Fig. 6. The simulated frequency response of the proposed C-TIA.

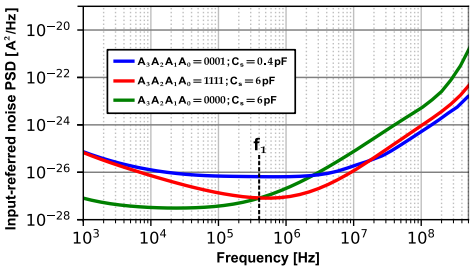

Fig. 7. The input-referred noise PSD of the proposed C-TIA.

Specifically, configurations with $N = 4$ ($A_3A_2A_1A_0 = 0100$) and $N = 8$ ($A_3A_2A_1A_0 = 1000$) achieve minimum RMS noise currents of $5.2\,\mathrm{nA}$ and $7.3\,\mathrm{nA}$ for $2\,\mathrm{pF}$ and $4\,\mathrm{pF}$ sensor capacitance, respectively. The observed deviation from ideal matching conditions is primarily attributed to the parasitic effects of bond pads.

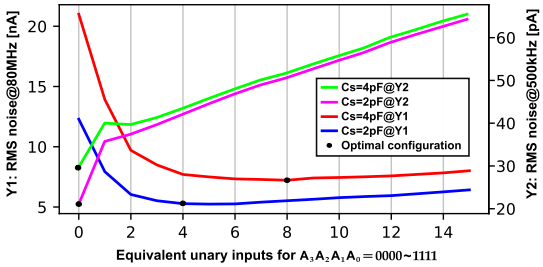

Fig. 8. The input-referred RMS noise of the proposed C-TIA.

Table I summarizes the performance of the proposed AFE and provides a comparison with recent state-of-the-art implementations. A key highlight of this work is the significant enhancement in bandwidth while preserving the optimized noise performance across a range of sensor capacitance, according to the target bandwidth.

TABLE I
Comparison of the Proposed Work with State-of-the-Art.

Works	[10]	[9]	[8]	This work
RMS noise	1.25pA @10kHz	1.8nA @950kHz	NA	29.7pA@(500kHz,4pF) 7.3nA@(80MHz,4pF)
C_s[pF]	NA	NA	1	0.4 to 6
Power[mW]	5.22	65	45	38 to 672
Gain[MΩ]	10	31.6	60	49.5
Bandwidth[MHz]	1.4	0.95	4	Max 82.3

V. Conclusion

In this work, a reconfigurable biasing C-TIA architecture has been presented to optimize broadband noise performance in biosensing applications. By dynamically adapting the input stage geometry and bias current to the sensor capacitance and target bandwidth, the proposed design achieves near-optimal noise performance across varying measurement conditions. In comparison to existing state-of-the-art solutions, the architecture offers a substantial enhancement in bandwidth while maintaining ultra-low noise, making it a promising solution for high-resolution, broadband biosensing AFEs.

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