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***Abstract*—Solder joint failure is one of the most common board-level failure modes in electronic components. It is crucial for a next-generation reliability assessment method to have an in-situ health monitoring system in place to evaluate the current state of degradation. This is achieved by specialized embedded sensors and processing the data on the edge. This study focuses on monitoring the mechanical degradation of package-to-PCB solder interconnects of a WLCSP using a high-resolution piezoresistive sensor. First, a measurement workflow was set up to optimize and significantly improve the sensor readout time. Then, utilizing a design of experiments, the test specimens were subjected to certain combinations of mechanical and thermal loads in a four-point bending setup. Temperature-coupled mechanical loading showed a greater impact on the resulting stress pattern compared to that of a superposition of the corresponding individual purely thermal and mechanical load configurations. Finally, the specimens were tested under a purely mechanical load until failure, and a correlation between the recorded stress pattern and the initiation and propagation of a crack was established.**

Keywords*—*solder joints, fatigue cracking, piezoresistive sensor, degradation monitoring, board-level reliability.

I. INTRODUCTION

Electronic components undergo degradation under the environmental and operating loads, which leads to package-level and board-level failures. These failures occur either due to an event of a sudden change in loads (such as excess temperature, excess current or voltage, mechanical shock, stress or impact, etc.) or a prolonged exposure to nominal operating conditions. About 70% of the failures in electronic components occur during the packaging process, and the predominant failure mode is associated with the solder joints [1].

Temperature, humidity, mechanical vibrations, and dust are the four key environmental factors that are responsible for component degradation, in which the temperature factor is the most dominant one [2] and is responsible for about 55% of the failures; whereas mechanical vibrations contribute to about 20% of the failures [3]. Failures related to semiconductors, connectors, and solder joints together account for over one-third of the share [4]. A solder joint failure is primarily governed by the variation of temperature and mechanical loads [5], [6], and thus, it is one of the key aspects of reliability engineering for IC packages and electronics-enabled systems.

For mission-critical electronics, it is crucial to predict a failure before it occurs. Therefore, it has become increasingly important to have a continuous health monitoring system in place to evaluate the current state of component degradation. This can be achieved by in-situ measurements using embedded sensors and processing the data on the edge. Thus, there is a need to develop and utilize specialized sensors and data processing workflows for in-situ condition monitoring.

There are a few established ways for condition-monitoring of solder joints, such as DC resistance measurement, Radio Frequency (RF) impedance measurement, Multivariate State Estimation Technique (MSET), and Sequential Probability Ratio Test (SPRT) [7], [8], [9]. The measurement of electrical resistance of a path through a daisy chain of solder joints is one of the most common ones. This method allows for the detection of failure (and even monitoring the stages of degradation); however, it is always a challenge to get localized information about a particular solder joint using this method. Another drawback is that the fractured interconnect may remain undetected for a longer time due to maintained spring contact [10]. On the other hand, active devices based on the piezoresistive effect can provide more localized details [11], [12], [13], [14]. Yet, such an implementation generally has to make a tradeoff between more piezoresistive cells and faster data collection, since a single measurement can typically be a lot slower.

This paper attempts to address this challenge by utilizing a high spatial-resolution piezoresistive sensor and optimizing its readout time. A sensor with 2100 piezoresistive cells, arranged in a 70×30 matrix, is utilized to monitor the mechanical degradation of package-to-PCB solder interconnects. First, an efficient software workflow was specifically designed to optimize the sensor readout time and achieve recording a set of data from all the cells within five minutes. Then, a Design of Experiments (DoE) with a four-point bending setup was utilized to study the effect of a combination of mechanical and thermal loads on the sensitivity of the sensor. Finally, the test specimens were subjected to a purely mechanical loading condition until a

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failure was observed. Based on the experimental data, a correlation between the stress pattern at the die, which sits right above the two solder bumps, and the corresponding state of solder crack initiation and propagation was established.

II. STRESS SENSING

The selected piezoresistive sensor consists of an N-type mono-doping resistance piezoresistive module with 2100 cells that are arranged in a 70×30 matrix. Each cell has a size of 10×10 μm^2, and thus, the whole sensor collectively provides a high spatial resolution. This sensor module (*i.e.*, the semiconductor die) is packaged in a test component and then assembled on a Printed Circuit Board (PCB) using the Surface Mount Technology (SMT) process. For this study, the sensor was packaged in a Wafer-Level Chip-Scale Package (WLCSP), where the die and the solder bumps are very close to each other, with only a few BEOL (back-end of the line) layers between them. Figure 1 shows the schematics of the piezoresistive sensor module and its 2100 cells and the footprint of the solder bumps.

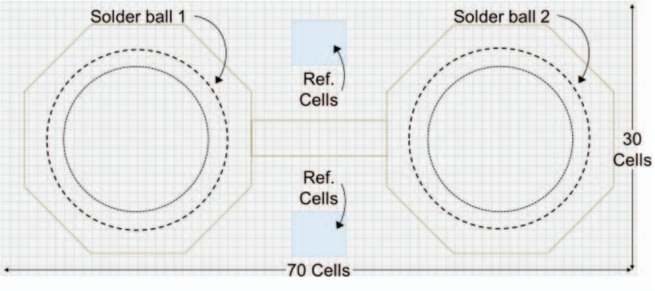


Figure 1: The distribution of the 2100 piezoresistive cells above the two solder bumps of the WLCSP test specimen. The two light-blue regions (strategically chosen not too close to the solder joints, the metal pad, and the package edge) are considered as 'reference' cells for the calculation of the relative change in resistance.

When the test specimen is subjected to thermal loads, it deforms due to a mismatch in the Coefficients of Thermal Expansion (CTE) of different sub-layers. Similarly, a mechanical load, static or dynamic, leads to deformation and damage accumulation. The deformation causes a change in the length of the piezoresistive path, and hence, changes its resistance. This change can be measured by correlating it to the change in current or voltage. Moreover, the resistance change (ΔR) can be expressed as a linear combination of normal stress components (σ_{xx}, σ_{yy}, σ_{zz}), each scaled with the corresponding piezoresistive coefficients (π_L, π_T, π_{out}), as indicated in (1), where π_L denotes the longitudinal, π_T the transverse, and π_{out} the out-of-plane piezoresistive coefficients.

$$\frac{\Delta \mathrm{R}}{\mathrm{R}} = \pi_{\mathrm{L}}\, \sigma_{\mathrm{xx}} + \pi_{\mathrm{T}}\, \sigma_{\mathrm{yy}} + \pi_{\mathrm{out}}\, \sigma_{\mathrm{zz}} \qquad (1)$$

In this way, the data recorded by the piezoresistive cells arranged in a matrix can provide a correlation to the map of stress distribution across the surface of the die. The two blocks of 30 cells marked as 'reference cells' in Figure 1 are used later to process the recorded data and visualize the changes in stress distribution corresponding to only the post-SMT loading conditions. A previous version of this sensor was utilized in [13], which reports that a single measurement (from all 2100 cells) takes up to 50 minutes. This duration is untenably lengthy for degradation monitoring during Board-Level Reliability (BLR) tests, and thus, needs to be optimized.

A. Sensor Readout Optimization

To obtain a stress distribution across the entire surface of the die, all the 2100 piezoresistive cells need to be accessed by address selection followed by data processing. An intermediate 'adapter PCB' was designed and utilized to connect the piezoresistive sensor with a microprocessor, which sends data to a computer. Figure 2 indicates the workflow of the measurement, including the annotations for different ports on the adapter PCB.

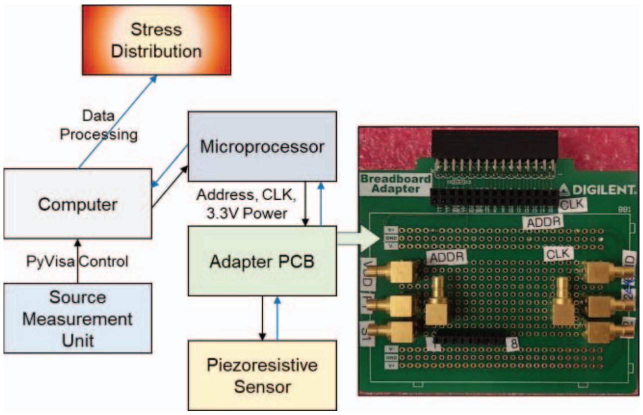


Figure 2: The flowchart for recording measurements from the piezoresistive sensor. The shown adapter PCB has several ports for governing certain signals that are an essential part of the measurement workflow.

The setup utilizes a Source Measurement Unit (SMU). A unique addressing technique was engineered to use a 100-bit address signal to access all 2100 sensor cells. Only when both the row and the column switches are active (set to '1'), are the force and sense ports connected to the desired piezoresistive cell. A Python program was utilized to handle the address allocation. A stable power supply of 3.3 V was also managed and maintained by enabling one DC voltage value with the Python program, which communicates with the SMU using the PyVISA library [15]. Sending the Standard Commands for Programmable Instruments' (SCPI) commands initializes the SMU, setting it to source current while measuring voltage [16].

The finalized measurement algorithm first selects a cell to measure and acquire its column number '*m*' and row number '*n*'. Next, it gives the DC voltage supply between VDD and GND and feeds the CLK port (corresponding to the clock) with 100 cycles square signal. Then, it feeds the address signal simultaneously with the clock signal from ADDR port, with only number 'm' and number '70 + n' of the address signal are set to '1' and the rest to '0'. It then sends a current of 50 µA forces and measurea the voltage between the two sense ports. Finally, it calculates the resistance based on the measured voltage and current and stores the result. This entire process is repeated until all 2100 cells are covered.

The measurement workflow was further improved by implementing a waveform correction to optimize the clock signal frequency. To ensure the accuracy and reliability of the measurements, a repeatability test was also included in the Python code. With these optimization steps, a single measurement from all 2100 cells takes less than five minutes, and thus, a significant reduction in the measurement time was achieved.

B. *Sensor Data Processing*

The optimized measurement workflow generates data when the test specimens with piezoresistive sensors are subjected to thermal or mechanical load. However, the sensor still shows non-zero default values under no load. This reflects the pre-stress resulting from the packaging and SMT processes. In order to record the changes due to the applied loading condition, *i.e.*, a relative change, a certain data processing must be put in place.

To achieve this, two blocks of 30 cells are selected as reference cells. The conductance values are calculated using the reciprocal values of the measured resistance. Then, the reference conductance value is obtained from the reference cells. The choice of these cell-blocks are made such that they are not too close to either of the solder joints. The average value of the selected 60 cells is used as the reference value for calculating the relative change under the applied load. Thus, at any loaded stage, the algorithm first calculates and plots all 2100 values relative to the average reference value. Each cell is then assigned a color based on the relative conductance value to form a gradient, in which red signifies a positive value, yellow the zero, and green a negative value. This results into a spatial plot with a clear gradient and the noise eliminated.

Figure 3 shows an example of the difference between a spatial plot of the absolute values and that of the relative values. These data correspond to a state after 50 thermal cycles relative to the first thermal cycle. The relative values provide a much better insight into the changes and give a much clearer idea of the stress distribution. Using the relative conductance values of each cell, the corresponding stress components can be evaluated using the literature reported values of the piezoresistive coefficients [17] to obtain a stress distribution plot.

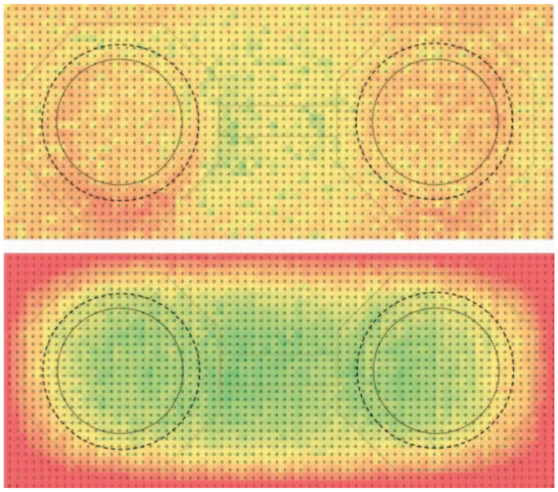


Figure 3: Comparison of the conductance data recorded by a test specimen under a thermal cyclic load, after the 50th thermal cycle. The first spatial plot (above) represents absolute values, while the second one (below) represents relative values.

III. TEMPERATURE-COUPLED BEND TEST

The piezoresistive sensor with its established measurement algorithm was first tested in a temperature-coupled mechanical bend test environment. This is an important intermediate step to characterize and test the component against a static thermal and mechanical load before utilizing it in BLR tests, which typically consider dynamic loads such as thermal cycling and mechanical vibrations. The state of solder joint degradation was monitored under a combination of isothermal conditions and static mechanical loads.

A. *Experimental Setup*

A four-point bending setup equipped with a temperature chamber was utilized to characterize the piezoresistive sensor under a combination of thermal and mechanical loads. Figure 4 shows the schematics of the four-point bending setup annotated with the dimensions (*viz.*, F, d_1, d_2, b, h) relevant for designing experiments. A load span of 30 mm and a support span of 66 mm was utilized (*i.e.*, $d_1 = 15$mm and $d_2 = 33$mm). A PCB with a WLCSP equipped with piezoresistive sensors was utilized as the test specimen such that the package is facing downwards. This orientation requires the recorded data matrix to be flipped horizontally, *i.e.*, along the shorter edge, before further analysis.

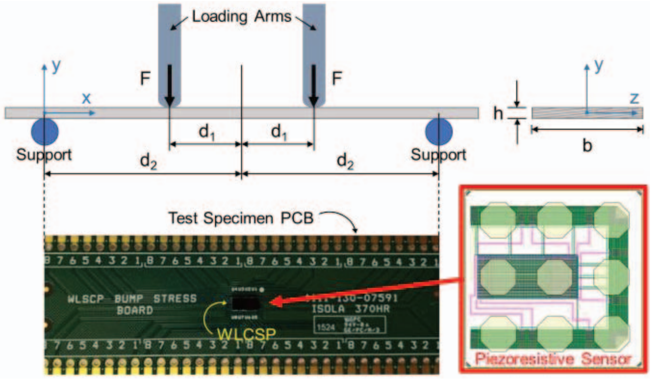


Figure 4: Schematics of the experimental setup for four-point bending with temperature variation. The test specimen PCB has a centrally placed WLCSP, equipped with the piezoresistive sensor.

According to the beam theory, the bending moment remains constant between the two loading arms at a constant applied static force F. The Euler-Bernoulli beam equations lead to the expression in (2) for the maximum bending stress, which occurs at the top-most and bottom-most layer of the beam.

$$(\sigma_{xx})_{\max} = \frac{6}{bh^2} F(d_2 - d_1) \tag{2}$$

$$(\tau_{xy})_{max} = \frac{3F}{2bh} \tag{3}$$

$$v_{max} = \frac{2F}{E_x bh^3}(d_2 - d_1)(2d_2^2 + 2d_1 d_2 - d_1^2) \tag{4}$$

The shear force is non-zero (and constant) only in the two regions between a support and a loading arm, and the maximum shear stress (at the neutral axis of the beam) is given by (3). The maximum bending displacement ($v_{\max}$) at the center of the beam-span is given by (4), where E_x is the modulus of elasticity along the x-direction. The displacement $v_{\max}$ was the considered as a control parameter for applying different mechanical load-steps.

B. Test Specimen

A PCB of the size 84 mm × 29 mm was utilized as the test specimen for the four-point bending experiment. For this study, a single wafer-level chip-scale package containing multiple piezoresistive sensor modules was utilized and assembled on the test specimen PCB. Figure 5 shows the layout of the die in the WLCSP test package that contains 8 piezoresistive sensor modules arranged in a 4×2 grid fashion.

Each unit consists of a total of 9 solder joints. The piezoresistive sensor sits above 2 of those solder joints while the rest are dedicated to circuit connections. Seven of the 8 units on the die feature different piezoresistive modules, providing diverse types of methods for evaluating stress distribution (such as resistance, current factor for MOS, and saturation collector current for bipolar transistors). Figure 5 highlights the location of the single unit that was utilized for the data collection and characterization experiments in this study.

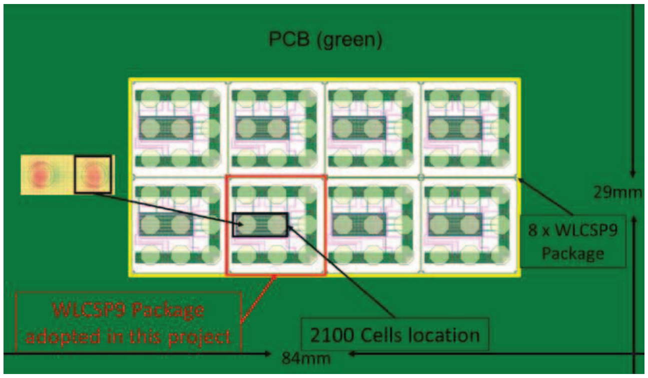
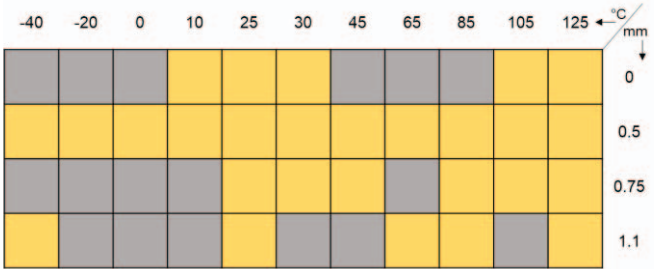


Figure 5: The layout of the die in the WLCSP test package that contains 8 piezoresistive sensor modules arranged in a 4×2 grid.

C. Loading Conditions

A design of experiments was prepared to expose the test specimen to various combinations of thermal and mechanical loads. The DoE considers 11 different temperature steps and 4 distinct mechanical displacements (including the zero displacement). The specimen was exposed to a static mechanical load equivalent of a 0 mm, 0.5 mm, 0.75 mm, and 1.1 mm of bending displacement ($v_{\max}$), along with an isothermal load of different ambient temperature values between -40 °C to 125 °C (*viz.*, -40, -20, 0, 10, 25, 30, 45, 65, 85, 105, and 125 °C). The change in resistance was recorded by the piezoresistive sensor embedded in the WLCSP at various load conditions, and the previously described data processing workflow was followed.

Figure 6 summarizes the DoE and highlights in yellow all the combinations for which data was recorded. A select number of combinations could be covered due to practical limitations. During the test, the PCB was first bent and then the temperature inside the chamber was adjusted in order to minimize the amount of repeated bending. Post each temperature cycle at a certain displacement, the motor reset to the zero displacement position before commencing the next cycle. A complete spectrum of displacements at 25 °C (room temperature) and 125 °C was captured. Similarly, data for all temperature steps at 0.5 mm displacement were collected.



-40	-20	0	10	25	30	45	65	85	105	125	← °C / mm ↓
⬜	⬜	⬜	🟨	🟨	🟨	⬜	⬜	⬜	🟨	🟨	0
🟨	🟨	🟨	🟨	🟨	🟨	🟨	🟨	🟨	🟨	🟨	0.5
⬜	⬜	⬜	⬜	🟨	🟨	🟨	⬜	🟨	🟨	🟨	0.75
🟨	⬜	⬜	⬜	🟨	⬜	⬜	🟨	🟨	⬜	🟨	1.1

Figure 6: The design space considered for the temperature-coupled bend test. The yellow squares indicate the final combinations for which data were recorded within this design of experiments.

D. Data Processing and Analysis

The recorded data was processed utilizing the blocks of 'reference cells' for each reading, as discussed in previous sections. Furthermore, the conductance change was plot relative to the reference state of room temperature (25 °C) and zero displacement, *i.e.*, the (25 °C, 0 mm) combination. The resulting plots of all yellow squares in Figure 6 (except the reference state) were analyzed, and the following two key observations were recorded.

1) Patterns of thermal expansion mismatch

The effect of only temperature variation was studied first. Figure 7 shows the evolution of the recorded pattern over the considered temperature range with a bending displacement of 0.5 mm. In order to accommodate more states, the individual patterns at different temperature values are presented in a 90° counterclockwise rotated way.

A significant change in the stress pattern is observed from low to high temperature values. The region under the left bump (bottom in the figure) first recovers from the green shade with the increasing temperature and then turns red. This signifies the sign change of the measured stress quantity. It is evident that this occurs due to a mismatch in thermal expansion (CTE-mismatch) of different involved materials. At low temperatures, the solder joint can stretch the die towards the center of the die; whereas at high temperatures, the stretch is in the other direction. In addition to showing the changes in the effective stress pattern, this enables visualizing the warpage behavior of the die/package under the influence of temperature variation.

2) Higher sensitivity towards a combined loading

The effect of purely mechanical load was also studied using the configurations corresponding to 25 °C and 125 °C columns in Figure 6. Neither of the two cases showed a significant change in the recorded pattern. For 25 °C cases, the change from 0 to 1.1 mm was nearly linear, whereas all non-zero displacement cases for 125 °C showed nearly the same pattern.

The effect of a combined thermal and mechanical load was also studied by comparing it with the individual effects. Figure 8 shows this comparison for the configuration for 125 °C and 1.1 mm bending displacement. An artificial superposition of the two configurations (125 °C, 0 mm) and (25 °C, 1.1 mm) was created using a vector sum of the values in each corresponding cell of their recorded patterns. A slightly more severe pattern was observed for the combined load.

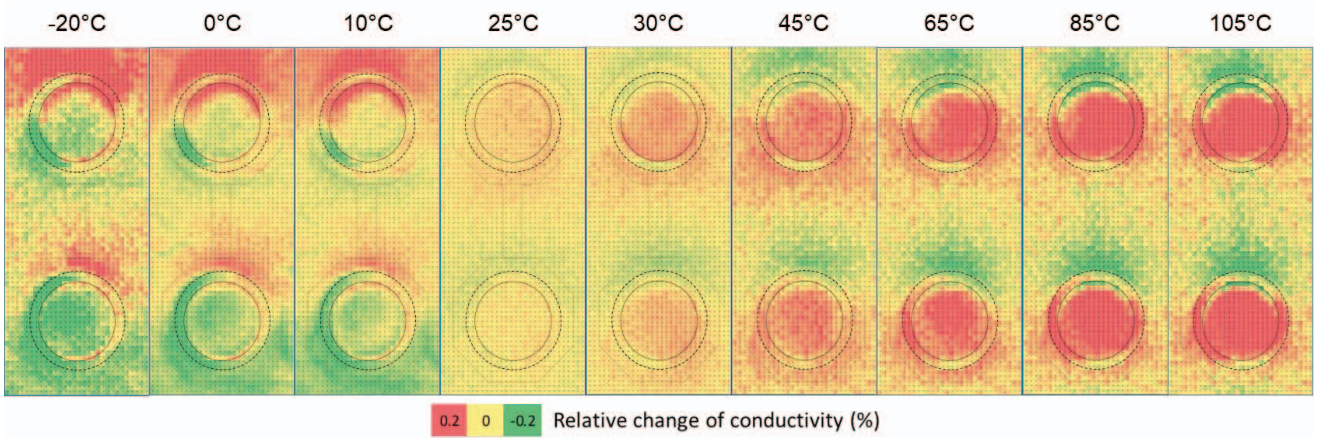


Figure 7: The evolution of the piezoresistive sensor measurements over the considered temperature range with a 0.5 mm bending displacement.

This can be visually confirmed from the marginally darker shades of red and green in the first pattern (above) in Figure 8. It hints that a coupled thermal and mechanical load could result in a more stressed state than the superposition of the individual effects. In other words, an electronic component can be more sensitive to a combination of operating loads than that of their individual effects together. This finding is particularly important, as real-life applications often involve a combination of multiple environmental and operating loads [18].

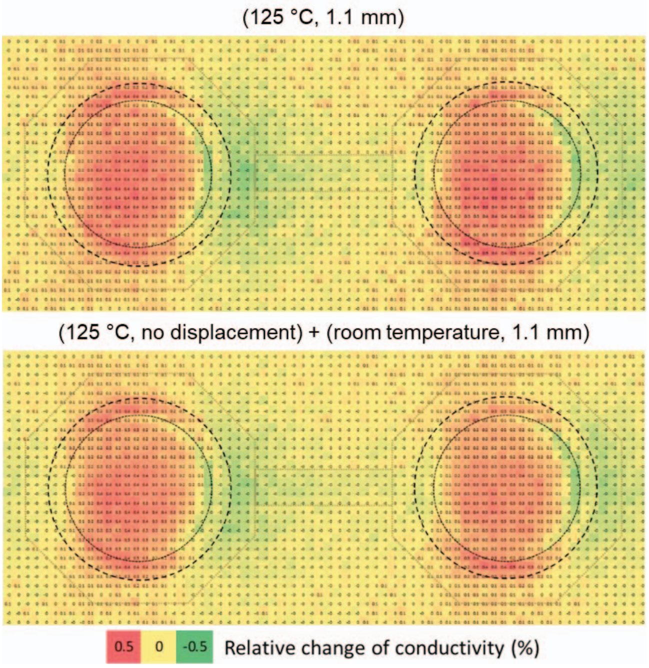


Figure 8: The comparison of the spatial plots obtained from a temperature-coupled bend test configuration (above) with that of a superposition of corresponding individual purely thermal and mechanical load configurations (below). The combined load configuration shows a slightly more stresses state.

IV. MECHANICAL BEND-TEST UNTIL FAILURE

The temperature-coupled bend test included mechanical loads equivalent of up to 1.1 mm of bending displacement, which did not show a significant change in the recorded pattern. Thus, a purely mechanical bend test at room temperature (25 °C) was carried out until a failure in solder joints was observed. The same four-point bending setup and measurement workflow were utilized. The considered $v_{\max}$ values range from 0.5 mm to 10 mm. After reaching each selected displacement value, the fixture maintained that position until two measurements are conducted. Collected data was processed and analyzed relative to the 0 mm displacement configuration. In order to have an effective comparison, a path formed by a single row (number 15 from the top) was selected, which coincides with the horizontal diameters of both solder bumps. The change in conductance was plot for all cells along this path, and this was repeated for all the considered displacement values.

Figure 9 shows the comparison of the obtained plots. The plots gradually move down until $v_{\max} = 3$ mm, and then a trend reversal was observed, which is indicated by yellow arrows in Figure 9. Moreover, a peculiar fluctuation in values was also observed in between the column number 45 and 50 (highlighted with a red rectangle in Figure 9) in the plots corresponding to the displacements larger than 3.5 mm. This location is the inner edge of the right solder joint. To investigate further, cross sections of the test specimen were studied under a Scanning Electron Microscope (SEM). A crack propagated in the region of PCB-solder interface was observed. Thus, it was concluded that the sudden change in the trend of conductance data and the localized fluctuation of values correspond to the release of surface energy due to crack initiation.

Figure 10 shows the cross section image captured by a SEM, and the location of the crack. The corresponding change in the recorded pattern before and after the crack initiation ($v_{\max} = 2$ mm and 4 mm, respectively) are also indicated in Figure 10. This clearly shows that the failure can be detected using the patterns generated using a piezoresistive sensor.

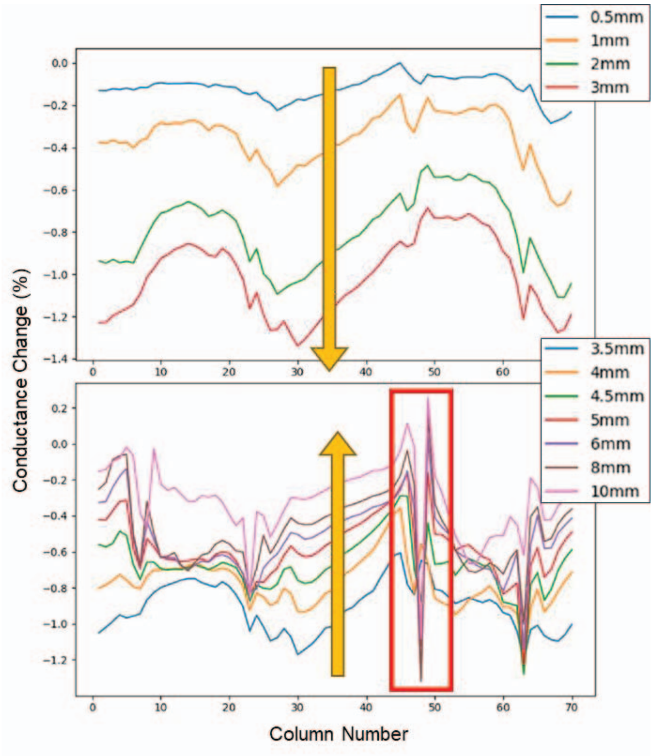


Figure 9: Plots of the conductance change along a path formed by a single row of the piezoresistive cell matrix that coincides with the diameters of both solder bumps. A trend reversal (yellow arrows) is observed after 3 mm of bending displacement, and a high fluctuation in readings (red rectangle) between the columns 45 and 50 indicates the existence of a crack.

Moreover, the patterns captured by the sensor at the stages before the crack was initiated were also further studied. They showed concentration of extreme conductance values (hinting to the stress concentration) around the inner edge of the right bump. This shows that the evolution of 'stress' patterns can serve as an indication of failure before it occurs.

V. CONCLUSION

This study utilizes a piezoresistive sensor with a high spatial resolution of 70×30 cells. With the developed time-optimized measurement workflow, this sensor can be practically used for real-time health monitoring of microelectronics. Moreover, depending on the choice of packaging, it can enable monitoring different layers of an electronic component. The unique construction of a WLCSP enabled in-situ monitoring of solder bumps in this work.

The spatial plots of conductance change provide more and localized information compared to other condition monitoring techniques for solder joints. The spatial plots reflect the changes caused by applied loading conditions. A coupled thermal and mechanical load appears to have a greater impact on resulting stresses compared to an artificial superposition of the individual effects. This aspect can be further investigated by using additional combinations of coupled loads and by including additional loading factors, such as exposure to humidity.

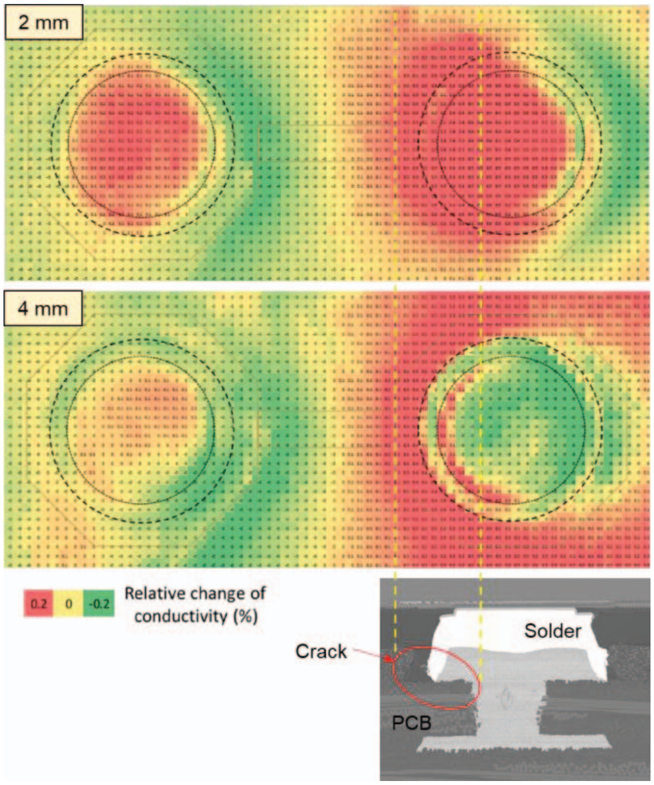


Figure 10: Spatial plots recorded by the piezoresistive sensor before and after the crack initiation (corresponding to the bending displacement of 2 mm and 4 mm, respectively). The cross section observed under a SEM indicates the position of the crack in the region next to the inner edge of the right solder bump.

Mechanical stress components can be visualized by processing the spatial plots of conductance change utilizing the literature reported values of the piezoresistive coefficients. However, these coefficients should be validated for the chosen test specimen/device using a Finite Element-based simulation. We plan this step for future work and thus have presented plots of only the conductance change in this paper.

The spatial plots obtained during the purely mechanical bend test with larger displacements not only helped in detecting a failure, (*i.e.*, the crack initiation) but also in determining the location of the defect. This unique functionality of the piezoresistive sensor has a great potential in applying an edge-based data-driven approach effectively for failure detection and prediction, which is also an essential part of the Digital Twin-based next-generation reliability assessment workflow for electronic components and systems.

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