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A -121.5 dB THD Class-D Audio Amplifier with 49 dB Suppression of LC Filter Nonlinearity and Robust to $\pm 30\%$ LC Filter Spread

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Abstract

This paper reports a Class-D audio amplifier that uses multi-loop feedback to suppress output LC filter nonlinearity by 49 dB, enabling the use of small, low-cost LC filters with $\pm 30\%$ spread while maintaining low distortion. Fabricated in a 180 nm BCD process, the prototype achieves a THD of -121.5 dB and a THD+N of -107.1 dB. It delivers 12W/21W into an $8\text{-}\Omega/4\text{-}\Omega$ load with 91%/87% efficiency.

Introduction

Class-D amplifiers (CDAs) are popular in audio applications due to their high power efficiency. Their switching operation, though, produces high-frequency tones, which often require bulky LC filters to comply with EMI regulations. To reduce LC filter size, recent designs have employed high-frequency (≥ 2 MHz) pulse-width modulation (PWM) schemes [1-3]. This also enables high loop gain (>76 dB in [2, 3]) and thus high linearity (THD < -100 dB). However, LC filters with commensurate linearity are then required, which again leads to increased cost and bulk. Incorporating the LC filter into the CDA's feedback loop can relax these requirements [4, 5]. However, loop stability must be maintained in the presence of LC tolerances, aging, and extra variation due to voltage/current dependencies. This work proposes a CDA achieving -121.5 dB THD and $\pm 30\%$ LC cut-off frequency (f_{LC}) tolerance.

Architecture

Fig. 1a shows the architecture of the proposed CDA. An outer loop around the LC filter is stabilized by a lead compensator, which consists of an inner loop around the PWM modulator ($f_{PWM} = 4.2$ MHz) and the output stage, and incorporates a 1st order RC low-pass filter (LPF) with a corner frequency $f_{RC} = 78$ kHz. Besides ensuring stability, the inner loop 1) provides extra loop gain around the output stage; and 2) decouples the bandwidth (f_{UG}) of the loop around the output stage from f_{LC} , so that the class-D stability criterion $f_{UG} < f_{PWM}/\pi$ [6] is met even in the presence of f_{LC} variations.

The lead compensator stabilizes the loop by pushing the LC filter's complex poles into the left half-plane (LHP). Together with the other two stages of the loop filter (Fig. 1a), it provides the gain needed to suppress LC filter nonlinearity. Fig. 1b plots the noise transfer functions (NTFs) of the distortion due to the LC filter and due to the output stage. As shown, LC filter distortion is suppressed by 49 dB in the audio band, while output stage distortion is suppressed by >82 dB. The proposed loop architecture is also robust to f_{LC} variation. As shown in Fig. 1c, its closed-loop poles remain well within the LHP even in the presence of $\pm 30\%$ variations in f_{LC} . Fig. 2 shows the loop gain around the output stage. Since its high-frequency response is dominated by the RC LPF, f_{UG} is little affected by f_{LC} variations and remains below f_{PWM}/π . The 41° worst-case phase margin is not an issue since the resulting signal transfer function (STF) peaking is well outside the audio band (Fig. 1b).

Circuit Implementation

The loop filter employs various techniques to guarantee high linearity and robustness while reducing the area. All its three stages employ active-RC integrators (Fig. 3). The RC LPF is realized by the T-network consisting of R_{FILT} , C_{FILT} , and R_{FB3} .

Setting $R_{FILT} = 2R_{FB3}$ ensures that the voltage across C_{FILT} never exceeds 5.5V, allowing it to be implemented with the same high-density MIM capacitors as C_{INT1} , C_{INT2} , and C_{INT3} . As is typically done in continuous-time $\Delta\Sigma$ modulators, the latter are implemented as switchable banks to enable a one-time trim to compensate for RC spread and center the tolerable f_{LC} range around 85 kHz. In contrast to [3], the first two stages of the loop filter employ a feedforward architecture to reduce the signal swing of A1, with R_{RES} realizing optimal pole placement. This reduces the size of C_{INT1} , simultaneously saving area and increasing the 1st integrator's gain, which further attenuates the noise and distortion caused by subsequent stages. V_{IN} is also directly fed to the input of A3 to reduce the swing of A2. When the CDA is overloaded, the loop filter's integrators will be driven into saturation. To ensure a smooth recovery without audible glitches, an overload detection circuit in the modulator shorts the integration capacitors when overload occurs.

Measurement Results

The proposed CDA is implemented in a 180 nm BCD process and occupies 5mm^2 (Fig. 4). It employs a fully differential multi-level output stage [3] operating at 14.4V. Fig. 5 shows the output spectra for a 1 kHz input at an output power of 1W. A THD of -121.5 dB and -119.0 dB is achieved for 8Ω and 4Ω loads, respectively. Fig. 6a and Fig. 6b show the measured THD+N for a 4Ω load using 3 different inductors for 1 kHz and 6 kHz inputs, respectively. Both the input and output of the LC filter are measured to quantify the suppression of its nonlinearity. The residual THD+N variation at 1 kHz is only 1.1 dB at full scale, and 3 dB at 6 kHz, confirming that it is no longer limited by LC filter nonlinearity. A 49-dB THD+N improvement is observed even with the most non-linear inductor. Fig. 6c shows the THD+N when various inductors are placed in series with R_{LOAD} to mimic a speaker coil. Fig. 6d shows the THD+N of 6 samples as f_{LC} is varied from 62 kHz to 106 kHz. It varies by only 1.7 dB (8Ω) and 2.9 dB (4Ω), demonstrating the design's robustness to both LC and process spread. Fig. 7 shows the CDA's response (after the LC filter) after it is driven into clipping, demonstrating a smooth recovery. The CDA draws an idle power of 120mW and achieves a peak efficiency of 91%/87% for 8Ω and 4Ω loads.

Table I compares this CDA with the state of the art. Compared to [1-3], it achieves the best THD (12.6 dB better than [2]) as well as the best THD+N for a 4Ω load, without the need for highly linear LC filters. Compared to [4], it achieves 39 dB more suppression of LC filter nonlinearity; and thanks to the higher loop gain around the output stage, 18 dB less THD+N than [5]. Last, but not least, this is the only design to demonstrate robustness to large ($\pm 30\%$) f_{LC} variations.

References

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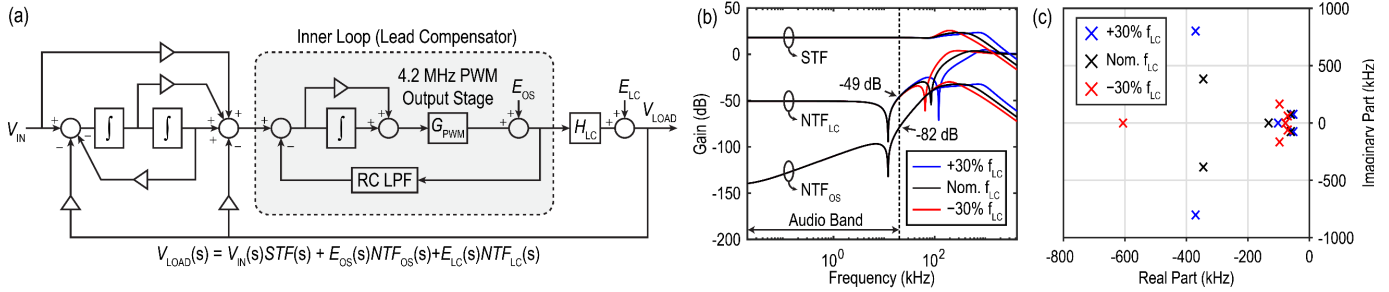


Fig. 1. (a) System-level block diagram, (b) NTFs for respective errors introduced in the output stage (E_{OS}) and LC filter (E_{LC}), STF, and (c) pole locations of the closed-loop system confirming stability under $\pm 30\% f_{LC}$ variations.

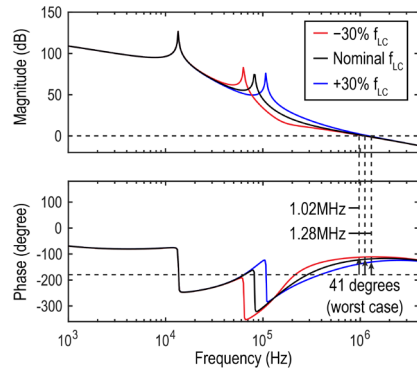


Fig. 2. Loop gain around the output stage.

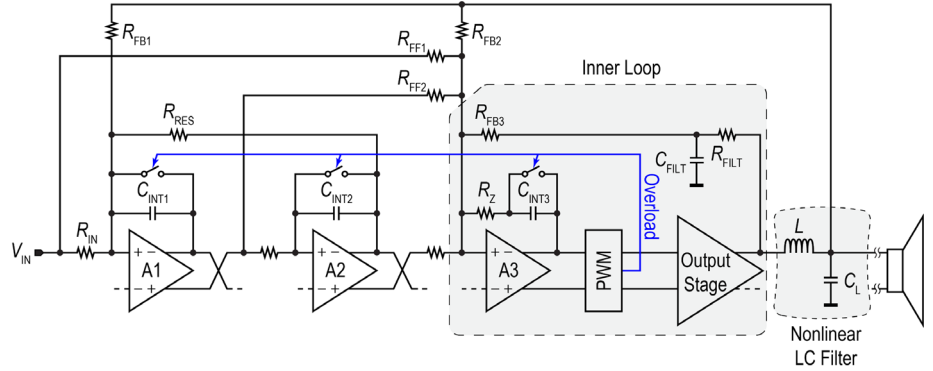


Fig. 3. Implementation of the CDA.

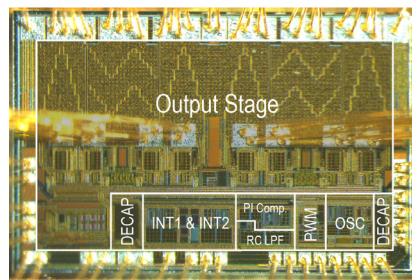


Fig. 4. Die photo.

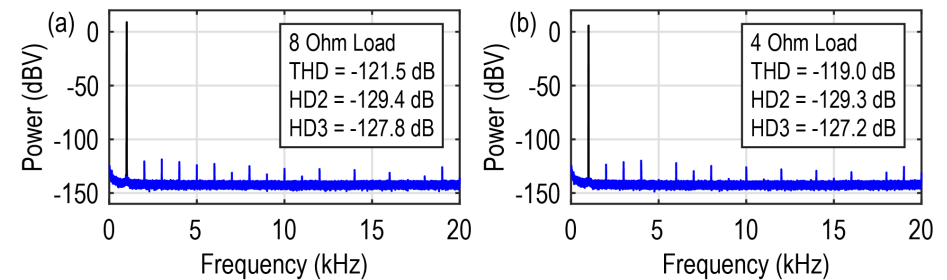


Fig. 5. FFT measured at the LC filter output for (a) 8- Ω load, and (b) 4- Ω load.

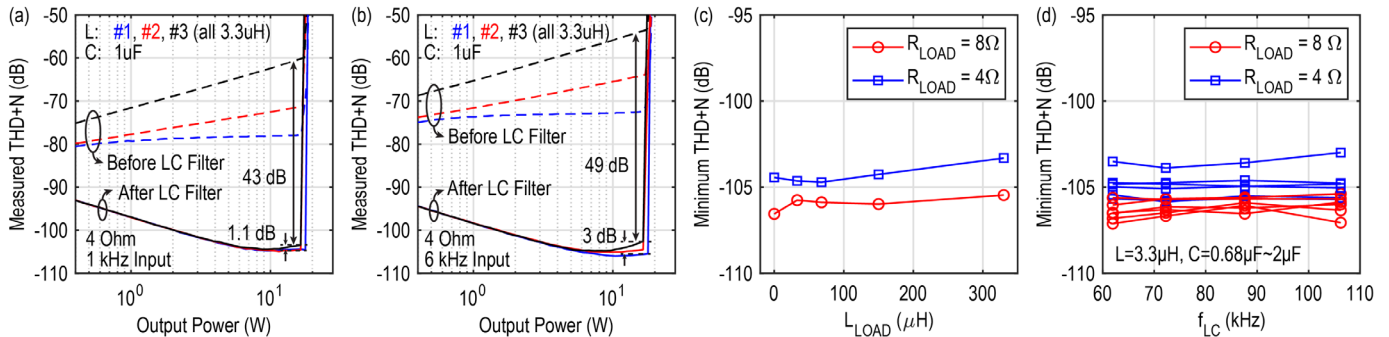


Fig. 6. THD+N vs. output power for (a) 1 kHz input, and (b) 6 kHz input, (c) THD+N for different load inductance, and (d) THD+N vs. f_{LC} for 6 samples.

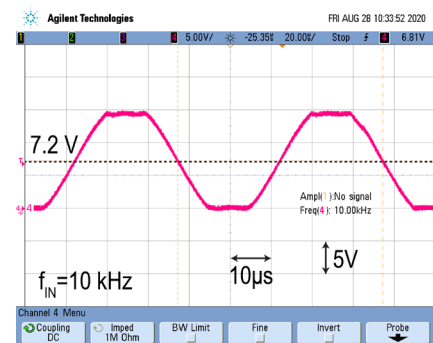


Fig. 7. Measured clipping behavior at the output of the LC filter.

Table I. Performance summary and comparison.

	This Work	[5]	[4]	[3]	[2]	[1]		
Supply Voltage (V)	14.4	14.4/25	25	14.4	14.4	14.4		
R_L (Ω)	8	4	4	8	4	4		
Efficiency	91%	87%	>90%	89%	91%	87%	91%	86%
THD (dB)	-121.5	-119.0	-	-	-	-	-108.9	-
THD+N at 1kHz (dB)	-107.1	-105.9	-87.9	-67.9	-107.8	-102.6	-102.2	-76.5
THD+N at 1kHz (%)	0.0004	0.0005	0.004	0.04	0.0004	0.0007	0.0008	~0.015
LC error suppression (dB)	49	50*	10*	0	0	0	0	0
f_{LC} tolerance	62 kHz ~ 106 kHz	-	-	N/A	N/A	N/A	N/A	N/A
SNR (dB-A)	110.0	-	110	109.7	109	-	-	-
DR (dB-A)	110.8	115	108	111.2	-	-	-	-

*Estimated from loop gain