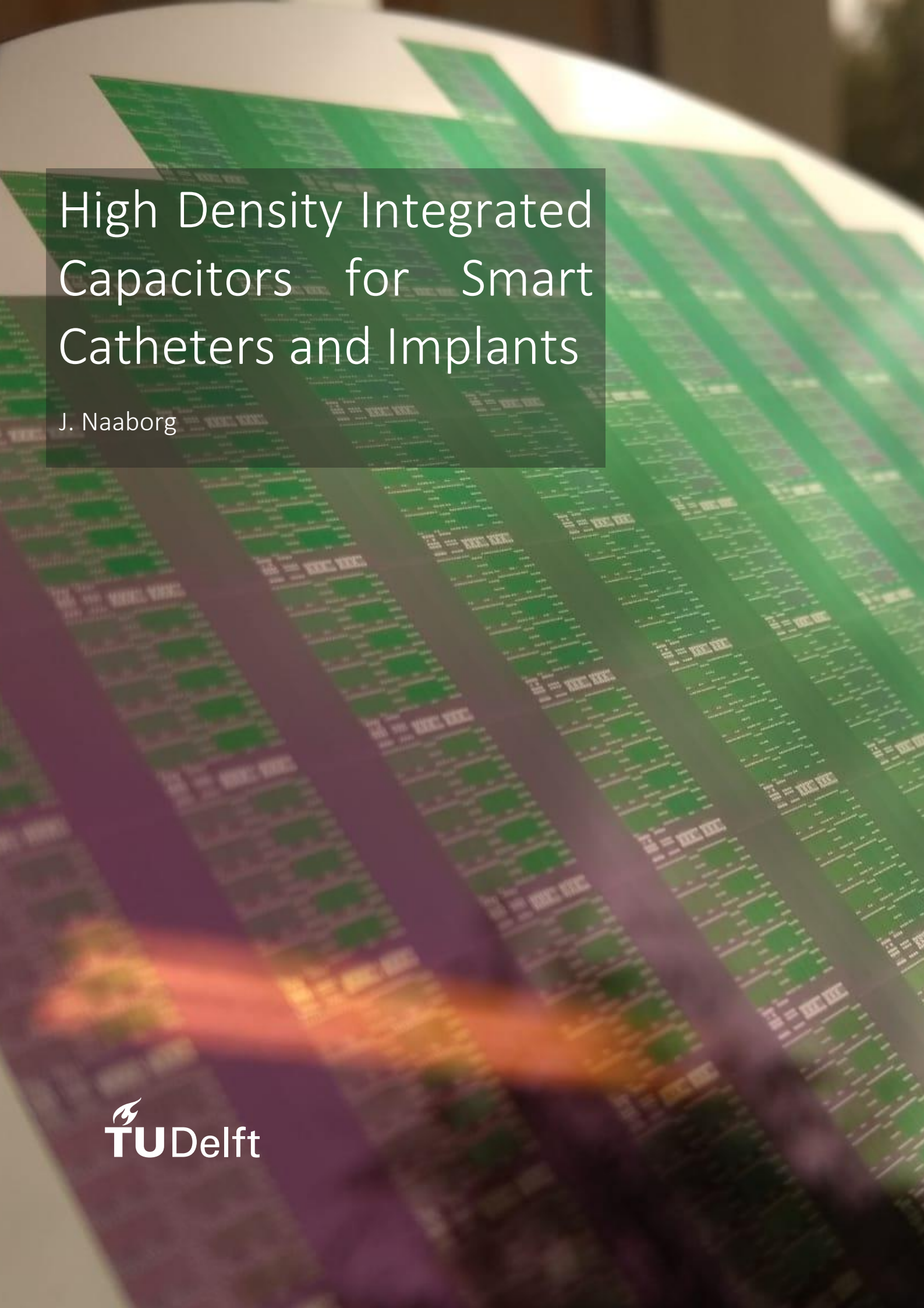

High Density Integrated Capacitors for Smart Catheters and Implants

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TU Delft

High Density Integrated Capacitors for Smart Catheters and Implants

By

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Abstract

The Flex-to-Rigid (F2R) technology platform is an interconnect platform to integrate heterogeneous electronic systems and devices onto a partially flexible chip for minimally invasive medical instruments. This technology platform allows for the integration of micro electro-mechanical systems (MEMS) and integrated circuits (IC) on a chip in a planar plane, which can later be folded into any arbitrary shape. Downscaling of the technology and the increasing number of integrated components in the F2R platform have a high impact on the power distribution and consequently on the signal integrity. It is widely accepted that one of the most powerful strategies to encounter signal integrity problems is to use decoupling capacitors. However, there is an inherent trade-off between the capacitance and size of a capacitor.

This thesis is focused on the development on high density capacitors for the integration in the F2R technology platform. One of the objectives was to increase the capacitance density. Because there is limited space available on the F2R chip, additional area to increase the capacitance is found in the depth of the silicon. By etching multiple trenches into the silicon, a capacitance density increase by a factor of 10 is obtained. To even further increase the capacitance, the use of a silicon dioxide – silicon nitride – silicon dioxide multilayer (ONO) dielectric is reviewed. Moreover, a first step has been made in the fabrication of high breakdown voltage and low breakdown voltage parts in this dielectric layer.

A second objective was to deliver the capacitors as a ‘’building block’’ that can be implemented in the F2R process flow. Therefore, the process needs to be compatible with the standard IC and MEMS technologies that are available in the Philips Innovation Service cleanroom. The steps of the fabrication process are verified and where needed optimized, and a dedicated mask set is designed for the fabrication of the capacitors. With this mask set, the so called trench capacitors have been made. These test devices are characterized in terms of breakdown voltage and capacitance. It is found that the capacitance density can be increased by an order of magnitude with the introduction of trenches to the test devices. In addition, the advantage of a multilayer dielectric compared to a single layer dielectric is shown.

Preface

This thesis concludes my master Biomedical Engineering degree. During this project, I worked at Philips research on the integration of high density capacitors in the Flex-to-Rigid (F2R) technology platform. The idea of doing my thesis on the subject of smart catheters and implantable devices, although it was not my field, came after attending an inspiring lecture by Ronald Dekker. Discovering the world of microfabrication was however a really nice experience, stimulated by the helpful people in the Philips Innovation Service cleanroom.

First of all, I would like to thank my supervisor Ronald Dekker for his assistance during the thesis and the opportunity of doing this project. Besides that I have learned a lot, I also enjoyed working at Philips. Secondly, I would like to thank Eugene Timmering for his guidance in the cleanroom and refreshing coffee. Furthermore, my thanks goes to Jian Li, Carlo Eugeni, Marcus Louwerse, Vincent Henneken and Johan Klootwijk for the enlightening discussion we had. To conclude I would like to thank my parents, the Sunday dinners together with grandpa were and will always be something to look forward to.

J. Naaborg

Eindhoven, August 22, 2019

Nomenclature

AC	Alternating Current
BOE	Buffered Oxide Etch
CAD	Coronary Atrial Disease
CCP	Capacitively Coupled Plasma
CMUT	Capacitive Micro-machined Ultrasound Transducers
CVD	Chemical Vapor Deposition
DC	Direct Current
DRIE	Deep Reactive Ion Etching
EPD	End Point Detection
F2R	Flex-to-Rigid
FEM	Focus Exposure Matrix
HARMS	High-Aspect Ratio Microstructures
IC	integrated circuit
ICP	Inductively Coupled Plasma
IVUS	Intravascular Ultrasound
LPCVD	Low Pressure Chemical Vapor Deposition
LTO	Low Temperature Oxidation
MCM	Multi-Chip Modules
MEMS	micro electro-mechanical systems
MFC	Mass Flow Controllers
ONO	Oxide-Nitride-Oxide
PCI	Percutaneous Coronary Intervention
PEB	Post Exposure Bake
PECVD	Plasma Enhanced Chemical Vapor Deposition
PInS	Philips Innovation Service
Poly-Si	Polycrystalline Silicon
PSG	Phosphosilicate Glass
PSV	Philips Sport Vereniging
PVD	Physical Vapor Deposition
RF	Radiofrequency
RIE	Reactive Ion Etching
SEM	Scanning Electron Microscope
TEOS	tetraethylorthosilicate

Contents

1. Introduction

1.1 Coronary Atrial Disease (CAD)

For decades, Coronary Atrial Disease (CAD) has been the leading cause of death worldwide with 9.4 million deaths per year and the prediction is that this number will steadily increase in the coming years[1], [2]. CAD is characterized by a partially or totally blockage of the blood flow to the heart due to a narrowing of the coronary arteries. The cause of this narrowing is the accumulation of atheromatous plaques on the arterial wall, called a stenosis. The reduction of blood flow leads to a lack of oxygen for the heart muscles, resulting in chest pain, shortness of breath, a heart attack or a thrombosis when the plaque breaks loose from the vessel wall.

The effects of CAD can be minimized by a healthy lifestyle or with appropriate medication [3]. However, in the case of a severe stenosis, an operation might be necessarily. An often-used method for the diagnosis and treatment of a stenosis is percutaneous coronary intervention (PCI) [4]. A visualization of PCI is shown in Fig 1.1. PCI is a minimally invasive treatment method where a guidewire is inserted in the cardiovascular system and navigated to the location of the intervention. Next, a balloon catheter is slid over the guidewire and inflated at the location of the stenosis. By compressing the plaque against the arterial wall, the vessel is opened and the blood flow is restored. A stent can be placed to keep the vessel dilated.

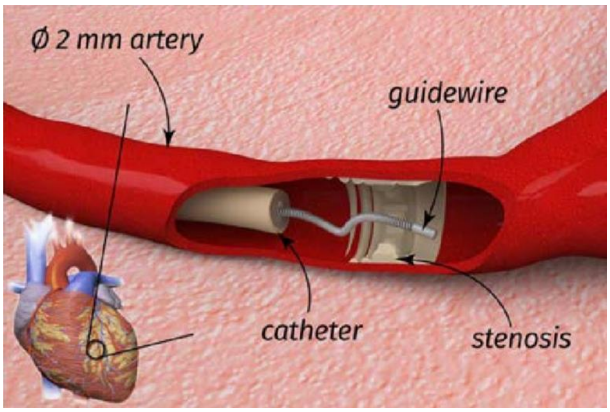


Figure 1.1. Visualization of percutaneous coronary intervention to treat CAD. A guidewire is inserted and navigated to the location of the stenosis, followed by a treatment catheter that slides over the guidewire [5].

A critical step during PCI is the determination of the severity and location of the stenosis. The current standard method for gathering this information is X-ray angiography [4]. This method is similar to PCI. A guidewire is inserted in the artery, followed by a catheter that slides over the guidewire. With the help of fluoroscopy and a radio-opaque contrast agent, an image of the artery is created. The drawbacks of this imaging technique are; 1) the created 2D image cannot provide enough detail, as the stenosis is a 3D problem; 2) the exposure of radiation to the patient and medical staff and 3) the lack of information regarding the nature of the stenosis. In the past, the blocking percentage of a stenosis used to be decisive for acute clinical events, while recent studies have revealed that compositions and structures are more determinative for operation [6].

A complementary methodology to image the coronary arteries is to use intravascular ultrasound (IVUS). With highly minimized and integrated ultrasound transducers (piezoelectric or CMUT), it applies ultrasound techniques inside the blood vessels. By mapping out the cross section of the coronary arteries, the IVUS technology allows 3D visualizations of the stenosis. These 3D visualizations help to determine the amount of

stenosis that is built up inside the coronary artery, which gives more insight and perspective for the diagnosis. However, the IVUS catheters used today are all manufactured with outdated and obsolete technologies, which limit their image resolutions. The lack of a good image quality forms a barrier for a high accuracy diagnosis of the stenosis and precise information regarding the nature of the plaque.

New microfabrication technologies have enabled improvement of the IVUS image quality. With the introduction of the Flex-to-Rigid (F2R) technology into the IVUS catheter manufacture process, it has become possible to integrate more ultrasound transducer elements onto the tip of an IVUS catheter. Additionally, recent studies have proposed IVUS technology integration into a guidewire (Ø360 µm) [4], [5]. This eliminates the need for a large diameter catheter (Ø1.2 mm). Consequently, the clinical intervention is less invasive and the investigation of smaller arteries is possible. Moreover, F2R also helps to digitize the electrical system in the catheter tip, which significantly improves the signal quality and image frame rate.

1.2 Flex-to-Rigid (F2R)

The Flex-to-Rigid (F2R) technology is an interconnect platform to integrate heterogeneous electronic systems and devices onto a partially flexible chip for minimally invasive medical instruments. This technology platform allows for the integration of the micro electro-mechanical systems (MEMS) and integrated circuits (IC) on a chip in a planar environment, which can later be folded into any arbitrary shape. The folding characteristic of the chip is established by the formation of rigid silicon islands that are connected by flexible interconnects. These separate silicon islands are isolated by the ‘’buried trenches’’. ‘’Buried trenches’’ in the F2R platform are developed to precisely define the dimensions of separated silicon islands. For the fabrication of buried trenches, a silicon dioxide sub-micro mesh mask with small holes or squares is first created. A deep reactive ion etch (DRIE) step (Appendix B.2) with negative etch slope then etches the Si substrate from underneath the masks. During the DRIE step, the etched trenches merge into bigger trenches underneath the oxide mesh at a certain point due to the DRIE negative etch slope. A thick silicon dioxide is applied to close the holes in the oxide mesh mask and flatten the substrate surface for further process. These closed merged bigger trenches, the “buried trenches”, define the silicon island dimensions with very high accuracy. A scanning electron microscope (SEM) image of a buried trench is shown in Fig 1.2. Within the flexible interconnects, metal interconnects are embedded to function as an electrical connection between the electrical systems on the different silicon islands. By placing the metal layer in the neutral stress plane of the polymer stacks, very high flexibility is obtained in the interconnects. A simplified version of the F2R process flow is explained in the following section.

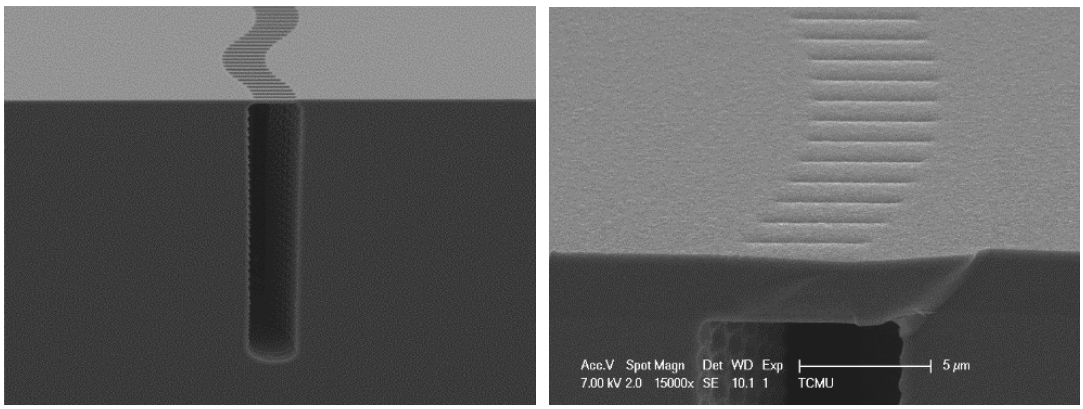
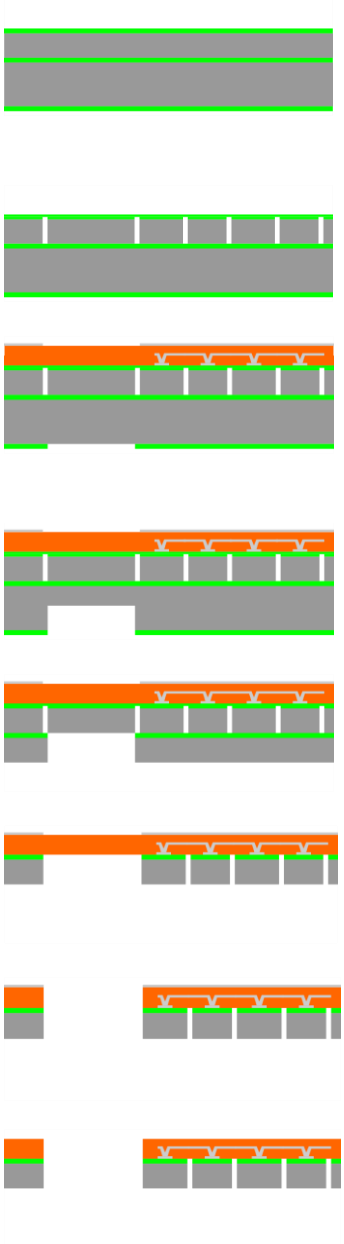


Figure 1.2. SEM images of a buried trench. (a) A buried trench is etched by DRIE step with negative etch slope. (b) Mesh mask of a buried trench that is closed by a 700 nm thick layer of silicon dioxide [7].

1.2.1 F2R process flow



The process starts with a silicon-on-insulator (SOI) wafer. The SOI wafer consists of a device layer of 40 µm, a buried silicon oxide layer of 1 µm and a substrate layer of 380 µm. The device layer is highly doped and both sides of the wafer are oxidized.

The device layer is separated by buried trenches to create the isolated rigid silicon islands. A 700 nm thick layer low stress silicon dioxide closes the silicon dioxide sub-micro mesh mask.

The flexible interconnects, with the metal layer in the stress neutral plane, are fabricated and a metal masking layer is deposited on top of the polyimide. Additionally, the oxide on the backside of the wafer is patterned

A 2-step etch is applied for backside Si substrate etching. First, the silicon substrate is etched halfway through from the backside.

Next, the backside oxide mask is removed and an overall silicon etch continues until etching stops on the buried oxide layer of the SOI wafer. The exposed buried oxide layer is then removed.

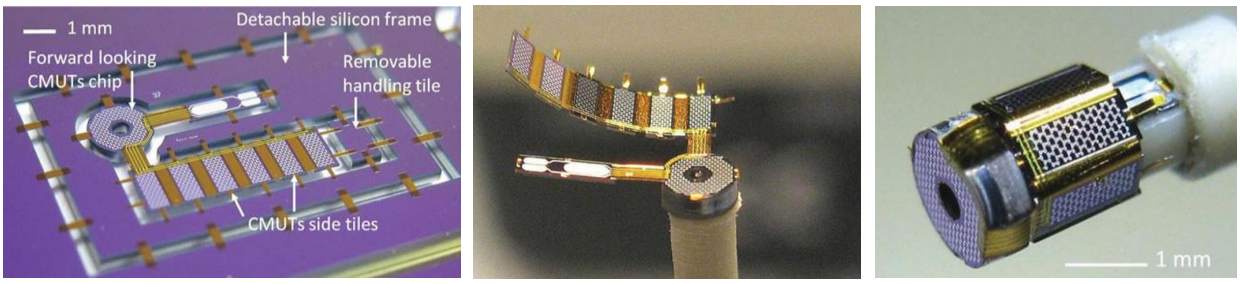
After removing the remaining exposed silicon, the oxide layers are removed. At this stage, the silicon islands are separated from each other and solely connected by the polyimide interconnects.

From the front side, the polyimide connections between the wafer and the chip are removed. Some small connections are preserved for handling of the wafer and chip.

After removal of the metal masking layer, the chip is finished.

Figure 1.3. Simplified process flow of the F2R technology.

The folding characteristics of F2R process makes it ideal for the fabrication of minimally invasive medical instruments such as catheters and guidewires [8]. Fig 1.4 shows an F2R device in a wafer after fabrication (a), the same F2R device removed from the wafer (b) and the F2R device folded around the tip of a catheter (c). In combination with MEMS ultrasound transducer technology, F2R can be a powerful tool for accurate imaging of the arteries.



a) *b)* *c)*

Figure 1.4. Folding of a F2R device, a) the device attached to the wafer, b) the device removed from the wafer and c) the device folded around the tip of a catheter [8].

1.2.2 Capacitive Micro-machined Ultrasound Transducers (CMUTs)

The F2R technology enables the integration of Capacitive Micro-machined Ultrasound Transducers (CMUTs) on the tip of an IVUS catheter. In the past, piezoelectric ultrasound transducers used to be the standard in IVUS. However, CMUTs have significant benefits compared to piezoelectric transducers. Compared to piezoelectric transducers, CMUTs offer: 1) a larger bandwidth and the possibility for scaling to higher frequencies, 2) reduced fabrication and assembly costs, hence more suitable for massive production and 3) easier integration with other electronic systems [9]. All these characteristics make CMUTs more attractive to IVUS technology.

CMUTs are transducer elements that can act both as a transmitter and as a receiver for ultrasound waves. The principle of a CMUT is based on a capacitor cell. A vacuum cavity is sandwiched by a membrane with a top electrode and a bottom electrode, which is often integrated in the substrate. A direct current (DC) voltage is applied over the top and bottom electrode. The DC-bias voltage causes the membrane to collapse towards the bottom electrode. By applying an alternating voltage, the CMUT generates vibrations in the membrane that produces ultrasound waves. Visa versa, the membrane is also able to generate an output current signal when it receives an ultrasound wave. A schematic cross section of a CMUT cell is given in Fig 1.5.

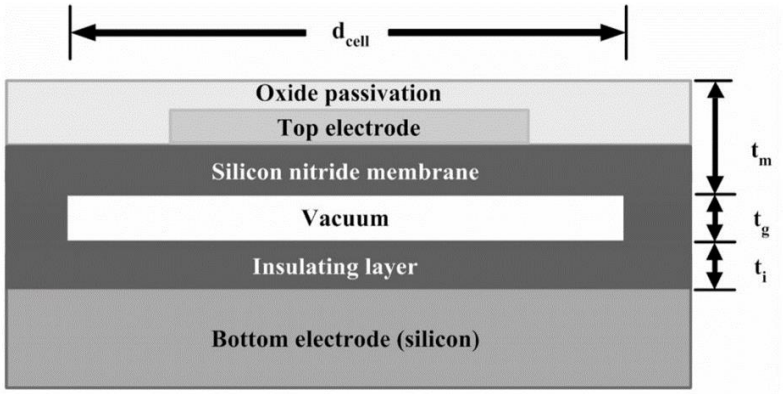


Figure 1.5. Schematic cross section of a CMUT Cell [9].

The image quality, or resolution, generated with CMUTs is characterized by two parameters: the axial resolution and the lateral resolution. The resolutions are given by equation 1.1 and 1.2,

$$Axial\ resolution = \frac{0.5c}{Bandwidth} \qquad (1.1)$$

$$Lateral\ resolution = \frac{Depth\ \lambda}{Array\ size} \qquad (1.2)$$

where c is the speed of sound in the tissue (1484 m/s) and λ is the ultrasound wavelength (37µm) [10]. To improve the image resolution, an increase in the transducer's operating frequency and the transducer array size is needed. A larger array size is established by increasing the number of elements. This requires a higher current supply. A consequence of the increased current supply and frequency is the generation of noise on the power-supply grid due to switching currents, called Delta-I noise. This problem can be mitigated by locating the power source as close as possible to the circuit. For catheters, this is practically impossible. Another very effective method to reduce the noise is to use decoupling capacitors, which act as a temporary power source [11]–[13].

1.2.3 Decoupling capacitors

The integration of the sensors and data transfer elements in the F2R platform has a high impact on the power distribution and consequently on the signal integrity. One of the most important issues in today's deep submicron designs is signal integrity [14]. Signal integrity can be compromised by various source. One of the main causes for signal degradation is Delta-I noise, caused by a sudden change in the amount of current that is drawn by the components in the circuit. This change in current can cause a momentary drop or surge in the voltage over the power distribution bus [15]. The voltage variation is given by equation 1.3,

$$\Delta V = L\frac{\delta I}{\delta t} \qquad (1.3)$$

where ΔV is variation in the power supply level, L is the effective wire inductance of the power busses, δI is the current change during transition and δt is the rise or fall time of the transition [14]–[16]. It is widely accepted that one of the most powerful strategies to encounter the delta-I noise problem is to use decoupling capacitors[13].

A capacitor is a passive electric component that can store electrical energy in the form of charge. The most commonly used capacitor is the parallel-plate capacitor, which consist of two conductors separated by a non-conducting medium. Applying a voltage difference over the capacitor causes one conductor to collect a negative charge and the other conductor to collect a positive charge. When the power source is removed and the circuit is opened, the charge is stored in the capacitor. By closing the circuit, the charge will generate a current flow through the circuit, which can be used to deliver power to a device.

A decoupling capacitor act as charge reservoir for switching circuits and reduces the effect of Delta-I noise. Most of today's multichip modules (MCM's) use surface-mounted stand-alone decoupling capacitors. However, these surface-mounted devices have their drawbacks. In-substrate integrated decoupling capacitors encounter most of the drawbacks by offering: 1) better electrical performance, 2) increased packaging efficiency, 3) better capacitance efficiency and 4) elimination of separate packaging and assembly to the board [13]. In in-substrate integrated capacitors, the silicon substrate is doped to function as the bottom electrode. A dielectric and top electrode layer are deposited on top to form the capacitor.

Trench capacitors

Although the in-substrate integrated capacitors are preferred for integration onto the F2R platform with other electrical systems, there is a very realistic problem: there is only a limited amount of surface area available in the catheter due to its small size. Therefore, a method to increase the capacitor functional area is found by expending the capacitors into the third dimension i.e. in the depth of the silicon islands. The idea of etching into the silicon in order to enlarge the functional area is not new and was first patented by Texas Instruments in 1976 [17]. Nowadays, these structures are frequently seen in the field of semiconductors and carry the name ''trench capacitors''.

1.3 Aim of the thesis

In summary, CMUTs in combination with the F2R technology platform enable the downscaling of IVUS catheters while maintaining, or even improving, the image quality. Furthermore, improving the image resolution, generated by CMUT transducers, requires an increase in ultrasound frequency. Equation 1.3 shows that this results in an increase in delta-I noise. With these trends in mind, the integration of decoupling capacitors in the F2R technology is an interesting option.

The first objective of this thesis is the theoretical investigation for trench capacitors. A mathematical relation is provided that illustrates the capacitance's dependency on different geometrical parameters and the influence of different dielectric materials is investigated. Furthermore, a design solution to meet the requirements regarding the breakdown voltage is proposed. The theoretical ideas are tested and verified in the Philips Innovation Services (PInS) cleanroom.

The second objective of the work is to develop trench capacitors that can be implemented, as a building block, in the existing F2R process flow. For the fabrication of the trench capacitors, a new dedicated mask set with and accompanying flowchart is designed. Furthermore, the process flow for the trench capacitors and the process steps are verified and, where needed, optimized. The fabrication processes and results are presented and further work about the integration of the decoupling capacitors in the F2R flow is discussed.

1.4 Organization of the Thesis

In Chapter 2, a mathematical relation between the trench geometry and the capacitance density is presented and a comparison is made between a single layer dielectric and a multilayer dielectric. Chapter 3 described the process flow and mask design. The process optimization of processes that needed more attention is shown in Chapter 4. In Chapter 5 the electrical characterization is presented. Finally, the Thesis is concluded in Chapter 6.

2. Trench Capacitors for IVUS

2.1 Introduction

To improve the image quality of the next generation IVUS catheters, additional decoupling capacitors are needed to meet the electrical demands of the CMUT elements and digital systems. Currently, surface-mounted stand-alone decoupling capacitors are flip chip bonded on the IVUS chip. However, in terms of performance and functionality, in-substrate integrated decoupling capacitors are preferred and these decoupling capacitors should be integrated as close to the CMUTs and digital systems as possible. In the IVUS F2R platform, six silicon islands with dimensions of 2600 um by 500 µm are designed as carrier substrates for ASICs (Fig. 2.1). Interconnects and contact pads are fabricated on the island surfaces and ASICs are flip-chipped directly onto these islands. Therefore, the silicon islands seem to be the ideal location to integrate the in-substrate decoupling capacitors. To effectively increase the in-substrate capacitance, trench capacitors are applied instead of plate capacitors. Trench capacitors increase the functional surface area by drilling trenches into the third dimension, i.e. the depth of the 40 µm thick silicon island. With stacked dielectric layers to improve relative dielectric permittivity, the capacitance can even be further enhanced.

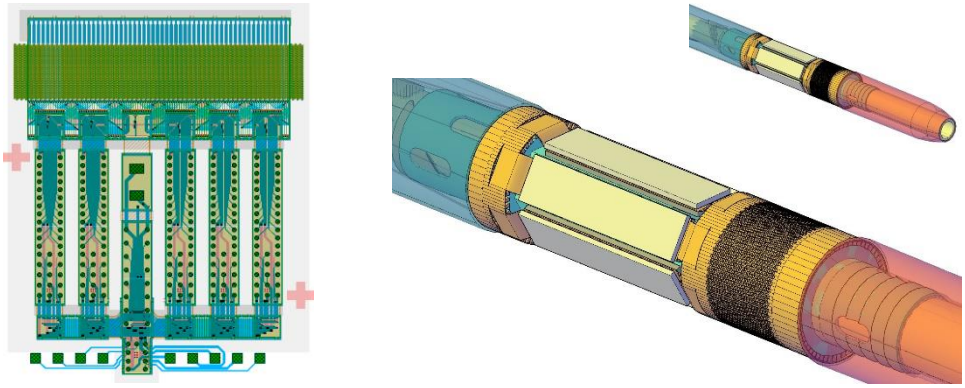


Figure 2.1. Illustration of the IVUS catheter showing the six silicon islands [7].

This chapter describes the theoretical approach of the decoupling trench capacitors integration in the F2R platform in terms of electrical characteristics. First, the requirements for of breakdown voltage and capacitance are calculated. Next, the theoretical solution to meet the requirements in terms of breakdown is explained. Finally, two approaches to increase the capacitance are reviewed. A mathematical relation between the trench geometrical parameters and the decoupling capacitance in derived, followed by a comparison between a multilayer dielectric and a single layer dielectric.

2.2 Requirements

The IVUS electrical system requires two different decoupling capacitors for two different purposes. First, a decoupling capacitor is needed to provide the peak currents drawn by the electrical system that is connected to the ASICs. This system operates at 3.3 V. Secondly, a decoupling capacitor is needed to prevent crosstalk to arise between the CMUT elements. This decoupling capacitor serve another purpose and the main requirement is the ability to withstand a voltage in the range of 35 V. Because of the likelihood of thin dielectric layers to deviate from the known electrical properties, an above average safety margin of three is taken into account in the first design of the trench capacitors. Therefore, the required breakdown voltages are

determined at 10 V for the low voltage capacitors and 100 V for the high voltage capacitors. In the remainder of this work, the corresponding decoupling capacitors are referred to as low voltage capacitors and high voltage capacitors respectively. Since the requirements for the high voltage capacitors are not very stringent, this chapter will address the estimation of the majority of the required value for the low voltage capacitors.

The exact operation specifications for the IVUS electrical system that is connected to the ASICs are hard to determine. However, a very realistic estimation of the values can be made. The following calculations are based on the estimated values, which are determined in consultation with the electrical system designers of the IVUS catheter at Philips.

For an IVUS catheter, operating at an ultrasound frequency of 30 MHz, which is sampled at 2.5 times the ultrasound frequency, the typical ASIC clock frequency (*f*) will be in the range of 100 MHz, and peak currents are expected up to 25 mA. To calculate the capacitance from the above-mentioned parameters by equation 2.1, first the charge drawn by the electrical system (*dQ*) and potential difference (*dV*) are calculated.

$$C = \frac{dQ}{dV}\ [F] \tag{2.1}$$

$$dQ = I(t)\ \cdot dt\ [C] \tag{2.2}$$

The change in the amount of charge follows from the peak current (*I(t)*) and the pulse duration (*dt*). Maximum peak currents are estimated at 25 mA. The pulse duration is defined as the time the peak current is drawn by the system and is calculated from the duty cycle (*D*) and the total period (*T*), which is defined by *1/f*. The pulse duration follows from the duty cycle of the period. The duty cycle in the IVUS electrical system is estimated at 20%.

$$dt = D \cdot T = 0.20 \cdot 1 \cdot 10^{-8} = \ 2 \cdot 10^{-9}\ [s] \tag{2.3}$$

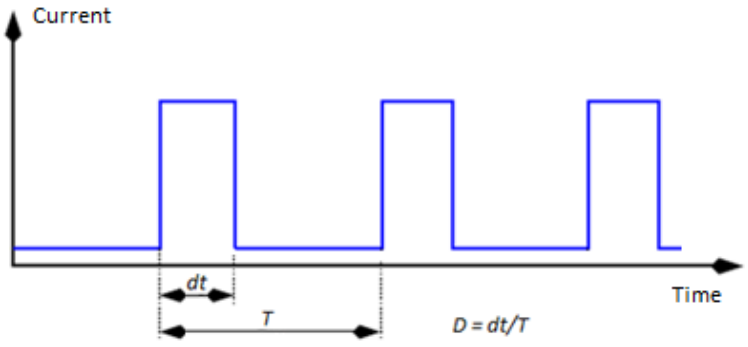


Figure 2.2. Illustration of a pulse duration (dt), period (T) and duty cycle (D) [18].

The change in charge is calculated by implementing the current and the period in equation 2.4.

$$dQ = I(t) \cdot dt = 25 \cdot 10^{-3} \cdot 2 \cdot 10^{-9} = 50 \cdot 10^{-12}\ [C] \tag{2.4}$$

The potential difference (*dV*) can be interpret as the acceptable voltage fluctuation over the electrical system. Generally, the acceptable potential difference is set as a fraction of the voltage and follows from $dV = n \cdot V$ with *n* typically in the range of 0.05 [11]. A realistic acceptable fluctuation in the IVUS system is 0.1 V.

From the potential difference and the change in the amount of charge the capacitance is calculated.

$$C = \frac{50 \cdot 10^{-11}}{0.1} = 500 \cdot 10^{-12}\ [F] \qquad (2.5)$$

The required target capacitance for optimal function of the IVUS electrical system is 500 pF.

2.3 Breakdown voltage

As explained in the section 1.2.3, capacitors are passive electric components that can store electrical energy in the form of charge. One of the main properties that characterize a capacitor is the breakdown voltage, or the dielectric breakdown. Generally, the design or selection of a capacitor start with the breakdown voltage. The dielectric breakdown of an insulator is defined as the moment where the dielectric starts to conduct, which is an irreversible phenomena. Therefore, it is crucial that the capacitor is able to meet the breakdown requirements. The dielectric breakdown is strongly related to the exact processing details during the manufacturing of these layers [19]. However, in first approximation the breakdown of a dielectric layer can be characterized by the maximum electric field at breakdown (E_{bd}) that can be applied to the dielectric before breakdown occurs. From the thickness of the dielectric layer (t_{di}) and the maximum electric field the maximum voltage (v_{bd}) that can be applied over the dielectric can be estimated from:

$$V_{bd} = E_{bd} \cdot t_{di}\ [V] \qquad (2.6)$$

The minimum thickness of the dielectric layer for a given working voltage is then found by:

$$t_{di} = \frac{V_{bd}}{E_{bd}}\ [cm] \qquad (2.7)$$

Note that the equation 2.6 is merely an indication. For an accurate estimation of the breakdown voltage, the effective dielectric thickness should be used instead of the physical thickness [20]. The effective dielectric thickness compensates for extrinsic defects.

2.3.1 Fabrication of low and high voltage capacitors

For the integration of low and high voltage capacitors in the F2R platform, two separate capacitors can be fabricated with different dielectric thicknesses. A thick dielectric layer for the high voltage capacitor and a thin dielectric layer for the low voltage capacitor. However, fabrication wise it is expensive to fabricate two separate dielectric layers independently from each other on one wafer. The use of a multilayer stacked dielectric offers the potential of fabricating the low and high voltage capacitors by the deposition of a triple layer dielectric and partially remove the top dielectric layer (Fig 2.3). With this method, low voltage and high voltage parts are created in the dielectric with the use of just one extra lithography mask. The dielectric layer thicknesses can be tuned to obtain a breakdown voltage of 100 V in the high voltage part and a breakdown voltage of 10 V in the low voltage part.

A commonly used multilayer stacked dielectric is a combination of silicon dioxide, silicon nitride and silicon dioxide, which is further discussed in section 2.3.2. For the best performance in terms of capacitance, the thickness of the first silicon dioxide layer is set at 5 nm [21].

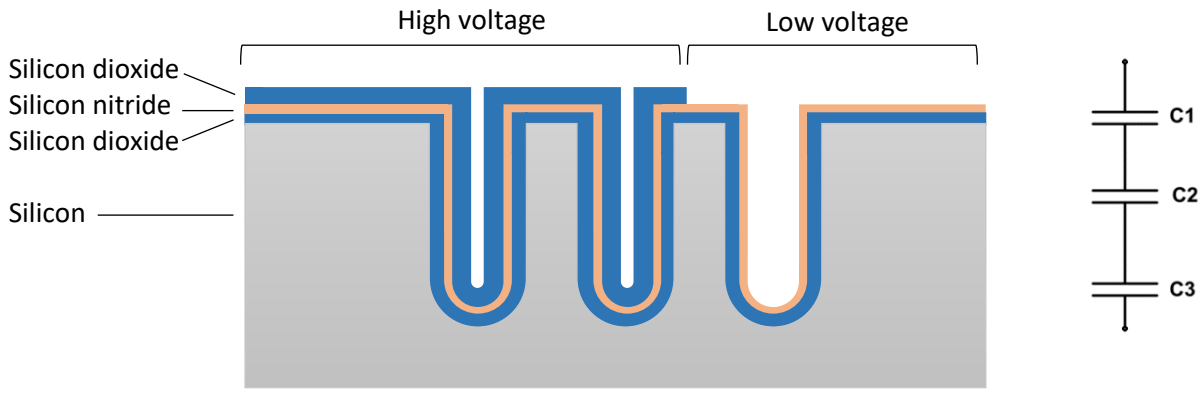


Figure 2.3. Illustration of the multilayer high and low voltage dielectric and on the right the equivalent circuit of a triple layer dielectric.

According to the capacitance equation $V = Q / C$, the voltage follows from dividing the charge by the capacitance. In a multilayer dielectric, the dielectric layers are placed in series (Fig 2.3). The charge over the three layers is equal and therefore, the voltage over the layers is inversely proportional to the capacitance (equation 2.8), where C is given by equation 2.9. The total voltage over the dielectric layer is found by the sum of the voltages over the individual layers (equation 2.9)

$$V_1 = V_{tot} \cdot \frac{C_2}{C_1 + C_2} \quad [V] \tag{2.8}$$

$$V_{tot} = V_1 + V_2 + \cdots \quad [V] \tag{2.9}$$

The design of the ONO dielectric starts with conforming the thickness of the first two layers to meet the required 10 V breakdown voltage. Next, the thickness of the second silicon dioxide layer, which is later added to withstand the 100 V breakdown voltage, is calculated.

Approach

The starting point for the design of the multilayer dielectric is the required breakdown voltage. This voltage dictates the total (acceptable) voltage in equation 2.9. From the thickness of the first silicon dioxide layer and the electric field at breakdown of silicon dioxide, the maximum acceptable voltage over this layer is calculated using equation 2.6. The voltage over the nitride then simply follows subtracting the voltage over the silicon dioxide from the total voltage (equation 2.9). The capacitance in equation 2.8 relates to the thickness of the dielectric layers:

$$C = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot A_{fun}}{t_{di}} \quad [V] \tag{2.10}$$

Where ε_0 is the electric constant in vacuum, ε_r the relative dielectric constant of the dielectric material, t the thickness of the dielectric layer and A_{fun} is the functional area of the capacitor. The relative dielectric constants for silicon dioxide and silicon nitride are 3.9 and 7.9, respectively [22]. Therefore, the thickness of the silicon

nitride is obtained by rewriting equation 2.11 in equation 2.12. Since A and ε_0 are equal for the dielectric layers, these terms are cancelled from the equation. Rewriting equation 2.11 to the thickness of the nitride results in:

$$V_{ni} = V_{tot} \cdot \frac{\frac{\varepsilon_{ox} \cdot \varepsilon_o \cdot A}{t_{ox}}}{\frac{\varepsilon_{ni} \cdot \varepsilon_o \cdot A}{t_{ni}} + \frac{\varepsilon_{ox} \cdot \varepsilon_o \cdot A}{t_{ox}}} \ [V] \qquad (2.11)$$

$$t_{ni} = \frac{\varepsilon_{ni}}{\frac{\varepsilon_{ox}}{t_{ox}} \cdot \left(\frac{V_{tot}}{V_{ni}} - 1\right)} \ [V] \qquad (2.12)$$

The thickness of the second layer silicon dioxide to fabricate the high voltage capacitors can be found by first calculating the capacitance of the low voltage dielectric part. A stacked dielectric layer is interpreted as a series capacitance and the capacitance of the combined dielectric layers is calculated according to equation 2.13.

$$\frac{1}{C_{tot}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} + \cdots \ [F] \qquad (2.13)$$

It is known that the low voltage part of the dielectric has a breakdown voltage of 10 V. Therefore, the added dielectric layer must withstand the remaining 90 V breakdown voltage. Since the voltage distribution is inversely proportional to the capacitance, the capacitance must be decreased a factor of 9 to increase the voltage by this same factor. The thickness of the silicon dioxide is then calculated by solving equation 2.10 for this capacitance.

Results and discussion

The required breakdown voltage of the low voltage dielectric is 10 V. Literature reports an electric field strength of approximately 1 V/nm for both silicon dioxide and silicon nitride [23]. However, several studies have shown the applicability of the empirical relation $E_{bd} = 20/\varepsilon_r^{1/2}$, which indicates a decrease in the dielectric breakdown for an increasing relative dielectric constant [24]. Since this relation is not proven, the calculations in this work are based on 1 V/nm electric field strength. From equation 2.6, a maximum acceptable voltage in the silicon dioxide of 5 V is calculated, the consequent acceptable voltage over the silicon nitride layer is also 5 V.

Solving equation 2.12 for the required breakdown voltages, silicon dioxide thickness and relative dielectric constants results in a required layer thickness of 10 nm for the silicon nitride. The breakdown voltage of the silicon nitride is verified with equation 2.6. Since the silicon nitride is expected to breakdown at 10 V, which is twice the applied voltage of 5 V, this layer thickness is sufficient to prevent the silicon nitride to breakdown. Moreover, it secures the maximum field in the silicon dioxide to remain below 5 V. Therefore, a 5 nm silicon dioxide – 10 nm silicon nitride configuration seems to be a proper configuration for the low voltage capacitor.

To determine the thickness of the second silicon dioxide layer, first the capacitance of the low voltage part is calculated. The capacitance of each individual layer is calculated using equation 2.10. The electric constant in vacuum is $8.85 \cdot 10^{-12}$ F/m. The total capacitance of the combined dielectric layers according to equation 2.13 is 3.5 nF/mm^2. Therefore, the second layer silicon dioxide must have a maximum capacitance of 390 pF/mm^2 to

account for 90% of the applied voltage. The thickness of the dielectric layer follows from equation 2.10 and is determined at 88.5 nm.

As mentioned in the requirements section, the breakdown voltages are overestimated and consequently, valuable capacitance is sacrificed. Therefore, it is advisable to revise these requirements when more insight is obtained regarding the behavior of the dielectric layers.

Conclusion

According to the calculations, the combination of 5 nm silicon dioxide, 10.1 nm silicon nitride and 88.5 nm silicon dioxide layer is suitable for the fabrication of low and high voltage parts in one dielectric layer. The three layers together achieve a breakdown voltage of 100 V and a capacitance density of 350 pF/mm^2. By removing the second silicon dioxide layer, the breakdown voltage is reduced to 10 V and the capacitance density increased to 3.4 nF/mm^2.

2.4 Decoupling capacitance

The second main characteristic of a capacitor is the capacitance. The capacitance of a capacitor is the ratio of the change of electrical charge (*dQ*) to the corresponding electrical potential difference (*dV*) (equation 2.14). The capacitance in expressed in Farad, or more frequently used, nanofarad or picofarad.

$$C = \frac{dQ}{dV}\ [F] \qquad (2.14)$$

The design of the decoupling trench capacitor for the IVUS catheter integration finds its origin in the same principle as the parallel-plate capacitor. The parallel-plate capacitor consists of a top and a bottom electrode, separated by a dielectric layer. The mathematical expression of the capacitance of a parallel-plate capacitor is given by equation 2.10. Since the breakdown voltage of a capacitor is determinative for the thickness of the dielectric layer, other solutions to increase the capacitance are investigated. This section describes two solutions to increase the capacitance. First, the capacitance increase by adding trenches is calculated, followed by a comparison of a single layer dielectric with a multilayer dielectric.

2.4.1 Capacitance increase through trenches

As previously mentioned, to increase the capacitance an increase in the functional area is found in the depth of the silicon islands by etching multiple trenches. This section describes the theoretical approach to calculate the capacitance increase based on a simple grid orientation. A comparison is made between flat capacitors and trench capacitors.

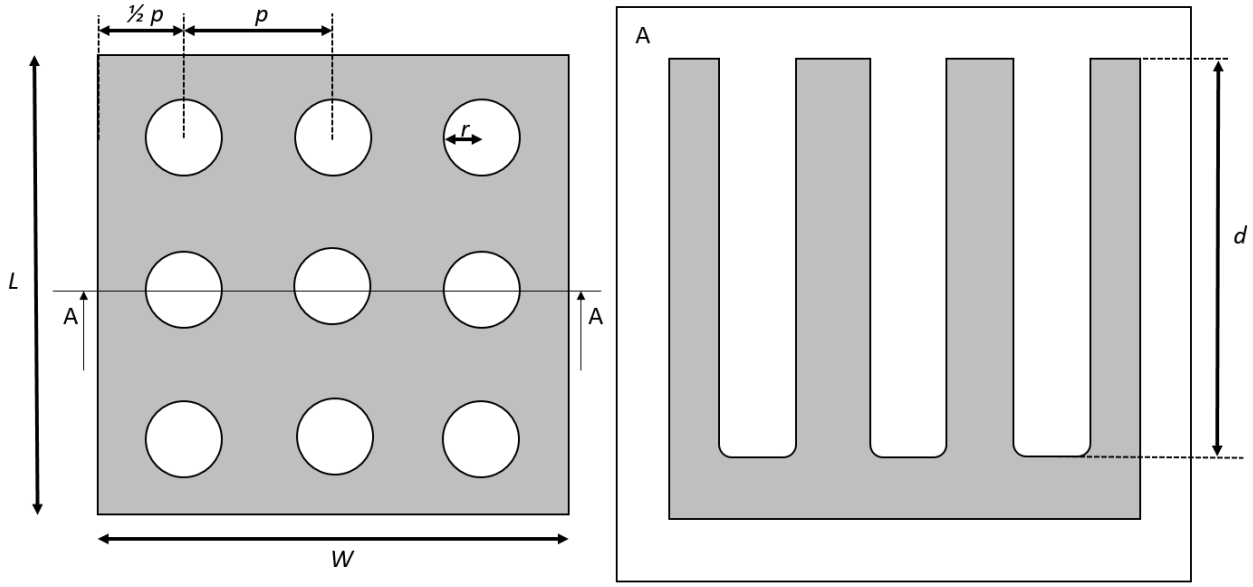


Figure 2.4. Illustration of the grid structure that is used for the theoretical approach to calculate the capacitance.

With the assumption of a straight wall profile and a flat bottom of the trench, the area of the trench walls directly adds up to the functional area of the capacitor. In the situation where the trenches are placed in a simple grid orientation (Fig 2.4) the functional area is given by equation 2.16.

$$A_{fun} = L \cdot W + \left(\left(\frac{L}{p} \cdot \frac{W}{p} \right) \cdot 2 \cdot \pi \cdot r \cdot d \right) \ [m^2] \qquad (2.15)$$

Where *L* and *W* are the length and the width of the grid resp. and *p* the pitch between the trenches. *r* is the trench radius and *d* the trench depth. Substituting equation 2.15 in equation 2.10 results in the capacitance for the trench capacitors:

$$C = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot \left(L \cdot W + \left(\left(\frac{L}{p} \cdot \frac{W}{p} \right) \cdot 2 \cdot \pi \cdot r \cdot d \right) \right)}{t_{di}} \ [F] \qquad (2.16)$$

It is Interesting to derive is the capacitance density (C_{den}) thus the capacitance per unit surface area. The capacitance density is obtained by dividing equation 2.10 and 2.16 by the surface area, A_{sur}. For the flat capacitors this results in equation 2.17 since A_{fun} and A_{sur} are equal and cancel each other out.

$$C_{den} = \frac{\varepsilon_0 \cdot \varepsilon_r}{t_{di}} \ [F/m^2] \qquad (2.17)$$

Dividing equation 2.16 by the surface area results in equation 2.18. Because A_{sur} equals $L \cdot W$, this equation is simplified (equation 2.19). The elimination of *L* and *W* makes the calculations independent of the surface dimensions of the capacitor.

$$C_{den} = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot \left(L \cdot W + \left(\left(\frac{L}{p} \cdot \frac{W}{p} \right) \cdot 2 \cdot \pi \cdot r \cdot d \right) \right)}{t_{di} \cdot A_{sur}} [F/m^2], \qquad r < \frac{1}{2}p \tag{2.18}$$

$$C_{den} = \frac{\varepsilon_0 \cdot \varepsilon_r}{t_{di}} \cdot \left(1 + \frac{2 \cdot \pi \cdot r \cdot d}{p^2} \right) [F/m^2], \qquad r < \frac{1}{2}p \tag{2.19}$$

Trenches with a radius that is larger than half the pitch will start to overlap each other and merge into one slit, thereby sacrificing functional area. Therefore, equation 2.18 and 2.19 are only valid for the boundary condition $r < \frac{1}{2}p$.

Results and discussion

Equation 2.10 and 2.19 are calculated and plotted for different values of the pitch, radius and depth to gain insight in the advantage of trench capacitors over the flat capacitors. The electric constant in vacuum is $8.85 \cdot 10^{-12}$ F/m. The relative dielectric constant is dimensionless and for silicon dioxide 3.9 [22]. The thickness of the dielectric layer is set at 10 nm to meet the 10 V breakdown voltage (equation 2.6). The radius, depth and pitch values are chosen based on what is needed and producible for the integration in the F2R.

Variation in pitch and radius

Equation 2.10 and 2.19 are calculated and plotted with different radii and pitch of the trench capacitors, while keeping the depth of the trench fixed at 30 µm. To avoid rigidity issues in the 40 µm thick silicon island, the depth of the trench is limited at 30 µm. Table 2.1 shows the results of the calculation of the relation between the radii of the trenches and the capacitance density for different pitch variations. The data is plotted in Fig 2.5 and 2.6.

Capacitance density (nF/mm²)

Trench radius (µm) \ *Pitch (µm)*	*0*	*7*	*6*	*5*	*4*
0	*3.5*	-	-	-	-
0.5	-	*10.1*	*12.5*	*16.5*	*23.8*
1.0	-	*16.7*	*21.5*	*29.5*	*44.1*
1.5	-	*23.4*	*30.6*	*42.5*	*64.5*

Table 2.1. Capacitance density for different trench radii and pitches.

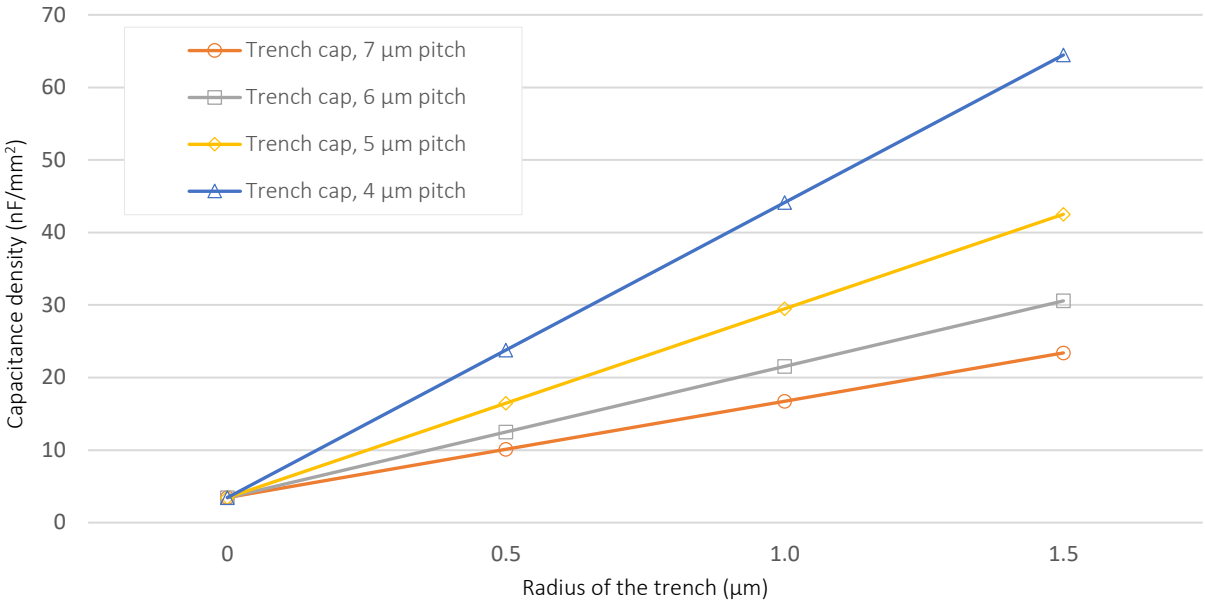


Figure 2.5. Relation between the capacitance density and different trench radii for varying pitches.

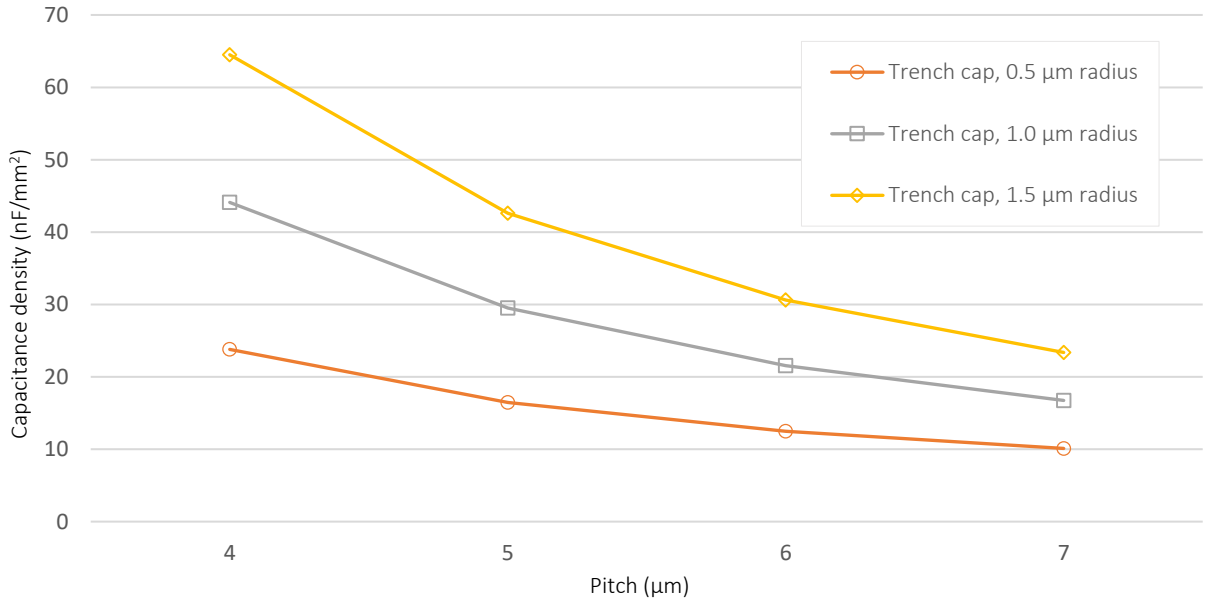


Figure 2.6. Relation between the capacitance density and different pitches for varying trench radii.

Fig 2.5 shows the linear relation between the trench radius and the capacitance density. Reflecting back on equation 2.19 this is expected. The equation shows an almost direct proportionality of the capacitance density to the radius since the first term in the equation ($\varepsilon_0 \cdot \varepsilon_r$) is negligible compared to the second term for the above-mentioned dimensions. However, when the pitch is increased to disproportionate dimensions compared to the radius, the first term starts to dominate. Fig 2.6 shows the parabolic relation between the pitch distance and the capacitance density for fixed trench radii, which is in line with term p^2 in equation 2.19.

Variation in pitch and depth

Equation 2.10 and 2.19 are plotted for different depths of the trenches and different pitch dimensions while keeping the trench radius fixed at 1.0 µm. Table 2.2 shows the results of the calculation of the relation between the depth of the trench and the capacitance density for different pitch variations. The data is plotted in Fig 2.7 and 2.8.

Capacitance density (nF/mm²)

Trench depth (µm) \ Pitch (µm)	0	7	6	5	4
0	3.5	-	-	-	-
10	-	7.9	9.5	12.1	17.0
20	-	12.3	15.5	20.8	30.6
30	-	16.7	21.5	20.5	44.1

Table 2.2. Capacitance density for different trench depth and pitch.

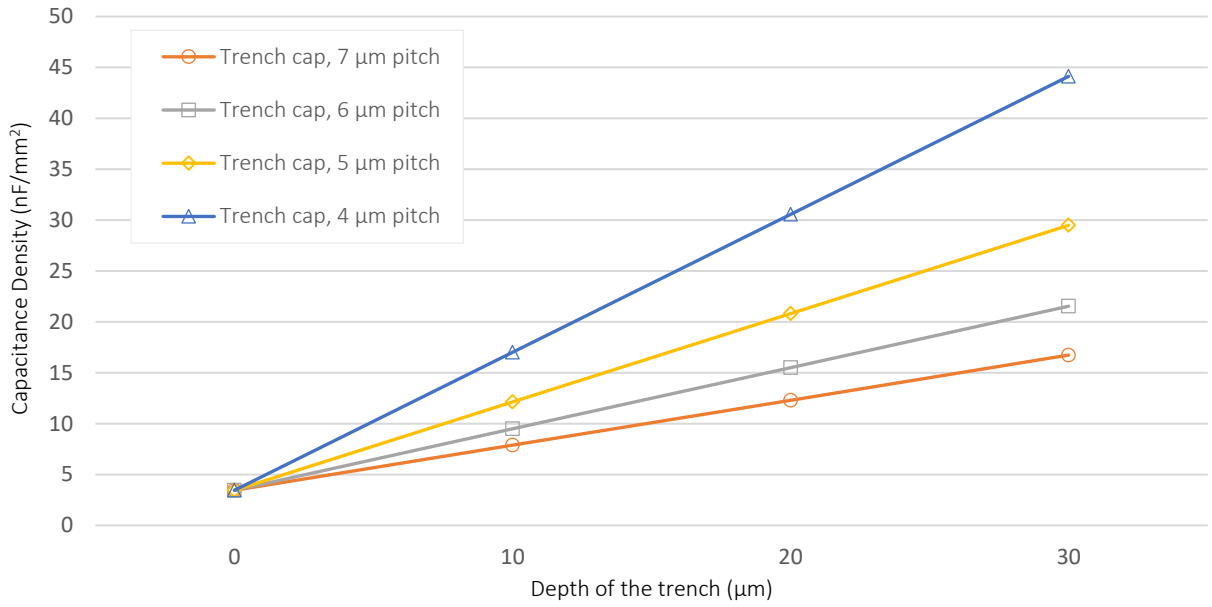


Figure 2.7. Relation between the capacitance density and different trench depth for varying pitches.

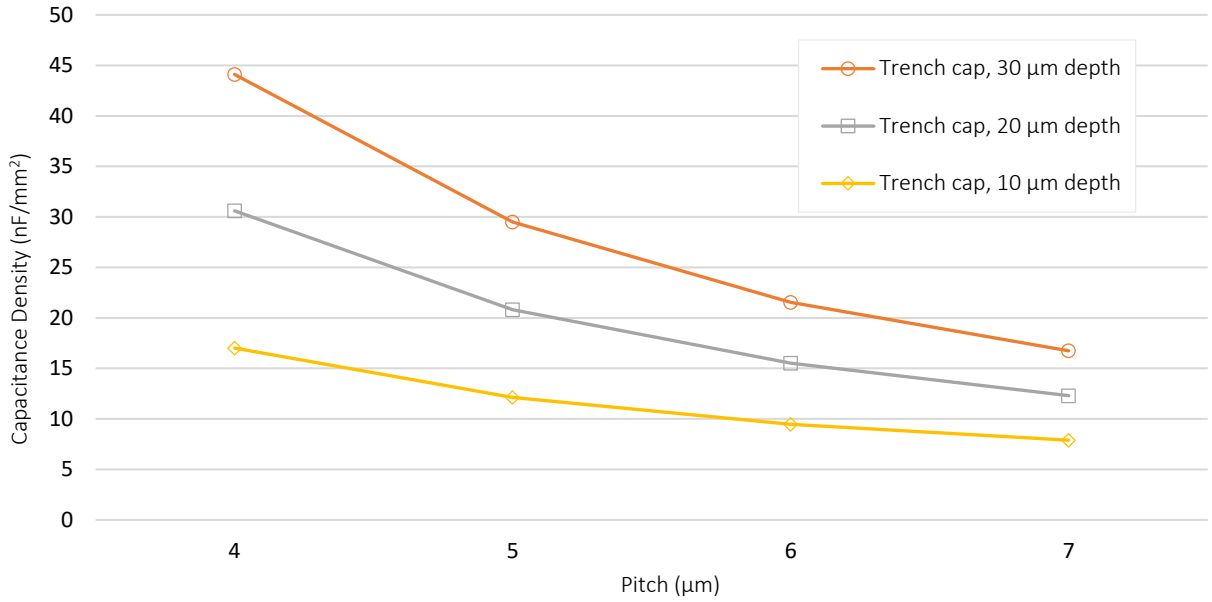


Figure 2.8. Relation between the capacitance density and different pitches for varying trench depths.

Fig 2.7 shows the linear relation between the trench depth and the capacitance density. Again, reflecting back on equation 2.19 this is expected. The equation shows the same direct proportionality of the capacitance density to the depth as to the radius. However, as mentioned before, the depth is limited since the silicon islands in the F2R flow only have a thickness of 40 µm. Trenches deeper than 30 µm are likely to cause problems in the rigidity of the silicon islands. Fig 2.8 shows the parabolic relation between the pitch distance and the capacitance density for fixed trench depth, which is in line with p^2 in equation 2.15.

Conclusion

To conclude the capacitance calculations, a relation between the geometrical parameters and the capacitance density is found. The model shows; 1) the linearity of the capacitance density to the trench radius and trench diameter for a fixed pitch and 2) the parabolic relation between the capacitance density and the pitch for fixed trench radii and trench depth. The model shows a theoretical increase in capacitance density from 3.5 nF/mm^2 for the flat capacitor to 64.1 nF/mm^2 for the optimal capacitor configuration with a pitch of 4 µm, a trench depth of 30 µm, a trench radius of 1.5 µm and a 10 nm thick silicon dioxide dielectric. This means a maximum capacitance density increase by a factor of 18.

2.4.2 Capacitance increase through stacked dielectrics

To increase the capacitance even further, the relative dielectric constant can be increased. Silicon dioxide has been the dominant dielectric throughout the history of IC production due to its unique compatibility with silicon IC manufacturing and the huge wealth of experience in industry in the reliable and repeatable production of this dielectric [19]. When the silicon dioxide thickness is scaled down to thicknesses of 5 nm or less, direct tunneling starts to limit the use of silicon dioxide in MOS devices. In order to increase the capacitance, research has been conducted towards dielectric materials with higher relative dielectric constant ε_r, the so-called high-k dielectrics, especially in the field of thin-film transistors. In literature the terms k and ε_r, are used interchangeably, in this work the relative dielectric constant is referred to as ε_r. Equation 2.10 shows the direct proportionality of the capacitance to the relative dielectric constant.

LPCVD silicon nitride is a dielectric that is commonly available in most micro fabrication facilities and which has a relatively high dielectric constant of 7.9. However, the interface between silicon nitride and silicon is not very well defined and can result in leakage currents and reduced breakdown voltages. A commonly used method to mitigate these issues is to line the silicon nitride layer with thin silicon oxide layers, resulting in a so called oxide-nitride-oxide (ONO) multilayered dielectric. Generally, a minimum of 5 nm silicon dioxide is needed for a reliable ONO dielectric [21].

To get a feeling for the increase in capacitance density that can be obtained by the use of an ONO stack instead of a pure oxide dielectric, a 25 nm thick silicon dielectric was compared with a 5-10-10 nm ONO stack. In the case of the silicon oxide layer the capacitance density is calculated to be 1.4 nF/mm^2. In the case of the ONO stack the capacitance density is calculated to be 1.7 nF/mm^2. Note that although the dielectric breakdown and the thickness of the layer is equal, an improvement in capacitance density is established.

2.5 Conclusion

The previous chapter has demonstrate the possibility to simplify the fabrication of low and high voltage capacitors by using a multilayer ONO dielectric. Next, the advantage of a trench capacitor over a plate capacitor is shown and the benefits of using a multilayered ONO dielectric is shown compared to a single layer dielectric.

3. Trench capacitor process flow and mask design

3.1 Introduction

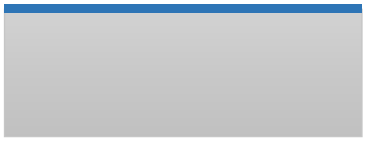
For the fabrication of the trench capacitors, a dedicated flowchart and mask set is design. Apart from the initial idea and the conditions that follow from the required integration in the F2R flow, little of the processing was defined. Therefore, numerous small experiments, so called shortloops, were performed to optimize the fabrication process. Many of the experiments were verified by one or two iteration steps. However, some processes needed more attention to achieve the desired result. These processes are discussed in Chapter 4. The combination of the process steps result in a device specific process flow, which can be seen as the blueprint for the fabrication of the trench capacitors. The designed process includes five photolithography steps that require five corresponding mask layers. This chapter first describes the fabrication of the trench capacitors, and choices that are made regarding the processing are discussed. Secondly, the mask set, which is designed for the fabrication process, is explained.

3.2 Process flow

The process flow for the trench capacitors describes the fabrication process from plane wafer to measurable devices. The process flow is accompanied with a dedicated flowchart, which can be found in the appendix section A. Due to the high aspect ratio of the trenches, it is difficult to visualize an on-scale representation of the trench capacitors. Therefore, the illustrations in the process flow in this section are schematic cross-sections and do not correspond to the real life dimensions and scales. Three off-scale trenches represent the trench field in the capacitor. In addition, the thickness of the layers is off-scale because some layers would disappear from the illustration in a true-to-life representation. The footnotes refer to corresponding sections in the appendix B for extensive information regarding the process technology that is involved in the fabrication. The process flow is split in three sections, called technical stages; 1) trench etch, 2) deposition of the dielectric and top electrode and 3) closing of the trench and bond pads deposition.

3.2.1 Trench etch

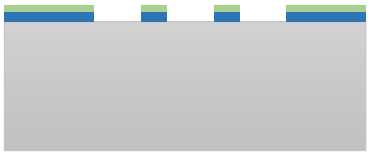
The fabrication of the trench capacitor starts with a highly arsenic doped n-type silicon wafer. The silicon substrate functions as the bottom electrode of the capacitor and therefore a low resistivity is required. the resistance of the doped silicon substrate is in the range from 1 to 3 mΩ·cm



The wafer is first cleaned in a Cintillio cleaning tool. Next, a 700 nm thick layer of silicon dioxide is deposited using PECVD[1]. The silicon dioxide will function as a hard mask to pattern the silicon substrate.

[1] Section 9.2.1

To pattern the silicon dioxide, a 1300 nm thick layer HPR504 in spin coated onto the wafer and patterned by a photolithography[2] step . The focus for the lithography is fixed and the exposure energy doses was determined at 100 mJ/cm^2. To pattern the photoresist the TRC_TRENCH mask is used.



A dry etch step transfers the pattern from the photoresist into the silicon dioxide. The process development for dry etching the silicon dioxide and the Deep Reactive Ion Etch (DRIE) for the trenches in the silicon substrate are explained in chapter 4.

The trenches in the silicon substrate are etched using the a special DRIE process, the so called BOSCH process[3]. In addition, the duration of the BOSCH process removes the photoresist from the wafer.

After etching the trenches, the silicon dioxide is removed by a wet etch step in a bath with BOE7:1[4] for 10 minutes, followed by a rinse and dry step to clean the wafer. After removal of the oxide, the polymers that are deposited on the trench wall during the DRIE process are removed in an oxygen plasma for 45 minutes at 130°C. The first technical stage ends with the clean patterned silicon wafer.

3.2.2 Dielectric and top electrode deposition

Two different dielectric layers are studied in the development of the trench capacitor. First, a silicon dioxide layer and second, a silicon dioxide – silicon nitride – silicon dioxide (ONO) multilayer dielectric. The thickness of the dielectric layers can be adjusted to the required breakdown voltage and capacitance. To fabricate the low and high voltage parts in the multilayer dielectric, the top silicon dioxide is partially removed, as explained in section 2.3.1. This technical stage first describes the fabrication of the silicon dioxide single layer dielectric, followed by the ONO multilayer dielectric and the creation of the low and high voltage parts in the dielectric. Subsequently, The process flow continues with the deposition of the top electrode.

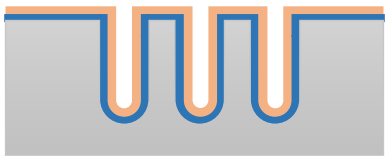
[2] B.2 Photolithography
[3] B.3 Dry Etching
[4] B.4 Wet Processing

Single layer silicon dioxide dielectric

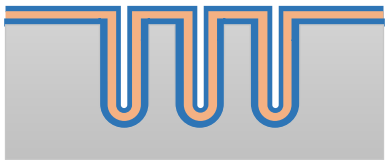
Before deposition of the dielectric layer and top electrode, the wafer is cleaned to prevent contamination of the furnace tubes. In addition, the native oxide is removed by an etch wet etch step in BOE7:1. After cleaning, a layer of silicon dioxide is thermally grown[5] on the wafer at 850°C. Is layer is deposited by dry oxidation. The thickness of the silicon dioxide is chosen according to the required breakdown voltage and capacitance.

Multilayer ONO stacked dielectric

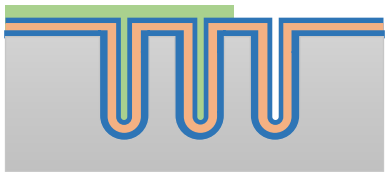
As with the single layer dielectric, before deposition of the first dielectric layer the wafer is cleaned. After cleaning, first a layer of silicon dioxide is thermally grown[5] at 850°C.



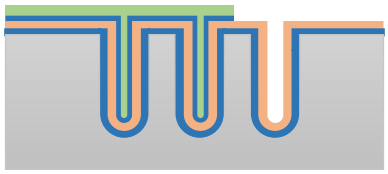
Onto the silicon dioxide layer, a silicon nitride layer is deposited using LPCVD[1].



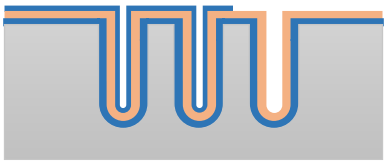
The second layer of silicon dioxide is deposited using LPCVD TEOS[1] and can chosen according to the required breakdown voltage for the high voltage part of the dielectric layer.



To pattern the top silicon dioxide layer, a negative photoresist is spin coated onto the wafer. Because it is difficult to illuminate a positive photoresist to the bottom of the trench in order to be able to expose and develop it[2], a negative photoresist is used. For this photoresist the unexposed resist will be removed during developing. To pattern the photoresist the TRC_ONO mask is used.

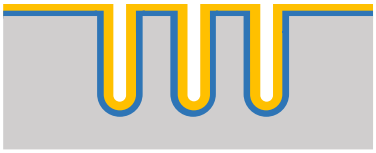


For the fabrication of the low voltage part in the dielectric, the top silicon dioxide is removed by a wet etch step in a bath with BOE7:1. The etch times is determined by the chosen layer thickness.

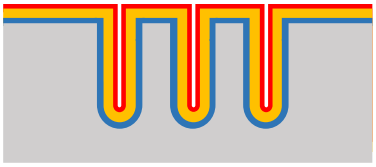


To remove the photoresist from the trenches after etching the silicon dioxide, the wafer is cleaned in an oxygen plasma for 45 minutes at 130°C.

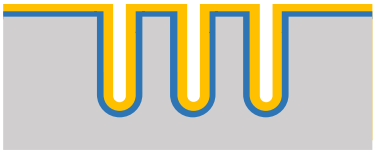
After fabrication of the dielectric layer, the top electrode is applied. In the remainder of the process flow, the single layer silicon dioxide dielectric is used in the illustrations.



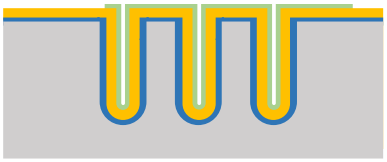
The top electrode of the capacitor is a 400 nm thick layer of doped polycrystalline silicon (Poly-Si). Details regarding the electrical properties of the Poly-Si are described in chapter 4. To obtain the Poly-Si layer, first a 400 nm thick amorphous silicon layer is deposited by LPCVD.



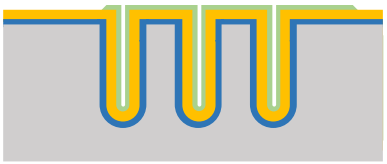
Next, a 100 nm thick layer of phosphosilicate glass[1] (PSG) is deposited as a solid dopant source. A 30 minutes anneal step at 1000°C migrates the dopant atoms from the PSG into the amorphous silicon[6]. The elevated temperature causes the crystals in the amorphous silicon to rearrange and thereby forming polycrystalline silicon.



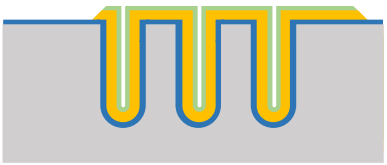
After the anneal, the PSG is removed using BOE7:1 for 90 seconds[4]. A sheet resistivity of ~1 mΩ·cm is obtained in the Poly-Si layer.



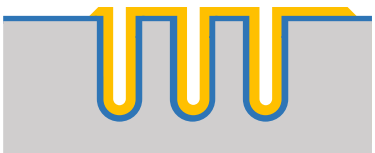
To pattern the Poly-Si, a 1300nm thick layer of HPR504 is spin coated onto the wafer and patterned by a photolithography step, using a focus of -0.3 µm and exposure energy doses of 120 mJ/cm^2. To pattern the photoresist the TRC_POLY mask is used.



To improve the step coverage of the silicon dioxide that will later be deposited over the Poly-Si, the photoresist is baked on a hot plate at 150°C for 120 seconds after development. The bake cause the photoresist to reflow, which creates a slope of ~45° at the edges of the photoresist.

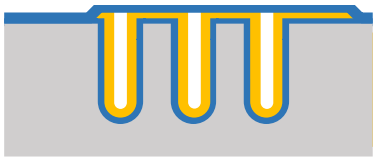


A dry etch process pattern the Poly-Si. During the etch, the slope in the photoresist is transferred into the Poly-Si.

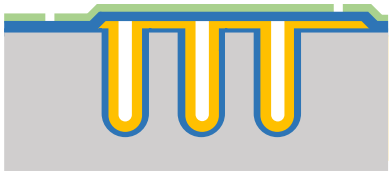


After etching of the Poly-Si, the photoresist is stripped in an oxygen plasma for 45 minutes at 130°C. The etch recipe to pattern the Poly-si lands on the dielectric layer, it is possible that very thin dielectric layers are removed in this process step despite the selectivity of the etch recipe.

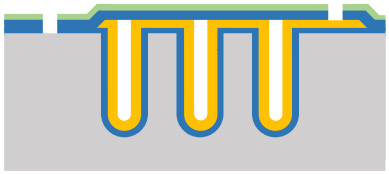
3.2.3 Trench closing and bond pad deposition



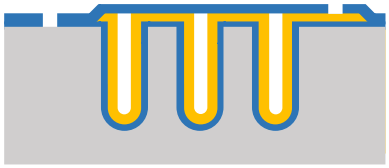
After deposition of the dielectric and top electrode, the trench capacitors are closed. Closing of the trenches is crucial to prevent damage to the capacitors by the etch process for the buried trenches in the F2R process flow, as discussed in section 1.2. Using PECVD[1], a 700 nm thick layer very low stress silicon dioxide closes the trenches.



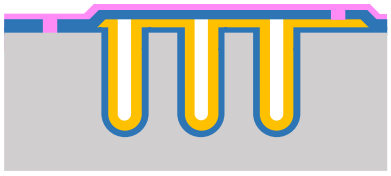
After deposition of the silicon dioxide, a 1300nm thick layer of HPR504 is spun onto the wafer and patterned by a photolithography step. The focus for the lithography is -0.3 µm and the exposure energy doses in determined at 150 mJ/cm. To pattern the silicon dioxide the TRC_ CONTACT mask is used.



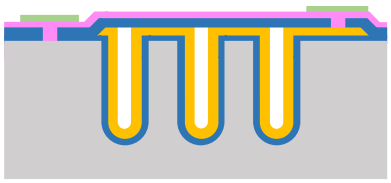
Next, the silicon dioxide is opened by a dry etch step to create contacts to the Poly-Si and the silicon substrate.



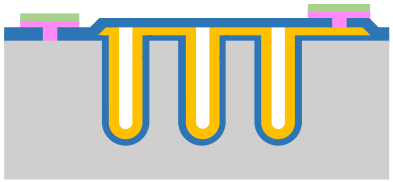
The photoresist is stripped in an oxygen plasma for 5 minutes.



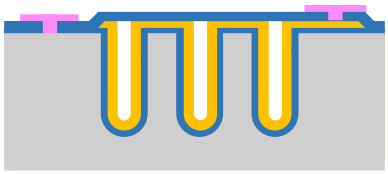
1 µm AlCu1% is deposited for the formation of bond pads. The small amount of copper in the aluminum expands the lifetime of aluminum by encountering damage due to electro migration in the aluminum layer [25]. Before deposition of the aluminum, the wafer is dipped in a bath of hydrogen fluoride (HF) and rinsed to remove the native oxide on the surface to improve the contact resistance of the metal to the silicon[4].



To pattern the bond pads, 1300nm HPR504 is spin coated on the wafer and patterned by a photolithography step. The focus for the lithography is -0.3 µm and the exposure energy doses in determined at 150 mJ/cm. To pattern the silicon dioxide the TRC_ AL mask is used.



To pattern the bond pads, 1300nm HPR504 is spin coated onto the wafer and patterned by photolithography. The focus for the lithography is -0.3 µm and the exposure energy doses in determined at 150 mJ/cm. To pattern the silicon dioxide the TRC_ AL mask is used.



Finally, the remaining resist is stipped in an oxygen plasma for 5 minutes.

3.3 Mask Design

3.3.1 Introduction

The TRC mask set can be considered as the starting point for the decoupling capacitors. The purpose of this mask set is to fabricate trench capacitors to verify the theoretically predicted capacitance values and to provide insight in the critical dimensions for the capacitor design. It was decided to design a new mask set for the production of the trench capacitors because there was no mask set available in the PInS cleanroom that could provide the required structures. This chapter describes the layout of the mask set and explains the different layers of the mask. Extensive information regarding the reticle information and mask design is given in section C.

3.3.2 TRC overall layout

The TRC mask set can be divided in three areas. Fig 3.1 shows the design with the three different areas indicated by the numbers and corresponding blue, green and red shaded areas. The first area, shaded blue, is designed to measure different capacitor designs. The second area, shaded green, includes structures to measure the sheet resistance and contact resistance of the used materials in the capacitors like the aluminum and Poly-Si. The third area, shaded red, provides insight in the operation window regarding to the diameters for the trenches.

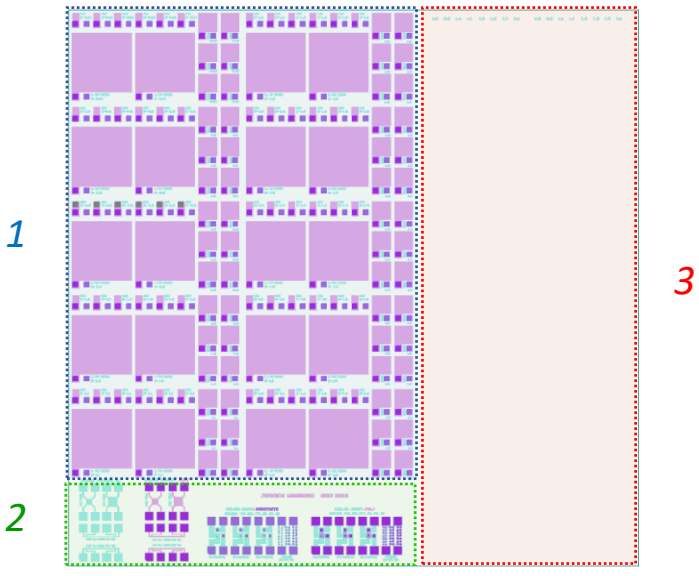
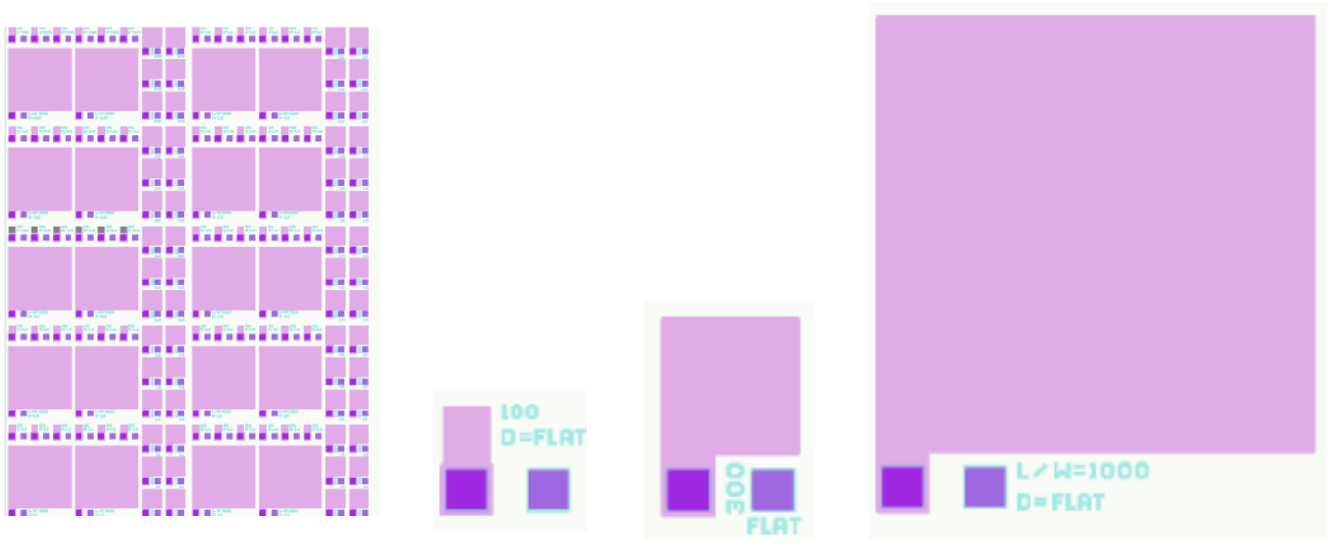


Figure 3.1, TRC Mask design with three different areas; 1) an area with capacitors, shaded blue, 2) test structures to test sheet and contact resistance, shaded green and 3) columns with different hole sizes for the investigation of the optimal trench size, shaded red.

Trench capacitors

The area with capacitors is designed to measure different configurations of the capacitors (Fig 3.2a). The TRC mask set includes three different sized capacitors. The capacitors are indicated with the numbers 100, 300 and 1000, as shown in Fig 3.2b, 3.2c and 3.2d. The number refers to the length and width of the area in the capacitor where trenches can be applied. In the remainder of this work, these capacitors are labeled as CAP100, CAP300 and CAP1000, respectively. The variation in area size enables testing of the scalability of the capacitors.

To gain insight in the influence of the trenches on the breakdown voltage and capacitance of the capacitor, trenches are applied to the CAP100, CAP300 and CAP1000 capacitors. The diameter of the holes on the mask to fabricate the trenches varies from 0.8 to 1.6 µm. In appendix section C.2, a detailed overview of the variation in trenches over the capacitors and the exact dimensions of the test devices is presented.



a) *b)* *c)* *d)*

Figure 3.2. Illustration of; a) the topography of the capacitors, b) the CAP100, c) the CAP300 and d) CAP1000.

Van der Pauw and Kelvin structures

The working principle of a capacitor is based on an insulating layer between two conducting plates. In an ideal capacitor, the thickness of the dielectric layer is the only parameter that influences the electrical behavior, and the capacitance is therefore directly inversely proportional to the thickness of the dielectric. However, in reality several other factors influence the electrical behavior as well [19]. The series resistances in the material that is used for the electrodes and the contact resistance between two materials are factors that influence the working of the capacitor. For accurate information regarding the performance of the capacitor, it is important to gain insights in the series resistances. Van der Pauw structures and Kelvin structures are included on the TRC mask set to provide insight into different sheet resistances and contact resistances.

By performing a Van der Pauw measurement, a four-point probe system is placed around the perimeter of a sample (Fig 3.3a). When a current is applied over two adjacent probes, the voltage can be measured over the other two probes and the resistance can be calculated. Van der Pauw found that the relation between the voltage, current and sheet resistance may be written as [26]:

$$R = 4.53 \cdot \frac{V}{I} \qquad (3.1)$$

The electrical resistance can be written proportional to the length *l*, cross section area *A,* or *w·t*, and specific resistivity *ρ* of the material (equation 3.2).

$$R = \rho \frac{l}{A} = \rho \frac{l}{w \cdot t} \tag{3.2}$$

The specific resistivity is expressed in *Ω·cm* and is inversely proportional to the electronic charge *e*, the carrier mobility *μ* and the carrier concentration *n* (equation 3.3). For semiconductors the carrier concentration can be either the electrons (n-type) or holes (p-type) concentration.

$$\rho = \frac{1}{n \cdot e \cdot \mu} \tag{3.3}$$

The sheet resistance R_s is the resistance per unit area and expressed in *Ω/square* (equation3.4). The sheet resistance is equal to the resistivity of the material divided by the thickness of the layer.

$$R_s = \frac{\rho}{t} \tag{3.4}$$

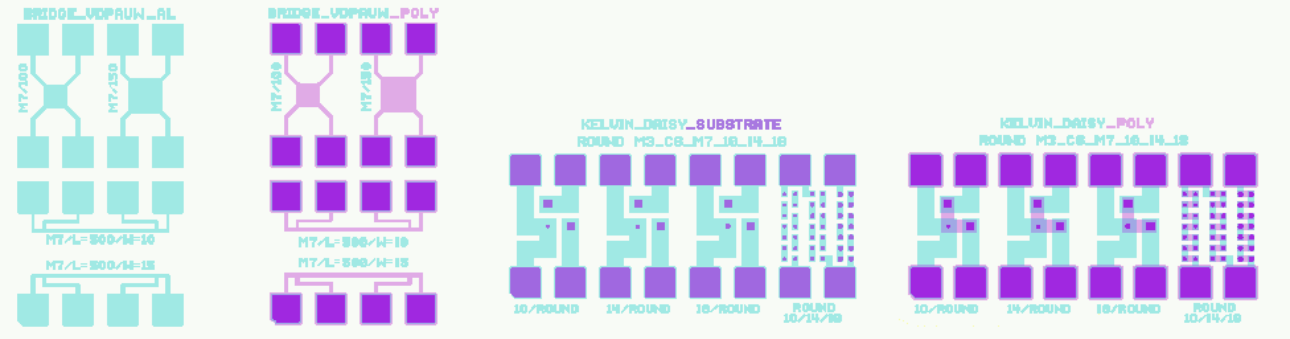
Van der Pauw structures are designed to have equal length and width. Therefore, the measured resistance is the same as the sheet resistance (equation 3.5).

$$R = R_s = \frac{\rho}{t} \tag{3.5}$$

The Van der Pauw measurement can be used to determine the resistivity of the material when the thickness of the layer is known or can be used to determine the thickness of the layer when the resistivity of the material is known.

Kelvin structures measure the contact resistance of metal-semiconductor junctions. Two probes are placed on an upper material layer and two probes are placed on an underlying layer (Fig 3.3b). The four-point measurement is carried out by forcing a current between a probe connected to an upper material and a probe connected to the bottom material. The voltage is then measured between two other probes and the specific contact resistance is calculated from the voltage, current and contact surface (equation 3.6).

$$\rho_c = R_c \cdot A_c \tag{3.6}$$



a) *b)*

Figure 3.3. a) Van der Pauw structures and b) Kelvin structures.

In the case of the trench capacitor, there are several factors that can influence the capacitance, for example; 1) the resistivity of the aluminum, Poly-Si and silicon substrate and 2) the contact resistance between the Poly-Si and aluminum, and between the silicon substrate and aluminum. With the above-mentioned structures, information regarding these values can be obtained.

Diameter test structures

An important step in the process flow of the trench capacitors is the closing of the trenches by a 700 nm thick very low stress silicon dioxide layer. This layer will function as the hard mask for the etching of the buried trenches in the F2R process as described in section 1.2.1. When the trenches are not closed, the etch process to etch the buried trenches will damage the capacitor. The diameter of the trench is a crucial parameter in the design of the trench capacitors. The silicon dioxide layer cannot close an oversized trench. On the other hand, an undersized trench causes problems with the deposition of the dielectric layer and top electrode inside the trench. Furthermore, experiments have shown the complexity to fabricate (sub)micron trenches. To determine the optimal trench diameter, long columns with holes of varying diameters are designed on the mask. The diameter varies from 0.8 µm to 1.5 µm. The coverage of the dielectric layers and top electrode inside the trench and the closing of the trench by the applied silicon dioxide is verified by cleaving the sample and investigating the cross-section. The direction of a cross-section through the sample is determined by the crystal orientation. The crystal orientation causes a silicon wafer to break in the <110> direction. This orientation corresponds to the x and y axis of the mask design. To increase the chance of a successful cross-sectional cleavage through a hole when the wafer is broken according to the x axis, each column is slightly shifted in the y direction (Fig 3.4).

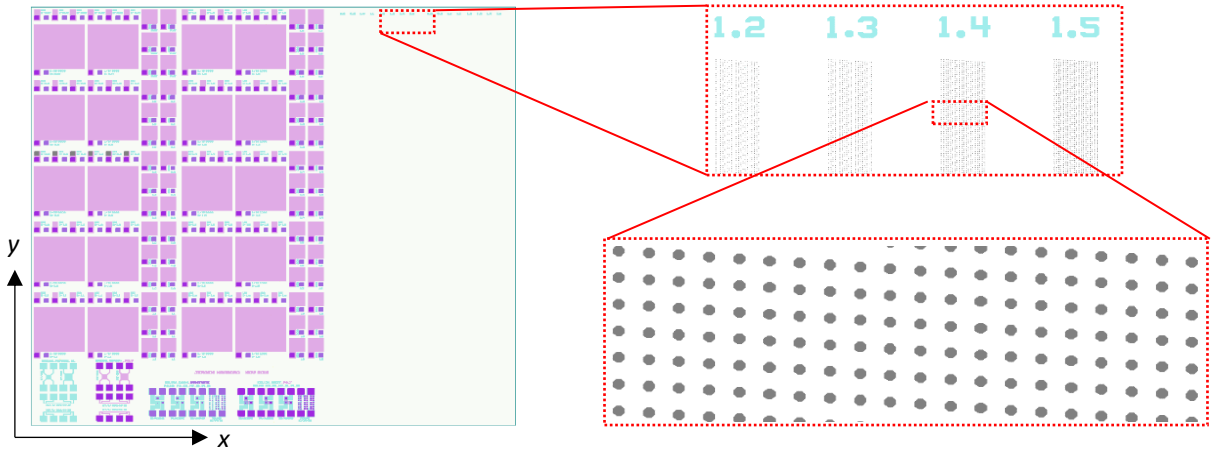


Figure 3.4. Illustration of the columns with holes of different diameter to provide insight in the optimal trench diameter.

3.3.3 TRC Mask set

The mask set is a five layer masks set, divided over two reticles, as described in table 3.1. This section describes the different layers of the mask. Fig 3.6 shows an image of the CAP100 on the mask with a legend that indicates the different mask layers.

Name	*Layer*	*Reticle*	*Mask type*
TRC_TRENCH	*1*	*TrenchCaps / 051218-JNG01*	*Clear tone*
TRC_POLY	*2*	*TrenchCaps / 051218-JNG01*	*Clear tone*
TRC_CONTACT	*3*	*TrenchCaps / 051218-JNG01*	*Clear tone*
TRC_AL	*4*	*TrenchCaps / 051218-JNG01*	*Clear tone*
TRC_ONO	*5*	*CBOX-OXIDE / 150319-JNG01*	*Clear tone*

Table 3.1, TRC mask information

TRC_TENCH mask

The TRC_TRENCH mask is the layer to pattern the silicon dioxide that forms the hard mask for the DRIE process to etch the trenches in the silicon substrate. The mask contains the columns with holes to investigate optimal trench diameter and the fields with trenches that are applied to the capacitors. The holes for the capacitors are orientated in a centered rectangular lattice at a pitch of 4 µm (Fig 3.5). To reduce the computer file size, the holes have an octagonal shape. The photolithography and etch processes in the cleanroom round the corners of the octagonal shape. The result is a circular hole in the silicon dioxide.

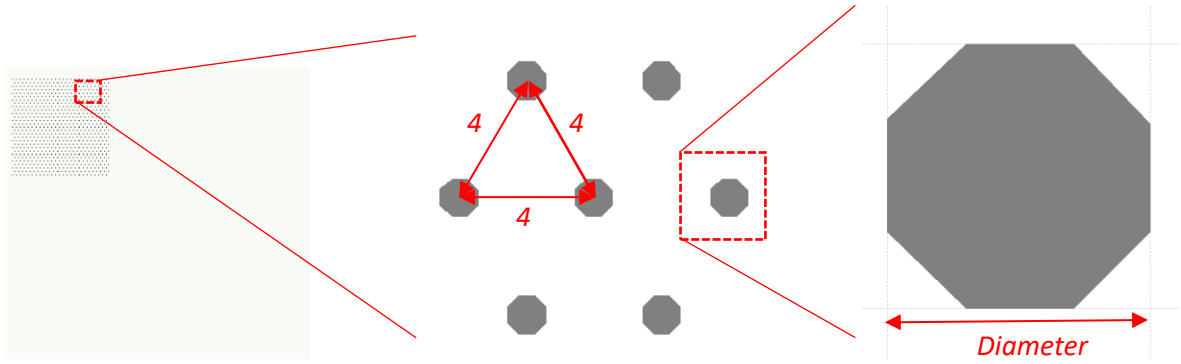


Figure 3.5. Image of the columns with holes of different diameter to test the trench size.

TRC_POLY mask

After etching of the trenches and the deposition of the dielectric layer and the Poly-Si, the Poly-Si is patterned with the TRC_POLY mask layer. Since the Poly-Si is the top electrode of the capacitors, the dimensions of the Poly-Si are determinative for the calculations of the absolute capacitance and the dimensions of the TRC_POLY mask layer are determinative for the calculation of the capacitance per footprint area. The TRC_POLY mask layer does also include structures that are integrated in the Van der Pauw and Kelvin structures to measure the characteristics of the Poly-Si and the aluminum-poly contacts.

TRC_CONTACT and TRC_AL mask

The purpose of the TRC_CONTACT mask is to open the silicon dioxide layer that is applied to close the trenches. The opening provides a contact between 1) the aluminum and the Poly-Si top electrode and 2) the aluminum and the silicon substrate, which functions as the bottom electrode. After opening of the silicon dioxide, a layer of aluminum is deposited. The TRC_AL mask layer patterns the aluminum to create the bond pads.

TRC_ONO mask

The fifth mask layer, which is located on the second reticle, is designed to fabricate the low and high voltage parts in the ONO dielectric layer. The top silicon dioxide layer of the ONO is patterned using the TRC_ONO mask layer. Where the other four mask layers are used in combination with a positive photoresist, this mask layer used with a negative photoresist. Therefore, the open mask areas are the areas where the silicon dioxide is preserved.

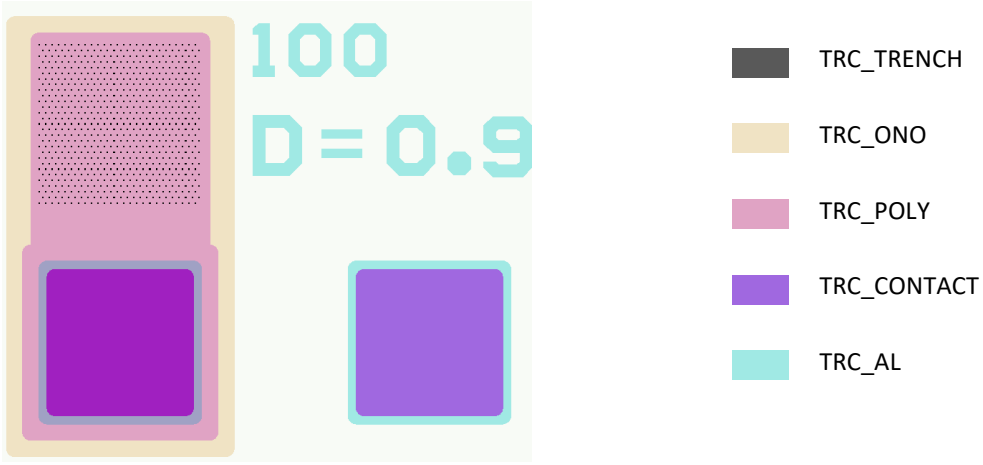


Figure 3.6, Illustration of the combined mask layers for the CAP100 with 0.9 µm holes.

4. Process development

4.1 Introduction

In the previous chapter the process flow and mask design were explained. The process flow for the trench capacitors consist of 94 individual process steps. The fabrication of the trench capacitors is step-by-step executed in Philips Innovation Service (PInS) cleanroom. A part of the fabrication is performed using established processes that are well understood. These processes are verified by one or two experiments to confirm their performance. However, some fabrication steps required more attention to achieve the desired result. Reasons to further investigate a specific topic can be 1) to obtain insight in the interaction of different parameters within one process or 2) the interaction with consecutive process steps.

This chapter first describes the development of a dedicated etch recipe to etch 1.2 µm wide, high aspect ratio trenches. Next, the dielectric deposition and patterning of this dielectric are explained, followed by the PSG deposition and doping of the Poly-Si and the patterning of the Poly-Si. Finally, the process to close the trench is reviewed.

4.2 DRIE etch for high aspect ratio microscale trenches

One of the objectives of this work is the development of high aspect ratio microscale (HARM) trenches. Section 4.5 addresses the process needed to close the trenches before the fabrication of the buried trenches. In the current stage of the integration process, there are different options to close the trench. However, it is beyond doubt that a small trench opening will be easier to close. In section 4.4 the necessity for a minimum trench opening of 1.2 µm will be shown. For the closing process, the trench diameter would ideally be exact this 1.2 µm. Since there was no DRIE etch recipe available in the PInS cleanroom to etch these kind of trench structures, a new recipe was developed. This section discusses the development of the DRIE recipe to etch 1.2 µm wide high aspect ratio microscale (HARM) trenches. The development is executed in close cooperation with the responsible process engineer. For confidentiality reasons, the exact operation settings are left out of the report.

The trenches are etched using the BOSCH process[5]. This dry etch process is characterized by an alternating introduction of passivation and etching gasses into the process chamber. The passivation gasses deposit a protective film in the trenches. During the etching cycle, a so called boost phase removes the protective film from the bottom of the trench. After the boost phase, the exposed silicon is etched in the etch phase. This etch technique allows the fabrication of high aspect ratio structures. An additional advantage of the BOSCH process is the controllability and high silicon to silicon dioxide selectivity. Typical parameters that enable accurate tuning of the process are; platen power in the boost phase, platen power in the etch phase, O_2/SF_6-flow, C_4F_8-flow, etch cycle time, etch cycle pressure, passivation cycle time and passivation cycle pressure.

The DRIE process, to etch the trenches, is performed on the STS CPX cluster tool in the Pins Cleanroom. Experiments have shown that the fabrication of HARM trenches is at the limit of the machine's capabilities. To get an impression of the etch behavior, trenches with a diameter from 1.0 µm to 2.0 µm are investigated. The trenches are located on the same wafer and etched with the same recipe, which was design for small structures. An overall stable relation between the trench diameter and depth can be observed from 1.3 µm to

[5] B.3 Dry etching

2.0 µm diameter (Fig 4.1). A tipping point in the etch behavior is found at 1.2 µm. From this point the depth of the trench drastically decreases. It is known that the etch rate in microstructures decreases when the aspect ratio increases [27]. Fig 4.1 shows that this behavior is magnified in trenches smaller than 1.2 µm. This phenomena is also found in other characteristics that are due to the etch recipe. The major bottleneck seems to be to control the flux of the gasses inside the HARM trenches.

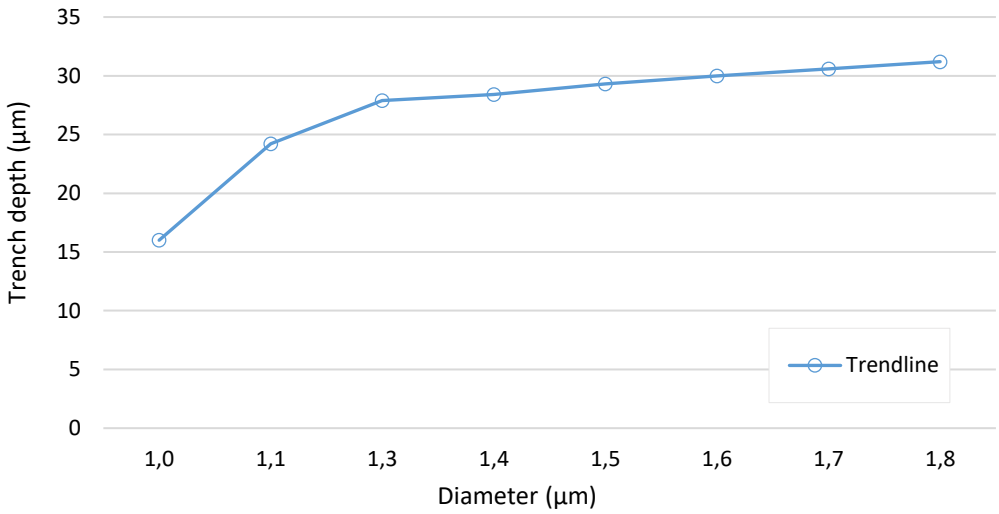


Figure 4.1. Etch rate vs. trench diameter for HARM trenches.

After verifying with the equipment manufacturer, it is confirmed that there is little to no information available regarding the process settings for this machine to obtain the desired result. Therefore, a new recipe is developed. Note that this recipe is optimized for the fabrication of 1.2 µm HARM trenches. Trenches with other diameters are probably more efficiently etched with other recipes.

The result of an etch recipe for HARM trenches is heavily dependent on the interplay between the different process settings. The development of a recipe is therefore an iterative process that requires constant tuning. For the development of the recipe for the HARM trenches, 36 test runs are performed to acquire insight in the behavior of the parameters and their influence on the process. This section describes the most important findings from the experiments. First, the photolithography procedure and silicon dioxide hard mask dry etch are discussed, followed by the optimization of the DRIE recipe for the trenches.

4.2.1 Oxide hard mask for DRIE

The trench etch procedure start with the photo mask. To control the flow of gasses in the trench during the BOSH process, it is important to have straight walled holes in the masking layer. In addition, to reach a depth of 30 µm in the trench, it is likely that the ion bombardment on the resist will be intense. In most cases the selectivity of the etchant towards the photoresist is significantly higher than its selectivity to the etch target, therefore the photoresist will remain with sufficient thickness to protect the etch target. However, when an etch recipe is excessively long, the photoresist can be etched away with exposure of the underlying material as a result. The duration of the dry etch recipe for the trenches reaches a critical length where the 1300nm thick layer of HPR504 resist will not be sufficient to protect the wafer.

A possible solution could be to increase the photoresist thickness. However, a thicker layer HPR504 is not suitable to pattern the 1.2 µm diameter holes with straight walls. Previous studies have shown promising results regarding the use SPR-220 resist for HAR structures in photoresist layers [28]. Unfortunately, SPR-220

is currently not available as a production photoresist in the PInS cleanroom, hence this is not an option for the production of the trench capacitors. Therefore, the use of silicon dioxide hard mask was selected. The silicon dioxide layer is patterned using photolithography and dry etched to transfer the pattern from the photoresist into the silicon dioxide. Since it is expected that the transfer of narrow holes from the silicon dioxide into the silicon substrate will increase ±0.2 µm, the fabrication of a 1.2 µm hole in the silicon requires a 1.0 µm mask hole.

To find the correct energy doses for the photolithography to pattern the silicon dioxide, a FEM is performed. The energy doses is varied over the x-axis of the wafer from 80 to 210 mJ/cm² by steps of 10 mJ/cm², the focus is kept constant. After the photolithography, the silicon dioxide is etched for 210 seconds, using recipe SIO01. Previous experiments have shown an endpoint detection (EPD) of this recipe after 180 sec for 700 nm of silicon dioxide. An additional ~20% over etch was used to compensate for etch rate variation over the wafer.

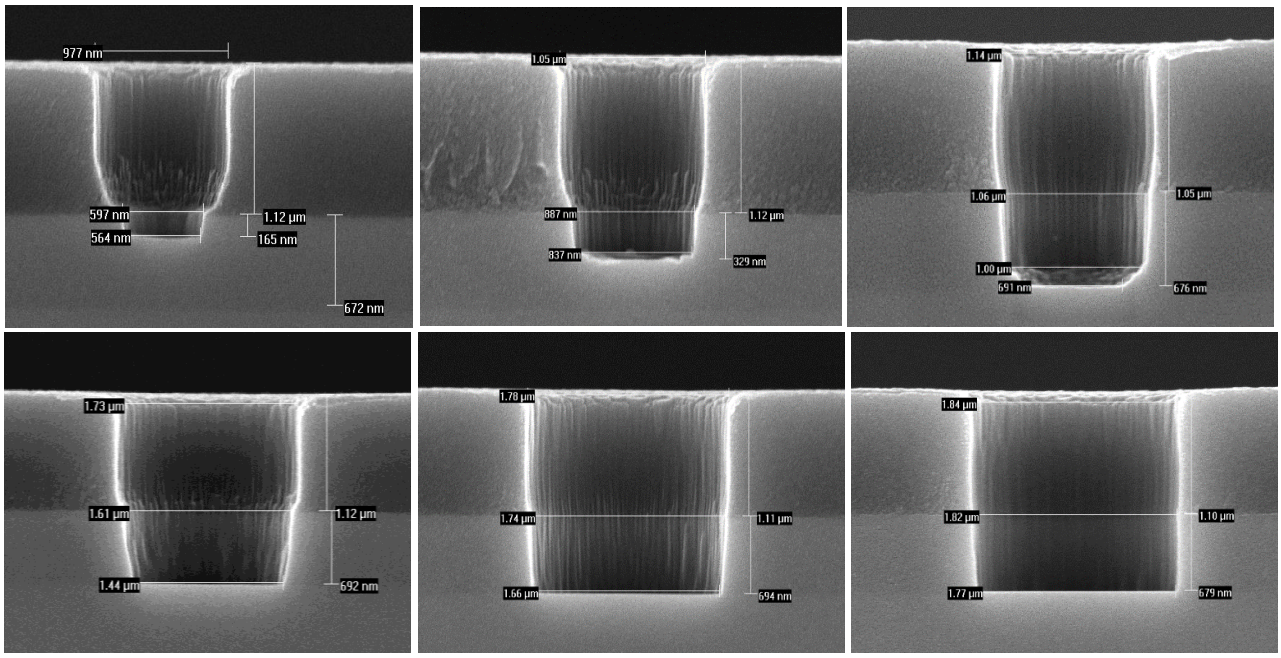


Figure 4.2. SEM image of the first test run for the oxide mask for exposure energies of 80 mJ/cm², 100 mJ/cm² and 140 mJ/cm² (left to right) and 0.8 µm and 0.9 µm holes (top to bottom).

The SEM images in Fig 4.2 show an increase in hole diameter with increasing energy dose, as expected. The 0.8 µm holes on the mask increase to 0.97 µm, 1.05 µm and 1.14 µm holes in the silicon dioxide by exposure energies of 80 mJ/cm², 100 mJ/cm² and 140 mJ/cm² respectively. The 1.5 µm holes increase to 1.73 µm, 1.78 µm and 1.84 µm. Energies above 140 mJ/cm² result in too much increase of the holes diameter in the silicon dioxide. Secondly, it is observed that the wall profile of the photoresist curves inwards at the photoresist – silicon dioxide interface. This is probably due to the interference of the incoming and reflected light waves during exposure. The nodes and antinodes of the waves add up which results in a waved surface of the wall profile and a ''foot'' at the place of reflection. Finally, it can be seen that the etch recipe SIO01 did not reach the bottom of the silicon dioxide layer in narrowest holes.

In a second run, the exposure energy range is narrowed to an energy range from 80 to 145 mJ/cm² by steps of 5 mJ/cm². A post-exposure-bake (PEB) is introduced to eliminate the foot. The PEB is used to induce the diffusion of the photogenerated compound in order to smooth out the interference effect on the resist profile. Furthermore, the etch time with recipe SIO01 is increased to 420 seconds.

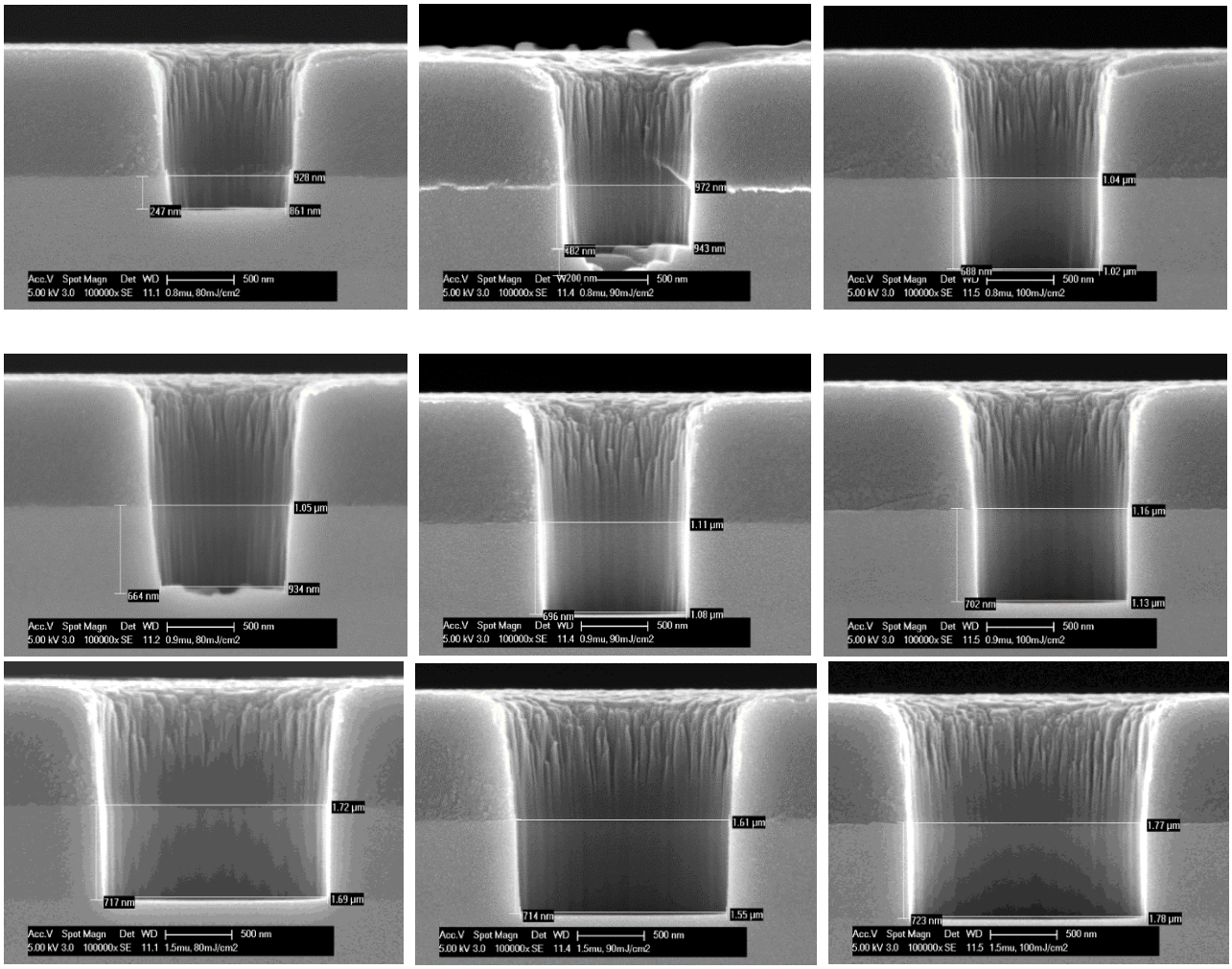


Figure 4.3. SEM image of the second test run for the oxide mask for exposure energies of 80 mJ/cm², 90 mJ/cm² and 100 mJ/cm² (left to right) and 0.8 µm, 0.9 µm and 1.5 µm holes (top to bottom).

The SEM images in Fig 4.3 show that the PEB eliminates the foot of the photoresist. Exposing with a dose of 100 mJ/cm² causes an increase in hole diameter of 0.2 µm. The 0.8 µm holes enlarge to 1 µm, which is the target of the photolithography optimization. In addition, the SIO01 recipe reaches the bottom of the silicon dioxide layer in the 1 µm holes after etching 420 seconds.

4.2.2 DRIE etch for HARM trenches

As mentioned in the introduction, proper control of the flow of species in the HARM trenches seems to be the bottleneck in the etch process. The small trench diameter hinders the in- and outflow of the ions and radicals and causes the species inside the trench to collide. The collisions of the different species cause some species to move in the horizontal direction and damages the trench walls. The main goal is to control the inflow and outflow of the species. The parameters that are adjusted during the experiments and their role in the process are listed in table 4.1

Chamber temperature	*Operation temperature during the etch process*
Etch pressure	*Pressure in the chamber during the etch cycle.*
Bias power	*The platen power during the complete etch cycle. This power determines the etch intensity of the etch phase in the etch cycle.*
Bias time	*Duration of the etch cycle, i.e. time that the bias power is tuned on.*
Bias delay	*The time between the end of the passivation cycle and the start of the etch cycle.*
Boost power	*Platen power during the boost phase. This power determines to the impact of the ion bombardment.*
Boost time	*Duration of the boost phase, i.e. time that the boost power is tuned on.*
Boost start	*The time between the end of the passivation cycle and the start of the boost phase.*
Deposition pressure	*Pressure in the chamber during the deposition of the passivating film in the passivation cycle.*
Deposition time	*Duration of the passivation cycle, i.e. time that the passivation is deposited on the etch target.*
Deposition start	*The time between the end of the etch cycle and the start of the passivation phase.*

Table 4.1, Parameters that are investigated in the development of the process and their meaning.

Etch split

As little information was known regarding the fabrication of HARM trenches, the first test recipe is designed based on educated guesses and results of comparable recipes. The results indicated the difficulty to transfer the mask pattern into the silicon. The DRIE process typically starts with an etch cycle. This first etch is anisotropic and results in under etch because there is no passivation layer deposited yet. The typical under etch is in the range of 100 nm to 300 nm, which is acceptable for most applications. However, for these micron size trenches, this is a significant increase. In order to transfer the silicon dioxide mask pattern, the etch recipe is split into two part. First, a start phase to transfer the pattern, followed by a main phase to fabricate the remainder of the trench, the phases are called ‘’start DRIE’’ and ‘’main DRIE’’, resp.

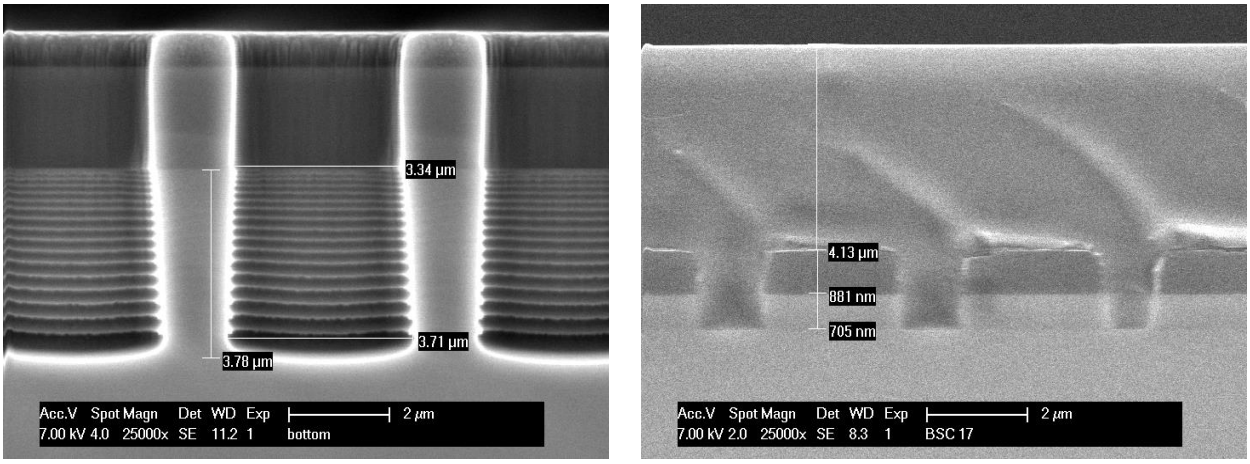
Start DRIE

The purpose of the start DRIE is to transfer the pattern from the silicon dioxide into the silicon. The collision of species is in the start DRIE not an issue because the aspect ratio of the trench is still small. The focus in the first etch cycles is on the sidewall protection to minimize the under etch.

First, the influence of gradually increasing the intensity of the etch cycle is investigated by ramping the bias power in 30 steps. The profile is evaluated by investigating cross-sections (Fig 4.4a). Only 20 scallops are identified, which suggest that during the first 10 etch cycles the bias power was insufficient to break through the passivation layer. In addition, the created scallops at the bottom of the trench are too large for the trench capacitors, which suggest that the bias power at the end of the process is too high. The bias power between the 10^{th} and 15^{th} etch cycle seems suitable for the start DRIE. This power is spread over 40 etch cycles to reduce

the size difference between subsequent scallops. Besides the ramp in the bias power, a ramped delay in the bias start is introduced, which will be discussed later.

To even further increase the accuracy of the pattern transfer, an increase in sidewall passivation by increasing the deposition time is reviewed. Although the time is increased by just a fraction of the total deposition time, the result is striking (Fig 4.4b). This adjustment result in the formation of the passivation layer of 1.4 µm on the whole wafer. Apparently, the amount of passivation that is deposited in this timespan is more than what could be removed in the boost phase. 550 cycles are involved in the total recipe, which means that approximately 7.5 nm passivation is deposited in every cycle. This approach is rejected.

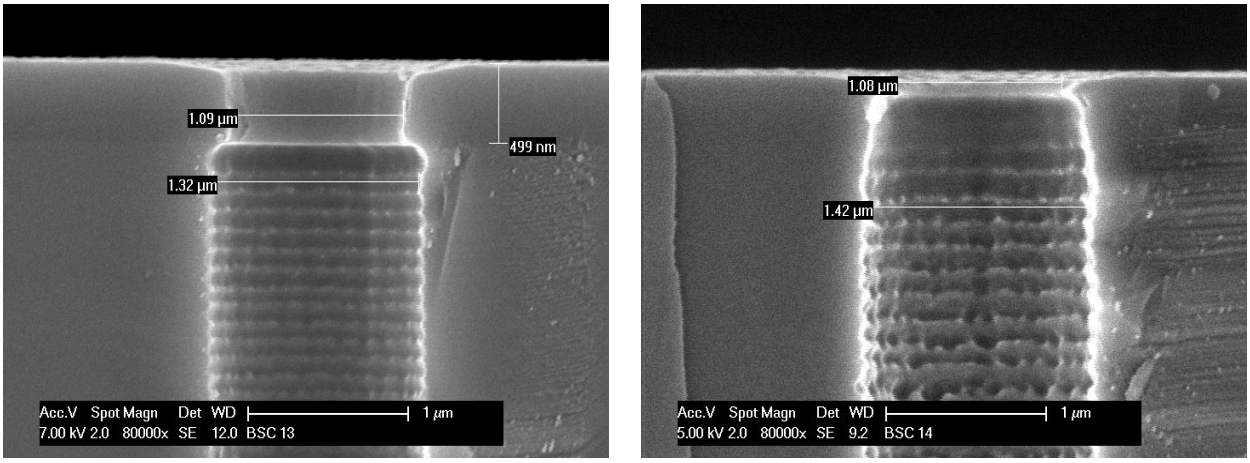


a) *b)*

Figure 4.4 SEM image of a cross-section showing a) the first start DRIE test run and b) result of an increase in deposition time.

Results and discussion

To evaluate the performance of the start DRIE, two wafers are etched with an existing recipe. One without the start DRIE (Fig 4.5a) and one with the start DRIE (Fig 4.5b). The figures show the difference in the profiles at the top of the trench. It must be noted that the test run for the recipe without start DRIE is stopped during the etch, which is also indicated by the thicker silicon dioxide layer. However, the prediction is that this does not affect the profile of the start DRIE.

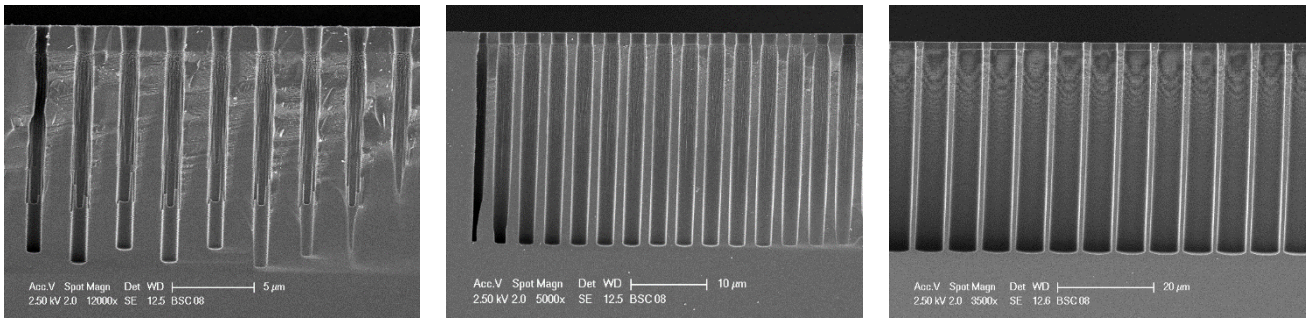


a) *b)*

Figure 4.5. SEM image of a cross-section of a) trench that is etched without start DRIE and b) trench that is etch with start DRIE.

Main DRIE

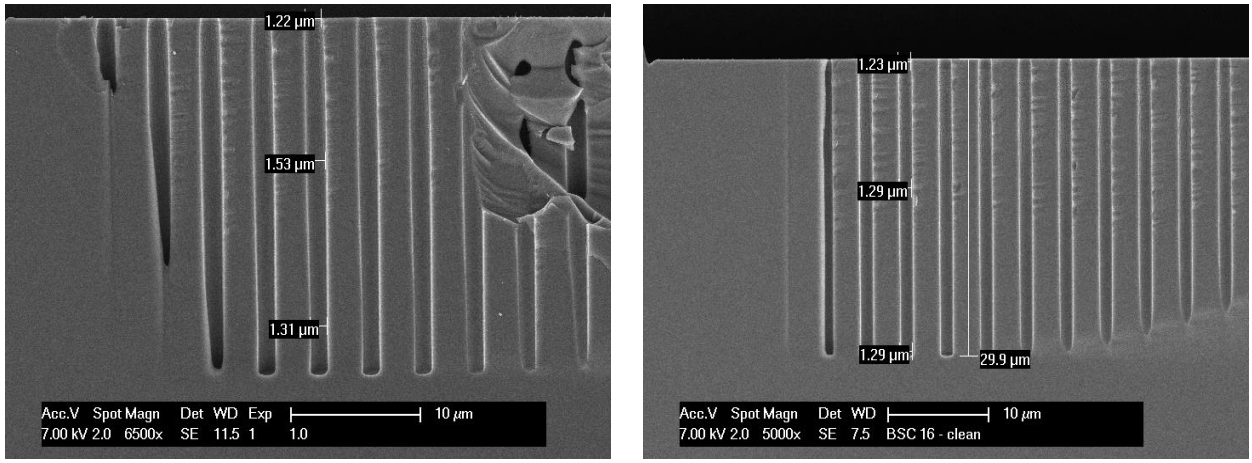
As mentioned in the introduction, the issue in the main DRIE is the control of the inflow and outflow of species in HARM trenches. This is illustrated by Fig 4.6, where the cross-sections of three trenches that were etched on the same wafer with the same recipe are shown. The wall profile in the 1.0 µm trenches (Fig 4.6a) show remarkable features that are not visible in the 1.4 µm and 1.6 µm trenches (Figs 4.6b and 4.6c). In addition, the depth of the 1.0 µm trench is drastically reduced and non-uniform.



a) *b)* *c)*

Figure 4.6 SEM image of cross-sections showing a) 1.0 µm trenches, b) 1.4 µm trenches and c) 1.6 trenches.

In contrast to the start DRIE, the etch intensity is not the issue in the main DRIE. Therefore, the bias power and boost power continue at a constant power from the last etch cycle of the start DRIE. In the main DRIE, the issue is related to the ability of the species to leave and enter trench. The result is unwanted etching in the horizontal direction. The unwanted etching is expressed in two effects. First, a belly half way the trench (Fig 4.7a) and secondly, an increase in surface roughness of the trench wall is noticed. The aim is to create an environment where the ions and radicals have enough space to freely enter and leave the trench. This is partly obtained by the introduction of a ramped increase in delay between the bias and boost steps. As the trench starts to increase in depth, the time between the deposition cycle and etch cycle is increased. This provides more time for species to enter and leave the trench. This delay is also applied to the start DRIE. The etch recipe is compared with the same recipe before the introduction of the ramped delay. Fig 4.7b shows that the belly is removed.

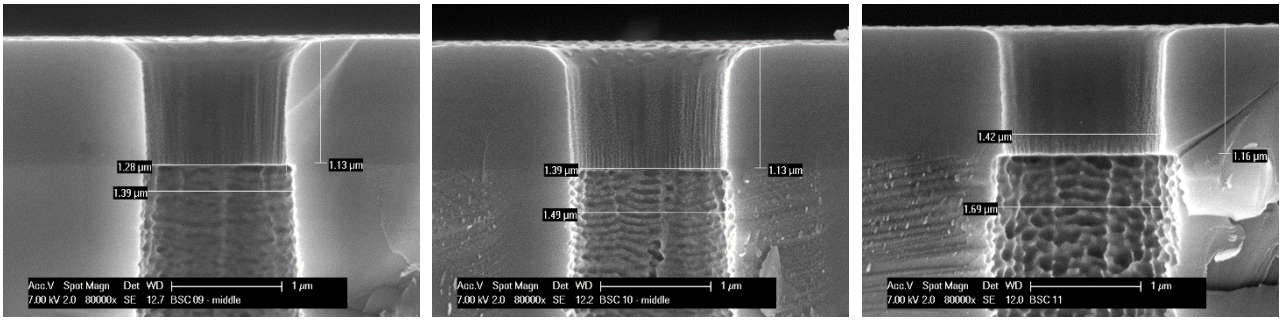


a) *b)*

Figure 4.7 SEM images to compare the etch recipe a) without a ramped delay in the bias and boost start and b) with a ramped delay in the bias and boost start.

The horizontal etching has an effect on the roughness of the trench wall as well. To mitigate this problem, the thickness of the passivation layer is increased. First, the deposition pressure is investigated. However, it was

found that no improvement can be made here. Both a decrease as well as an increase in passivation pressure introduced more surface roughness (Fig 4.8).



a) *b)* *c)*

Figure 4.8 SEM images to compare the etch recipe a) with deposition pressure b) with increased deposition pressure and c) with decreased deposition pressure.

Next, the operation temperature was reviewed. The prediction is that evaporation of the passivating film will reduce with decreasing temperature. Two wafers are etched with the same recipe but with different operation temperatures. Experiments have shown the prediction is correct (Fig 4.9). The result was even beyond the expectations, since the under etch is significantly reduced as well.

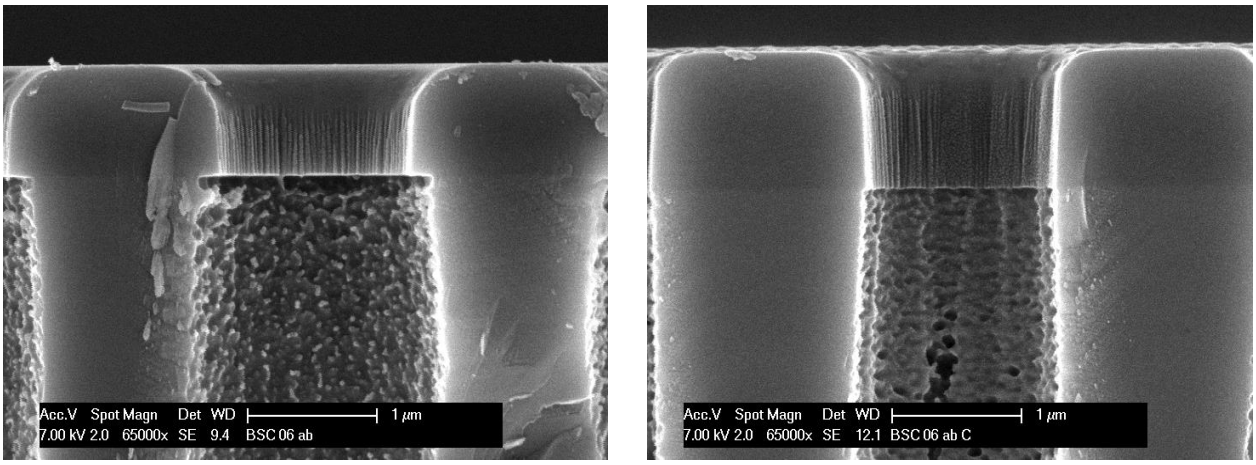


Figure 4.9 SEM images that show a comparison of an etch recipe at a) normal temperature and b) a low temperature

Result an discussion

In a final step, the start DRIE and main DRIE are combined and the recipe's length is adjusted to obtain a trench depth of 30 µm. After fabrication of the trenches, a thin passivation layer remains on the trench walls that needs to be removed. In this experiment, the passivation layer is removed in an oxygen plasma for 45 min at 130 °C in the barrel. However, it would be interesting to investigate if a 5 min descum in the Trymax at 250°C is sufficient to remove the scum. For the integration in the F2R flow, this process step is preferred for the shorter process time. The final result of the trench etch process optimization is shown in Fig 4.10. The opening and the depth of the trench are measured 1.2±0.1 µm and 30±0.1 µm, resp. A detailed overview of the trench is presented in section D.1. In the top part of the trench is still some surface roughness present. Compared to previous results, the roughness is considerably reduced and the prediction is that the thermal oxidation step for the first dielectric layer will further flatten the wall profile. As expected, the etch recipe heavily erodes the photoresist and the silicon dioxide mask. The photoresist is completely removed and only 80±10 nm silicon

dioxide is left. If this recipe needs to be used for even deeper structures, it is advisable to use a thicker silicon dioxide masking layer.

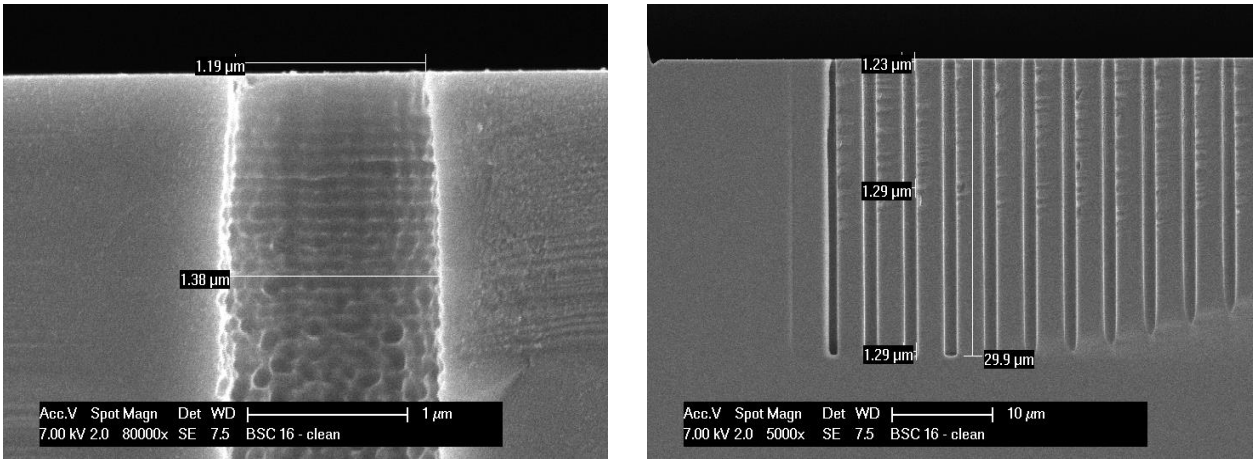


Figure 4.10. SEM image of the trench that is etched with recipe BSC16

4.2.3 Conclusion

A new etch recipe is designed for the fabrication of 1.2 µm wide HARM trenches with a straight wall profile. The surface roughness of the trench wall is minimized to improve the uniformity of the dielectric coverage. The recipe can be found under the name BSC 16 in the PInS cleanroom.

4.3 Dielectric deposition and patterning

The performance of a capacitor is largely determined by the quality of the dielectric. Poor dielectric layers that contain impurities or defects are more prone to an early dielectric breakdown. The impurities and defects are strongly related to the deposition processes of the dielectric layers. This section first describes the formation of silicon dioxide using dry oxidation. Next, the patterning of the silicon dioxide – silicon nitride – silicon dioxide (ONO) layers for the fabrication of the low and high voltage capacitors is reviewed.

Dry oxidation of silicon

The oxidation rate of silicon in a dry oxidation process[6] is related to the process temperature, the silicon's impurity concentration and crystal orientation. For a fixed impurity concentration, the crystal orientation dependency decreases with a temperature increases, while the oxidation rate increases (Fig 4.11).

[6] B.5 Oxidation

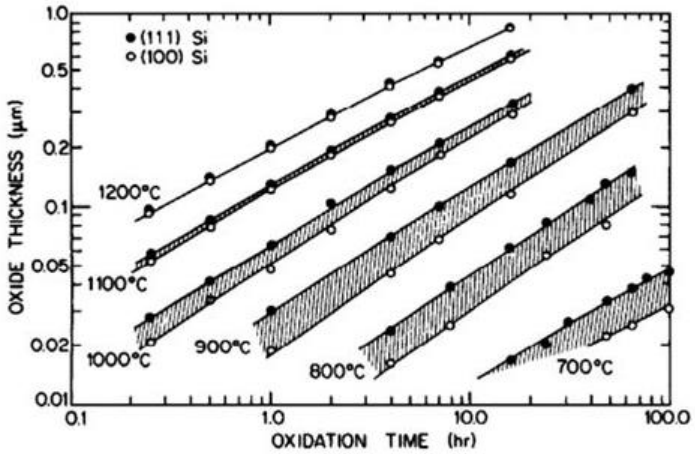
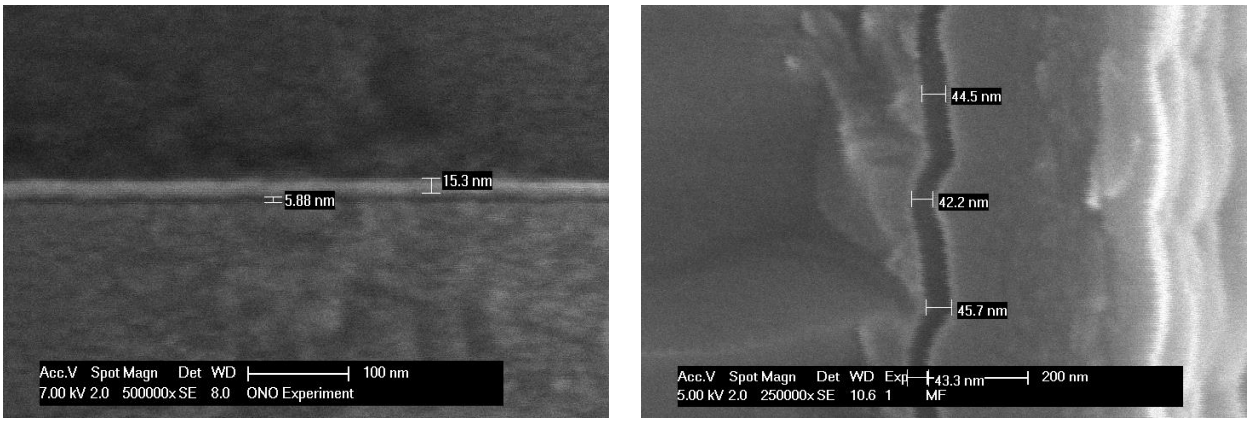


Figure 4.11. Silicon dioxide thickness as a function of the reaction time for two crystal orientations in a dry oxidation process [23].

To control the formation of a thin layer silicon dioxide in the range of 5 nm, low oxidation temperatures are preferred. However, due to the topography of the trenches and the roughness of the trench walls, the oxidation of the silicon happens in different crystal orientations. For a uniform silicon dioxide layer inside the trench a high temperature is preferred. To investigate the best deposition temperature, test wafers that contain highly scalloped trenches are oxidized at different temperatures and the uniformity and thickness of the layers is reviewed by the scanning electron microscope (SEM). Furthermore, the grow rate of the silicon dioxide on a lightly doped test wafer is compared with the grow rate on a highly doped n-type silicon wafer.

Result and discussion

It is found that at 850°C the dry oxidation process can be controlled to from thin silicon dioxide layers (Fig 4.12). A slight variation in the uniformity of the layer is measured between the valley and the peak of a scallop (Fig 4.12b). This could be assigned to the difference in crystal orientation. However, the trenches in the capacitors have a more flat wall profile and the expectation is that this will sufficiently decrease the influence of the crystal orientation to obtain a uniform layer. Therefore, a the dry oxidation at 850°C was selected to control the thickness of the silicon dioxide. A 10% difference in oxidation rate is found between the lightly doped test wafer and highly doped n-type wafer.

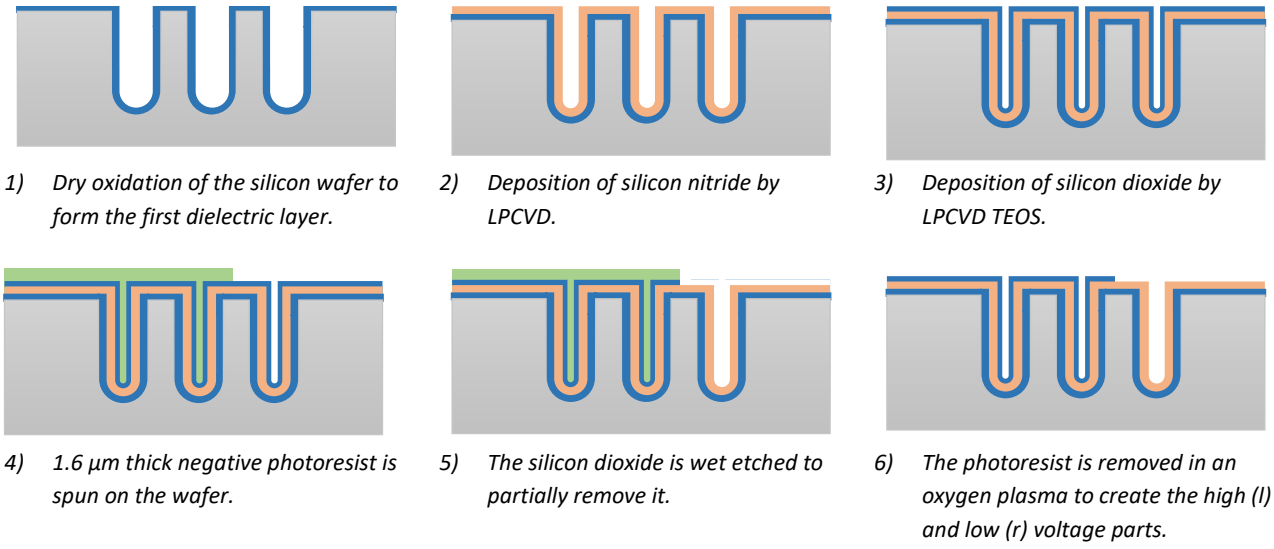


a) *b)*

Figure 4.12. SEM images showing a) the thickness of a thin layer silicon dioxide (5.88 nm) after dry oxidation at 850°C on an n-type doped wafer and b) the uniformity of the silicon dioxide layer inside a scalloped trench after dry oxidation at 850°C on a test wafer.

Fabrication of high and low voltage dielectric

After the dry oxidation, the low and high voltage dielectric parts are fabricated. First, the silicon nitride and silicon dioxide layers are deposited by LPCVD nitride and LPCVD TEOS, resp. These are established processes in the cleanroom that did not require special attention. After deposition of the silicon nitride and silicon dioxide, the latter is removed for the creation of a low voltage part in the dielectric (Fig 4.13).



1) *Dry oxidation of the silicon wafer to form the first dielectric layer.*
2) *Deposition of silicon nitride by LPCVD.*
3) *Deposition of silicon dioxide by LPCVD TEOS.*
4) *1.6 µm thick negative photoresist is spun on the wafer.*
5) *The silicon dioxide is wet etched to partially remove it.*
6) *The photoresist is removed in an oxygen plasma to create the high (l) and low (r) voltage parts.*

Figure 4.13. Fabrication of the low and high voltage part in the dielectric layer.

To pattern the top silicon dioxide layer, a negative photoresist is spin coated onto the wafer. Because it is difficult to illuminate a positive photoresist to the bottom of the trench in order to be able to expose and develop it[2], a negative photoresist is used. For this photoresist the unexposed resist will be removed during developing. The negative photoresist is ma-N1410. After patterning, the silicon dioxide is etched in BOE7:1. According to the layer thickness the etch time is determined.

To verify the process, 6 nm silicon dioxide is grown in 25 µm deep trenches, followed by the deposition of 10 nm silicon nitride and 30 nm silicon dioxide. Next, The photoresist is spin coated onto the wafer and patterned using the TRC_ONO mask. In the last step, the silicon dioxide is removed in BOE7:1 for 10 seconds. Next, the wafer is covered with HPR504 and a cross-section is made. The side of the cross-section is etched in BOE7:1 to create a step height between the different layers. The difference in height provides a better contrast to identify the layers during the SEM inspection.

The SEM images show the high voltage and low voltage dielectric (Fig 4.14). However, the high voltage dielectric is not preserved over the whole area of the wafer where the negative photoresist was applied.

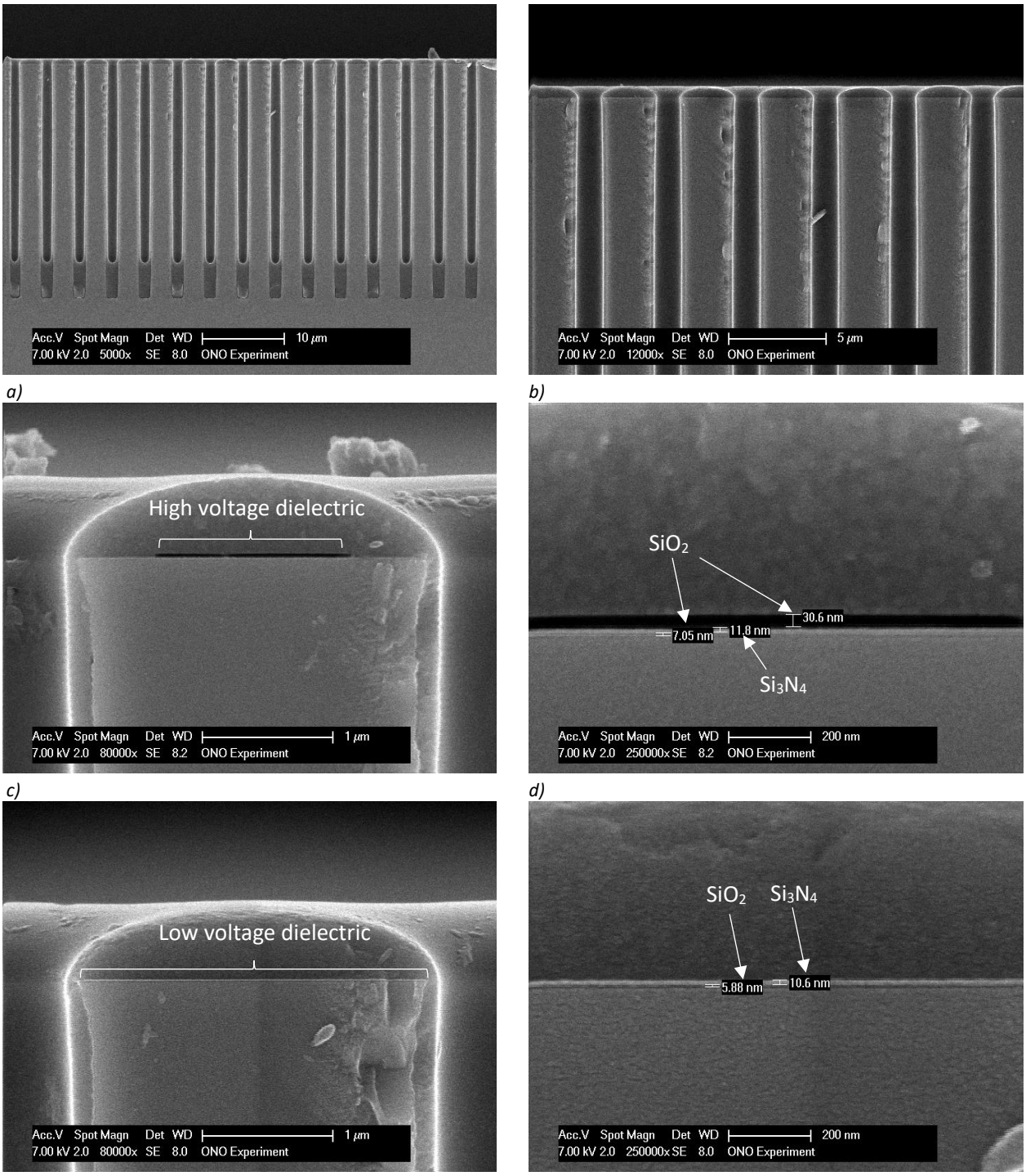
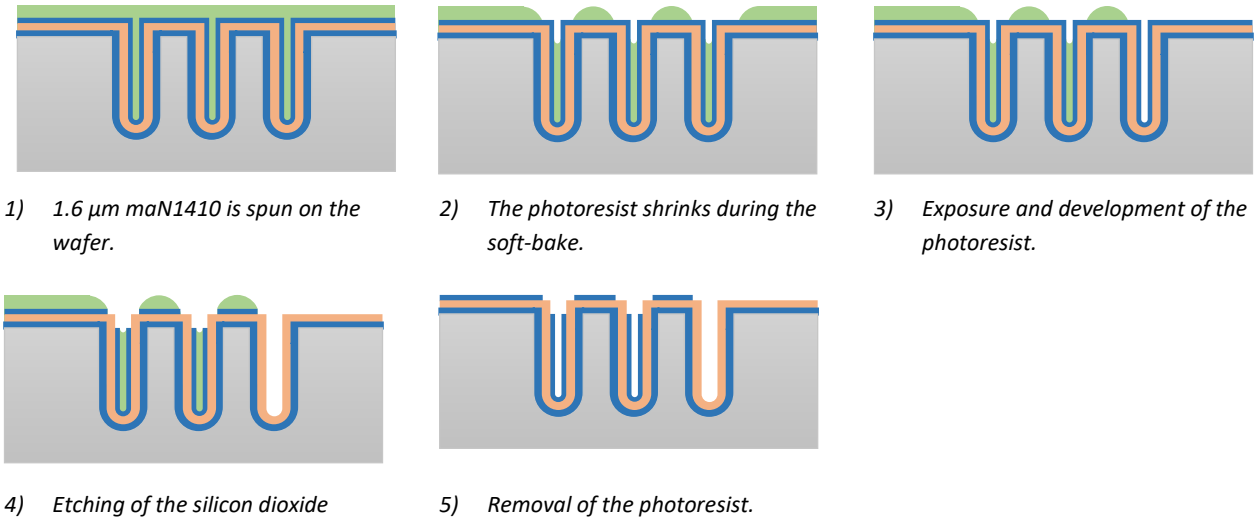


Figure 4.14. SEM image of a) cross-section overview of the trenches, b) the top part of six trenches, c) the top surface area between two trenches where the high voltage dielectric is partly preserved, d) a close-up of the high voltage dielectric, e) the top surface area between two trenches where the top dielectric layer is removed to create the low voltage dielectyric and f) a close-up of the low voltage dielectric.

It is very likely that the negative photoresist contains too much solvent for this application. The solvent evaporates during the soft-bake. A relative high percentage of solvent causes a significant reduction in the photoresist volume after this soft bake (Fig 4.15). Due to the high volume of the trenches, the shrinking of the photoresist causes insufficient coverage of the top part of the trench and in these areas the silicon

dioxide is removed. It must be noted that only 0.6 µm of the 25 µm deep trench is exposed, which is just under 2.5% (Fig 4.16).



1) *1.6 µm maN1410 is spun on the wafer.*
2) *The photoresist shrinks during the soft-bake.*
3) *Exposure and development of the photoresist.*
4) *Etching of the silicon dioxide*
5) *Removal of the photoresist.*

Figure 4.15. Illustration of the reduction in photoresist volume after the soft-bake.

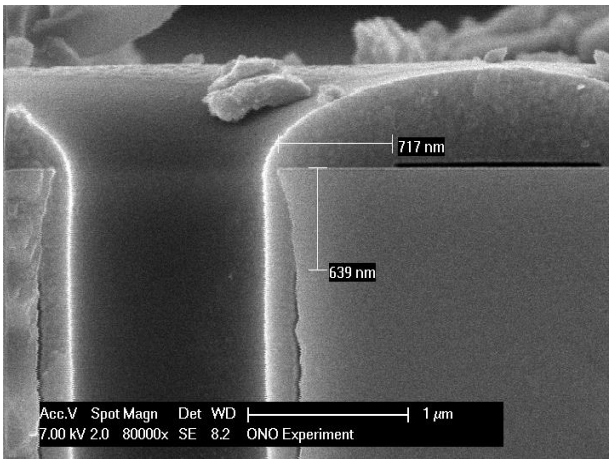


Figure 4.16. SEM images of the top part of the trench that indicates the area where the high voltage dielectric is lost.

Result and discussion

This experiment shows the viability of the low and high voltage part in one dielectric. However, the current processing in combination with a 25 µm deep trench is not suitable. To further investigate this process option, it is suggested to repeat the experiment with a thicker layer of negative photoresist. A second possibility is to adjust the depth of the trench according to the required capacitance requirements to reduce unnecessarily volume that need be filled with photoresist.

4.4 Fabrication of the polycrystalline silicon top electrode

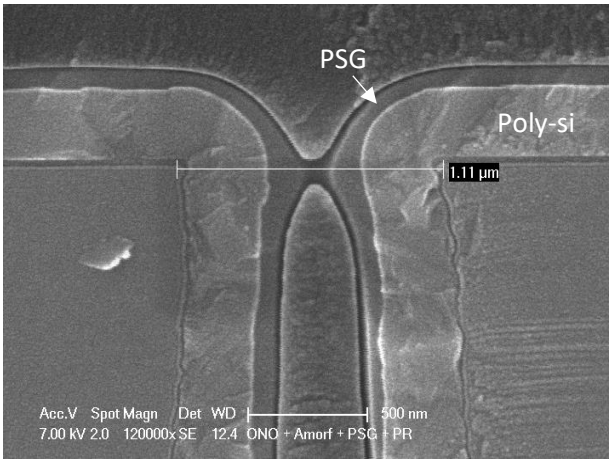
The previous section addresses the dielectric layer that is used for the fabrication of the capacitors. This section elaborates on the top electrode. For the trench capacitors, a highly doped silicon wafer is used to function as the bottom electrode. For the top electrode, a metal electrode would be ideal because of its high conductance.

However, due to the non-conformal deposition of metals in high aspect ratio structures this is not feasable. Therefore, the use of a highly doped Poly-Si layer as the top electrode is investigated. By increasing the impurity concentration in the Poly-Si, it behaves more or less like a metal. To dope the Poly-Si, first a layer of amorphous silicon is deposited using LPCVD. The low pressure in LPCVD ensure that the reactant diffuses deep inside trenches for a good step coverage of the layer. Next, the PSG is deposited as solid dopant source, followed by a heat anneal to migrate the dopant atoms from the PSG into the Poly-Si.

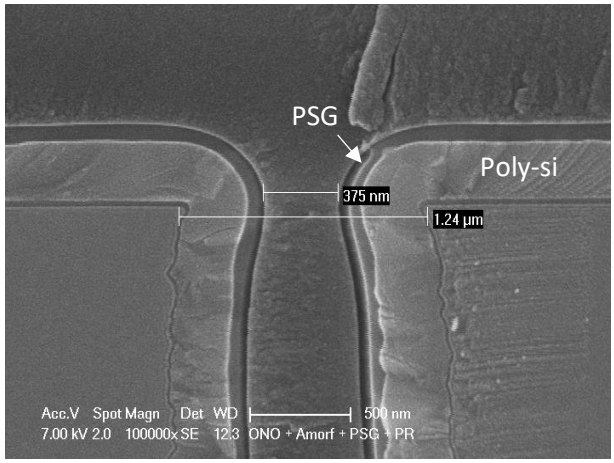
One of the objectives of this experiment is to verify the uniform coverage of the trench walls by the Poly-Si and the coverage of the Poly-Si by the PSG. Good coverage of the layers is necessarily to obtain the required electrical properties down to the bottom of the trench. A cross-section sample of the wafer with a dielectric, the Poly-Si and the PSG was inspected. On the wafer, trenches varying from 1.1 µm to 1.8 µm are fabricated. The depth of the trenches varies from 20 µm to 32 µm. The second objective of this experiment is to evaluate the electric properties of the Poly-Si after doping.

Result and discussion

The SEM images in Figs 4.17a and 4.17b show the coverage of the Poly-Si and PSG in a 1.1 µm and a 1.2 µm trench. It is observed that the PSG start to close the trench for a diameter of 1.1 µm, in addition the layer thickness inside the trench is thinner compared to layer ticknesses in wider trenches. Figs 4.17c and 4.17d show the coverage of the Poly-si and PSG outside the trench and in the bottom of a trench. Good step coverage is observed in both locations. Although the PSG thickness was thinner in the 1.1 µm trenches, the measurements during the electrical characterization did not indicate an abnormale behaviour of the the Poly-Si. Therefore it can be concluded that ~70nm PSG is sufficient to dope 300nm Poly-Si.



a)



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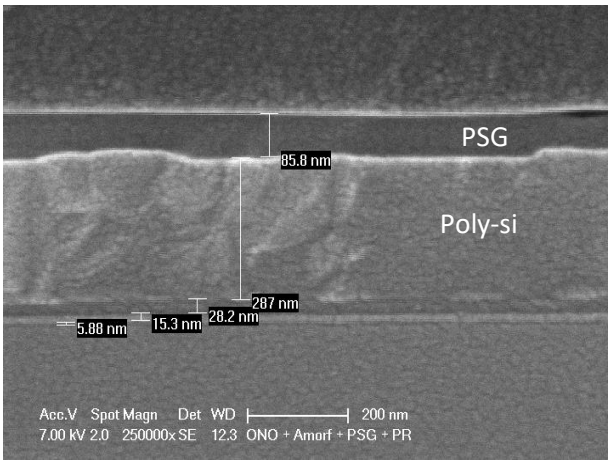
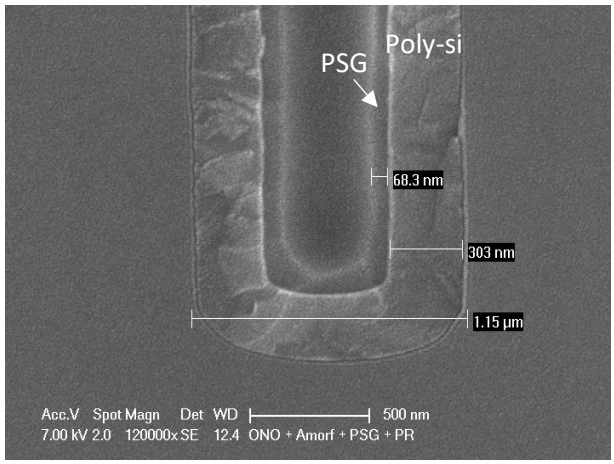




c) *d)*

Figure 4.17 SEM images of the Poly-Si and PSG layer in a) a 1.1 µm trench, b) a 1.2 µm trench, c) outside the trench and d) at the bottom of a 20 µm deep trench.

The resistivity of the Poly-Si is measured at different location on the wafer. A resistivity of 1.1±0.2 mΩ·cm is measured, which corresponds to a dopant concentration of $2 \cdot 10^{20}$ cm^{-3}. This is not far from the in literature reported resistivity plateau of 0.4 mΩ·cm for dopant concentrations higher than $6 \cdot 10^{20}$ cm^{-3}[27], [29]. Moreover, during the electrical characterization a nearly perfect ohmic contact was observed between the aluminum coper and the Poly-Si, which confirms the low resistivity and metallic behavior of the Poly-Si.

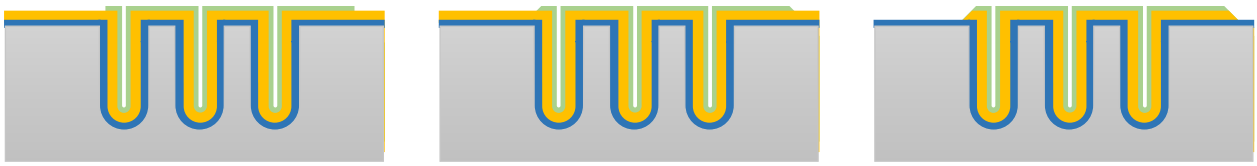
Conclusion

It is demonstrated that a good top electrode can be fabricated from a 300 nm thick layer Poly-Si that is doped from a 70 nm thick layer PSG. Furthermore, a minimum trench width for the deposition of 300 nm Poly-Si and 80 nm PSG is determined at 1.2 µm. It is observed that the PSG starts to close the trench opening in the fabrication process, which reduce the coverage of PSG. Although the PSG is slightly thinner, the result does not seem to suffer from it. However, for reliability reasons, it is recommended to fabricate a trench with a minimum diameter of 1.2 µm.

4.5 Photoresist reflow to improve silicon dioxide coverage

The largest part of this report discusses the fabrication of the trench capacitors. However, the ultimate goal is to integrate the trench capacitors as a ''building block'' into the F2R platform. Therefore, some design considerations are investigated that are required for this integration. The most important requirements is that the trenches are closed before the etching of the buried trenches. This will be discussed in the next section. A second topic is the step coverage of the silicon dioxide that will be deposited in the F2R flow over the Poly-Si of the trench capacitors. After the fabrication of the trench capacitors on the silicon islands in F2R, 700 nm very low stress silicon dioxide is deposited and patterned using photolithography. For a good flow of the photoresist over the wafer, the step transition from the Poly-Si to the silicon substrate is smoothed.

To smoothen the transition, a slope is created in the edge of the Poly-Si. This is established by introducing a bake step after development of the photoresist (Fig 4.18). The influence of the temperature of this bake to the slope is experimentally reviewed by preparing three wafers with Poly-Si and patterning them with 1.3 µm HPR504. One wafer is not baked, one wafer is baked at 125°C for two minutes and the third wafer is baked at 150°C for two minutes. After baking, the silicon dioxide is etched using an etch recipe with a normally straight etch profile to transfer the pattern and the slope into the Poly-Si.



a) *1.3 µm HPR504 is spun on the wafer and patterned.*

b) *The photoresist is baked on a hot plate for 2 min to create a slope.*

c) *The poly silicon is etched and the slope is transferred to the Poly-Si.*

Figure 4.18. Illustration of the transfer of the slope from the photoresist into the Poly-Si.

Result and discussion

It is found that the not baked photoresist result in a straight edge, the bake at 125°C in a 45° slope and the photoresist that is baked at 150°C in a 23° slope. Since the 45° slope occupies les space and this slope is most likely sufficient to provide a good flow of the photoresist, this process is transferred to a production wafer to pattern the Poly-Si. The SEM images in Fig 4.19 show the result of the post exposure bake and the coverage of the silicon dioxide over the Poly-Si. The same slope of ~45° is obtained at the edge of the Poly-Si. A next step would be to investigate the flow of the photoresist and check at what distance from the edge of the Poly-Si the photoresist is flat enough to pattern it with high accuracy.

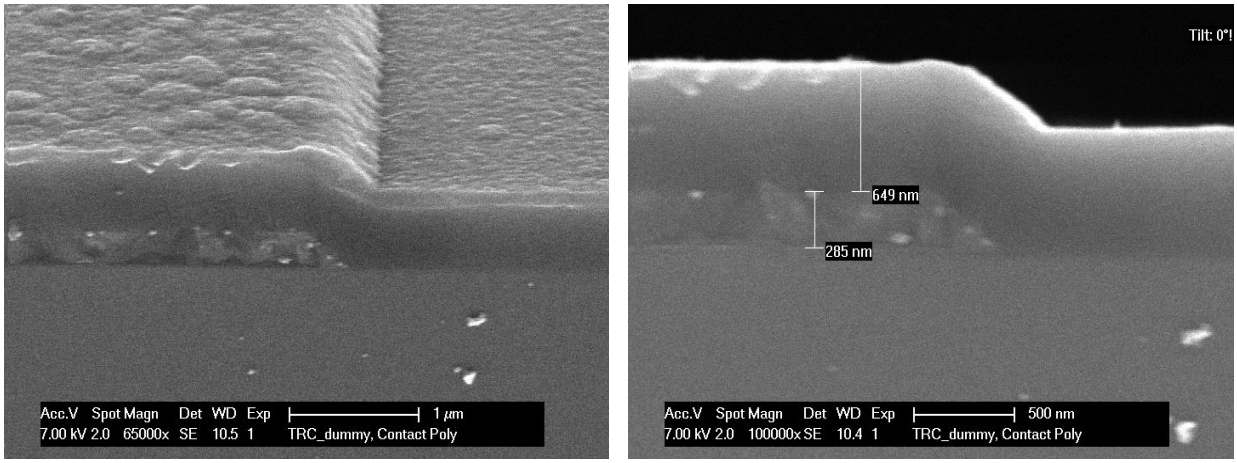


Figure 4.19 SEM images of the slope in the 285 µm thick Poly-Si and the coverage of the 649 µm thick silicon dioxide.

Conclusion

It is shown that the reflow of the photoresist creates a slope in the Poly-Si and that the coverage of the silicon dioxide over the Poly-Si is uniform.

4.6 Silicon dioxide deposition for trench closing

For the integration of the trench capacitors in the F2R platform, it is critical that the capacitor trenches are closed before the buried trenches are etched. In the DRIE process to etch the buried trenches, a 700 nm thick layer of very low stress silicon dioxide is used as a hard mask. This silicon dioxide layer is deposited by PECVD. The non-conformal step coverage of PECVD in the high aspect ratio capacitor trenches results in a thin silicon dioxide layer deep inside the trench [30]. The poor coverage of the silicon dioxide is insufficient to protect the capacitors during the dry etch for the buried trenches. Therefore, other solutions must be found to protect the trenches during the fabrication of the buried trenches.

One possible solution is to use the 700 nm thick very low stress silicon dioxide layer to close the trenches. Literature shows that PECVD silicon dioxide tends to build up at the edges of bulging structures[31]. When a hole or via is small enough, this characteristic can be used to close the structure (Fig 4.20).

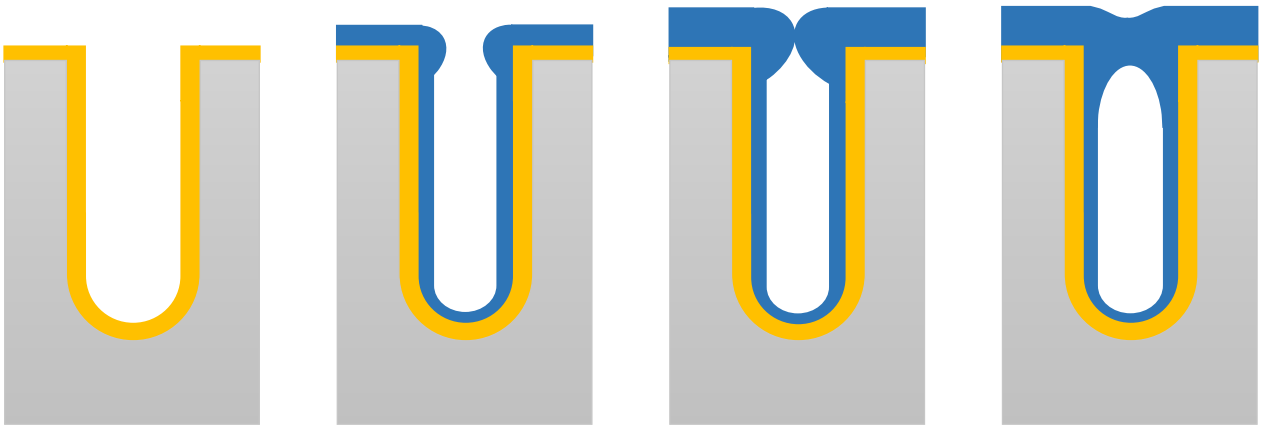


Figure 4.20, Closing of the trench by PECVD of silicon dioxide.

To investigate the possibility to close the trenches with the 700 nm thick layer of very low stress silicon dioxide used in the F2R flow, a test wafer is patterned with trenches and the dielectric layer and top electrode are deposited on the test wafer as explained in chapter 3, followed by the deposition of 700 nm very low stress silicon dioxide. After deposition, cross-section samples are investigated using a SEM.

Result and discussion

First, the diameters of the trenches, after removing the PSG, were inspected. It was found that the openings to close in the 0.8 µm and 0.9 µm trenches (dimensions refer to the mask holes) are 320±10 nm and 550±10 nm, resp. Fig 4.21 shows the SEM image after the deposition of the 700 nm thick layer of very low stress silicon dioxide layer used to close the trench openings. The pictures show that this layer does not close the 0.8 µm and 0.9 µm trenches completely.

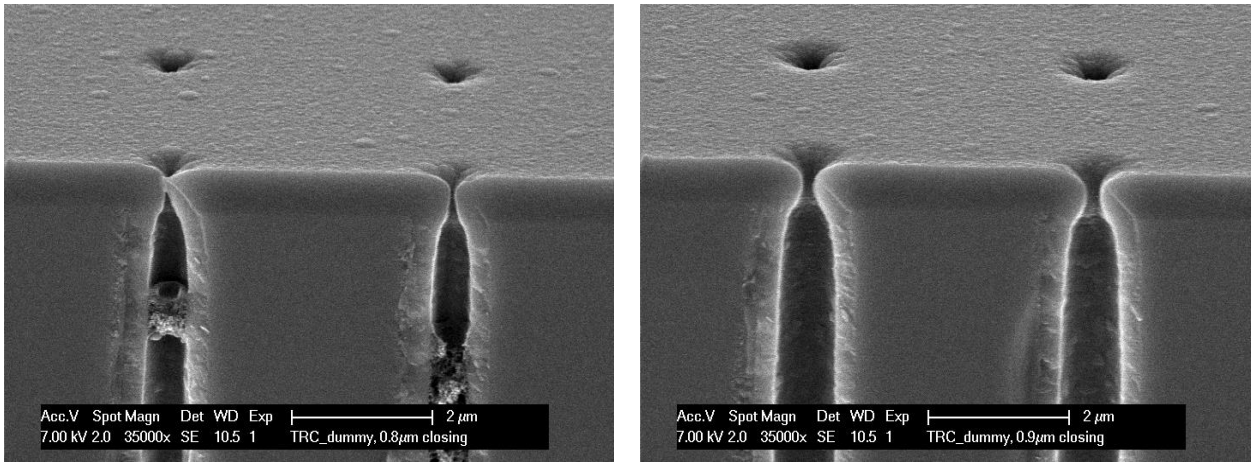


Figure 4.21, SEM cross-section images of the silicon dioxide deposition onto the a) 1.0 µm trench and b) 1.2 µm trench.

Conclusion

It is shown that the approach to close the trenches with the silicon dioxide mask to pattern the buried trenches is not feasible.

5. Characterization

5.1 Introduction

After the fabrication of the trench capacitors, their electrical behavior is evaluated. This Chapter describes the electrical characterization of the capacitors. First, the quality of the dielectric layers is studied by measuring the leakage current and breakdown voltage. Next, the quality of the dielectric is investigated by means of its capacitance. The capacitance behavior is measured for different frequencies and areas. Finally, the increase in capacitance density by applying trenches to the capacitors is evaluated.

In this work, two kind of dielectric layers are used for the capacitors. A single layer silicon dioxide dielectric and an ONO multilayer dielectric (Chapter 2). The individual thicknesses of the layers were verified using the Nanospec II and by scanning electron microscopy (SEM) cross-sections. The single layer dielectric measured to be 33±2 nm. For the multilayer dielectric, the Silicon dioxide measured 7±2 nm for the bottom and 30±2 nm for the top layer. The Silicon nitride measured 15±2 nm. No major defects in the dielectrics were found throughout the trench (Fig 5.1).

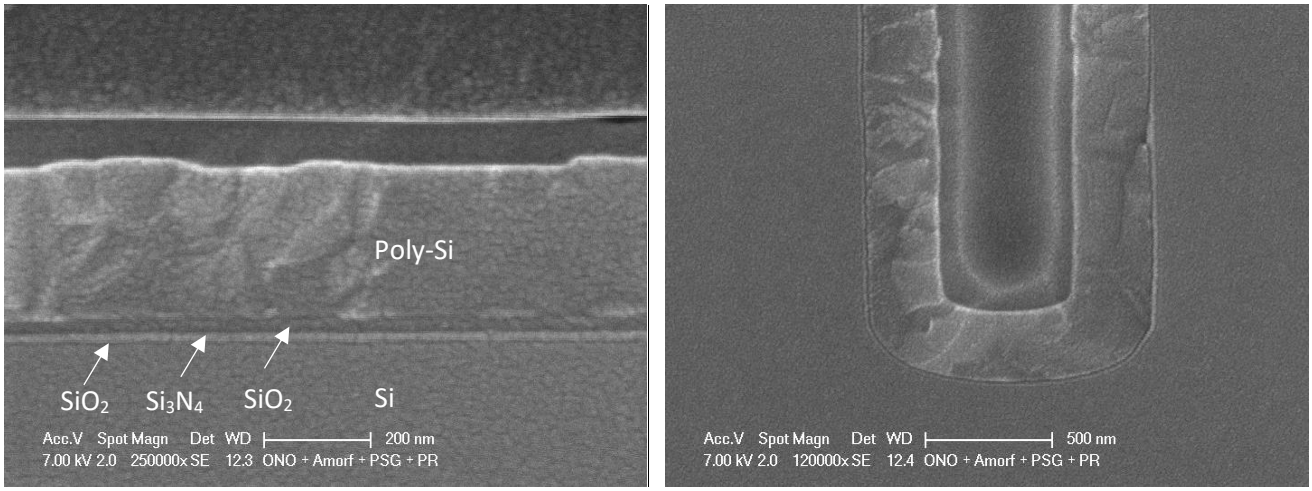


Table 5.1, SEM cross-section of the ONO capacitor. a) Top of the capacitor showing the Si and Poly-si bottom and top electrode and the three layers corresponding to the SiO_2 – Si_3N_4 – SiO_2 dielectric. b) Bottom of the trench, which indicates good step coverage of the layers throughout the whole trench.

The measurements for both dielectrics are performed on the CAP100, CAP300 and CAP1000 test devices as described in section 3.3.2. Table 5.1 lists the different capacitor variations that are used for the measurements.

Name	*Dielectric*	*Area (mm2)*	*Circumference (mm)*
CAP100-O	*33 nm silicon dioxide*	*0.03*	*0.7*
CAP300-O	*33 nm silicon dioxide*	*0.11*	*1.2*
CAP1000-O	*33 nm silicon dioxide*	*1.04*	*4.3*
CAP100-ONO	*7-15-30 nm O-N-O*	*0.03*	*0.7*
CAP300-ONO	*7-15-30 nm O-N-O*	*0.11*	*1.2*
CAP1000-ONO	*7-15-30 nm O-N-O*	*1.04*	*4.3*

Table 5.1, Description of the names that are used to indicate the measurement graphs.

5.2 Measurement set up

The measurements are executed using a four-point needle probe system and the KEITHLEY 4200-SCS semiconductor characterization system. It should be noted that the measurement set up has an open structure. Because it is not shielded from the environment, it is possible that the measurements can be influenced by noise from the surrounding. Especially high frequency measurements and measurements that are performed on large area structures are more likely to pike up noise.

First, the intrinsic breakdown is characterized. The intrinsic breakdown mechanism is a rather complex mechanism and full characterization is beyond the scope of this report. However, to get an impression of the intrinsic or best-case performance, measurements were performed on the CAP100-O and CAP100-ONO devices. The relatively small area reduce the change of defects in the dielectric. Typical areas to measure these properties would be in the region of 0.01 mm^2[19], which comes close to the area of the CAP100 design. However, an inherent trade-off is the increase in the edge-to-area ratio, which could alter the characterization. Secondly, the extrinsic related breakdown is studied. Extrinsic properties can be related to the design and processing, examples can be defects due to irregularities in the dielectric or at the dielectric – electrode interface. The measurements to investigate the influence of extrinsic defects are generally performed on three scaled area capacitors, a typical large area would be in the order of 0.1 to 1 mm^2 [19]. The difference between CAP100, CAP300 and CAP1000 is in the range of an order of magnitude and the CAP1000 correspond to the required large area size. Therefore, the characterization to study the influence of extrinsic properties is performed on these test devices.

Before the measurements were started, the expected values are calculated. Based on the layer thicknesses of the dielectrics the expected breakdown voltage of the single layer dielectric is ~33 V and of the multilayer dielectric ~42 V. Due to a mask misalignment in the fabrication process, the number of trenches in the capacitors is different from the mask specifications. The CAP1000 contains 67512 trenches, the CAP300 5529 and no trenches were fabricated in the CAP100 devices. Furthermore, due to the DRIE etch process, the diameter of the trenches is not equal to the mask hole diameter. Detailed information regarding the geometry of the trenches and functional area can be found in the appendix section E. Based on the geometry of the trenches, the expected capacitance density (per footprint area) is calculated. For fair comparison is the amount of capacitance due to the contact pads extracted from the total capacitance. Because no trenches were etched in the CAP100 devices, the expected capacitance density for these capacitors is 1.13 nF/mm^2 for all devices. The expected values for the CAP300 and CAP1000 are presented in table 5.2 and 5.3.

Mask hole (µm)	*Capacitance density CAP300-O (nF/mm^2)*	*Capacitance density CAP1000-O (nF/mm^2)*	*Increase factor*
No hole	*1.13*	*1.13*	*1*
0.8	*4.7*	*5.9*	*5.1*
0.9	*7.1*	*9.1*	*7.9*
1.0	*9.7*	*12.4*	*10.8*
1.1	*9.8*	*12.7*	*10.9*
1.2	*11.0*	*14.3*	*12.4*
1.3	*11.8*	*15.3*	*13.3*
1.4	*12.6*	*16.3*	*14.1*
1.5	*13.3*	*17.3*	*15.0*
1.6	*14.1*	*18.4*	*15.9*

Table 5.2. Expected capacitance density for the CAP300-O and CAP1000-O devices.

Mask hole (µm)	*Capacitance density CAP300-ONO (nF/mm^2)*	*Increase factor*	*Capacitance density CAP1000-ONO (nF/mm^2)*	*Increase factor*
No hole	*1.9*	*1*	*1.9*	*1*
0.8	*7.7*	*4.0*	*9.7*	*5.0*
0.9	*11.8*	*6.1*	*15.1*	*7.8*
1.0	*15.1*	*8.3*	*20.5*	*10.7*
1.1	*16.2*	*8.4*	*20.9*	*10.9*
1.2	*18.2*	*9.4*	*23.5*	*12.2*
1.3	*19.4*	*10.1*	*25.2*	*13.1*
1.4	*20.7*	*10.7*	*26.9*	*14.0*
1.5	*21.9*	*11.4*	*28.5*	*14.8*
1.6	*23.25*	*12.1*	*30.1*	*17.1*

Table 5.3. Expected capacitance density for the CAP300-ONO and CAP1000-ONO devices.

5.3 Sheet resistance and contact resistance characterization

The sheet resistance of the aluminum and Poly-Si are measured on the van der Pauw structures. A current of 4.53 mA is applied over two adjacent contacts and the voltage is measured over the two remaining contacts. According to equation 3.1, the value of the measured voltage is equal to the sheet resistance. The resistivity of the material is found by multiplying the sheet resistance with the thickness of the measured layer. The measured resistivity of the aluminum is 2.9 mΩ·cm, which is comparable to values reported in literature[32]. The resistivity of Poly-Si is 1.1 mΩ·cm. As mentioned in chapter 4, this is close to the minimum resistivity that can be obtained in Poly-Si.

The contact resistance is measured on the Kelvin test devices.

Waardes liggen nog op Philips, maandag toevoegen, Contact tussen Al – Substrate zeer hoog!

5.4 I-V Characteristics

To study the leakage current performance of the two dielectric layers, an experiment on the leakage current density dependencies on the voltage (I-V) is performed. To measure the leakage current, a voltage is applied over the capacitors and increased from zero to 50 V, while the current is measured with an accuracy of 100 pA. For fair comparison, the measured current is normalized to the surface area of the test device in order to obtain the current density. The current density is plotted on a logarithmic scale versus the applied voltage. First, the difference in leakage current of the CAP100-O and CAP100-ONO is measured on test devices without trenches, so called flat devices. Secondly, the leakage current dependency on the surface area of the flat devices is investigated by measuring the Cap100, Cap300 and Cap1000. Finally, the influence of trenches on the leakage current is studied. These measurements are performed on the CAP300 devices.

5.4.1 Comparison between a single layer and multilayer dielectric plate capacitor.

The measured leakage current density for the CAP100-O and CAP100-ONO is plotted versus the applied voltage (Fig 5.2). For Cap100-O, the current density remains almost constant between 5 V and 18 V and then increases

from 3.9 nA to 18 mA, followed by a sharp increase to 0.35 mA at 34.5 V. The current density for the CAP100-ONO increases slowly from 0.9 nA to 29 nA between 5 V to 26.5 V, followed by a more rapid increase to 350 mA at 46.5 V. From Fig 5.2, it can be seen that the dielectric breakdown occurs at 34.5 V and 46.5 V for CAP100-O and CAP100-ONO, respectively.

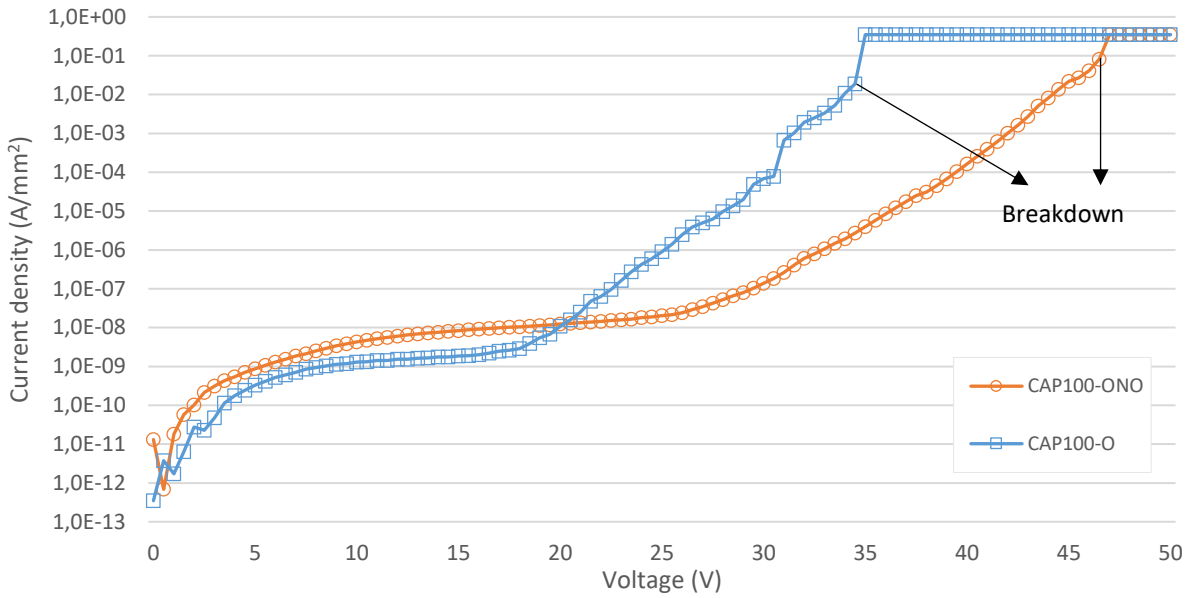


Fig 5.2, Dependency of leakage current density on the voltage for CAP100-O and CAP100-ONO.

Compared to the expected 33 V and 42 V breakdown voltages for the single layer and multilayer dielectric devices, the measured values are slightly higher. Reasons for the deviation could be due to, 1) the assumptions that are made in the calculations, 2) deviation of the layer thicknesses or 3) introduction of noise in the measurement set up. However, for this work it is sufficient to confirm that the measured breakdown voltage is in the range of the expectations.

5.4.2 Extrinsic properties of a single layer and a multilayer dielectric plate capacitor

To evaluate the extrinsic properties of the silicon dioxide dielectric layer, the current density is plotted versus the voltage for the CAP100-O, CAP300-O and CAP1000-O (Fig 5.3). The I-V curve can be divided in two regions. In the first region, up to 18V, the CAP100-O and CAP300-O show a stable leakage current density around 1 nA/mm^2 and 0.1 nA/mm^2 resp. The leakage current density of the CAP1000-O shows fluctuations between 1 and 10 nA/mm^2. In the second part, the three curves show a similar behavior. From Fig 5.3 it is observed that the dielectric breakdown occurs at 34.5 V, 33.5 V and 32 V.

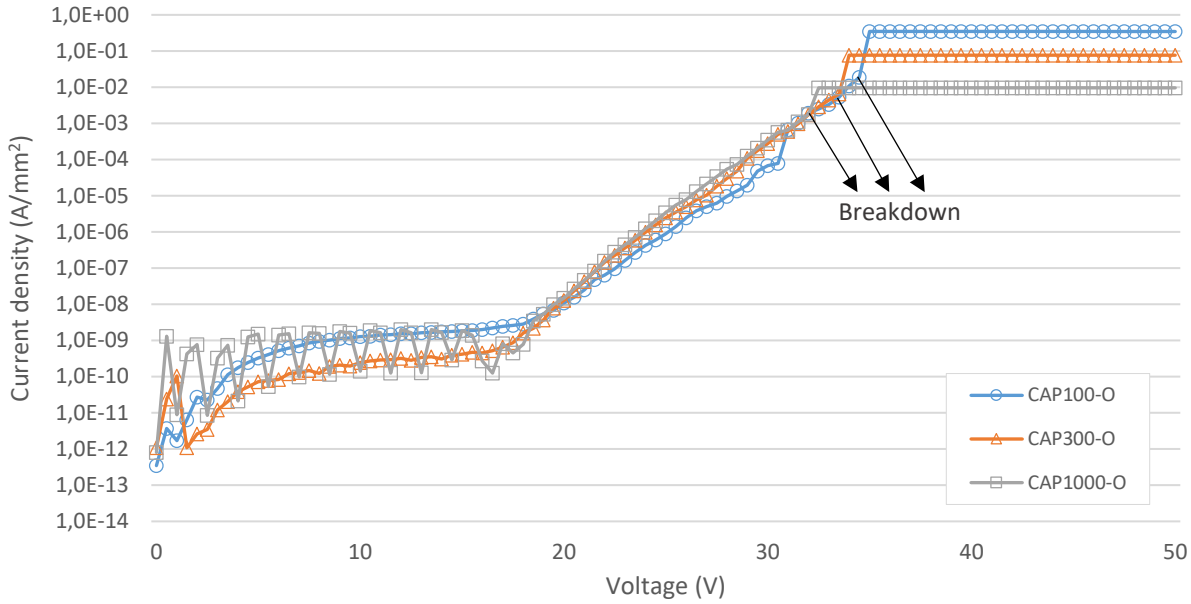


Fig 5.3 Dependency of leakage current on the voltage for CAP100-O, CAP300-O and CAP1000-O.

The same measurement is performed on the ONO dielectric layer. The current density is plotted versus the voltage for the CAP100-ONO, CAP300-ONO and CAP1000-ONO (Fig 5.4). The I-V curve can be divided in two regions. In the first region, up to 26.5 V, the CAP100-ONO and CAP300-ONO show a stable leakage current density of around 10 nA/mm^2 and 1 nA/mm^2, resp. The leakage current density of the CAP1000-ONO shows fluctuations around 1 nA/mm^2. In the second part, the three curves show a similar increasing behavior. The dielectric breakdown occurs at 47 V, 42 V and 37.5 V for the CAP100-ONO, CAP300-ONO and CAP1000-ONO, respectively.

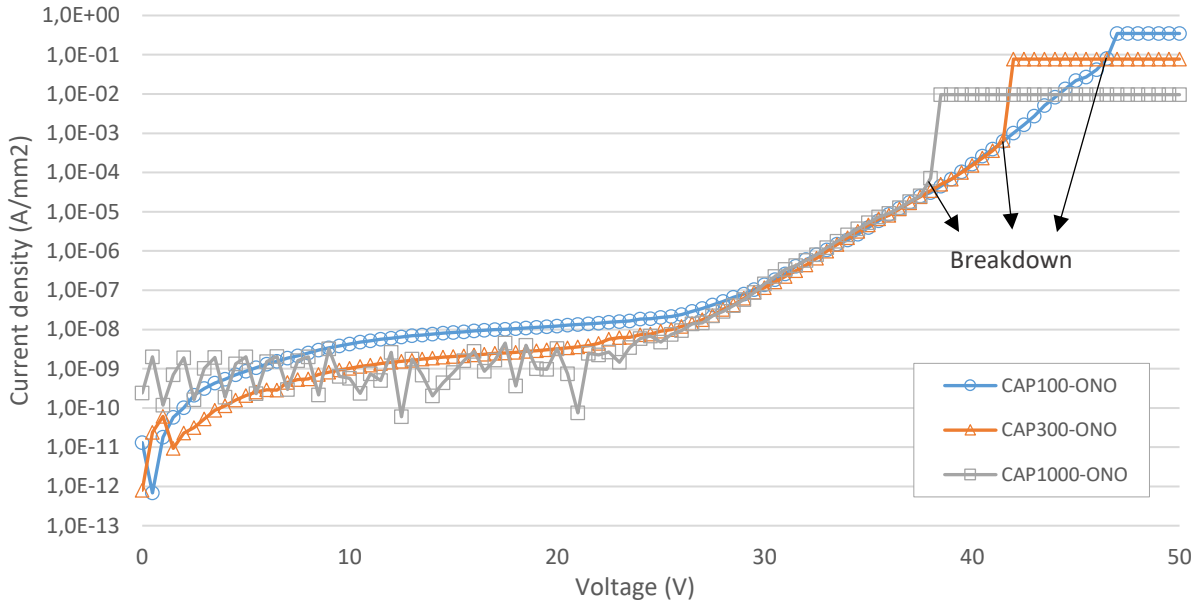


Fig 5.4, Dependency of leakage current on the voltage for Cap100-ONO, Cap300-ONO and Cap1000-ONO.

Result and discussion

Dielectric breakdown occurs at the weakest spot in the dielectric layer. The likelihood of imperfections in the dielectric layer increases when the area of the capacitor is increased. Therefore, it is expected that for both the single layer as well as the multilayer dielectric the breakdown voltage will decrease with increasing capacitor area. Furthermore, the higher leakage current at low voltages of the CAP100 compared to the CAP300 can be attributed to fringing fields at the edge of the capacitor [x]. Due to the difference in edge-to-area ratio, the effect of this field is larger in the CAP100. Finally, the fluctuation in the leakage current density at low voltages for the CAP1000 device is probably due to the accuracy of the measurement set up in combination with the large area of the structure.

5.4.3. Influence of the introduction of trenches.

To study the influence of trenches on the leakage current density, the current density is plotted versus the voltage for CAP300-O and CAP300-ONO with varying trench sizes (Fig 5.5). The introduction of trenches to the CAP300-O causes the current density to increase from ~1 nA/mm^2 to ~1 mA/mm^2 from 9 V to 25 V, followed by a dielectric breakdown in the range of 20 V to 25 V.

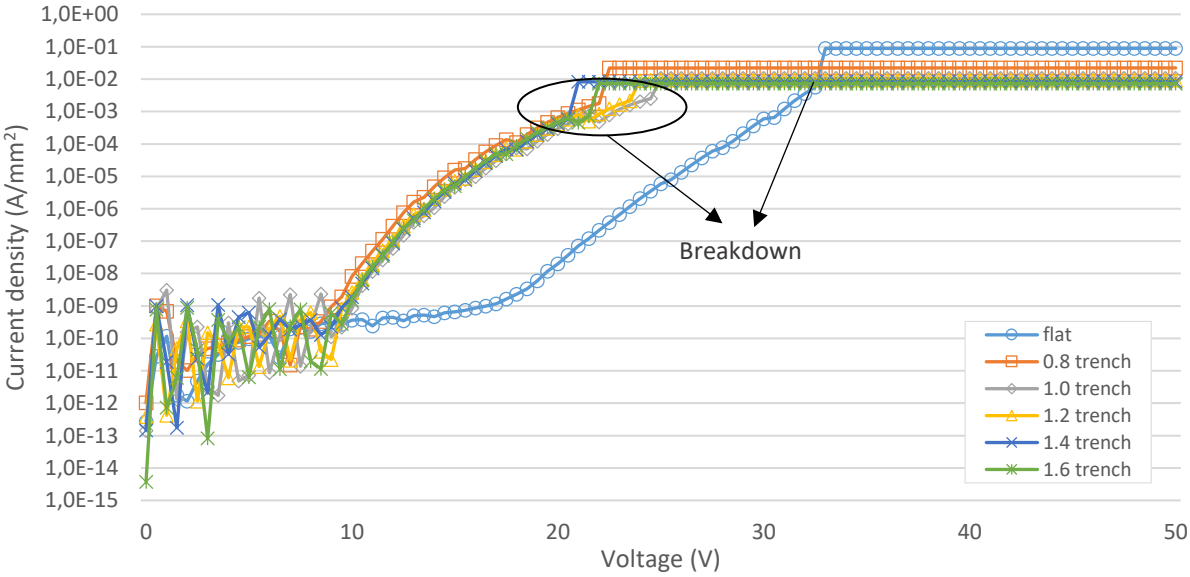


Fig 5.5, Dependency of leakage current density on the voltage for Cap300-O with varying trench diameter.

For the CAP300-ONO with added trenches up to 1.2 µm, the current density increases from 10 nA/mm^2 to 10 mA/mm^2 between 20 V to 35 V, followed by a dielectric breakdown around 35 V (Fig 5.6). The CAP300-ONO with trenches larger than 1.2 µm show the same behavior up to 36 V. However, the breakdown of these test device could not be measured due to the maximal current compliance of the measurement equipment.

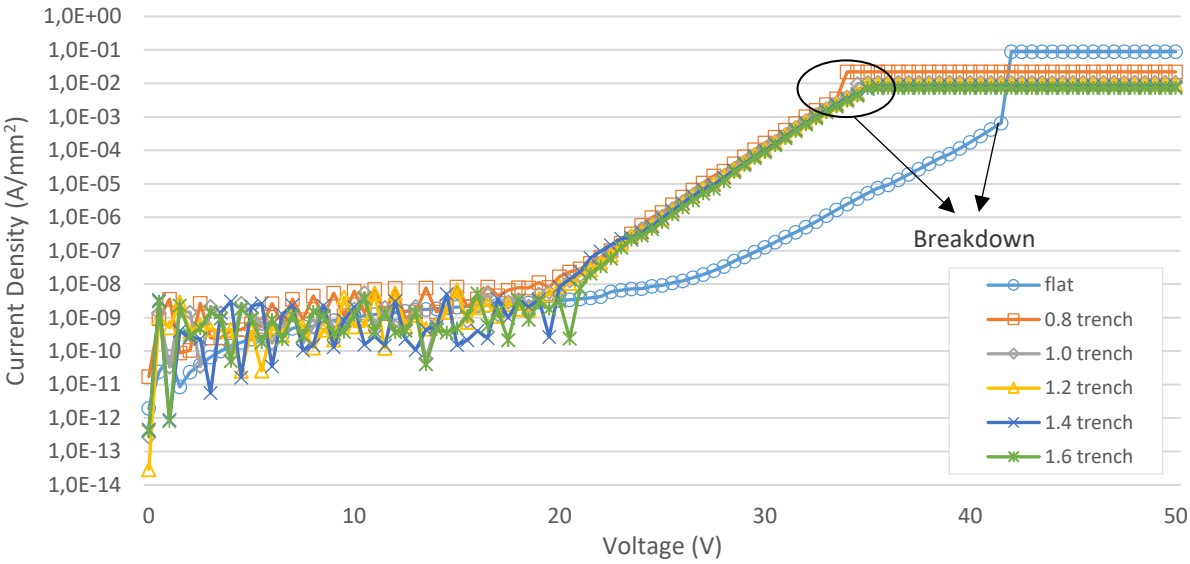


Fig 5.6, Dependency of leakage current density on the voltage for Cap300-ONO with varying trench diameter.

Results and discussion

The difference in leakage current behavior and point of breakdown in Figs 5.5 and 5.6 is in agreement with previous publications [33], [34]. Due to the area increase, topography of the trenches and roughness of the trench walls, the dielectric is more prone to impurities and imperfections that can cause the leakage current to increase and dielectric breakdown to occur. Moreover, the figures show a slight increase in leakage current density by applying 0.8 µm trenches compared to the other trenches. SEM cross-sections have shown that the roughness of the sidewalls in the 0.8 µm trenches is higher compared to the larger trenches due to the DRIE process. Therefore, the higher leakage current is expected.

The breakdown voltage in the single layer dielectric is decreased from 34.5 V to ~22 V, which is a reduction of 36%. For the multilayer dielectric the breakdown voltage is reduced by 25% from 46.5 V to 35 V. These results indicate that the topography of the trenches has less effect on the quality of multilayer dielectric compared to the single layer dielectric.

Furthermore, remarkable is the difference in the shape of the graphs where the current density start to increase more rapidly. This difference can be explained by the different conduction mechanisms in silicon dioxide and silicon nitride. In silicon dioxide the conduction mechanism is dominated by the Fowler –Nordheim tunneling. In silicon nitride the conduction is characterized by the Poole-Frenkel emission [35].

5.5 C-V Characteristic

To study the performance of the dielectric layers in terms of capacitance, first the capacitance is plotted for different frequencies to get an impression of the capacitance behavior over different frequencies. Next, the influence of the area increase to the capacitance density is studied. The first two measurements are performed on the flat capacitors. Finally, the effect of applying trenches to the capacitance and the capacitance density is investigated.

5.5.1 Capacitance for different frequencies for a single layer and multilayer dielectric plate capacitor

To study the behavior of the test devices over different frequencies, the capacitance is plotted versus the voltage for different frequencies. The first measurements indicated a strong frequency dependency of the test devices (Appendix Figs E.1 and E.2). Most likely is this frequency dependency is caused by the high contact resistance between the aluminum contact pads and the silicon substrate. To eliminate the influence of this contact resistance, the measurements are performed on two capacitors in series (Fig 5.7). The capacitance of one individual test device is than twice the measured capacitance of two identical capacitors (equation 2.13).

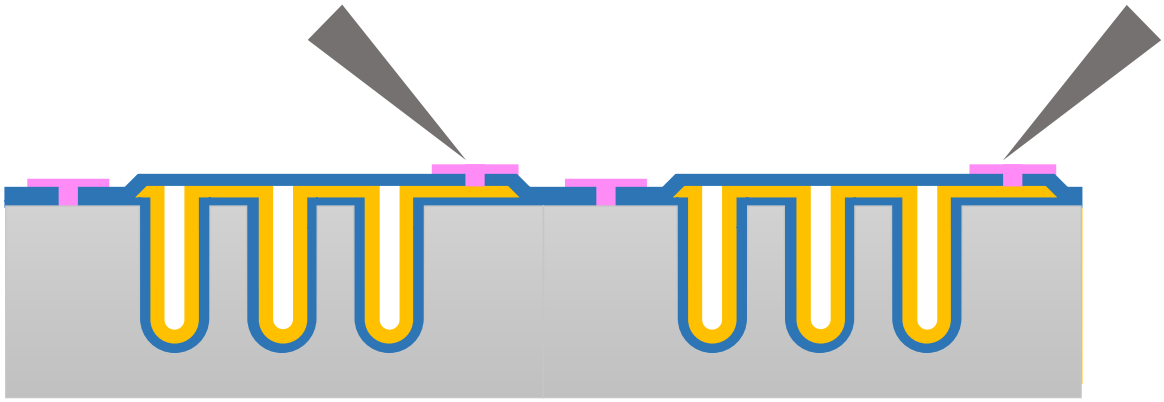


Fig 5.7. Illustration of the probing situation during the characterization.

Fig 5.8 and Fig 5.9 show the plots for the capacitance versus the voltage for CAP100-O and CAP100-ONO at different frequencies. It is observed that the capacitance remains nearly constant for both test vehicles at 10 kHZ, 100 kHz and 1 MHz, which indicates the capacitor's stability under a continuously increasing voltage stress. However, it was found that both capacitors exhibit a drastic increase in capacitance when measured at 10 MHz. In addition, the response to 1 kHz fluctuates heavily (appendix Fig E.3 and E.4). The measured data at 10 MHz are effected by limitations of the measurement setup, which is not designed for high frequency measurements. The fluctuations in the low frequency response are a result of the very high impedance of these small capacitors at 1 kHz. Because the response between 10 kHz and 1 MHz is stable, the measurements for further characterization are performed in this frequency range.

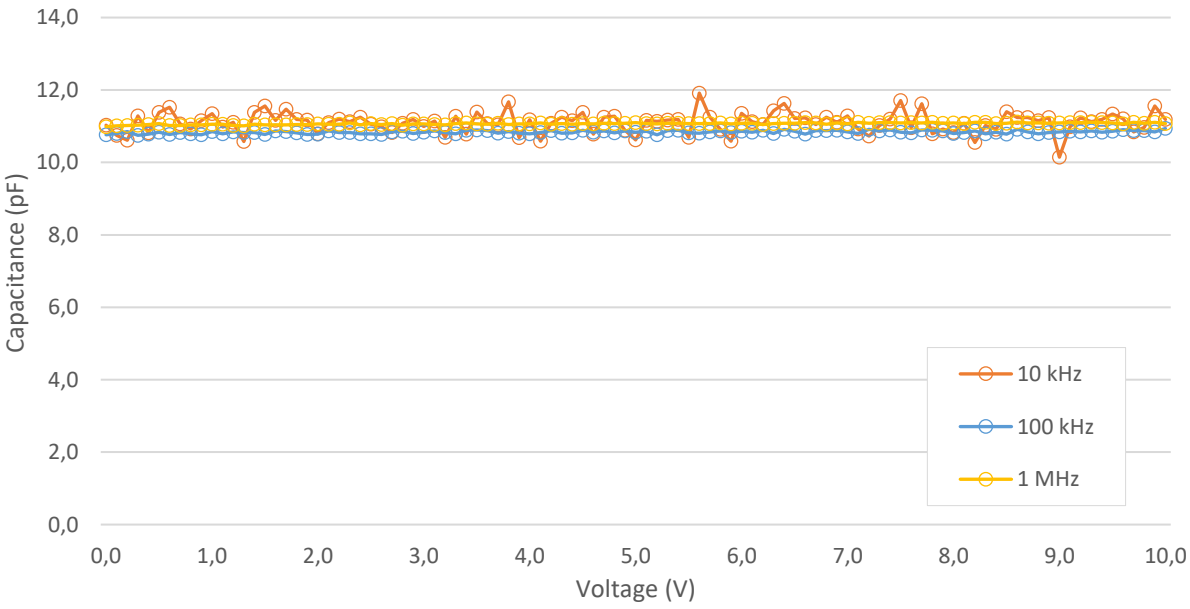


Fig 5.8, Dependency of capacitance on the voltage for CAP100-O at different frequencies

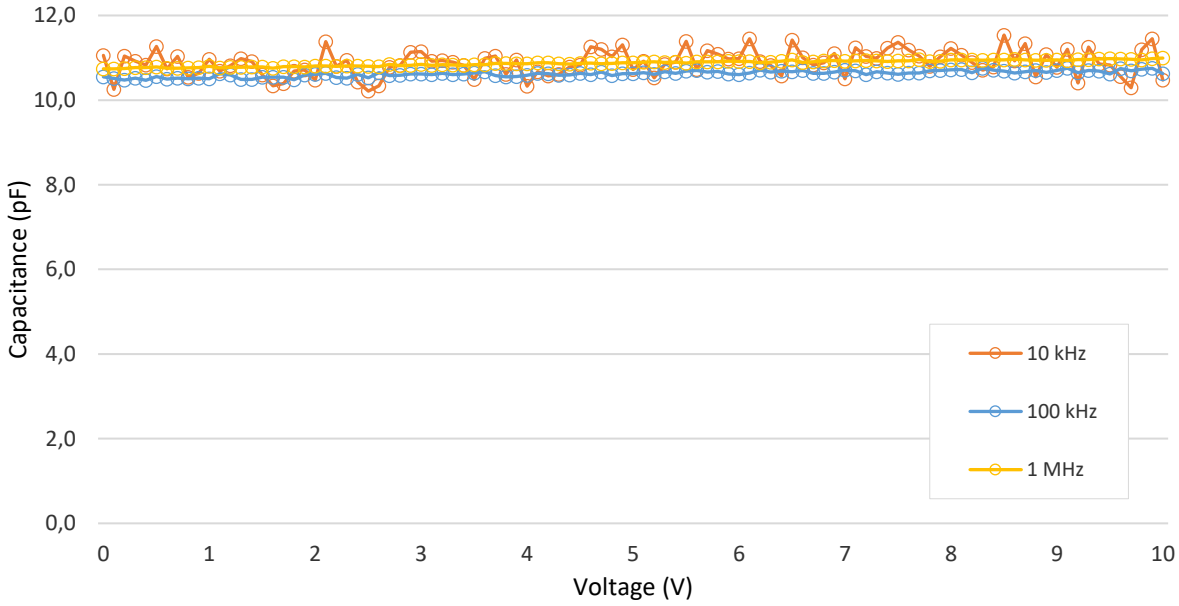


Fig 5.9, Dependency of capacitance on the voltage for CAP100-ONO at different frequencies

5.5.2. Capacitance for different areas for a single layer and multilayer dielectric plate capacitor

To further study the performance of the dielectric layer, the capacitance of the CAP100, CAP300 and CAP1000 is measured for both dielectrics. Figs 5.10 and 5.11 show the capacitance versus the applied voltage for the single layer and the multilayer dielectric, respectively. For fair comparison, the capacitance is normalized to the surface area to obtain the capacitance density. The absolute capacitance is displayed on the left of the graph, the capacitance density is displays right. It is found that for both dielectrics the capacitance density decrease with a decreasing area.

Weet nog niet zo goed hoe ik dit moet plaatsen, maandag even navragen bij Johan

Mask hole (µm)	*Capacitance (pF)*	*Capacitance density (pF/mm^2)*
CAP100-O	*10.8*	*377.6*
CAP300-O	*79.5*	*703.7*
CAP1000-O	*1001.1*	*962.6*
CAP100-ONO	*10.6*	*370.1*
CAP300-ONO	*78.6*	*695.4*
CAP1000-ONO	*990.1*	*952.1*

Table 5.4, Capacitance and Capacitance density of the different test devices without trenches.

5.5.3. Influence of the introduction of trenches.

Finally, the influence of the trenches on the capacitance density per footprint area is investigated. The capacitance density is measured for the CAP300 devices with varying trench diameters. For the single dielectric layer an increase in capacitance density is found from 1.8 nF/mm^2 to 10 nF/mm^2, which is an increase by a

factor 5. For the multilayer dielectric an increase by a factor 7 is observed from 2.0 nF/mm^2 to 14 nF/mm^2 (Table 5.5). Although the capacitance for the flat capacitors is comparable, the ration of increase is higher in the multilayer dielectric device.

Mask hole (µm)	*CAP300-O (nF/mm^2)*	*Increase*	*CAP300-ONO (nF/mm^2)*	*Increase*	*Expected*
Flat	*1.8*	*1*	*2.0*	*1*	*1*
0.8	*5.2*	*2.9*	*5.8*	*2.9*	*5.1*
1.0	*6.4*	*3.6*	*9.0*	*4.5*	*10.8*
1.2	*7.6*	*4.2*	*10.6*	*5.3*	*12.4*
1.4	*8.8*	*4.9*	*12.2*	*6.1*	*14.1*
1.6	*10.0*	*5.5*	*14.0*	*7.0*	*15.9*

Table 5.5, Capacitance density of the different CAP300-O and CAP300-ONO test devices for different trench diameters.

Both devices are not able to reach the calculated capacitance ratio (Fig 5.10). However, the trend line is comparable. Due to the difference in depth of the trenches, the capacitance increase between no trench and the 1.0 µm trench is expected to be more than the between 1.0 µm and 1.6 µm. This behavior is confirmed by the measurements.

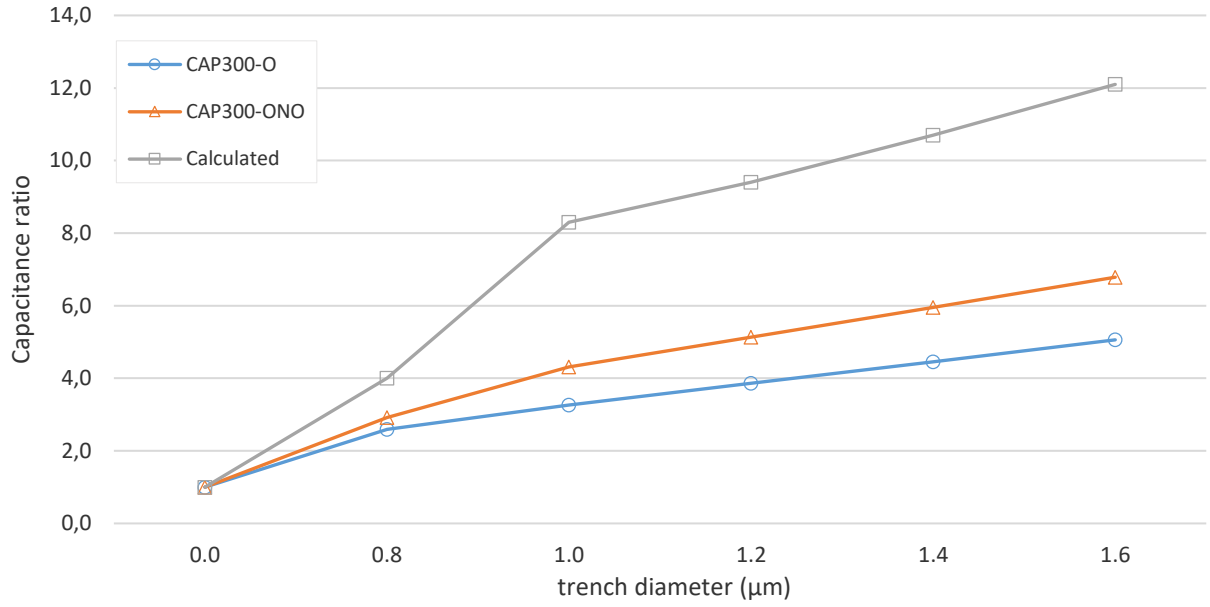


Fig 5.10, Capacitance density versus the trench diameter for the CAP300-O, CAP300-ONO and the calculated increase.

5.6 Conclusion

In this chapter, first the breakdown voltage of the single layer and the multilayer dielectric are compared to the expected breakdown voltage. It is shown that the measurements were in line with the expected values. It must be noted that the calculated value of the breakdown voltage is merely an indication. Many assumptions are made here. Furthermore, the influence of 1) an increase in area and 2) the introduction of trenches to the breakdown voltage is studied. The increase in area cause a decrease in breakdown voltage of 3% in the single layer dielectric compared to 16% in the multilayer dielectric. The introduction of the trenches reduced the breakdown voltage by 36% and 25% for the single layer and multilayer respectively.

The measured capacitance density for the dielectrics in flat devices is almost the same. Although the capacitance is comparable, the multilayer dielectric performs better with respect to the breakdown voltage. In addition, the increase in capacitance by introducing trenches to the devices was higher for the multilayer dielectric compared to the single layer dielectric. In combination with the more stable breakdown voltage that is observed for the multilayer dielectric in trenches, the multilayer dielectric seems to be the preferred dielectric.

6. Conclusion

In this thesis, challenges related to the integration of high density capacitors in the F2R technology platform have been addressed. The design of a dedicated mask set and flowchart together with the optimization of some bottleneck process steps have led to the fabrication of the first trench capacitors for the integration in the F2R platform.

A new DRIE recipe is created for the fabrication of 1.2 µm wide high aspect ratio trenches. The problem to control the inflow and outflow of etch and passivation species was identified. Using an etch split the mask pattern is better transferred into the silicon substrate and a straight 1.2 µm wide trench is etched with a low surface roughness.

Furthermore, a first step has been made towards the fabrication of a low breakdown voltage and a high breakdown voltage part in a silicon dioxide – silicon nitride – silicon dioxide multilayer dielectric. The uniform deposition of the layers is shown and the possibility to partly remove the top silicon dioxide layer has been investigated and demonstrated. However, further research is needed to better protect the top silicon layer in the etch process to remove the top silicon dioxide.

Using the mask set and process flow, the test devices are fabricated. The breakdown voltage and capacitance are measured for different area devices and two different dielectric configurations. In addition, the influence of applying trenches to the devices is investigated. The introduction of trenches increased the capacitance density on the test devices by a factor of 10 for the silicon dioxide dielectric. By using the multilayer dielectric the capacitance density is even further increased to a factor of 14. Furthermore, for a comparable capacitance, the point of breakdown in the multilayer dielectric is 35% higher compared to the point of breakdown in the single layer dielectric.

The developed trench capacitors in this work are expected to play an important role in the development of the next generation smart catheters and implants. Increasing the capacitance density on these devices enables further downscaling of catheters and implants without compromising on electrical specifications. Regarding the hart catheters, this allows for better images and the possibility to diagnose smaller arteries.

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A. Flowchart

Info \ Attention \ Backup equipment					Closed Coupled	
TS	**Step ID**	**DC**	**Operation**	**Resource**	**Process (Operation Description)**	**(special) Instruction**
01	010		0601-TS01	START	Start of Technical Stage	Marker etch, Collect Wafers
01	020		RCA1014	R72	FHZ4mHCl4m	
01	030		BCA1225	F78	HMDS_HPR504_1300nm_SB110	
01	040		BEX3400	B22	TRC_MRKS_65	Energy= 150 mJ/cm2, Focus=0µ
01	050		BDA0122	F78	Develop_HPR504	recipe: **Develop_HPR504**
01	060		EDA0000	E28A	Marker etch	"Tdesc met dechuck 6mAPS MRK01_COND 3 m on res dummy)EDA0000 (APS MRK01 140nm)Every 4th wafer Tdesc met dechuck 30s"
01	070		0019-LASER_MARKING	DEFAULT	Laser marking acc. WI	number wafer: TrenchCap_0001 … 0006 Test_TrenchCap_0001 … 0006
01	080		RSA1015	R72	HZNH4OH36m	HZplus36min
01	090		RCA1014	R72	FHZ4mHCl4m	
02	010		0602-TS02	START	Start of Technical Stage	Trench etch
02	020		COE4103	C03	SiO2 400 700 Eng	deposit low stress SiO2 on 400 deg C, thickness: 700nm
02	030		BCA1225	F78	HMDS_HPR504_1300nm_SB110	recipe: **HMDS_HPR504_1300 nm_SB110**
02	040		BEX3402	B22	TRC_TRENCH	Reticle: TrenchCaps / 051218-JNG01 Layer: TRC_TRENCH Reticle locatie: 1fa1 Belichting: 100 mJ/cm2; Focus: vast 0
02	050		BDA1123	F78	Develop_HPR504_PEB110	recipe: **Develop_HPR504_PEB110**
02	060		0010-BATCH_ON_HOLD	DEFAULT	Batch on hold	Contact batch owner for litho (pattern) inspection
02	070		IIA9999	I23	Inspection Ergoplan	Inspect Litho pattern
02	080		EOE0000	E28A	SiO2 deep etch	Tdesk met dechuck 6minutes PR wafer APSSiO01 cond 3 min EOE0000 (SiO01) ~1 µm Tdesk 2 minutes between wafers Fixed Time 7 min
02	090		EXX0004	E28C	Experimental E28C	Run recipe ENG Test\Carlo\BSC 03
02	100		EPA0009	E33	resist strip 5 minutes	resist strip 5 minutes
02	110		NEA1034	N26	BOE_ETCHANT	10 min
02	120		RRA1009	R80	QDR	Process 3 (5 cycles)

02	130		NDA1036	R108	Rinse / Dry	STD program
03	010		0603-TS03	START	Start of Technical Stage	ONO deposition
03	020		0100-CLOSE_COUPLE_START	DEFAULT	Close couple	
03	030		RCA1014	R72	FHZ4mHCl4m	
03	040		0050-SPLIT_START	DEFAULT	Split batch	Start of Split
03	041		ODA9001	O35B2	B2 DRY 900 15	O35B2, **30±2 nm** DRY 850 ipv DRY 900. (DRY 850 op B2 staat niet in O.L.)
03	042		ODA9001	O35B2	B2 DRY 900 15	O35B2, **5±2 nm** DRY 850 ipv DRY 900. (DRY 850 op B2 staat niet in O.L.)
03	050		0051-SPLIT_END	DEFAULT	Split batch	End of Split (Merge Batch)
03	060		0101-CLOSE_COUPLE_END	DEFAULT	Stop close couple	
03	061			-		Move SFC to TS02
03	070		ONE6001	O35B3	B3 NITRI 800 - 150	O35B3, deponeer **10±2** nm, 150mm, 800°C, NITRIDEN
03	80		0050-SPLIT_START	DEFAULT	Split batch	Start of Split
03	081		OTX8001	O34A3	Experiment TEOS,inform PE	Depositie van een zo dun mogelijke laag oxide. Target is **5±2 nm** oxide
03	082		OTX8001	O34A3	Experiment TEOS,inform PE	Depositie van **35±2** nm oxide.
03	090		0051-SPLIT_END	DEFAULT	Split batch	End of Split (Merge Batch)
03	091			-		Move SFC to TS02
03	100		NDA1039	R30	Rinse / Dry 150 mm	STD program
03	110		BCA1501	F78	HMDS_maN1410_SB120	
03	120		BEX3406	B22	TRC_ONO	Reticle: CBOX-OXIDE / 150319-JNG01 Layer: TRC_ONO Reticle locatie: 1Ca3 Belichting: 250 mJ/cm2; Focus: vast 0
03	130		BDA0640	F78	Developer maD533/s	For maN1400 resist on Stepper
03	140		0010-BATCH_ON_HOLD	DEFAULT	Batch on hold	Contact batch owner for litho (pattern) inspection
03	150		IIA9999	I23	Inspection Ergoplan	Inspect Litho pattern
03	160		NEA1034	N26	BOE_ETCHANT	1.5 min
03	170		RRA1009	R80	QDR	Process 3 (5 cycles)
03	180		NDA1036	R108	Rinse / Dry	STD program
04	010		0604-TS04	START	Start of Technical Stage	Top electrode
04	020		OSX8001	O37C3	Experiment ASI, inform PE	O37C3, Inform PE, deposit 400nm d A-SI560-recipe
04	030		OPX0001	O37C1	PH3 dope	10min P-glass depositie, 30min anneal op 1000°C
04	040		NEA1018	N34	BOE,7:1, No M	2 minutes
04	050		RRA1009	R81	QDR	Process 3 (5 cycles)
04	060		NDA1039	R108	Rinse / Dry 150 mm	STD program
04	070		BCA1225	F78	HMDS_HPR504_1300nm_SB110	

04	080		BEX3403	B22	TRC_POLY	Reticle: TrenchCaps / 051218-JNG01 Layer: TRC_POLY Reticle locatie: 1fa1 Belichting: 120 mJ/cm2; Focus: vast 0
04	090		BDA0122	F78	Develop_HPR504	recipe: **Develop_HPR504**
04	100		0010-BATCH_ON_HOLD	DEFAULT	Batch on hold	Contact batch owner for litho (pattern) inspection
04	110		IIA9999	I23	Inspection Ergoplan	Inspect Litho pattern
04	120		BBA2102	O187	Bake on Hotplate	Hotplate T=150°C t=2min
04	130		EXX0003	E28B	Experimental E28B	Tdesk ICP P01 cond (resist dummy 1minutes), EXX0003 (ICP P01, 80sec)
04	140		EPA0009	E33	resist strip 5 minutes	resist strip 5 minutes
05	010		0601-TS01	START	Start of Technical Stage	contact
05	020		NDA1039	R108	Rinse / Dry 150 mm	STD program
05	030		COE4201	C03	SiO2 400 0 req thickness	Use 0stress SiO2 recipe at 400degC 700nm
05	040		RDA1011	R108	Rinse / Dry	STD program
05	050		BCA1225	F78	HMDS_HPR504_1300nm_SB110	
05	060		BEX3404	B22	TRC_CONTACT	Reticle: TrenchCaps / 051218-JNG01 Layer: TRC_CONTACT Reticle locatie: 1fa1 Belichting: 150 mJ/cm2; Focus: vast 0
05	070		BDA0122	F78	Develop_HPR504	recipe: **Develop_HPR504**
05	080		0010-BATCH_ON_HOLD	DEFAULT	Batch on hold	Contact batch owner for litho (pattern) inspection
05	090		IIA9999	I23	Inspection Ergoplan	Inspect Litho pattern
05	100		EOE2001	E28A	SiO2 deep etch	Tdesk met dechuck 6minutes APS SiO01 cond 3 minutes EOX2000 (SiO01 3min 30 sec) Tdesk 2 minutes between wafers Stop on manual EP
05	110		EPA0010	E15	Descum/resist strip	60 min. 130°C
06	010		0601-TS01	START	Start of Technical Stage	Aluminum deposition
06	020		0100-CLOSE_COUPLE_START	DEFAULT	Close couple	
06	021		NEA1004	N25	HF1%,6"	1min
06	022					
06	023		SAE0499	S31	AlCu1% EXP opcode	Ets 0nm Thickness 1000nm, power 8kW, Stress
06	030		0101-CLOSE_COUPLE_END	DEFAULT	Stop close couple	
06	040		BCA1225	F78	HMDS_HPR504_1300nm_SB110	recipe: **HMDS_HPR504_1300 nm_SB110**

06	050		BEX3405	B22	TRC_AL	Reticle: TrenchCaps / 051218-JNG01 Layer: TRC_AL Reticle locatie: 1fa1 Belichting: 150 mJ/cm2; Focus: vast 0
06	060		BDA0122	F78	Develop_HPR504	recipe: **Develop_HPR504**
06	070		0010-BATCH_ON_HOLD	DEFAULT	Batch on hold	Contact batch owner for litho (pattern) inspection
06	080		IIA9999	I23	Inspection Ergoplan	Inspect Litho pattern
06	090		NEA1000	N24	PES,30°C,6"	11min
06	100		RRA1009	R80	QDR	Process 3 (5 cycles)
06	110		NDA1036	R108	Rinse / Dry	STD program
06	120		EPA0009	E33	resist strip 5 minutes	resist strip 5 minutes

B Process Optimization

B.1 Chemical Vapor Deposition

Chemical vapor deposition (CVD) is a process to deposit solid films on the surface of a substrate. The process is based on a surface reaction between a vapor phase reactant and a substrate. In order for this reaction to take place, the substrate must be heated (typically higher than 300°C) [36]. The reaction rate is determined by an activation energy and the rate at which the reactant arrive at the surface. The activation energy can be supplied by various sources, however temperature is the most used energy source. CVD processes are characterized by their good step coverage compared to Physical Vapor Deposition (PVD).

There are different kind of flavors in CVD. The most used techniques are low pressure chemical vapor deposition (LPCVD) and plasma enhanced chemical vapor deposition (PECVD). In general LPCVD is characterized by a low operation pressure (0.1-2.0 Torr) and high temperature (700-900°C) and PECVD by a lower temperature (200-400°C). Due to the low pressure in LPCVD, the diffusivity of the reactant gas is increased by one order of magnitude compared to atmospheric conditions. This is highly beneficial for the transport of the reactant to the surface. Therefore, the reaction rate-limiting factor is the temperature. Furthermore, the high diffusivity enables multiple closed to each other stacked wafers to be processed in one batch. In the deposition process of the dielectric and Poly-Si, this characteristic cause the uniform coverage of the layers inside the trenches. PECVD enables deposition of solid films at low temperature. In these processes a RF-induced plasma is used as the activation energy source for the reaction, which lowers the operation temperature. A lower temperature can be desirable but could result in a less dense solid film that is more prone to impurities.

LPCVD TEOS

LPCVD TEOS (tetraethyl orthosilicate) is the reaction of tetraethyl orthosilicate with water to form silicon oxide and ethanol, $Si(OC_2H_5)_4 + 2\ H_2O \rightarrow SiO_2 + 4\ C_2H_5OH$, under typical temperatures of 650°C to 750°C. This temperature results in a good step coverage and good process control. LPCVD TEOS is used for the deposition of a thin oxide film on top of the nitride as dielectric layer.

PECVD Oxide

In contrast to LPCVD TEOS, PECVD oxide is deposited at lower temperatures of about 300°C to 400°C. By deposition at lower temperatures, the stresses in the oxide layer are reduced. Low stresses are essential for the fabrication of the buried trenches. The low temperature makes these layers also suited to deposit on top of low melting point metals like aluminum. A drawback of the low process temperature is the higher degree of porosity of and the increased change of impurities in the thin layer.

LPCVD Nitride

The formation of silicon nitride using LPCVD is based on the reaction of dichlorosilane with ammonia to form silicon nitride, hydrochloric acid and hydrogen, $3\ SiH_2Cl_2 + 4\ NH_3 \rightarrow Si_3N_4 + 6\ HCl + 6\ H_2$. This reaction takes place at 700°C to 900°C and typical pressure of 200 to 500 mTorr. In micromachining LPCVD nitride is often used as an dielectric in combination with an thermal grown oxide layer, which is also the application for this project.

LPCVD Silicon

Silicon can be deposited from trichlorosilane or silane. The reactions involved are $SiHCl_3 \rightarrow Si + Cl_2 + HCl$ and $SiH_4 \rightarrow Si + 2\ H_2$ respectively. The top electrode is a layer of doped poly-silicon. In the PInS cleanroom direct deposition of poly-si is not possible. However, the deposition of a layer of amorphous silicon followed by a heat anneal step results in a layer poly-si as well.

CVD Phosphosilicate Glass

The deposition of PSG is based on a low temperature oxidation (LTO) with the addition of phosphine (PH_3). LTO operates at relatively low temperatures, 400°C to 450°C, and low pressure, 200 to 400 mTorr. The reaction is based on the spontaneous combustion of silane in the presence of oxygen, $SiH_4 + O_2$. By adding a flow of PH_3 to the furnace, a layer of PSG is obtained. This layer is needed as a solid diffusion source to dope the silicon and make it suitable as top electrode.

B.2 Photolithography

Photolithography is a process to transfer a pattern from a mask into a photoresist layer. The photoresist can be used as a masking layer for etching processes or ion implantation. During this project, photolithography is used for pattern transfer by etching. Photolithography consist of three main steps; 1) spinning the resist, 2) an exposure treatment and 3) the development.

As a start, a photoresist is spun on the wafer, it might be necessarily to first apply a primer on the surface to promote the adhesion. The photoresist contains solvent, which may contain built-in stresses. Therefore, the wafers are soft baked to remove the solvent. Next, the wafer is transported to an exposure system that illuminates the wafer through a mask. The photons of the incoming UV light reacts with the photoresist. The photochemical reaction due to the photons in the photoresist bleaches the sensitizer in the resist [37]. After exposure and before development, a post-exposure bake can be applied. During the development phase a developing solvent selectively dissolves the resist, generally positive photoresists are used in which the unexposed resist is removed. During an optional de-scum step, an oxygen plasma removes scum from polymers that is deposited after development. Before etching, the photoresist can be hard baked to remove the residual solvents and anneal the thin film to promote the quality and hardness of the resist film.

This project has several lithography steps involved. The pattern size on the mask ranges from 0.8 to 1.6 µm. To accurately transfer the mask pattern into the photoresist, optimization of the lithography job is needed. By performing a focus exposure matrix (FEM) insight is given in the optimal job setup. A FEM is characterized by a varying exposure doses on the x-axis and a variation of the focus on the y-axis. By investigating the different combinations, the preferable energy and focus combination can be determined. There can also be chosen to adjust just one of the two parameters in case one of the two is already known.

Four of the five lithography processes in this project use a 1300nm HPR504 photoresist and soft bake it at 110°C. The choice for HPR504 is based on the current developments within the PInS cleanroom where HPR504 is chosen as the standard photoresist for production. Since the trench capacitors will become part of a production chip the use of HPR504 is recommended. Before spinning the resist, the surface is treated with HMDS primer for improved adhesion of the layers. One of the photolithography steps uses a negative photoresist, this photoresist will harden under the influence of UV light. The best focus exposure values for the lithography steps in the process flow of the trench capacitors are listed in x.x in section 9.3.2.

B.3 Dry Etching

Dry etch processes combine physical and chemical etching techniques to remove material. The big advantage of dry etching, compared to wet etching, is the capability of directional (anisotropic) etching without relying on the crystal planes of the material. The anisotropic etching character enables an accurate transfer of the mask pattern into the etch target.

During dry etching, a gas is pumped into a vacuum chamber and ionized by an electric field. The electric field is generated by applying a radiofrequency (RF) field over a pair of electrode (Fig B.1). The ionized gas is called a plasma. In the plasma, electrons are accelerated towards the positive lower electrode. The electrons collide with atoms and molecules. The lower electrode is connected to an RF power supply with a typical frequency of 13.56 MHz via a blocking capacitor. The upper electrode is connected to the ground. The electrons have a smaller mass than ions (approx. 100000 times smaller), therefore they are able to follow the oscillations of the field and jump into the lower electrode. The lower electrode will gradually build up a negative bias potential (V_{dc}) due to the blocking capacitor and push the electrons away. The migration of electrons from the lower electrode forms a region with a low electron density, called an ion sheath. Ions in the plasma travel around freely with an energy equal to the plasma energy (V_p). The negative potential near the ion sheath pulls the ions towards the lower electrode. This phenomena result in a bombardment of ions on the etch target that is placed on the lower electrode and can be seen as the physical etching of the material [38].

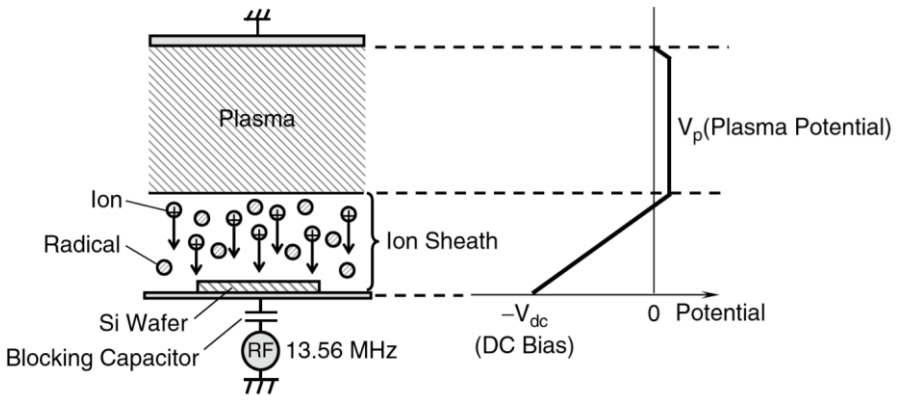


Figure B.1. Overview of RIE reactor [39].

Simultaneously, there are reactive species, called radicals, floating around in the plasma that react with the etch target on the surface. The radicals etch the material in an isotropic way. In combination with the ion bombardment, an ion-assisted reaction is generated, forming an anisotropic etching profile.

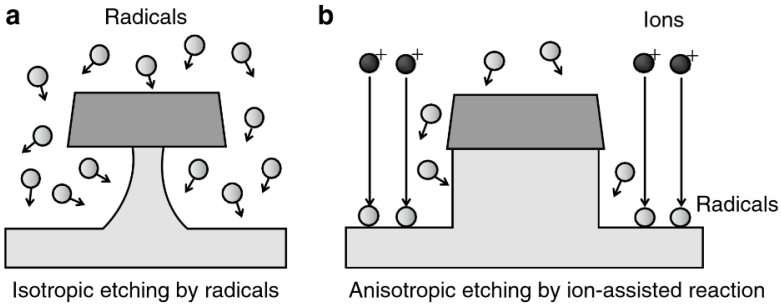


Figure B.2. isotropic and anisotropic etching [39].

Inorganic materials like silicon dioxide and organic polymers generated in the plasma form a protective film on the surface of the etch target that prevent radicals from etching. Because of the vertical direction in which the ions bombard the etch target, the ions remove the protective film on the horizontal surface. The radicals can now react with the exposed etch target. The vertical sidewalls of the etch target will experience a very limited amount of incoming ions and stays protected for the radicals (Fig B.3).

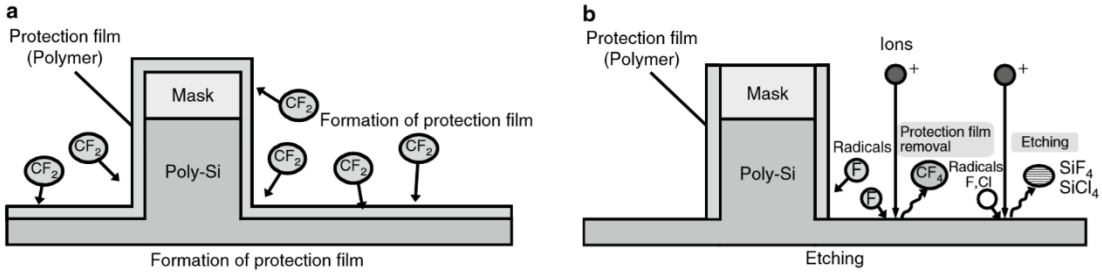


Figure B.3. Model of sidewall protection process [39]

Dry etching has two classification, Reactive Ion Etching (RIE) and Deep Reactive ion Etching (DRIE). In a RIE reactor, or parallel plate reactor, a capacitively coupled plasma (CCP) source creates both the plasma and the bias potential. DRIE differs from RIE while it consist of at least two RF generators for independent control of plasma generation and ion bombardment. A DRIE reactor makes use of an inductively coupled plasma source (ICP), which can generate a plasma with a density of one or two orders of magnitude higher than with a CCP. Furthermore, DRIE operates in a lower pressure range and has fast mass flow controllers (MFC) which control the flow of gas in and out of the vacuum chamber. DRIE enables the fabrication of deep and narrow structures, called high-aspect ratio microstructures (HARMS). The most used process to fabricate HARMS is with the use of the ‘’Bosch process’’, a process patented by Robert Bosch GmbH [40].

Bosch Process

The Bosch process is characterized by an alternating introduction of passivation and etching gasses into the process chamber, C_4F_8 and SF_6/O_2, respectively. During the passivation cycle, a thin Teflon-like film is deposited on the walls of the etched structure. The etching cycle starts with a ''boost phase'' where the passivating film on the bottom of the structure is removed by ion bombardment. After the boost phase there is an ''etch phase'' where the etch target is etched by the fluorine radicals released from SF_6 in the plasma [39], [41].

An advantage of the Bosch Process is the controllability and high mask selectivity values. Typical parameters that enable accurate tuning of the process are; ICP power, CCP power, SF_6-flow, C_4F_8-flow, etch cycle time, etch cycle pressure, passivation cycle time and passivation cycle pressure.

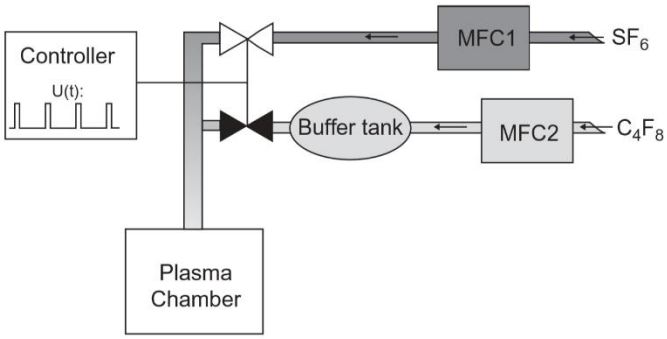


Figure B.4. MFC for the Bosch process [42].

B.4 Wet processing

Wet processing, or wet etching, is a process where the etch target is brought in a bath with chemicals that react on the surface with the exposed etch target. Wet etching proceed by 1) the transport of the reactant to the etch target, 2) reaction at the surface of the etch target and 3) transport of the reaction product away from the surface. The etch rate is thus determined by the transport of the reactant to, and reaction product from, the surface and the reaction rate at the surface. The etch rate can be increased by stirring or heating up the chemical bath respectively. The wet etch process is often an isotropic process and etches evenly quick in all crystalline directions which causes under etch. Some applications for wet etching are shaping 3D structures, cleaning and polishing.

The wet processing is used for different purposes in the fabrication of the trench capacitors. The process is used for removal of complete layers like oxide and PSG, as a cleaning step before aluminum deposition and as a wet etch step to bring the aluminum into pattern.

For the removal of the oxide and PSG layer, a bath of buffered oxide etch (BOE) is used. BOE 7:1 is a chemical composition of ammonium fluoride (NH_4F) and hydrofluoric acid (HF) in the ratio 7:1, respectively. The typical etch rate of BOE 7:1 is ~80 nm per minute for silicon dioxide [43]. The 700nm silicon dioxide, used as hard mask for the DRIE of the trenches, is etched for 10 minutes in the BOE 7:1. PSG etches quicker than normal silicon dioxide due to the dopant in the material. Taking some over etch time into consideration, 100 nm PSG is removed in an etch time of 90 seconds. LPCVD TEOS, used in the multilayer dielectric, has a typical etch rate of 400 nm per minute.

Before deposition of aluminum, the wafer is dipped in a HF bath to clean the wafer. HF removes the native oxide and promotes the adhesion between aluminum and the Poly-Si and substrate. Native oxide layers have typically a thickness of 20 Å, a quick dip for a few seconds is sufficient to remove the native oxide. To pattern the aluminum, PES is used. PES is a mixture of nitric acid (HNO_3), phosphoric acid (H_3PO_4), acetic acid ($C_2H_4O_2$) and water (H_20). Typical etch rates of PES for aluminum are around 100 µm per minute. To pattern the aluminum the wafer is placed in a bath filled with PES for 12 minutes.

B.5 Oxidation

In the manufacturing of IC's the formation of oxide films on silicon, oxidation, is an important process step. Oxide layers form passivation of the surface, electrical insulation and dielectric properties that form the bases for semiconductor devices [27]. Oxidation can be executed dry or wet. Dry oxidation of silicon is based on the reaction of oxygen (O2) with the silicon (Si) surface, $Si + O_2 \rightarrow SiO_2$. Wet oxidation is based on the reaction of steam (H_2O) with Silicon (Si), $Si + H_20 \rightarrow SiO_2 + 2H_2$. At a given temperature the oxidation rate in steam is about 5 to 10 times higher than for dry oxygen. The dry oxidation reaction readily takes place, even at room temperature, forming a native oxide layer (~20Å). Performing this reaction in furnace tubes at elevated temperatures between 600°C and 1250°C cause the oxidant to diffuse through the surface oxide layer and form a thick oxide. During this reaction, the oxide layer consumes the silicon with a ratio of 1:0.46, i.e. when 100 nm of oxide is grown, 46 nm of silicon is consumed [27]. A dry oxidation consist of three steps; 1) transport of oxidant to the surface, 2) diffusion through the existing oxide and 3) the oxidation reaction. The oxidation rate of Si depends on temperature, pressure, oxidant, doping and crystal orientation.

The first dielectric layer is deposited by a dry oxidation at 850°C. Because the layer thickness is in the range of 5 nm the deposition is performed at a relatively low temperature. The oxidation process slightly smoothens the wall since it consumes a bit of the silicon. It is however possible that after the DRIE process the wall profile of the trench is slightly scalloped. Oxidation in combination with a wet etch process step can then be used to smoothen a rough silicon surface. The peaks in the profile oxidize quicker than the valleys since they are oxidizing from different directions. Removing the oxide layer results in a more flattened profile. However, since the oxidation in the trench is performed in the direction of different crystal planes of the silicon, it is important to perform this oxidation at high temperature to eliminate difference in the oxidation rates. Although the design of the trenches for the trench capacitors seems smooth enough for proper functioning of the device, this process can be taken in consideration in the fabrication.

B.6 Doping by diffusion

Doping is a process to implement impurities into a semiconductor (silicon) to adjust its electrical, optical or structural properties. Elements with one valence electron more or less then silicon can be used as a donor (n-type) of acceptor (p-type) material. Phosphorus is widely used as a donor dopant. There are different techniques available to dope the silicon, doping by diffusion, in-situ doping and doping by ion implantation. Doping by diffusion is based on the principle of the diffusion of electrons from or to the dopant. This can be established by a gaseous dopant or a solid diffusion source [44]. In the case of a solid diffusion source, a solid thin layer of a dopant is deposited on the silicon, by heating the materials (annealing) electrons migrate from one material to the other. Removing the dopant material results in a doped silicon layer. Doping of the semiconductor reduces the resistivity of the material, an often used application of such materials is to establish an ohmic contact [45]. The top electrode in the trench capacitor is fabricated using the principle of doping by diffusion with PSG as the solid dopant source.

C. Mask Design

C.1 Reticle design

The reticles that contain the images for the lithography jobs for the trench capacitors, are designed in the software program Clewin. The images TRC_TRENCH, TRC_POLY, TRC_CONTACT, TRC_AL and TRC_ONO are drawn on five different layers and saved as a GDS-file. In the software program K-Layout the images are flattened and converted to a OAS-file. The masks are ordered clear-tone, which means that the majority of the mask is covered by chromium and that purple shaded area in Fig C.1 is open and able to let UV light pass through.

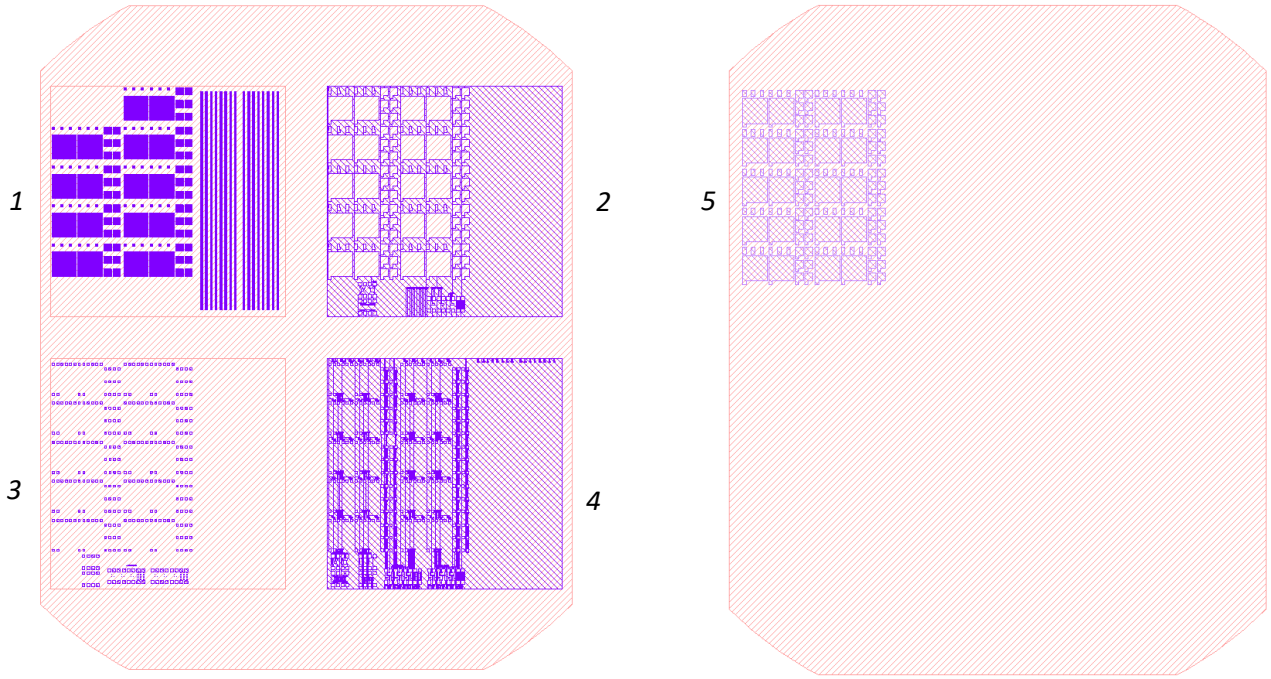


Figure C.1, Image of the TRC mask set in K-layout with the; 1) TRC_TRENCH layer, 2) TRC_POLY layer, 3) TRC_CONTACT, 4) TRC_AL layer and 5) TRC_ONO layer.

The mask set can be found in the PInS cleanroom by the name TrenchCaps and CBOX-OXIDE. The names of the individual layers are listed in table C.1, accompanied with the corresponding operation codes and exposure energies. For the alignment marks the exposure doses is known, for the mask images these value depend on the target outcome and should be determined by a FEM.

Layer	*Name*	*Opcode*	*Energy, Focus*
0	*TRC_MRK_65*	*BEX3400*	*150 mJ/cm², 0 µ*
0	*TRC_MRKFR*	*BEX3401*	*150 mJ/cm², 0 µ*
1	*TRC_TRENCH*	*BEX3402*	*To be determined by FEM*
2	*TRC_POLY*	*BEX3403*	*To be determined by FEM*
3	*TRC_CONTACT*	*BEX3404*	*To be determined by FEM*
4	*TRC_AL*	*BEX3405*	*To be determined by FEM*
5	*TRC_ONO*	*BEX3406*	*To be determined by FEM*

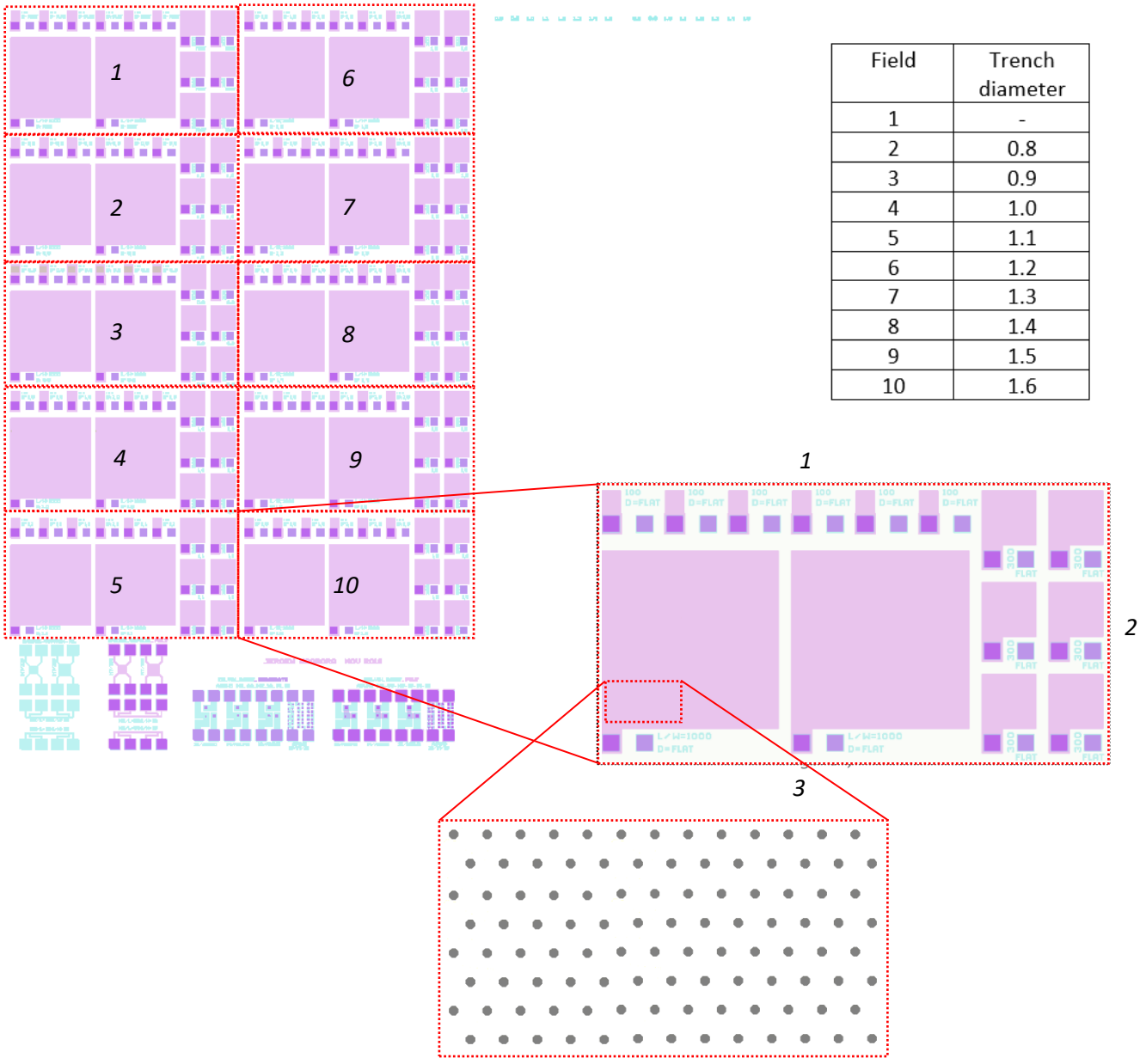
Table C.1. Names of the TRC mask layers with the corresponding opcodes and exposure settings.

The first image, TRC_TRENCH, is the mask to pattern holes in an oxide layer. This layer will function as a hard mask for the trench etch in the silicon. The second image, TRC_POLY, is the mask to bring the Poly-Si into pattern. TRC_CONTACT is the mask layer to pattern contact holes to the substrate and the Poly-Si. The contact

holes are filled with an aluminum layer, which is patterned by the TRC_AL mask. The TRC_ONO layer patterns the second silicon dioxide layer for the fabrication of low and high voltage parts in the dielectric. The five images pattern different layers on the wafer. In combination with the deposition of other layers and other micro fabrication processes, the result is a chip containing trench capacitors and test structures. This chip is printed on the wafer in thirteen columns and fourteen rows.

C.2 Trench capacitors

The area with trench capacitors is divided in ten subareas. The subareas differ in the diameter of the holes on the mask. The size of the holes in the individual subareas are listed in the table in Fig C.2. Each subarea contains six small capacitors (CAP100), six medium sized capacitors (CAP300) and two large capacitors (CAP1000). The dimensions of the aluminum bond pads and contact holes are identical for all capacitors. The aluminum bond pads are 100*100 µm and the contact holes 90*90 µm. The planar surface area of Poly-Si is heavily dependent on the trenches and is different for the different devices.



Field	Trench diameter
1	-
2	0.8
3	0.9
4	1.0
5	1.1
6	1.2
7	1.3
8	1.4
9	1.5
10	1.6

Figure C.2. a) Global layout of the mask with ten areas filled with capacitors, each area has a variation in the diameter of the trench, b) each individual area holds three different sized capacitors; 1) six capacitors with an area of 100x100 µm, CAP100 2) six capacitors with an area of 300x300 µm, CAP300 and 3) two capacitors with an area of 1000x1000 µm, CAP1000.

The area that is covered by the trenches in the CAP100 is 100*100 µm, this area contains 725 trenches. For the CAP300 this area is 300*300 µm and contains containing 7275 trenches. The largest capacitors, CAP1000 have an area of 1000*1000 µm which holds 72750 trenches. The exact dimensions of the CAP100, CAP300 and CAP1000 are shown in Fig C.3. The Poly-Si is designed to overlap the trench area by five µm. The capacitors are marked by an accompanying text. This in aluminum patterned caption provides information regarding the trench diameter and capacitor size.

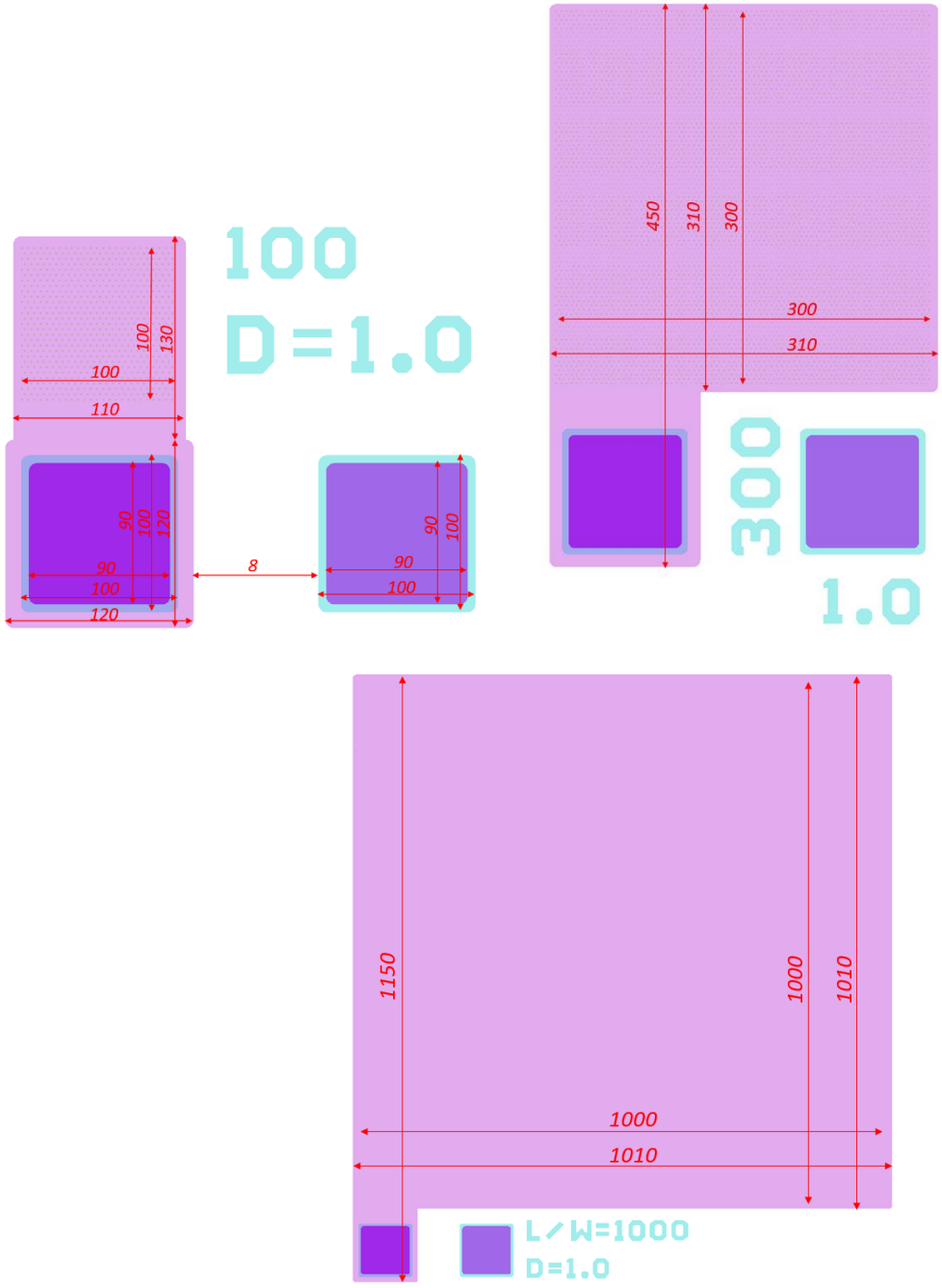


Figure C.3. Illustration of CAP100, CAP300 and CAP1000.

The holes in the TRC_TRENCH mask that are used to pattern the trenches have an octagonal shape, see Fig C.4. The use of circles on the mask for trench patterning resulted in a too large OAS-file. It is found that in the transfer of the mask pattern into the silicon dioxide the octagonal shape result in a circlar hole in the silicon dioxide. The pitch between each octagonal is four µm and kept constant for al diameters.

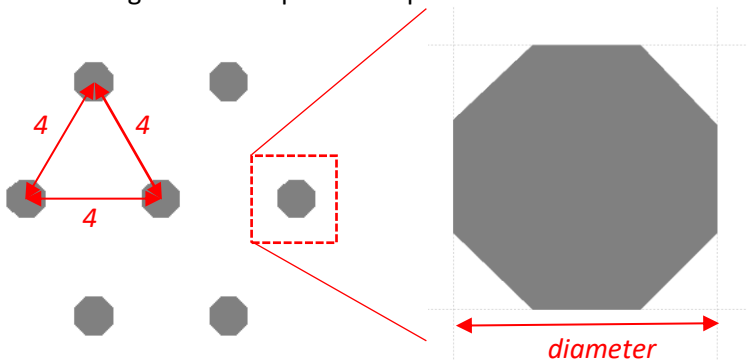


Figure C.4, Shape of the holes on the TRC_TRENCH mask layer.

D. Process Optimization

D.1 Process optimization

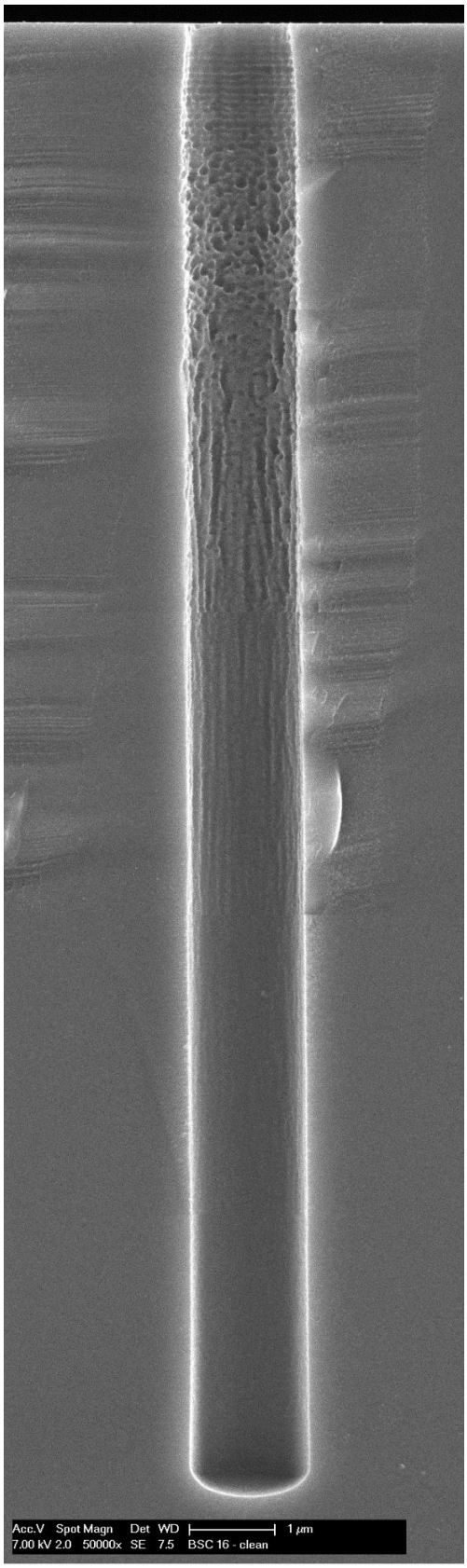


Figure D.1 Close-up of the trench that is etched with recipe BSC 16.

E. Appendix

Mask hole	*Trench diameter*	*Trench depth*	*Functional area CAP300 (5529 trenches)*	*Increase factor*
No hole	*No trench*	*No depth*	*0.03*	*1*
0.8	*1.1*	*18.1*	*0.45*	*4.1*
0.9	*1.4*	*24.2*	*0.70*	*6.2*
1.0	*1.7*	*27.9*	*0.94*	*8.4*
1.1	*1.8*	*28.5*	*0.96*	*8.5*
1.2	*1.9*	*29.3*	*1.08*	*9.5*
1.3	*2.0*	*30.0*	*1.15*	*10.3*
1.4	*2.1*	*30.6*	*1.23*	*10.9*
1.5	*2.2*	*31.2*	*1.30*	*11.6*
1.6	*2.3*	*31.8*	*1.38*	*12.3*

Table E.1. Dimension of the trenches that are applied to the CAP300 devices.

Mask hole	*Trench diameter*	*Trench depth*	*Functional area CAP1000 (67512 trenches)*	*Increase factor*
No hole	*No trench*	*No depth*	*1.0*	*1*
0.8	*1.1*	*18.1*	*5.3*	*5.1*
0.9	*1.4*	*24.2*	*8.2*	*7.9*
1.0	*1.7*	*27.9*	*11.2*	*10.8*
1.1	*1.8*	*28.5*	*11.4*	*10.9*
1.2	*1.9*	*29.3*	*12.9*	*12.4*
1.3	*2.0*	*30.0*	*13.8*	*13.3*
1.4	*2.1*	*30.6*	*14.7*	*14.1*
1.5	*2.2*	*31.2*	*15.6*	*15.0*
1.6	*2.3*	*31.8*	*16.5*	*15.9*

Table E.2. Dimension of the trenches that are applied to the CAP300 devices.

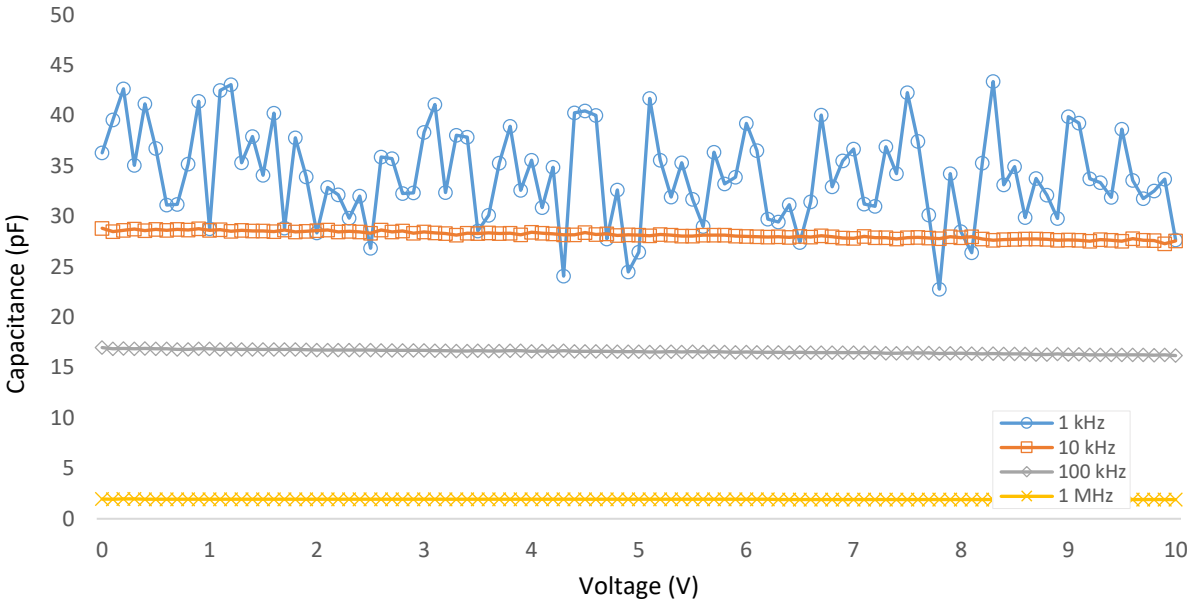


Figure E.1, Dependency of capacitance on the voltage for Cap100-O at different frequencies measured on the substrate and capacitor.

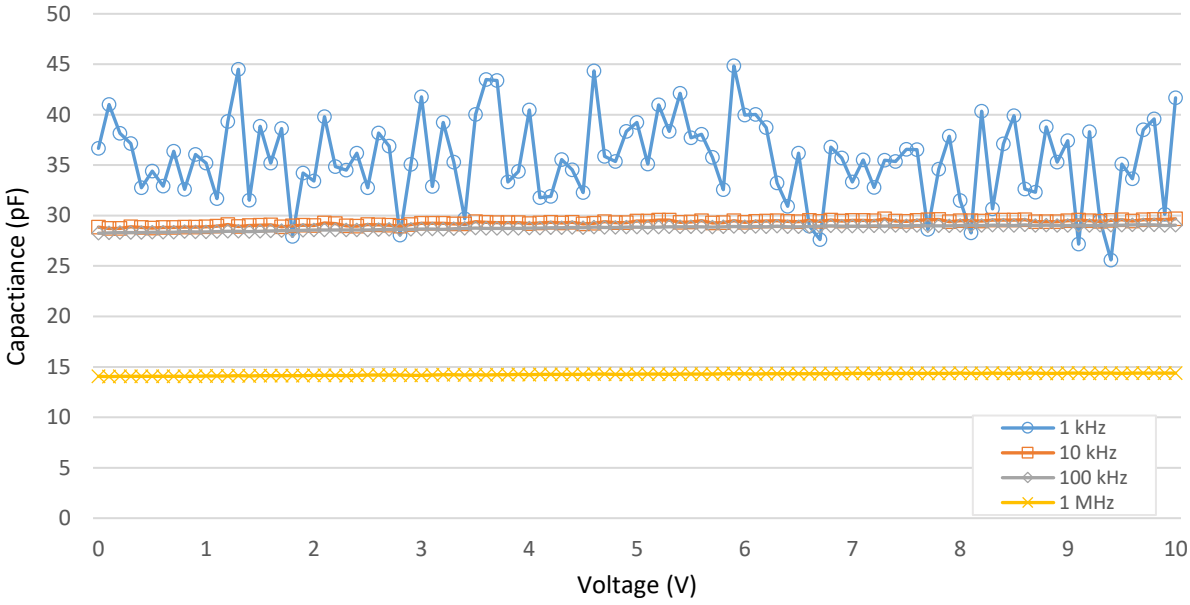


Figure E.2, Dependency of capacitance on the voltage for Cap100-ONO at different frequencies measured on the substrate and capacitor.

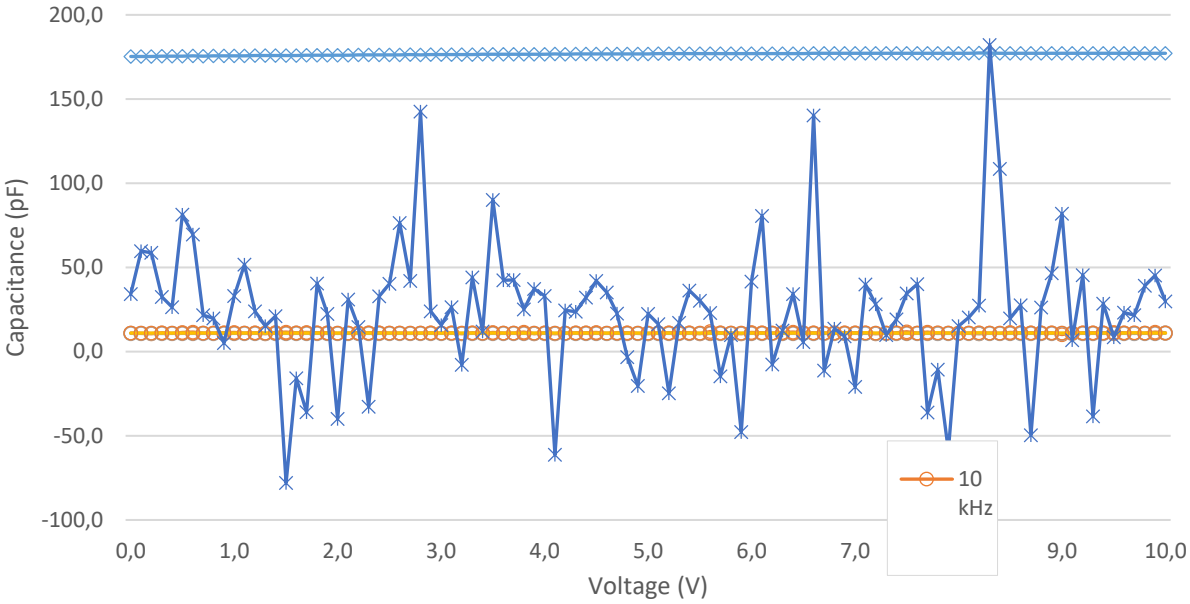


Figure E.3 Dependency of capacitance on the voltage for CAP100-O at different frequencies.

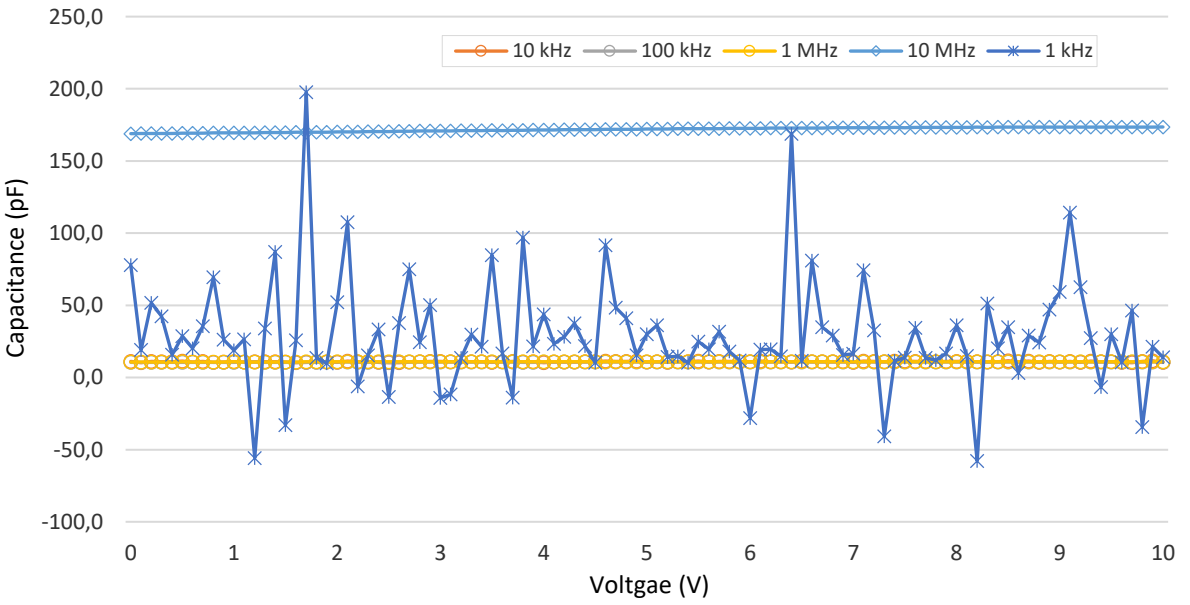


Figure E.4 Dependency of capacitance on the voltage for CAP100-ONO at different frequencies.