A Low-Power Class-AB Residue Amplifier for a 12bit 500MS/sec Pipeline ADC with Digital Calibration

Md. Shakil Akter

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THESIS

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by

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Abstract

This work mainly focuses on designing a low-power class-AB residue amplifier for a 12bit 500MS/sec pipeline ADC with digital calibration. A foreground ideal calibration test bench has been implemented in MATLAB to correct non-linearities of the amplifier up to the 5th order. A detailed comparison has been made between a class-A amplifier and a class-AB amplifier. Simulation results show that the class-AB amplifier outperforms the class-A amplifier in all performance aspects such as gain, bandwidth, linearity, noise and power consumption, except for the CMRR. A new class-AB amplifier topology has been proposed, which alleviates problems associated with the level shifting capacitors. Due to an insufficient accuracy of the proposed class-AB amplifier in order to save power, the residue output signal from the flip-around MDAC topology becomes distorted. To resolve this problem, the flip-around MDAC has been replaced by a simple charge amplifier MDAC topology. Timing scheme of the pipeline ADC has been modified due to remove the timing related problems and ISI. In addition, layout of the first stage MDAC has been done in TSMC 40nm CMOS technology. Post-layout simulations have shown an excellent Figure-of-Merit (FOM) of 8.08fJ/conv, at an ENOB of 10.8bit and signal bandwidth of 250MHz, which prove that the design is not only energy efficient, but also have a superior speed-resolution product.

Thesis Committee:

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Preface

This thesis presents the work I have done for my graduation project at Delft University of Technology and at Broadcom Netherlands BV as an intern. With this thesis, I will complete my master's degree program in Microelectronics at the Electrical Engineering, Mathematics and Computer Sciences (EEMCS) faculty of TU Delft. I would first like to thank my supervisor, Dr. Klaas Bult, for giving me the opportunity to do an internship in Broadcom and for his continuous support and encouragement during the thesis. I would also like to thank Prof.dr. J.R. Long for his valuable feedback.

This work would have been incomplete if I had not received support from an outstanding group of engineers in Broadcom Netherlands. My special thanks go to Rohan Sehgal, Frank van der Goes, Xiaodong Liu, who have provided me immense technical guidance. I had my first layout experience while doing the thesis and without the help of Xiadong Liu, Stefano Bozzola and Han Yan, it would not have been possible. I would like to thank Els van Zijl and Cora Gunsing, for all their administrative supports. With the utmost appreciation, my gratitude goes to the people mentioned above and others, in Broadcom Netherlands BV.

I would like to appreciate all my family members and friends, especially Adil and Marjana, for their great support and inspiration. Last but not the least, I would like to thank my parents Abdul and Aklima, and my wife Kashmiena; without them I would not have made so far.

Md. Shakil Akter
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July 2, 2012

Contents

List of Figures

List of Tables

Chapter 1

Introduction

Continuous scaling in technology has paved the way to enormous improvements of electronic systems over the past few decades. Higher device integration density, superior speed and reduced energy consumption per binary operation in fine line technologies have made it possible to implement highly complex systems using digital electronic circuits. For example, due to these developments in digital circuits, the performance of microprocessors have improved 1000 times over the past 15 years [1].

While moving towards fine line technologies provide increasingly better performance for digital circuits [1]; the design of analog circuits face several challenges [2]. With the technology scaling, the threshold voltage [2] of the transistors does not scale linearly with the supply voltage, resulting in less headroom for the signal swing, eventually leading to poor SNR. This also makes it difficult to use analog circuit techniques like cascoding and gain boosting [3] to achieve high loop gain. Moreover, the lower intrinsic gain of the transistor in modern technologies also adds to this problem, resulting in poor linearity.

The simultaneous requirements of meeting high speed with low noise and low distortion limit the analog circuits to take the full advantage of technology scaling. While matching, noise, and linearity restrain the analog signal processing accuracy [4], they are virtually absent in digital circuit design. Due to this as shown in [1], while the performance of digital circuits doubles every 1.5 years, the performance of analog-to-digital converters takes approximately 5 years to gain the same improvement. This continuous and increasing gap between the performance of analog and

digital circuit brings more attention towards delegating the analog domain problems to the digital domain, where they can be solved more efficiently.

1.1 Motivation

The analog-to-digital converter (ADC) is one of the few circuit blocks that cannot be implemented completely by digital circuits, as it interfaces "real life" analog signals like image, radio and speech with digital signal processor (DSP). Fast improvements in the digital circuits demand high speed, high precision interface devices which are normally not power efficient, and thus limit the throughput of the DSP based system. In spite of being a small portion of the whole system, the ADC consumes a significant portion of the allocated power and often restricts the achievable performance of the system. Moreover, trends toward portable electronic devices demands low power dissipation in analog-to-digital converters to enhance its battery life.

Among the key building blocks of the pipeline ADC, the residue amplifier is the most critical one that interfaces successive pipeline stages. Along with the ever growing demand of high operating speed, the amplifier has to also provide high dynamic range and high linearity, which is becoming an increasingly difficult task in deep submicron technologies. In order to meet these stringent performance criteria of speed-noise-linearity, the design of the amplifier most often becomes sub-optimal with regards to power consumption which is very critical for system-on-chip (SoC) integration [5].

The residue amplifier in a pipeline ADC suppresses the noise of the later stages of the pipeline ADC, thus reducing the accuracy requirements from those stages. However, it has to meet various precision requirements, such as noise, linearity and matching [4]. Pipeline ADCs published today typically place stringent design requirements on the residue amplifiers, often requiring a loop gain greater than $50dB$, a unity gain loop bandwidth approaching $1GHz$, and a SNDR of more than 10-bits, all while reducing power dissipation to a minimum. Among the various requirements that a residue amplifier has to meet, only noise is a fundamental problem that cannot be corrected in the digital domain. For the rest, digital assistance can be taken to relax the matching and linearity requirements from the amplifier; thus making the design only thermal noise limited. Since, high loop gain is not required

to suppress the non-linearity; a simple amplifier can be used as residue amplifier, which is not very accurate but provides better performance in terms of noise, speed and power consumption than a conventional high gain feedback amplifier.

Digital calibration and correction of analog domain non-idealities [6–9] is not a new idea. The problem of offset and unit element mismatch in pipeline ADCs have been overcome by different digital correction [6, 7, 10] and digital calibration [7–9] techniques. To extend the concept of digital calibration to correct for the analog domain non-linearities, Murmann et al. [5] have implemented a simple open loop residue amplifier and have showed 75% power savings on that compared to the conventional high gain feedback amplifier.

Therefore, the main research goal and subject of the thesis can be formulated as follows.

> *Design a low-power class-AB residue amplifier for a* $12bit$ $500MS/sec$ *pipeline ADC that is intended to be used with digital calibration. While treating linearity as a digital domain problem, the research motivation is to find out how far we can reduce the power consumption of the residue amplifier while maintaining the speed and noise requirements.*

1.2 Thesis Structure

The organization of the thesis is as follows: Chapter 2 revisits the basic operation of the pipeline ADC and its several design considerations. Chapter 3 aims at reviewing different topologies for multiplying analog-to-digital converters (MDACs) and residue amplifiers. Chapter 4 and 5 focuses on the design of the pipeline ADC. Chapter 4 proposes a new class-AB amplifier and describes the detail of the MDAC design which is the most important part of a pipeline stage. Chapter 5 illustrates the design of the first pipeline stage and also presents the ideal calibration scheme used during the design to calibrate for the non-linearities. Chapter 6 shows the simulation results of the first stage of the pipeline ADC and compares its performance with the state of the art. Chapter 7 gives a summary of our work and presents the possibilities of future research and development.

Chapter 2

Pipeline ADC Overview

This chapter gives a brief overview of the pipeline ADC. It explains the basic conversion principles of the pipeline ADC, and describes the digital correction and digital calibration scheme used in our design. The requirements on the residue amplifier in terms of the gain and the bandwidth have also been discussed.

2.1 System Architecture

The pipeline ADC is a popular form of multi-stage analog-to-digital converter in CMOS technology. It consists of a pipeline of several stages as shown in Figure 2.1, where each stage contains a coarse-ADC (CADC), a sub-DAC, a subtractor, and a residue amplifier, except for the last stage, which only contains a flash-type coarse-ADC. Sometimes it includes a dedicated sample and hold (S/H) circuit at the input of the pipeline ADC to reduce any timing or aperture error [11].

Normally, in every pipeline stage, either a S/H or a track and hold (T/H) circuit samples the value of the input signal, which is then coarsely quantized by the low resolution flash-type coarse-ADC to provide the digital codes $D_{out}(i)$. The sub-DAC uses this digital code to reconstruct the analog signal $V_{dac}(i)$, which is basically an estimation of the original analog signal $V_{in}(i)$. Subtraction of the $V_{dac}(i)$ from the $V_{in}(i)$ gives the residue input or the quantization error $V_{residue}(i)$ associated with the i-th pipeline stage. To keep the same input dynamic range for all the pipeline stages, the quantization error is multiplied with a gain of $2^{n_{i,eff}}$, where $n_{i,eff}$ is the effective number of bits resolved from the stage i. Please note that the

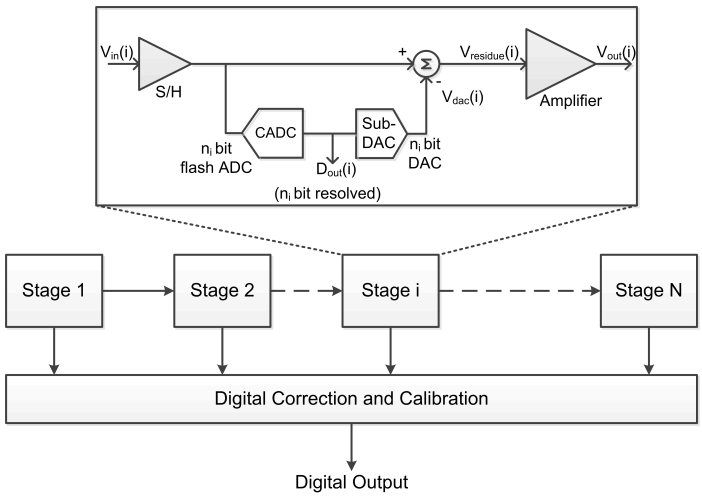


Figure 2.1: Pipeline ADC architecture

total number of bits resolved (n_i) from a pipeline stage could be different than the effective number of bits ($n_{i,eff}$) resolved from that stage. For example, the quantization error signal (residue input) and output of the residue amplifier (residue output) of a 2-bit pipeline stage are shown in Figures 2.2 and 2.3 respectively.

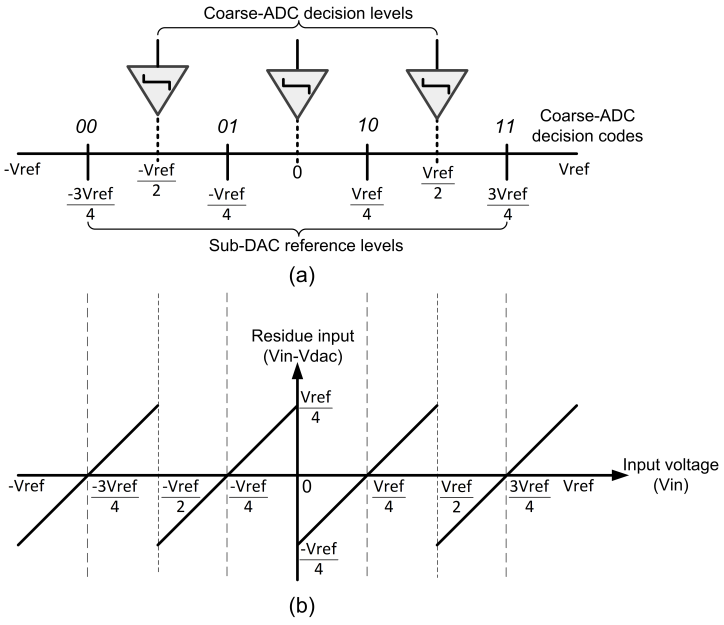


Figure 2.2: (a) Coarse-ADC and sub-DAC reference levels (b) Residue input or quantization signal of a 2-bit pipeline stage.

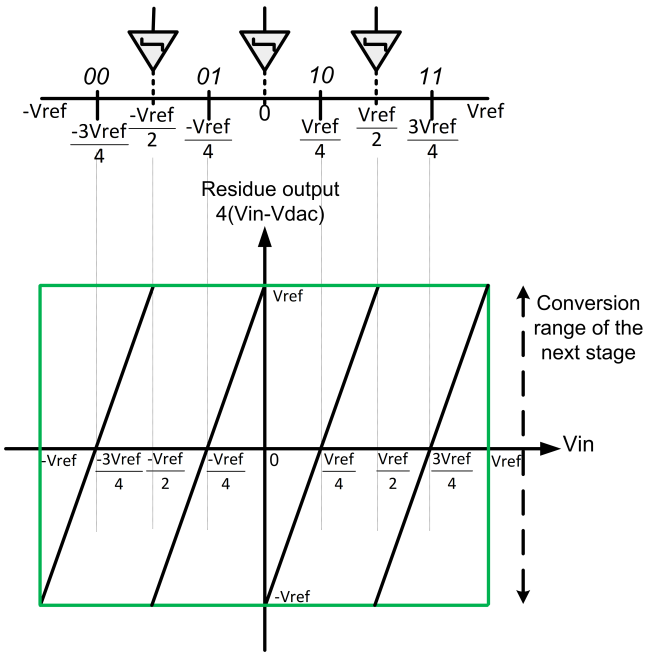


Figure 2.3: Residue output of the amplifier of a 2-bit pipeline stage.

The basic operation of a pipeline ADC is shown in Figure 2.4. While the first stage operates on the most recent input sample, the rest of the stages process or quantize the residue from the previous input samples. Each clock phase lasts for approximately half of the clock period ($\frac{T_s}{2}$); thus the time that the pipeline ADC takes (i.e., latency) to digitize an input sample becomes $n_{stage}\frac{T_s}{2}$, where T_s and n_{stage} are the duration of the clock period and the number of stages of the pipeline ADC respectively. In a pipeline ADC, all the stages can operate concurrently. While one stage amplifies its residue input signal, the next stage samples that amplified residue, which is later used in the succeeding quantization. As a result, the pipeline ADC can provide the same throughput as that of the flash ADC (convert one sample per period) while occupying much less die area [12].

Since the primary focus of our design is to design a low power residue amplifier for the pipeline ADC, we have simplified the pipeline ADC architecture in our simulations by assuming the back end to be ideal (i.e., infinite resolution). Figure 2.5 shows this simplified block diagram of the pipeline ADC containing only a single stage. Please note that for the proper operation of the pipeline ADC, it has to meet many static and dynamic performance parameters. For a comprehensive

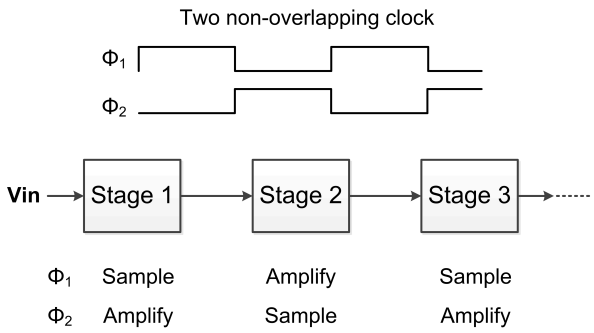


Figure 2.4: Simplified timing scheme of a pipeline ADC.

overview of the performance matrices or parameters, we refer to the textbooks on data converters [12, 13].

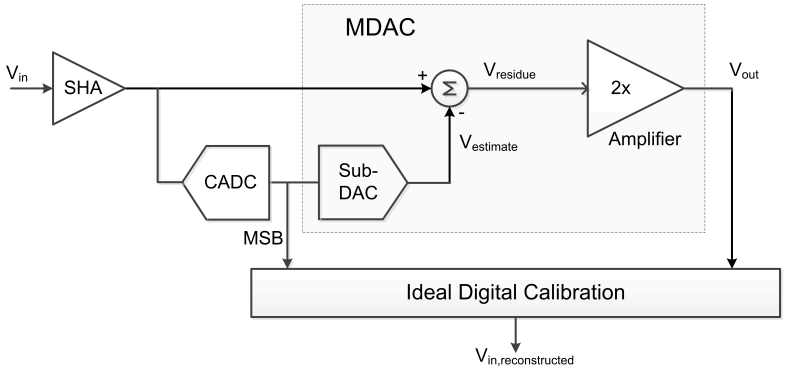


Figure 2.5: First stage of the pipeline ADC.

2.1.1 Digital Correction

Any non-ideality in the coarse-ADC such as comparator noise or comparator offset can saturate or overload the following pipeline stages as shown in Figure 2.6. This results in a significant error (more than $\pm\frac{1}{2}LSB$) in the conversion process and impairs the ADC transfer function. To overcome the requirement of accurate comparators, many techniques [6, 7, 10, 14] have been implemented; all aiming at adding redundancy in the coarse-ADC to keep the residue within the conversion range of the next stage [6, 7, 10] or to return the residue inside the full scale range (FSR) of the converter before it reaches the last stage [14].

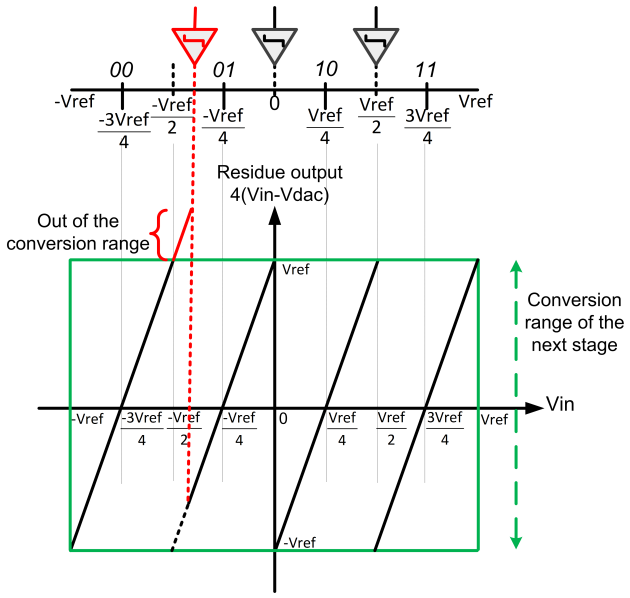


Figure 2.6: Sensitivity to the comparators level without any overrange

In order to incorporate redundancy to deal with the coarse-ADC non-idealities such as noise, offset, non-linearities, 1.5-bits per stage [10, 15] have been implemented in our design as shown in Figure 2.7. Although the number of bits resolved is only one, two comparators have been employed (i.e., three decision ranges, $n_{bits} = log_2(2+1) = 1.589$) to provide an overrange of $\frac{V_{ref}}{4}$. Due to this, if the decision level of the comparators of a pipeline stage move from its ideal position by no more than the allocated overrange $\frac{V_{ref}}{4}$, then the residue output signal of that stage remains within the conversion range of the following stage. This is graphically shown in Figure 2.8, where the decision level of the left comparator moves from its ideal position due to any offset or noise. However, as the change in the comparator threshold or decision level is less than the allocated overrange, the residue output signal is still within the conversion range of the next stage, and does not cause an error. Since the coarse-ADC output bits of the two subsequent pipeline stages overlap, arithmetic circuits are needed along with the shift registers in order to combine the digital bits of the pipeline stages. This is illustrated in Figure 2.9 for a four stage pipeline ADC, where the first three stages are 1.5-bit/stage and the last stage is a 3-bit flash ADC.

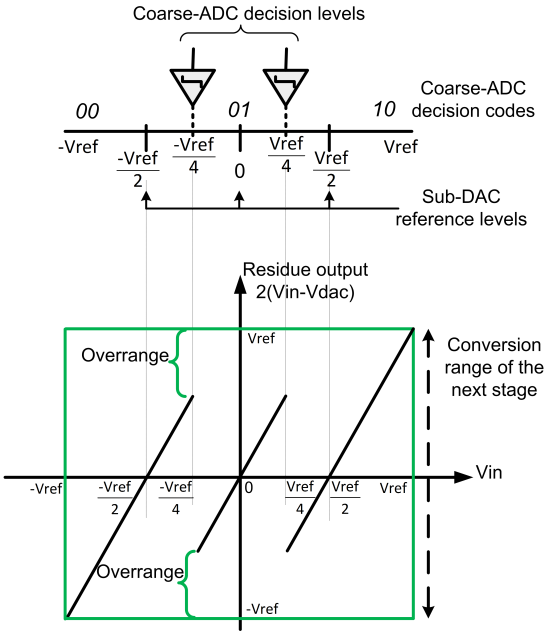


Figure 2.7: Residue output of 1.5bit per stage pipeline ADC.

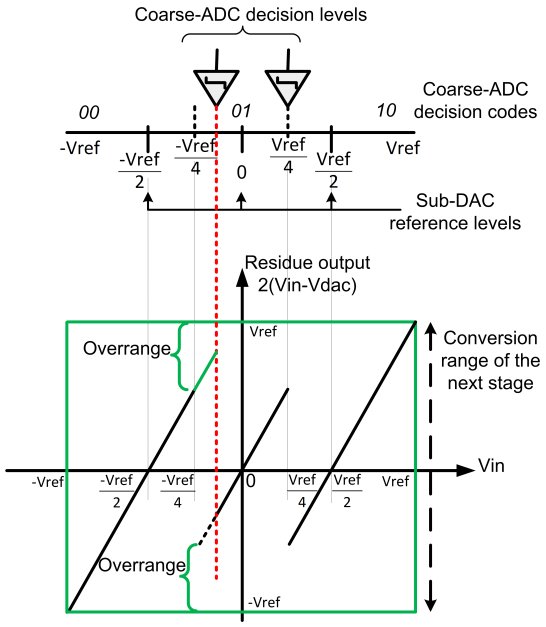


Figure 2.8: Effect of overrange in solving the comparator inaccuracy

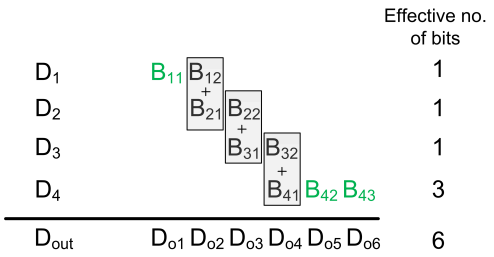


Figure 2.9: Combining the output bits of 1.5-bit/stage pipeline ADC stages.

2.1.2 Digital Calibration

Digital calibration helps to alleviate the analog domain requirements such as offset, matching, non-linearities, and correct for these inaccuracies in the digital domain at much lower power consumption and area, thus making the system more power efficient. Digital calibration schemes are mainly categorized in two groups: statistical [5] and deterministic [11]. Among them, deterministic calibration is faster as it operates on the error signal directly. Deterministic digital calibration can either be foreground [7] or background [8, 11, 16]. For our final design of the pipeline ADC, we have intended to use split-ADC [11, 17] deterministic background calibration, as it has already been implemented by a previous design [11] in MATLAB. In a pipeline split-ADC, the ADC is split into two identical half-ADCs. The average of outputs of the two half-ADCs gives the final ADC output code, whereas their difference gives a error signal that is utilized to calibrate the pipeline ADC. Please note that during this research, our main focus is to reduce the power consumption of the residue amplifier, and thus we have used a very simple but ideal foreground digital calibration scheme. This ideal digital calibration scheme is described in the next section. Moreover, we have focused on one half of the pipeline split-ADC.

Ideal Digital Calibration

The ideal digital calibration works as a tool to verify how much improvement in linearity can be brought by doing the digital calibration perfectly. Figure 2.10 shows the block diagram of the proposed ideal digital calibration scheme. We split the digital calibration in two phases: (1) calibration phase: provide a known and accurate signal at the input and characterize the first stage of the pipeline ADC by

building a look-up table or transfer curve , (2) test phase: reconstruct the unknown input signal by using the output of the first stage, the coarse-ADC decision, and the look-up table from the calibration phase.

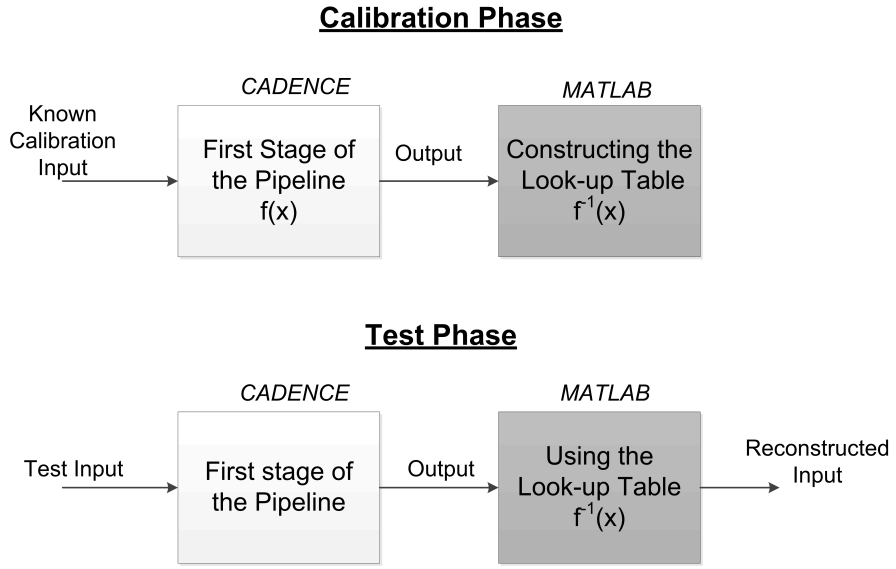


Figure 2.10: Block diagram of the ideal digital calibration scheme.

Figure 2.11 shows graphically how the digital calibration works. We provide a known and accurate ramp input signal to characterize the first pipeline stage (i.e., 1.5-bit per stage) during the calibration phase. It is similar to build a look-up table for the input-output transfer. The input-output transfer curve should contain all the non-linearities, associated with that stage. Now, we can derive an inverse transfer function (i.e., output-input transfer) from the look-up table that will be used in the test phase. During the test phase, we get an output signal in response to an unknown input signal. Now, we can use the inverse transfer function to reconstruct the input signal from the output signal, but it might have three possibilities (i.e., three sub-ranges), as shown in Figure 2.11 by the blue arrows. Finally, depending on the decision of the coarse ADC (i.e., MSB bit), the proper sub-range can be easily selected and the correct input signal is reconstructed.

Please note that this ideal digital calibration works perfectly as long as the system (i.e., the first stage of the pipeline ADC) remains exactly the same during both the calibration phase and the test phase. To accomplish this, we have temporarily

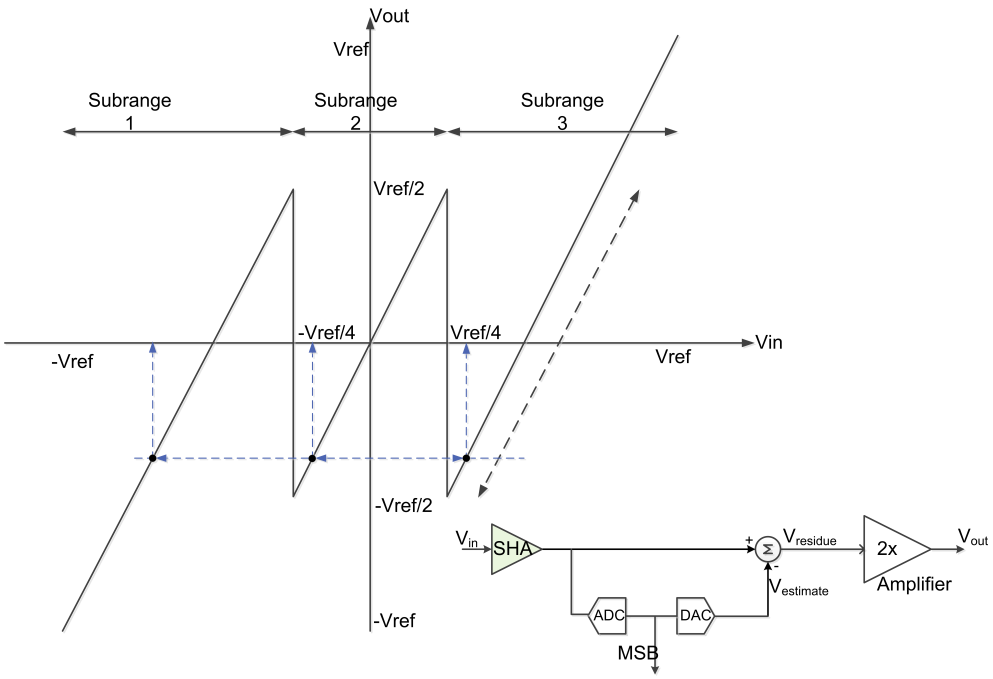


Figure 2.11: Graphical representation of the ideal digital calibration scheme.

used an ideal S/H at the input of the pipeline ADC while using this ideal digital calibration scheme.

2.2 Design Requirements of the Residue Amplifier

The residue amplifier of the pipeline stages needs to provide precise amplification unless assisted by any error correction mechanisms. A popular way of achieving precise amplification is to implement a high gain amplifier in negative feedback, as shown in Figure 2.12. The amplifier also needs to be very fast to amplify the signal to the correct level within the specified amplification time. Insufficient gain (A) or loop gain ($A\beta$), and insufficient speed of the amplifier result in errors in the signal amplification. These errors in amplification can be decoupled in two parts: (1) errors resulting from finite gain (static error) and (2) errors resulting from finite speed or bandwidth (dynamic error). The following section discusses more about these two errors in amplification.

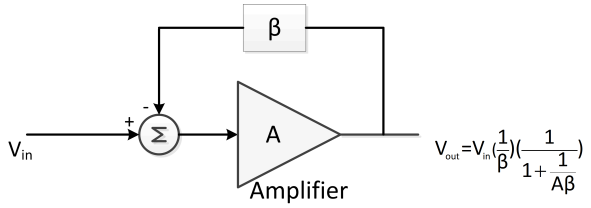


Figure 2.12: High gain amplifier in negative feedback.

2.2.1 Static Gain Error

If the residue amplifier has infinite gain and infinite bandwidth, then the overall gain of the system is completely determined by the feedback elements, which are normally very accurate [18]. In the following analysis, we have assumed that the residue amplifier has finite loop gain (LG), but infinite bandwidth (BW) so that it can respond to any input signal infinitely fast. To observe the effects of the amplifier gain limitation, an inverting amplifier configuration is considered, as shown in Figure 2.13, where $V_{in1} = V_{in}(1-\beta)$. The closed loop gain of such an amplifier is given by

$$\begin{aligned} V_{out} &= V_{in1}\,(\frac{1}{\beta})\,(\frac{1}{1+\frac{1}{A\beta}}) \\ &= V_{in}\,(1-\beta)\,(\frac{1}{\beta})\,(\frac{1}{1+\frac{1}{A\beta}}) \\ &= V_{in}\,\underbrace{(\frac{1-\beta}{\beta})}_{\text{ideal gain}}(\frac{1}{1+\underbrace{\frac{1}{A\beta}}_{\text{finite LG}}}) \end{aligned} \tag{2.1}$$

where β is called the feedback factor. The absolute error ε_{static} in the output voltage due to the finite gain of the amplifier can be expressed as in Equation 2.2.

$$\begin{aligned}
\varepsilon_{static} &= V_{out(ideal)} - V_{out} \\
&= V_{in}\,(\frac{1-\beta}{\beta}) - V_{in}\,(\frac{1-\beta}{\beta})\,(\frac{1}{1+\frac{1}{A\beta}}) \\
&= V_{in}\,(\frac{1-\beta}{\beta})\,(\frac{1}{1+A\beta}) \qquad (2.2)
\end{aligned}$$

Hence, the relative static gain error Δ_{static} is given by

$$\begin{aligned}
\Delta_{static} &= \frac{\varepsilon_{static}}{V_{out(ideal)}} \\
&= \frac{V_{in}\,(\frac{1-\beta}{\beta})\,(\frac{1}{1+A\beta})}{V_{in}\,(\frac{1-\beta}{\beta})} \\
&= \frac{1}{1+A\beta} \approx \frac{1}{A\beta} \qquad (2.3)
\end{aligned}$$

Equation (2.3) shows that Δ_{static} approaches zero when the loop gain of the amplifier reaches to infinity ($A\beta \to \infty$). The step response of the residue amplifier that has finite gain but infinite bandwidth can be graphically shown in Figure 2.14.

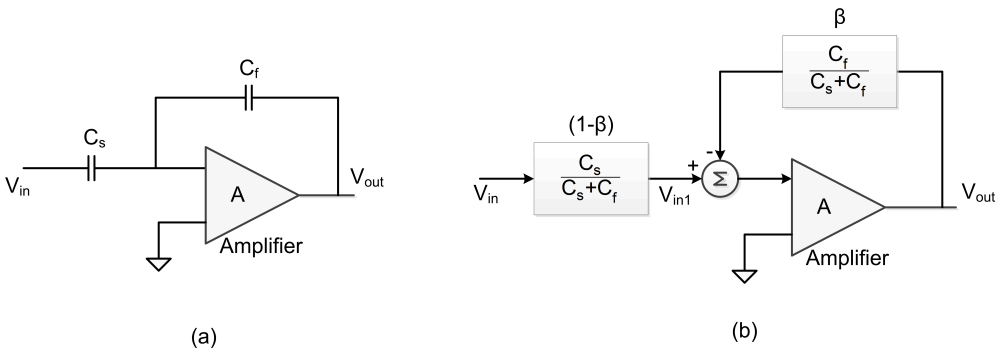


Figure 2.13: (a) Inverting amplifier configuration (b) Representation in block diagram as in Figure 2.12

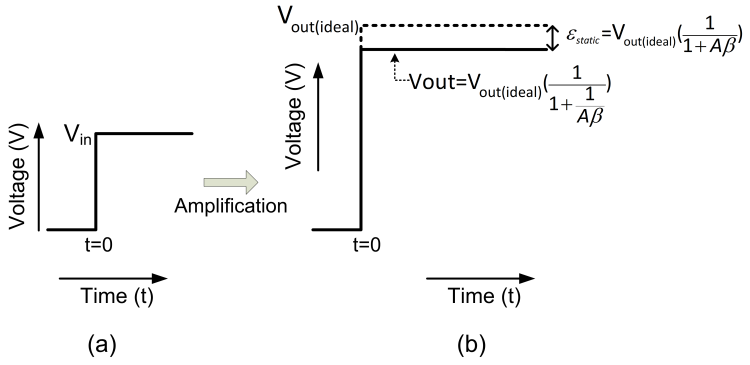


Figure 2.14: Step response of the amplifier having finite gain but infinite bandwidth.

2.2.2 Dynamic Gain Error

Dynamic gain error arises from the fact that the amplifier cannot respond infinitely fast to a given input signal. In other words, the amplifier requires finite amount of time to amplify the input signal to the desired level. In this section, we consider only the effects of the finite bandwidth (BW) of the amplifier, assuming that the amplifier has infinite gain. Considering the amplifier in Figure 2.13 as a single pole system, the output voltage V_{out} of the amplifier in response to a step input can be expressed as

$$V_{out}(t) = V_{in}\,(\underbrace{\frac{1-\beta}{\beta}}_{\text{ideal gain}})\,(1-\underbrace{\exp^{-t/\tau}}_{\text{BW limitation}}) \tag{2.4}$$

where τ is the time constant of the circuit of Figure 2.13 assuming dominant single pole response, given by

$$\tau = \frac{1}{\omega_{-3dB}} \approx \frac{1}{\beta\omega_u} \tag{2.5}$$

where ω_{-3dB} and ω_u are the -3dB bandwidth and unity gain bandwidth of the amplifier respectively. The absolute dynamic error $\varepsilon_{dynamic}(t)$ in the output voltage of the amplifier can be expressed as in Equation 2.6.

$$\begin{aligned}\varepsilon_{dynamic}(t) &= V_{out(ideal)} - V_{out}(t) \\ &= V_{in}\,(\frac{1-\beta}{\beta}) - V_{in}\,(\frac{1-\beta}{\beta})\,(1-\exp^{-t/\tau}) \\ &= V_{in}\,(\frac{1-\beta}{\beta})\,(\exp^{-t/\tau}) \end{aligned} \tag{2.6}$$

So, the relative dynamic error $\Delta_{dynamic}(t)$ is given by

$$\begin{aligned}\Delta_{dynamic}(t) &= \frac{\varepsilon_{dynamic}(t)}{V_{out(ideal)}} \\ &= \frac{V_{in}\,(\frac{1-\beta}{\beta})\,(\exp^{-t/\tau})}{V_{in}\,(\frac{1-\beta}{\beta})} \\ &= \exp^{-t/\tau} \end{aligned} \tag{2.7}$$

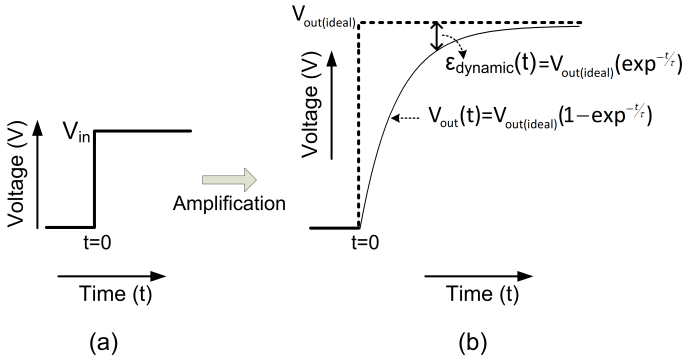


Figure 2.15: Step response of the amplifier having finite bandwidth but infinite gain.

Equation (2.7) shows that $\Delta_{dynamic}(t)$ approaches zero if $t \to \infty$ or $\tau \to 0$. In a pipeline ADC, the amplification time (t) is approximately half of the clock period, $t \approx \frac{T_s}{2} = \frac{1}{2f_s}$, where f_s is the clock frequency or the sampling frequency of the pipeline ADC. So, in order to reduce the relative dynamic error $\Delta_{dynamic}$, we need to make the time constant (τ) lower, which is actually the same as to increase the unity-gain bandwidth ω_u of the amplifier.

2.2.3 Total Gain Error

If we consider that the amplifier have finite gain (static error) and finite bandwidth (dynamic error), then the output voltage of the amplifier can be expressed as

$$V_{out}(t) = V_{in}(\frac{1-\beta}{\beta})(\frac{1}{1+\frac{1}{A\beta}})(1-\exp^{-t/\tau}) \tag{2.8}$$

Due to the finite loop gain and finite bandwidth of the residue amplifier, absolute total error $\varepsilon_{total}(t)$ in the output voltage can be expressed as

$$\begin{aligned} \varepsilon_{total}(t) &= V_{out(ideal)} - V_{out}(t) \\ &= V_{in}(\frac{1-\beta}{\beta}) - V_{in}(\frac{1-\beta}{\beta})(\frac{1}{1+\frac{1}{A\beta}})(1-\exp^{-t/\tau}) \\ &= V_{in}(\frac{1-\beta}{\beta})(\frac{1}{1+A\beta}+\frac{\exp^{-t/\tau}}{1+\frac{1}{A\beta}}) \end{aligned} \tag{2.9}$$

and the relative total error $\Delta_{total}(t)$ is given by

$$\begin{aligned} \text{and, } \Delta_{total}(t) &= \frac{\varepsilon_{total}(t)}{V_{out(ideal)}} \\ &= \frac{1}{1+A\beta}+\frac{\exp^{-t/\tau}}{1+\frac{1}{A\beta}} \\ &\approx \underbrace{\frac{1}{A\beta}}_{static\ part} + \underbrace{\exp^{-t/\tau}}_{dynamic\ part} \quad [\text{if } A\beta \gg 1] \end{aligned} \tag{2.10}$$

Figure 2.16 graphically shows the absolute total error $\varepsilon_{total}(t)$ of the residue amplifier. If the amplifier should keep the error less than $\frac{1}{2}$ LSB at an accuracy level of N-bit (relative LSB value = $\frac{1}{2^N}$), then the total relative error $\Delta_{total}(t)$ in the output voltage of the amplifier has to meet the following constraint:

$$\Delta_{total}(t) \leq \frac{1}{2}\times\frac{1}{2^N} \tag{2.11}$$

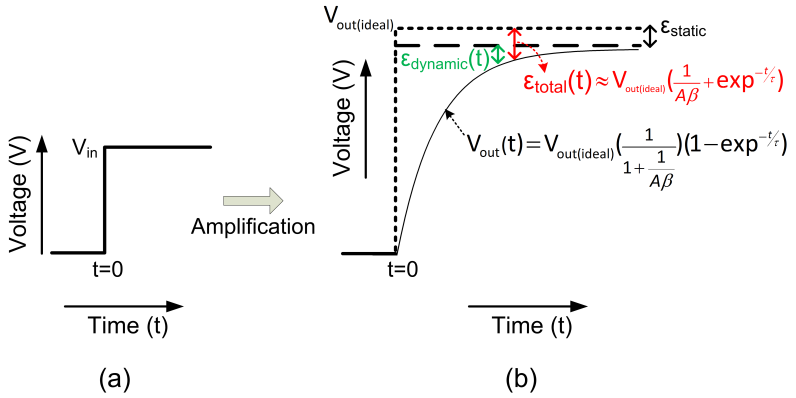


Figure 2.16: Step response of the amplifier having finite gain and finite bandwidth.

In order to find the required amplifier gain (A) and the unity-gain frequency (f_u), we can do an error budgeting. For instance, 50% of the $\Delta_{total}(t)$ is allocated to the Δ_{static} and the rest is allocated to the $\Delta_{dynamic}(t)$. Please note that, the loop gain of the amplifier is typically made very high in order to reduce the static gain error, so that we can allow comparatively larger error due to the bandwidth limitation. The reason behind this can be stated as follows: bandwidth of the amplifier is directly proportional to the transconductance (g_m) of the amplifier and thus to the power consumption; whereas making high loop gain arguably does not require a lot of power. The required amplifier gain (A) can be found from the Δ_{static} requirement as follows:

$$\begin{aligned} \Delta_{static} &= \frac{1}{2} \times \Delta_{total} \leq \frac{1}{2} \times \frac{1}{2} \times \frac{1}{2^N} \\ or, \frac{1}{A\beta} &\leq \frac{1}{2^{(N+2)}} \\ or, A &\geq \frac{2^{(N+2)}}{\beta} \end{aligned} \tag{2.12}$$

Similarly the required unity-gain frequency (f_u) of the amplifier can be derived from the $\Delta_{dynamic}(t)$ as shown in Equation 2.13.

$$\begin{aligned} \Delta_{dynamic}(t) &= \exp^{-t/\tau} \leq \frac{1}{2^{N+2}} \\ or, \frac{t}{\tau} &\geq (N+2)\ln 2 \end{aligned} \tag{2.13}$$

Assuming $t \approx \frac{1}{2f_s}$ and using Equation (2.5), we can express Equation (2.13) as

$$\begin{aligned} \frac{\frac{1}{2f_{clk}}}{\frac{1}{\beta(2\pi f_u)}} &\geq (N+2)\ln 2 \\ or, f_u &\geq \frac{(N+2)f_{clk}\ln 2}{\pi\beta} \end{aligned} \tag{2.14}$$

For example, assume the amplifier is operating in a system with $f_s = 500MHz$ and $\beta = \frac{1}{3}$ (i.e., ideal closed loop gain of 2 in Figure 2.13), and needs to achieve an accuracy of 12-bit. Then the required gain (A) and the required unity-gain frequency (f_u) of the amplifier can be found from Equations (2.12) and (2.14) respectively as

$$\begin{aligned} A &\geq 93.8dB \\ f_u &\geq 4.6GHz \end{aligned}$$

Please note that the amplifier will require higher A and higher f_u, when the accuracy requirement (i.e., the number of bits, N) is increased, as can also be seen from the Equations (2.12) and (2.14) respectively.

Slew rate Normally an amplifier slews, when the drive current reaches to the maximum current that the amplifier can deliver. This is due to the fact that either the input voltage or the signal frequency is too big [19]. In this situation, the output voltage begins to change at a constant maximum rate (i.e., slew rate) and does not depend on the input signal anymore.

Slew rate can be expressed as [19] -

$$SR = \frac{dV}{dt} = \frac{I_{max}}{C_L}$$

In case of a class-A amplifier with a tail current source, the biasing current (i.e., the tail current) has to be sufficiently big to avoid slewing. However, in our design, the residue amplifier that has been implemented is a push-pull type class-AB amplifier. Since the amplifier can deliver any amount of current to charge or discharge the load capacitor, it does not slew. For a detailed overview of the slew rate problem, we refer to the following textbook [20] on analog circuit design.

2.3 Summary

In this chapter, a brief overview of the pipeline ADC operation has been described. Comparator non-idealities have been resolved by introducing redundancy or over-range in 1.5-bit/stage topology. The ideal digital calibration scheme used during the design phase of the residue amplifier has been discussed. The requirements on the residue amplifier gain and the amplifier unity-gain frequency in order to achieve a specific bit-accuracy have been derived.

Chapter 3

Topology Choices

This chapter elaborates the various topologies that have been reviewed during the research. Different MDAC and residue amplifier topologies are shown and their basic operations have been explained. Also, several comparisons have been made to show the relative performance of different MDACs and different amplifiers.

3.1 MDAC Topologies

This section describes the open-loop and the closed-loop MDAC topologies. Among the different closed-loop MDAC topologies, flip-around MDAC topology and charge amplifier MDAC topology have been discussed.

3.1.1 Open-loop MDAC Topology

Recently, there have been many efforts in reducing the precision requirements [4, 5, 21] from the residue amplifier and transfer it to the digital domain. Using an open-loop MDAC topology is one of them, where the amplifier is in the open-loop [5]. Since there is no loading from the feedback capacitor, the bandwidth of the open-loop amplifiers should be slightly higher than the closed-loop amplifiers for a fixed overall gain. Moreover, in an open-loop topology, both the amplifier noise and the signal sees the same gain, therefore should result in a slightly better SNR. Please note that for a closed-loop amplifier topology, the amplifier noise voltage is at the virtual ground of the amplifier. Thus, it transfers to the output of the amplifier with

a higher gain (i.e., 1+ closed-loop signal gain) compared to the input signal. Normally an open-loop amplifier topology is stable because there are no closed-loop to create potential instability. Though in our design, the stability of the amplifier is not very critical, because the amplifier that has been used is a single stage amplifier. All of the above observations indicate towards having a lower power consumption in the open-loop residue amplifier, which is the main motivation of our work. Figure 3.1 shows a single-ended circuit for the open-loop MDAC.

The drawback open loop MDAC topology is that the gain is not stable. Since there is no loop gain to suppress the non-linearity, the linearity performance of this topology is very poor and might be intolerable, even after doing extensive digital calibration, which also demands power.

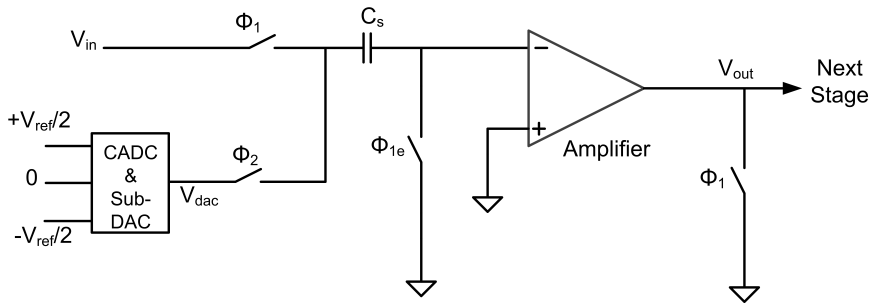


Figure 3.1: Single-ended open-loop MDAC topology.

3.1.2 Closed-loop MDAC topologies

In the closed-loop MDAC topologies, the loop gain helps to suppress the non-linearity and makes the gain more predictable. Compared to an open-loop MDAC topology, the bandwidth and the SNR of a closed-loop MDAC topologies should be slightly lower, as also been discussed in the last section. In this section, we discuss the two closed-loop MDAC topologies.

Flip-around MDAC topology

In the flip-around MDAC topology, both the sampling capacitor (C_s) and the feedback capacitor (C_f) are used to sample the input signal (V_{in}). Figure 3.2 shows a single-ended schematic of the flip-around MDAC. It operates on two phases, which

are the sampling phase (ϕ_1) and the amplification phase (ϕ_2). Figure 3.3 shows the flip-around MDAC in both ϕ_1 and ϕ_2.

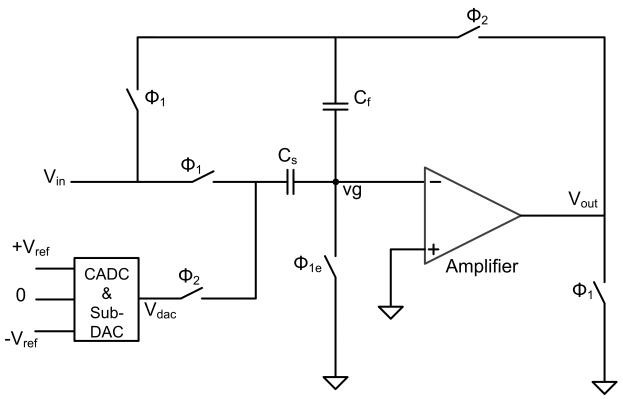


Figure 3.2: Flip-around MDAC topology.

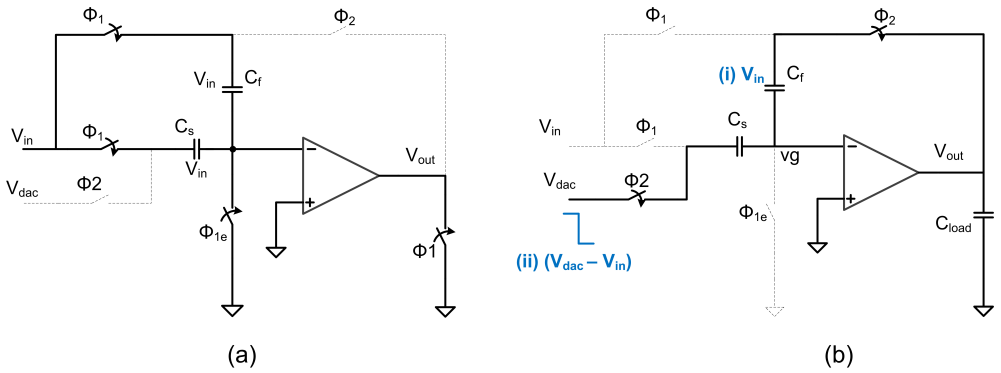


Figure 3.3: Flip-around MDAC during (a) the sampling phase, ϕ_1 and (b) the amplification phase, ϕ_2.

During ϕ_1, V_{in} is sampled across both the C_s and the C_f. In this phase, the amplifier is reset to the desired common mode voltages. During ϕ_2, the input terminal of the MDAC gets a reference value (V_{dac}) from the sub-DAC. This reference gets subtracted from the V_{in} that has been sampled during the ϕ_1. For 1.5-bit per pipeline stage, V_{dac} can have one of the three values ($V_{ref}, 0, -V_{ref}$) in case of the flip-around MDAC. During ϕ_2, the amplifier is connected in the feedback configuration, and the charge stored on the C_s is forced to transfer to the C_f by the amplifier to make the node vg virtual ground. From Figure 3.3(b), we can see the following two inputs during ϕ_2: (i) flip-around input (V_{in}) that is stored across C_f from ϕ_1

and (ii) residue input ($V_{dac} - V_{in}$) that is the step at the input of MDAC. The output voltage of the MDAC at the end of the ϕ_2 can be calculated by combining the individual transfer of each input to the output.

Flip-around input ideally transfers to the output with a gain of 1. But, there is some gain error due to the finite loop gain (static error) and finite bandwidth (dynamic error) of the amplifier, as been described in Section 2.2. Similar to Equation (2.8), the output voltage of the flip-around MDAC in response to this input can be expressed as

$$V_{out1} = xV_{in} + (1-x)V_{in}(1-\exp^{-t/\tau})(\frac{1}{1+\frac{1}{A\beta}})gain_1 \tag{3.1}$$

where x is the fraction of the flip-around input that feeds through to the output just at the beginning of the ϕ_2 and $gain_1 = 1$, which is the ideal gain of the flip-around input to the output.

Residue input ideally transfers to the output with a gain defined by the capacitor ratio $\frac{C_s}{C_f}$. However, again due to the finite loop gain and finite bandwidth of the amplifier, overall gain deviates from the ideal value . Note that there is also a feed through component at the output due to the residue input but for simplicity, we ignore that part in this analysis. So, the output of the flip-around MDAC in response to the residue input is given by

$$V_{out2} = -(V_{dac} - V_{in})(1-\exp^{-t/\tau})(\frac{1}{1+\frac{1}{A\beta}})gain_2 \tag{3.2}$$

where $gain_2$ = ideal gain of the residue input to the output = $\frac{1-\beta}{\beta} \approx \frac{C_s}{C_f}$

In ideal case, the residue amplifier has infinite gain and infinite bandwidth. Thus, both the $(1-\exp^{-t/\tau})$ and the $(\frac{1}{1+\frac{1}{A\beta}})$ terms become 1. From this, we can compute the total output voltage in ideal situation as

$$V_{out1} = xV_{in} + (1-x)V_{in} = V_{in} \quad \text{[From Equation (3.1)]}$$

$$V_{out2} \quad = \quad -(V_{dac} - V_{in})\frac{C_s}{C_f} \quad \text{[From Equation (3.2)]}$$

Now, the total output voltage V_{out} is

$$\begin{aligned} V_{out} &= V_{out1} + V_{out2} \\ &= V_{in}(1 + \frac{C_s}{C_f}) - V_{dac}(\frac{C_s}{C_f}) \end{aligned} \tag{3.3}$$

If $C_s = C_f$, then equation 3.3 resolves to

$$\begin{aligned} V_{out} &= 2V_{in} - V_{dac} \\ &= 2(V_{in} - \frac{V_{dac}}{2}) \end{aligned} \tag{3.4}$$

Depending on the input voltage sampled by the coarse ADC during ϕ_1, sub-DAC gives one of the three reference voltages $(-V_{ref}, 0, V_{ref})$ as the V_{dac} value. So, V_{out} can be expressed as

$$V_{out} = \begin{cases} 2(V_{in} + \frac{V_{ref}}{2}) & \text{if } V_{in} \leq -\frac{V_{ref}}{4} \\ 2V_{in} & \text{if } -\frac{V_{ref}}{4} \leq Vin \leq \frac{V_{ref}}{4} \\ 2(V_{in} - \frac{V_{ref}}{2}) & \text{if } Vin \geq \frac{V_{ref}}{4} \end{cases} \tag{3.5}$$

One advantage of the flip-around MDAC is that it offers higher feedback factor (β) to achieve a particular closed-loop gain. For example, in order to have a closed-loop gain of 2, β is $\frac{1}{2}$ for the flip-around MDAC compared to $\frac{1}{3}$ in case of the charge amplifier MDAC. Thus, the flip-around MDAC exhibits higher bandwidth than the charge amplifier MDAC.

Charge amplifier MDAC topology

In the charge amplifier MDAC topology, only the C_s is used during the ϕ_1 to sample the input signal V_{in} rather than both the C_s and the C_f in case of the flip-around MDAC topology. As a result, β is lower for a particular closed-loop gain and so is the bandwidth. Figure 3.4 shows the basic topology of the charge amplifier MDAC.

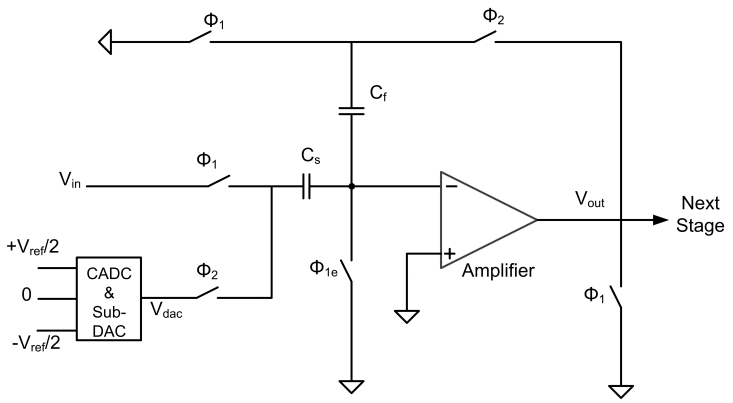


Figure 3.4: Single-ended charge amplifier MDAC topology.

Figure 3.5 shows the charge amplifier MDAC during the ϕ_1 and the ϕ_2 phase. During the ϕ_1 phase as shown in Figure 3.5(a), the input voltage (V_{in}) is sampled on the C_s. During the ϕ_2 phase as shown in Figure 3.5(b), the amplifier is connected in feedback and a reference voltage is given to the input of the MDAC by the sub-DAC . We can also see from Figure 3.5(b) that the charge amplifier MDAC has only one input (residue input), which gets amplified to the output during ϕ_2. Thus, the output voltage of the charge amplifier MDAC can be expressed as

$$V_{out} = -(V_{dac} - V_{in})(1 - \exp^{-t/\tau})(\frac{1}{1 + \frac{1}{A\beta}})gain \tag{3.6}$$

where $gain = \dfrac{1-\beta}{\beta} \approx \dfrac{C_s}{C_f}$. For infinite loop gain and bandwidth, Equation (3.6) resolves to

$$\begin{aligned} Vout &= (V_{in} - V_{dac})\frac{C_s}{C_f} \\ &= 2(Vin - Vdac) \qquad [\text{if } C_s = 2C_f] \end{aligned} \tag{3.7}$$

Please note that for the charge amplifier MDAC, the references $(\frac{V_{ref}}{2}, 0, \frac{-V_{ref}}{2})$ provided by the sub-DAC are different, compared to the flip-around MDAC. Thus, V_{out} of the charge amplifier MDAC can be expressed as in Equation 3.8.

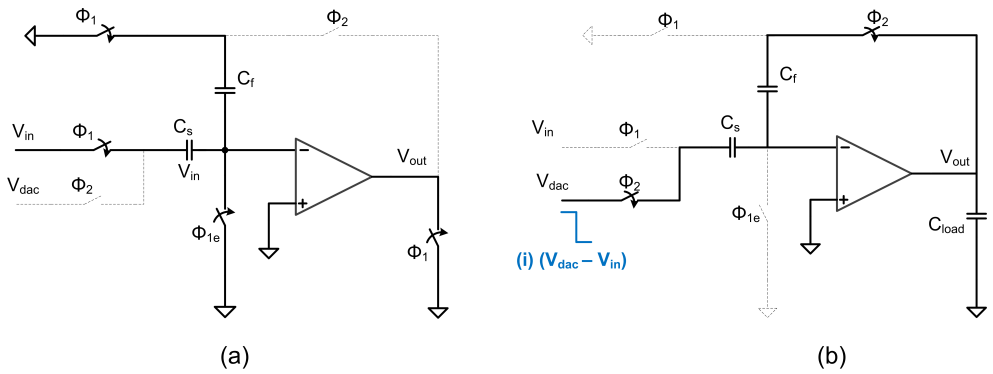


Figure 3.5: Charge amplifier MDAC in a) the sampling phase, ϕ_1 and in b) the amplification phase, ϕ_2.

$$V_{out} = \begin{cases} 2(V_{in} + \frac{V_{ref}}{2}) & \text{if } V_{in} \leq -\frac{V_{ref}}{4} \\ 2V_{in} & \text{if } -\frac{V_{ref}}{4} \leq Vin \leq \frac{V_{ref}}{4} \\ 2(V_{in} - \frac{V_{ref}}{2}) & \text{if } Vin \geq \frac{V_{ref}}{4} \end{cases} \tag{3.8}$$

which is exactly the same as that of the flip-around MDAC topology. The difference lies in the reference values of the sub-DAC, and the capacitor ratio used to reach a closed-loop gain of 2.

3.2 Thermal Noise Analysis

In the thermal noise perspective, there is arguably no difference between the flip-around MDAC and the charge amplifier MDAC. This is because for the noise analysis we can assume that $V_{in} = 0$, i.e., the input terminal of the MDAC is connected to a common mode voltage V_{cm}. During the sampling phase ϕ_1, switches that are on produce noise. At the end of ϕ_1, those switches are turned off. Since it is a sampling event, all the noise of the switches fold back to the first Nyquist band (i.e., the frequency band upto $\frac{f_s}{2}$). As a result, noise power sampled across the C_s and the C_f becomes $\frac{kT}{C_s}$ and $\frac{kT}{C_f}$ respectively, irrespective of the MDAC topologies. Figure 3.6 shows the noise sources of both the closed-loop MDAC topologies during ϕ_1.

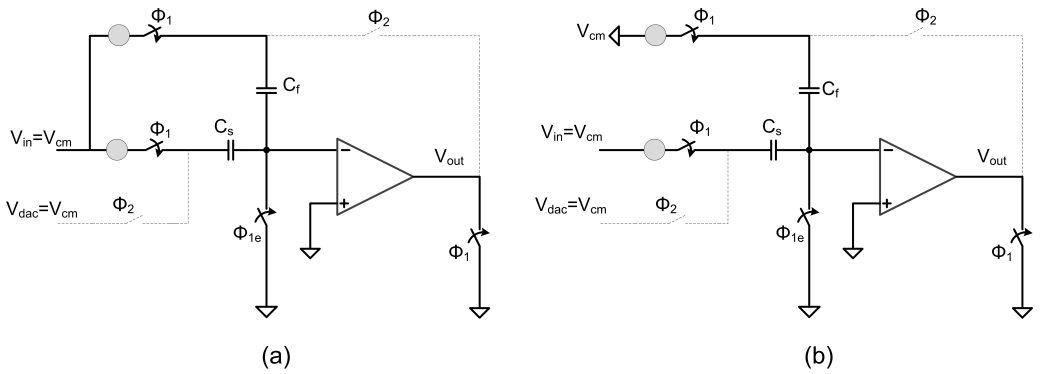


Figure 3.6: Noise sources of (a) the flip-around MDAC, and (b) the charge amplifier MDAC topologies during ϕ_1.

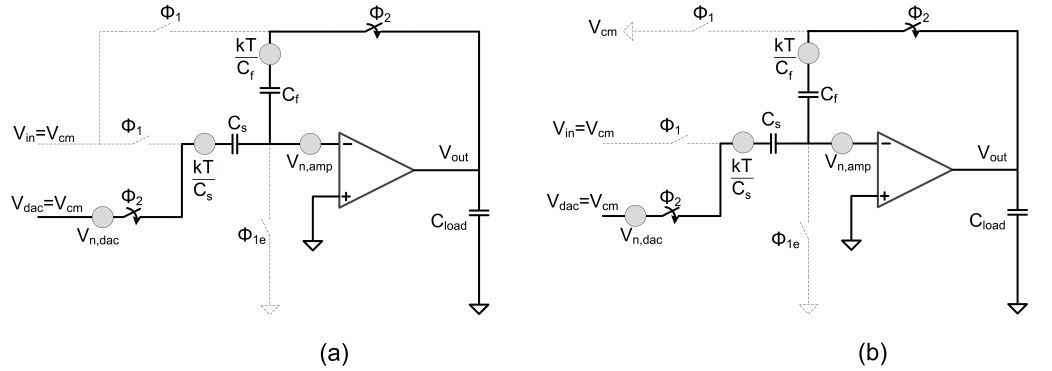


Figure 3.7: Noise transfer during ϕ_2 of (a) the flip-around MDAC, and (b) the charge amplifier MDAC.

During ϕ_2, the amplifier is connected in feedback and the sampled noise charge on C_s transfers to the output. Figure 3.7 shows the different noise contributors of both the closed-loop MDAC topologies during $\phi 2$. While the $\frac{kT}{C_f}$ noise component is already at the output, the $\frac{kT}{C_s}$ noise and the sub-DAC noise ($V_{n,dac}$) components have to transfer to the output with a gain given by $\frac{C_s}{C_f}$. The amplifier noise ($V_{n,amp}$) also transfers to the output, but with a higher gain $(1+\frac{Cs}{Cf})$. The total integrated output noise power of both the closed-loop MDACs at the end of the ϕ_2 can be expressed as

$$V_{n,out}^2 = \frac{kT}{C_f} + (\frac{kT}{C_s} + V_{n,dac}^2)(\frac{C_s}{C_f})^2 + V_{n,amp}^2(1+\frac{Cs}{Cf})^2 \tag{3.9}$$

If only the noise components from the sampling phase are considered (i.e., ignoring $V_{n,dac}$ and $V_{n,amp}$), Equation (3.9) becomes

$$V_{ns,out}^2 = \frac{kT}{C_f} + (\frac{kT}{C_s})(\frac{C_s}{C_f})^2 \tag{3.10}$$

3.2.1 SNR comparison

We have already derived the expressions of the integrated output noise power for both the closed-loop MDAC topologies in Section 3.2. In this section, we will calculate and compare the signal-to-noise (SNR) ratio of the flip-around MDAC and the charge amplifier MDAC.

Flip-Around MDAC Topology In order to calculate the SNR, we need to derive the expression for the output signal power of the MDAC. Ideally, the flip-around MDAC topology has a closed-loop gain of $(1 + \frac{C_s}{C_f})$ as shown in Equation (3.3). Therefore, the output signal power of the flip-around MDAC by the end of ϕ_2 can be written as

$$V_{out}^2 = (1 + \frac{C_s}{C_f})^2 V_{in}^2 \tag{3.11}$$

Therefore, the SNR of the flip-around MDAC can calculated by taking the ratio of the signal power of Equation (3.11) and the noise power of Equation (3.9) as

$$SNR_{FA} = 10\log(\frac{(1 + \frac{C_s}{C_f})^2 V_{in}^2}{\frac{kT}{C_f} + (\frac{kT}{C_s} + V_{n,dac}^2)(\frac{C_s}{C_f})^2 + V_{n,amp}^2(1 + \frac{C_s}{C_f})^2}) \tag{3.12}$$

For the ease of the SNR comparison between the flip-around MDAC and charge amplifier MDAC topologies, we have ignored $V_{n,dac}$ and $V_{n,amp}$ noise components, and also the $10\log$ factor. As a result of these considerations, the output noise power only consists of noise contributions from the sampling phase (ϕ_1), as given in Equation (3.10). The simplified SNR is stated in Equation (3.13), which shows that the SNR of the flip-around MDAC is always fixed for a given $(C_s + C_f)$, irrespective

of the closed-loop gain (i.e., $\frac{C_s}{C_f}$).

$$\begin{aligned} SNR_{FA,simplified} &= \frac{(1+\frac{C_s}{C_f})^2 V_{in}^2}{\frac{kT}{C_f}+(\frac{kT}{C_s})(\frac{C_s}{C_f})^2} \\ &= \frac{\frac{(C_s+C_f)^2 V_{in}^2}{C_f^2}}{\frac{kT(C_s+C_f)}{C_f^2}} \\ &= \frac{V_{in}^2}{\frac{kT}{C_s+C_f}} \end{aligned} \tag{3.13}$$

Charge Amplifier MDAC Topology For the charge amplifier based MDAC, there is no extra gain component from the flip-around input. The output signal power of the charge amplifier MDAC can be expressed as

$$V_{out}^2 = (\frac{C_s}{C_f})^2 V_{in}^2 \tag{3.14}$$

Since the integrated output noise powers of both the charge amplifier MDAC and flip-around MDAC topologies are the same, the simplified SNR for the charge amplifier MDAC can be expressed as in Equation (3.15).

$$\begin{aligned} SNR_{CA,simplified} &= \frac{(\frac{C_s}{C_f})^2 V_{in}^2}{\frac{kT}{C_f}+(\frac{kT}{C_s})(\frac{C_s}{C_f})^2} \\ &= \frac{\frac{C_s^2 V_{in}^2}{C_f^2}}{\frac{kT(C_s+C_f)}{C_f^2}} \\ &= \frac{V_{in}^2}{\frac{kT}{C_s+C_f}}(1-\beta)^2 \end{aligned} \tag{3.15}$$

where $1-\beta = \frac{C_s}{C_s+C_f}$.

From the SNR requirement and the noise budgeting (i.e., the portion of the total noise allocated to the sampling phase noise), the required $(C_s + C_f)$ can be derived. Since the capacitor ratio $\frac{C_s}{C_f}$ follows from the closed-loop gain needed, we

can easily find the capacitor values C_s and C_f needed to achieve a particular noise performance.

Comparison If we compare the SNR of the flip-around MDAC and the charge amplifier MDAC given in Equation (3.13) and (3.15) respectively, we get the following relationship:

$$SNR_{CA,simplified} = (1-\beta)^2 SNR_{FA,simplified} \tag{3.16}$$

Equation (3.16) shows that the flip-around MDAC always gives better SNR compared to the charge amplifier MDAC, but the effectiveness of the flip-around MDAC reduces with the decrease of the β or with the increase of the closed-loop gain ($\frac{C_s}{C_f}$). For example, if $C_s = C_f$ ($\beta = 0.5$), then the SNR of the flip-around MDAC is 4 times or $6dB$ better than that of the charge amplifier MDAC. But when $C_s = 4C_f$ ($\beta = 0.2$), the SNR of the flip-around MDAC becomes only 1.6 times or $2dB$ better than that of the charge amplifier MDAC.

3.3 Residue Amplifier

The residue amplifier is probably the most important building block of the MDAC and also of the entire pipeline ADC. The purpose of using the residue amplifier is to suppress the noise and the non-linearities from the latter stages of the pipeline ADC, which means that the latter stages can be made with less accuracy compared to the first stage. In this section, two amplifier classes have been discussed and a detailed comparison is made between them. Please note that we have intentionally used very simple amplifiers because they do not need to provide a high loop gain to suppress non-linearities, due to an assistance of digital calibration. The amplifiers only need to meet the speed and the noise requirements.

3.3.1 Class-A Amplifier

Class-A amplifiers are arguably the most popular amplifier configurations that have been used as the residue amplifier of the pipeline ADC [11]. In a class-A amplifier, the maximum drive current is limited by the supplied bias or quiescent current.

This bias current always flows in the amplifier and needs to be at least as high as the maximum drive current needed. As a result, the class-A amplifier shows poor power efficiency. Figure 3.8 shows a very simple class-A amplifier topology with an ideal common mode feedback (CMFB) loop.

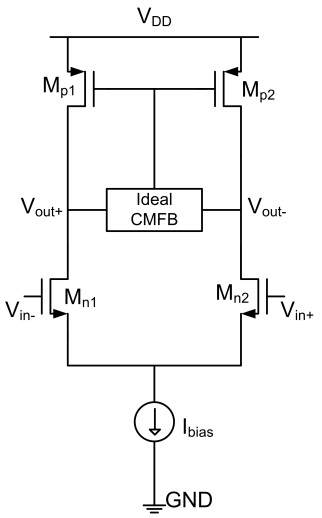


Figure 3.8: Class-A amplifier topology.

In a class-A amplifier as shown in Figure 3.8, the input signal is fed to the NMOS differential pair transistors M_{n1} and M_{n2}. I_{bias} is the biasing current of the tail current source that flows through the amplifier all the time and limits the maximum drive current that the amplifier can provide. For simplicity, an ideal CMFB circuit is used to control the common mode voltage at the output of the amplifier. PMOS transistors M_{p1} and M_{p2} serve as the active load of the amplifier and do not contribute to the effective transconductance ($g_{m,eff}$) of the amplifier. So, the $g_{m,eff}$ of such an amplifier [20] can be expressed as

$$g_{m,eff} = 2\frac{g_{mn1}g_{mn2}}{g_{mn1} + g_{mn2}} \tag{3.17}$$

Equation (3.17) shows that the $g_{m,eff}$ is two times the parallel combination of the transconductances g_{mn1} and g_{mn2} of the transistors M_{n1} and M_{n2} respectively. This means that the amplifier has the maximum $g_{m,eff}$ at the biasing condition, where $g_{mn1} = g_{mn2}$ and the $g_{m,eff}$ decreases from its maximum value when any

signal is applied to the amplifier. Using the above expression of the $g_{m,eff}$, the small-signal gain (A) of the class-A amplifier in Figure 3.8 can be derived as

$$\begin{aligned} A &= g_{m,eff}\, r_{ds,eff} \\ &= 2\frac{g_{mn1}g_{mn2}}{g_{mn1}+g_{mn2}}(r_{ds,mn1}||r_{ds,mp1}) \end{aligned} \tag{3.18}$$

where $r_{ds,mn1}$and $r_{ds,mp1}$ are the output resistance of the NMOS transistor M_{n1} and PMOS active load M_{p1} respectively. The biasing current of the class-A amplifier is very stable since it is defined by the tail current source. Furthermore, the common mode rejection ratio of this amplifier is very good and reaches to infinity [20], if the tail current source has infinite output resistance.

3.3.2 Class-AB Amplifier

In a class-AB amplifier, the maximum drive current can be much higher than the biasing current. This makes the class-AB amplifier more power efficient than the class-A amplifier. Since we are using a single stage amplifier, stability of the amplifier should always be ensured by the design. But the stability and the predictability of the biasing current need to be ensured. Figure 3.9 shows a simple class-AB amplifier, where the level shifters V_{LS1} and V_{LS2} are implemented by ideal voltage sources.

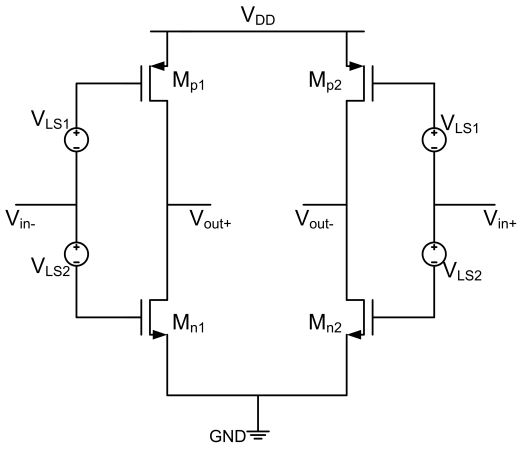


Figure 3.9: Class-AB amplifier topology.

All the NMOS and the PMOS transistors of the class-AB amplifier in Figure 3.9 contribute to the $g_{m,eff}$, whereas for the class-A amplifier in Figure 3.8, only the NMOS transistors contribute to the $g_{m,eff}$. The $g_{m,eff}$ of the class-AB amplifier can be expressed as

$$g_{m,eff} = \frac{(g_{mn1} + g_{mp1}) + (g_{mn2} + g_{mp2})}{2} \tag{3.19}$$

At the quiescent condition, the $g_{m,eff}$ of the class-AB amplifier is minimum and it increases as any input signal is applied to the amplifier. Since all the transistors contribute to the $g_{m,eff}$, the class-AB amplifier always exhibits higher $g_{m,eff}$ than the class-A amplifier for the same quiescent current. For example, if all the transistors of Figures 3.8 and 3.9 have approximately the same g_m, then the $g_{m,eff}$ of the class-AB amplifier is approximately two times higher than the $g_{m,eff}$ of the class-A amplifier. This is also illustrated in Figure 3.10 in which the biasing current of both the amplifiers are kept the same.

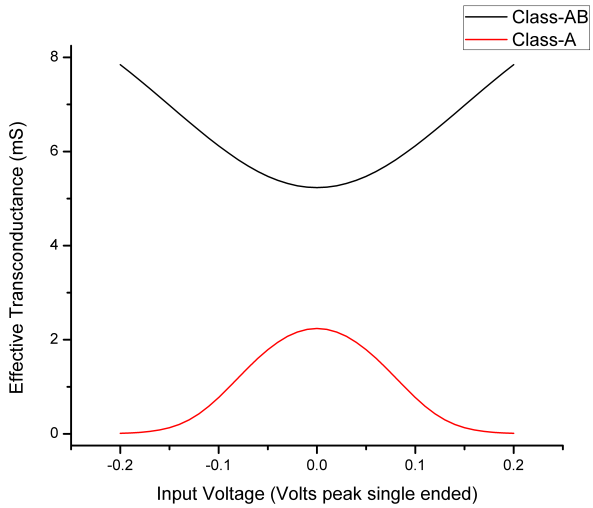


Figure 3.10: Effective transconductance ($g_{m,eff}$) of the class-A and the class-AB amplifier as a function of the input step or input voltage V_{in}.

The small-signal gain (A) of the class-AB amplifier of Figure 3.9 is expressed in Equation 3.20.

$$\begin{aligned} A &= g_{m,eff}\, r_{ds,eff} \\ &= \frac{(g_{mn1}+g_{mp1})+(g_{mn2}+g_{mp2})}{2}(r_{ds,mn1}||r_{ds,mp1}) \end{aligned} \tag{3.20}$$

Since the effective output resistance $r_{ds,eff}$ of both the amplifiers are essentially the same for the same quiescent current and the $g_{m,eff}$ of the class-AB amplifier is higher than the class-A amplifier, then the small-signal gain (A) would also be higher for the class-AB amplifier compared to the class-A amplifier. As a result, the non-linearities of the class-AB amplifier is less due to its high loop gain ($A\beta$). A disadvantage of class-AB amplifier of Figure 3.9 is that it does not have any common mode rejection ratio (CMRR).

3.3.3 Comparison: Class-A and Class-AB Amplifier

In this section, we have made a comparison between the class-A amplifier of Figure 3.8 and the class-AB amplifier of Figure 3.9. In this comparison, both amplifiers have to work in a system that has a sampling frequency of $f_s = 500MHz$ and a large-signal closed-loop gain of 2. Since the residue amplifiers of a pipeline ADC operate for approximately half of the clock period ($\frac{T_s}{2} = 1ns$), thus the amplifiers have to reach a large-signal closed-loop gain of 2 within that specified time. To achieve these specifications, the class-A amplifier requires higher biasing current than that of the class-AB amplifier. Please note that in order to change the biasing current of an amplifier, we have either increased or decreased the number of parallel transistors while keeping their V_{gt}'s the same as before. During this comparison, different performance aspects of the residue amplifiers such as gain, bandwidth, linearity, noise, power consumption have been compared. For this comparison, the flip-around MDAC topology of Figure 3.2 has been used as a test vehicle, but with only one sub-DAC reference level ($V_{dac} = V_{cm}$) instead of three. The simulation setup for the comparison of the class-A amplifier and the class-AB amplifier is shown in Figure 3.11.

Please note that the focus of this comparison is to see how the two amplifiers perform with respect to each other. So, all the switches that have been used for

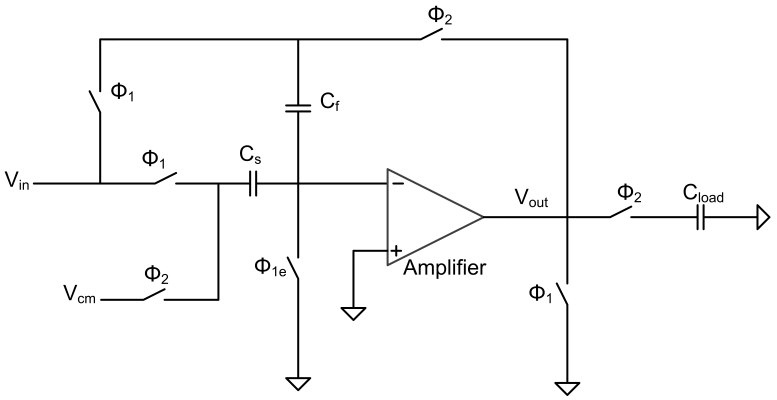


Figure 3.11: Simulation setup for the comparison of the class-A and the class-AB amplifier.

this comparison are kept ideal, thus ignoring effects like finite on resistance, charge injection etc.

Gain and Bandwidth

We have already discussed about the gain and the bandwidth behavior of the class-A amplifier and the class-AB amplifier in Section 3.3.1 and 3.3.2, respectively. Figure 3.12 shows the simulated open-loop gains and bandwidths for both the amplifier. As expected, the class-AB amplifier shows higher $A\beta$ than the class-A amplifier irrespective of the biasing current. This is because in order to change the biasing current, we either have scaled up or scaled down the whole design (i.e., change the width of all the transistors of the amplifier in the same way) and since $g_m \propto I_D$ and $r_{ds} \propto \frac{1}{I_D}$, the gain ($A = g_m r_{ds}$) of the amplifier remains constant.

Please note that the the two amplifiers that are being compared are very simple and do not provide a large loop gain. Moreover, we do not want to let the amplifiers to settle to a high accuracy in order to reduce power consumption. Due to these reasons, the $\frac{C_s}{C_f}$ ratio needs to be higher than 1 in order to reach a large-signal closed-loop gain of 2 for the flip-around MDAC of Figure 3.2. For this comparison, we have used a $\frac{C_s}{C_f}$ ratio of 2.

We have seen from Figure 3.10 that the $g_{m,eff}$ of the class-A amplifier is less than that of the class-AB amplifier at the quiescent condition (i.e., zero input signal)

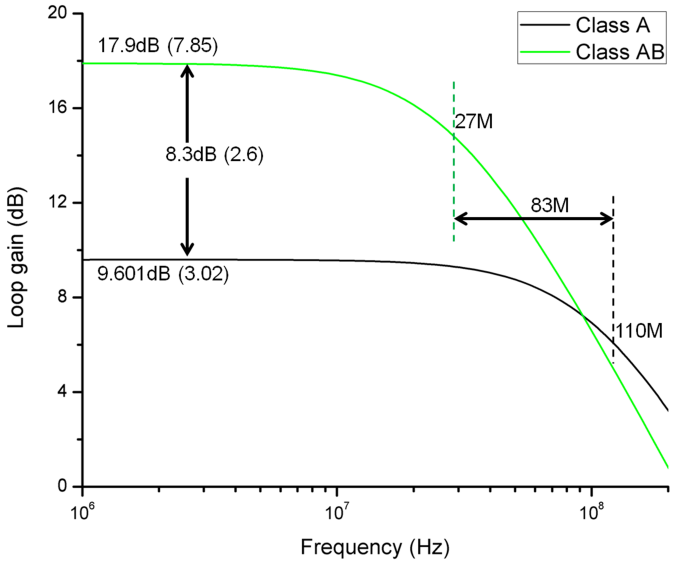


Figure 3.12: Simulated loop gain of the class-A and the class-AB amplifier.

and it decreases even more when an input signal is applied. This indicates that in order to reach a large-signal closed-loop gain of 2 within approximately half of the clock period ($\frac{T_s}{2} = 1ns$), the bandwidth of the class-A amplifier at quiescent condition needs to be much higher than that of the class-AB amplifier. In other words, the biasing current needed by the class-A amplifier is much higher than that of the class-AB amplifier. The difference in bandwidths between the class-A and the class-AB amplifiers, for the open-loop and closed-loop configurations are shown in Figures 3.13 and 3.12, respectively. We can see from those figures that the bandwidth required by the class-A amplifier is higher than that required by the class-AB amplifier in both the cases, in order to reach to the same gain of 2 within the specified time.

The small-signal closed-loop gain of the amplifiers are shown in Figure 3.13. Since the class-AB amplifier has higher $A\beta$ compared to the class-A amplifier, its small-signal closed-loop gain is closer to the ideal value (i.e., $\frac{C_s}{C_f} = 2$). Please note that the small-signal closed-loop gains do not include the gain contributions from the flip-around input. In order to see the real gain or the large-signal gain of the amplifier, a large-signal simulation needs to be done, which includes the

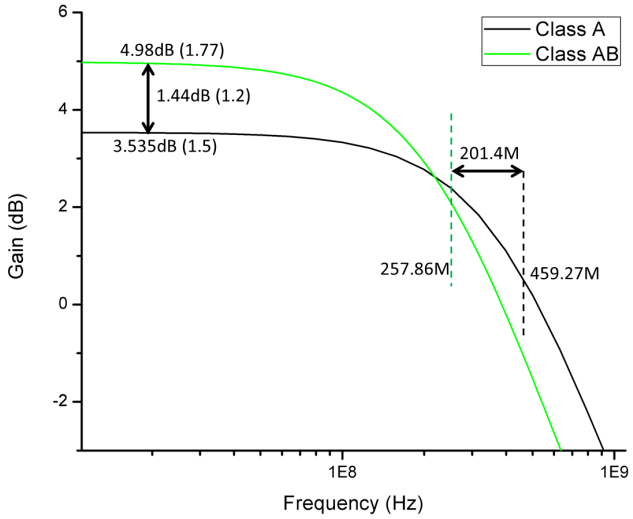


Figure 3.13: Simulated small-signal closed-loop gain and closed-loop bandwidth.

contribution from the flip-around input. Figure 3.14 shows the simulated large-signal closed-loop gain of both the amplifiers, which are basically $6dB$ or 2 as per the specification. This proves that both the amplifiers indeed reach the specified large-signal closed-loop gain of 2 within the specified time, that is approximately half of the clock period.

Linearity

Many applications (e.g., audio) require highly linear amplification. High-gain amplifiers in a negative feedback loop can be used to obtain highly linear operations for many electronic circuits, but this comes at the cost of complex circuitry and degradation of the performance parameters such as speed, noise and power consumption [4]. Since this work has been intended to be assisted by the digital calibration to correct for non-linearities, we have utilized simple low gain amplifiers that achieve better performance in terms of speed, noise and power consumption. In this section, we have shown both theoretically and with simulation results that the class-AB amplifier as shown in Figure 3.9 is inherently more linear than the class-A amplifier of Figure 3.8.

For the class-A amplifier, as shown in Figure 3.8, the source terminals of the

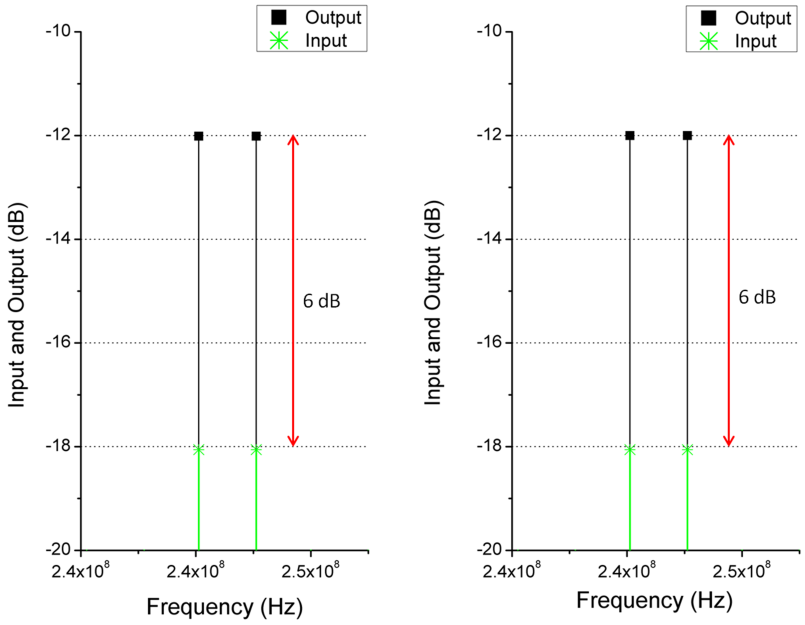


Figure 3.14: Simulated large-signal closed-loop gain.

differential pair transistors M_{n1} and M_{n2} are connected to the tail current source, but for the class-AB amplifier, as shown in Figure 3.9, those are connected to the ground. For this analysis, we have assumed that the MOS transistors are quadratic devices biased in strong inversion saturation. So, currents I_1 and I_2 that flows through M_{n1} and M_{n2} transistors, respectively, are given by

$$I_1 = \frac{1}{2} K V_{gt1}^2 \tag{3.21}$$

$$I_2 = \frac{1}{2} K V_{gt2}^2 \tag{3.22}$$

where $K = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}$. Therefore, the output current I_o can be calculated from Equations (3.22) and (3.21), as stated in Equation 3.23.

$$\begin{aligned} I_o &= \frac{1}{2}KV_{gt2}^2 - \frac{1}{2}KV_{gt1}^2 \\ &= \frac{1}{2}K(V_{gt1} + V_{gt2})(V_{gt2} - V_{gt1}) \\ &= \frac{1}{2}K(V_{gt1} + V_{gt2})V_{in} \end{aligned} \tag{3.23}$$

If $(V_{gt1} + V_{gt2})$ remains constant, then the I_o varies linearly with the V_{in}, resulting in a perfectly linear system. Let's see how the $(V_{gt1} + V_{gt2})$ term behaves for the class-A and class-AB amplifiers.

For the class-A amplifier, as shown in Figure 3.8, $(V_{gt1} + V_{gt2})$ term is given by

$$V_{gt1} + V_{gt2} = \sqrt{\frac{4I_{tail}}{K} - V_{in}^2} \tag{3.24}$$

Equation (3.24) shows that the summation of the V_{gt}'s varies non-linearly with the input signal V_{in}, and thus resulting in distortion. However, for the class-AB amplifier, as shown in Figure 3.9,

$$\begin{aligned} V_{gt1} + V_{gt2} &= (V_{cm} - 0.5V_{in} - V_t) + (V_{cm} + 0.5V_{in} - V_t) \\ &= 2(V_{cm} - V_t) = constant \end{aligned} \tag{3.25}$$

Since the summation of the V_{gt}'s remains constant for the class-AB amplifier, it behaves more linearly than the class-A amplifier. Please note that Equation (3.25) only holds as long as both the V_{gt}'s are above zero. Outside this range, the class-AB amplifier becomes slightly non-linear. How significant this non-linearity is compared to that of the class-A amplifier can be illustrated by a numerical example, as shown in Table 3.1.

Numerical Example: To illustrate the difference in linearity behavior between the class-A amplifier and the class-AB amplifier, we have used a simple numerical example. Please note that the values stated in this example are not taken from any simulation results. For this example, we have assumed that $\frac{1}{2}K = 1$ and $I_{tail} = 50$. Table 3.1 shows the values that will be used in this numerical example, where row

11 (i.e., $V_{in} = 0$) represents the quiescent current or the biasing conditions of both the amplifiers.

In Table 3.1 column 7, 8 and 9 show the following parameters:

$I_{sum} = I_1 + I_2$,

$I_{o,ideal}$ =output current in case of perfectly linear system;

$error_{rel} = | \frac{I_o - I_{o,ideal}}{I_o} |$=relative error in the current value compared to the ideal current value.

Please note that the subscript cA indicates the parameters for the class-A amplifier and the rest represents that of the class-AB amplifier.

Table 3.1 shows that for the differential input (V_{in}) ranging from -10 to +10, the ($V_{gt1} + V_{gt2}$) term remains constant. This results in 0% relative error ($error_{rel}$) for the class-AB amplifier operating in that input range, meaning perfectly linear system. On the other hand, the relative error for the class-A amplifier ($error_{rel,cA}$) is much higher because the summation of the V_{gt}'s follow a square-root relationship with the V_{in} and is never constant. Figures 3.15(a) and 3.15(b) show the transfer functions ($I_o \, vs \, V_{in}$) and the relative errors of both the amplifiers respectively as a function of the input voltage V_{in}. From the figure, we can see that the transfer curve of the class-AB amplifier is more linear than that of the class-A amplifier. Also, the relative error in the output current for the class-AB amplifier is much less than that of the class-A amplifier.

Please note that the whole numerical example is based on the following assumption: the MOS transistors behave like quadratic devices in the strong inversion saturation region. Actually, this is no more true in the deep sub-micron CMOS technologies due to the various second-order effects (e.g., velocity saturation, mobility reduction). Moreover, we intentionally bias the transistors in the moderate inversion region sometimes to get a good speed and a lower power consumption [22] at the same time. Note that in the moderate inversion saturation region, the MOS transistor behaves somewhere between an exponential device (e.g., BJTs) and a quadratic device.

Table 3.1: Numerical example showing the transfer characteristics of the class-A amplifier and the class-AB amplifier.

V_{in}	V_{gt1}	V_{gt2}	I_1	I_2	I_o	I_{sum}	$I_{o,ideal}$	$error_{rel}$	$I_{o,cA}$	$I_{sum,cA}$	$error_{rel,cA}$
20	0	15	0	225	225	225	200	11%	50	50	300%
18	0	14	0	196	196	196	180	8%	50	50	260%
16	0	13	0	169	169	169	160	5%	50	50	220%
14	0	12	0	144	144	144	140	3%	50	50	180%
12	0	11	0	121	121	121	120	1%	50	50	140%
10	0	10	0	100	100	100	100	0%	50	50	100%
8	1	9	1	81	80	82	80	0%	50	50	60%
6	2	8	4	64	60	68	60	0%	48	50	25%
4	3	7	9	49	40	58	40	0%	36.7	50	9.1%
2	4	6	16	36	20	52	20	0%	19.6	50	2%
0	5	5	25	25	0	50	0	0%	0	50	0%
-2	6	4	36	16	-20	52	-20	0%	-19.6	50	2%
-4	7	3	49	9	-40	58	-40	0%	-36.7	50	9.1%
-6	8	2	64	4	-60	68	-60	0%	-48	50	25%
-8	9	1	81	1	-80	82	-80	0%	-50	50	60%
-10	10	0	100	0	-100	100	-100	0%	-50	50	100%
-12	11	0	121	0	-121	121	-120	1%	-50	50	140%
-14	12	0	144	0	-144	144	-140	3%	-50	50	180%
-16	13	0	169	0	-169	169	-160	5%	-50	50	220%
-18	14	0	196	0	-196	196	-180	8%	-50	50	260%
-20	15	0	225	0	-225	225	-200	11%	-50	50	300%

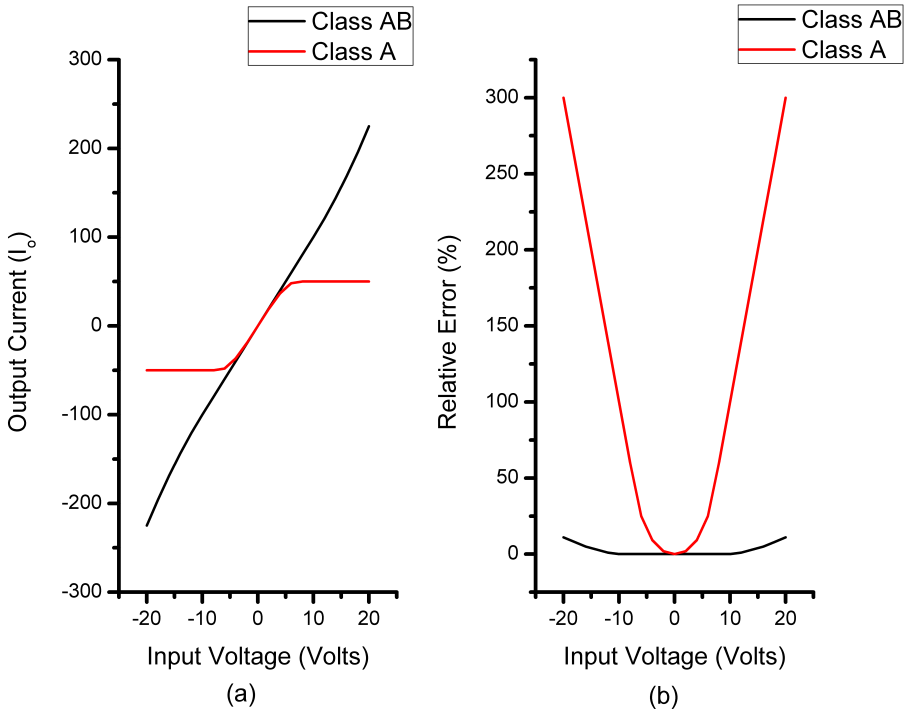
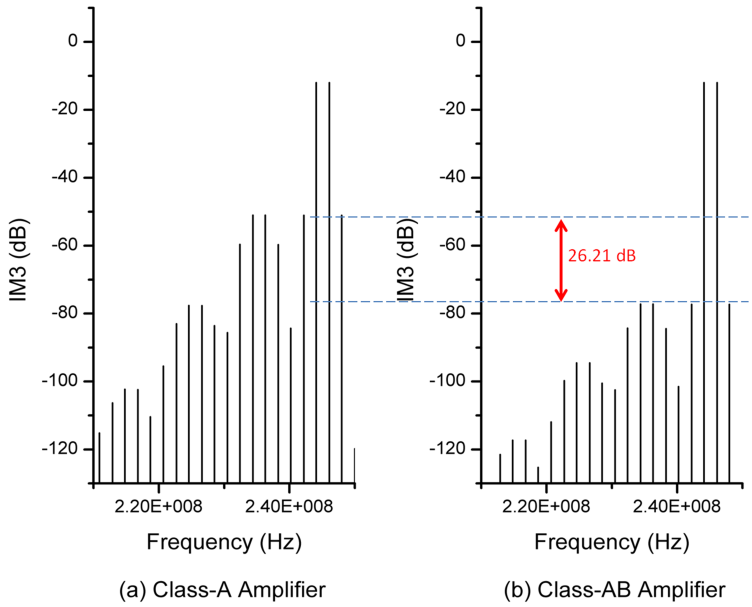


Figure 3.15: (a) Transfer curves (to the left), and (b) relative errors (to the right) as a function of the input voltage for both the amplifiers.

We have done a two-tone simulation for the input signals close to the Nyquist frequency. The output swing for both the amplifiers have been kept at $1V$ peak-to-peak differential. The simulation results are shown in Figure 3.16. From the two-tone test, we can see that the class-AB amplifier achieves approximately $26dB$ better linearity than the class-A amplifier. This improvement is not only coming from the higher loop gain in case of the class-AB amplifier, but also because of the fact that the class-AB amplifier of Figure 3.9 is inherently more linear than the class-A amplifier of Figure 3.8.

Thermal Noise

Since the design is intended to be used with the digital calibration to correct for the non-linearities, thermal noise becomes the most important performance aspect of the residue amplifier. In this section, we first compared the noise behavior of the two amplifiers analytically and then show the simulation results.



(a) Class-A Amplifier (b) Class-AB Amplifier

Figure 3.16: Two-tone simulation of the class-A amplifier and the class-AB amplifier.

Class-AB Amplifier For the class-AB amplifier, both the NMOS and the PMOS transistors produce thermal noise and also contribute to the $g_{m,eff}$ (i.e., bandwidth). Figure 3.17 shows the small-signal half-circuit of the class-AB amplifier with regards to the thermal noise. For simplicity, we exclude the capacitors from the small-signal circuit of Figure 3.17.

Figure 3.17 shows the noise current of the transistors that flows into the output resistance to create the output noise voltage. If we integrate the output noise power density over the whole frequency spectrum, we get the following expression for the integrated output noise power of the amplifier in closed-loop configuration as

$$V_{n,amp}^2 \approx 4kT\gamma(g_{mn1} + g_{mp1})r_{out}^2 BW_{noise} \tag{3.26}$$

where:

γ = noise parameter of the MOS transistor [23];

$r_{out} = \frac{r_{ds,mn1} || r_{ds,mp1}}{1+A\beta} \approx \frac{r_{ds,eff}}{A\beta}$ = closed-loop output resistance of the amplifier;

BW_{noise}= noise bandwidth of the amplifier which is $\frac{\pi}{2}$ times the closed-loop

signal bandwidth for the first order linear system.

Please note that the integrated output noise power of the amplifier is calculated in closed-loop configuration. Although this might not be the standard approach for calculating the integrated output noise power of an amplifier, but we have followed this in our analysis.

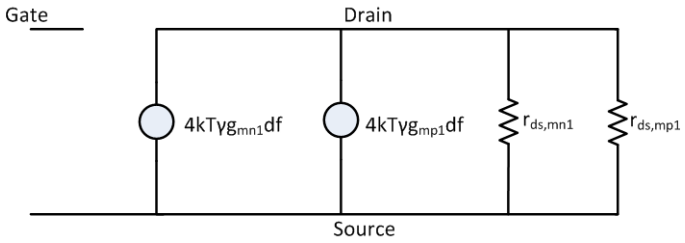


Figure 3.17: Small-signal half circuit of the class-AB amplifier for noise.

At the quiescent condition, the $g_{m,eff}$ of Equation (3.19) is $(g_{mn1} + g_{mp1})$, since $g_{mn1} = g_{mn2}$ and $g_{mp1} = g_{mp2}$. If we replace the value of the amplifier gain A with that of Equation (3.20), the r_{out} becomes

$$\begin{aligned} r_{out} &= \frac{r_{ds,eff}}{\beta g_{m,eff} r_{ds,eff}} \\ &= \frac{1}{\beta(g_{mn1} + g_{mp1})} \end{aligned} \tag{3.27}$$

The noise bandwidth BW_{noise} for the first order linear system can be expressed as

$$\begin{aligned} BW_{noise} &= \frac{\pi}{2} \times \frac{1}{2\pi r_{out} C_{out}} \\ &= \frac{\beta(g_{mn1} + g_{mp1})}{4C_{out}} \end{aligned} \tag{3.28}$$

where C_{out} = total output capacitance of the amplifier.

Substituting the value of the r_{out} and the BW_{noise} of Equations (3.27) and (3.28) respectively into Equation (3.26), we get the following expression for the closed-loop integrated noise power at the output:

$$\begin{aligned} V_{n,amp}^2 &= 4kT\gamma(g_{mn1}+g_{mp1})\frac{1}{\beta^2(g_{mn1}+g_{mp1})^2}\times\frac{\beta(g_{mn1}+g_{mp1})}{4C_{out}} \\ &= \gamma\frac{kT}{\beta C_{out}} \end{aligned} \tag{3.29}$$

Equation (3.29) shows that there is no excess noise (i.e., excess noise factor = 1) for the class-AB amplifier. The reason is because the transistors that produce the noise also produce the output signal, i.e., there is no biasing transistor that produces noise but no gain. It also shows that integrated noise power at the output of the amplifier does not depend on the biasing condition ($g_{m,eff}$). It depends only on the feedback factor (β) and the output capacitor (C_{out}) of the amplifier. Please note that the β is in the denominator of Equation (3.29) because if we increase the closed-loop gain (i.e., decrease the β) of the amplifier, the $V_{n,amp}^2$ will also increase along with the increase in the output signal.

Class-A Amplifier In the class-A amplifier, the PMOS current sources or active loads M_{p1} and M_{p2} at the top only contribute to the noise but do not contribute to the signal gain and bandwidth. If we derive the parameters such as r_{out}, BW_{noise} and $V_{n,amp}^2$ of the class-A amplifier similar to that of the class-AB amplifier, we get the following expressions:

$$r_{out} = \frac{1}{\beta g_{mn1}} \tag{3.30}$$

$$BW_{noise} = \frac{\beta g_{mn1}}{4C_{load}} \tag{3.31}$$

$$\begin{aligned} V_{n,amp}^2 &= 4kT\gamma(g_{mn1}+g_{mp1})\frac{1}{\beta^2{g_{mn1}}^2}\times\frac{\beta g_{mn1}}{4C_{load}} \\ &= \gamma\frac{kT}{\beta C_{load}}(1+\frac{g_{mp1}}{g_{mn1}}) \end{aligned} \tag{3.32}$$

where $(1+\frac{g_{mp1}}{g_{mn1}})$ is called the excess noise factor of the amplifier. Since the excess noise factor factor is always greater than 1, the class-A amplifier always gives more

integrated noise than the class-AB amplifier. Normally, we try to optimize the noise performance of the class-A amplifier by increasing the channel length of the M_{p1} and M_{p2}. This results in lower g_ms but higher V_{gt}s of the M_{p1} and M_{p2} transistors, thus reducing the allowable signal swing at the output and eventually leading to lower SNR. So, there is not a lot of scope for the noise optimization. This is especially true in the deep sub-micron technologies, where the supply voltage is very low (e.g., $1V$ supply voltage is used for our design in $40nm$ CMOS technology). For simplicity, the noise optimization for the class-A amplifier has not been done in this comparison and the g_ms of all the NMOS and the PMOS transistors for both the amplifiers are almost kept the same. As a result, the excess noise factor for the class-A amplifier is approximately 2, which would be a bit less in practice due to the noise optimization.

Conclusion We have used C_{load} of $836fF$ for the comparison of the class-A and class-AB amplifiers. This results in an approximate differential output noise power of $1 \times 10^{-8}V^2$ (assuming γ =1), according to Equation 3.29. For the class-A amplifier, $\frac{g_{mp1}}{g_{mn1}}$ ratio is 1.27 and thus, the differential output noise power is $2.27 \times 10^{-8}V^2$ according to Equation 3.32. We have also simulated large-signal noise of both the amplifiers. The simulation setup is the same as shown in Figure 3.11 except for the fact that $V_{in} = 0$. Simulated differential output noise power ($V^2_{n,amp}$) for the class-AB amplifier is $1.12 \times 10^{-8}V^2$ and for the class-A amplifier is $2.244 \times 10^{-8}V^2$, which are in accordance with the calculated differential output noise powers of the respective amplifiers. Therefore, we conclude that the class-A amplifier of Figure 3.8 produces more noise (about $2\times$ in this example) than the class-AB amplifier of Figure 3.9.

Common-Mode Rejection Ratio

Common-mode rejection ratio (CMRR) of a differential amplifier is defined [24] as the ratio of the desired differential-mode gain (A_{dm}) to the undesired common-mode gain (A_{cm}).

$$CMRR = \left|\frac{A_{dm}}{A_{cm}}\right| \tag{3.33}$$

The class-AB amplifier of Figure 3.9 is pseudo-differential and hence, the common-mode gain is equal to the differential-mode gain (i.e., CMRR=0dB). However, for the class-A amplifier of Figure 3.8, the common-mode gain is 38.11dB lower than the desired differential-mode gain due to the high output resistance of the tail current source. We have simulated common-mode and differential mode gains of the class-A amplifier and calculated the CMRR (i.e., 38.11dB). This is shown in Figure 3.18.

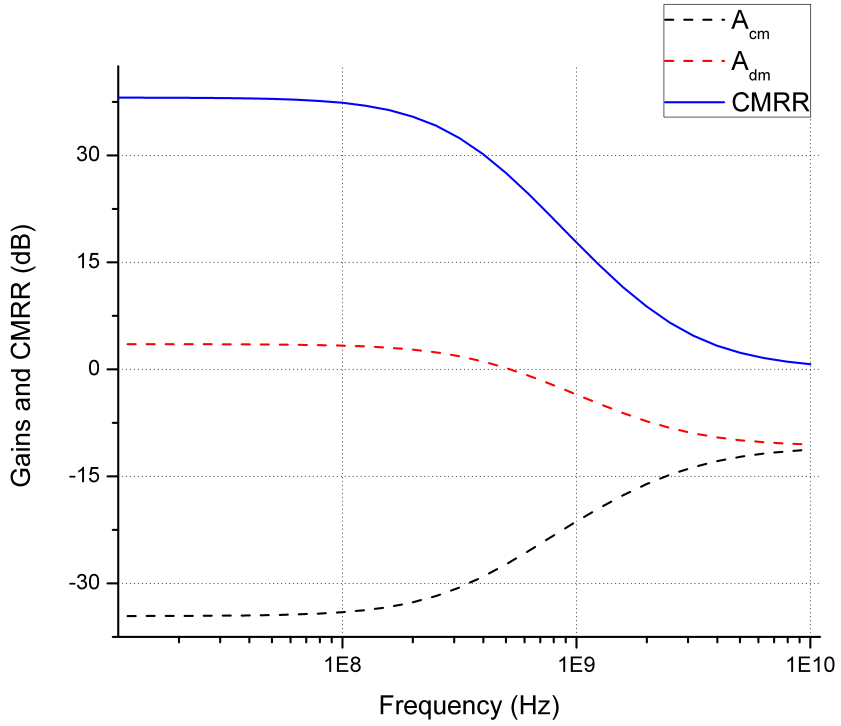


Figure 3.18: Different gains and CMRR of the class-A amplifier.

Power Consumption

For the class-A amplifier, the current consumption is always fixed and equal to the quiescent current, but for the class-AB amplifier, the current consumption increases as the amplifier drives any load. Figure 3.19 shows the current consumption of the class-AB amplifier of Figure 3.9. The average value of all the currents is taken arbi-

trarily as an estimation of the current consumption in the class-AB amplifier. Please note that the estimation of the proper current consumption in a class-AB amplifier is not straightforward, because it depends on the input signal distribution of the pipeline ADC. If we assume that the distribution of the input signal to the pipeline ADC is flat, then the residue input voltage to the amplifier is small for most part of the input signal range. This would make our choice of the estimated current consumption a bit pessimistic. However, if we assume the input signal distribution to be sinusoidal, then for most part of the input signal range, the amplifier's input residue voltage (i.e., the input voltage to the amplifier) is high. This would make the choice of the estimated current consumption to become a bit optimistic. Multiplying the estimated current consumption (I) with the supply voltage (V_{DD}) gives the power consumption ($P = IV_{DD}$) of the amplifier.

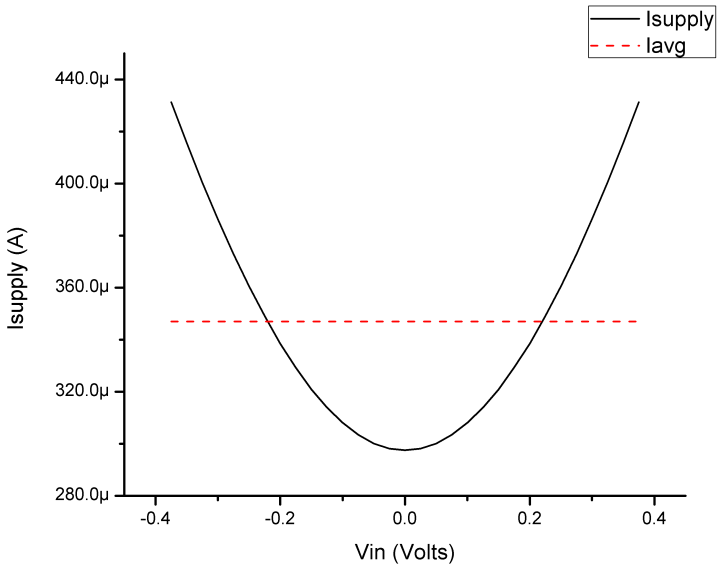


Figure 3.19: Current consumption of class-AB amplifier.

Table 3.2 lists all the performance aspects of the comparison made between the class-A amplifier of Figure 3.8 and the class-AB amplifier of Figure 3.9. From this table, we can see that the class-AB amplifier performs better than the class-A amplifier in all the performance aspects. We can calculate the Figure-of-Merit (FOM) of a pipeline ADC using Equation (3.34) [12], by considering the following

assumptions: only the amplifiers in the pipeline ADC produce noise and consume power. The amplifier design is only limited by noise due to the assistance of a digital calibration (i.e., SNDR=SNR). Therefore, we will ignore the linearity performance of the amplifier in the FOM_1 calculation. Moreover, the pipeline ADC architecture is assumed to be similar to that in [11]. From this, we can estimate the total power consumption and the total input referred differential noise power of the pipeline ADC.

$$FOM_1 = \frac{Power}{2^{ENOB} \times Minimum(2f_{sig}, f_s)} \tag{3.34}$$

where the minimum of the $2f_{sig}$ or f_s is taken, which is $500MHz$ in our design. The calculated FOM_1 is listed in Table 3.2, which shows that the class-AB amplifier achieves $5.4\times$ better FOM_1 compared to the class-A amplifier. Please note that the class-AB amplifier also achieves $26.21dB$ better linearity than the class-A amplifier, which has not been considered in FOM_1 calculation.

Table 3.2: Comparison table: class-A and class-AB amplifiers.

Performance Aspects	Class-A Amp.	Class-AB Amp.
Peak input signal (V diff.)	0.5	0.5
Loop gain (dB)	9.6	17.9
Bandwidth (MHz)	459.27	257.86
small-signal gain (dB)	3.53	4.98
Large-signal gain (dB)	6.05	6.06
IM3 (dB)	39.05	65.26
CMRR (dB)	38.11	0
Noise power (V^2 output referred diff.)	2.244×10^{-8}	1.12×10^{-8}
Noise power (V^2 input referred diff.)	5.61×10^{-9}	2.8×10^{-9}
Total noise power (V^2 input referred diff.)	1.028×10^{-8}	5.132×10^{-9}
Static power consumption (mW)	1.34	0.35
Total power consumption (mW)	4.69	1.225
FOM_1 (fJ/conv)	3.29	0.61

3.4 Summary

Different MDAC topologies and their basic operations have been discussed in this chapter. Thermal noise analysis of the two closed-loop MDAC topologies have been made, where the flip-around MDAC topology shows better SNR than the charge amplifier MDAC. Two classes of amplifiers, namely the class-A amplifier and the class-AB amplifier are discussed and a comparison has been made between them. Many performance aspects like gain, bandwidth, linearity, noise and power consumption are compared, which concludes that the class-AB amplifier outperforms the class-A amplifier in all the aspects except for the CMRR. Assuming that the CMRR of the class-AB amplifier can be improved in another way, we can thus conclude that the class-AB amplifier would be the better choice as the residue amplifier of the pipeline ADC in our design.

Chapter 4

MDAC Design

In this chapter, we present the design of the MDAC for our pipeline ADC. Firstly, a new class-AB amplifier is proposed and its performance parameters are compared with an existing class-AB amplifier [21]. Several problems with the flip-around MDAC topology are discussed and a solution is proposed. Finally, the layout of the MDAC for the first pipeline stage is described.

4.1 Amplifier Design

In the class-AB amplifier of Figure 3.9, ideal voltage sources have been used as level shifters. Capacitors with switches [21] can be used to implement these level shifters as shown in Figure 4.1. During the reset phase ϕ_1, capacitors C_{LS1} and C_{LS2} are pre-charged to the desired voltages so that they can be used to shift the voltage levels in the amplification phase ϕ_2. However, there are many problems related with this solution, which are addressed in the next section.

4.1.1 Problems with the Existing Class-AB Amplifier

Implementing level shifters by capacitors with switches reduces the gain and speed of the class-AB amplifier of Figure 4.1. Moreover, it introduces extra noise components. These problems are discussed in this section.

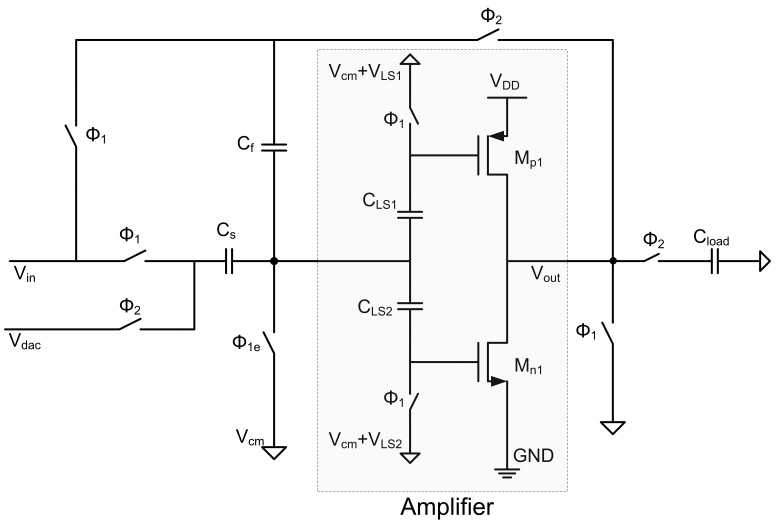


Figure 4.1: The class-AB amplifier with capacitor level shifters in a flip-around MDAC topology.

Gain and Bandwidth

There are different approaches for implementing capacitors such as metal-insulator-metal (MIM) capacitor, metal-metal finger capacitors or MOS capacitors. No matter how capacitors are implemented, they always introduce parasitic capacitance to ground and also to other circuit nets. This situation can be illustrated by Figure 4.2, where C_{p1}, C_{p2} and C_{p3} represent the parasitic capacitors from different nets to ground.

We can express the parasitic capacitance (C_{px}) from node x to ground and the output capacitance (C_{out}) of Figure 4.2 by

$$C_{px} = \frac{C_{LS1}C_{p1}}{C_{LS1} + C_{p1}} + \frac{C_{LS2}C_{p2}}{C_{LS2} + C_{p2}} + C_{p3} \tag{4.1}$$

$$C_{out} = C_{load} + \frac{(C_{px} + C_s)C_f}{(C_{px} + C_s) + C_f} \tag{4.2}$$

Using C_{LS1} and C_{LS2} introduce more parasitic capacitances and that raise the values of C_{p1}, C_{p2} and C_{p3}. As a result, C_{px} and C_{out} increase according to Equations (4.1) and (4.2) respectively, and hence reduce the speed of the class-AB amplifier as shown in Figure 4.1. In order to maintain the same speed as before, more bias cur-

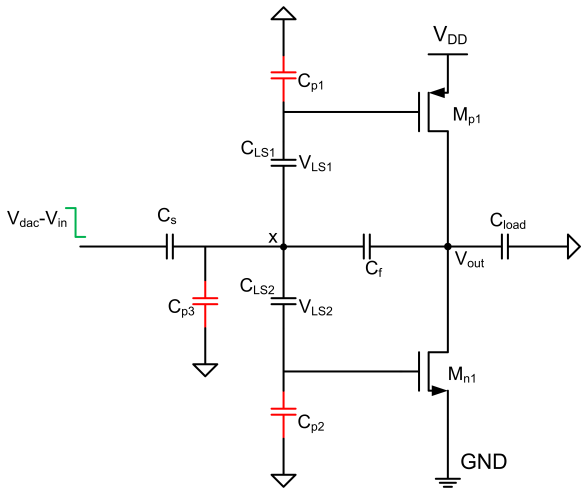


Figure 4.2: Parasitic capacitors associated with the class-AB amplifier of Figure 4.1.

rent is required for the amplifier. The increase in C_{px} also have effect on feedback factor (β) and closed loop gain (A_{CL}) of the amplifier as follows:

$$\beta = \frac{C_f}{C_s + C_{px} + C_f} \tag{4.3}$$

$$\begin{aligned} A_{CL} &= \frac{1-\beta}{\beta}\left(\frac{1}{1+\frac{1}{A\beta}}\right)(1-\exp^{-t/\tau}) \\ &= \frac{C_s + C_{px}}{C_f}\left(\frac{1}{1+\frac{1}{A\beta}}\right)(1-\exp^{-t/\tau}) \end{aligned} \tag{4.4}$$

Equation (4.3) shows that with the increase in C_{px}, β decreases. This results in a lower open loop gain ($A\beta$) and a lower small-signal bandwidth (f_{-3dB}) of the amplifier. The A_{CL} given in Equation (4.4) also deviates from the desired value due to C_{px} term in it. We have simulated and compared $A\beta$, A_{CL} and f_{-3dB} of the amplifiers as shown in Figures 3.9 and 4.1. Table 4.1 lists the parameters used for the comparison. Please note that we have kept the values of the sampling capacitor (C_s) and the feedback capacitor (C_f) the same. Therefore, the ideal closed-loop gain of the amplifier in this case is $0\,dB$.

Figure 4.3 shows $A\beta$ results and Figure 4.4 shows A_{CL} and f_{-3dB} results of the two class-AB amplifiers. Please note that we have annotated the class-AB amplifier

Table 4.1: Parameters used during the comparison of different class-AB amplifiers.

Parameter	Value
Supply voltage (V)	1
Biasing current (μA)	257.6
NMOS transistor dimension (μm)	$5.4(W) \times 0.72(L)$
PMOS transistor dimension (μm)	$12.6(W) \times 1.68(L)$

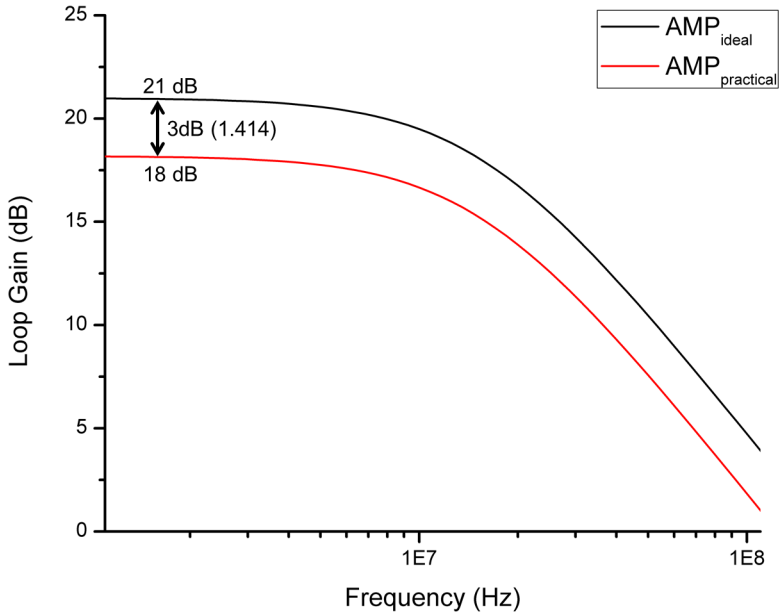


Figure 4.3: Open-loop gain $(A\beta)$ comparison of AMP_{ideal} and $AMP_{practical}$.

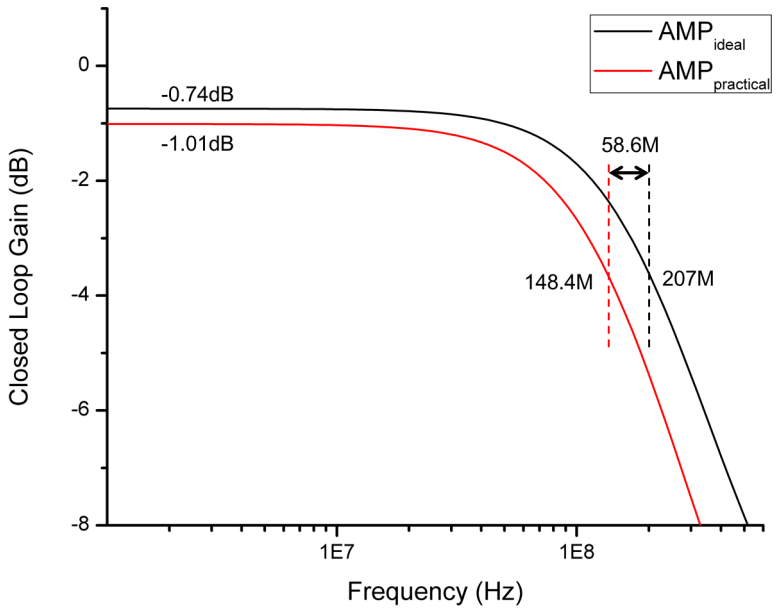


Figure 4.4: Small-signal closed-loop gain (A_{CL}) and bandwidth (f_{-3dB}) comparison of AMP_{ideal} and $AMP_{practical}$.

of Figure 3.9 as AMP_{ideal} and the class-AB amplifier of Figure 4.1 as $AMP_{practical}$. From the figures, we can see that all performance parameters like $A\beta$, A_{CL} and f_{-3dB} degrade for $AMP_{practical}$ due to the added parasitic capacitors from the level shifters.

Thermal Noise

In Section 3.2, we have discussed the integrated thermal noise power at the output of the MDAC. In this section, we analyze the effects of using capacitors as level shifters on the noise performance of the MDAC. The circuit schematic of $AMP_{practical}$ in the flip-around MDAC architecure is shown in Figure 4.1.

When the switches are opened at the end of the sampling phase (ϕ_1), noise is sampled on the capacitors. The integrated noise powers sampled across C_{LS1} and C_{LS2} are $\frac{kT}{C_{LS1}}$ and $\frac{kT}{C_{LS2}}$, respectively. During the amplification phase (ϕ_2), this noise is transferred to the output. Figures 4.5 and 4.6 show the noise situation during ϕ_1

and ϕ_2 of the MDAC.

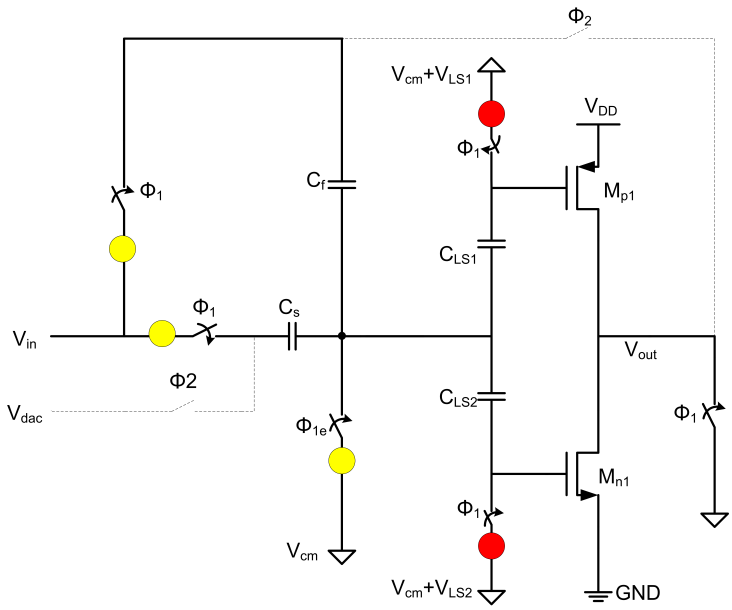


Figure 4.5: Noise of the MDAC with $AMP_{practical}$ during ϕ_1.

We can express the total integrated output noise power ($V^2_{n,out}$) of the MDAC by the end of ϕ_2 as

$$\begin{aligned} V^2_{n,out} &= \frac{kT}{C_f} + (\frac{kT}{C_s} + V^2_{n,dac})(\frac{1-\beta}{\beta})^2 + (V^2_{n,amp})(\frac{1}{\beta})^2 \\ &\quad + \frac{kT}{C_{LS1}} + \frac{kT}{C_{LS2}} \end{aligned} \tag{4.5}$$

where $V^2_{n,amp} = V^2_{n1,amp} + V^2_{n2,amp}$.

The last two terms of Equation (4.5) show the noise contributions of capacitor level shifters C_{LS1} and C_{LS2}. To reduce these noise contributions, we need to increase the size of C_{LS1} and C_{LS2} much higher than C_s and C_f. However, this increases C_{px} according to Equation (4.1), and thus reduces bandwidth and increases power consumption of the amplifier. We have also seen from Equation (3.29) that the noise contribution from the amplifier increases as β reduces. Table 4.2 lists the different noise contributors at the output of the MDAC for AMP_{ideal} and

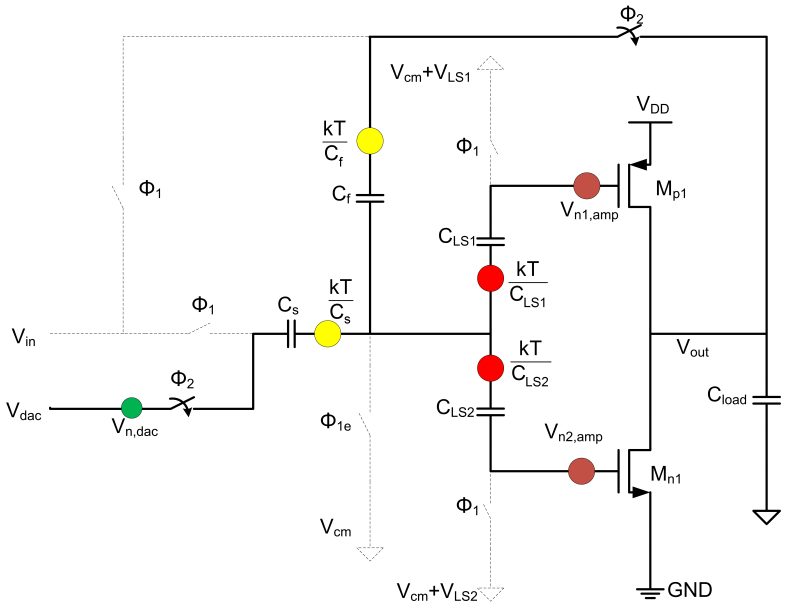


Figure 4.6: Noise of the MDAC with $AMP_{practical}$ during ϕ_2.

$AMP_{practical}$. Please note that the noise simulations have been performed large-signal in order to take the noise correlations of ϕ_1 and ϕ_2 phases into account. We have assumed that $C_{LS1} = C_{LS2} = C_s = C_f$ for the noise values listed in Table 4.2. Simulation results given in Table 4.2 show that $V_{n,out}$ of the MDAC with $AMP_{practical}$ is much higher than that with AMP_{ideal}.

Table 4.2: Simulated large-signal noise voltages of the MDAC with AMP_{ideal} and $AMP_{practical}$ (single ended).

Contributor	AMP_{ideal}	$AMP_{practical}$
Sampling noise voltage (μV)	75.32	143.7
Amplifier noise voltage (μV)	55.84	61.62
Total noise voltage (μV)	93.48	157.5

4.1.2 Proposed Class-AB Amplifier Topology

In this section, we propose a new class-AB amplifier topology that alleviates the problems discussed in the last section. The proposed amplifier topology is shown in Figure 4.7, where level shifting capacitors are removed completely and bias voltages are given directly to the gate of the MOS transistors during ϕ_1. Capacitors C_s and C_f are split into two equal halves while keeping their total values the same as before. Therefore, two identical negative feedback loops are created. Note that from now on, we will annotate this class-AB amplifier as $AMP_{proposed}$. The biasing circuit used to generate $(V_{cm} + V_{LS1})$ and $(V_{cm} + V_{LS2})$ voltages is shown in Appendix A.

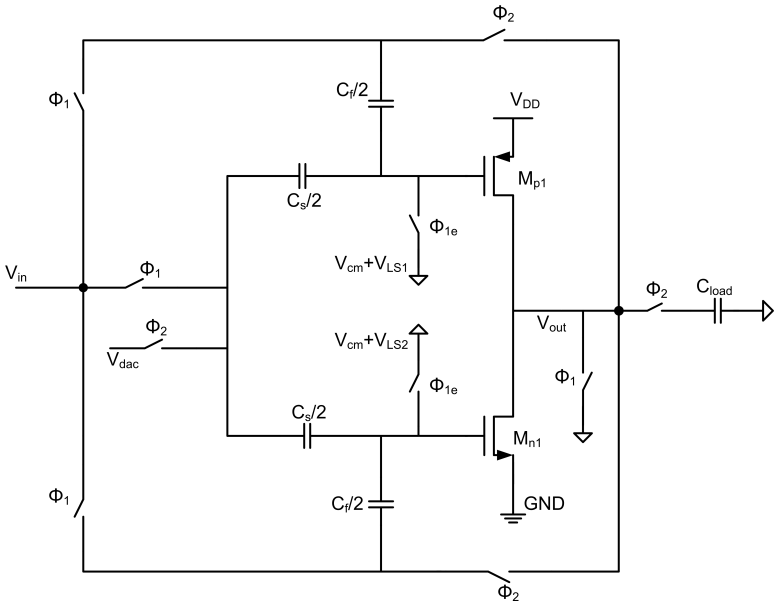


Figure 4.7: Proposed class-AB amplifier in a flip-around MDAC topology.

Gain and Bandwidth Comparison

We have simulated different performance parameters like $A\beta$, A_{CL} and f_{-3dB} of $AMP_{proposed}$ in order to make a comparison with AMP_{ideal} and $AMP_{practical}$. The simulation results are given in Figures 4.8 and 4.9, which show that $AMP_{proposed}$ achieves similar gain and bandwidth as AMP_{ideal}. Table 4.3 lists the simulation results for the different class-AB amplifiers.

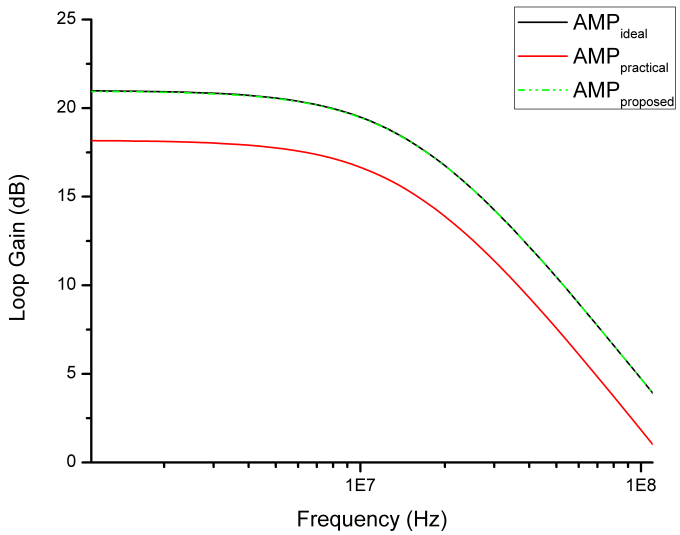


Figure 4.8: Loop gain comparison of different class-AB amplifiers.

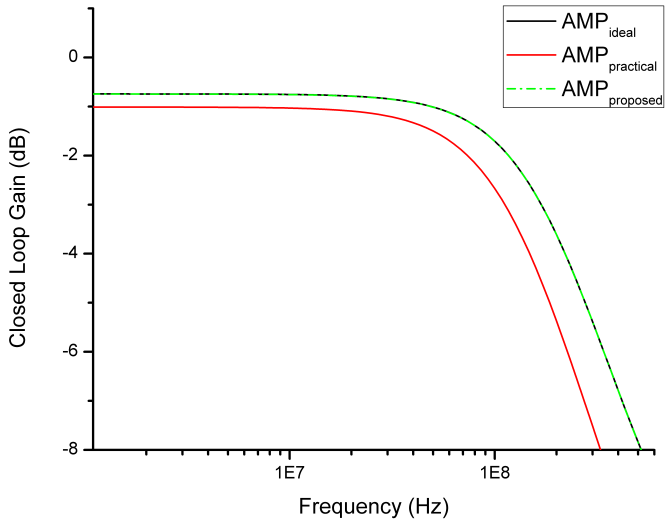


Figure 4.9: Small signal gain and bandwidth comparison of different class-AB amplifiers.

Table 4.3: Simulated gain and bandwidth of different class-AB amplifiers.

Performance	AMP_{ideal}	$AMP_{practical}$	$AMP_{proposed}$
Loop gain (dB)	20.97	18.17	20.95
Closed loop bandwidth (MHz)	207.01	148.38	206.84
Closed loop gain (dB)	-0.743	-1.011	-0.746

Thermal Noise Comparison

In the proposed amplifier topology, we have removed level shifting capacitors and also associated noise sources. Figure 4.10 shows the noise sources of the proposed class-AB amplifier during ϕ_1. Since we assume that $C_s = C_f = C$, noise power sampled across each of the capacitors of Figure 4.10 at the end of ϕ_1 is $\frac{kT}{C/2}$, which is shown in Figure 4.11(a).

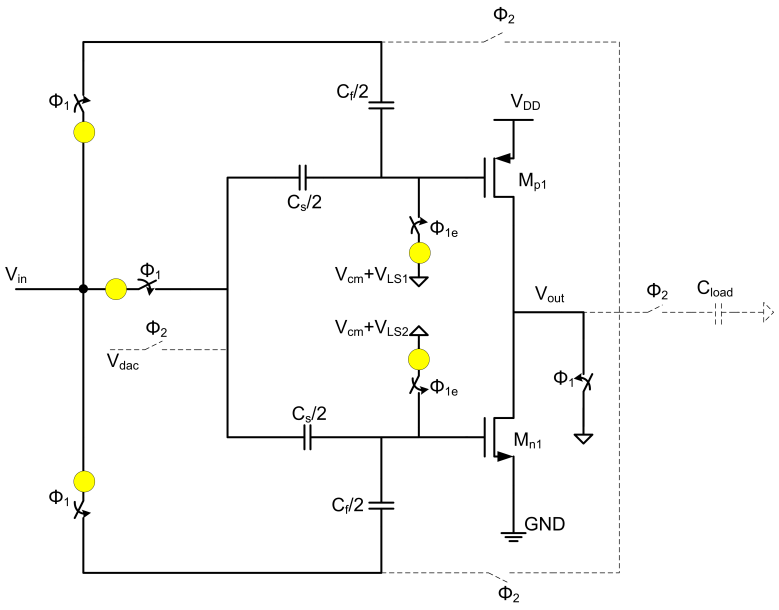


Figure 4.10: Noise sources of the MDAC with $AMP_{proposed}$ during ϕ_1.

During ϕ_2, all noise sources transfer to the output, but with different transfer functions. This noise transfer mechanism is illustrated in Figure 4.11, where we focus on the transfer of the sampling phase noise. Figure 4.11(b) shows that the

Table 4.4: Simulated large-signal noise voltages of the MDAC with different class-AB amplifiers (single ended).

Contributor	AMP_{ideal}	$AMP_{practical}$	$AMP_{proposed}$
Sampling noise voltage (μV)	75.32	143.7	76.89
Amplifier noise voltage (μV)	55.84	61.62	54.88
Total noise voltage (μV)	93.48	157.5	93.54

noise sampled across the feedback capacitors ($\frac{C_f}{2} = \frac{C}{2}$) are already at the output, but the noise sampled across the sampling capacitors ($\frac{C_s}{2} = \frac{C}{2}$) transfer to the output with a closed loop gain of 1. More detail about the noise transfer of various MDACs are given in Section 3.2.1. Since the noise sources from the top-half side and the bottom-half side of Figure 4.11 are mutually independent, charge redistribution occurs at the output. This has been shown in Figure 4.11(c), which results in a final sampling noise power equal to half of the sampling noise power from each side. The resultant sampling noise power at the output of the MDAC becomes $\frac{2kT}{C}$, which is exactly the same as the net sampling noise power when AMP_{ideal} is used as the residue amplifier in the MDAC.

Conclusion We have simulated the noise of $AMP_{proposed}$ and compared it with AMP_{ideal} and $AMP_{practical}$. Table 4.4 lists large-signal noise simulation results for the different class-AB amplifiers. From the results, we can see that $AMP_{proposed}$ has similar noise performance compared to that of AMP_{ideal}.

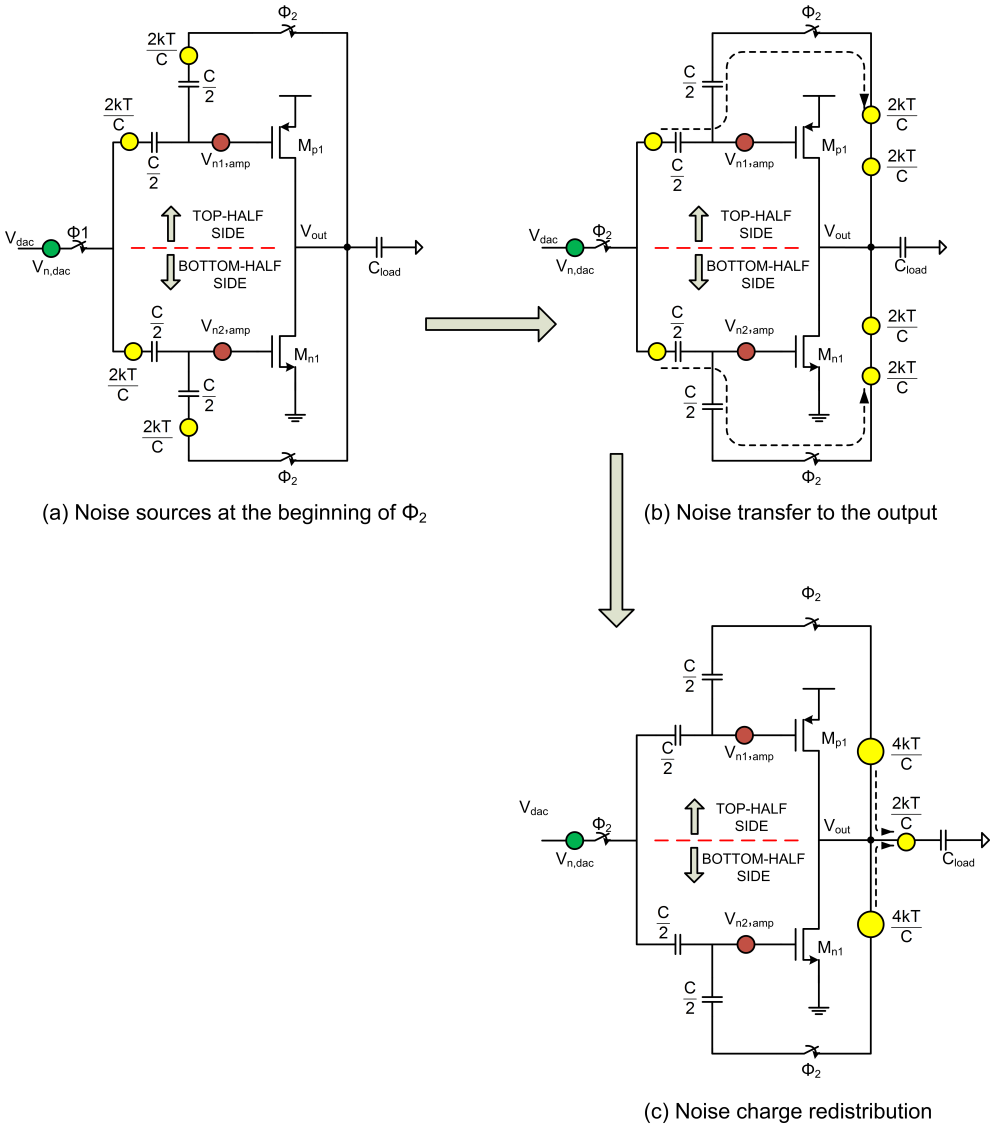


Figure 4.11: Noise transfer mechanisms of the MDAC with $AMP_{proposed}$ during ϕ_2.

4.2 Problems with the Flip-Around MDAC

In Section 3.1.2, we have discussed the fact that the flip-around MDAC topology has two inputs (i.e., the flip-around input and the residue input) and each of the input transfers to the output with a different gain. In this section, we discuss the problems related to the flip-around MDAC topology when the amplifier has finite loop gain and bandwidth.

We have seen from Figure 3.10 that $g_{m,eff}$ of the class-AB amplifier increases with the input signal level. But to keep the following analysis simple, we have assumed that $A\beta$ and f_{-3dB} are independent of any input signal level. So,

$$(1-\exp^{-T_{amp}/\tau})(\frac{1}{1+\frac{1}{A\beta}}) = constant = y \tag{4.6}$$

where T_{amp} is the amplification time. We can substitute Equation (4.6) in Equations (3.1) and (3.2) as

$$\begin{aligned} V_{out1} &= xV_{in} + (1-x)V_{in} \times y \\ V_{out2} &= -(V_{dac} - V_{in}) \times y \times gain_2 \end{aligned}$$

$$\begin{aligned} V_{out} &= V_{out1} + V_{out2} \\ &= (x(1-y) + y(1+gain_2))V_{in} - (y \times gain_2)V_{dac} \end{aligned} \tag{4.7}$$

Equation (4.7) resolves to the ideal result of Equation (3.4) if $y = 1$ and $gain_2 = 1$. Equation (4.7) shows that V_{in} and V_{dac} scale differently with any error in gain. As a result, the residue output signal of the MDAC deviates from the ideal residue output that we would like to have. We have also explained the same thing in a graphical way, considering the following two cases: (*i*) ideal case: when $A\beta$ and f_{-3dB} are infinite, and (*ii*) real case: when $A\beta$ and f_{-3dB} are finite. Please note that this graphical analysis has been done in MATLAB with the help of the equations derived before. In order to get a gain of 2 from the flip-around MDAC topology, we have used a capacitor ratio ($\frac{C_s}{C_f}$) of 1 and 3 for cases (*i*) and (*ii*) respectively.

Figure 4.12 shows the inputs of the flip-around MDAC, which are basically the same and independent of $A\beta$ and f_{-3dB} as expected.

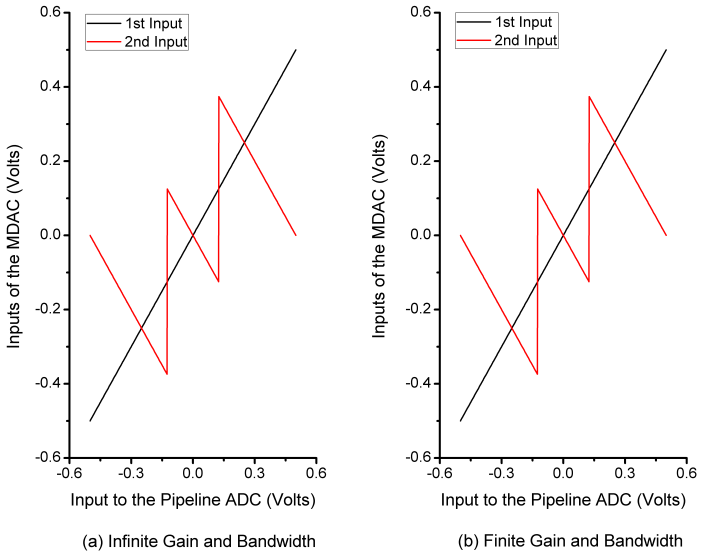


Figure 4.12: Inputs of the flip-around MDAC.

Figure 4.13 shows the transfer of the flip-around input to the output of the MDAC. For case (i), the flip-around input transfers to the output with a closed loop gain of 1 as can be seen from the figure. But for case (ii), the gain for the flip-around input becomes less than 1 due to static and dynamic error in the amplifier gain.

Figure 4.14 shows the transfer of the residue input to the output of the flip-around MDAC. Ideally (i.e., case (i)), the residue input transfers to the output with a inverting gain of 1. However, when $A\beta$ and f_{-3dB} of the amplifier are finite (i.e., case (ii)), the residue input signal transfers to the output with an error, as given in Equation 2.10. In this situation, since the gain for the flip-around input is less than 1, we need a gain higher than 1 for the residue input in order to reach a overall closed loop gain of 2. The final output can be derived by adding the individual outputs, which has been shown in Figure 4.15. We can see from the figure that the final residue output of the MDAC for case (ii) becomes distorted. It is especially the difference in behavior of these two inputs that make the final residue output signal of the flip-around MDAC distorted. In other words, the input signal V_{in} and

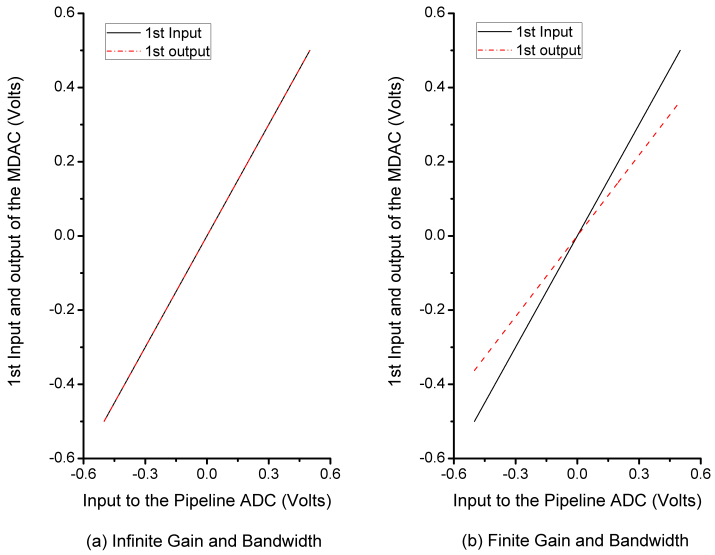


Figure 4.13: Transfer of the flip-around input to the output of the MDAC.

the reference signal V_{dac} of the flip-around MDAC scale differently with any error in gain, which makes it much harder to calibrate digitally. Moreover, if there is any comparator offset, the residue output signal of Figure 4.15 for case (ii) might saturate or overload the following pipeline stages, resulting in severe distortion.

We have seen from Chapter 3 that the flip-around MDAC topology achieves a higher SNR and a higher β compared to that of the charge amplifier MDAC. However, these improvements decrease when the capacitor ratio ($\frac{C_s}{C_f}$) increases. Since we are already using a capacitor ratio much higher than 1 in order to reach a gain of 2, the difference in SNR and β, between the flip-around MDAC topology and the charge amplifier MDAC topology are much smaller. All of these motivate to replace the flip-around MDAC topology with the charge amplifier MDAC topology, which is discussed in the next section.

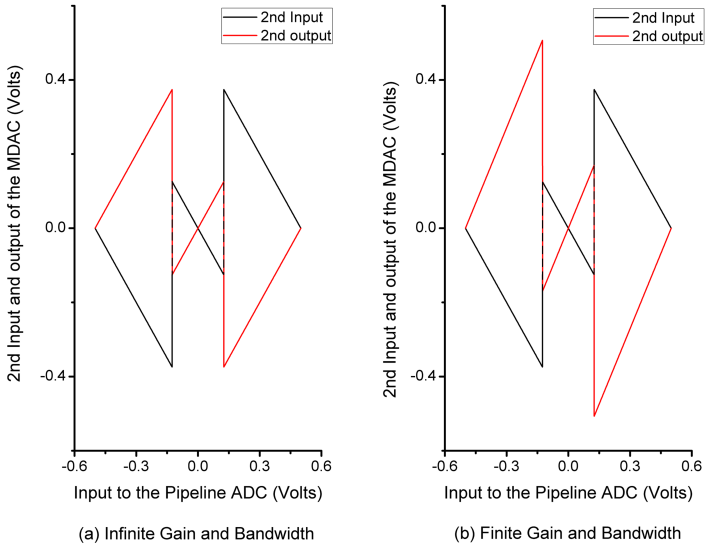


Figure 4.14: Transfer of the residue input to the output of the MDAC.

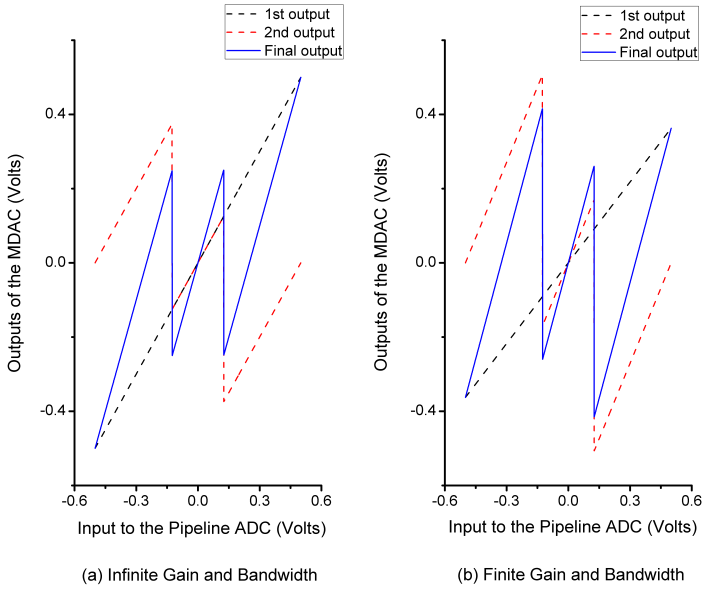


Figure 4.15: Final output of flip-around MDAC.

4.3 Moving to the Charge Amplifier MDAC

In the charge amplifier MDAC, V_{in} is sampled only across C_s. Thus, only the residue input transfers charge to the output during ϕ_2 as described in Section 3.1.2. Especially the fact that there is only one type of transfer function makes this topology more attractive for digital calibration. Figure 4.16 shows this input signal for the two cases mentioned in the last section. Please note that in order to get a gain of 2 from the residue amplifier, we have used a capacitor ratio ($\frac{C_s}{C_f}$) of 2 and 4 for cases (i) and (ii), respectively, which are different from that of the flip-around MDAC topology. For simplicity, the graphical analysis is done in MATLAB and $A\beta$ and f_{-3dB} are assumed to be independent of any signal level. Using Equations (4.6) and (3.6), we get the following expression of V_{out} for the charge amplifier MDAC:

$$\begin{aligned} V_{out} &= -(V_{dac} - V_{in}) \times y \times \frac{C_s}{C_f} \\ &= A_{CL} \times (V_{in} - V_{dac}) \end{aligned} \tag{4.8}$$

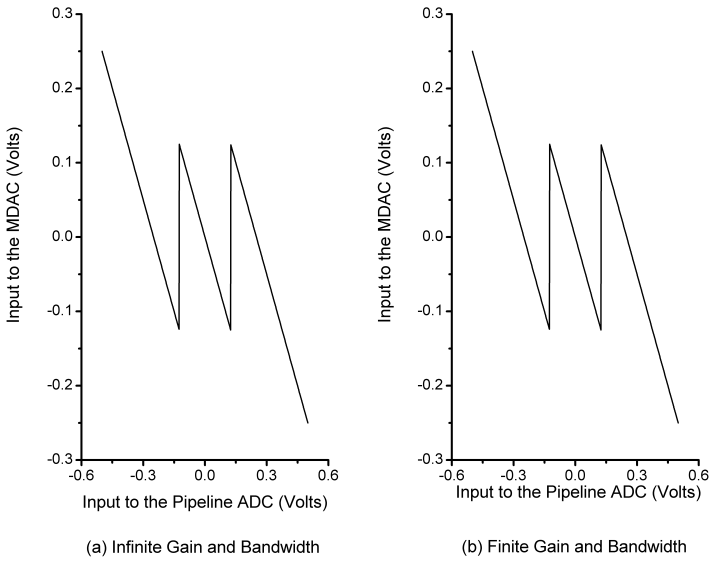


Figure 4.16: Input of the charge amplifier MDAC.

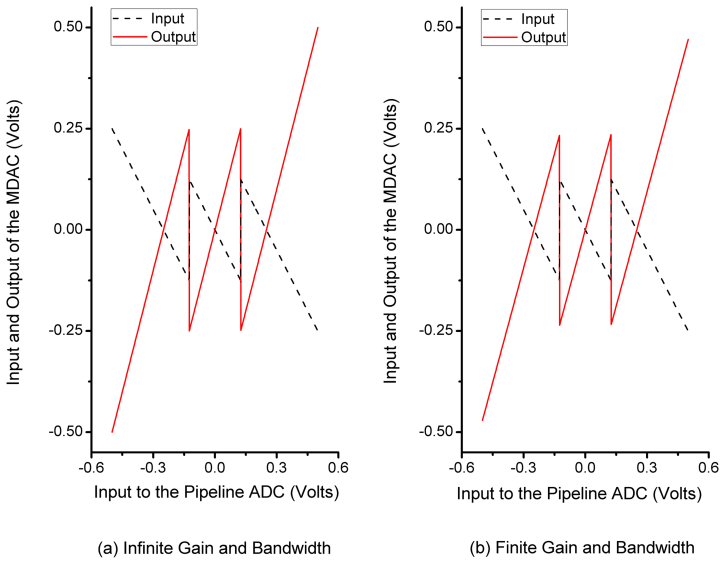


Figure 4.17: Output of the charge amplifier MDAC.

The output of the charge amplifier MDAC for both the cases are shown in Figure 4.17. For the first case of infinite $A\beta$ and f_{-3dB}, the residue output signal (V_{out}) is perfect as shown to the left of Figure 4.17. But for the case of limited $A\beta$ and f_{-3dB}, y is less than 1 and therefore, we have used $\frac{C_s}{C_f} = 4$ in order to achieve a closed loop gain of 2. The residue output signal in case (ii) is shown to the right of Figure 4.17. Equation (4.8) shows that V_{in} and V_{dac} scale the same way with the gain of an amplifier (i.e., $y\frac{C_s}{C_f}$). If the gain deviates from 2 due to any error, the residue input signal ($V_{in} - V_{dac}$) ensures that gain error and scales in the same way. Since it is like a gain error, digital calibration can be used easily to resolve this problem. Therefore, we have finally implemented a fully differential charge amplifier MDAC for the design of our pipeline ADC, which is shown in Figure 4.18.

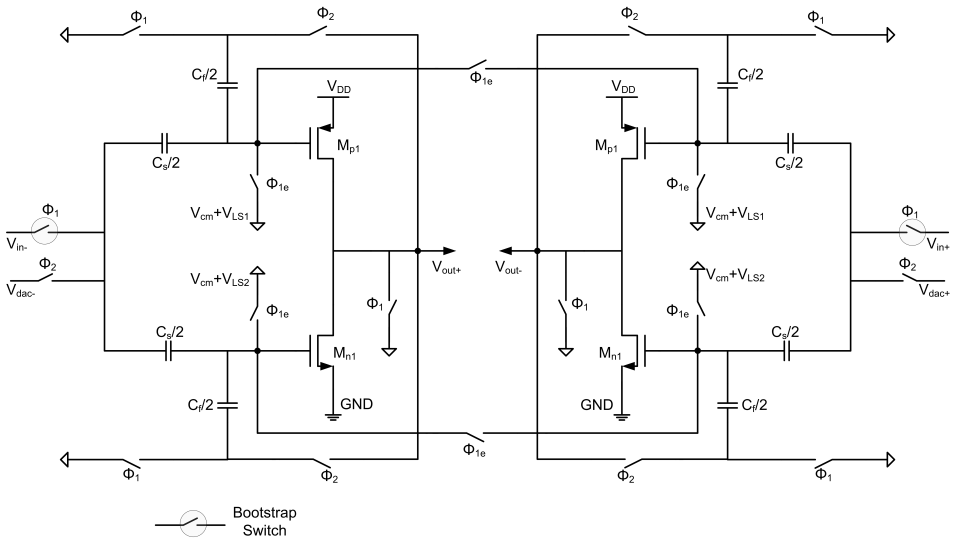


Figure 4.18: Fully differential charge amplifier MDAC.

4.4 MDAC Layout

The layout of the MDAC (as shown in Figure 4.18) has been done in TSMC 40nm CMOS technology. Since it's a fully differential design, the layout has been done carefully to make the two half-circuits as symmetrical as possible and to match each other. It is also important to match parasitics like metal wire capacitances, resistances, etc., of both the half-circuits in order to avoid any offset error. To do so, we have laid out the switches that are common to both sides of the MDAC in such a way that the number of dummy transistors seen from each side are the same.

This results in balanced parasitic capacitances seen from each side of the charge amplifier MDAC. Figure 4.19 shows the layout of the MDAC for the first pipeline stage except for the sub-DAC. Please note that this research work is a continuation of [11] and the coarse-ADCs and the sub-DACs from that work are reused for this design.

An array of metal-metal finger capacitors are used to implement C_s and C_f as shown in yellow in Figure 4.19. Unit capacitors are used and placed nearby in order to have better matching among the capacitor values. For the residue amplifier, even number of fingers are used for the transistors so that we do not need to keep track of the current direction. This also helps in achieving better matching of the amplifier.

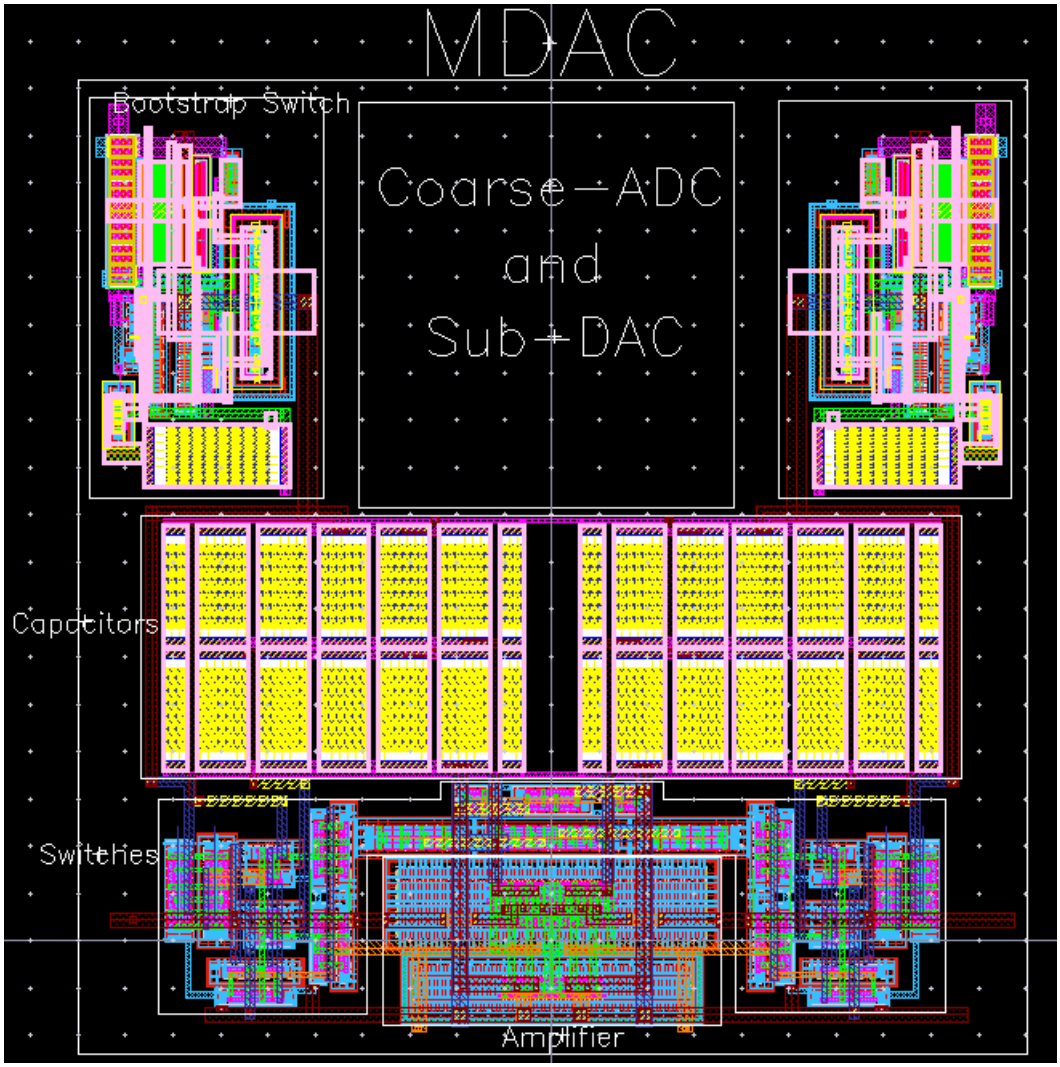


Figure 4.19: Layout of the fully differential charge amplifier MDAC for the first stage of the pipeline ADC.

An array of dummy transistors are used in all side of the amplifier to reduce the stress effects at the edges, so that all the transistors of the amplifier have the same characteristics (e.g., same threshold voltage).

The metal wires for the input and the output signals of the MDAC have the same physical direction so that interconnections between the successive pipeline stages become simpler. To route the supplies throughout the MDAC, the top metal layer ($M7$) is used in order to reduce the IR drop in the supply lines. $M7$ is also used to route metal wires connected to the virtual ground of the amplifier, in order to reduce any resistance associated with those wires, because it directly adds to the noise of the amplifier.

4.5 Summary

The topology of the residue amplifier and the MDAC have been described in this chapter. Problems related to capacitor level shifters in the existing class-AB amplifier topology have been discussed together with a proposal of a new class-AB amplifier topology. The proposed class-AB amplifier topology shows similar performance compared to the class-AB amplifier topology that uses ideal voltage sources as level shifters. Due to finite accuracy of the residue amplifier, we have seen several problems related to the flip-around MDAC topology and decided to use the charge amplifier MDAC topology for our pipeline ADC design. Finally, the layout of the MDAC for the first stage of the pipeline ADC has been described along with its various considerations.

Chapter 5

Pipeline ADC design

To test the design of our class-AB amplifier, the amplifier is used in a previously designed pipeline ADC [11]. This chapter first presents the architecture of that pipeline ADC [11], which has been used as a test vehicle for our amplifier design. A new timing scheme is proposed for the pipeline ADC to resolve problems encountered with the conventional timing scheme, used in [11]. In conclusion, the effectiveness of an ideal digital calibration in terms of improving the non-linearity of the first pipeline ADC stage is demonstrated.

5.1 ADC Architecture

The system architecture of a pipeline ADC and its basic operation has been discussed briefly in Section 2.1. There are 10 stages in the pipeline ADC used in our design, among which the first 9 stages are 1.5-bit/stage and the final stage is a 5-bit back-end flash ADC. For each 1.5-bit/stage, the charge amplifier MDAC of Figure 4.18 together with the coarse-ADC and the sub-DAC designed in [11] are used. The extra bits added in the back-end flash ADC help to make the quantization noise much smaller than the thermal noise and improve the error estimation accuracy.

Figure 5.1 shows the architecture of the pipeline split-ADC, where two identical pipeline ADCs are used. This architecture is exactly the same as implemented in [11]. The split-ADC digital calibration scheme will be used as a test vehicle for our design to measure the improvements that the proposed class-AB residue amplifier brings over the conventional high accuracy residue amplifiers.

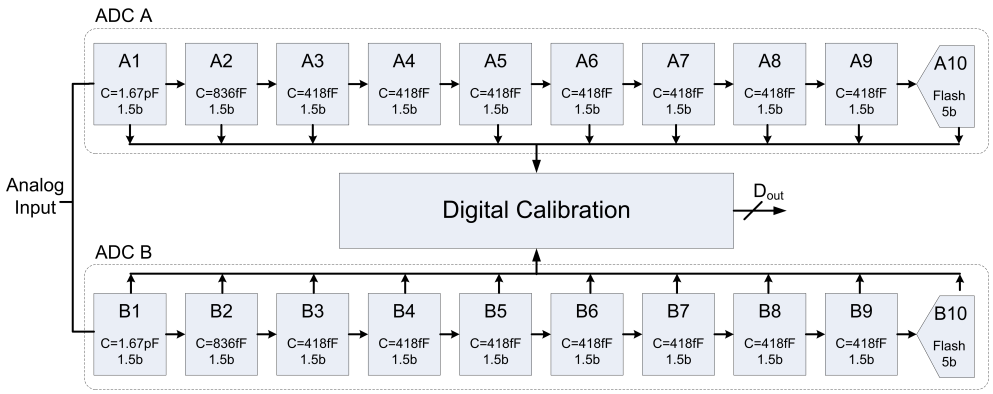


Figure 5.1: SHA-less pipeline ADC architecture [11] used for our design.

The pipeline ADC architecture used does not include any dedicated sample-and-hold (SHA) amplifier at the front, because it consumes a lot of power without being an essential part of the quantization process. Since without a SHA, the signal at the input of the pipeline ADC can move continuously upto frequencies of $\frac{f_s}{2}$, the first stage MDAC and the coarse-ADC have to sample at the same moment to capture the same signal. Any deviation in the sampling moment causes timing or aperture error [11], which means the signal processed by the coarse-ADC and the MDAC are different. This type of error can be dealt with to some extent, by using overrange in 1.5-bit/stage as discussed in Section 2.1.1.

In order to distribute the total thermal noise budget among the pipeline stages, we should know the optimum capacitor scaling. If all stages have the same capacitance, then the last few stages contribute very little noise but still consume the same power as the first stage. On the other hand, if the capacitors are scaled down quadratically with inter-stage residue amplifier gain, noise contributions from all the pipeline stages become equal. To reduce the total thermal noise, the capacitors of the first few stages need to be increased. However, to keep the same speed of the amplifier ($\propto \frac{g_m}{C}$) in those stages, the power consumption has to go up. Cline et al. [25] have shown that there is a optimum capacitor scaling in terms of power consumption, which is approximately equal to the inter-stage amplifier gain. In [11], capacitors are scaled with the inter-stage gain (i.e., 2) only two times. Therefore, we have distributed the thermal noise budget among the pipeline stages considering the same stage scaling as in [11]. This results in a sub-optimal stage scaling with re-

gards to the overall power consumption of the pipeline ADC, but saves some design time.

5.2 Timing Scheme

Normally in a pipeline ADC without a SHA, only the first stage is critical for the aperture error. This is because only the first stage is sampling a moving signal. However, due to the incomplete settling of the residue amplifier, the timing or the aperture error remains critical, also for the later stages of the pipeline ADC in our design. Please note that after 1τ or 2τ settling, the signal is still moving considerably. This section first discusses the timing scheme of a conventional SHA-less pipeline ADC. Then, it describes timing problems related to our design and proposes a solution.

5.2.1 Conventional timing scheme

The residue amplifier in a pipeline ADC needs to provide accurate amplification when it is not supported by any digital calibration. To achieve this, high gain amplifiers using negative feedback are implemented [18]. The amplifier also needs to provide a large bandwidth to achieve the required settling accuracy in a specified time. As a result, the output signal from such an amplifier almost behaves like a held signal for the latter part of the amplification period. This has been illustrated in Figure 5.2.

At the input of the first stage of the pipeline ADC, both the MDAC and the coarse-ADC samples at the same moment to avoid any aperture error. This has been shown in Figure 5.3, where the green and red down-arrow represents the sampling moment of the coarse-ADC and the MDAC, respectively. Note that for the first stage there is only one down-arrow, which means that the sampling moment of the MDAC and the coarse-ADC are the same. It also shows that if the MDAC of the first stage samples at the end of the sampling period, there would be a big difference in the input signal sampled by the MDAC and the coarse-ADC. In the later stages of the pipeline chain, for example, in the second stage, the sampling phase duration of the MDAC is approximately half of the sampling period ($t \approx \frac{T_s}{2}$), whereas the coarse-

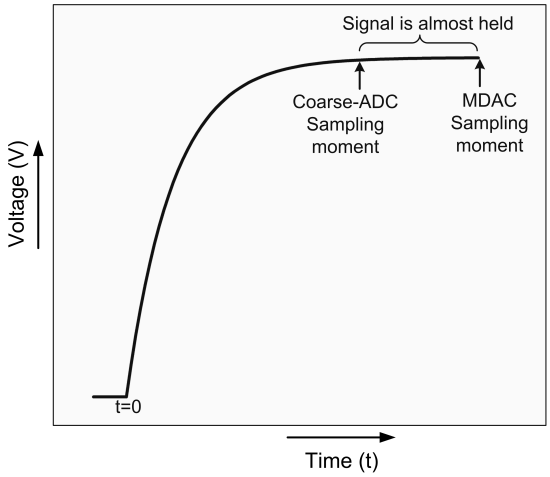


Figure 5.2: Output voltage signal of a conventional residue amplifier during the amplification phase.

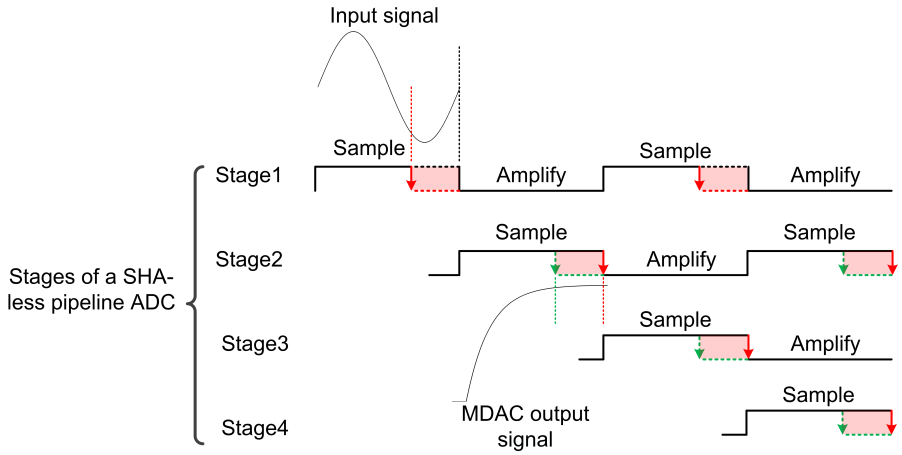


Figure 5.3: Conceptual timing diagram of a SHA-less pipeline ADC [11], when amplifiers settle to a high accuracy.

ADC sampling phase duration is still the same as before. This is also illustrated in Figure 5.3 by showing the green down-arrow appearing before the red down-arrow. Please note that the sampling phase duration of a coarse-ADC always needs to be less than $\frac{T_s}{2}$. This allows sufficient decision time for the comparator so that it can select the proper sub-DAC reference level before the start of the amplification period.

When the residue amplifier of the first stage operates (i.e., ϕ_1 of the second stage), the signal at the output of the amplifier behaves more like a held signal as shown in Figure 5.2. As a result, the signal sampled by the MDAC and the coarse-ADC remains almost the same, even though there is a difference in their sampling moment. The resulting small error can be tolerated easily, thanks to the large overrange ($V_{ref}/4$) of the 1.5-bit per stage architecture. Figure 5.4 shows this conventional timing scheme of the SHA-less pipeline ADC, which is similar to that in [11].

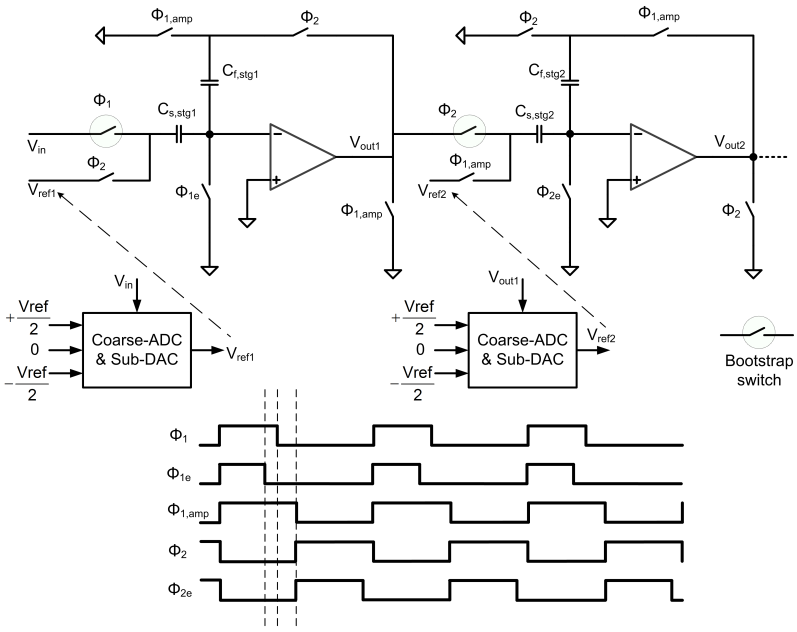


Figure 5.4: Timing scheme of a conventional SHA-less pipeline ADC [11].

5.2.2 Modified Timing Scheme

Due to the incomplete settling of the residue amplifier, we can not use the conventional timing scheme of the pipeline ADC for our design. There are mainly two factors contributing towards this: (1) large difference in the sampled signal between the MDAC and the coarse-ADC and (2) inter-symbol-interference (ISI). When the amplifier is not settled completely, the signal at the output of the amplifier can not be considered as a held signal. Therefore, even for the latter stages of the pipeline ADC, the sampling moment of the MDACs and the coarse-ADCs need to be the same, in order to avoid any large aperture error. This is illustrated in Figure 5.5, where the red down-arrow indicates the sampling moment of both the MDACs and the coarse-ADCs.

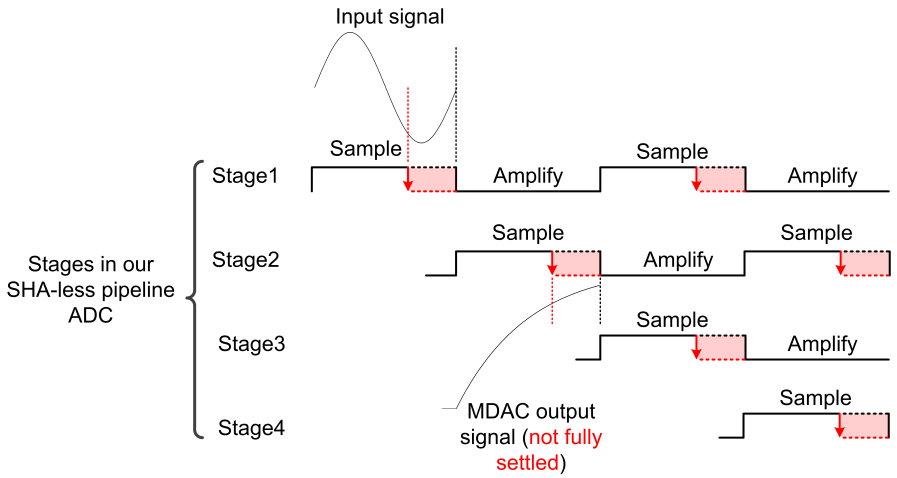


Figure 5.5: Conceptual timing diagram of our SHA-less pipeline ADC design with incomplete amplifier settling.

To describe the problem of ISI, we consider only the first two stages of the pipeline ADC as shown in Figure 5.6. During the sampling phase of the first stage, the output of the first stage residue amplifier is tied to a common-mode signal, V_{cm}. At that time, the second stage is in the amplification phase, thus amplifying its residue signal. The green line of Figure 5.6 indicates this phase. At the end of this phase, the voltage at the two sides of the second stage sampling switch (shown in red in Figure 5.6) are different. This voltage difference depends on the second stage sub-DAC reference level (V_{ref2}), which in turn depends on the output signal of the

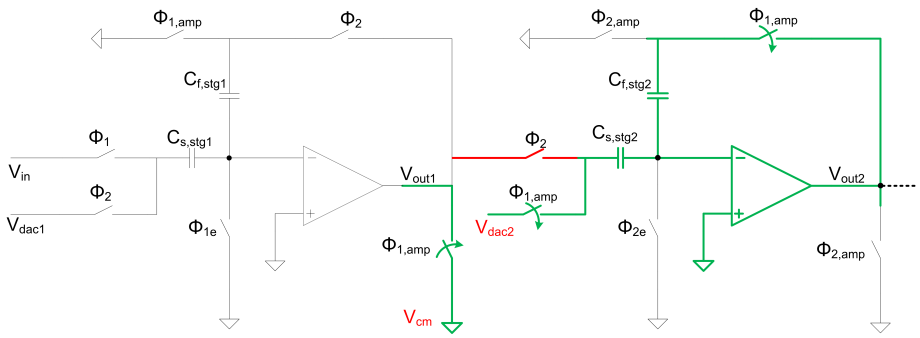


Figure 5.6: Two pipeline stages to illustrate the ISI.

first stage. Thus in ϕ_2, when the second stage sampling switch turns on, the first stage residue amplifier has to reset the memory (i.e., the charge stored across C_{s_stg2}) and then start amplifying its own input residue signal. It takes a significant amount of time of settling for this memory of the previous sample to disappear. However, in this design we try to settle only to a few τ. Therefore, This results in a memory effect or ISI, which eventually leads to distortion.

Figure 5.7 shows the proposed timing scheme of the pipeline ADC to deal with both of the above problems. First of all, the sampling instant of the the coarse-ADCs and the MDACs have been made equal for all the pipeline stages as shown in Figure 5.5. This resolves the first problem, since the coarse-ADCs and the MDACs are now sampling the same signal. Next, switches have been introduced to reset the sampling capacitors (C_s) of the pipeline stages. To reset the sampling capacitor (C_{s_stg2}) of the second stage, we do the following: after the amplification phase of the second stage (i.e., sampling phase of the first stage), switches with ϕ_1 signals turn off. Then, we turn on the reset switch (ϕ_{rst2}) and the bottom plate sampling switch ($\phi 2e$) to reset C_{s_stg2} to the same common mode voltage (V_{cm}) as that of the first stage amplifier. As a result, the voltage difference across the second stage sampling switch (shown in red in Figure 5.7) becomes almost zero and independent of the input signal, thus removing any ISI.

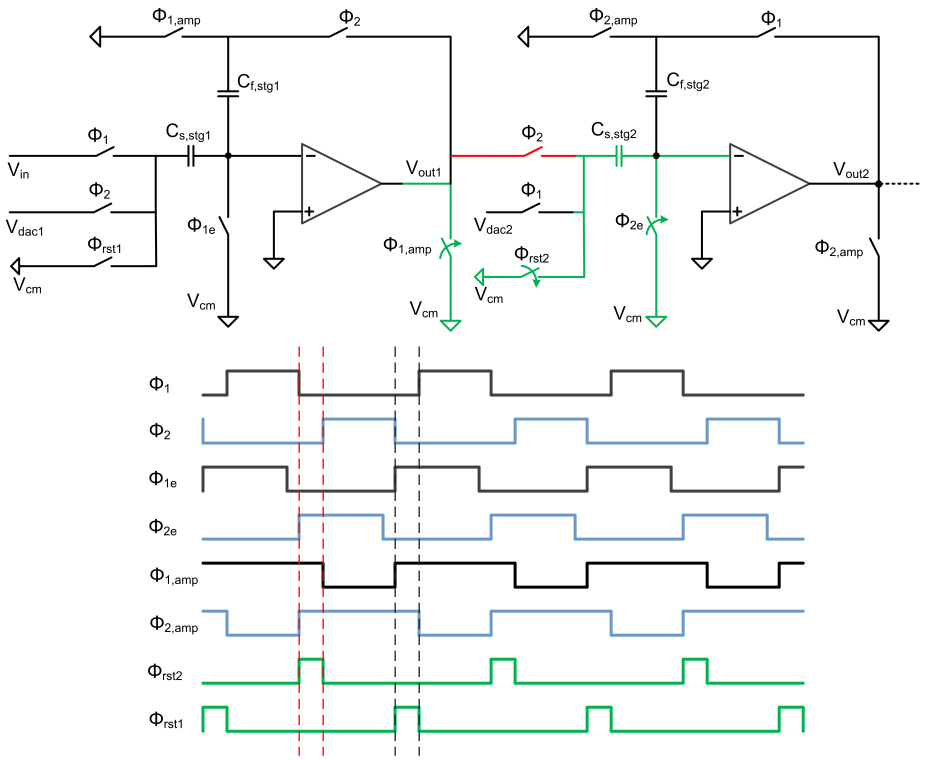


Figure 5.7: Modified timing scheme (coarse-ADC and sub-DAC not shown).

5.3 Results: Ideal Digital Calibration

In Section 2.1.2, we have described the foreground (ideal) digital calibration that has been used during our design. Please note that later on, this ideal calibration will be replaced by a background digital calibration scheme called split-ADC [11]. In this section, we have investigated how much improvement in linearity can be realized by doing an ideal digital calibration. The block diagram of Figure 2.5 has been used as the conceptual test bench to test the ideal calibration scheme, where only the first pipeline ADC stage is considered. We have used different output signal swings to observe the linearity behavior, both before and after doing the calibration. We have also swept the supply voltage ($\pm 5\%$) from $0.95V$ to $1.05V$, to observe the sensitivity of the proposed class-AB residue amplifier to the supply voltage (V_{dd}) variation. Note that, in this analysis, ideal digital calibration has been used to correct for the non-linearities upto the 5th order. Moreover, in situations when no digital calibration is utilized, the digital back-end uses a digital gain of 2 to reconstruct the

input signal.

Figure 5.8 shows the linearity performance of the first stage of the pipeline ADC for different output signal swings and supply voltages, both before and after doing the ideal digital calibration. As expected, we can see from the figure that when the output signal swing is low i.e., $1.2V$ peak-to-peak differential, the linearity of the pipeline stage is better, both before and after doing the digital calibration. Also, the linearity performance does not vary much with the supply voltage variation. In Section 2.1.2, we have mentioned that the ideal digital calibration works perfectly as long as the system remains exactly the same during the calibration phase and the test phase. When the signal swing at the output gets higher, the CMOS switches used in the MDAC cannot reset circuit nodes perfectly, thus limiting the achievable linearity.

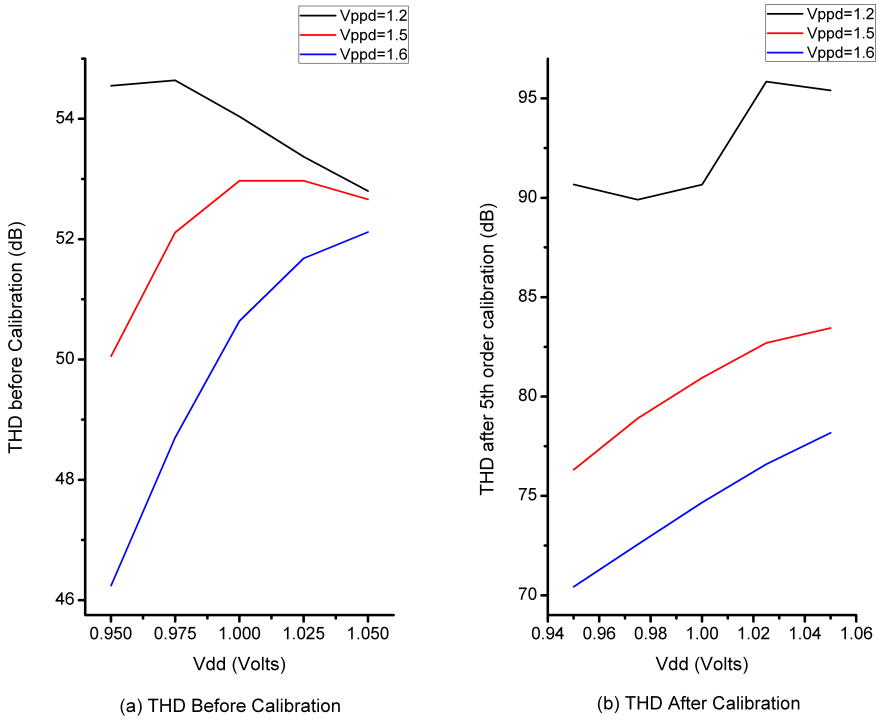


Figure 5.8: Linearity of the residue amplifier before and after doing the ideal digital calibration.

Figure 5.9 shows the THD and the SNR results of the first stage of the pipeline

ADC for different output swings and supply voltages. As expected, SNR improves when the signal level at the output increases. In all the cases shown in Figure 5.9, the linearity does not limit the achievable SNDR after doing the calibration. The resulting SNDR is shown in Figure 5.10, where the SNDR is maximum for most of the supply voltage range for an output signal swing of $1.5V$ peak-to-peak differential. Thus for our design, we have chosen an input or output signal swing of $1.5V$ peak-to-peak differential. Figure 5.10 also shows that the resulting SNDR is insensitive to supply voltage variations.

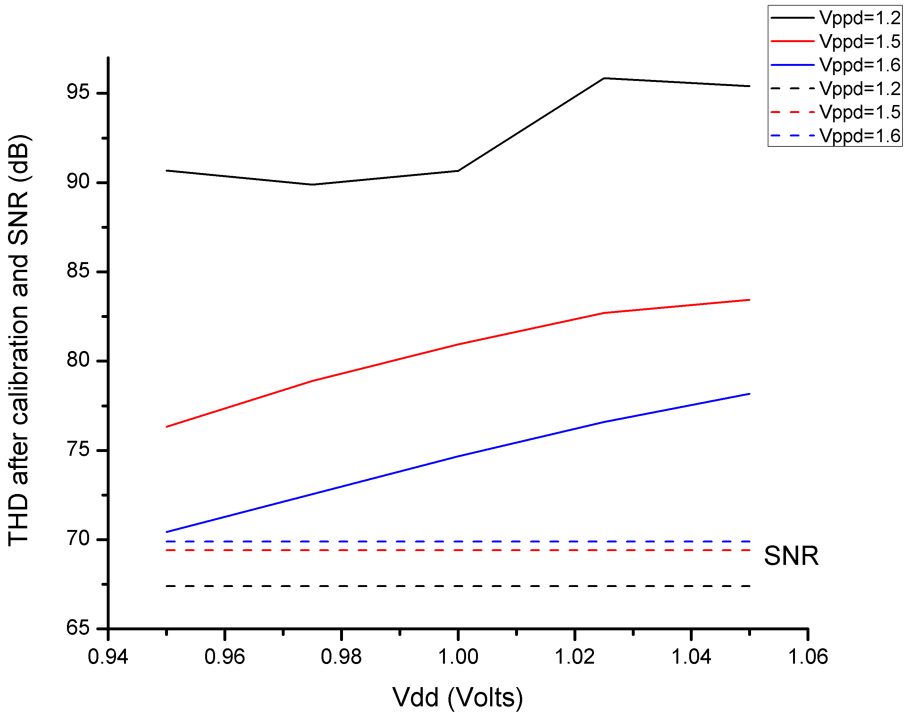


Figure 5.9: THD and SNR after ideal digital calibration.

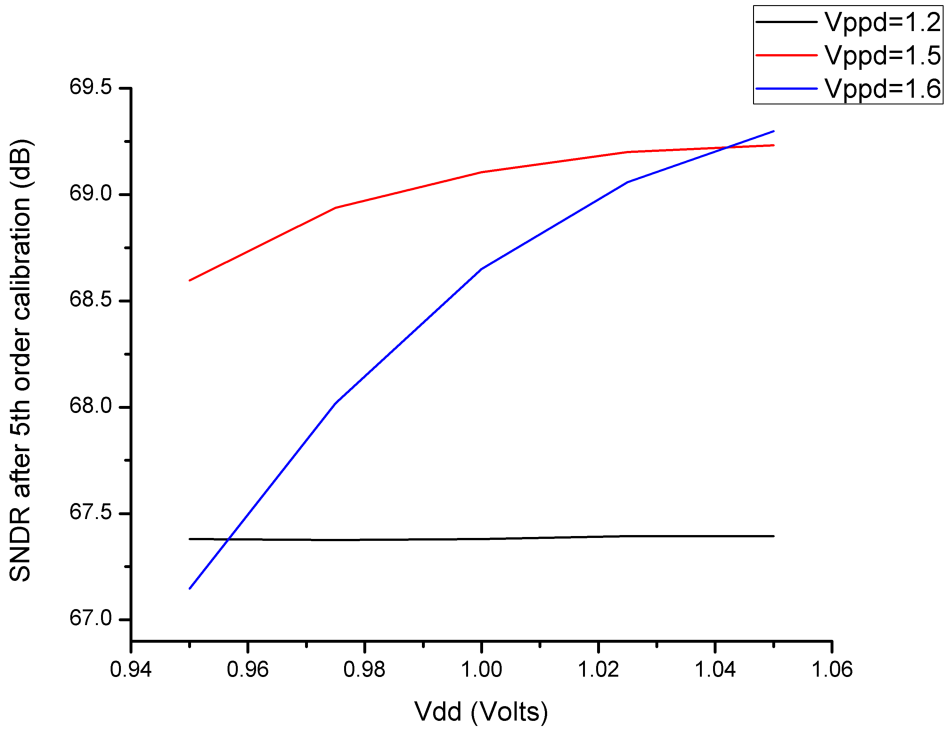


Figure 5.10: SNDR of the amplifier after ideal digital calibration.

5.4 Summary

In this chapter, the architecture of the pipeline ADC has been discussed. The capacitor scaling (or the stage scaling) used in our design has been explained. The problems with the conventional timing scheme of a SHA-less pipeline ADC, when the residue amplifiers do not settle completely, have been discussed. To address these problems, a new timing scheme of the pipeline ADC has been proposed. Finally, the results after doing the ideal digital calibration have been shown.

Chapter 6

Simulation Results

The simulation results of different performance parameters like noise, linearity, large-signal gain and power consumption for the pipeline half-ADC are presented in this chapter. Figures-of-Merit (FOMs) of the pipeline ADC are calculated and compared with other state-of-the-art ADC designs.

6.1 Power Consumption

In Figure 4.18, we have shown the fully differential charge amplifier MDAC that has been used in the pipeline ADC. The layout of the first stage MDAC has been shown in Figure 4.19. We have simulated the power consumption of the first stage MDAC using large-signal analysis, from both schematic view and extracted layout view. For the purpose of this simulation, we have applied input steps of various amplitudes to the MDAC and observe the current consumption. Note that the extracted layout view of the MDAC is C-extracted, which means that it does not introduce any parasitic resistances. This is shown in Figure 6.1 for both schematic and extracted layout views, where the red dotted line indicates the average current of the MDAC. As been discussed in Section 3.3.3, a class-AB amplifier consumes more current when the input signal level gets higher, and thus we can take the average current as an estimation of the current consumption in the amplifier (or in the MDAC).

Please note that the biasing current of the class-AB amplifier in schematic and extracted layout views are adjusted so that we can achieve a large-signal closed-loop gain of 2 within the allowed amplification time. As a result, the power consumption

of the first stage MDAC in extracted layout view is approximately 20% higher than that in schematic view, to reach the same gain of 2. This is due to the extra parasitic capacitances introduced in extracted layout view. The power consumption of the first stage MDAC together with the information about the stage scaling are used to calculate the total power consumption of the pipeline half-ADC, as shown in Table 6.1. Please note that the total power consumption of the pipeline half-ADC does not include the power of the digital calibration and also that of the biasing block and references.

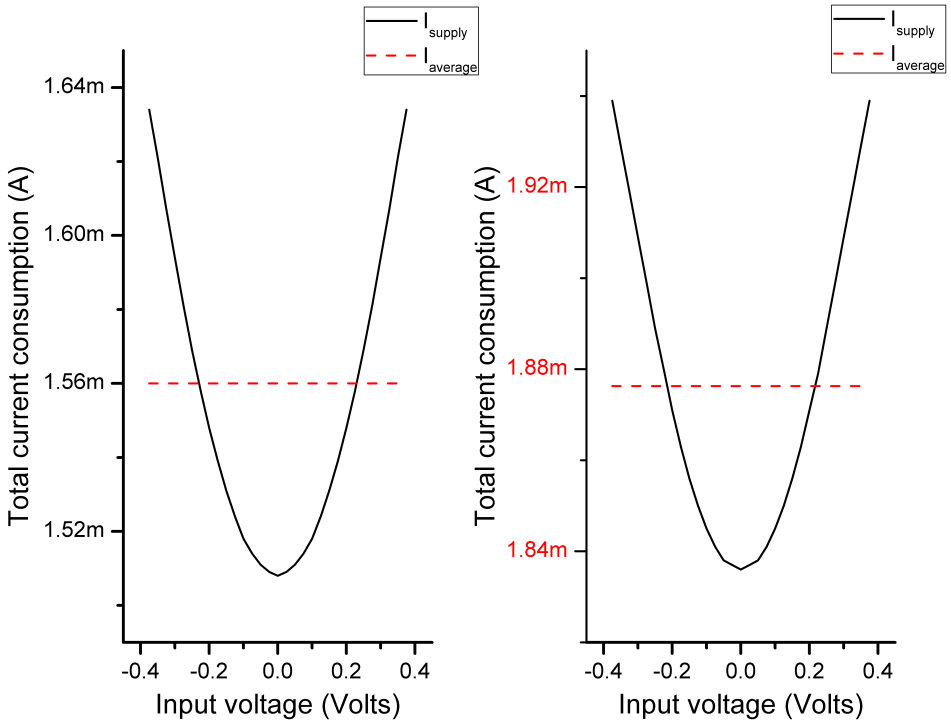


Figure 6.1: Simulated current consumption of the first stage MDAC for the pipeline half-ADC.

Table 6.1: Calculation of total power consumption of the pipeline half-ADC

Block	Power Consumption (mW)	
	Schematic	Extracted Layout
1st stage MDAC	1.56	1.88
1st stage comparator	0.022	0.022
Total amplifier power	5.46	6.58
Total comparator power	0.484	0.484
Total Power (half-ADC)	5.944	7.064

6.2 Noise

Table 6.2: Noise breakdown among the pipeline ADC stages.

Stage	Capacitor	Noise power	Input-referred noise power
Stage 1	1	N	N
Stage 2	0.5	$2N$	$\frac{2N}{2^2}$
Stage 3	0.25	$4N$	$\frac{4N}{2^2 2^2}$
Stage 4	0.25	$4N$	$\frac{4N}{2^2 2^2 2^2}$
$\vdots$	$\vdots$	$\vdots$	$\vdots$
Stage 10	0.25	$4N$	$\frac{4N}{(2^2)^9}$
			sum of stages 1-10 = $1.833N$

The noise behavior of the first stage MDAC (as shown in Figure 4.18) is simulated in large-signal with the V_{in} terminal connected to V_{cm}. The noise from the

coarse-ADC is ignored due to the large overrange in the 1.5-bit per stage design. In Section 5.1, we have explained that the stage capacitors are scaled down only twice in our design. The thermal noise distribution among the pipeline stages according to this stage scaling is shown in Table 6.2. We can see from the table that the total input-referred differential noise power of a pipeline ADC is 1.833 times greater than the input-referred differential noise power of the first pipeline stage (N).

Table 6.3: SNR calculation of the pipeline half-ADC

Parameter	Design	
	Schematic	Extracted Layout
Peak input signal (V diff.)	0.75	0.75
RMS input signal (V diff.)	0.53	0.53
First stage noise power (V^2 input referred diff.)	3.08×10^{-8}	3.35×10^{-8}
Total noise power (V^2 input referred diff.)	5.65×10^{-8}	6.14×10^{-8}
SNR (dB)	67	66.6

Table 6.3 shows the SNR calculation of the pipeline half-ADC from schematic and extracted layout views. The input-referred differential noise power of the first pipeline stage is $0.4dB$ higher in extracted layout view compared to that in schematic view. This is because in extracted layout view, extra parasitic capacitances are introduced at the virtual ground node of the amplifier, which is the most sensitive node of the circuit. As a result, the noise gain of the amplifier increases, resulting in more noise. Due to this reason, the SNR of the pipeline half-ADC in extracted layout view becomes $0.4dB$ lower than that in schematic view.

6.3 Linearity and Large-Signal Gain

In this section, we discuss the simulation results of some large-signal behaviors such as linearity and large-signal gain. The results are shown for both the MDAC and the first stage of the pipeline half-ADC.

6.3.1 MDAC Simulation

We have simulated the linearity behavior of the MDAC of Figure 4.18 in two types of views, namely schematic and extracted layout. While doing the simulations, we have connected $V_{dac}-$ and $V_{dac}+$ signals of Figure 4.18 to the common-mode voltage V_{cm}. Two-tone input signals of $0.75V$ peak-peak differential (p-p diff.) each close to $\frac{f_s}{2}$ are applied to the MDAC of Figure 4.18, thus resulting in an approximate output voltage of $1.5V$ p-p diff.

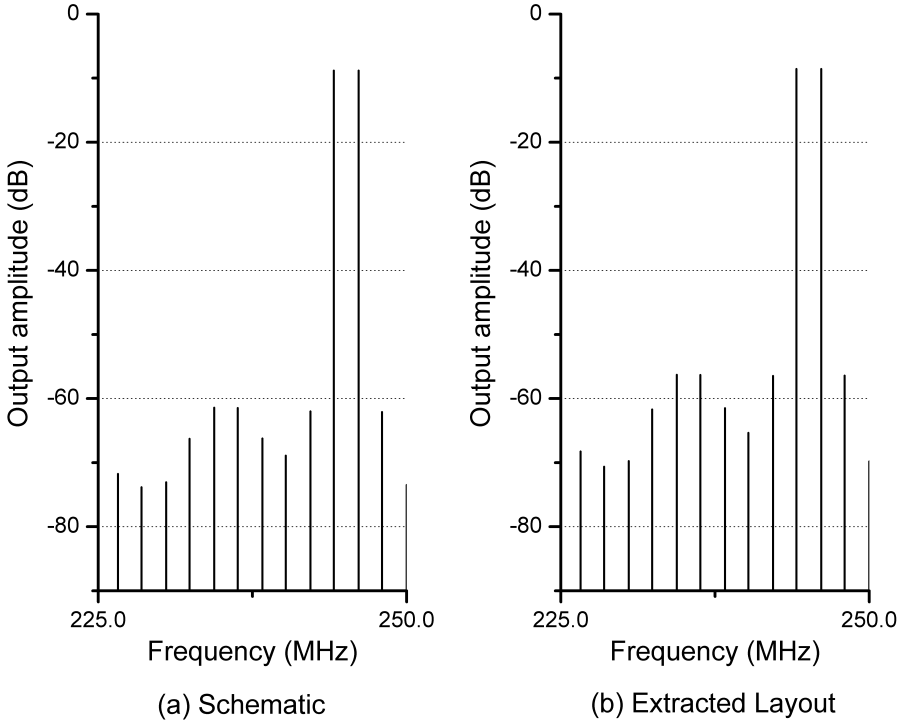


Figure 6.2: Two-tone simulation results of the charge amplifier MDAC.

Figure 6.2(a) and (b) display the two-tone simulation results of the charge amplifier MDAC using schematic and extracted layout views respectively. We can see from the figure that the IM3 tones resulting from extracted layout view are $5.3dB$ higher (i.e., degraded IM3) than that from schematic view. This might be due to the fact that in schematic view, the two half-circuits are perfectly matched resulting in a better suppression of the even order tones. We have tried to match the lay-

out design of both the half-circuits of the MDAC as good as possible. However, it can never be perfect, thus resulting in a slightly higher non-linearities in extracted layout view. Please note that matching only takes care of even order tones, and thus better matching should not improve IM3. However, if there are even order tones due to any mismatch, then they will also produce odd order tones through the feedback [19] and degrade IM3 performance. Another reason for the degradation of linearity of the MDAC in extracted layout view could be due to the increased parasitic capacitances at the virtual ground node of the amplifier, thus making $A\beta$ lower.

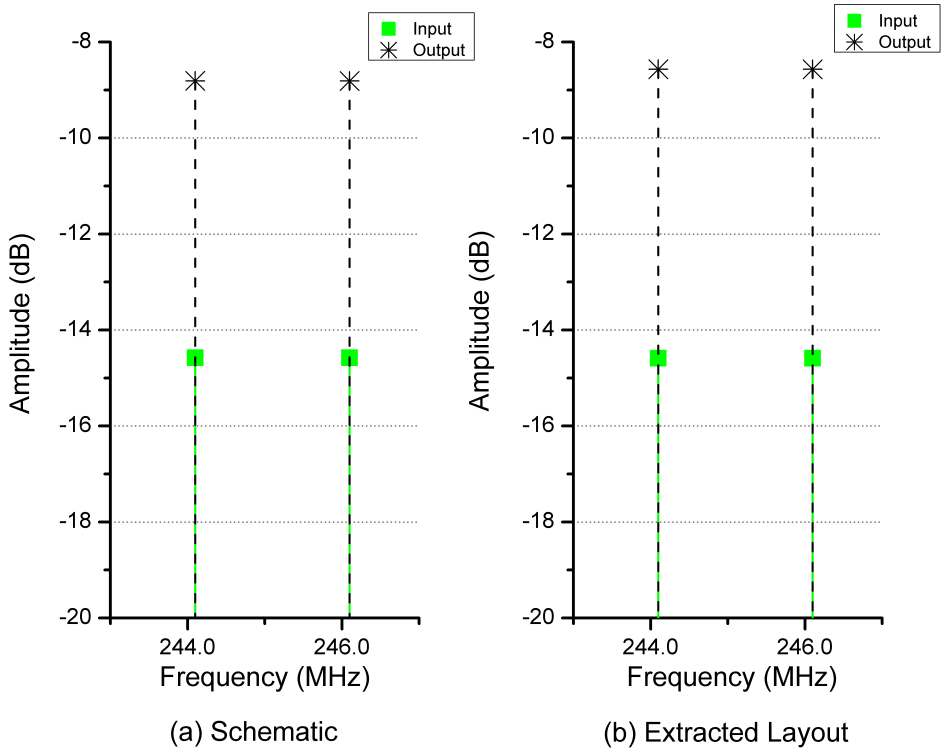


Figure 6.3: Simulated large-signal closed-loop gain of the charge amplifier MDAC.

Figure 6.3(a) and (b) show the large-signal closed-loop gain of the MDAC from schematic and extracted layout views respectively. Note that the large-signal gain of the MDAC from the extracted layout view is $0.252dB$ higher than that from schematic view. This is because the biasing current required for the amplifier (i.e., the MDAC) in layout design is 20% higher than that used in schematic, to reach a

Table 6.4: Linearity and large-signal gain of the MDAC for the first pipeline stage.

Specification	Design	
	Schematic	Extracted Layout
IM3 (dB)	53.19	47.89
THD (dB)	48.61	43.8
Large-signal gain (dB)	5.77	6.022
1st stage MDAC power (mW)	1.56	1.88

large-signal gain of 2, due to added parasitic capacitances (e.g., wire capacitances) in extracted layout view. Table 6.4 lists performance parameters like large-signal gain, IM3, THD and power consumption of the first stage charge amplifier MDAC, both from schematic and extracted layout views.

6.3.2 Pipeline First Stage Simulation

The first stage of the pipeline half-ADC has been simulated assuming the back-end to be ideal (i.e., zero quantization error). In this stage, the charge amplifier MDAC of Figure 4.18 has been used along with the coarse-ADC and the sub-DAC designed in [11]. In all simulations, we have used a digital gain of 2 to reconstruct the input signal in the digital domain, without doing any calibration. If the analog gain of the residue amplifier deviates from 2, there would be an error in the reconstructed signal. Thus, this gain error leads to non-linearities in the ADC transfer function. Please note that in extracted layout simulations, only layouts of the MDAC and the bias transistors are used. For the coarse-ADC and the sub-DAC, schematic views are used.

A two-tone test is conducted on the first stage of the pipeline ADC that is 1.5-bit/stage. The input amplitude used for the simulation is $1.5V$ p-p diff. Since the effective number of bits resolved from the first stage is 1, a gain of 2 is used in the first stage MDAC so that we get the same input dynamic range again (i.e., $1.5V$ p-p diff.), for the second stage of the pipeline ADC. Figure 6.4(a) and (b) shows the input and the output signal amplitudes of the first pipeline stage from schematic and

extracted layout views, respectively. We can see from the figure that the input and the output signal amplitudes are almost equal (as expected), since the gain of the amplifier is approximately 2. Please note that the biasing current of the amplifier in layout design is higher than that in schematic, to achieve the same gain of 2. This is due to the extra parasitic capacitances in extracted layout view, as explained in Section 6.1.

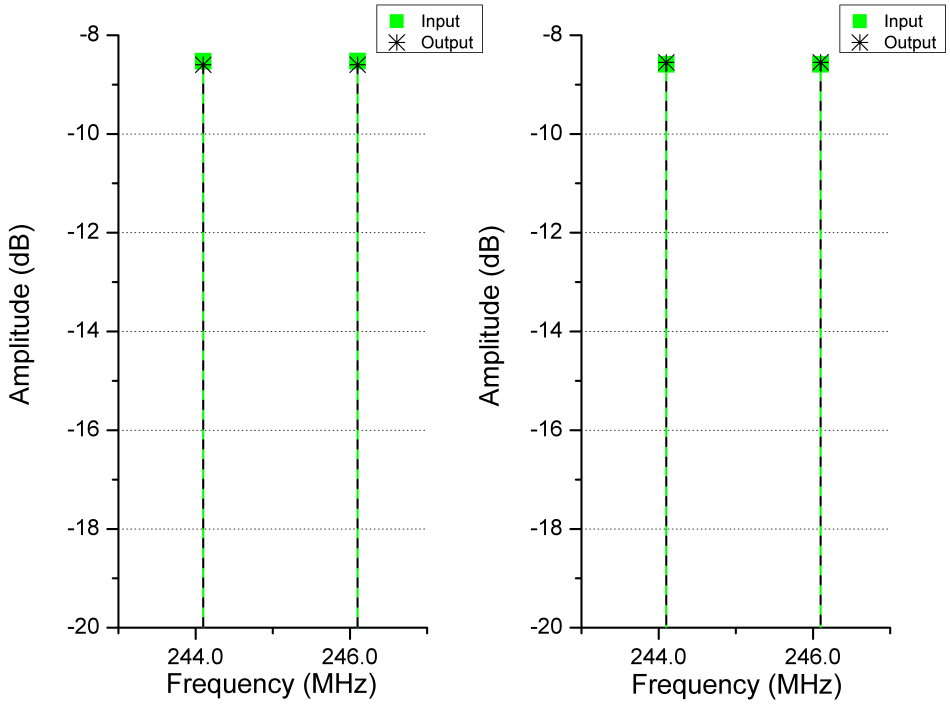


Figure 6.4: Simulated large-signal closed-loop gain of the first pipeline stage.

Figure 6.5(a) and (b) shows the two-tone simulation results of the first pipeline stage using schematic and layout views, respectively. From Figure 6.5(b), we can see that the IM3 tones for the extracted layout view are much below ($17.3dB$) compared to the other output intermodulation tones. This might be due to a cancellation of odd order non-linearities along with the even order ones. Based on our conjecture, it can be explicated as follows. Arguably, the distortion mechanism in an amplifier can be split into two parts. First is the voltage to current ($V - I$) transfer of an amplifier, which has an expanding behavior for the proposed class-AB am-

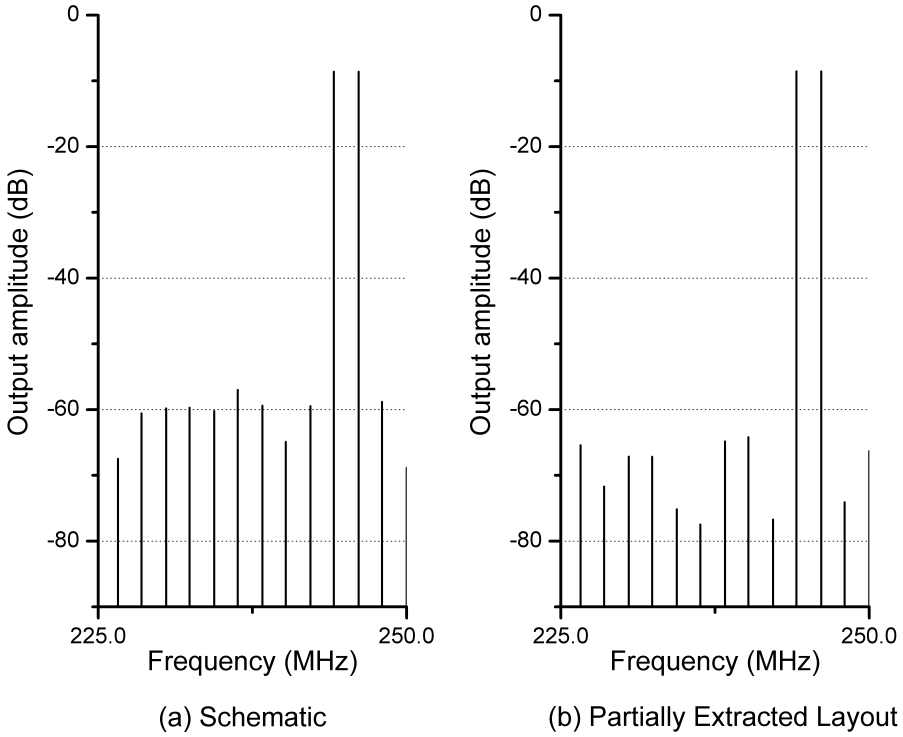


Figure 6.5: Two-tone simulation results of the first pipeline ADC stage.

plifier of Figure 4.7. This expanding behavior of the $V - I$ relationship has been shown in Figure 3.15(a). The second distortion mechanism might come from the reduction in output resistances of the MOS transistors (i.e., the reduction in $A\beta$ of the amplifier). This occurs when the signal amplitude at the output of the proposed class-AB amplifier increases and pushes the MOS transistors out of the saturation region. This distortion mechanism might have a compressing behavior, which can be compensated by the distortion resulting from the expanding $V - I$ transfer of the amplifier. However, the amount of this compensation arguably depends not only on the output signal swing of the amplifier, but also on the coefficients of the expanding and compressing transfers, which requires further investigation.

Another reason for a better linearity of the first pipeline stage in extracted layout view is because the large-signal gain of the MDAC is closer to 2 in extracted layout view than that in schematic view. The reason for this is the following: we have increased the biasing current of the amplifier in extracted layout view more than

Table 6.5: Linearity and large-signal gain for the first stage of the pipeline half-ADC.

Specification	Design	
	Schematic	Partially Extracted Layout
IM3 (dB)	50.86	68.16
THD (dB)	40.29	45.03
Input amplitude (each tone, dB)	-8.589	-8.589
Output amplitude (each tone, dB)	-8.599	-8.55
1st stage MDAC power (mW)	1.56	1.88

that in schematic view, to overcome (or compensate) the effects of the extra parasitic capacitances and get a gain of 2. While doing so, the biasing current of the amplifier becomes such that the gain of the amplifier (i.e., the MDAC) precisely matches with 2. We can also precisely make the gain of the amplifier 2 for schematic view, by fine tuning the biasing current. However, since the gain of the amplifier is almost 2 in schematic view and later on, we will be using digital calibration to calibrate for the gain and higher order non-linearities of the amplifier, we have not done the fine tuning of the biasing current to make the gain=2 in our schematic design. As a result, the analog gain of the amplifier better matches with the digital gain of 2 in the extracted layout view compared to that in schematic view and hence, the transfer function of the pipeline first stage is more linear in extracted layout view for our design. Table 6.5 lists all the simulation results of the first pipeline stage that have been discussed in this section.

6.4 FOM Calculation

To compare the performance of different ADCs, various Figures-of-Merit [26] are used. In this section, we calculate the Figure-of-Merit of our pipeline ADC from the simulation results, and compare it with state-of-the-art ADC designs. The following is a popular ADC Figure-of-Merit [12] that has been used in our design:

$$FOM_1 = \frac{Power}{2^{ENOB} \times Minimum(2f_{sig}, f_s)} \tag{6.1}$$

where the minimum of the signal frequency (f_{sig}) or the Nyquist frequency ($\frac{f_s}{2}$) is considered. This FOM_1 captures the trade-off between the speed and the power correctly. It also predicts that each additional bit in resolution can be achieved by doubling the power consumption. However, when the circuit is only limited by thermal noise, an increase by 1 bit of the ENOB comes at the cost of fourfold increase in power. Therefore, to capture the trade-off between ENOB and power, the following figure of merit can be used:

$$FOM_2 = \frac{Power}{2^{2ENOB} \times Minimum(2f_{sig}, f_s)} \tag{6.2}$$

Table 6.6 shows the calculation of the Figures-of-Merit for our pipeline ADC design. In this calculation, we have assumed that only the SNR contributes to the ENOB. This assumption is valid since our design is assisted by a digital calibration, and thus any non-linearity will be calibrated out in the digital domain. Please note that although Figures-of-Merit are calculated from the pipeline half-ADC, it should be the same for the whole pipeline ADC.

Table 6.6: FOM calculation of the pipeline ADC

Specification	Design	
	Schematic	Extracted layout
SNR (dB)	67	66.6
Total Power (half-ADC)	5.944	7.064
Signal bandwidth (MHz)	250	250
FOM_1 (fJ/conv)	6.52	8.08
FOM_2 (fJ/conv)	3.57×10^{-3}	4.62×10^{-3}

The calculated Figure-of-Merit is compared with state-of-the-art ADC measurement results, by using the survey done in [27]. Please note that we have only implemented and simulated the first stage of the pipeline half-ADC and from there, we

have estimated the FOMs. Moreover, in FOMs calculations, we have excluded the power dissipation from the digital calibration, reference buffers, clock drivers etc. Therefore, the comparisons that we have made in this section are not completely fair and display an optimistic result for our design.

In the first comparison, energy of an ADC is plotted with respect to SNDR, which is shown in Figure 6.6 (energy plot [27]). The lines labeled as FOM=10/100-fJ/conv-step in the figure are corresponding to FOM_1 at the respective energy/conversion-step value. Since our design is only limited by thermal noise, SNDR is equal to SNR. The energy plot plot shows the energy efficiency of an ADC design. The red circle on Figure 6.6 represents the performance of our pipeline ADC design from the extracted layout view. In particular, it has been able to reduce the energy to 14.12pJ, while achieving a SNDR (i.e., SNR) of 66.6dB (i.e., 10.77-bits).

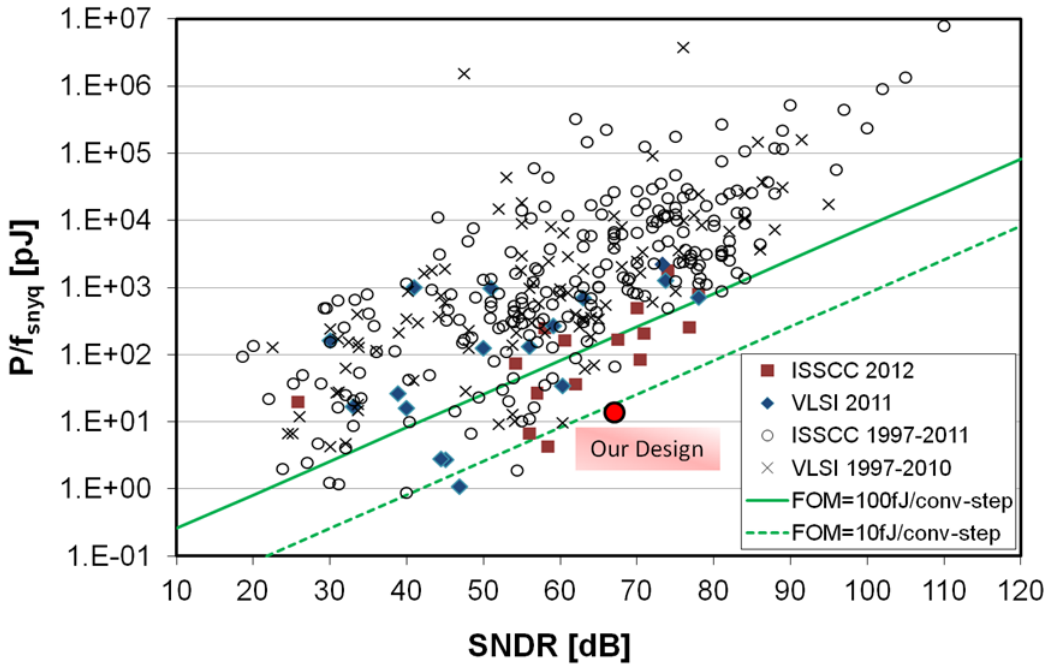


Figure 6.6: Energy plot of ADCs with respect to SNDR [27].

The second comparison is to show how efficient an ADC is in achieving high speed-resolution product. This plot is shown in Figure 6.7, where the speed of an ADC is plotted against its resolution (aperture plot [27]). The red circle on the plot represents our design in extracted layout view, which displays a bandwidth of

$250MHz$ at a SNDR (i.e., SNR) of $66.6dB$. Please note that in the aperture plot, the performance lines representing jitter of 0.1ps-rms/1ps-rms are for a fictitious sampler that only has the specified jitter numbers (i.e., no other nonidealities, such as quantization noise). There are actually very few ADC designs that can achieve high speed-resolution product and high energy efficiency at the same time. From Figures 6.6 and 6.7, we can see that our pipeline ADC design performs well in both the plots and achieves an excellent speed-resolution product together with a high energy efficiency.

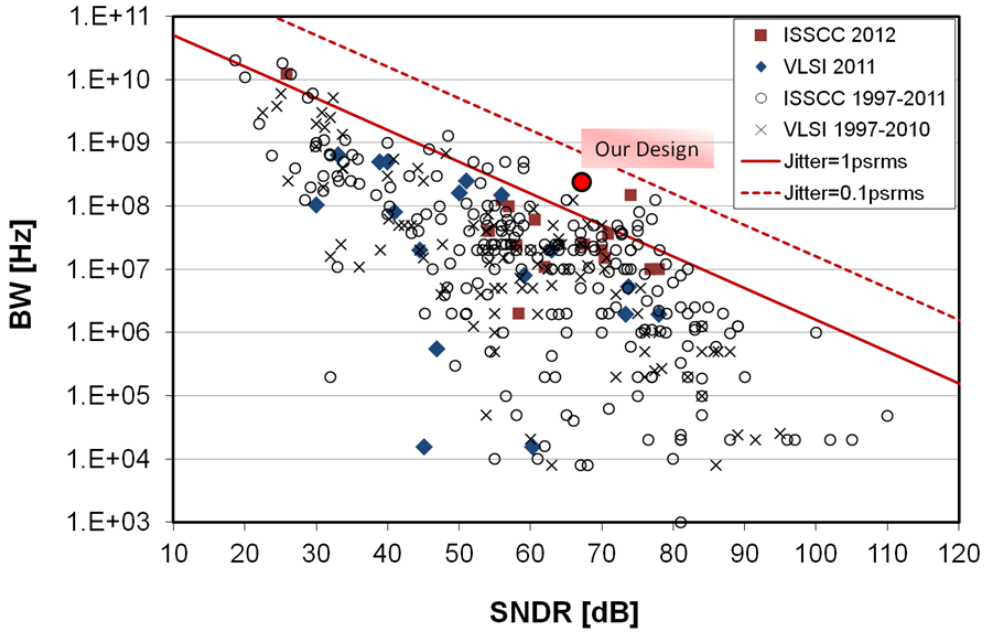


Figure 6.7: Aperture plot of ADCs with respect to SNDR [27].

Figure 6.8 shows the last comparison of the ADCs [27] that capture the effect of increasing the Nyquist sampling rate (f_{snyq}) on the FOM_1. From the trend of Figure 6.8, we can see that FOM_1 degrades at a higher f_{snyq}. Although the pipeline ADC of our design operates at $f_{snyq} = 500MHz$, it achieves an excellent FOM_1 of 8.08fJ/conv from extracted layout view, which is represented by the red circle on Figure 6.8. Please note that for our design, the f_{snyq} is equal to the sampling frequency (f_s), which is $500MHz$.

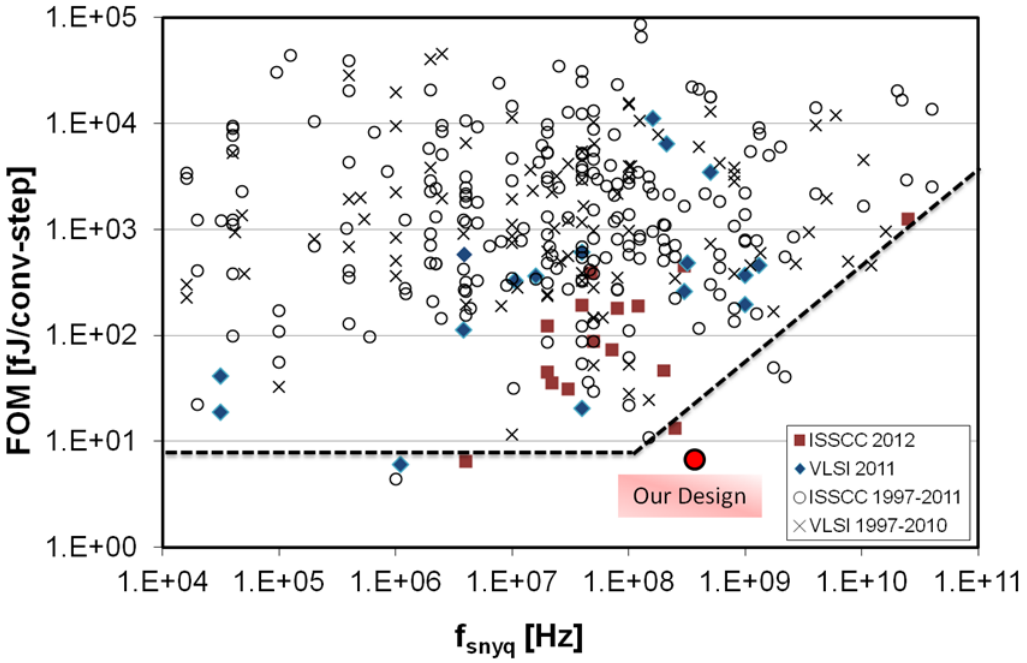


Figure 6.8: FOM_1 as a function of the Nyquist sampling rate (f_{snyq}) [27].

6.5 Summary

The linearity behavior of the fully differential charge amplifier MDAC and the first stage of the pipeline half-ADC have been shown in this chapter. For all the simulations, both schematic view and extracted layout view of the MDAC have been used. Thermal noise distribution among the pipeline stages are shown together with large-signal noise simulation results of the first stage MDAC. The power consumption of the first stage MDAC has also been simulated in large-signal, and from that, the total power consumption of the pipeline half-ADC has been estimated. Finally, the Figures-of-Merit of our pipeline ADC are calculated and compared with state-of-the-art ADC measurement results. From those comparisons, we have concluded that our simulated pipeline ADC design achieves an excellent performance in all aspects such as high energy efficiency, high speed-resolution product.

Chapter 7

Conclusion

7.1 Summary

In this dissertation, a low-power class-AB residue amplifier was designed for a 12-bit 500Msamples/s pipeline ADC. The main objective of this thesis was to reduce the power consumption of the residue amplifier. During the design, an ideal digital calibration was used to shift the linearity requirement of the residue amplifier to the digital domain. Since a high loop gain was not required to suppress the non-linearities of the amplifier, a simple amplifier topology was chosen that could give better speed and noise performance. As a result, the power consumption of the residue amplifier as well as of the whole pipeline ADC was reduced.

We did a detail review of various MDAC and residue amplifier topologies for the pipeline ADC. To achieve better power efficiency, we took a very simple class-AB amplifier with ideal voltages acting as level shifters and compared it with a simple class-A amplifier. The simulation results showed excellent performance for the class-AB amplifier in gain, bandwidth, linearity, noise and power consumption over the class-A amplifier.

In order to replace the ideal voltage source level shifters, we introduced capacitors with switches at the initial stage of the design. However, this approach had an adverse effect on the gain and bandwidth, and also introduced extra noise components for the class-AB amplifier. To resolve this problem, we proposed a new class-AB amplifier topology that removed all level shifting capacitors and applied bias voltages directly to the gate of the MOS transistors. The proposed class-AB

amplifier was simulated and compared with other class-AB amplifiers. From the simulation results, we concluded that the proposed class-AB amplifier topology performed similar to the class-AB amplifier with the ideal voltage source level shifters.

Among the MDACs, two closed-loop MDAC topologies, namely the flip-around MDAC and charge amplifier MDAC, were analytically compared to show their relative advantages to each other. From the comparison, we observed that the flip-around MDAC topology achieved a higher SNR and a higher feedback factor compared to the charge amplifier MDAC topology. However, this relative advantage of the flip-around MDAC topology reduced, as the $\frac{C_s}{C_f}$ ratio increased. Due to finite speed and accuracy of the proposed class-AB residue amplifier, the residue output signal of the flip-around MDAC topology became distorted. This was especially due to the different behavior of the path of the input signal and that of the sub-DAC (or reference) signal. Furthermore, in our design we used a capacitor ratio of 4 in order to reach a large-signal closed-loop gain of 2 because of insufficient $A\beta$ and f_{-3dB} of the residue amplifier. As a result, the relative advantages of the flip-around MDAC topology became less compared to the charge amplifier MDAC topology. Therefore, we finally implemented a fully differential charge amplifier MDAC for the design of our pipeline ADC.

We scaled down the capacitors of pipeline stages only twice to reduce power dissipation, similar to that in [11]. To achieve the same goal (i.e., power reduction), no dedicated sample and hold circuit was used at the front of the pipeline ADC. As a result, the pipeline ADC architecture became sensitive to aperture error. To reduce this error, sampling moments of the first stage MDAC and the coarse-ADC were made the same, like in [11]. However, due to an incomplete settling of the residue amplifier, the rest of the pipeline stages also require the same sampling moments for the MDACs and the coarse-ADCs to avoid any aperture error. We also introduced reset switches to remove the previous sample memories (i.e., intersymbol interference) from the sampling capacitors. Therefore, the whole timing scheme of the pipeline ADC was redesigned.

Only the first stage of the pipeline half-ADC was implemented and simulated in this dissertation, assuming a back-end processor of infinite resolution. The fully differential charge amplifier MDAC was designed and laid out in 40nm CMOS technology, and the coarse-ADC and the sub-DAC were reused from [11]. Simulations

were performed on both schematic and extracted layout views to observe the different performance parameters, such as large signal gain, linearity, noise and power consumption.

From the simulation results of the first pipeline stage, we calculated the SNR of the pipeline half-ADC, which was 66.6dB for extracted layout view at a full-scale input of 1.5V p-p diff. Since a digital calibration was assumed to correct the non-linearities of the pipeline ADC, the design became limited only by thermal noise (i.e., SNDR=SNR). From the simulated total power consumption of the pipeline first stage, we estimated the total power consumption of the pipeline half-ADC, which was 7.064mW in extracted layout view, resulting in a FOM of 8.08fJ/conv at a sampling frequency of 500MHz. The simulation results of our design from extracted layout view was compared with the simulation results of the previous work [11]. Compare to [11], where the FOM_1 was 300fJ/conv, our design achieved 37.12$\times$ better FOM_1.

It is worth noticing that the approach presented in [11] achieved FOM_1 of 300fJ/conv without any digital calibration, and it only used calibration to improve the power efficiency of the design in a latter stage. However, without any calibration, [11] achieved a THD of 50dB with a full scale input of 0.8V p-p diff at 500MHz sampling frequency, whereas in our design, the pipeline first stage achieved a THD of 45.03dB with a much higher full scale input of 1.5V p-p diff. Therefore, the difference in linearity performance between the approach in [11] and our design, without doing any calibration, is not significant, despite the fact that the amplifier used in [11] has approximately 43dB higher $A\beta$ than that of the class-AB amplifier of our design. This indicates that the proposed class-AB amplifier of our design is inherently more linear than the class-A amplifier designed in [11]. The simulation results of our design from extracted layout view were also compared with the measurement results of state-of-the-art ADCs. We observed from those comparisons that the designed pipeline ADC displayed a high energy efficiency (i.e., 14.12pJ) along with a high speed-resolution product (i.e., bandwidth of 250MHz at a SNR of 66.6dB).

Thesis Contributions

To sum up, we identify the following primary contributions from this work:

Residue Amplifier The designed class-AB residue amplifier indeed achieved a low-power ($1.88mW$) consumption. The proposed class-AB amplifier topology did not include any level shifting capacitors and thus, removed their associated problems, as discussed in Section 4.1. Compared to the amplifier designed in [11], it consumes $11.9\times$ lower power. However, there was not a significant class-AB amplifier behavior (i.e., drive current is only 5.4% higher than the quiescent current) that contributed towards this low-power consumption. Instead, the key advantages that made our proposed class-AB amplifier more power efficient are listed as follows:

- *High Signal Swing*: The proposed amplifier only consists of a NMOS and a PMOS transistor, thus provides more headroom for signal swing. In particular, the amplifier allowed for a relatively large full-scale input swing of 1.5V p-p diff at a 1V supply. This improves the SNR achieved by the amplifier.
- *No excess Noise*: Both the NMOS and PMOS transistors contribute to the signal gain and therefore, there is no excess noise. This results in a higher SNR, e.g., $3dB$ compared to the class-A amplifier (Section 3.3.3).
- *Current Reuse*: Same biasing current flows though the NMOS and PMOS transistors. As a result, we get a higher effective transconductance for the same biasing current, thus increasing the speed of the amplifier along with making it more power efficient.
- *Better Linearity*: The class-AB amplifier is inherently more linear than the class-A amplifier because it can suppress even order non-linearities better. IM3 comparison showed a $26.21dB$ better performance for the class-AB amplifier compared to the class-A amplifier (Section 3.3.3).

MDAC Design Insufficient accuracy (i.e., finite $A\beta$ and f_{-3dB}) of the proposed class-AB amplifier resulted in many problems, when used with the flip-around MDAC topology. In order to resolve those problems, we replaced the flip-around MDAC with a charge amplifier MDAC topology (Chapter 4).

Modification of Timing Scheme Making use of incomplete settling to save power in the amplifier showed different timing related problems and ISI for the pipeline ADC. We proposed a new timing scheme for the pipeline ADC and presented a solution for the ISI (Chapter 5).

7.2 Future Work

Although the primary goal of this thesis was achieved, there were several limitations that we would like to improve in future. This section addresses these limitations and discusses some design recommendations, which are as follows:

- In this dissertation, only the first stage of the pipeline half-ADC was fully-implemented and simulated, considering an ideal back-end pipeline ADC of infinite resolution. The performance of the pipeline ADC was estimated from the extracted layout simulation results of the first stage. Therefore, we have to implement the other stages to build the complete pipeline ADC. In this thesis, an ideal clock generator was used with a modified timing scheme compared to that in [11], and thus we need to re-design and implement the clock generator. Moreover, we have to fully implement other circuit blocks such as biasing circuit, references.
- In this research, we narrowed down our focus to design a power-efficient residue amplifier, and thus used an ideal digital calibration scheme, due to limitation of time. Please note that our pipeline ADC was intended to be used with split-ADC digital calibration, which was implemented in [11] in MATLAB software. Therefore, the split-ADC digital calibration needs to be realized in hardware (i.e., on chip).
- During the reset phase, the input and output terminals of the amplifier were connected to the common-mode voltages and a biasing current flowed through the amplifier. Since the amplifier only operated during the amplification phase, the power spent during the reset time was a complete waste. Moreover, the duration of the amplification phase was much shorter than the reset time of the amplifier, due to the reasons mentioned in Section 5.2. Therefore, in order to save power during the reset phase of the amplifier, it should be

turned off. While doing so, we have to keep some non-overlapping time, between the turning on of the amplifier again and the start of the amplification phase. This is because an amplifier requires some time to start-up and reset its nodes to the desired common-mode voltages.

- The proposed class-AB residue amplifier had a pseudo-differential topology, and thus did not provide any CMRR. As there are a cascade of residue amplifiers in the signal path of a pipeline ADC, any small common mode error at some point in the pipeline chain will be amplified and becomes a much bigger error by the time it reaches the last stage. To prevent this from happening, the common mode gain of the amplifier should be reduced by using circuit techniques, such as applying a small amount of differential positive feedback by cross-coupling the amplifier's feedback capacitors, as shown in [28].
- In Section 6.3.2, we saw that the expanding $V - I$ transfer characteristics of the proposed class-AB residue amplifier compensated the distortion resulting from the compressing transfer characteristics, such as reduction in output resistances of the transistors with the increased output signal swing. This compensation mechanism improved the linearity performance of our proposed class-AB residue amplifier. However, the amount of the compensation depends on the co-efficients, characterizing those transfer functions, which should be investigated.
- Update the FOM with inclusion of the power of the digital calibration, reference buffers, clock drivers etc. It is clear that at this point we can only make estimates, but if more work is done we can include those numbers.

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Appendix A

Biasing Circuit

The biasing circuit used to generate the gate voltages (i.e., ($V_{cm} + V_{LS1}$) and ($V_{cm} + V_{LS2}$)) of the MOS transistors (of Figure 4.7) is shown in Figure A.1.

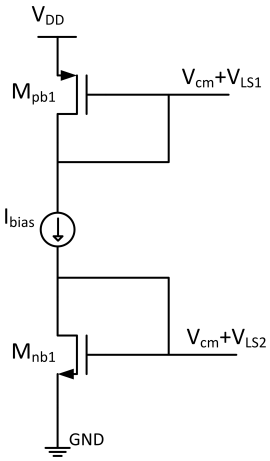

Figure A.1: Biasing circuit used for the proposed class-AB amplifier of Figure 4.7.